MODELING AND DIGITAL CONTROL OF HIGH FREQUENCY DC-DC POWER CONVERTERS

by

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ABSTRACT

The power requirements for leading edge digital integrated circuits have become increasingly demanding. Power converter systems must be faster, more flexible, more precisely controllable and easily monitored. Meanwhile, in addition to control process, the new functions such as power sequencing, communication with other systems, voltage dynamic programming, load line specifications, phase current balance, protection, power status monitoring and system diagnosis are going into today's power supply systems. Digital controllers, compared with analog controllers, are in a favorable position to provide basic feedback control as well as those power management functions with lower cost and great flexibility.

The dissertation gives an overview of digital controlled power supply systems by comparing with conventional analog controlled power systems in term of system architecture, modeling methods, and design approaches. In addition, digital power management, as one of the most valuable and "cheap" function, is introduced in Chapter 2. Based on a leading-edge digital controller product, Chapter 3 focuses on digital PID compensator design methodologies, design issues, and optimization and development of digital controlled single-phase point-of-load (POL) dc-dc converter.

Nonlinear control is another valuable advantage of digital controllers over analog controllers. Based on the modeling of an isolated half-bridge dc-dc converter, a nonlinear control method is proposed in Chapter 4. Nonlinear adaptive PID compensation scheme is implemented based on digital controller Si8250. The variable PID coefficient during transients improves power system's transient response and thus output capacitance can be reduced to save cost. In

Chapter 5, another nonlinear compensation algorithm is proposed for asymmetric flyback-forward half bridge dc-dc converter to reduce the system loop gain's dependence on the input voltage, and improve the system's dynamic response at high input line.

In Chapter 6, a unified pulse width modulation (PWM) scheme is proposed to extend the duty-cycle-shift (DCS) control, where PWM pattern is adaptively generated according to the input voltage level, such that the power converter's voltage stress are reduced and efficiency is improved. With the great flexibility of digital PWM modulation offered by the digital controller Si8250, the proposed control scheme is implemented and verified.

Conclusion of the dissertation work and suggestions for future work in related directions are given in final Chapter.

This document is dedicated to my parents.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 Background and Motivations

The advances and explosion in VLSI technologies for the past thirty years impose new challenges for delivering high-quality power to processors. As transistor lithography drops dramatically below the 0.1um level, Moore's Law promises sufficient transistor density and speed extremely increased. The power requirements for leading edge processors and ASICs have become increasingly demanding. Power converter system must be faster, more flexible, more precisely controllable and easily monitored. Meanwhile, in addition to control process, the new functions such as power sequencing, VID programming, load line specifications, phase current balance, protection and power status monitoring involve more and more to power system [A1].

This proceeding toward increased speed and performance is taxing the limits of today's power systems. Power architecture is needed to meet higher requirements, more functionality and new challenges while delivering high performance, fast time-to-market, and scalability. This demand from the controller and the continuing advance of digital technology has pushed many power manufactures to look at digital power control.

The relatively early application of digital power control is motor control [A2]. However, for high-frequency switching power converters used in computing and telecom power systems, digital power faces new challenges and need to raise new functionalities and solutions for more demanding power requirements. The digital control for dc-dc converters has been becoming a

hotspot in both industry and academia in the past 4 years. It was expected that the revenue of digital power reach $1 billion in the year of 2010, which includes the products of both digital power management and digital power loop control.

"Digital Power" is defined as digitally controlled power products that provide configuration, monitoring, and supervisory functions, even extended to fully digital loop control. It is important to note that "digital power" really includes two different areas of power technologies. One is "digital control", the real-time, cycle-by-cycle control of power switches. The other area is "digital power management" [A3]. Figure 1-1 is showing a multi-POL power management system with PMBus protocol, which is based on physical transport layer SMBus. In the system, each POL is controlled under its own digital loop. The system host manages multiple POLs through the series SMbus. The power management may include switching frequency adjustment, sequencing, voltage margining, voltage/current/temperature monitoring and protection etc.

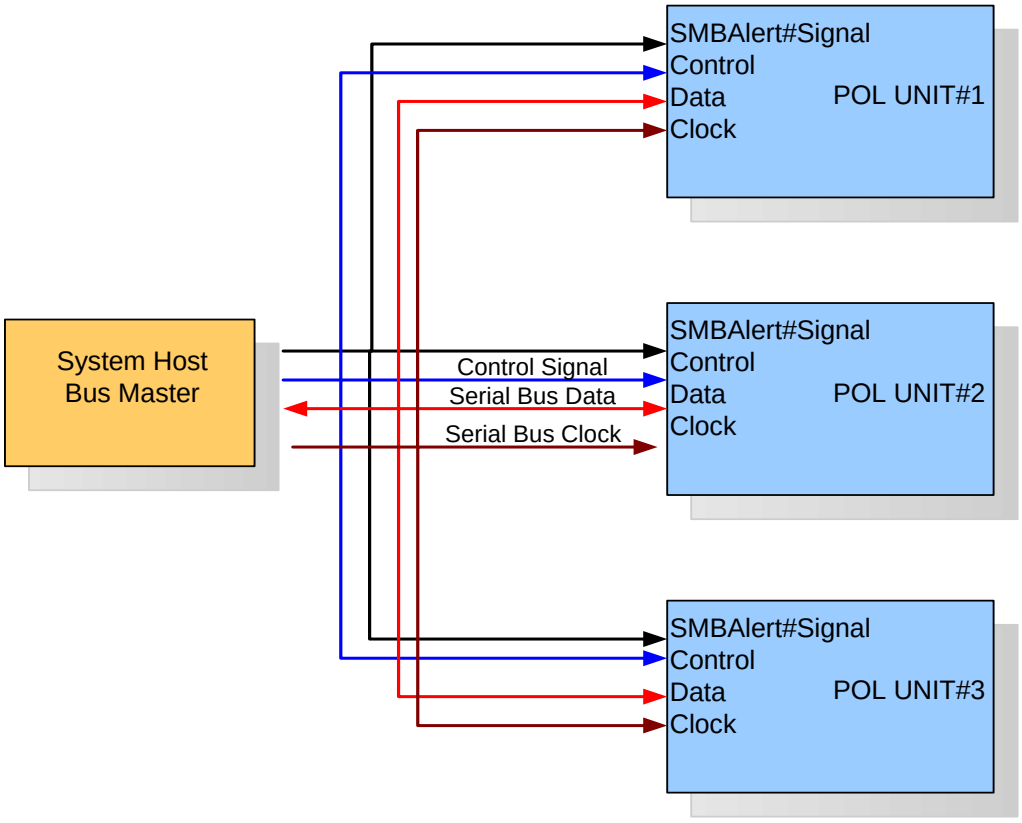


Figure 1-1 Digital power management with PMBus

Form power converter designer's perspectives, digital controllers have many advantages over their analog counterparts. An analog controller needs a number of passive components and occupies large footprint. The values of those analog components are sensitive to temperature. Those sensitivity and aging effect limits the mass-production of products. Compared with the analog controller, digital controllers provides easy of integration and improves system reliability. Since only a few components are needed, digital controlled system is less sensitive to components tolerance, and the Mean Time Between Failures (MTBF) can be reduced. One of the most important benefits digital controllers provide is the flexibility. By utilizing the program

memory, sophisticated control and monitoring schemes can be built in digital control systems. For example, the control functionality and parameters can be changed to meet the new requirements, which results in less design and development time - faster time-to-market [A4].

Fundamentally, digital architectures differ from analog ones in the fact that digital controllers use AD converters to digitize current and voltage information, and complete the compensation and regulation based on programmable digital filters techniques. Additionally, digital architectures utilize some forms of program memory, which not only allows for more sophisticated monitoring and control schemes such as nonlinear control, but also adds a software graphical user interface (GUI) as a design tool to simplify the system design. These GUIs are used in the design phase to configure the digital controller for specific design parameters and reduce the product development time. Moreover, digital processes tend to exist in smaller geometries, offering lower-cost solutions where there is a high degree of circuit function integration.

The use of software to change the controller functionality makes a system based on a digital controller very flexible. The digital controller offers the ability to add, eliminate or change any parameter in the system in order to meet new requirements, or to optimize and calibrate the system. For example, the same POL (Point of Load) can be programmed to meet different design specifications allowing the supplier to have a single module that meets several design points. It also offers the capability to integrate and cascade multiple systems together because of the ease of integrating communication capability into the digital controller. For example, where multiple POL boards are used, the need of current sharing can be implemented through a standard communication bus without the need for any hardware additions.

Systems based on digital controllers require fewer components, which decreases the mean time before failure (MTBF) of the system. For example, all the components for the feedback loop are eliminated along with the "select at test" and "select according to design specification" components. The added capability of monitoring protection and prevention also increases the system reliability. For instance, an engineer can choose to monitor the system temperature to decrease the current limit level, or turn on a fan. This scenario decreases the stress on the power components and fans.

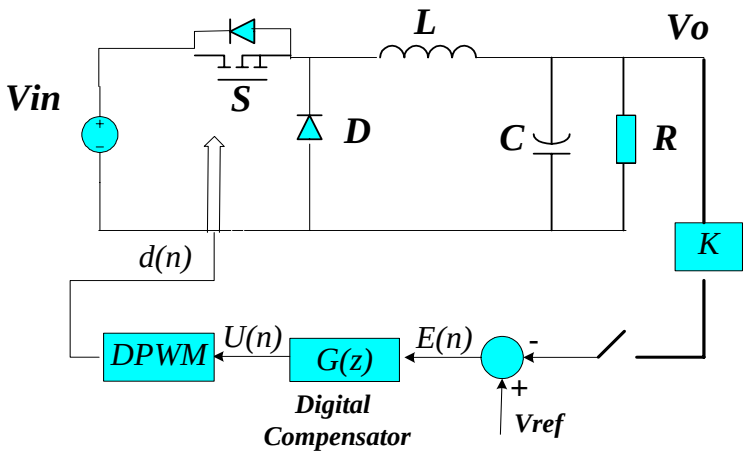


Figure 1-2 Typical digital controlled switching power converter

A typical digital controlled switching power converter is shown in Figure 1-2. Compared with analog controller, DPWM in the digital controller performs the same function of drive signal generation as the analog counterpart, but it does so by "calculating" and "timing" the desired duration of ON and OFF periods of its output signal. By contrast, an analog PWM usually operates by triggering ON at a clock transition and triggering OFF when a fixed voltage

"ramp" reaches a pre-set trip voltage. In addition, unlike analog controller, the digital system compensation is conducted under "clock" in discrete domain. Those differences offer digital controlled system some advantages and but also challenges.

The digital compensation is typically implemented with PI or PID style subsystem, which translates a digital representation of output voltage into duty-cycle information fed to DPWM block. PID controller adjusts the output voltage on a programmable reference by adjusting pulse width, in real-time, to provide output voltage regulation. The PID compensator is required to compensate for gain and phase-shift factors around the control loop to achieve desirable performance as in the analog controller. In digital controlled systems, there is additional phase shift arising from time delays in processing the digital data. The major gain and phase-shift factors in an analog system are considered when designing a digital controlled system, taking into consideration the time delay from AD conversion and other delay factors.

AD converter converters analog output voltage to digital data. Each binary "word", containing upwards of N bits of data, is sent to the PID control law processor at a high clock rate. Analog control provides very fine resolution for output voltage adjustment. In principle, an output voltage can be regulated close to any programmed reference, and the precision is only limited by the steady-state error, thermal effects and system noise. On the other hand, a digital control loop has a finite set of discrete "set points" resulting from the resolution of "quantizing elements" in the system.

The usual digital compensator design methods include *direct digital design* and d*igital redesign* approaches. For *direct design* approach, a discrete model of switching power converter that includes sampled analog components is first constructed; then, the compensator design is directly conducted in discrete Z-domain.

Digital redesign assumes the sampling frequency is much greater than the system crossover frequency, so the design equivalent approach is accurate. First a linear model of a switching power converter is established based on some assumptions such as low-frequency small-signal disturbance. Based on the liner model, the controller design is done in S domain. Finally, the design of analog compensator is mapped into Z domain to complete the digital controller design.

It has been known that, to design a converter system incorporating feedback control loop to meet the specification, the dynamic model of the switching converter is needed. The purpose of the model is to analyze and design the power system to meet the requirements. From the feedback design perspective, it is desired to design a feedback system, such that the output voltage is precisely regulated, and the output is insensitive to disturbances from input voltage and load. For a digital controlled power converter, the modeling of the power stage is as important as in analog controlled power systems.

The coming question is how we could implement a digital controller? As we know, power electronics systems themselves are typically a complex combination of linear, nonlinear and switching elements. High-frequency converters add another dimension of complexity because of their fast dynamics. Real-time power electronics systems, therefore, demand the use of high-speed data acquisition and control. Unlike analog control, digital control introduces latency due to feedback parameter quantization and calculation times. To minimize these delays, digital control functional blocks are characterized by high data throughput and low latency, in particular the loop compensation and DPWM modulation algorithms. While various implementations have been reported, the most common digital controller implementations can be

grouped into three major types: programmable signal processor (typically a digital signal processor (DSP)), custom hardware, or some combination of both [A5].

The DSP executes discrete time calculations of control variable values in real time. Some suppliers offer DSPs with Flash memory allowing the user to address multiple system topologies and control strategies with a common processor platform. However, this approach is limited by DSP throughput, which, in turn, is limited by the DSP clock frequency and memory resources. These factors adversely impact cost, size, supply current and scalability at higher DPWM frequencies.

The dedicated hardware-based approach uses fixed architecture state machines to execute the control algorithm. Hardware can be optimized for cost and performance making this a potentially lower-cost and more efficient approach than the DSP. However, this approach lacks flexibility because the control hardware cannot be significantly changed once fabricated. Therefore, the hardware must be designed for a specific end application, which adversely impacts non-recurring engineering cost and time-to-market and increases design risk.

The other digital controller implementation type is IC device combined the hardware controlling and microprocessor management functions, so extracted maximum benefit from each. For instance, Silabs' Si8250 is a mixed-signal device partitioned into a hardware digital controller comprised of a digital signal processor (DSP) controller and an instruction based microcontroller (MCU) system management processor section.

Digital power provides and additional functionality and extreme flexibility to the power converter systems. However, there are several issues needed to be carefully considered when designing a digitally controlled power converter system. These issues include digital compensator design, resolution of ADC and DPWM, and quantization and limit word length

effect of digital coefficients. Unlike analog controllers in power converters, the digital controlled system is pretty probably affected by ADC's performance. A complete analog controlled power system could be simpler and cheaper than a high-speed and high-resolution ADC. Therefore, the cost and performance of an ADC conflict with each other. Moreover, available microcontrollers or DSPs are now still too slow and too costly for the power converter applications. A high speed and high resolution of DPWM is also too costly for the power application. Furthermore, digital controller increases the complexity of the system due to ADC and digital processing and need more software knowledge for power designers. With advance of technology, the issues mentioned above could be resolved in the near future. Without doubt, digital control is a trend in power converter applications.

1.2 Dissertation Outline and Major Results

The dissertation is organized into four parts and divided into eight chapters. Part I of the dissertation consists of Chapter 1 and 2, which introduce the fundamental of digital controlled power systems, review and compare analog and digital power systems, and modeling and design approaches for digital controlled power converters. Part II - chapter 3 focuses on the digital PID compensator design methodology, design issues, and optimization and development of digital controlled single-phase POL converter based on the digital controller Si8250. Part III consisting of chapters 4, 5 and 6 proposes two digital control schemes for half bridge dc-dc converter based on the DC and AC modeling of half bridge dc-dc converters. An adaptive nonlinear compensation algorithm is proposed for asymmetric half bridge dc-dc converter in Chapter 5, and a digital adaptive unified control scheme for half bridge converter is proposed to extend the

"duty cycle shift (DCS)" concept. Chapter 7 proposes control architecture of voltage regulation featuring fast transient response, which can be favorably implemented with digital control.

Chapter 2 first offers an overview of modeling techniques for power converters. Analog and digital controller design techniques are discussed, respectively. Particularly, digital control theory and design methodology are presented in this chapter. Digital management, as a part of digital power, is reviewed in the end o f Chapter 2.

Chapter 3 addresses the digital controller design challenges and presents digital control design approaches to reduce the design and development time. In the conventional redesign method, a controller designed in S domain is mapped to digital Z domain. However, the obtained PID coefficients in Z domain is hard to tune up due to power designers' limited knowledge in Z domain. Based on redesign method, Chapter 3 presents a design approach, which remaps the digital coefficients to continuous time domain, and thus optimizes digital coefficients directly in discrete domain. Due to limited resolution of ADC and DPWM, calculation error of digital coefficients and quantization effect, the performance of a digital controlled power system is degraded. Based on the constructed PID structure, those key issues are discussed in Chapter 3. A POL demo prototype is designed and developed with digital controller- combined MCU/hardware IC Si8250 based on the presented design approach. A nonlinear control algorithm trigged by large-signal output voltage transients is proposed and implemented on the POL prototype. The experimental result shows that digital controller is favorable in implementing advanced control techniques.

Chapter 4 investigates digital controlled high-frequency-switched half-bridge dc-dc converter in term of modeling, digital controller design and control system realization. First a unified average space-state model is established for the half-bridge dc-dc converter with current doubler

rectifier considering the parasitic DC parameters. Based on the dc model, a number of important issues of current doubler rectification in both symmetric and asymmetric HB dc-dc converters are presented. Based on the unified small signal model, a digital controller is designed to meet the converter system performance requirement with *digital redesign* method. This digital controller is implemented with Si8250. Experiment results and comparison of two digital controllers are also given.

Chapter 5 first investigates a new half-bridge flyback-forward converter topology. In this topology, a forward half-wave rectification is presented as the secondary rectifier associated with asymmetric half-bridge converter. Compared to the center-tapped rectification, the transformer secondary winding structures is simplified and better transformer window utilization is achieved. Compared to the current doubler rectification, only one inductor is used and the inductor utilization is improved. Meanwhile, the average small-signal model of an AHB flyback-forward converter is derived with the average state-space small signal modeling method. Based on the model, the nonlinear characteristics of this topology are investigated. A nonlinear adaptive control is proposed and implemented in the simulation to achieve a unified loop gain and system bandwidth under load and input voltage variations based on a digital PI compensation.

In Chapter 6, DCS (Duty Cycle Shift) PWM control concept is extended to a unified PWM control scheme, which is between asymmetric control and the original DCS control. Corresponding mathematical model is established to analyze a half bridge DC-DC converter under control of the proposed unified PWM scheme. With the digital controller Si8250, the implementation of the proposed scheme is easy to implement. By changing the coefficient of the control scheme, the control mode can adaptively slide from one mode to another. The digital

control offers this advanced control great flexibility. Experimental results show the performance improvement under control of extended DCS PWM scheme.

Chapter 7 gives a brief conclusion of the dissertation work and comes to suggestions for future work in related directions.

2 ANALOG AND DIGITAL CONTROLLED DC-DC CONVERTERS

2.1 Introduction

Regulated power converter system invariably requires feedback control. In a typical dc-dc converter application, the output voltage is regulated regardless of changes of input voltage or load. To design a converter system incorporating feedback control loop to meet the specification, we need to know how variations in the input voltage, the load current, or the duty cycle affect the output voltage. Mathematical model of the switching power converter is necessarily constructed to analyze and design a power converter system [B1, B2].

As of today, most feedback controllers for dc-dc converters are based on analog technique, where comparators and amplifiers and so on analog circuits are typically utilized to control a dc-dc converter. The switching frequency and compensator coefficients consist of resistors and capacitors, where the components values are sensitive to noise and temperature. As a result, the component tolerance and ambient temperature may affect mass production and system reliability. In addition, an analog system is inflexible in term of changing control parameters such as switching frequency and PID coefficients.

Digital controllers for switching power supplies offer a number of advantages including a reduction of the number of passive components, programmability, flexibility, implementation of more advanced control algorithms and reduced sensitivity to parameter variations. In addition, digital techniques ease the communication. Those techniques provide digital communication interface that allows a host or system level processor to control and monitor power converters.

This chapter will first discuss about modeling techniques of power converter since a mathematical model is the representation of a power converter. Analog and digital controlled dc-dc converters as well as the associated design techniques are also discussed, respectively. Analog controller design approaches has been mature for many years, in the other hand, digital controller design for dc-dc converter needs more research work since digital control of dc-dc conversion is a relatively new field. This chapter discusses the fundamental of digital modeling and design approaches. In the end, digital power management is also addressed in the chapter.

2.2 Modeling of High Frequency Switching DC-DC Converters

Modeling is the representation of physical circuits by mathematical means. For a power converter, it is desired to design a feedback system such that the output voltage is regulated accurately, and is insensitive to disturbances in input voltage or in the load current. In addition, the feedback system should be stable, and properties such as transient overshoot, settling time and steady-state regulation should meet specifications. To design a system with requirement like those, we need a dynamic AC model of the switching power converters [B1].

The basic concept to predict ac behavior is to average the converter waveforms over one switching cycle. Thereby the desired DC and low frequency AC components of waveforms are exposed. Since switching power converters are nonlinear systems, by perturbing and linearizing the average model about a quiescent operating point, small-signal linearized models could be constructed.

There are two well-known variants of ac modeling method, *state-space averaging*, and *circuit averaging*. *Averaged switch modeling* as an extension of circuit averaging is also used in many applications widely.

The *state-space averaging* technique generates the low-frequency small-signal ac equations of PWM dc-dc converters. Converter transfer functions and equivalent circuit models can be obtained. The converter contains independent state variables such as inductor currents and capacitor voltages, that form the state vector ***x(t)***, and the converter is driven by independent sources that form the input vector ***u***(*t*). The output vector ***y***(*t*) contains dependent signals of interest. During the first subinterval, when the switches are in position 1 for time *dT*s, the converter reduces to a linear circuit whose equations can be written in the following state-space form:

$$\begin{aligned} \frac{dx(t)}{dt} &= A_1 x(t) + B_1 u(t) \\ y(t) &= C_1 x(t) + E_1 u(t) \end{aligned} \qquad \text{2-1}$$

The matrices A_1, B_1, C_1 and E_1 describe the network connections during the first subinterval. The duty cycle *d*(*t*) may now be a time-varying quantity. During the second subinterval, the converter reduces to another linear circuit, whose state space equations are

$$\begin{aligned} \frac{dx(t)}{dt} &= A_2 x(t) + B_2 u(t) \\ y(t) &= C_2 x(t) + E_2 u(t) \end{aligned} \qquad \text{2-2}$$

The matrices A_2, B_2, C_2 and E_2 describe the network connections during the second subinterval, of length (1 – *d*)*T*s. It is assumed that the natural frequencies of the converter network are much smaller than the switching frequency. This assumption coincides with the small ripple approximation, and is usually satisfied in well-designed converters. It allows the high-frequency switching harmonics to be removed by an averaging process. In addition, the waveforms are linearized about a dc quiescent operating point. The converter waveforms are expressed as quiescent values plus small ac variations, as follows:

$$y(t) = Y + \hat{y}(t) \quad x(t) = X + \hat{x}(t) \quad u(t) = U + \hat{u}(t) \quad d(t) = D + \hat{d}(t) \qquad 2\text{-}3$$

This small-signal linearization is justified provided that

$$\|X\| \gg \|\hat{x}(t)\|, \|U\| \gg \|\hat{u}(t)\|, \|Y\| \gg \|\hat{y}(t)\|, D \gg \left|\hat{d}(t)\right| \qquad 2\text{-}4$$

where || ***X*** || represents the norm of vector ***x***.

The state-space averaged model that describes the quiescent converter waveforms is

$$\begin{aligned} 0 &= AX + BU \\ Y &= CX + EU \end{aligned} \qquad 2\text{-}5$$

where the averaged state matrices are

$$
\begin{aligned}
A &= DA_1 + (1-D)A_2 \\
B &= DB_1 + (1-D)B_2 \\
C &= DC_1 + (1-D)C_2 \\
E &= DE_1 + (1-D)E_2
\end{aligned}
\qquad \text{2-6}
$$

The steady-state solution of the converter is

$$
\begin{aligned}
X &= -A^{-1}BU \\
Y &= (-CA^{-1}B + E)U
\end{aligned}
\qquad \text{2-7}
$$

The state equations of the small-signal ac model are

$$
\begin{aligned}
\frac{d\hat{x}(t)}{dt} &= A\hat{x}(t) + B\hat{u}(t) + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(t) \\
\hat{y}(t) &= C\hat{x}(t) + E\hat{u}(t) + [(C_1 - C_2)X + (E_1 - E_2)U]\hat{d}(t)
\end{aligned}
\qquad \text{2-8}
$$

These equations describe how small ac variations in the input vector and duty cycle excite variations in the state and output vectors.

The *circuit averaging* technique also yields equivalent results, but the derivation involves manipulation of circuits rather than equations. Switching elements are replaced by dependent voltage and current sources, whose waveforms are defined to be identical to the switch waveforms of the actual circuits. This leads to a circuit having a time-invariant topology. The waveforms are then averaged to remove the switching ripple, and perturbed and linearized about a quiescent operating point to obtain a small-signal model.

To be specific, usually the switches in converters can be represented by two-port network with terminal waveforms $v_1(t)$, $i_1(t)$, $v_2(t)$, $i_2(t)$. And with any two-port network, two of these terminal quantities can be treated as independent inputs to the switch network. The remaining two can be viewed as dependant signals. For example, for a boost converter, we replace the switch network with two-port network with independent sources as inductor current $i_1(t)$ and output voltage $v_2(t)$, which correctly represent the dependent output waveforms of the switch network.

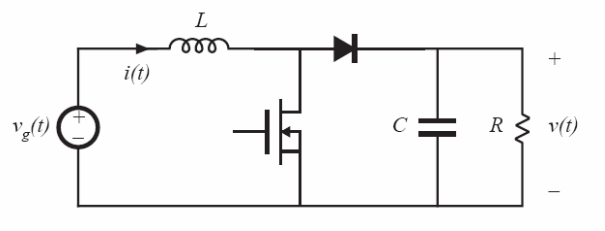


Figure 2-1 Boost converter example

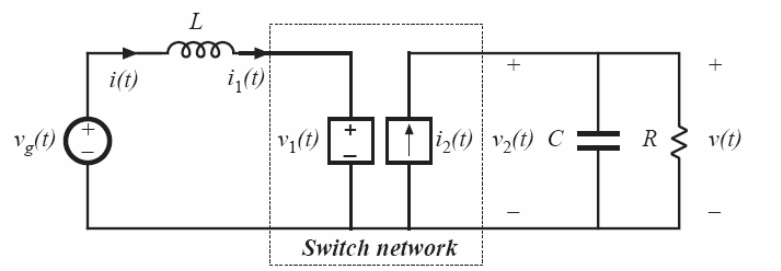


Figure 2-2 Replace the switches with independent network

The next step is averaging circuit. The basic assumption is made that the natural time constants of the converter are much longer than the switching period, so that the converter

contains low-pass filtering of the switching harmonics. One may average converters over the switching period Ts removing the switching harmonics, while preserving the low-frequency components of the waveforms. So if we average the switch dependent waveforms with considering duty cycle, the circuit will be shown in Figure 2-3. The $d'(t)$ represents $1-d(t)$ derived from the operation of the boost converter.

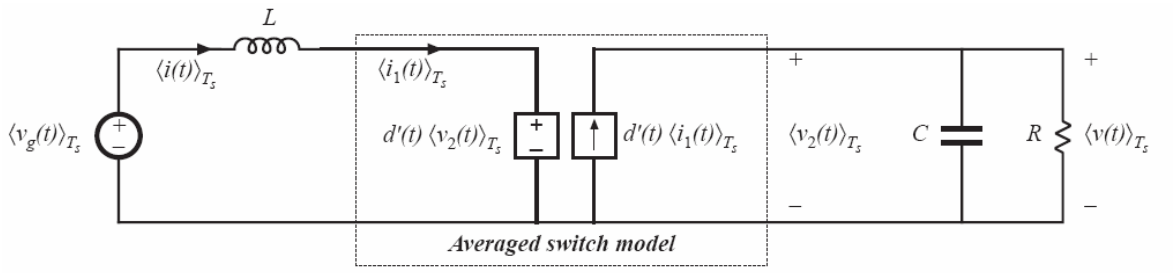


Figure 2-3 Averaged switch model

The model in Figure 2-3 is still nonlinear since the dependent source involves the multiplication of $d'(t)$ and inductor current $i_1(t)$ and output voltage $v_2(t)$. The network can be linearized by perturbing and linearzing the converter waveforms about a quiescent operating point, let

$$
\begin{aligned}
d(t) &= D + \hat{d}(t) \\
d'(t) &= D' - \hat{d}(t) \\
\langle v_g(t) \rangle_{Ts} &= Vg + \hat{v}_g(t) \\
\langle i(t) \rangle_{Ts} &= \langle i_1(t) \rangle_{Ts} = I + \hat{i}(t) \\
\langle v(t) \rangle_{Ts} &= \langle i_2(t) \rangle_{Ts} = V + \hat{v}(t) \\
\langle v_1(t) \rangle_{Ts} &= V_1 + \hat{v}_1(t) \\
\langle i_2(t) \rangle_{Ts} &= I_2 + \hat{i}_2(t)
\end{aligned}
\qquad \text{2-9}
$$

In equations 2-9, the model contains both dc and small signal as terms. Since the small signal assumption is satisfied the high order term like $\hat{v}(t)\hat{d}(t)$ can be neglected. Then linearized model is obtained in Figure 2-4. Then replace dependent generators with an ideal transformer, as in Figure 2-5.

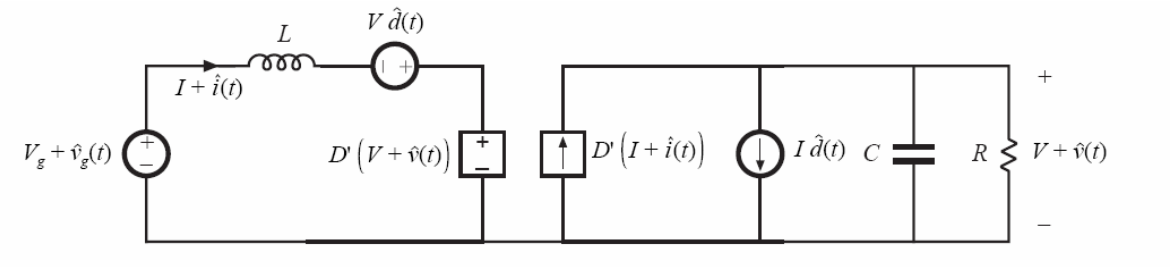


Figure 2-4 Linearized circuit-averaged converter model

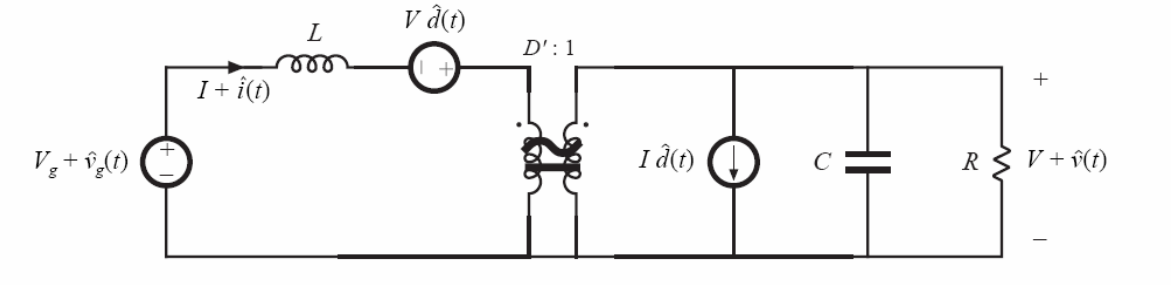


Figure 2-5 Final linearized circuit-averaged model

Figure 2-5 shows the complete circuit-averaged model, which functions simultaneously as the dc and the small signal as equivalent circuit for the boost converter. This model-derived procedure suggests that, to obtain a small signal ac converter model we need only to replace the switch network with its averaged model. This procedure is called *averaged switch modeling.*

2.3 Analog Controlled DC-DC Converters

It's known that the goal of designing a control system is to change system parameters to achieve certain desired system characteristics or performance. Therefore, it is necessary to have knowledge of system plant response and the loop response before design the feedback controller [B1, B2, B3]. The small signal models derived in section 2.2 are usually used to find the effects of feedback on the small signal transfer functions of the regulator.

A block diagram of a typical analog controlled buck small signal model is shown in Figure 2-6. The output voltage is sensed with gain $H(s)$, which is usually a voltage divider. The sense output $H(s)\hat{v}_o(s)$ is compared with V_{ref} to generate the error signal $\hat{v}_e(s)$. The objective of feedback loop is to make $H(s)\hat{v}_o(s)$ equal to V_{ref} regardless of the load and line disturbances.

That is to say, if the feedback system works perfectly, the error signal should be zero. To achieve small error signal here is one of the objectives of compensator network $G(s)$. $\hat{v}_c(s)$ is control signal generated by compensator and is fed into PWM to achieve the duty cycle gate signal for drivers.

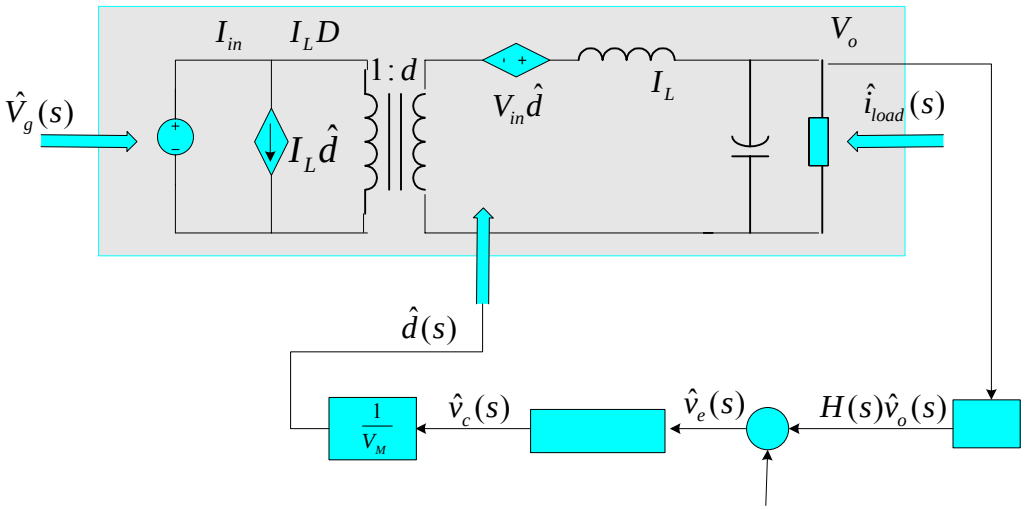


Figure 2-6 Analog controlled buck feedback model

So the system loop gain, $T(s)$, is defined in general as the product of the gains around the forward and feedback paths of the loop.

$$T(s) = \frac{H(s)G(s)G_{vd}(s)}{V_M} \qquad 2\text{-}10$$

$$\text{Where } G_{vd}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{V_{in}}{(LCs^2 + \frac{L}{R}s + 1)}.$$

The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output as long as adequate phase margin is maintained. Also stability and transient performance can be assessed using the phase margin test of loop gain. To be specific, the objective of compensation is to design the feedback network with suitable gain and phase delay to achieve a desirable bandwidth and sufficient phase margin, in order to make system achieve desired steady state accuracy, transient response, relative stability and the sensitivity to change in system parameters.

There are several typical types of analog compensation consisting of an amplifier and RC network. Lead compensator is also called proportional-derivative (PD) controller, which is usually utilized to improve the phase margin in a system originally consisting of a two poles. The possible side effect of PD compensation is that the PD compensator is sensitive to noise due to the derivative function.

Lag compensator (also called proportional-integral PI) is used to increase the low frequency loop gain, such that the output is better regulated at dc and at frequencies well below the loop crossover frequency. Combined PID compensator is to obtain both wide bandwidth and large dc loop gain for reduced steady-state error. The conventional Type III PID compensator consisting of an operational amplifier and RC network is realized in Figure 2-7 and the frequency response is shown in Figure 2-8. It is observed that, at low frequency, the integrator pole in the same manner as the PI compensator leads to large low-frequency loop gain and accurate regulation of low frequency component. The zero fz adds phase lead to improve the

phase margin as in PD compensator. High frequency poles fp1 and fp2 prevent the switching ripple from the disturbance of the PWM.

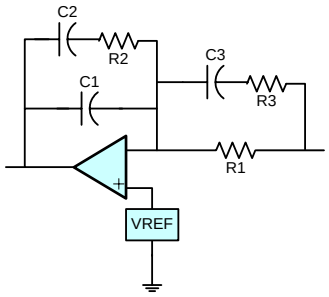


Figure 2-7 Type III compensator

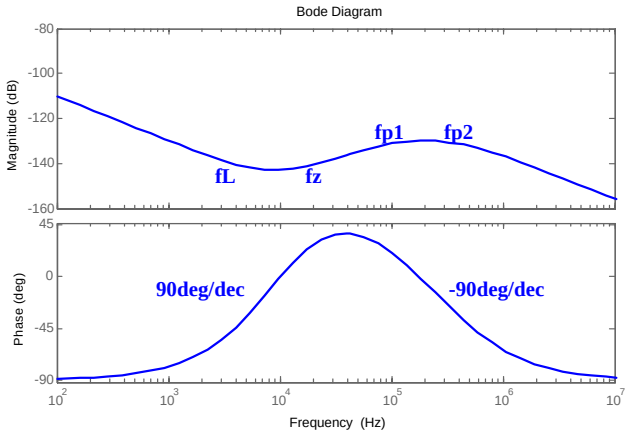


Figure 2-8 Response of Type III compensator

In generally, when one designs feedback compensation loop for power stage, it is desired to achieve loop bandwidth below 1/5 to 1/10 of switching frequency. In this case, the phase delay due to PWM modulation could be ignored. To achieve small steady state error and 'flat' closed-loop output impedance, the dc gain and low frequency gain should be as large as possible. The

loop gain is usually required to be –20dc/dec at the crossover frequency in order to have sufficient phase margin. Beyond crossover frequency, loop gain with a slope of –40 dB/dec provides good rejection of high frequency noise. The phase margin is required larger than 45 deg and the Gain margin is higher than 6 dB to 12 dB in general.

2.4 Digital Controlled Power Converter and Theoretical Basis

Conventional controllers for dc-dc converters are based on duty ratio adjustment for voltage regulation, and most of the commercially available controller products are based on analog techniques. Even though the above-mentioned analog control techniques have been matured, they are limited by sensitivity to noise and temperature, component parameter variation, and non-flexibility.

Digital controllers for switching power supplies offer a number of advantages including reduced number of passive components, programmability, implementation of more advanced control algorithms and additional power management, as well as reduced sensitivity to parameter variations.

A typical digital control system is shown in Figure 2-9. The system contains a sampler to detect continuous analog signal at discrete instances of time. Before a data hold is employed to reconstruct the original signal, a digital compensator block is added to improve system performance [B4].

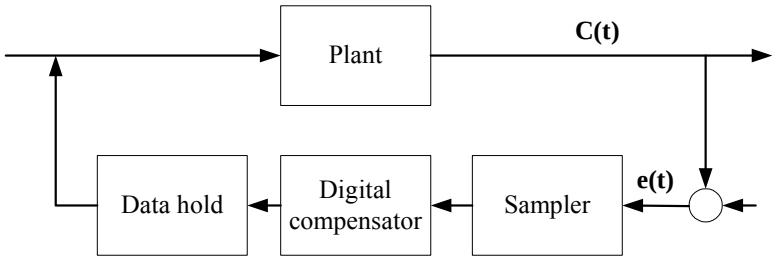


Figure 2-9 Typical digital control system

A commonly used method of data reconstruction is polynomial extrapolation [B4]. Using a Taylor's series expansion, one can express $e(t)$ as:

$$e(t) = e(nT) + e'(nT)(t - nT) + \frac{e''(nT)}{2!}(t - nT)^2 + ... \qquad 2\text{-}11$$

If the first term above is used, the data hold is called a zero-order hold (ZOH), which is expressed as $e_0(t) = u(t) - u(t - T)$. The corresponding transfer function is $G_{h0}(s) = \frac{1 - e^{-Ts}}{s}$, so the frequency response of the zero-order hold can be obtained as $G_{h0}(j\omega) = T \frac{\sin(\pi\omega / \omega_s)}{\pi\omega / \omega_s} e^{-j(\pi\omega/\omega_s)}$, and response in frequency domain of ZOH is shown in Figure 2-10.

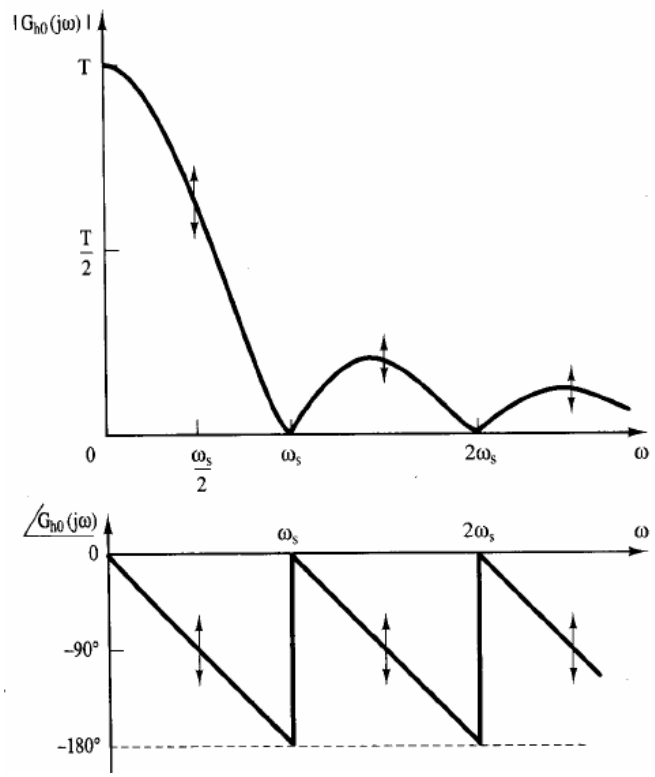


Figure 2-10 Frequency responses of ZOH

According to the Shannon sampling theorem, when the input signal is reconstructed, any frequencies $\omega > \omega_s / 2$ will reflect into the frequency range $0 < \omega < \omega_s / 2$. This effect is called frequency aliasing. The frequency aliasing can be prevented either by increasing ω_s or by placing an analog antialiasing filter in front of the sampler. The antialiasing filter is a low pass filter that removes any frequency components in $e(t)$ that is greater than $\omega_s / 2$, since the low pass filters introduce phase lag. However, the cutoff frequency of the antialiasing filter cannot be made so low as to destabilize the control system.

From the phase plot of zero-order hold, we can see that the zero-order hold introduces the phase lag into the system. When the bandwidth of the system is equal to the sampling frequency, the phase delay goes to 180^0. Generally, in order to make the phase delay of the zero-order hold as small as possible, the sampling frequency should be greater than the system bandwidth by at least 10 times, which means the phase delay goes to $\omega_s / 10 = 18^0$.

Applying digital control theory to power converter, compared to analog controlled system, the digital controlled power converter is shown in Figure 2-11. The output voltage is sensed by sensor circuit, and then the sense output $H(s)\hat{v}_o(s)$ is sampled by AD converter. The digital sensed output is compared with the reference signal v_{ref} and thus digital error signal is generated. The digital compensator generates the duty cycle control signal according to the input error signal $\hat{v}_c(z)$ and feeds the control signals into PWM to get the drive signal to power stage [B5, B6].

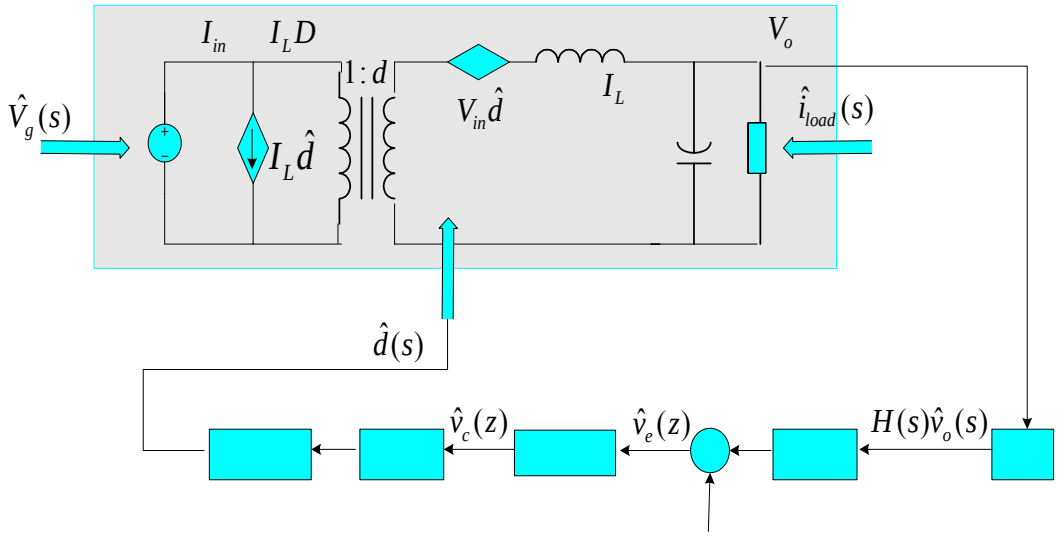


Figure 2-11 Digital controlled power converter feedback model

For the digital control loop, the loop gain turns out to be

$$T(s) = H(s)G(s)G_{vd}(s)G_{PWM}G_{ADC} \qquad Vin \qquad \text{2-10}$$

Where G_{PWM} and G_{ADC} are the gain of DPWM module and gain of AD converter respectively. G_{PWM} is the ratio of PWM switching frequency and clock frequency, which is[B6]

$$G_{PWM} = \frac{f_{PWM}}{f_{Clock}} \qquad \text{2-11}$$

G_{ADC} is reverse proportional to resolution LSB of ADC, or [B6]:

$$G_{ADC} = \frac{1}{LSB} \qquad 2\text{-}22$$

Therefore, the DPWM and ADC introduce the gain changes to loop gain over analog controller, which need to be considered when designing the digital compensator.

Meanwhile, the sensitivity of the AD converter, inherent time delay of the calculation/sampling and the precision of the numerical value all affect the performance of the system. It is therefore necessary to give careful consideration to ADC sampling frequency and resolution design.

Generally speaking, ADC resolution is determined by the precision requirements of power stages. That is to say, the LSB value of ADC must be smaller than the minimum required output voltage resolution. The sampling frequency of ADC should generally be 10 or 20 times of system bandwidth to minimize phase delay due to sampling.

DPWM acts as a DA converter, and generates pulse width modulated switching waveforms for driving power stage switches. Since the discrete change in duty ratio due to resolution of DPWM, there is a corresponding discrete change in output voltage. It is important that the value of the minimum output voltage change be smaller than the LSB size of the ADC to avoid limit cycle oscillation. Therefore, the DPWM resolution must be greater than the resolution of ADC. This point will be discussed more in Chapter 3.

2.5 Digital Controller Design Methodology

Usually, digital compensator design has two design methods: *Digital redesign* approach and *direct digital design* approach [B5]. In *direct design* approach first discrete model of sampled analog components is built. Then, the compensator design is done directly in Z-domain including the accurate modeling of sampling functions. With the *direct design*, the frequency response techniques, such as gain margin and phase margin, can be used also.

Digital redesign assumes the sampling frequency is much greater than the system crossover frequency, so the design equivalent approach is accurate. This approach first models the discrete components as analog components approximately, and then designs the analog controller with standard analog control technique. Finally, it maps the analog compensator into digital with equivalent mapping methods. Since the techniques of modeling power converter to linear continuous time domain are well known, this dissertation will focus on the *Digital redesign* approach

As mentioned in above section, usually an analog PID compensator is consists of proportional coefficient Kp , integral coefficient Ki and derivative coefficient. Kd . So an s-transform PID description in continuous time domain is shown in equation 2-23,

$$G(s) = Kp + \frac{Ki}{s} + Kd \cdot s \qquad 2\text{-}23$$

Let's consider how to derive the discrete-time equivalent to PID compensator. Figure 2-12 shows an *RC* integrator implemented with amplifier. $v_e(t)$ is the input error voltage and $v_c(t)$ is the output voltage of *RC* integrator. For this integral term, assuming we sample the input

error signal with sampling period T, then $v_e(t)\big|_{t=nT} = v_e(nT) = v_e(n)$. To derive an equation for the discrete compensator output, we need an approximation to the continuous integral (or area under the curve).

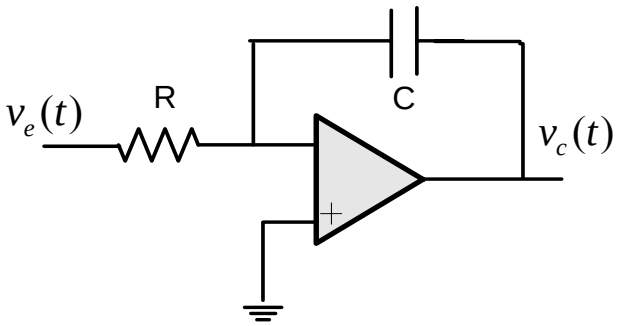


Figure 2-12 RC integrator

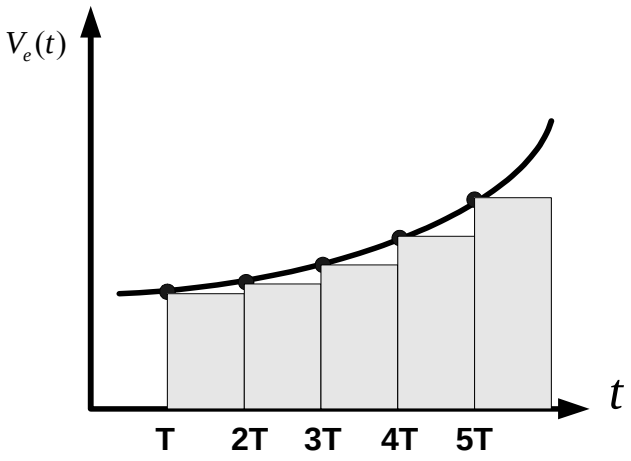


Figure 2-13 ZOH sampling approximation

A zero-order-hold (ZOH) or forward rectangular approximation is shown in Figure 2-13, resulting in the output [B4]:

$$v_c(n) = v_c(n-1) - \frac{T}{\tau_i} v_e(n-1) \qquad 2\text{-}24$$

where τ_i is the time constant RC. And a more accurate straight-line approximation (trapezoid) requires the ability to compute the current output based on the current input:

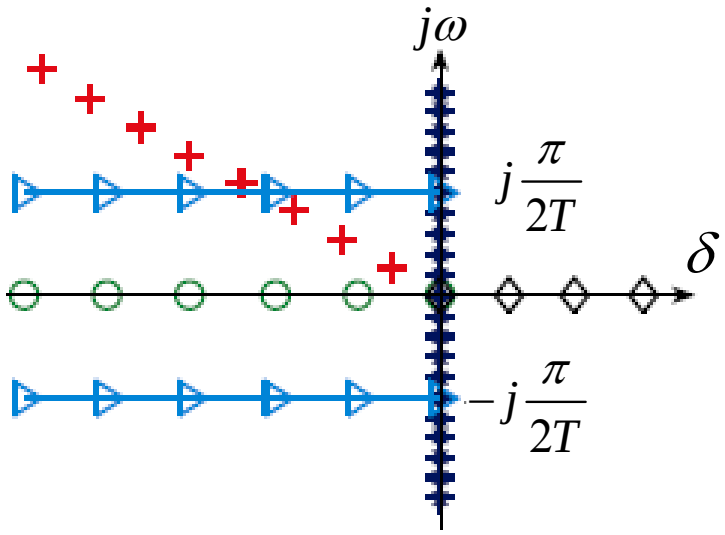
$$v_c(n) = v_c(n-1) - \frac{T}{2\tau_i}[v_e(n) + v_e(n-1)] \qquad 2\text{-}25$$

Therefore, the discrete-time equations can be written in "difference equation" and infinite summation forms, as the dual to the continuous-time differential and integral forms: $\Delta v_c(n) = v_c(n) - v_c(n-1) = -\frac{T}{\tau_i} v_e(n-1)$ and $v_c(n) = -\frac{T}{\tau_i} \sum_{k=-\infty}^{n-1} v_e(k)$. We will use the terminology of difference equation, but continue to use the recursive form due to the convenience in working with the z-transform and hardware implementation [B4]. The z-transform is a discrete-time, sampled-data dual of the Laplace transform, which contains duals of all the well known intuitive characteristics and can be used to analyze constant coefficient, linear difference equations:

$$\text{Z-transform: } v_c(z) = \sum_{n=-\infty}^{n=\infty} v_c(n) z^{-n}$$

$$\text{Laplace transform: } v_c(s) = \int_{-\infty}^{\infty} v_c(t) e^{-st} dt \qquad 2\text{-}26$$

Note that with $z = e^{sT}$ the z-transform has the form of a sampled version of the Laplace transform. Therefore, the s-plane stability boundary, $s = j\omega$ maps to the unit circle in the z-plane ($z = e^{j\omega T}$). Thus our considerations before with the s-plane "left-half-plane (LHP)" will map to considerations inside the z-plane "unit-circle", as shown in Figure 2-14.



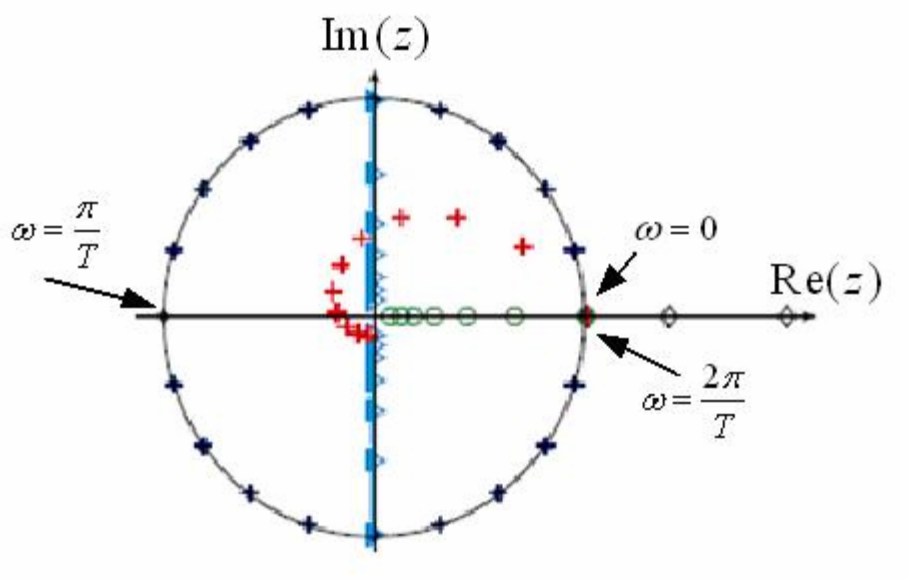


Figure 2-14 ZOH sampling approximation

Need to point out that mapping from s to z is many-to-one, and this is due to periodic behavior around the unit circle. Thus multiple poles/zeros in s-plane map one location in z-plane, which actually means multiple time signals have identical discrete samples.

Therefore, applying z- transformation to zero-order-hold (ZOH) equation, we will obtain $V_c(z) = z^{-1}V_c(z) - \frac{T}{\tau_i} z^{-1}V_e(z)$, and then the z form transfer function is $H(z) = \frac{V_c(z)}{V_e(z)} = -\frac{T}{\tau_i}\frac{1}{z-1}$. Figure 2-15 plots the z-form block diagram of an integrator.

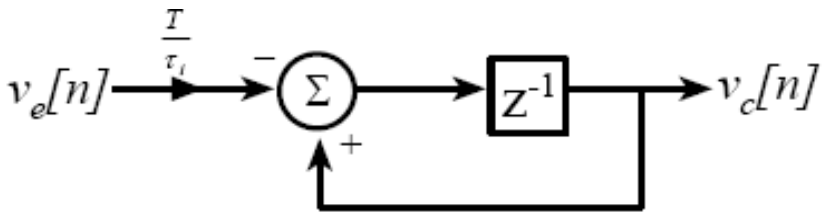


Figure 2-15 Z form integrator with ZOH approximation

Meanwhile, applying z-transformation to straight-line approx, trapezoid (bilinear or Tustin) rule, we get $V_c(z) = z^{-1}V_c(z) - \frac{T}{2\tau_i}(1+z^{-1})V_e(z)$ and transfer function:

$$H(z) = \frac{V_c(z)}{V_e(z)} = -\frac{T}{2\tau_i}\frac{z+1}{z-1}.$$

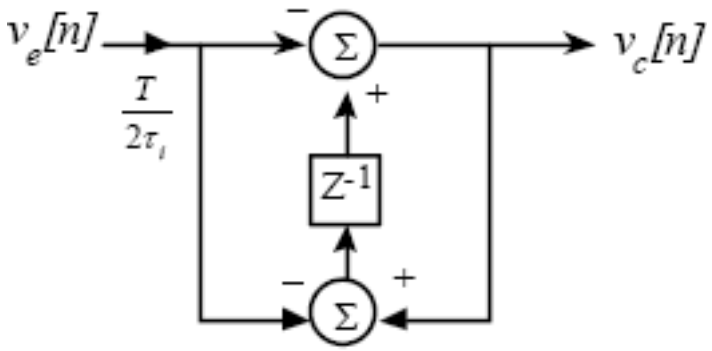


Figure 2-16 Z-form integrator with straight-line approximation

Figure2-17 is the frequency response comparison of the continuous time (black), ZOH (red) and Bilinear (blue) mapping of integrator. The discrete time responses are really accurate when frequency is much less than sampling frequency, but exhibits aliasing when frequency is larger than half of the sampling frequency.

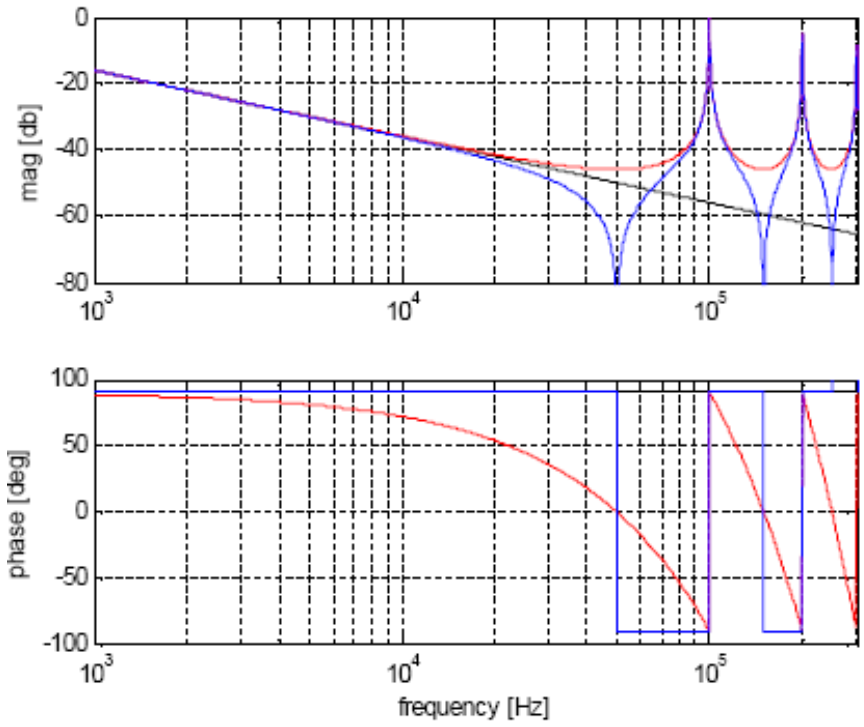


Figure 2-17 Response comparison of continuous time, ZOH and bilinear transformer

Besides ZOH and bilinear, there are a number of other different approaches are commonly used to estimate the transformation from continuous to discrete filter designs. We are going to compare three widely used approaches: Bilinear, Pole-zero mapping and Triangle hold transformation [B5~B6].

As discussed above, *Bilinear transformation (BLT)* basically performs approximation to integral using the area of a trapezoid between points. It is using pre-warping to map the entire left-half s-plane to inside the unit circle. This perfectly maps the stability axis $j\omega$ to unit circle, and there is no aliasing consequently. The basic procedures are first selecting a critical frequency (e.g. relative to sampling, filter corner or system crossover frequency) ω_{crit} to match, and then substitute for s in $H(s)$ to determine $H(z)$:

$$H(z) = H(s)\Big|_{s=\frac{\omega_{crit}}{\tan(\omega_{crit}T/2)}\cdot\frac{z-1}{z+1}} \qquad 2\text{-}27$$

With Bilinear transformation (BLT) the number of poles and zeros are equal. If number of poles is more than that of zeros, additional zeros at $s=\infty$ are mapped to $z=-1$, and this represents the highest frequency $f_s/2$ available in the z-domain. If the number of zeros is more than that of poles, additional poles at $s=\infty$ are mapped to $z=-1$, which creates problems in a compensator since it creates significant peaking as f approaches $f_s/2$. Since the BLT maps the entire s-domain LHP once around the unit circle, there is no aliasing in added poles.

The *Pole-Zero Mapping* method maps all poles and finite zeros using the transformation pole or zero at $s=-a$ using pole at $z=e^{-aT}$. If there are m more poles than zeros (e.g. zeros at $s=\infty$), then map m zeros to $z=-1$. This requires the ability to apply the current input to the current output (as discussed below). Then set the gain of the filter such that the magnitude of $H(z)$ matches the magnitude of $H(s)$ at a critical frequency (such as

the crossover frequency). But we must consider how to map when the number of poles and zeros are different. If the number of poles is more than that of zeros, additional zeros at $s = \infty$ are mapped to $z = -1$ and this represents the highest frequency $f_s / 2$ available in the z-domain and is a reasonable mapping. But if the number of zeros is more than that of poles, a direct pole-zero map of pole at $s = \infty$ is to $z = 0$. So these poles must be added to make the system realizable (causal). Mapping to $z = 0$ represents a z^{-1} unit delay, which corresponds to an effective e^{sT} delay term in the s-domain transfer function. Alternatively, poles can be placed in the Z-plane; this requires manual modification of pole/zero mapping. As an additional pole is moved from $z = 0$ to $z = -1$, peaking is introduced in the magnitude response.

Triangle Hold effectively extrapolates samples of the continuous time filter in a straight line, then solves for the z-transform of the samples like the following equation: $H(z) = \frac{(z-1)}{Tz} Z(\frac{H(s)}{s^2})$. *Triangle hold* always results in the same number of poles and zeros (just as with the BLT), however, extra zeros are NOT mapped to $z = -1$.

There are many options for hardware implementation for this digital compensator function. The delays can be implemented as a code step (DSP/micro) or a clocked latch (FPGA/custom), and multiply and add blocks can be implemented in arithmetic units, dedicated multipliers, or look-up tables, which are especially useful when a reduced set of possible inputs can be pre-computed. The digital coefficients can be hardwired, boot-time programmable, or real-time adaptive with look-up tables, can also create non-linear control possibilities.

Recall the PID compensator in continuous time domain mentioned earlier. $G(s) = Kp + \frac{Ki}{s} + Kd \cdot s$ Applying bilinear transformation $s = 2 f_s \frac{z-1}{z+1}$, then we will get discrete PID compensator as follows:

$$G(z) = K_P + K_I \frac{1}{2 f_s} \frac{z+1}{z-1} + K_D 2 f_s \frac{z-1}{z+1} \qquad 2\text{-}28$$

Where K_P is the gain in the proportional path, K_I the gain in the integral path, and K_D the gain in the derivative path and f_s sampling frequency. But in most cases, to easily implement the digital compensator, a typical digital PID structure is shown is Figure 2-18. This PID structure is corresponding to Equation 2-29, which provides one pole and two zeros.

$$G(z) = K_P + K_I (\frac{1}{1 - z^{-1}}) + K_D (1 - z^{-1}) \qquad 2\text{-}29$$

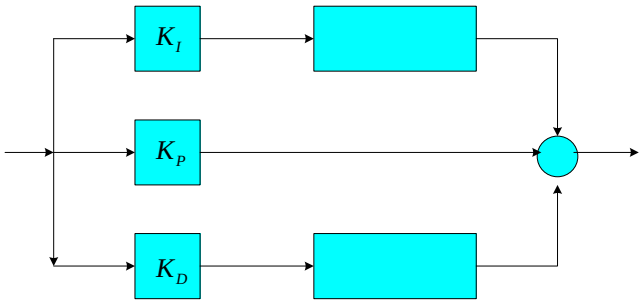


Figure 2-18 Typical digital PID structure

Term Kp applies a proportional gain to the error $E(n)$. As the gain term is increased, the power supply responds faster to changes in $d(n)$, but decreases system damping and stability. Step response overshoot and ringing could be caused by too a large value of the gain term.

Integral term Ki reduces steady state error to zero. The integrator has infinite dc gain, and consequently adjusts the mean supply output voltage to drive its input to zero. The amount of time power supply takes to reach its steady state is inversely proportional to the integral gain Ki. Instability and oscillation can also be caused by too large value of the integral term. Too small of an integral gain can result in limit cycle oscillation.

The derivative term Kd can improve stability, reduce step-response overshoot and reduce step-response time. The derivative term is proportional to the rate of change of the error signal $E(n)$ and therefore improves controller reaction time by predicting changes in the error. Following an output disturbance, the supply output will return to its nominal value faster as Kd is increased, however output overshoot could be caused by too much damping from the derivative term.

2.6 Digital Power System Management

Digital Power is usually defined as digitally controlled power products that provide configuration, monitoring, and supervisory functions, which extends to full loop control. It is important to note that “digital power” really includes two different areas of power technology. One is “digital control”, the real-time, cycle-by-cycle control of the switches. The other area is “digital power management” [B9].

"Digital control" involves feedback control design, which is the main contribution of this dissertation. "Digital power management" generally refers to non-real-time interaction with a power converter to:

- Configure or program a power converter's operational characteristics or identification information.
- Control the converter (e.g. turn it on, turn it off, adjust the output).
- Monitor the state of the converter.

Digital power management is growing in popularity for two reasons. First, it allows the user to do things that are not possible with a purely analog system, like communication, power-up sequencing, margining and other configuration chores. An analog system does not allow the user to retrieve a converter's status. The reported information can be in the form of binary information or as parametric information. For example, the unit is on or off, is OK or has a fault, or has normal temperature or is operating in an overtemperature condition. The parametric information could be output voltage, output current or temperature. If the status information is stored in non-volatile memory and is available after a fault, this information can be very useful in determining the real cause of failure. Because "no problem found" faults a large problem with the system Original equipment manufacturers, the ability to retrieve a converter's operating condition in the moments before a failure is reported may save a lot of money in service costs.

Second, digital power management makes some tasks easier and cheaper than in the analog domain. For example, in the application of wide range of output voltage, the programmability of digital power management allows to change the output voltage just by sending commands over a communications link and not by changing voltage divider. And also for adjustment of protection thresholds, such as output overcurrent or overtemperature, digital

management allows the protection of the system to be optimized without any physically changing parts. The ability to program also allows for converter calibration. The converter manufacturer might use this to reduce cost by using less expensive analog components and making up for the error with a digital calibration.

Currently, there are several choices of power system management protocols available for general use. Table 2-2 shows comparison of digital power management buses. One possible choice is IPMI (Intelligent Platform Management Interface) but it is much more than what is needed for power system management since it's complicated. For portable and handheld devices, National Semiconductor and ARM have created the PowerWise. This protocol is suited for small devices and does have the advantage of being an open standard. As part of their Z-One Digital IBA product set, Power-One has created a digital power management protocol. This protocol is embedded in Power-One's product offerings. Recently, several power supply and power semiconductor companies joined together to create the PMBus. This protocol is touted as being a comprehensive solution that will be freely available to any who wish to use it.

For the transport method of digital power management, there are several physical lay buses available to choose for data transferring.

Table 2-1 Digital power management buses comparison [B9]

BUS	**Advantages**	**Disadvantages**
I^2C and SMBus	Low cost, Easy to use, Well understood, Lots of support in Ics	Distance limited, Number of devices limited, Noise sensitive if not properly designed, Fault tolerance requires lots of extras design work
Point-to-point UART (RS-232, RS-422)	Medium cost, Well supported in silicon	Point-to-point only, Complex to program, Requires precision clocks
Multi-point UART (RS-485)	Up to 32 connections, Good noise immunity, Good for medium distance	Complex to program, Moderately expensive, Requires precision clocks
SPIBus	Low cost, Good speed	Limited support in silicon, Each device requires a DEVICE SELECT line, Only supports single master systems
CANBus	Highly robust	Expensive, Hot swap Is difficult, Requires high precision clocks
Ethernet	Good for very long distance, Supports a large number of devices, Robust, Hot swappable	Very expensive for a power application, Complex to program
Universal Serial Bus (USB)	Promising, Widely used in computing world, Potential for high speed (480 Mbps)	Unproven for power. Not the lowest cost, Programming complexity
IEEE 1394 (Firewire)	Potential for high speed (800 Mbps)	Unproven for power, Higher cost, Not widely used in the Computer world, Programming complexity

Until recently, digital power manage functions relied on proprietary interface protocols and the use of the physical layer of popular buses such as I^2C and SMBus. But selecting a part with a proprietary protocol forces the designer to stay with a particular manufacturer for the entire design. A standard, on the other hand, allows for multiple manufacturers to be used within a single design.

PMBus is an open-standard digital power-management protocol with a fully defined command language and transport and physical interface. PMBus is used for host systems to communicate with power converters (see Figure 2-19). The protocol was founded and is being maintained by power supply and semiconductor manufacturers, such as Artesyn Technologies, Astec/Emerson Network Power, Intersil Corp., Microchip Technology, Summit Microelectronics, Texas Instruments, Volterra Semiconductor, Zilker Labs Inc., and others. The first release of the protocol was in March 2005.

The PMBus transport layer is based on the SMBus. The main difference between SMBus and I^2C is a signal line called SMBALERT, which in the PMBus case allows power converters to interrupt the host of the system. This results in efficient and flexible power control designs.

One thing to note is that the PMBus protocol dictates that a power converter must power-up and work even if there is no digital communication. The configuration is stored in non-volatile memory or is pin-programmed. The physical address of each device is set with pins on the power converter. In addition to the SMBus' clock, data and interrupt lines, the PMBus

protocol also specifies two hardwired signals for use with power converter devices. One is a control signal to turn individual power converters on and off and the other is an optional write-protect signal that can be used to prevent any changes to memory-held data. PMBus has the advantage that the host device is not based on a proprietary digital interface. The host device can be a processor or a microcontroller as well as any other intelligent device (i.e. laptop computer). The laptop can be used in manufacturing and test for pre-production calibration.

PMBus communicates via a simple set of commands. Every packet contains an address byte, followed by a command byte, then, if needed, data bytes and an optional packet error code byte. The host uses single start-and-stop conditions to indicate the start and end of the process, and the addressed power converter uses a single bit to acknowledge reception of each byte. Power converters not meeting the manufacturer's specification can be repaired, replaced or recalibrated as part of the test process.

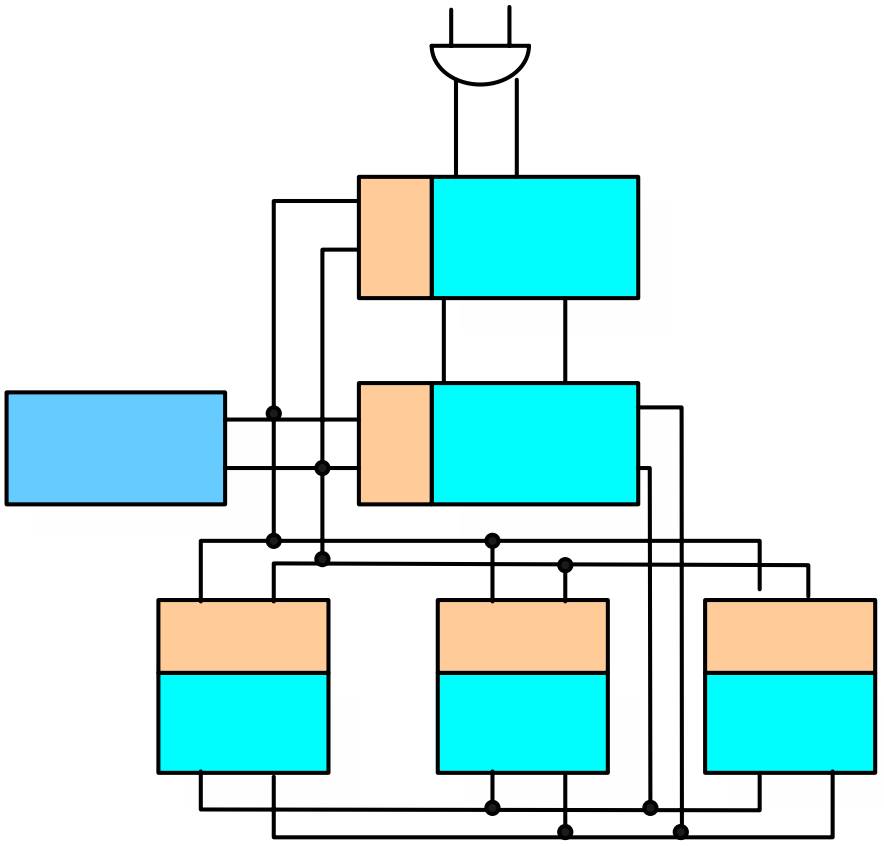


Figure 2-19 Digital power management with PMBus

2.7 Summary

Power converter system needs feedback controller to tune up system performance to meet the stability, regulation and transient response specifications. Modeling techniques of power converter provides mathematical analysis means to obtain converter's behaviors. Analog controller design is traditionally mature and has a lot of advantages, in the other hand, digital power is the feedback control of a power converter via digital methods as opposed to analog

means. In addition, digital power also refers to the digital communication that takes place between the host controller and the power converters in a system. The latter is sometimes referred to as digital power management.

3 ALGORITHMS AND DESIGN OPTIMIZATION BASED ON DIGITAL CONTROLLER SI8250

3.1 Introduction

A typical digital controlled switching power converter is discussed in Chapter 2. Compared with analog control loop, DPWM performs the same drive signal generation function as its analog counterpart, but it does so by "calculating" and "timing" the desired duration of ON and OFF periods of its output signal. By contrast, an analog PWM usually operates by triggering ON at a clock transition and triggering OFF when a fixed voltage "ramp" reaches a pre-set trip voltage. The difference is important because it leads to many of the advantages and challenges associated with digital control.

Typically a digital PI or PID style subsystem acts as compensator to perform the task of translating a digital representation of output voltage into duty-cycle information fed to the DPWM block. PID controller adjusts the output voltage on a programmable reference by adjusting pulse width, in real-time, to provide output voltage regulation. The PID compensator is required to compensate for gain and phase-shift factors around the control loop to achieve desirable performance as in the analog controller. In digital controlled systems, there is additional phase shift arising from time delays in processing the digital data. The major gain and phase-shift factors in an analog system are considered when designing a digital controlled system, taking into consideration the time delay from AD conversion and other delay factors.

Analog control provides very fine resolution for output voltage adjustment. In principle, output voltage can be regulated the programmed reference, the error between the reference and output is only limited by finite loop gain, thermal effects and system noise. On the other hand, a digital control loop has a finite set of discrete "set points" resulting from the resolution of "quantizing elements" in the system. The following points have to be carefully considered in digital power design:

- Digital compensator design law
- Resolution of ADC and DPWM
- Quantization and limit word length effect of digital coefficients

As we know, with *Digital redesign,* discrete components are approximately modeled as analog components, and then analog controller is designed with standard analog control technique. The analog compensator is mapped into digital domain with equivalent mapping methods. With this approach, direct tuning digital coefficients of a controller would be difficult since controller design knowledge is based on S domain. Thus to remap the digital coefficients change to continuous domain response would be quite helpful for designers, but it need to point out that remapping digital coefficients to poles/zeros location in continuous domain won't be one-to-one mapping.

This chapter will discuss about the digital controller design challenges, such as how to optimize digital coefficients directly from discrete domain and how to remap the coefficients to poles/zeros location change in continuous time domain. Further, the system performance deviation due to limited resolution of ADC and DPWM, calculation error of digital coefficients and quantization effect in the digital design will be discussed. Based on the constructed PID structure, those issues have been explored in term of simulation and experiments. A single phase

POL converter is developed with digital controller Si8250, and the control loop design is accomplished based on Matlab. A nonlinear control algorithm is proposed and implemented based on the digital controlled POL converter.

3.2 Digital control design for power converters

As we know, an analog compensator is usually implemented with RC network and an operational amplifier. Let's consider a type III PID compensator and its network is shown in Fig 3-1 and the associated frequency response in Fig 3-2. Type III compensator has one pole f_{p1} at DC, other two high frequency poles f_{p1}, f_{p2} and two zeros f_{z1}, f_{z2}. First pole f_{p1} at 0 frequency is able to improve the DC gain resulting in smaller steady state error. And first zero f_{z1} is recommended to place around 1/10 of crossover frequency of loop response since the phase lag due to the integrator pole won't be completely canceled out by this zero until 10 times of f_{z1} reaches. That means in order to make the phase not be degraded at the crossover frequency f_{z1} must be greater than $1/10$ of crossover frequency. However, the lower f_{z1} will give the higher dc gain, which benefits the loop performance. The second zero is recommended to locate around or less than crossover frequency to improve the phase margin and make the response magnitude achieve $-20dB$ attenuation at crossover frequency. And the other two poles could be utilized to cancel out the ESR zero or attenuate the high frequency noise in the system [B10].

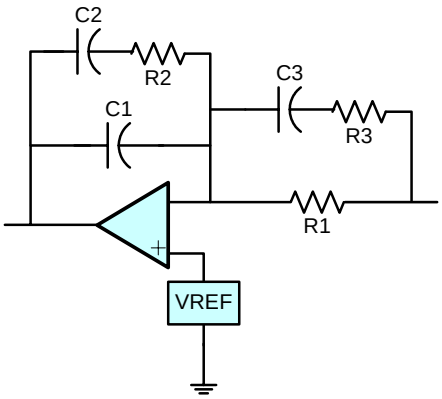


Figure 3-1Type III compensator

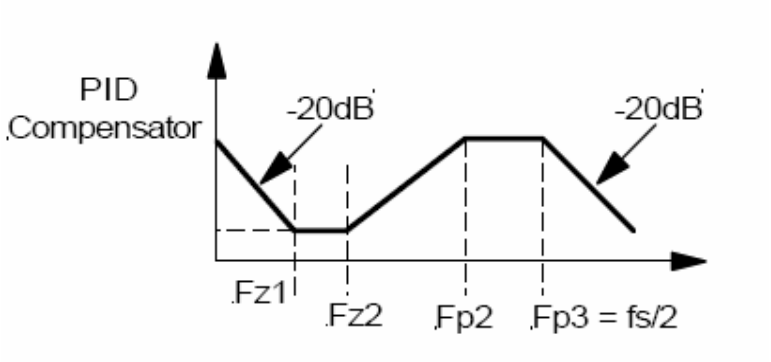


Figure 3-2 Frequency response of Type III compensator

Therefore, type III network is basically a three poles two zeros PID structure. Write type III to s-domain transfer function in equation.

$$G_c(s) = G_{oc} \cdot \frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{s \cdot \left(\frac{s}{\omega_{p1}}+1\right)\left(\frac{s}{\omega_{p2}}+1\right)}$$

$$G_{oc} = \frac{1}{R_1(C_1+C_2)}, \quad \omega_{z1} = \frac{1}{R_2 C_2}, \quad \omega_{z2} = \frac{1}{C_3 \cdot (R_1+R_3)},$$
$$\omega_{p1} = \frac{1}{R_2(C_1 // C_2)}, \quad \omega_{p1} = \frac{1}{R_3 C_3}$$

3-1

To construct this PID structure, we split the function into two stages to avoid 3rd order structure. Assuming we have first stage PID $G_{PID}(s) = \frac{(s-z_{s1})(s-z_{s2})}{s}$, which is two zeros one pole PID filter, and second stage $G_{LPF}(s) = \frac{1}{(s-p_{s1})(s-p_{s2})}$, which is a two poles filter. Thus those two stage filters construct a type III PID network and the response is shown in Figure 3-3.

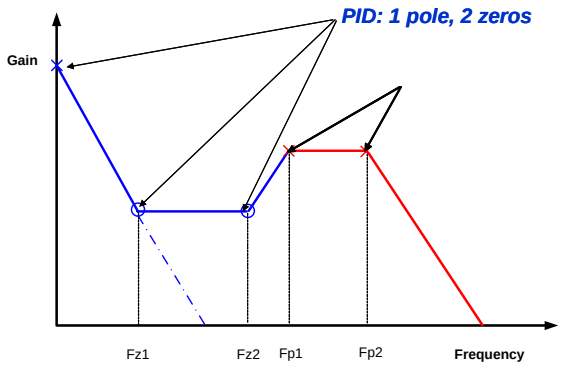


Figure 3-3 Frequency response of two stage PID structure

Applying bilinear transformation to those two stages filter, the z-transform function will be derived in equation. Since bilinear transformation will keep the number of poles and zeros equal, the function has equal order of denominator and numerator.

$$G(z)\cdot = G_{PID}(z)\cdot G_{LPF}(z) = G_0 \cdot \frac{(z+1)(z-z_{z1})(z-z_{z2})}{(z-1)(z-p_{z1})(z-p_{z2})} \qquad 3\text{-}2$$

Where z_{z1}, z_{z2} and p_{z1}, p_{z2} are the zeros and poles in z-plane respectively and G_0 is the normalized gain.

Considering the feasibility of digital PID hardware, the compensator will be implemented as two-stage structure too; we use a usual digital PID compensator as the first stage and a two-pole filter as second stage. Then the whole filter will be constructed in following fig 3-4.

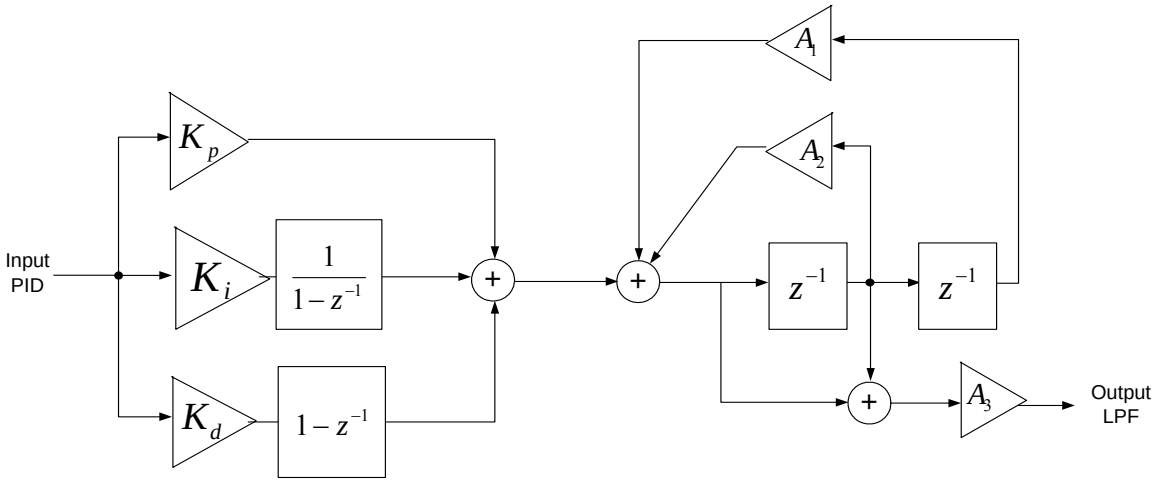


Figure 3-4 Two stage digital PID structure

According to this structure, the first stage filter will provide one pole and two zeros and transfer function is shown in equation:

$$K_P + K_I(\frac{1}{1-z^{-1}}) + K_D(1-z^{-1}) = \frac{(K_P + K_I + K_D) - (K_P + 2K_D)z^{-1} + K_D z^{-2}}{1-z^{-1}} \qquad 3\text{-}3$$

The second filter is a two-pole filter with pole coefficients of A_1 and A_2, plus a gain term with coefficient of A_3. Coefficients A_1 and A_2 will control the cutoff frequency of the two poles. The frequency of the first zero is located at one-half of sampling rate. Gain term A_3 adjusts the dc gain of the low-pass filter. The transfer function is shown in Equation:

$$\frac{A_3(1+z^{-1})}{1+A_1 z^{-1} + A_2 z^{-2}} \qquad 3\text{-}4$$

We are using *digital redesign* approach to design a flow chart as shown in Figure 3-5. First we design continuous time domain controller, which means we place poles and zeros in s-domain, and then map the s domain compensator into z domain with bilinear transformation. Since we already constructed two-stage PID compensator, the z domain function with digital coefficients $K_P, K_I, K_D, A_1, A_2, A_3$ could be formed. So the design goal now is to derive $K_P, K_I, K_D, A_1, A_2, A_3$ according to s domain compensator function, which is ready to meet the system performance requirement in continuous time domain.

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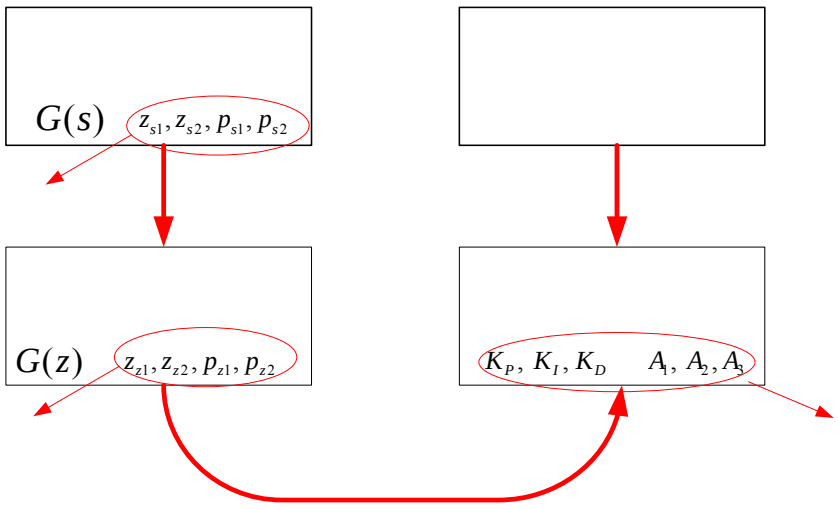


Figure 3-5 Design procedures of digital compensator

Now we split digital compensator

$$G_0 \cdot \frac{(z+1)(z-z_{z1})(z-z_{z2})}{(z-1)(z-p_{z1})(z-p_{z2})} \tag{3-5}$$

into two terms of $\frac{(z-z_{z1})(z-z_{z2})}{(z-1)}$ and $\frac{(z+1)}{(z-p_{z1})(z-p_{z2})}$ to match two stages.

Then the first stage contributes two zeros and one integrator pole at dc, and the second stage contributes two poles. Note that in the second stage filter $(z+1)$ presents one zero at half of the sampling frequency and $z_{z1}, z_{z2}, p_{z1}, p_{z2}$ are zeros and poles formed in *redesign* approach from s domain response consideration.

Then we compare the split digital compensator forms with transfer function of constructed PID filter. Considering Equation 3-3, 3-4 and 3-5, we have:

$$\frac{(K_P+K_I+K_D)-(K_P+2K_D)z^{-1}+K_D z^{-2}}{1-z^{-1}} \cdot \frac{A_3(1+z^{-1})}{1+A_1 z^{-1}+A_2 z^{-2}} =$$

$$G_0 \cdot \frac{(z+1)(z-z_{z1})(z-z_{z2})}{(z-1)(z-p_{z1})(z-p_{z2})} \tag{3-6}$$

The digital coefficient can be derived as:

$$\begin{aligned} K_d &= z_{z1} \cdot z_{z2} \\ K_p &= z_{z1} + z_{z2} - 2 \cdot z_{z1} \cdot z_{z2} \\ K_i &= 1 + z_{z1} \cdot z_{z2} - z_{z1} - z_{z2} \\ A_1 &= -(p_{z1} + p_{z2}) \\ A_2 &= p_{z1} \cdot p_{z2} \end{aligned} \tag{3-7}$$

Apparently, from the above equations, A_1, A_2 are determinate by poles and K_P, K_I, K_D are determinate by zeros. And gain A_3 is related to the S domain gain and gain change in converting from S domain to Z domain.

3.3 Digital Controller Design Case Study

Let's use buck converter as a case study to verify the design with constructed two-stage PID compensator structure. The specifications of this buck are shown again in figure 3-6. The input voltage *Vin* is 4v and is desired to supply a 0.1ohm resistor.

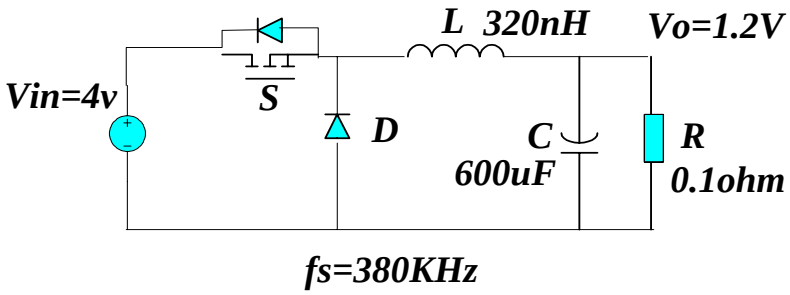


Figure 3-6 Case study - Buck converter

MatLab is used to construct the transfer function of buck converter with consideration of ESR/ESL values of inductor and capacitor in this case study.

The response of buck converter is drawn in MatLab and shown in Figure 3-7. The power stage response has crossover frequency of approximately 30 kHz, with a phase margin of 20^0. The resonant peak due to LC is around 11 kHz. Apparently this uncompensated response has no sufficient phase margin and needs more dc gain as well. Therefore, the compensated loop response is desired to have more bandwidth with large enough phase margin at least 60^0 to make system good stability in regulation and small overshoot and ringing in transient response.

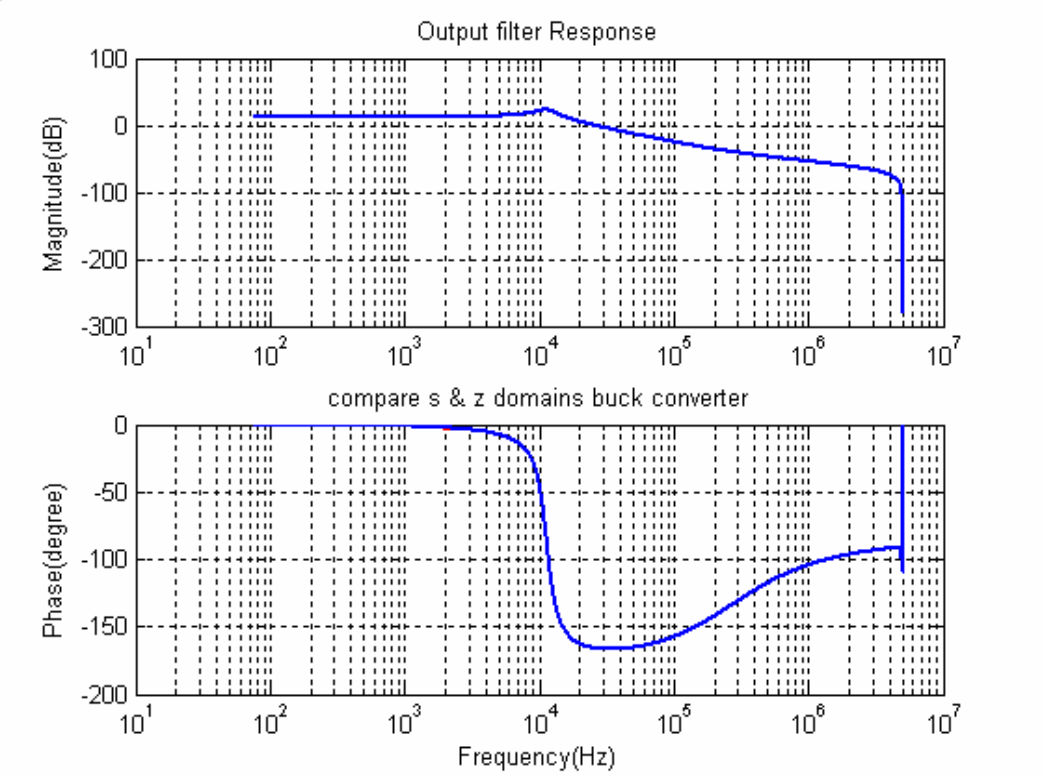


Figure 3-7 Response of Buck converter

The switching frequency of converter is designed at 380 kHz. Applying three poles/two zeros type III compensator to feedback loop, we place the first zero at 4 kHz to cancel out the phase degrading around the crossover frequency and the second zero at 19 kHz to improve the phase margin. Two poles of low pass filter are put around switching frequency 400 kHz to reduce the switching noise. The resistors and capacitors are picked out according to the desired locations of poles and zeros as below equations (3-8). Then the continuous time domain PID compensator response is obtained.

$$C_1 = 2.2\times10^{-10},\ C_2 = 2.178\times10^{-8},\ C_3 = 7.979\times10^{-9},$$
$$R_1 = 1\times10^{3},\ R_2 = 1.827\times10^{3},\ R_3 = 49.9$$

$$G_{oc} = 4.545\times10^{4},\ \omega_{z1} = 2\pi\cdot2\times10^{3},\ \omega_{z2} = 2\pi\cdot19\times10^{3},$$
$$\omega_{p1} = 2\pi\cdot400\times10^{3},\ \ \omega_{p1} = 2\pi\cdot400\times10^{3}$$

$$G_c(s) = 4.545\times10^{4}\cdot\frac{\left(3.979\times10^{-5}s+1\right)\left(8.377\times10^{-6}s+1\right)}{s\cdot\left(3.979\times10^{-7}s+1\right)^2}$$

(3-8)

Applying bilinear transformation to this response, the discrete time domain response is obtained as well as in Figure 3-8. Since the sampling frequency we choose is 10MHz, there just comes out difference between two responses above 5MHz. The bilinear transformation of transfer function can be expressed in Matlab:

$$[b,a] = bilinear(B,A,fs)$$

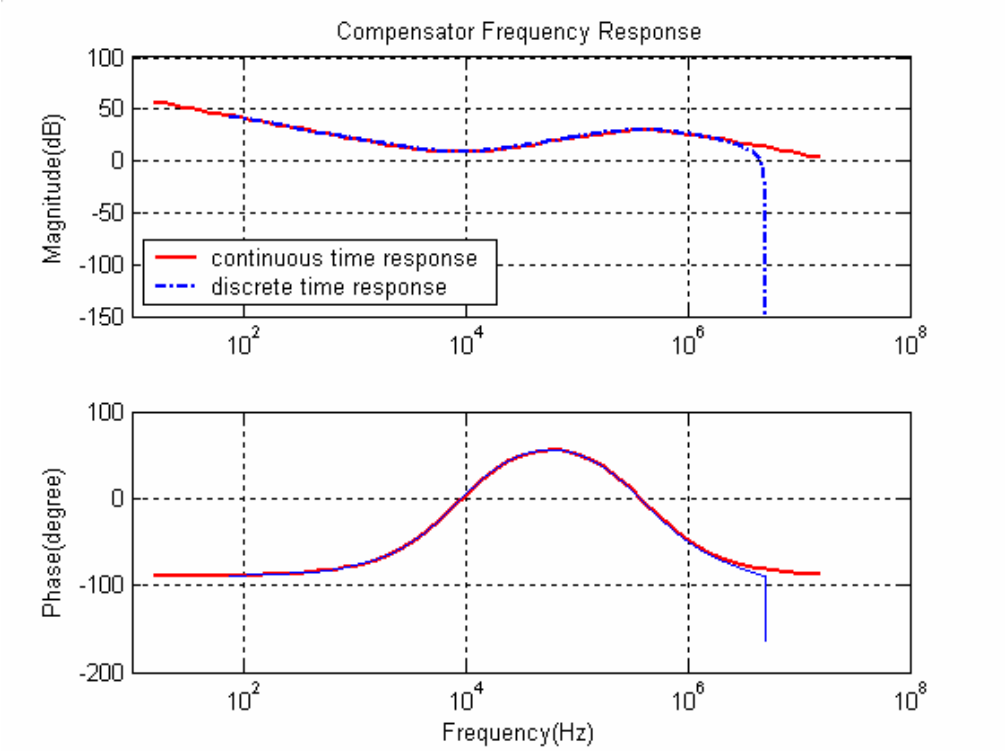


Figure 3-8 Response of continuous/discrete time domain of PID compensator

Then according to the equations, the floating-point values of digital coefficients K_P, K_I, K_D, A_1, A_2, A_3 could be calculated based on the z domain poles and zeros, which are derived from s domain compensator after bilinear transformation.

$$\begin{aligned} kd &= [z(2)\cdot z(1)]; \\ kp &= [z(2) + z(1) - 2\cdot z(2)\cdot z(1)]; \\ ki &= [1 + z(2)\cdot z(1) - z(2) - z(1)]; \\ A_1 &= -p(1) - p(2); \\ A_2 &= p(1)\cdot p(2); \end{aligned} \tag{3-9}$$

$$
\begin{aligned}
kp &= 0.8999 \\
ki &= 0.0025 \\
kd &= 79.3388 \\
A_1 &= -1.5535 \\
A_2 &= 0.6033 \\
A_3 &= 0.0746
\end{aligned}
\tag{3-10}
$$

Construct the digital PID compensator by plug those coefficients into equation. Then the PID, LPF and composite filter response and the whole open loop response are obtained in the compensator graph as shown Figure 3-9.

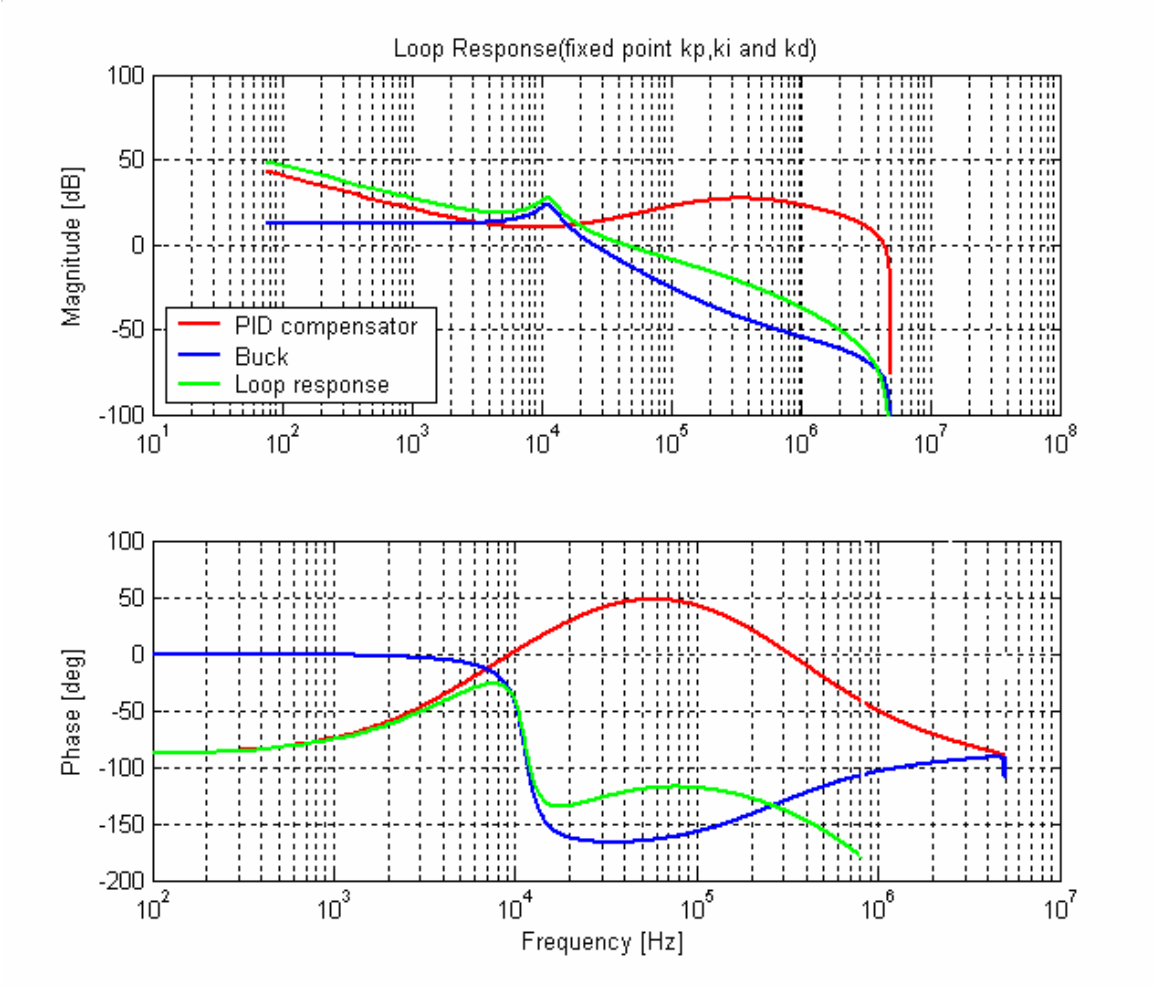


Figure 3-9 PID compensator, Buck stage and designed open loop responses

It can be seen that, after digital PID compensation, the dc gain of loop response has been improved due to the integrator pole and the system BW is 35 kHz, the phase margin is boosted to almost 50^0. As a result, this system has large dc gain for steady state, desired BW and sufficient phase margin for transient response.

3.4 Digital PID Coefficients Optimization and Limitation

3.4.1 Optimization of Digital Coefficients

Once PID digital coefficients are generated from S-domain compensator, it can't be avoided to tweak the compensator parameters to meet the real converter performance. It is possible to change the poles/zeros location in s-domain design and then recalculate the digital coefficients back and forth. So it would be better for designers to directly optimize the digital coefficients and achieve satisfied system response. The analysis on changing digital coefficients is discussed below.

According to equation, K_P, K_I, K_D are only related to the zeros. Figure 3-10 sketches the response changes as K_I change inside its range. It can be seen that as K_I increases, the compensator dc gain and low frequency gain increase and phase degrades more. Therefore, increasing K_I reduces steady state error and lifts bandwidth and short system response time, but cause less stability for system and worse transient response.

Figure 3-11 shows the locus of two S-domain zeros as K_I changes. Apparently if K_I increases, the zero at lower frequency will move towards higher frequency while the higher frequency zero will go opposite to lower frequency. The zero location change brings out the clear explanation on the response gain and phase changes.

One thing to be pointed out is that if K_I is increased too much, the two zeros will turn out to be two complex zeros, which will cause gain overshoot and 180degree phase boost. How much increase of K_I causes complex zeros is related to K_P and K_D values also.

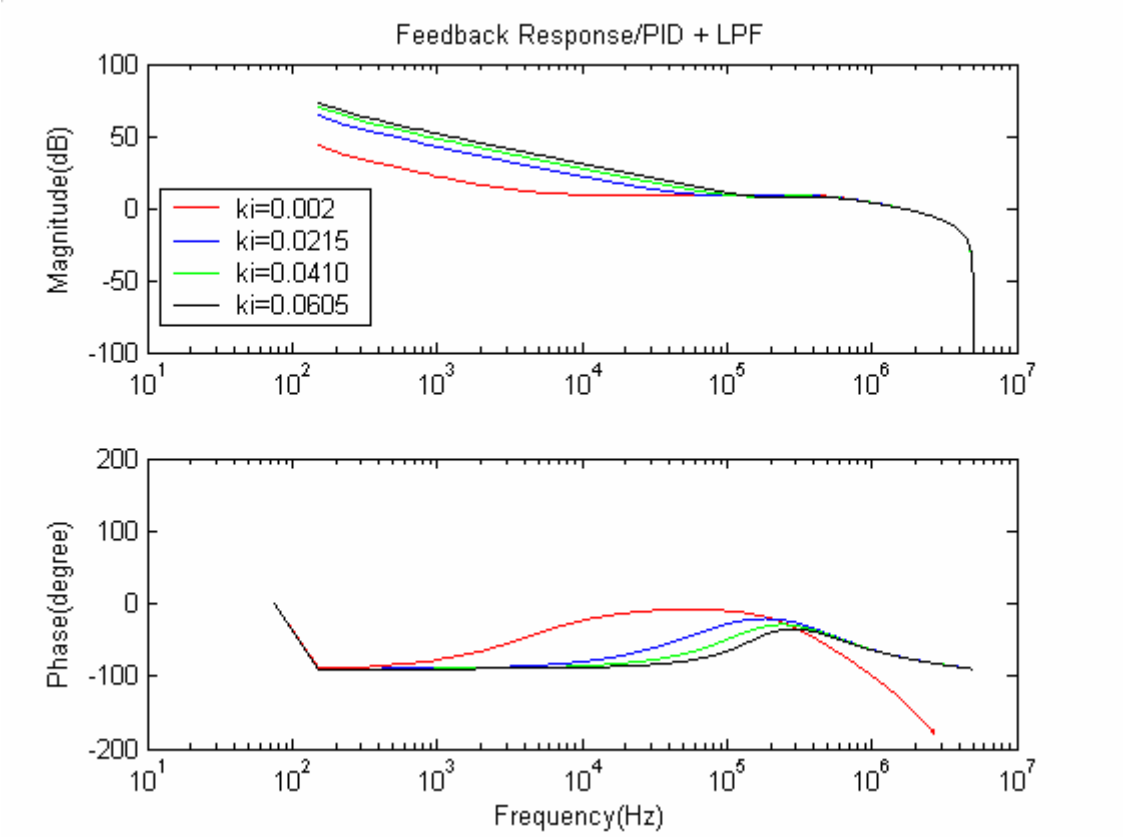


Figure 3-10 Response changes as Ki changing

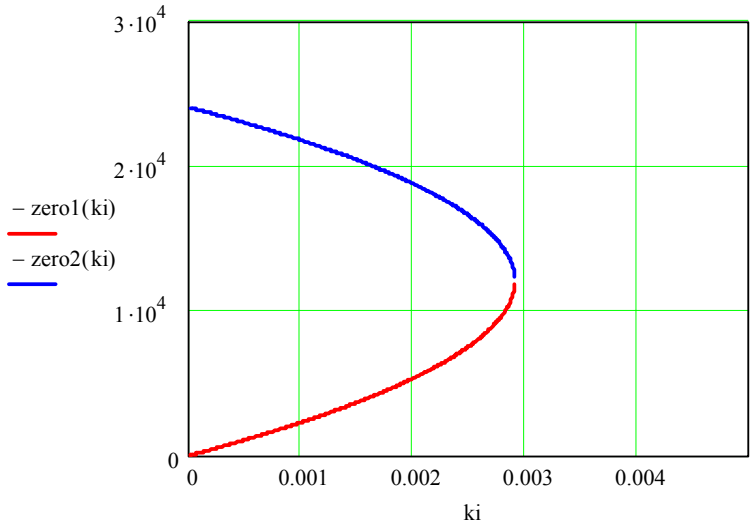


Figure 3-11 Zeros' locus as Ki changing

In general, increasing K_D enhances the effect of differentiation; lift bandwidth and boost phase margin. Therefore system stability is improved and response time is reduced, transient response is getting better. But as the bandwidth gets wider, more noise is introduced into system and it also probably affects system large signal response, such as output voltage ripples. Figure 3-13 shows the locus of two zeros as K_D changes. When K_D increases, lower frequency zero is almost unchanged but the higher frequency zero moves close to first zero promptly. That explains the corresponding gain and phase changes in the response.

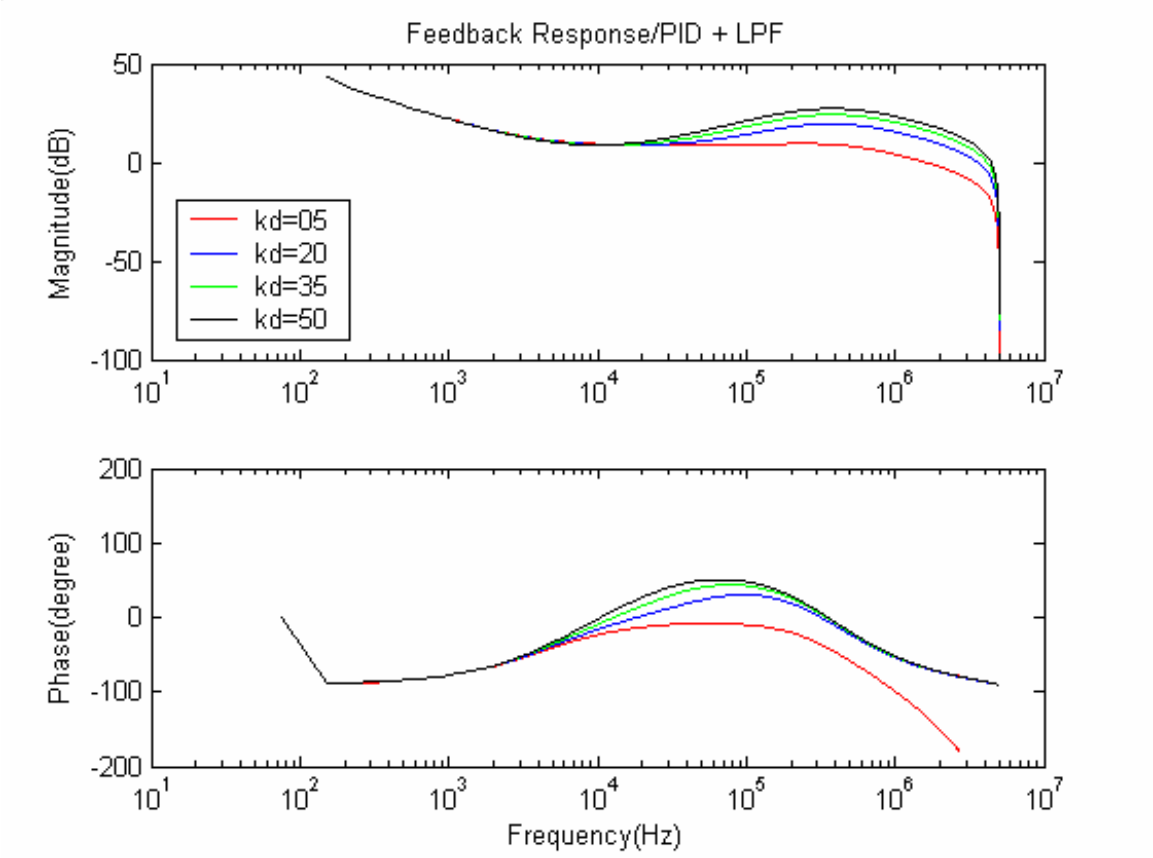


Figure 3-12 Response changes as Kd changing

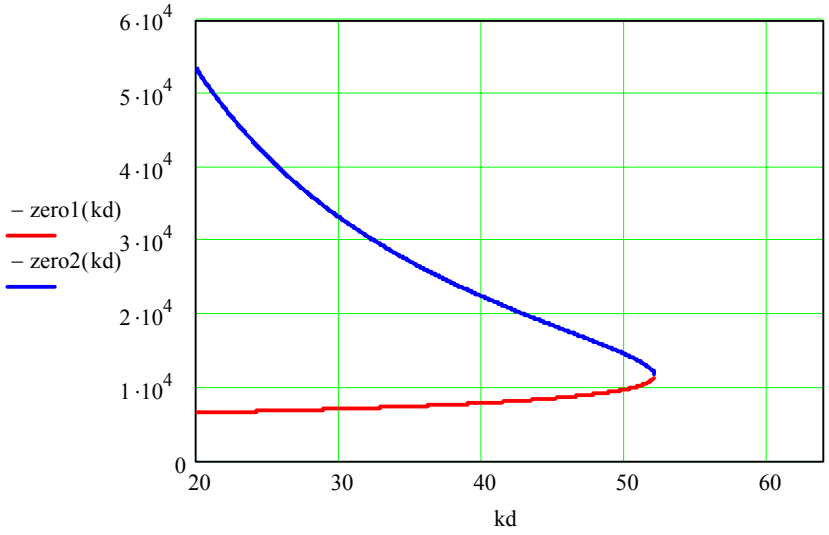


Figure 3-13 Zeros' locus as Ki changing

According to the response figures, the change of K_p almost just affects low frequency gain with little influence on the phase. From the locus of zeros, it can be recognized that the first zero moves to lower frequency promptly, which basically cause the lift of low frequency gain.

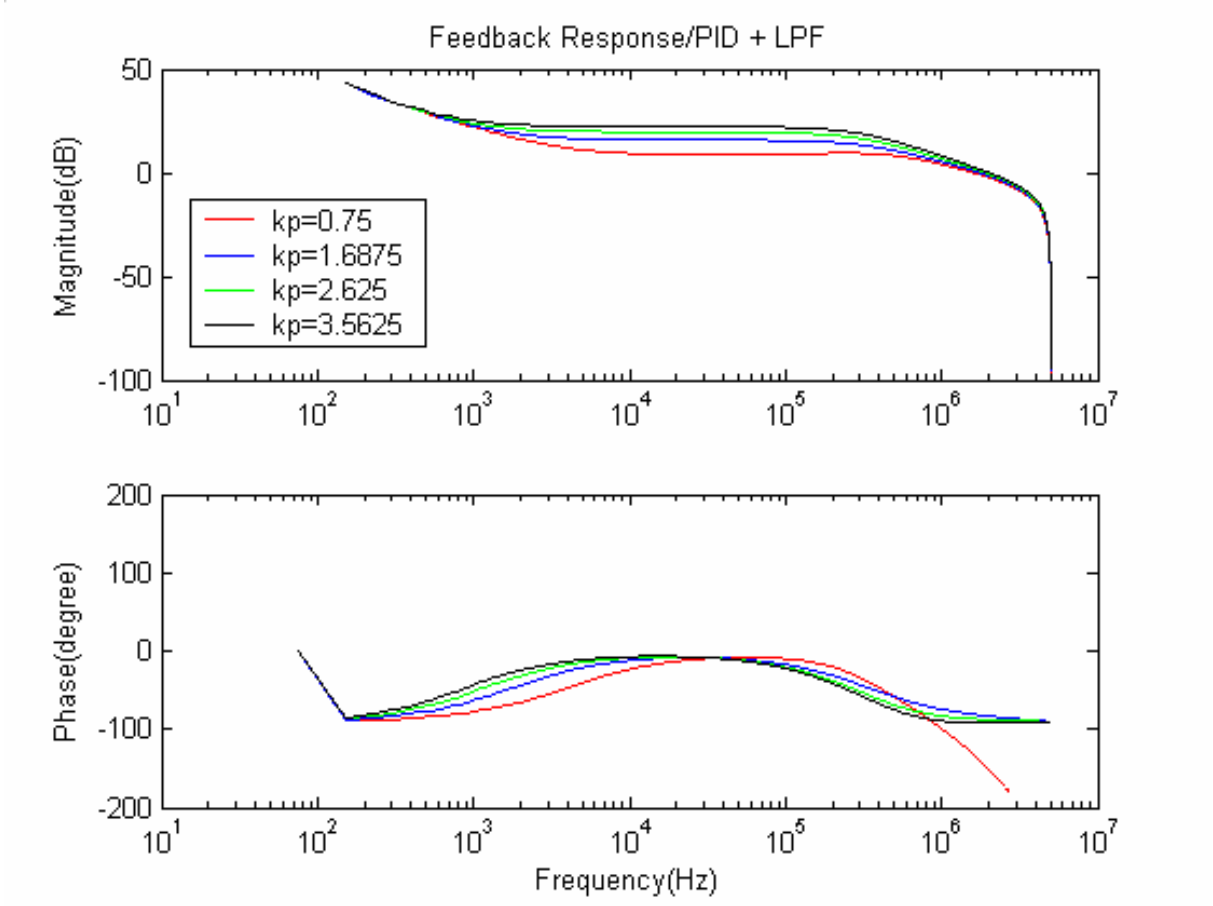


Figure 3-14 Response changes as Kp changing

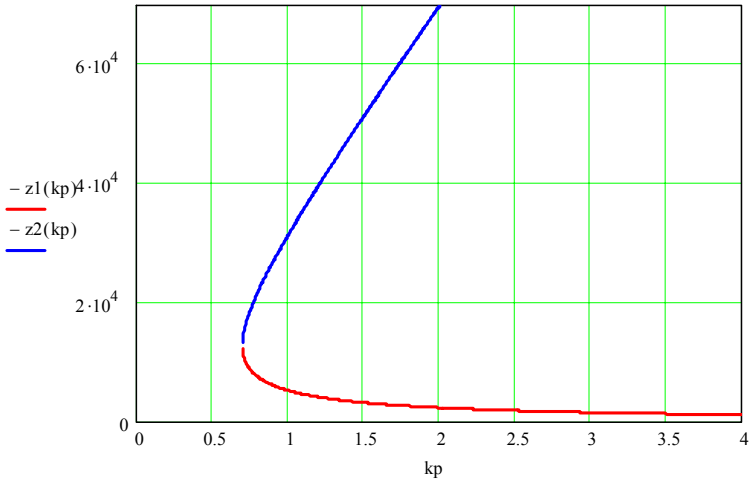


Figure 3-15 Zeros' locus as Kp changing

As we discussed above, A_1, A_2 are only related poles. Figure 3-16/3-17 sketches the response change as A_1, A_2 change. As A_1, A_2 increase, the responses both show gain decreased and phase boost around or outside the bandwidth.

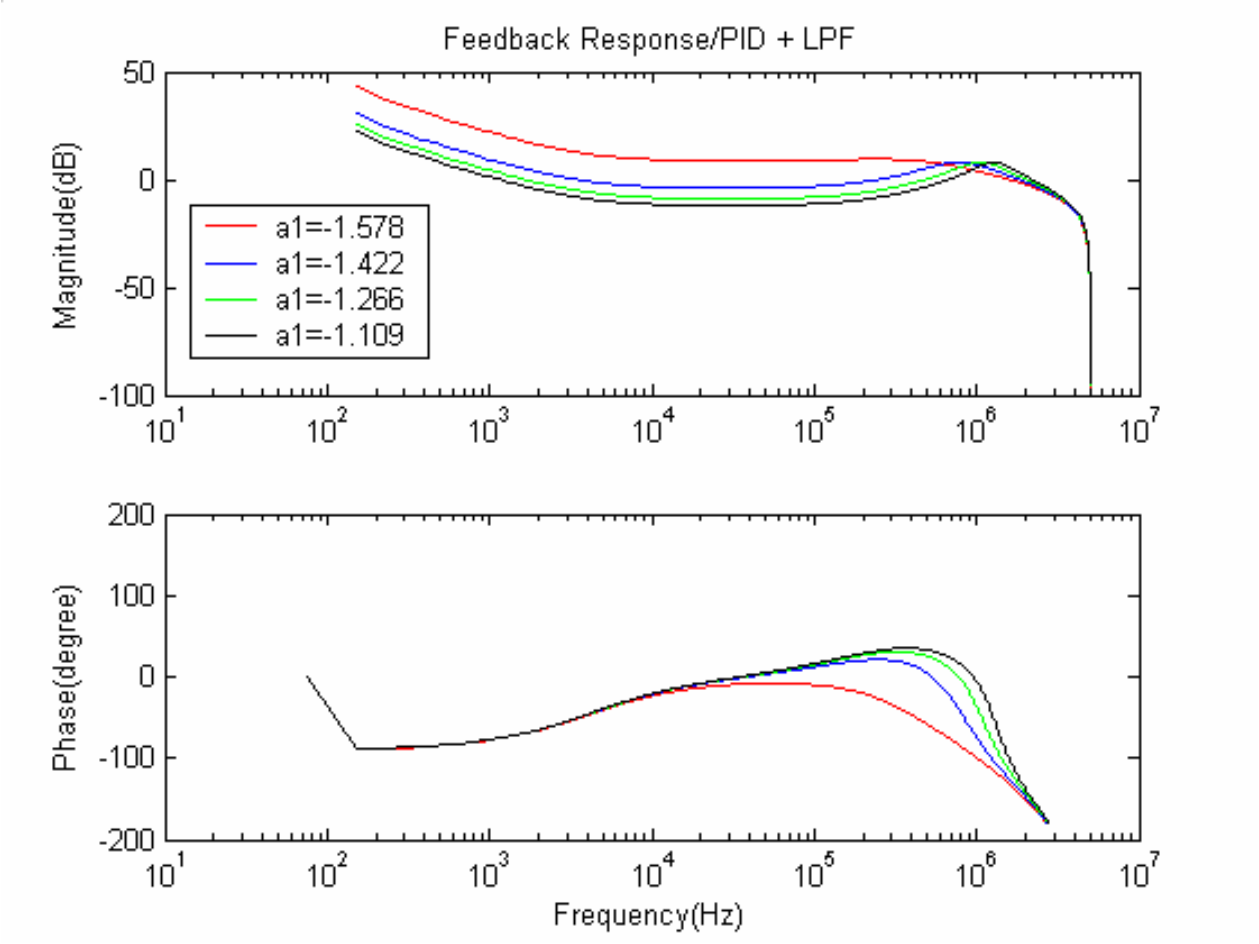


Figure 3-16 Response changes as a1 changing

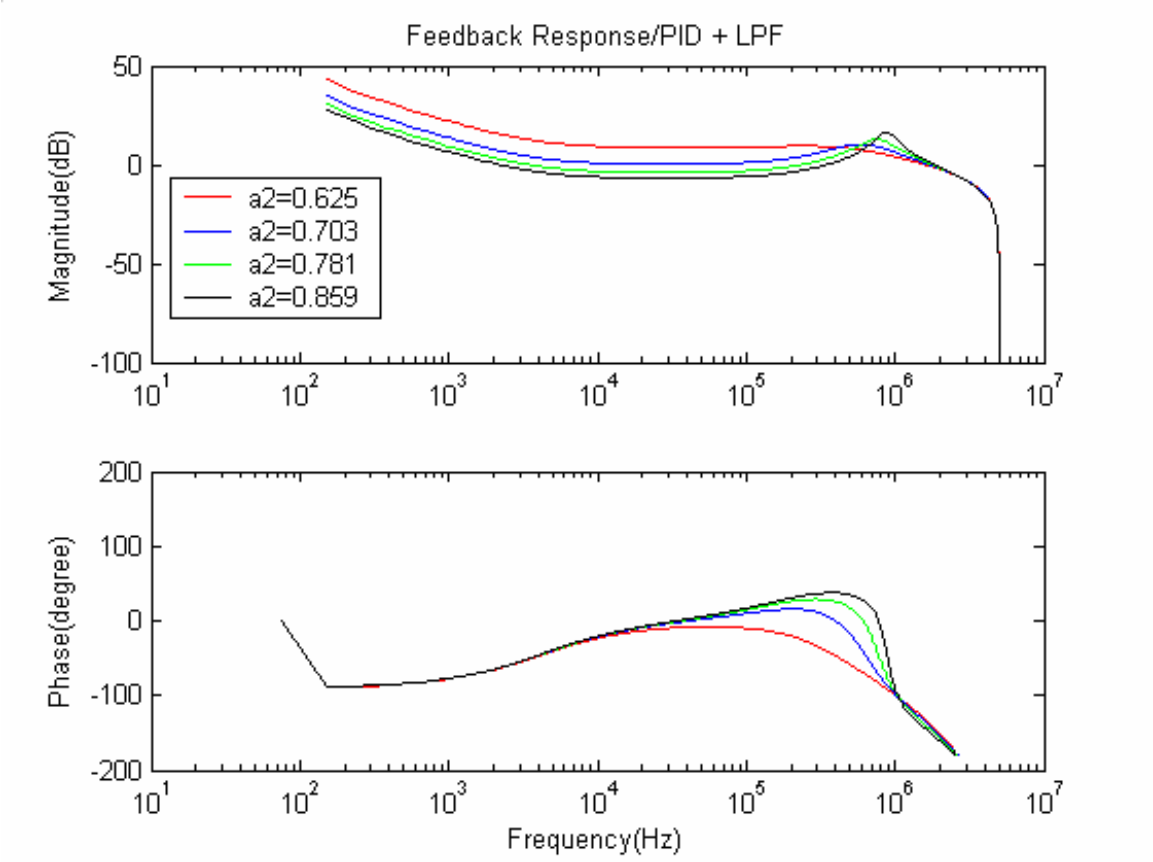


Figure 3-17 Response changes as a2 changing

3.4.2 ADC and DPWM design considerations

In digital controller design, the sensitivity of the ADC converter, inherent time delay of the calculation/sampling and the precision of the numerical value all affect the performance of the system. It is therefore necessary to give careful consideration to ADC sampling frequency and resolution; DPWM resolution, computational delay time, quantization/word length effects and calculation precision [B6~B8].

ADC resolution is determined by the precision requirements of power stages. That is to say, the LSB value of ADC must be smaller than the minimum required output voltage resolution. The sampling frequency of ADC should generally be 10 or 20 times of system bandwidth to minimize phase delay due to sampling.

Meanwhile, generally the dynamic voltage regulation requires that output voltage V_o must always follow reference voltage V_{ref} during load or input voltage transients. As matter of fact, only a small window around Vref is needed to sample. Therefore, ADC converter can be used to sample the error signal instead of output voltage and the resolution can be improved and less bits of ADC converter is required.

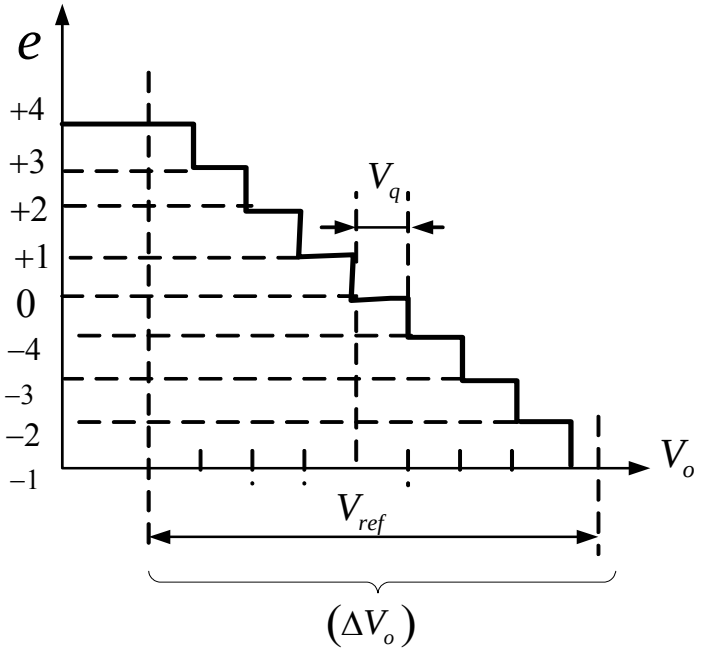


Figure 3-18 ADC conversion characteristic

Figure 3-18 shows the AD conversion characteristic, which indicates that the output voltage is sampled by an AD converter and produces the digital error signal. Vq is the smallest difference corresponding to the least level of ADC analog equivalent voltage difference of LSB. In order to meet the requirement that ADC can sense the smallest change of the output voltage, the Vq should not be greater than the smallest change of output. So the smallest output change that can be distinguished determinates the resolution of ADC.

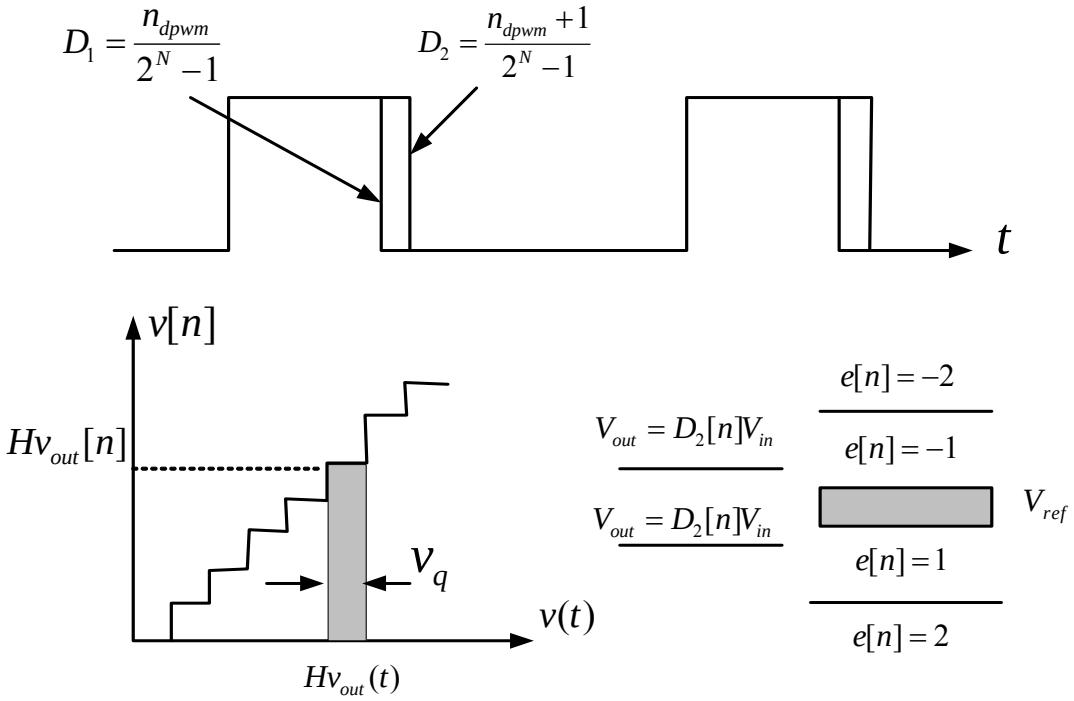


Figure 3-19 Resolution requirement of the DPWM

Another important issue for ADC is to determine the sampling frequency. Theoretically, higher the sampling frequency is better for the system due to less time delay. However, in practice, the cost of hardware implementation and the calculation capability have to be considered. In the discussion of the zero-order hold in the early chapter, we recognize that a sampling frequency must be two times greater than the bandwidth of the system to reconstruct the input without errors. Even at this case, the zero-order hold still introduces significant phase lag into the system. Generally, in order to make the phase delay as small as possible, we pick up the sampling frequency at least 10 times greater than the system bandwidth, which means the phase delay goes to /10 = 180 s w. For a switching power system, one option is to sample at the switching frequency.

In a digital controller, a DPWM acts as a DA conversion to generate pulse width for a switch. Obviously, the minimal time increment of duty ratio depends on N, which is the resolution of DPWM. Because the discrete change of duty ratio causes the discrete change of output voltage, if the smallest change of out Vo caused by the discrete change of duty cycle is greater than the smallest difference of out Vo ADC can be distinguished. This means the DPWM resolution is too low, and in this case, a so-called limit cycle can occur. The basic requirement of the DPWM is that the resolution of DPWM should be greater than the resolution of ADC. Figure 3-20 “Limit cycle” happens when the resolution of the DPWM is too coarse.

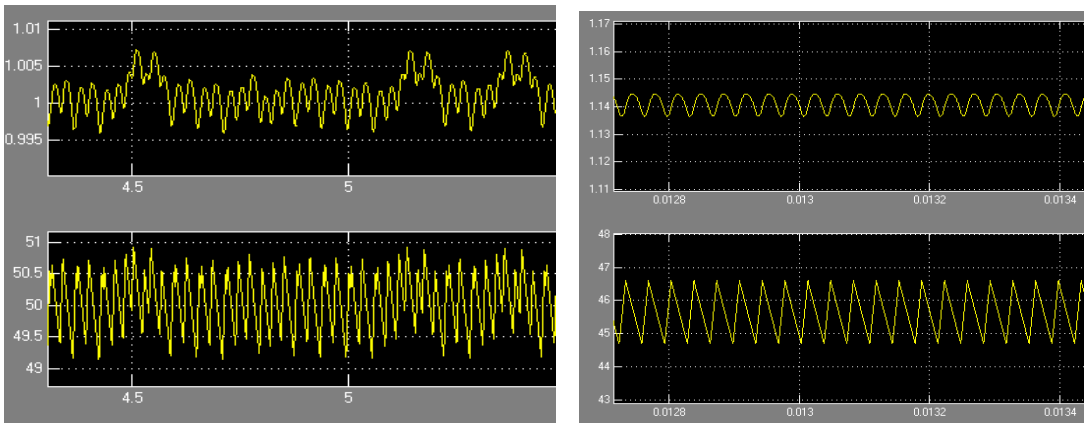


Figure 3-20 "Limit cycle" happens when the resolution of the DPWM is too coarse

3.4.3 Limitation and calculation error of digital coefficients

All of discussions we have done above are based on the consideration of floating point values of digital coefficients. However, in real cases digital PID coefficients have to suffer from limited bit range and limited precision (resolution). Considering the PID hardware implementation feasibility, the data formats and ranges of digital coefficient $K_P,\ K_I, K_D, A_1, A_2, A_3$ are assigned in table.

Table 3-1 Digital coefficient formats and range in digital compensator

Coefficient	Data Format	Range
Kp	xx.xxxx	0 to 3.9375
Ki	.00xxxxxxx	0 to 0.248047
Kd	xxxxxx.	0 to 63
A0	.xxxxxxxx	0 to 0.996094
A1	Sx.xxxxxx	–2 to 1.984375
A2	.xxxxxxx	0 to 0.9921875
A3	.xxxxxxx	0 to 0.9921875

Then following the data formats assigned, the floating point coefficients are converted to fixed-point values and the hex values. Obviously converting from floating fixed point values cause coefficient changes. Meanwhile some of coefficients are limited to maximum or minimum values.

$$\begin{aligned} kp &= 0.8750 \\ ki &= 0.0020 \\ kd &= 63.000 \\ A_1 &= -1.5625 \\ A_2 &= 0.6016 \\ A_3 &= 0.0703 \end{aligned} \Rightarrow \begin{aligned} kp &= 0.8999 \\ ki &= 0.0025 \\ kd &= 79.3388 \\ A_1 &= -1.5535 \\ A_2 &= 0.6033 \\ A_3 &= 0.0746 \end{aligned} \Rightarrow \begin{aligned} kp &= 0x0\mathrm{E} \\ ki &= 0x01 \\ kd &= 0x3F \\ A_1 &= 0x9C \\ A_2 &= 0x4D \\ A_3 &= 0x17 \end{aligned}$$

Therefore here comes out one of big concerns in digital control design. The range limits of the digital coefficients will probably cause the compensation response deviation and the

precision limits may come up with the coefficients calculation error. Some points regarding the error and limits are discussed below.

For example, if the frequency locations of two poles are too low, the requirement for the A1 and A2's precision will be very high. In this case it probably causes compensator response error due to the precision loss during the coefficients converting from floating point to fix point numbers. Therefore, precision and limitation of digital coefficients need be considered carefully while the hardware resources are limited.

Assuming PID coefficients are following the data formats in table. Then let's have a look at the response deviation due to the precision loss and data limitation.

Figure 3-21/22 illustrates compensator errors due to low frequency poles. Figure 3-21 is the case of poles at 150 kHz and the response based on floating point (blue curves) and fix point number (red curves) are almost the same except a little difference on the phase. In Figure 3-22 two poles are placed at 80 kHz, the precision loss of coefficients due to fix point number calculation causes two complex poles at 80 kHz, which generates overshoot of gain and phase shown in the Figure 3-22. And the lower frequency the poles locate, the more overshoot on gain and phase responses will be caused.

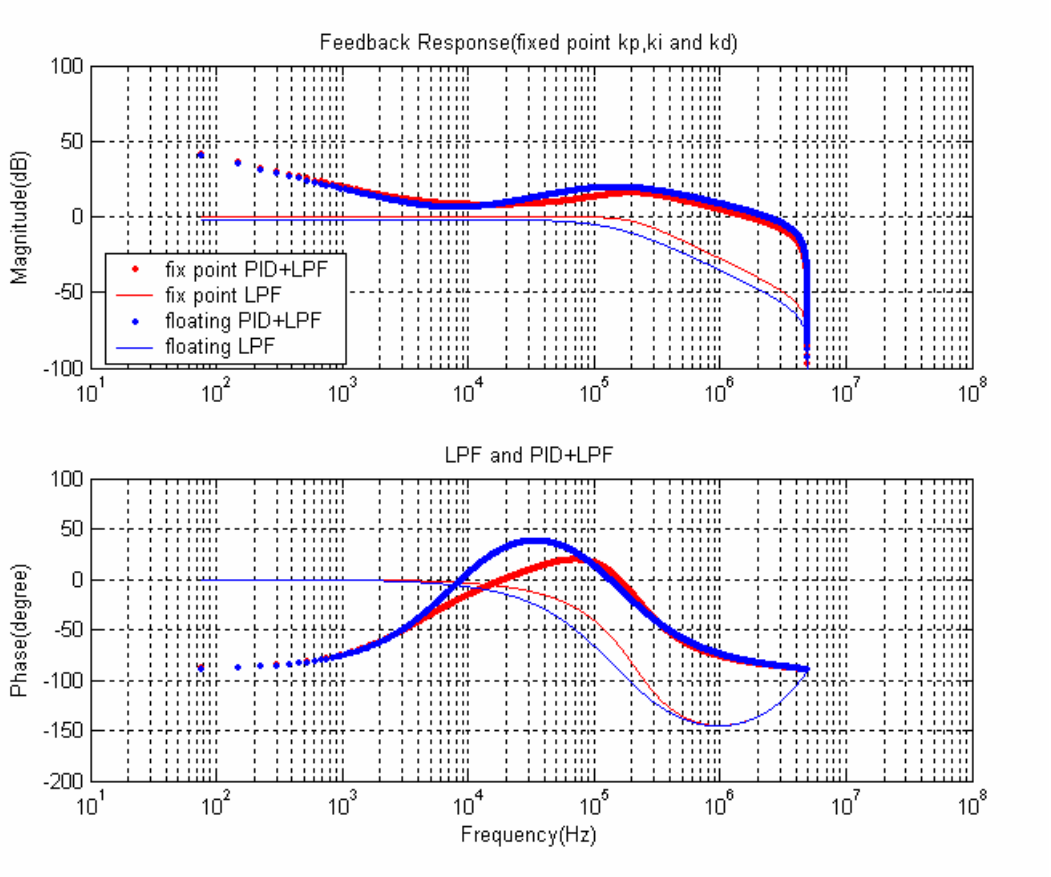


Figure 3-21 fp1=fp2=150K

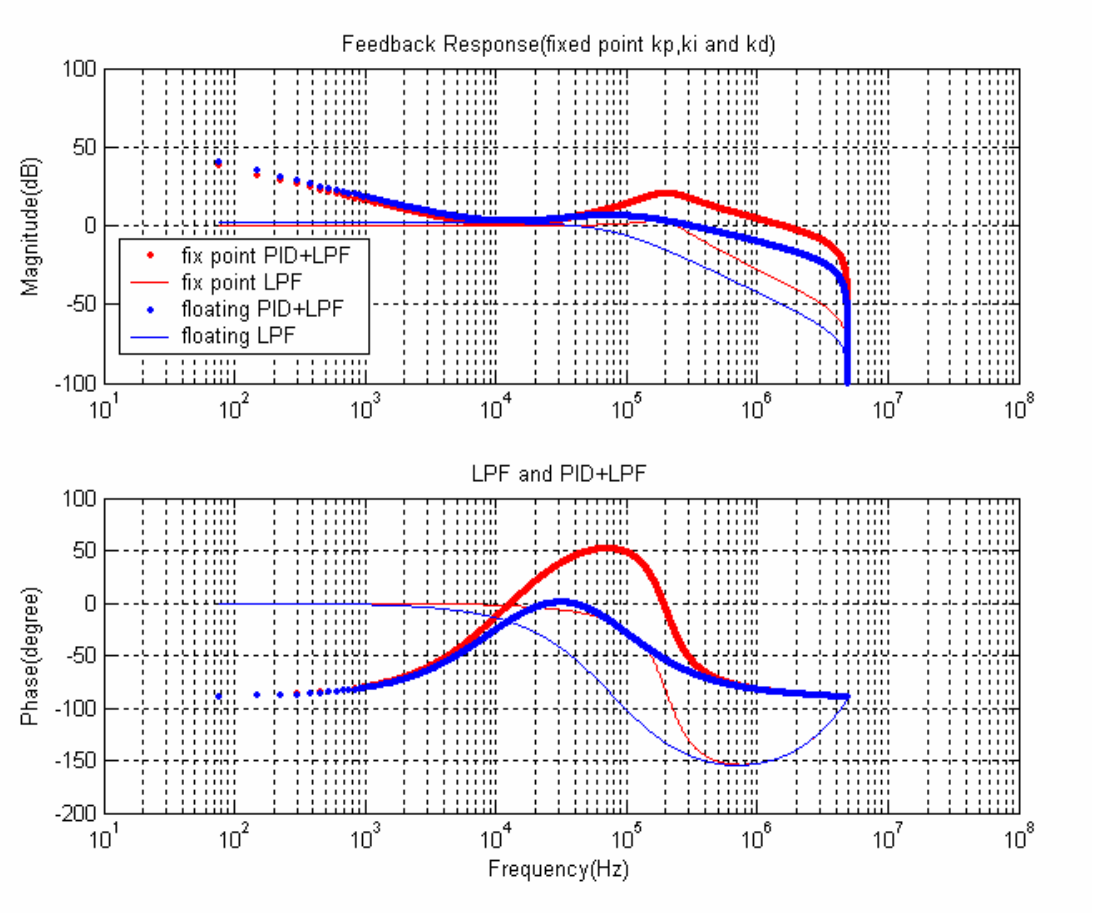


Figure 3-22 fp1=fp2=80K

The location of zeros basically determinates the K_P, K_I, K_D. Since K_P, K_I, K_D all have the specified range and resolution, too low frequency zeros will cause the compensation error. To be specific, if zero locates at too low frequency, coefficients K_P, K_I are probably too small to be in the range. In this case, simulation file will adjust K_I to the minimum value to maintain the integration attenuation at low frequency and increase K_P, K_D with the same ratio to keep gain unchanged. This process will introduce K_P, K_I, K_D errors and cause all compensation error correspondingly.

Figure 3-23 show the accurate compensator responses for floating point and fix point coefficients when place two zeros at 8 kHz. And Figure 3-23 and Figure 3-24 illustrate the compensation response errors when one of zeros is placed at 2 kHz.

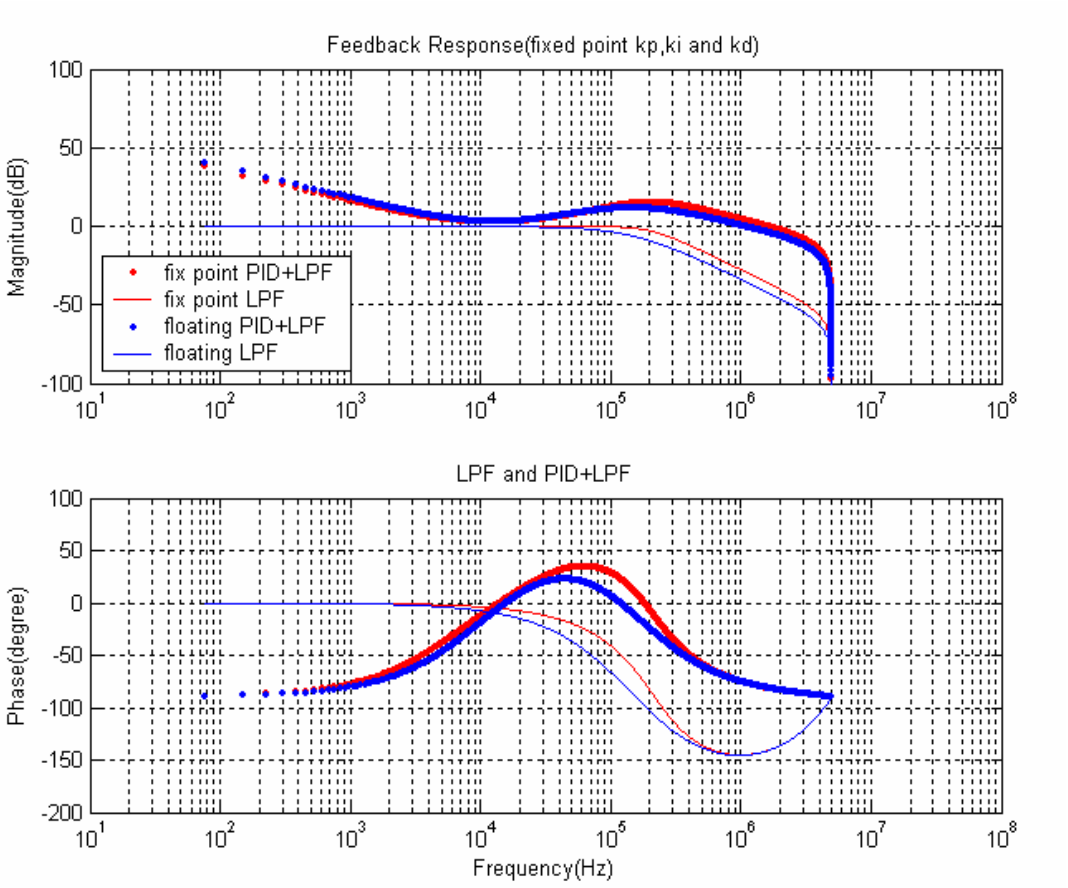


Figure 3-23 fz1=fz2=8K

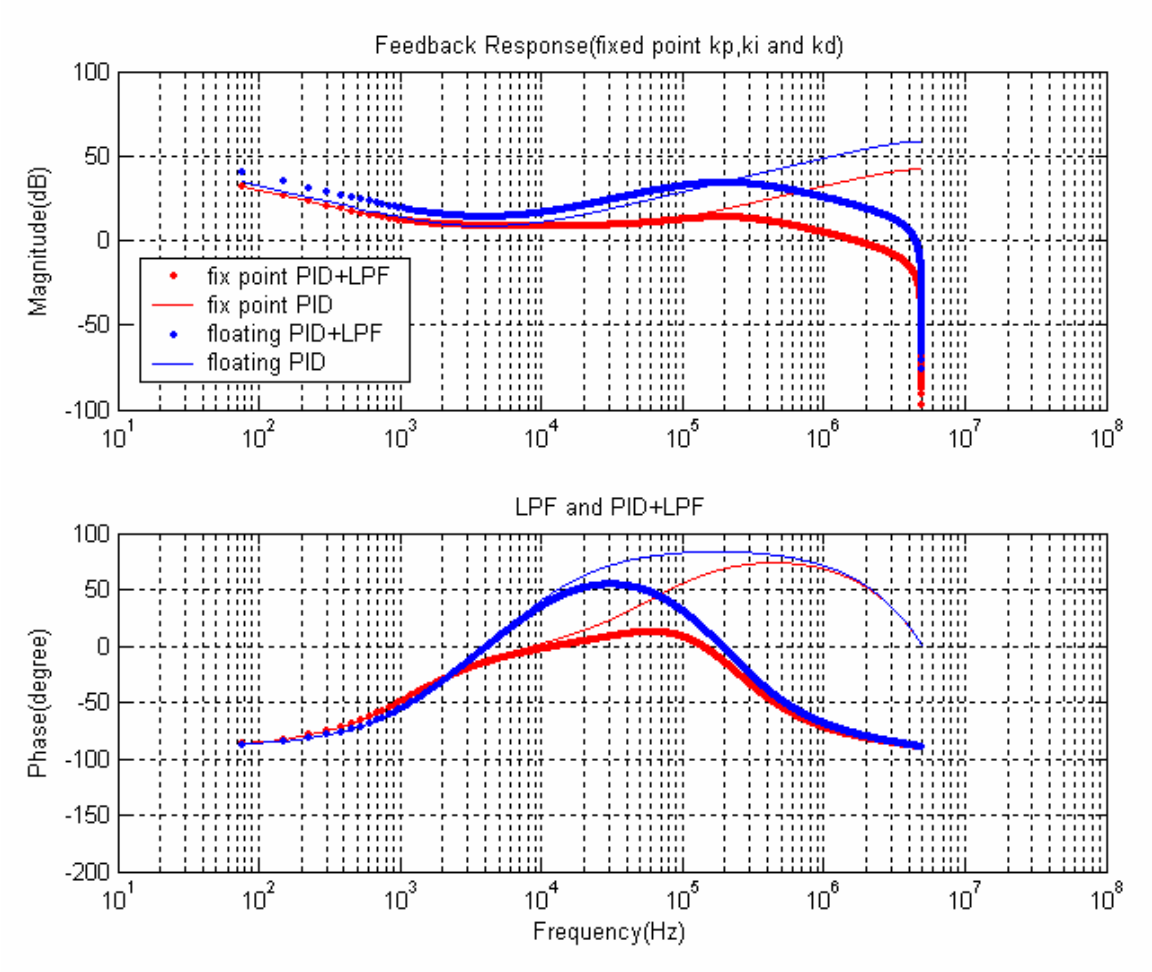


Figure 3-24 fz1=2K fz2=8K

3.5 Digital controller Si8250 introduction

3.5.1 Si8250 overview

Si8250 is a dedicated mixed-signal integrated circuit implemented in low-cost CMOS technology optimized for dc-dc and ac-dc converter applications. Figure 3-25 is showing the architecture of Si8250. The device is partitioned into a power supply specific hardware block DSP to provide a high bandwidth, fully independent digital control loop function and a software programmable system management processor section to provide system functionality. The hardware block control path includes a high-speed differential ADC, a voltage-reference DAC, a programmable infinite-impulse response compensator and a six-phase DPWM finite state machine. The reference DAC, ADC and compensator together generate a duty cycle control signal to modulate six independently controlled phase outputs of the DPWM. Protection circuits providing cycle-by-cycle current limiting and fault detection are integral parts of the hardware digital control loop. The system management processor section provides an instruction-based engine, including an 8-channel self-sequencing ADC, a 50 MIPs 8051-based MCU, four 16- bit timers and other system peripheral I/O. They together provide system initialization, control loop optimization, fault recovery, housekeeping, communication interface, soft start/stop and other user-defined functions. Other system functions include a high-precision (2.0%) oscillator, PLL clock multiplier for providing all necessary clocks to DSP and MCU, program storage non-volatile memory for user-defined program, UART and GPIO ports. To facilitate interfacing between two processors, there are provided monitor registers and configuration registers [B14]

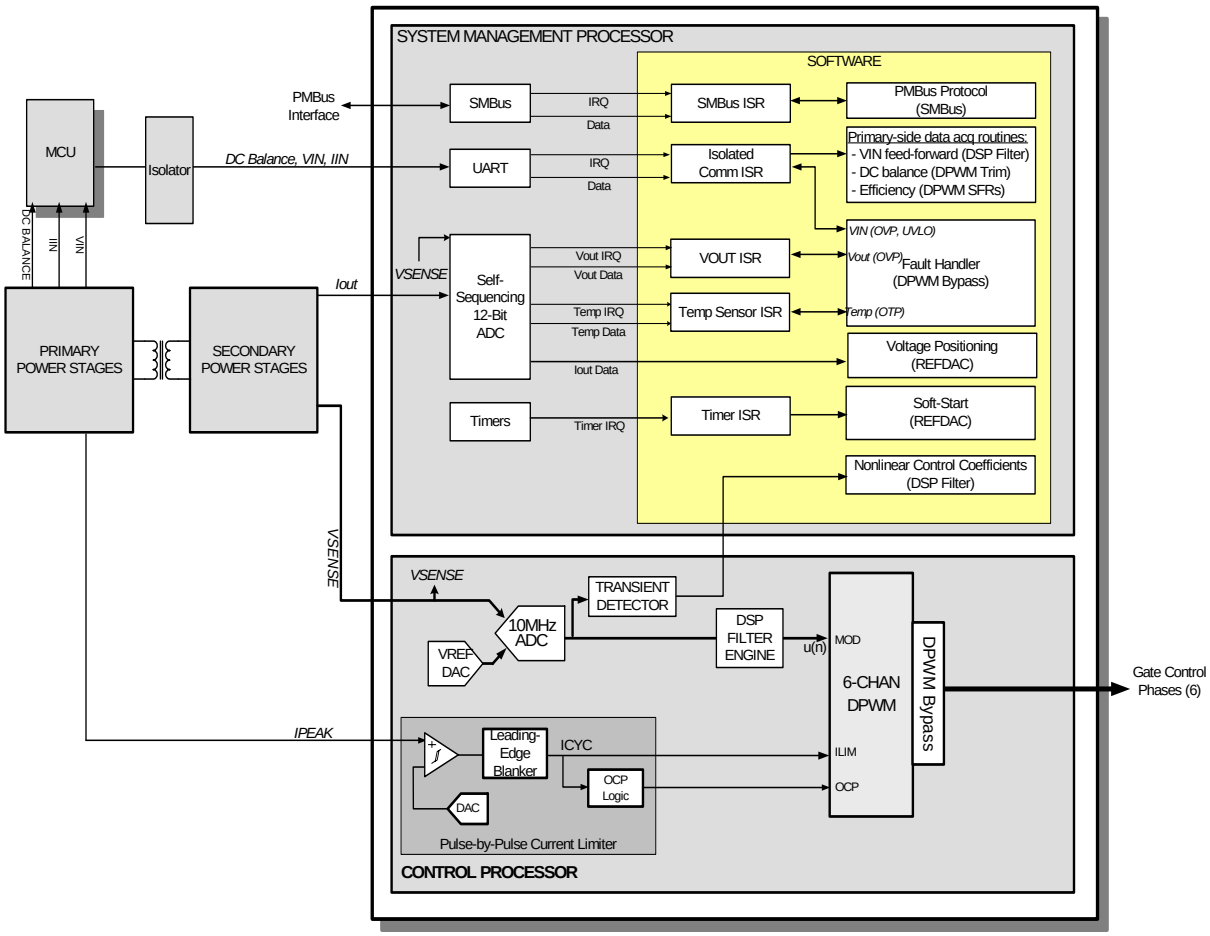


Figure 3-25 Si8250 block diagram

The Silicon Laboratories Si825x architecture is similar to analog voltage mode control. Like the analog counterpart, output voltage is subtracted from a reference voltage by a "digital error amp" consisting of a differential input analog-to-digital converter (ADC) and a digital filter. Digital error term u(n) is analogous to the analog error term VERROR in Figure 3-25. The

digital PWM (DPWM) is analogous to an analog PWM in that output duty cycle is a function of the compensated error variable u(n). Like many analog controllers, there is a dedicated pulse-by-pulse current limiter that terminates the on-going portion of the active PWM waveform when current reaches the maximum allowable value.

3.5.2 System operation

Figure 3-25 also shows typical hardware connections for a Si825x-based power delivery system. With Si8250/1/2 controlling power converters operating in digital voltage mode control, the output voltage signal connects to the VSENSE input through a resistive divider, limiting the common mode voltage range applied to ADC1 to a maximum of VREF. The equivalent resistance of the divider and the capacitor form an anti-aliasing filter with a cutoff frequency equal to ADC1 sampling frequency of divided by 2 (the amplitudes of frequencies above fs/2 must be minimized to prevent aliasing). Differential ADC1 and the DSP Filter Engine together perform the same function as an analog error amplifier and associated RC compensation network. ADC1 digitizes the difference between the scaled output voltage and a programmable reference voltage provided by the REFDAC. The ADC1 output signal is frequency compensated (in digital domain) by the DSP Filter Engine. The resulting output from the DSP Filter Engine is a digital code that represents the compensated duty cycle ratio, u(n). The digital PWM generator (DPWM) directly varies output timing to the external gate drivers based on the value of u(n) until the difference between VSENSE and ADC1 reference level is driven to zero. Sensing circuitry within the power stages (current transformer, sense amp, etc.) provides a signal representative of inductor or transformer current. This signal connects to the pulse-by-pulse

current limiting hardware in the Si8250/1/2 via the IPK input pin. This current limiting circuitry is similar to that found in a voltage mode analog PWM. It contains a fast analog comparator and a programmable leading-edge blanking circuit to prevent unwanted tripping of the current sensing circuitry on the leading edge of the current pulse. Current limiting occurs when the sensed current exceeds the programmed threshold. When this occurs, the on-going active portions of the PWM outputs are terminated. A programmable OCP counter keeps track of the number of consecutive current limit cycles, and automatically shuts the supply down when the accumulated number of limit cycles exceeds the programmed maximum [B15].

The System Management Processor is based on a 50 million instruction per second (MIPS) 8051 CPU and dedicated A/D converter (ADC0). ADC0 digitizes key analog parameters that are used by the MCU to provide protection, as well as manage and control other aspects of the power system. On-board digital peripherals include: timers, an SMBus interface port; and a universal asynchronous receiver/transmitter (UART) for serial communications, useful for communicating across an isolation boundary.

The System Management Processor serves several purposes, among these are:

- Continuously optimizes Control Processor operation (e.g. efficiently optimization).
- Executes user-specific algorithms (e.g. support for proprietary system interfaces).
- Provides regulation for low-bandwidth system variables (e.g. VIN feed-forward).
- Performs system fault detection and recovery.
- Provides system housekeeping functions such as SMBus communication support.
- Manages external device functions (e.g. external supply sequencing, fan control/monitoring).

3.5.3 ADC and Reference DAC

The control loop front end, shown in Figure 3-26, is comprised of a differential input, 6-bit 10MHz Flash ADC with programmable LSB size. It digitizes the difference between the sense output voltage, VSENSE, and the programmable voltage reference with a programmable resolution ranging from 2mV to 24mV. This range allows the ADC to modify control loop gain on the fly and prevents limit cycle oscillation. The digitizer captures sensed output voltage up to 25 times in a 400 kHz switching cycle to reduce control loop latency. Figure 3 illustrates how the pulse duty cycle is extended momentarily to react to output voltage drop [B14].

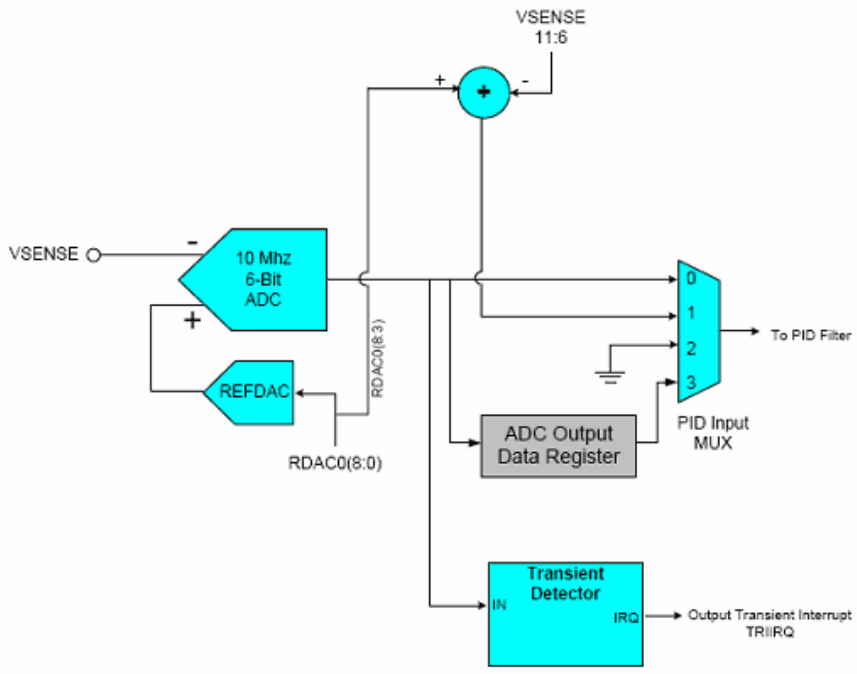


Figure 3-26 10M control processor ADC

The transient detector monitors the output of the ADC at a 0.1uS interval and asserts a transient interrupt when the absolute value of the ADC output exceeds the limits of a predefined value. The response to a transient detector interrupt can be programmed to increase the loop gain, reconfigure the pulse waveform or control mode switching. The set point of the power supply is defined by the output of a 9-bit reference DAC. The reference DAC includes an internal band-gap voltage reference with 0.5% accuracy over a temperature range of -40 to 125ºC. An external voltage reference may be connected to the VREF pin to attain a better accuracy and the internal reference disabled by a configuration register. The reference DAC provides a 1.8MHz bandwidth and 2uS settling time useful for power supply soft starts and power factor correction. The DAC also has 2.4mV resolution at a 1.25V voltage reference. The reference DAC can also be used for dynamic voltage positioning and power factor correction, which will be described in the application sections. A 4-channel MUX provides the system management processor section the ability to route one of multiple different analog inputs to the digital controller section. Channel 0 is the output of ADC. The sampling rate of the DSP is automatically adjusted to the sampling rate of the ADC to perform high-speed control loop operation. Channel 1 comprises the difference between VSENSE (as measured by a 12-bit ADC).

3.5.4 Si8250 filter engine

Si8250's loop filter engine provides a hardware digital compensation platform to realize the digital control loop design for high switching power converters. Differenced from programmed difference equations in most of cases of digital control implementation, Si8250's

hardware PID compensator exhibits the specialty of high-speed response, and it is still allowed to program by setting up the digital coefficients registers. So based on Si8250 digital compensator platform, digital PID strategy and some optimization approaches can be verified and realized [B11~B13].

Si8250 DSP filter engine consists of a first-stage PID filter and second-stage low-pass filter. All coefficients in this filter engine are dynamically programmable enabling the system management processor to optimize loop response as load conditions change.

One of two second-stage low-pass filters can be selected by software: a two-pole low pass that is updated at 10 MHz or a single switching cycle "quiet mode" SINC decimation filter that generates zeros at frequency intervals equal to fs/(2 x Decimation Ratio). The decimation ratio should be chosen to place a zero at the PWM frequency for the maximum attenuation of the PWM frequency component.

The composite filter (PID and LPF) provides up to three poles and three zeros, while the composite filter (PID and SINC) provides one pole and multiple zeros. Figure 3-25 is a block diagram of the DSP filter engine. This PID compensator structure happens to be the same as what discussed about in previous sections (except SINC filter).

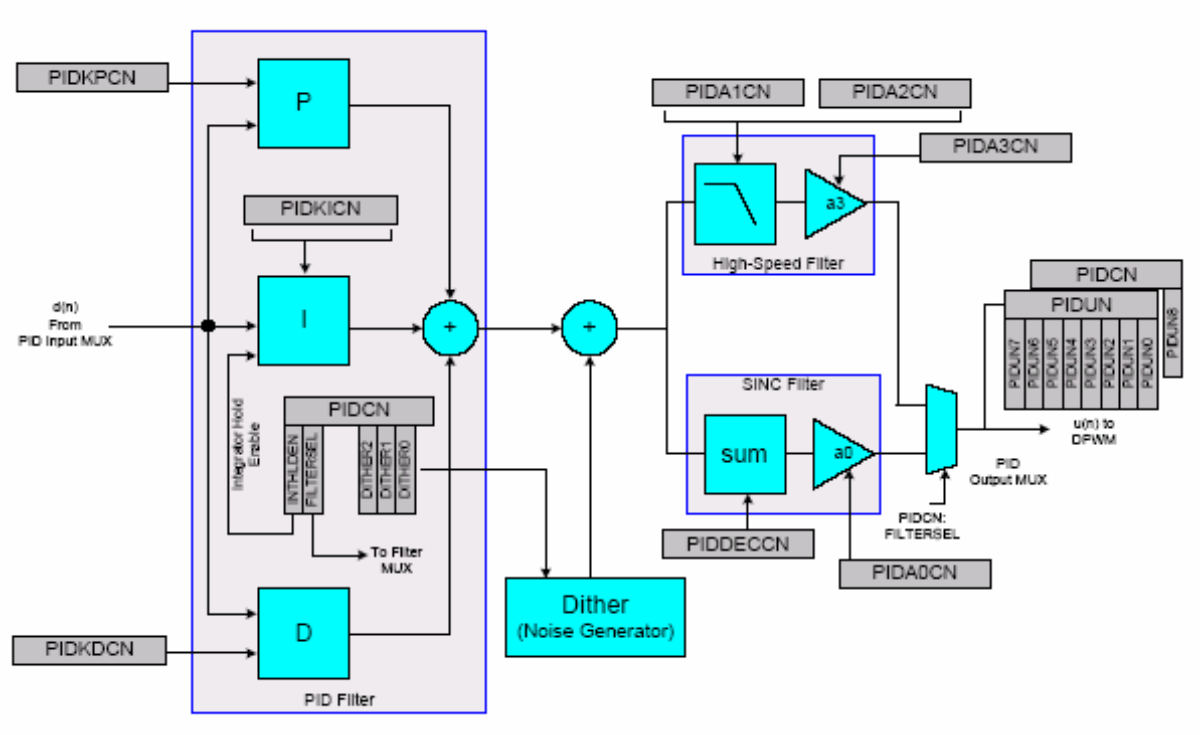


Figure 3-27 Si8250 digital filters

3.5.5 DPWM

The DPWM generates up to six timing phases that can be hardware or software modulated in real time. The DPWM is designed to accommodate an isolated or non-isolated power supply topology, which provides the user the flexibility to apply different phase modulation schemes to the power supply. The flexibility of the DPWM relies on the fact that phase-to-phase timing can be programmed for a fixed dead time, or the system management processor section can dynamically vary the dead time during converter operation to account for temperature, loading and input voltage variation. The DPWM can be clocked at 25MHz, 50MHz or 200 MHz [B14].

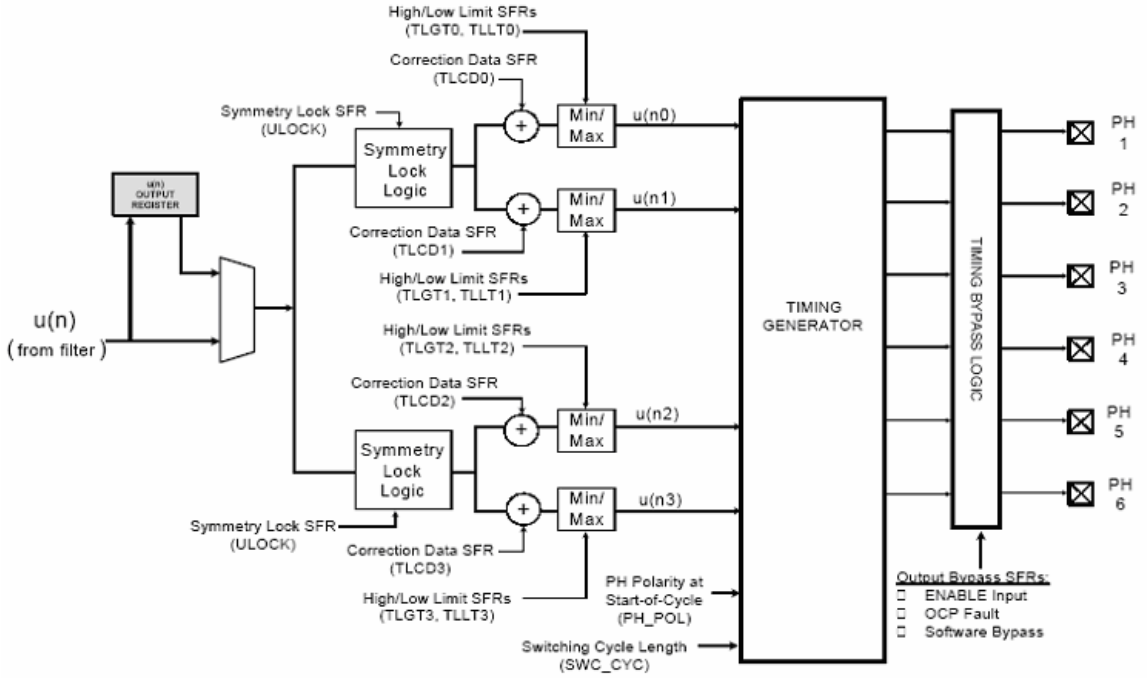


Figure 3-28 DPWM block diagram

As shown in Figure 3-28, the main input of the DPWM is u(n) from the compensator output MUX, this value representing a duty cycle. The multiplexer, the DPWM input MUX, selects either the output of the DSP filter or a software generated output from the system management processor section as the DPWM modulation source. The MUX input is connected to a pair of registers to control a symmetry locking function. This symmetry locking function is useful in applications where the duty cycle of the DPWM is slaved to a selected master pulse. The symmetry lock output is connected to a plurality of limiter circuits which allows the system management processor section the ability to offset and set limits of u(n), which results in setting minimums and maximums for the duty cycle of the output gating pulse. This results in up to four

individual corrected u(n) functions. The heart of the DPWM is a finite state-machine (FSM) based timing generator, each edge of each phase of the DPWM having a separate FSM provided for the control thereof. Each edge of each phase output of DPWM has a timing dependency on any of the other DPWM phases or on itself. The dependency is set up by initiation of individual configuration registers for each FSM. Once initialized, the input to each FSM is hardware-modulated to select from one of the four corrected u(n) functions, and each u(n) can be fed into the timing generator of each FSM. Positive, negative or MCU-controlled phases, overlapping or non-overlapping, can be implemented with this architecture.

Each edge of each phase of DPWM is controlled by one of either a u(n)-modulated, an absolute or a relative command to construct the output pulse of each phase. By providing this FSM-based architecture, each edge of each phase output pulse can be defined separately so as to generate the associated edge virtually independent of the other edges. With such an architecture based in hardware, each FSM decision requires only one or two clock cycles as compared to an instruction-based engine. Phase output bypass logic provides safe stop states for all phase outputs in the event of a predetermined existing condition. When this predetermined condition occurs, the bypass logic overrides the DPWM output by forcing each phase output into user-defined states during power supply shutdown, thus placing the power supply in a "known safe state." The bypass logic can be programmed to occur automatically during over-current protection or when an external pin is enabled. The bypass operation can also be initiated by the system management processor section in software. Each of these bypass conditions has an associated programmable stop pattern.

3.5.6 System Management Processor

The system management processor section, shown in Figure 3-25, implements a standard 8051 organization and peripherals. The MCU core employs a pipelined architecture that executes most if its instructions in one or two system clock cycles; and the MCU is capable of running at 50MHz, and has a peak throughput of 50MIPs.

The analog front-end of the MCU consists of a 12-bit, 200ksps ADC and associated auto sequencing logic, limit registers and temperature sensor. The ADC has 8 input channels, and each channel has a corresponding output register and limit detector. The limit detectors compare the converted output to user-programmed limits and generate an MCU interrupt when these limits are exceeded. The ADC is also equipped with auto sequencing logic, which does not require MCU supervision during data conversion. The auto-sequencing feature automates the analog data acquisition process and enables system protection functions, such as input over-voltage protection, input under-voltage lockout, output voltage monitoring and over-temperature protections, to be implemented in firmware. The MCU has an internal temperature sensor, which monitors chip temperature from -55C to 125ºC. The temperature monitoring is also useful in providing necessary compensation to optimize power efficiency of switchers and gate drivers.

The system management processor section also features four counter/timers for use with device peripherals or for general-purpose use. Other system functions include a high-precision oscillator, a PLL-based clock multiplier, a UART and two GPIO ports.

3.6 Digital controller design implementation – Single-phase POL converter

3.6.1 Hardware and specification overview

POL (point of load) converter is the closest dc-dc power stage to the end load. A product demo board of single-phase POL converter with specifications of 10-15V input and 3.3V/20A output, controlled by the digital controller based on Si8250, is developed by the dissertation author. The design and development are based on the previous analytical results. The simplified schematic of the POL demo board is shown in Figure 3-30, and the top and bottom views of the demo board are shown in Figure 3-29. The Si825x single-phase POL design implements a digitally-controlled POL with a DPWM switching frequency of 391 kHz. The Si8252 single-phase POL target board contains system power stages and digital control circuits with debug connectors for the Si8250 digital power controller. The user can also access and control the target board using SMBus. Table 3-1 is showing the specifications of Si8250 single-phase POL board.

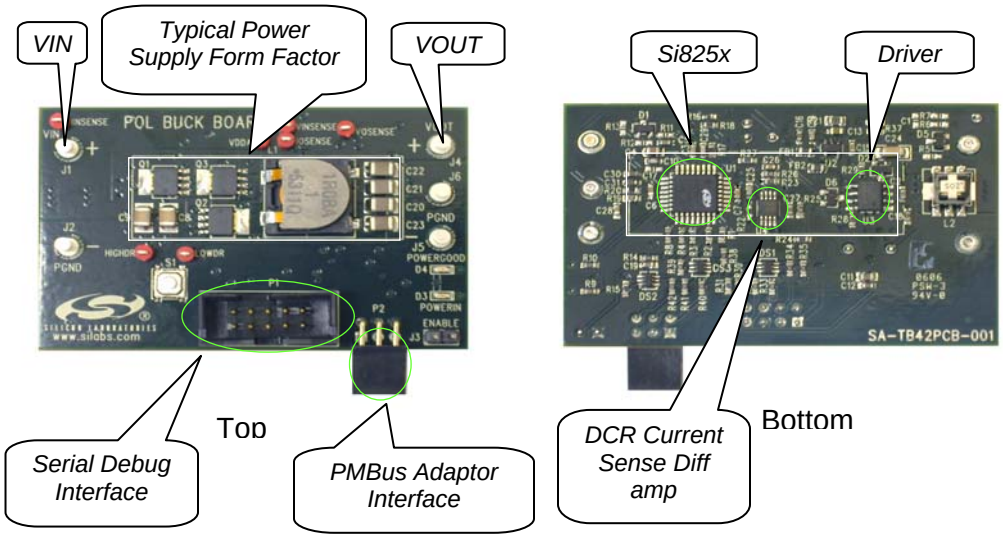


Figure 3-29 Single-phase POL demo board

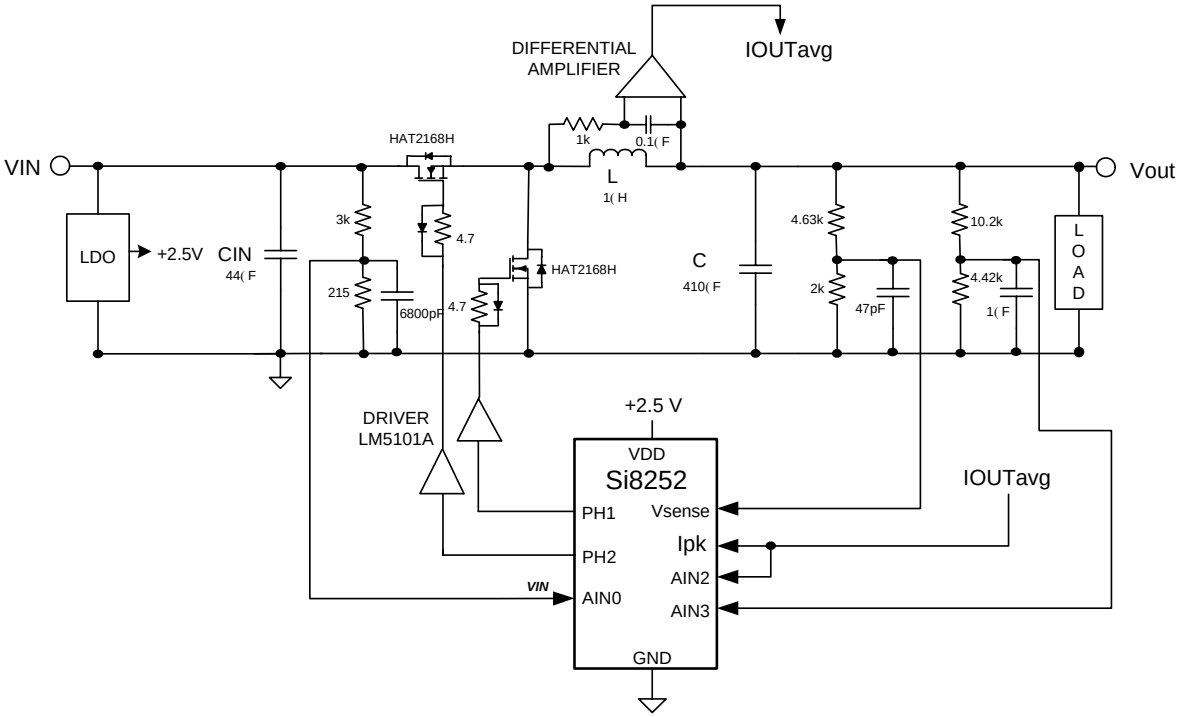


Figure 3-30 Single phase POL converter schematic

Table 3-2 Specification of single phase POL converter with Si8250

Input voltage	10-15Vdc
Output voltage	3.3Vdc @ 20A max
Maximum Power efficiency	92%
Switching frequency	380kHz
Line Regulation	0.42% (15A load)
Load Regulation	0.3% (0~18A load)
Nominal dead time	20ns
Output voltage ripple	30mV@3.3V
Output regulation	±5mV@3.3V, ±8mV@1.5V
Transient response	100mv under/overshoot 100us settling time @ load step 5-10A, 2.5A/us
Output inductor	1uH (DCR: 1.56mΩ)
Output caps	410uH (Capacitor ESR: 1.25mΩ)
Measured nominal loop Bandwidth	36.8 kHz
Measured nominal loop Phase margin	69 deg

3.6.2 Control loop design

As discussed previously, usually the resolution of the ADC determines the output voltage sensitivity (ΔVo/Vo). To satisfy the output voltage regulation specification (1%), resolution of the ADC has to detect output voltage errors lower than the allowed variation of the output voltage ΔVo. However, ADC1 of Si8250 is with differential input, which means it basically sampling the deference of input and reference voltage. This feature realizes very high precision sampling performance with feedback voltage.

The resolution of the ADC1 (LSB size) is programmable from as low as 4 mV up to a maximum of 20 mV. The gain of the ADC1 is equal to 1/LSB, which should be count in loop gain design.

The DPWM resolution determines the smallest discrete time movement an output timing edge can make. (For example, a 10 ns resolution means any given output timing edge can move a minimum of 10 ns.) As a result, DPWM resolution also determines the smallest output voltage correction that a change in duty cycle can make. If resolution of the DPWM is less than the resolution of ADC1, the zero error output voltage value will not fit within the zero error bin of the ADC, and the feedback controller will periodically switch among two or more discrete values of the duty ratio causing a tone in the supply output. This type of oscillation is referred to as a "limit cycle", and can be avoided by ensuring the minimum change in the output voltage (mV) caused by one LSB change in the duty ratio is smaller than the LSB size (mV) of the ADC converter.

S-domain loop compensation design techniques can be applied (and later translated to Z domain) if the ADC sampling frequency in the digital control loop is much higher than the

control loop bandwidth (known as "*digital redesign*"). The equivalent model control loop of the block level diagram is given below in Figure 3-31.

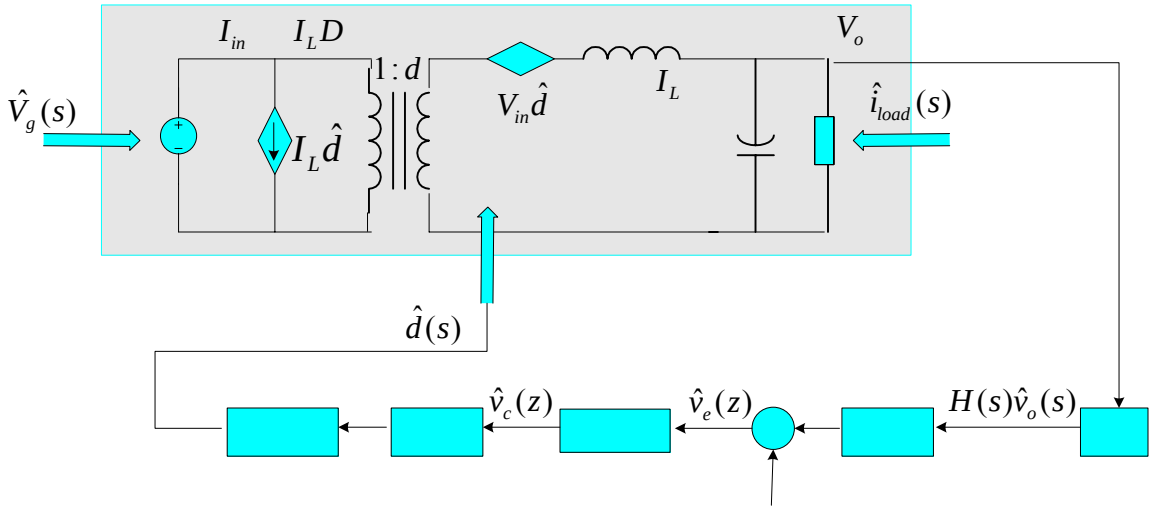


Figure 3-31Digital Control Loop Block Diagram

As discussed in Chapter 2, the loop gain is represented by

$$T(s) = H(s)G(s)G_{vd}(s)G_{PWM}G_{ADC} \qquad 3\text{-}11$$

Where G_{PWM} and G_{ADC} are the gain of DPWM module and gain of AD converter respectively. G_{PWM} is the ratio of PWM switching frequency and clock frequency, which is $G_{PWM} = \frac{f_{PWM}}{f_{Clock}}$ [B6]. In single-phase POL design, 391 kHz PWM frequency and 200 MHz clock frequency will

attenuate loop gain $G_{PWM} = \frac{391k}{200M} = 1.5 \times 10^{-3}$ (-57dB). G_{ADC} is reverse proportional to resolution LSB of ADC[B6] represented by $G_{ADC} = \frac{1}{LSB}$, which will contribute loop gain $G_{ADC} = \frac{1}{10m} = 1 \times 10^{4}$ (80dB) with 10mV LSB size. $H(s)$ is the voltage sense gain, which is equal to 0.3 when desired output voltage is 3.3V.

The output inductor of POL converter is 1uH and the output capacitance is 410uF, so we have the small-signal transfer function of single-phase POL as equation 3-12 and the frequency response is shown in Figure 3-32.

$$G_{vd}(s) = \frac{12}{(4.1 \times 10^{-10} s^2 + 6.06 \times 10^{-6} s + 1)} \qquad 3\text{-}12$$

Since the output filter determinates the resonant peak at 7.8 kHz, with the three poles/two zeros digital PID structure of Si8250, we place the first zero at 4 kHz in s domain, and second zero at 20 kHz, and two poles around 400 kHz. With 10 MHz sampling of ADC performance of Si8250, the discrete and continuous compensator response is shown in Figure 3-33.

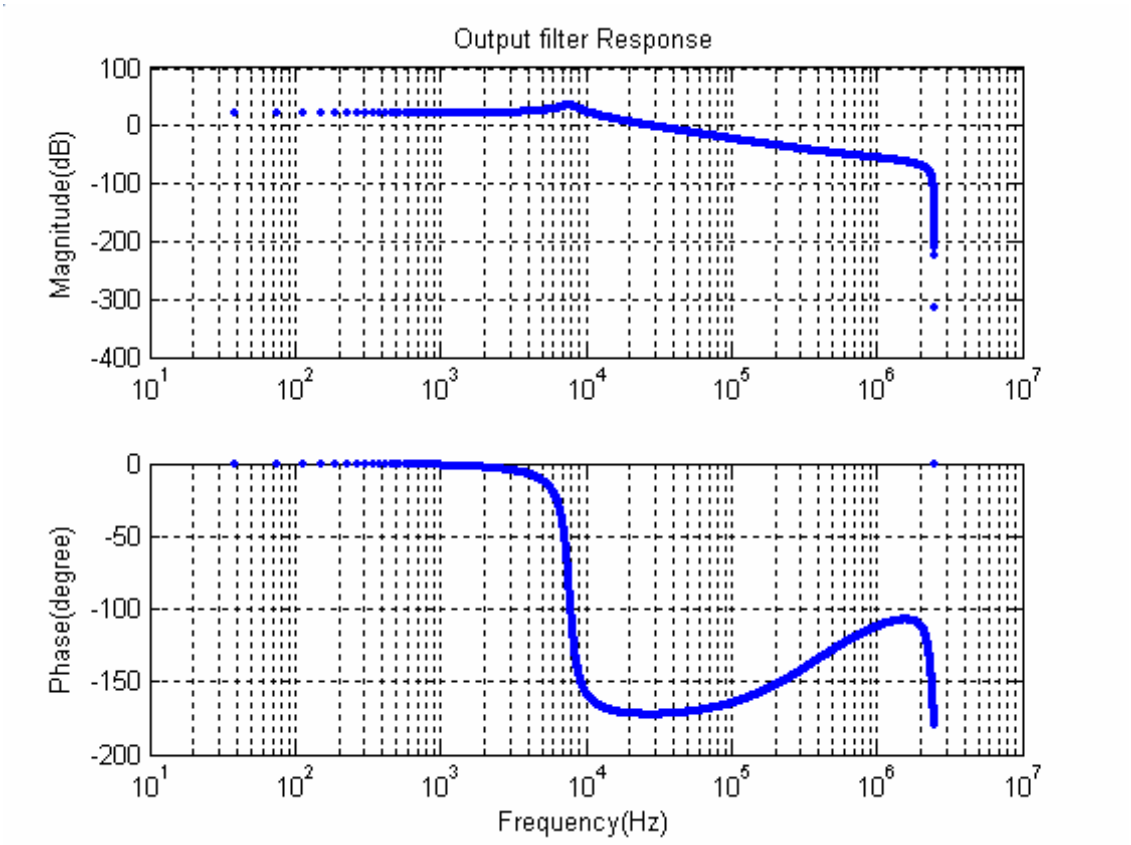


Figure 3-32 Single phase POL converter frequency response

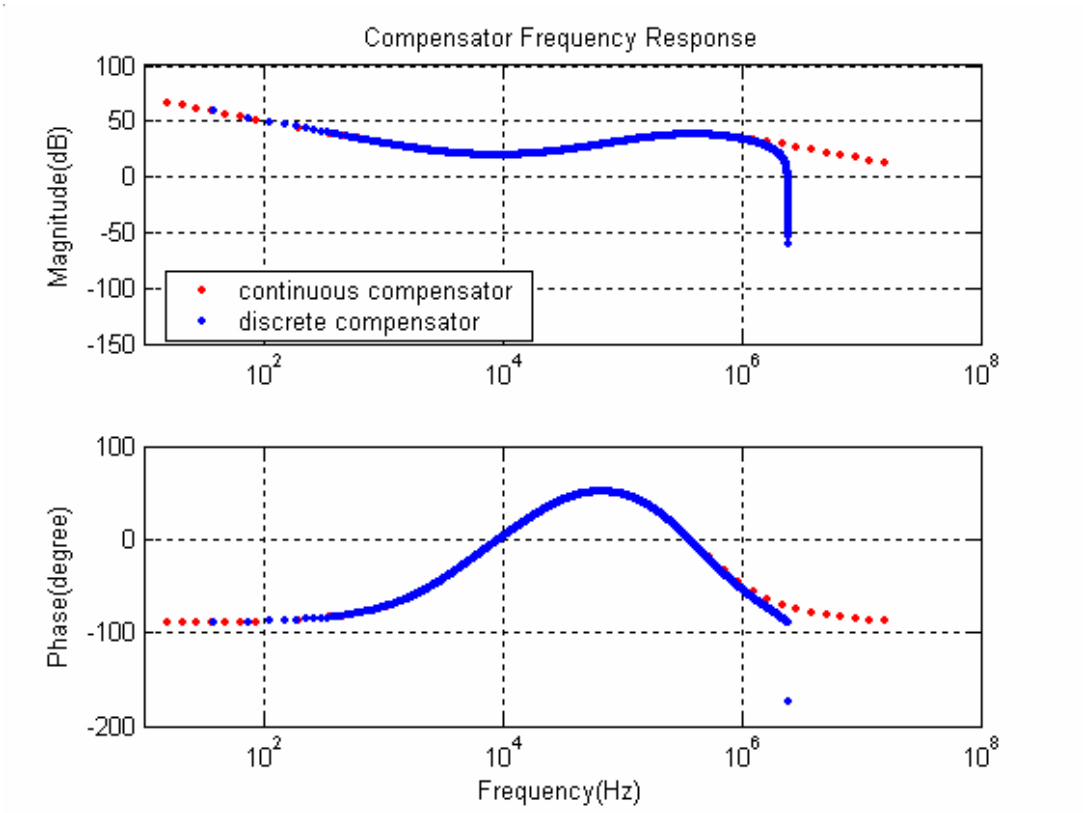


Figure 3-33 Continuous/discrete PID compensator responses

Considering all of gain items in equation 3-11, compensate gain to achieve the desired bandwidth and phase margin in bode diagram. Then the floating-point values of digital PID coefficients are able to be derived in MatLab simulation from the equation 3-9 according to the s domain response and transformed z domain response. Then the digital coefficients are converted to fixed value and hexadecimal values as following.

$$\begin{array}{lll} kp = 0.7334 & kp = 0.6857 & kp = 0x0\mathrm{B} \\ ki = 0.0031 & ki = 0.0020 & ki = 0x01 \\ kd = 24.0527 \Rightarrow & kd = 24.0000 \Rightarrow & kd = 0x18 \\ A_1 = -1.1966 & a1 = -1.2031 & a1 = 0xB3 \\ A_2 = 0.3580 & a2 = 0.3594 & a2 = 0x3E \\ A_3 = 2.6290 & a3 = 0.9922 & a3 = 0x7F \end{array} \qquad 3\text{-}13$$

With those digital coefficients the system bandwidth of POL converter will be 37.8 kHz and phase margin 52.3 deg in MatLab simulation, which meats the requirement of system steady stage regulation.

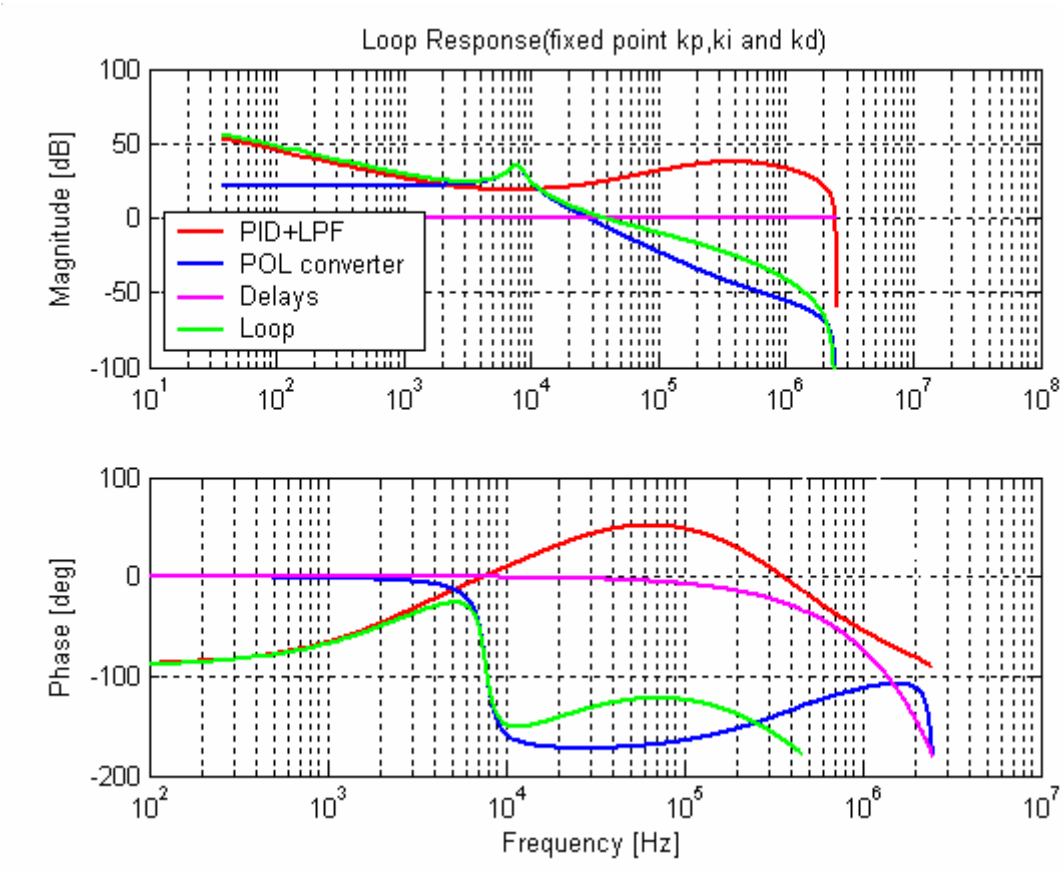


Figure 3-34 POL, PID, delay and open loop responses

3.6.3 Non-linear transient response control

Si8250 allows a transient detector to monitor the output of the differential ADC and generates an interrupt to the system management processing section when the output of the differential ADC exceeds a user-defined range, for example load changes causes voltage overshoot or undershoot.

To be specific, during steady-state operation, the PID filter engine operates with the relative low bandwidth coefficients to maintain small steady-state error and good immunity of disturbance. When load changes transient detector monitors the output voltage exceed the range, then an interrupt is triggered. During this interrupt routine, system processor can update a set of new digital coefficients to filter engine to improve the system performance in transient, for instance, higher bandwidth coefficients to speed up the responding.

Figure 3-35 shows the nonlinear control processing for POL converter. When transient interrupt is triggered system updates a set of 100 kHz bandwidth coefficients to replace steady-state 40 kHz bandwidth coefficients. Then those new coefficients would be held for a while in transient blanking period, after that, system decreases the loop bandwidth gradually in phase 1 and phase 2 by updating the coefficient registers continuously till bandwidth reaches back the steady-state bandwidth.

Since nonlinear control changes system's linearity, improper switch of system gain and bandwidth will cause worse undershoot or overshoot. So tweaking the transition of switching coefficients on the fly would be necessary.

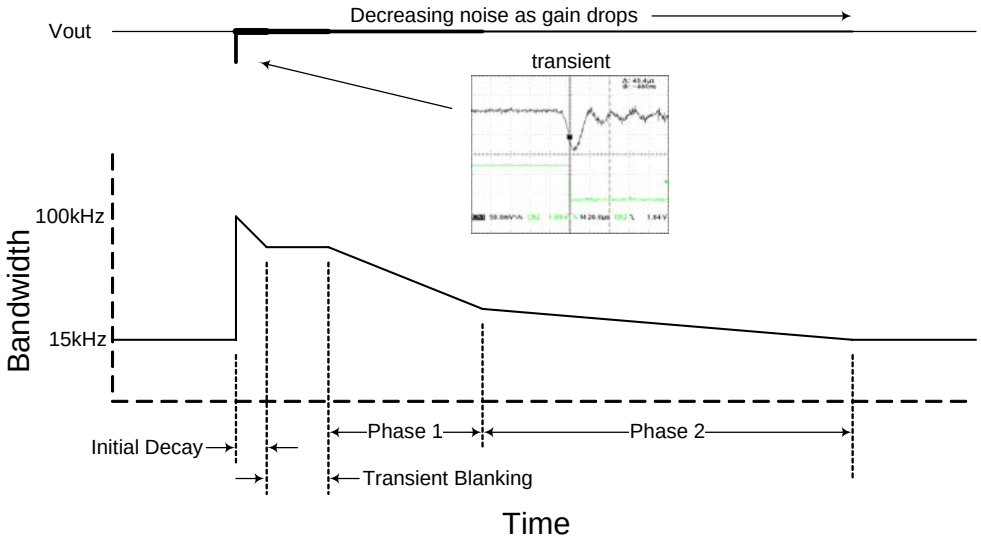


Figure 3-35 Nonlinear control algorithm for POL converter

3.6.4 Experiment results

Timing design ensures that the timing of DPWM outputs (PH1 to PH2) driving the power switches is accurately maintained for better efficiency and protection of the converter, and it is necessary to minimize the deadtime to ensure minimum body diode conduction losses without jeopardizing the normal operation. The timing editing is implemented in DPWM timing editor of Si8250 in figure 3-36.

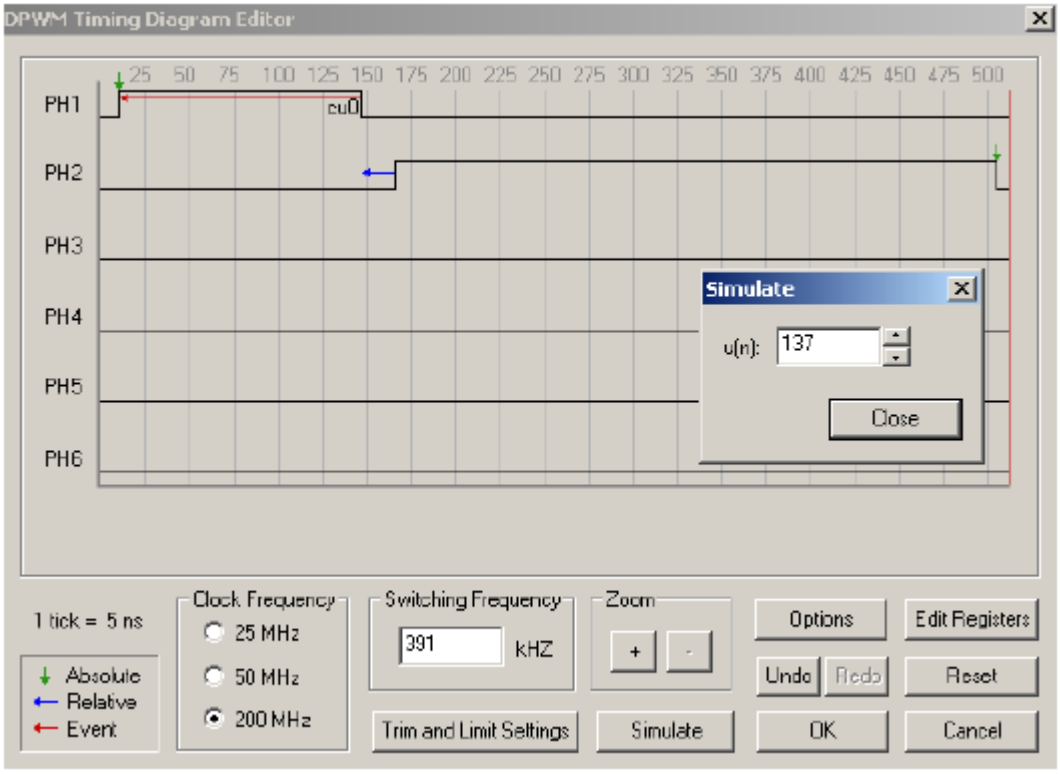


Figure 3-36 DPWM timing editing for single-phase POL converter

PMBus is a connectivity solution designed for networking multiple power supplies using a single management bus(see chapter 2).The Real-time Kernel provided with the Si825x Single-Phase POL Reference Design includes optional support for PMBus. In addition, the Si825x POL design kit also comes with a PMBus Monitor application and USB to SMBus Bridge Board to manage the power supply through PMBus. PMBus monitor is shown in figure 3-37.

Figure 3-37 View of PMBus monitor

The Silicon Laboratories IDE combines an editor, project manager, code environment tools, and a debugger into a single intuitive environment for code development and in-system debugging. Figure 3-38 shows the IDE.

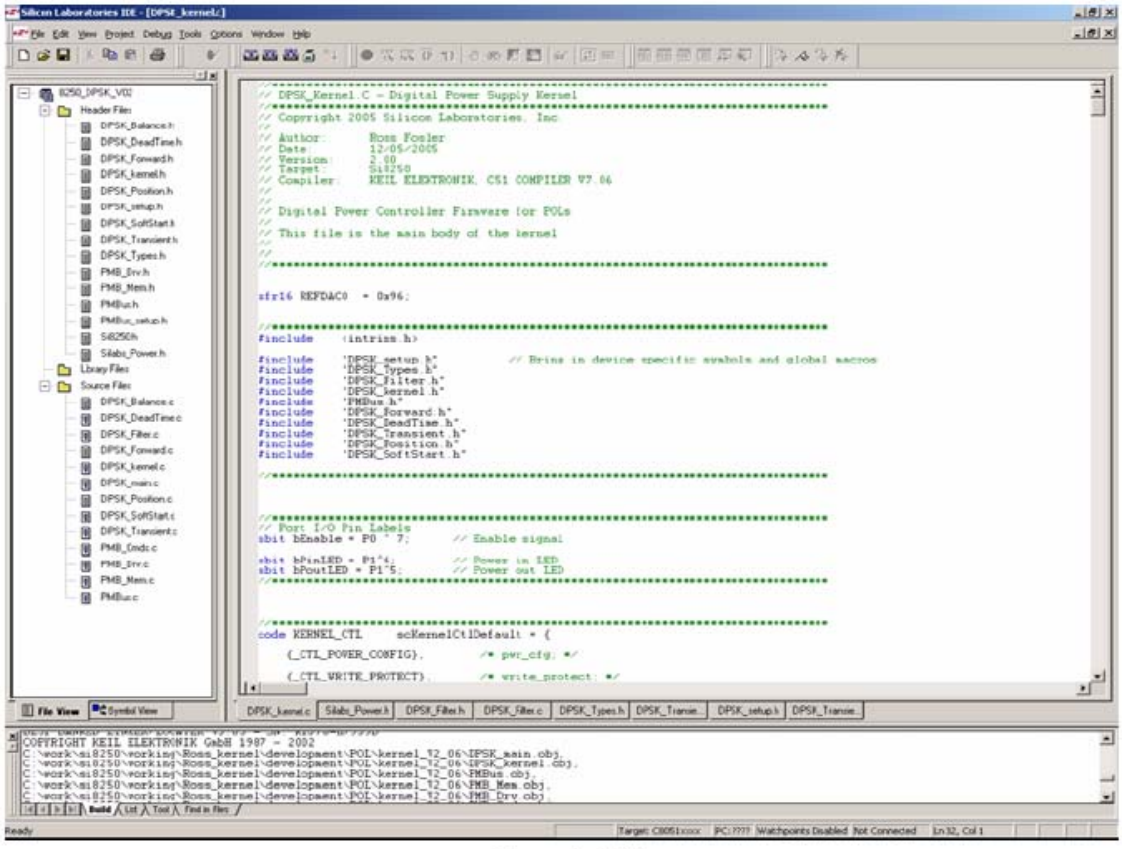


Figure 3-38 IDE

Figure 3-39 shows the measured POL board loop response from network analyzer. This response is with digital coefficients achieved from previous simulation design, and the digital coefficients of PID engine are set up as follows in hexadecimal values, which are derived from equation 3-13:

$$kp = 0x0\mathrm{B}\ ki = 0x01\ kd = 0x18\ a1 = 0xB3\ a2 = 0x3E\ a3 = 0x7F$$

The real response with those PID design loop shows that the bandwidth is 36.86 kHz and phase margin is 69deg, which are very close to the simulation of 37.8 kHz bandwidth and

52.3 deg phase margin. The phase margin difference between simulation and experiment is from practical time delays that are not considered in the simulation. The accuracy of MatLab simulation of digital PID has been proved through this POL controller design realization.

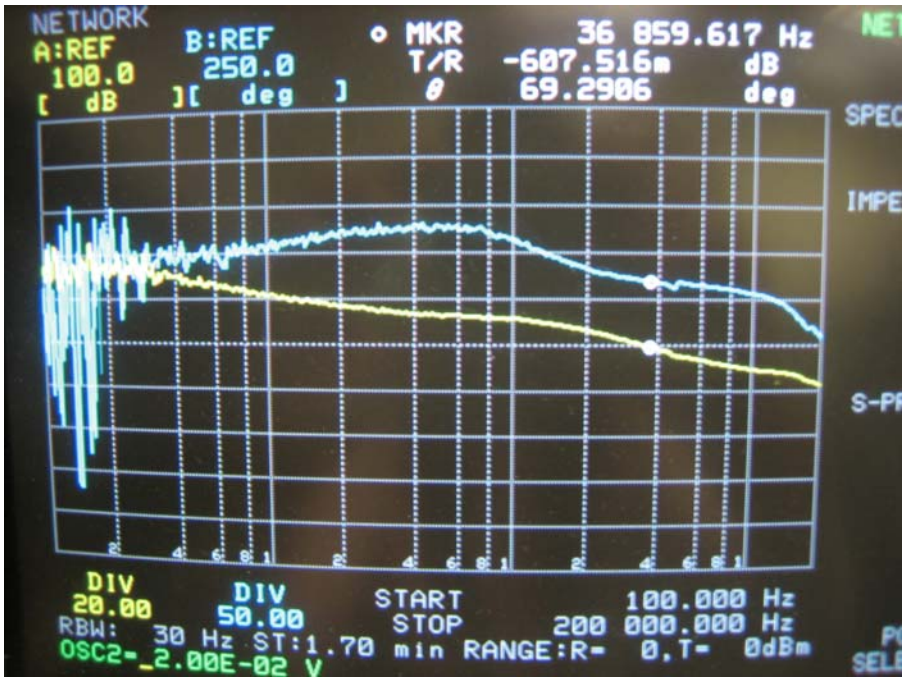


Figure 3-39 Measured frequency response of POL converter

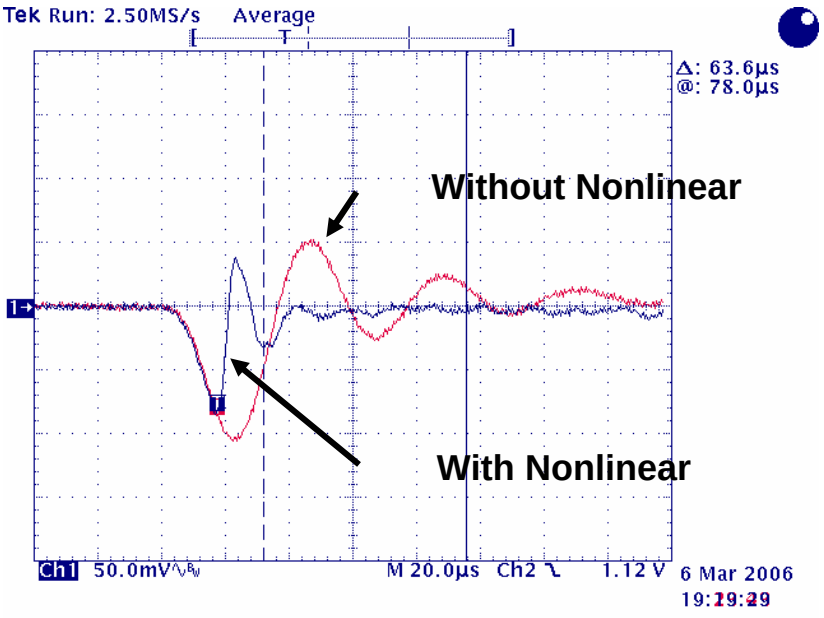


Figure 3-40 Transient response of POL w/ and w/o nonlinear control

Figure 3-40 shows the transient response improvement with nonlinear control proposed in above section. This response is with load step from 25% to 50% and di/dt = 2.5A/us. It can be seen that, with nonlinear coefficients switching, the output voltage undershoot is less and the settle time is reduced a lot. Therefore, the digital nonlinear control improves the POL performance in term of transient response.

The output ripple is shown in figure 3-41 and 30mV peak to peak voltage difference represents 1% ripple in terms of 3.3V output. Output regulation shows that there is no limit cycle oscillation occurring in the system by setting up appropriate ADC and DPWM resolution. The power efficiency curve of single phase POL converter is shown in figure 3-42. The maximum power efficiency achieved is around 92% at half of load.

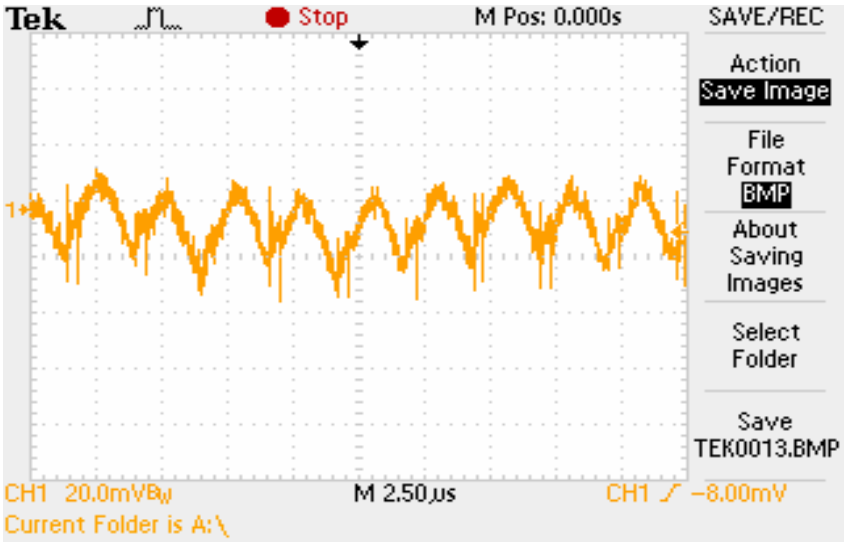


Figure 3-41 Output regulation of single-phase POL converter (30mV ripple@3.3V)

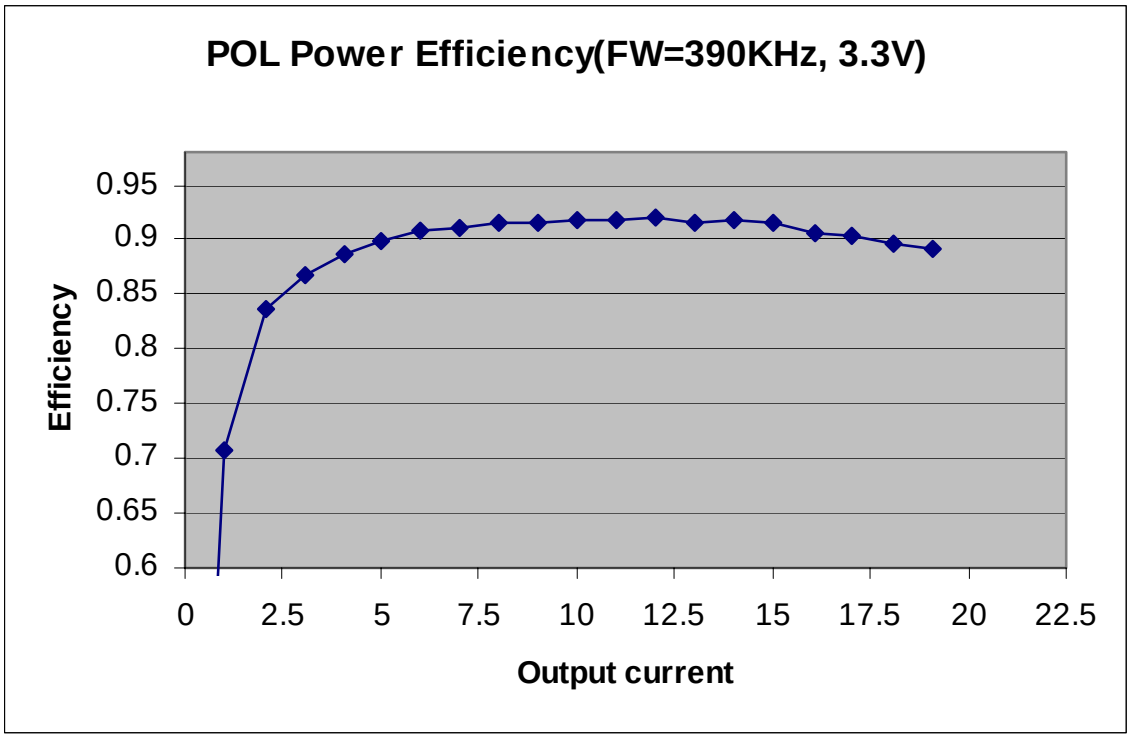


Figure 3-42 Power efficiency of single-phase POL converter

3.7 Summary

Digital redesign addresses modeling power converters as linear system and designing controller in continuous time domain. Mapping from s to z domain is to transform the controller from analog form to discrete form. However, direct tuning digital coefficients for a digital controller would be difficult since power designers' knowledge is based on s domain. The chapter provides a design approach that remaps the digital PID coefficient changes to s domain response in order to reduce the time of digital design and development. Further, the coefficients

resolution, limited word length and quantization effects are all key issues in digital controller design. This chapter addresses all those design issues from practical perspective.

Prototype of single-phase POL demo board is developed with digital controller Si8250 based on the constructed PID structure and the design approach. ADC, DPWM and digital filter completes the digital control loop of POL prototype and the digital controller design issues have been explored from simulation and experiment perspective. In addition, nonlinear transient response control implemented in the developed POL demo board shows the great advantage of digital controller in implementing advanced control techniques. PMBus and power management are implemented through SMBus and system management processor in the prototype.

4 MODELING AND DIGITAL CONTROL OF HALF-BRIDGE DC-DC CONVERTERS

4.1 Introduction

In isolated DC-DC converters, due to some excellent features, half-bridge DC-DC converter is particularly suitable for low-voltage high-current on-board DC-DC converters compared to other converter topologies. There are two conventional control schemes for the HB DC-DC converter, namely, symmetric control and asymmetric (complimentary) control. A HB DC-DC converter with a Current Doubler Rectifier (CDR) is suitable for high-current low-voltage applications since the CDR structures have lower conduction loss compared to the center-tap rectifier. By changing the control from symmetric to asymmetric, Zero-Voltage-Switching (ZVS) can be achieved and the primary-side ringing is eliminated [C6, C7].

Due to the excellent features of HB converter and widely utilization in DC-DC converters, HB converter has been selected as the main topology this dissertation research work concentrated on. The research perspectives consist of mathematically modeling analysis and control scheme unification for HB converter operating in different approaches, including symmetrically, asymmetrically and DCS (Duty cycle shift) controlled HB converters. Meanwhile, digital controlled HB converter is modeled, analyzed and implemented with Si8250. As part of main contribution of this dissertation research work, a new asymmetrical flyback forward HB (AFFHB) converter will be discussed in chapter 5 and a digitally adaptive gain compensation algorithm is proposed to improve the AFFHB converter's performance.

In this chapter, first a unified average space-state model is established for the half-bridge converter with current doubler rectifier considering the parasitic DC parameters. According to the dc model, a number of important issues of current doubler rectification in both symmetric and asymmetric HB dc-dc converters will be presented in term of numerical equations. Then a unified small-signal model is established and investigated, and the controller design guidelines are provided with both symmetric and asymmetric HB dc-dc converters. Based on this unified small signal model, control loop design guidance will be given and digital controller based on Si8250 is designed to meet the HB converter system performance requirements with *digital redesign* method.

4.2 Unified Model of Symmetrical and Asymmetrical HB Converters

The half-bridge dc-dc converter with a current doubler rectifier (CDR) is shown in Fig. 4-1, which could be controlled symmetrically or asymmetrically. Neglecting the leakage inductance and transient commutation, and considering the converter operating at CCM mode due to the synchronous rectifier, the converter has three typical modes as shown in Fig. 4-2 (a)(b)(c), where the load are assumed as a constant current source since the voltage ripple is ignorable [C1]. In a switching cycle, the converter can be denoted using three linear state-space equations, respectively. The three corresponding space-state equations can be expressed as:

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \tag{4-1}$$

$$y = Cx + Eu \tag{4-2}$$

$$\text{where } \dot{x} = \frac{dx}{dt} \qquad u=\left[V_{in} \;\; I_o\right]^T \qquad y = v_o \tag{4-3}$$

During the on time of switch S1, the corresponding matrices are A_1 and B_1; during the on time of switch S2, the corresponding matrices are A_2 and B_2; during the off time of both switch S1 and S2, the corresponding matrices are A_3 and B_3.

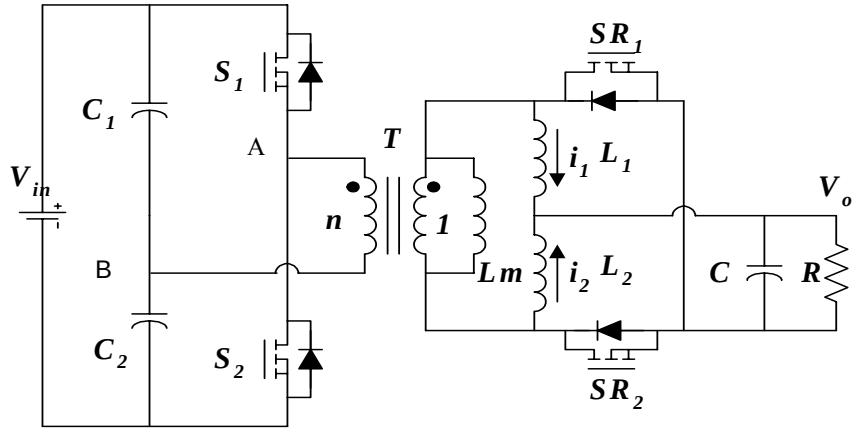
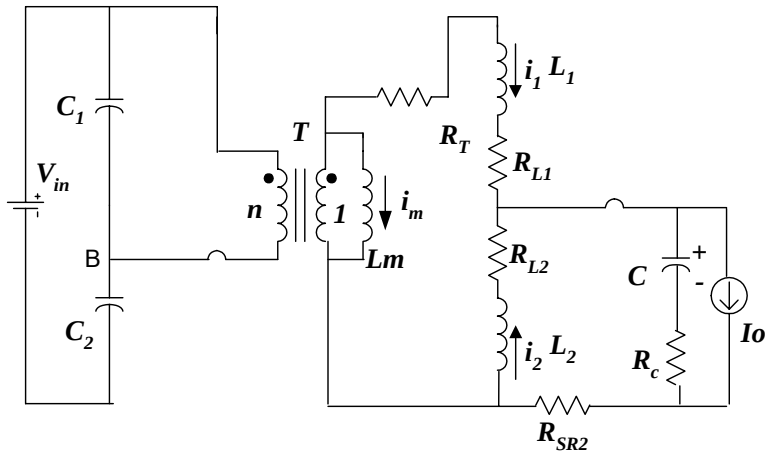
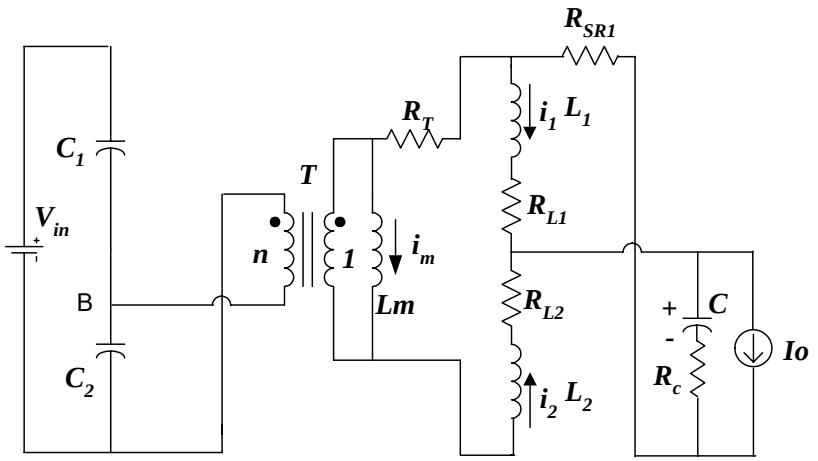


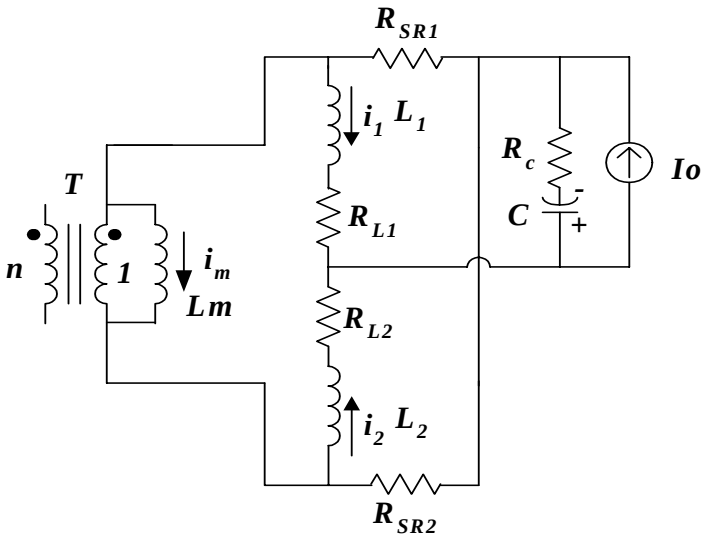
Figure 4-1 CDR half-bridge DC-DCConverter



(a). Mode 1: S1 is on



(b) Mode 2: S2 is on



(c) Mode 3: Both S1 and S2 are off

Figure 4-2 Modes of operation

All matrixes above are as follows:

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{n} & 0 & 0 & -\frac{1}{n} \\ \frac{1}{n} & -(R_{L1}+R_C+R_{SR2}+R_T) & -(R_C+R_{SR2}) & -1 & 0 \\ 0 & -(R_C+R_{SR2}) & -(R_{L2}+R_C+R_{SR2}) & -1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{1}{n} & 0 & -\frac{1}{n} \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -(R_C+R_{SR1}) & -1 & 0 \\ -\frac{1}{n} & -(R_C+R_{SR1}) & -(R_{L2}+R_C+R_{SR1}+R_T) & -1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -R_C & -1 & -R_{SR1} \\ 0 & -R_C & -(R_{L2}+R_C+R_{SR2}) & -1 & R_{SR2} \\ 0 & 1 & 1 & 0 & 0 \\ 0 & -R_{SR1} & R_{SR2} & 0 & -(R_{SR1}+R_{SR2}) \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & R_c & R_c & -1 & 0 \end{bmatrix}^T$$

$$B_2 = \begin{bmatrix} 0 & 0 & \frac{1}{n} & 0 & -\frac{1}{n} \\ 0 & R_c & R_c & -1 & 0 \end{bmatrix}^T$$

$$B_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & R_c & R_c & -1 & 0 \end{bmatrix}^T$$

$$C = [0 \quad R_c \quad R_c \quad 1 \quad 0]$$

$$E = [0 \quad -R_c]$$

4-4

Assuming the switch S_1 on time is D_1T, switch S_2 on time is D_2T, the switching cycle is T. The key concept in state-space averaging is the replacement of the above three sets of state-space equations by a single equivalent set

$$\dot{x} = Ax + Bu \qquad y = Cx + Eu \tag{4-5}$$

Where the equivalent matrices are defined by

$$A = D_1 A_1 + D_2 A_2 + (1 - D_1 - D_2) A_3$$

$$B = D_1 B_1 + D_2 B_2 + (1 - D_1 - D_2) B_3 \tag{4-6}$$

The steady-state solution, with DC values indicated by capital letters, is obtained by setting $\dot{x} = 0$:

$$X = -A^{-1} B U \tag{4-7}$$

From Equation 4-7, the steady-state DC quiescent point can be obtained, where the inductor and magnetizing average currents are as follows:

$$I_{L1} = \frac{d_2 R_T + R_{L2}}{(d_1 + d_2)R_T + R_{L1} + R_{L2}} I_o$$

$$I_{L2} = \frac{d_1 R_T + R_{L1}}{(d_1 + d_2)R_T + R_{L1} + R_{L2}} I_o$$

$$I_M = \frac{d_2 R_{L1} - d_1 R_{L2}}{(d_1 + d_2)(R_{L1} + R_{L2}) + (d1 + d2)^2 R_T} I_o$$

4-8

The equations derived above are general solutions for both symmetric and asymmetric half-bridge dc-dc converter [C6]. From equations above, it can be observed that:

1. Only DC resistances and duty cycles, other than capacitance and inductance, have effect on the DC currents distribution.
2. Unbalanced inductor average currents and DC bias of magnetizing current exist due to either asymmetry of equivalent DC resistance (DCR) or duty cycles.
3. On-resistance of synchronous rectifiers has no effect on the DC currents distribution and averaged magnetizing current.

For the HB converter, peak-current-mode control cannot be applied. The natural current sharing between the two inductors is in need. However, the DC current sharing cannot be achieved due to unbalanced DC resistive parameters $R_{L1} \neq R_{L2}$ or unbalanced duty cycle

$D_1 \neq D_2$. The PCB layout of two-channel inductors should be as symmetric as possible, and the both driving channel and switch should match to achieve symmetric duty cycles. If the PCB layout has to be asymmetric, synchronous rectifiers can be asymmetric instead of inductors. As a result of asymmetry, there is a DC magnetizing current bias in the transformer, and which should be estimated when designing the transformer.

For asymmetric HB converter, DC solutions can be obtained by substituting $D_2 = 1 - D_1$ into the DC solutions. From the solution, one may conclude:

The current sharing between two inductors is uneven because of the asymmetric duty cycle.

1. The transformer has DC bias of magnetizing current due to asymmetric duty cycle, and a air gap have to be added to avoid the transformer saturation

4.3 Unified Small-Signal Model of HB converters

The unified small-signal model of the half-bridge converter with a current doubler can be derived based on the unified model shown in Equation 4-5 and a small-signal assumption. Perturbing the unified state-space average equation 4-5 as follows:

$$y = Y + \hat{y} \quad x = X + \hat{x} \quad u = U + \hat{u}$$

$$d_1 = D_1 + \hat{d}_1 \qquad d_2 = D_2 + \hat{d}_2 \qquad \text{4-9}$$

Substituting Equation 4-9 into 4-5 and removing the DC bias from the obtained equation and ignoring high-order terms, one can derive the unified small-signal linear models for both symmetrical and asymmetrical HB converters:

$$\hat{x}(s) = (sI - A)^{-1} B\hat{u}(s) + (sI - A)^{-1}[\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)]X$$
$$(sI - A)^{-1}[\hat{d}_1(s)(B_1 - B_3) + \hat{d}_2(s)(B_2 - B_3)]U$$

4-10

$$\hat{y}(s) = C(sI - A)^{-1} B\hat{u}(s) + C(sI - A)^{-1}[\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)]X$$
$$C(sI - A)^{-1}[\hat{d}_1(s)(B_1 - B_3) + \hat{d}_2(s)(B_2 - B_3)]U + E\hat{u}(s)$$

4-11

The unified output-to-control transfer function can be obtained:

$$\frac{\hat{y}(s)}{\hat{d}(s)}\Big|_{\hat{u}(s)=0} = C(sI - D_1A_1 - D_2A_2 - (1-D_1-D_2)A_3)^{-1}[\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)] *$$
$$[D_1A_1 + D_2A_2 + (1-D_1-D_2)A_3]^{-1}[D_1B_1 + D_2B_2 + (1-D_1-D_2)B_3]\frac{-U}{\hat{d}(s)}$$
$$+ (sI - D_1A_1 - D_2A_2 - (1-D_1-D_2)A_3)^{-1}[\hat{d}_1(s)(B_1 - B_3) + \hat{d}_2(s)(B_2 - B_3)]\frac{U}{\hat{d}(s)}$$

4-12

The open-loop output impedance of the half-bridge converter can be derived as:

$$Z_{output} = \frac{\hat{V}_o}{\hat{i}_o}\Big|_{\hat{d}(s)=0} = [C(sI - A)^{-1} B + E]_{12} \qquad 4\text{-}13$$

For symmetrical HB, the two switches operate at the same steady-state duty cycle $D_1 = D_2 = D$, and the duty cycles of the two switches disturbance are $\hat{d}_1(s) = \hat{d}(s)$ and $\hat{d}_2(s) = \hat{d}(s)$ [C2-C4]. Substituting the two conditions into Equations 4-10, the linearized small-signal state-space equation of symmetric HB is obtained:

$$\hat{x}(s) = [sI - D(A_1 + A_2) - (1-2D)A_3]^{-1}[D(B_1 + B_2) + (1-2D)B_3]\hat{u}(s) + (sI - A)^{-1}[(A_1 + A_3 - 2A_3)X + (B_1 + B_3 - 2B_3)U]\hat{d}(s)$$

4-14

The output-to-control transfer function of symmetric HB is:

$$\hat{y}(s) = C(sI - A)^{-1}B\hat{u}(s) + C(sI - A)^{-1}[(A_1 + A_3 - 2A_3)X + (B_1 + B_3 - 2B_3)U]\hat{d}(s) + E\hat{u}(s)$$

4-15

If the HB converter has half-bridge circuits are balanced, which means $L_1 = L_2 = L$, $R_{L1} = R_{L2} = R_L$ without consideration of R_{SR}, from Equation 4-15 yielding the output-to-control transfer function:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{(V_{in} - R_T I_o n)(sC_o R_c + 1)}{n(s^2 C_o L + sC_o D R_T + sC_o R_L + 2sC_o R_c + 2)}$$

4-16

From equation 4-16, we can see that symmetric HB is a second-order system. Due to the symmetric control, the magnetizing inductance and input capacitance has no impact on the dynamic system model. From control stand point of view, this is an advantage over asymmetric HB, because which makes the system design easier. The output impedance is give in Equation 4-17, and the bode diagram and output impedance is plotted in Figure 4-3.

$$Z_{output} = \frac{\hat{V}_o}{\hat{i}_o}\Big|_{\hat{d}(s)=0} = \frac{s^2 LC_o R_c + sL + sdR_T C_o R_c + sR_L C_o R_c + dR_T + R_L}{s^2 C_o L + sC_o dR_T + sC_o R_L + 2sC_o R}$$

4-17

For asymmetric HB, the two switches operate at duty cycle D and 1-D, so we set the steady-state values D_1=D and D_2=1-D. Substituting them into Equation 4-16:

$$A = D(A_1 - A_2) + A_2 \qquad B = D(B_1 - B_2) + B_2 \qquad \text{4-18}$$

Setting the disturbance $\hat{d}_1 = \hat{d}$, $\hat{d}_2 = -\hat{d}$, substituting them into equations 4-15 yielding:

$$\hat{y}(s) = C(sI - A)^{-1} B\hat{u}(s) + C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(s) + E\hat{u}(s)$$

4-19

$$\frac{\hat{y}(s)}{\hat{d}(s)}\Big|_{\hat{u}(s)=0} = C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U] \qquad \text{4-20}$$

The bode diagram is plotted as shown in Figure 4-5.

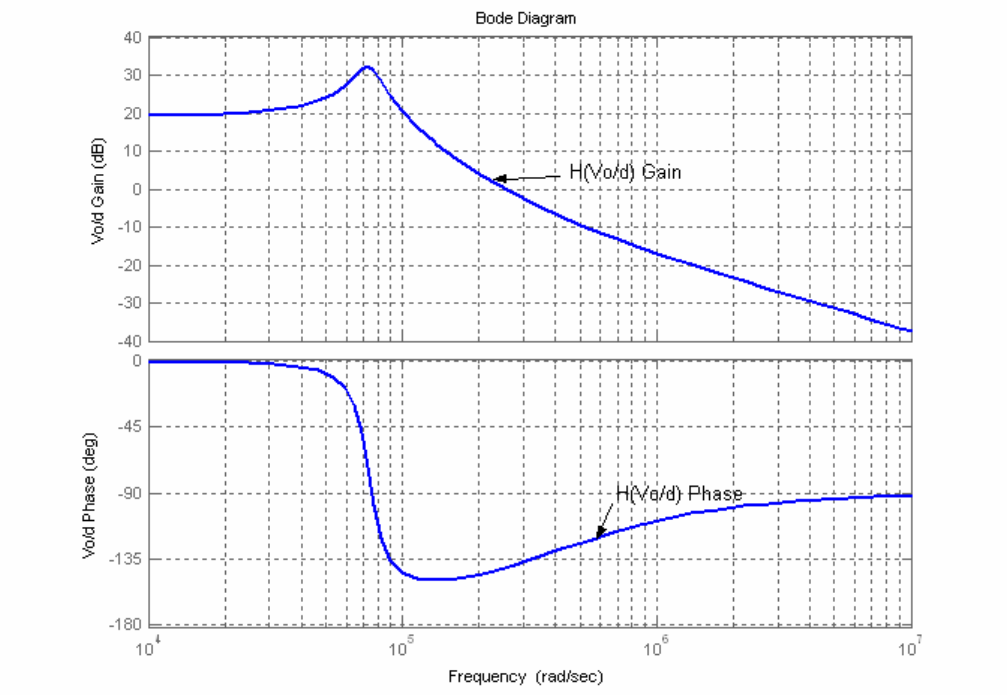


Figure 4-3 Symmetric HB bode diagram

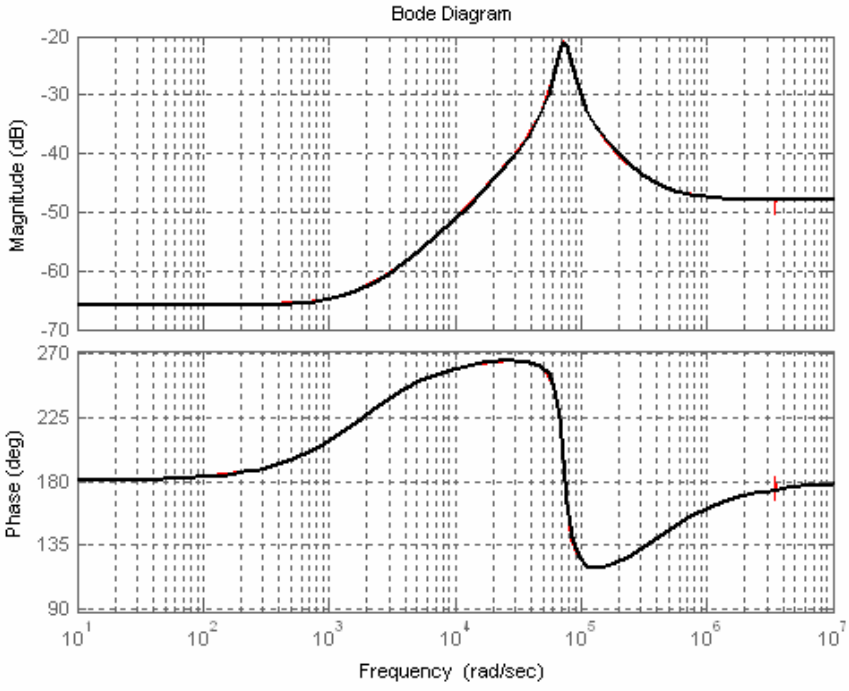


Figure 4-4 Output impedance of both symmetric HB and asymmetric HB

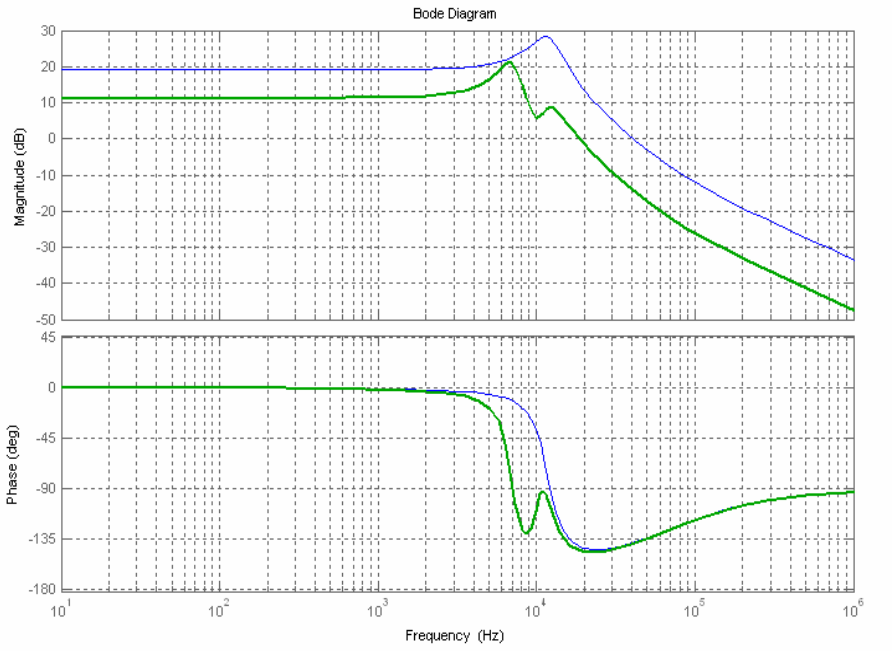


Figure 4-5 Bode diagram of symmetric and asymmetric HB converters

(Blue: symmetric HB, green: asymmetric)

From Figure 4-4, we can figure out the output impedance of the symmetrical and asymmetrical HB converters. Even the symmetric HB and asymmetric HB have different average matrixes A and B. They have identical open-loop output impedance. Obviously, over some frequency range the open loop output impedance Z_{out} has an overshoot magnitude, which causes difficulty to remain the output voltage within a specified range when the load current changes. So the loop gain must be sufficient large to reduce the close-loop output impedance when designing the feed back loop.

The asymmetric HB bode diagram is illustrated in Figure 4-5. Compared with symmetric HB, the asymmetrical HB has two zeros and four poles, which is actually due to

two pairs of LC poles. A LC pole is constituted of transformer magnetizing inductance L_m and the input equivalent capacitance $2C_1$. Another LC pole is determined by equivalent output inductance $L/2$ and output capacitor C_o. Four poles could unfortunately cause a 360^o phase shift, but the two zeros compensates the effect so the final phase shift could not be larger than 180^o. Due to these reasons, some design issues regarding the input capacitance and output filter are needed to consider [C2, C5]:

In order to get wider bandwidth, the resonant frequency $f_2 = \frac{1}{2\pi\sqrt{LC_o/2}}$ should be much larger than the resonant frequency of the input LC network, which is $f_1 = \frac{1}{2\pi\sqrt{2L_mC_p}}$. Therefore, high input capacitance and large magnetizing inductance are good for the loop design.

1. When the input capacitance and magnetizing inductance are small the transfer function exhibits resonant poles with a high Q, which means system transient response will exhibits an overshoot and ringing. So theoretically, the larger is the input capacitance, the better is the system response. However, in the practical design, the cost and the dimension of the system requirement limit the increasing of the input capacitance.
2. When the input filter LC pole appears in low-frequency band, the system comes to be close to symmetric HB, which is good and convenient for the control loop compensation.

3. The higher Q factor of the resonant poles causes the higher overshoot and longer ringing of the system. One approach to damping the high Q is to add a resistor in parallel with input capacitance.
4. From Figure 4-8, we can realize with the decreasing duty cycle, the gain increases and results in lower phase margin, which means the less stable for the system. So the high-line input is the worst case for designing the feed back loop.

4.4 Simulation and Experimental Verification of Modeling of HB Converter

A 3.3V/30A prototype with 36-75V input is built in the lab to verify the unified models. The prototype photo is shown in Figure 4-6. The prototype has the following parameters:

$$F_s = 300\ kHz,\ L1 = L2 = 3.5uH,\ Lm = 25uH,\ n1:n2 = 4:2,$$
$$C1 = C2 = 22uF,\ Co = 470uF$$

Figure 4-7 shows the symmetric HB output-control bode diagram. With different operating duty cycle, asymmetric HB bode diagram comparison between theoretical and experimental results are given in Figure 4-8. The two sets of bode plots are in good agreement. The resonant pole of the input capacitance and magnetizing inductance appears in the low frequency since the input capacitance is large and Q factor is reduced due to the damping effect of the snubbers in the primary side of the converter. Meanwhile, due to the

zero effect of the ESR of output capacitance, the gain of the transfer function is –20dB/dec at high frequency, and the phase shift goes up to -90^{o}.

Figure 4-6 Half bridge with current doubler prototype

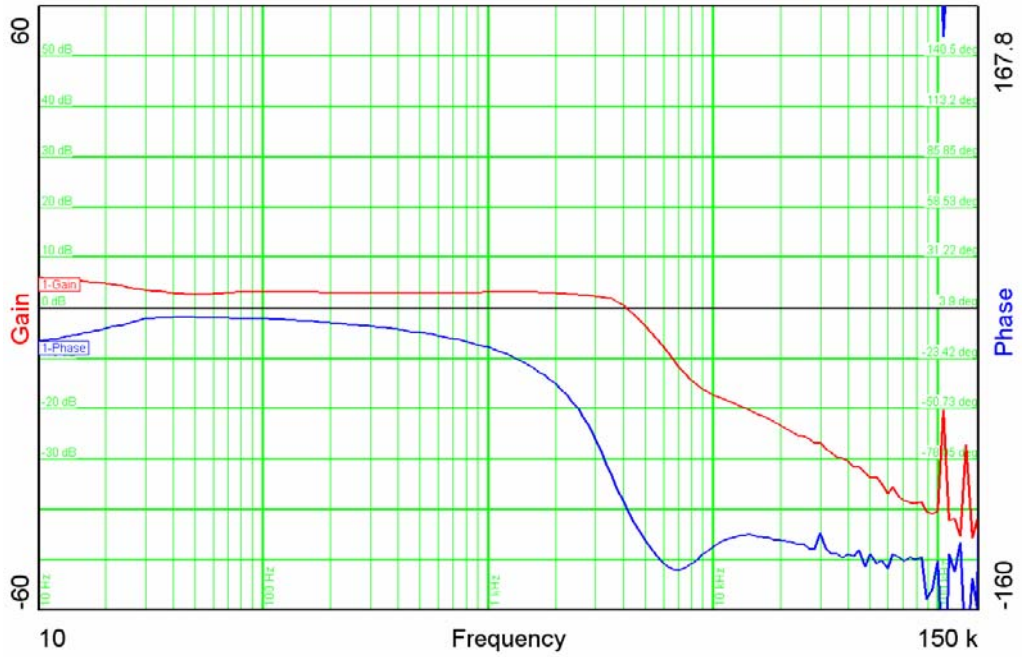
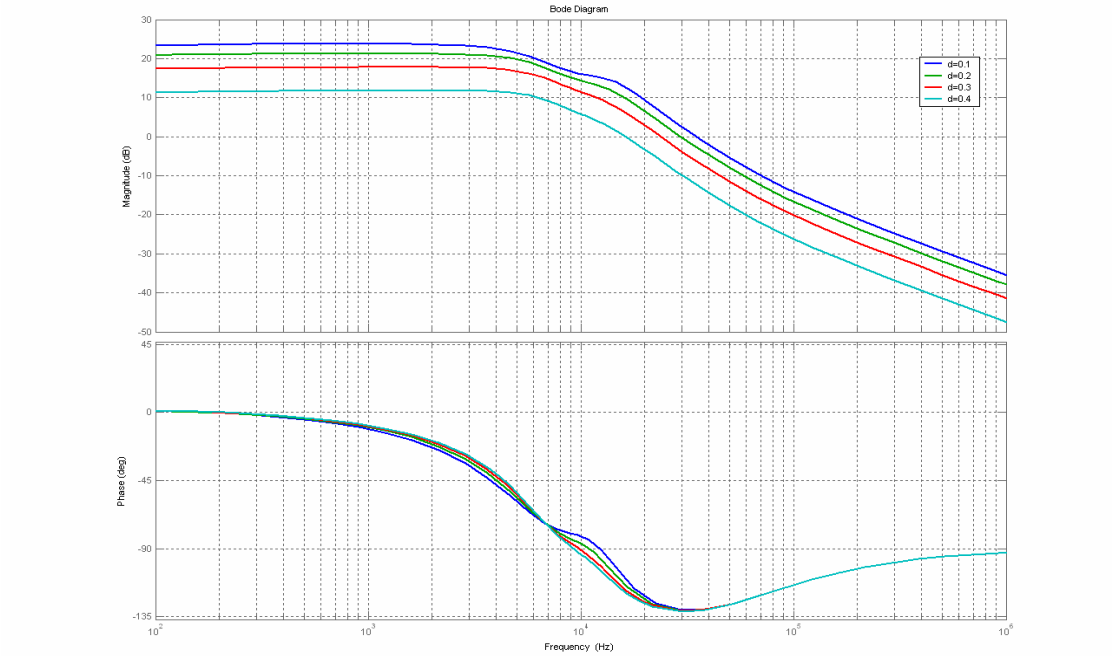
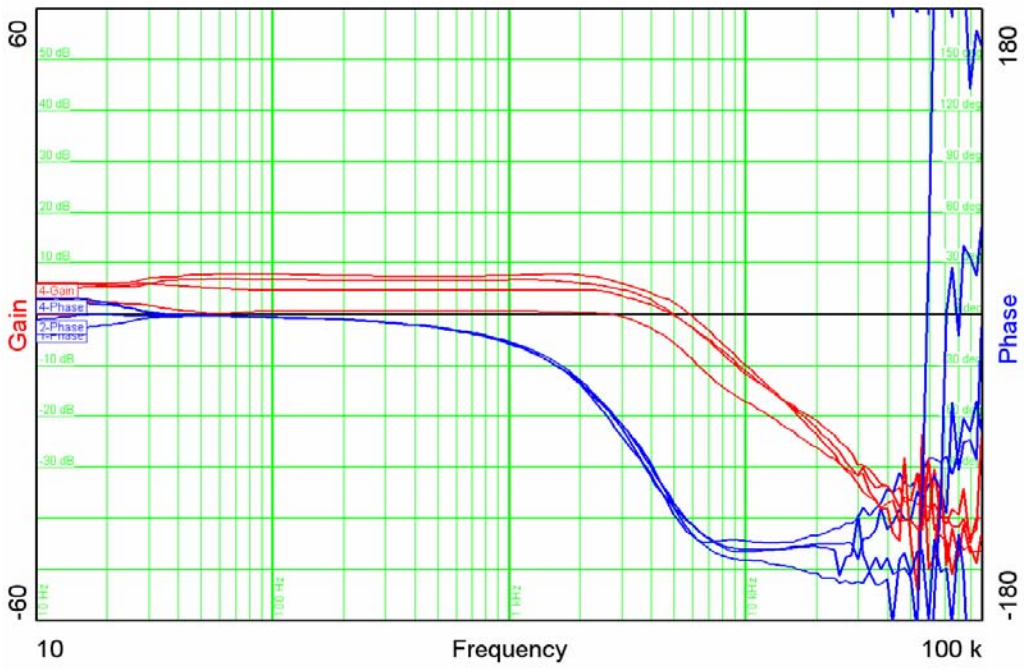


Figure 4-7 Experimental Bode diagram of symmetric HB



(a) Theoretical analysis



(b) Experimental results

Figure 4-8 Asymmetric HB bode diagram comparison between theoretical and experimental results

4.5 Digital Controlled HB converter with Si8250

4.5.1 Hardware overview

As discussed in chapter 3, Si8250's architecture uses dedicated programmable signal processors to perform high-speed control calculations under the supervision of a Flash-programmable microcontroller (MCU) [C13]. The signal processors provide minimum latency calculations and offer die area efficiency. The integrated MCU makes the controller

flexible and enables user firmware to precisely set and modify system attributes (i.e. frequency compensation and system protection). Because the MCU does not perform high bandwidth calculations, it can be lower cost and easier to program than a DSP.

Si8250's digital filter engine and design procedures and consideration have been present in Chapter 3. The schematic of the HB converter prototype is shown in Figure 4-9 and Figure 4-10 shows the photo of the demo prototype. Figure 4-11 shows the power efficiency curve of HB converter. And the specifications of HB converter are listed in Table 4-1.

Table 4-1 Specifications of Si8250 controller half-bridge converter

Input Voltage Range	30 to 72 V
Maximum Output Power	35 W
Output Voltage Range	1.0 V at 35 A max
Output Ripple Voltage	10 mVPeak-to-Peak
Output Regulation	±1.5%
Transient Response	50 mV max deviation for 40 ms max
Efficiency	86%
Connectivity	PMBus

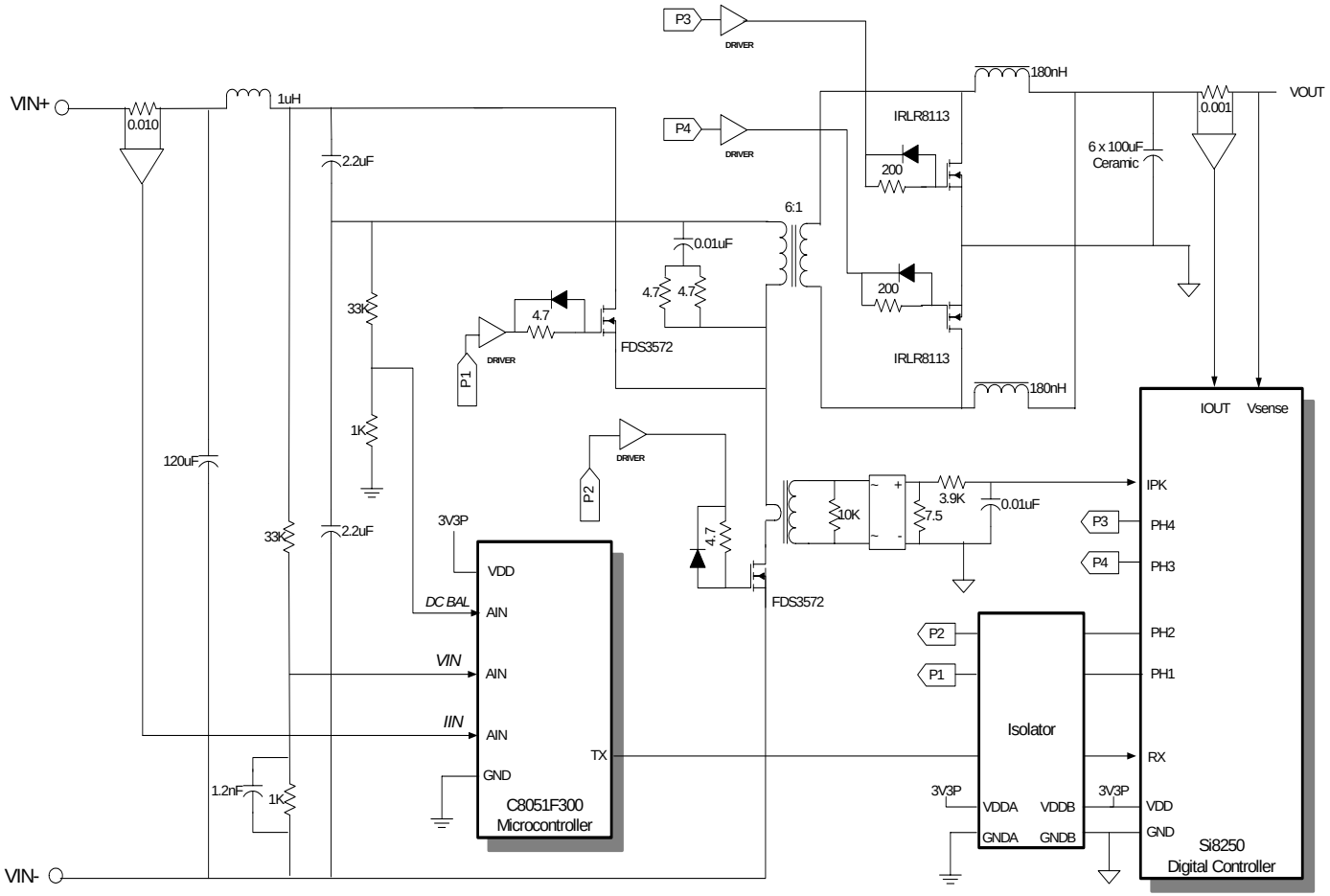


Figure 4-9 Schematic of HB converter with Si8250

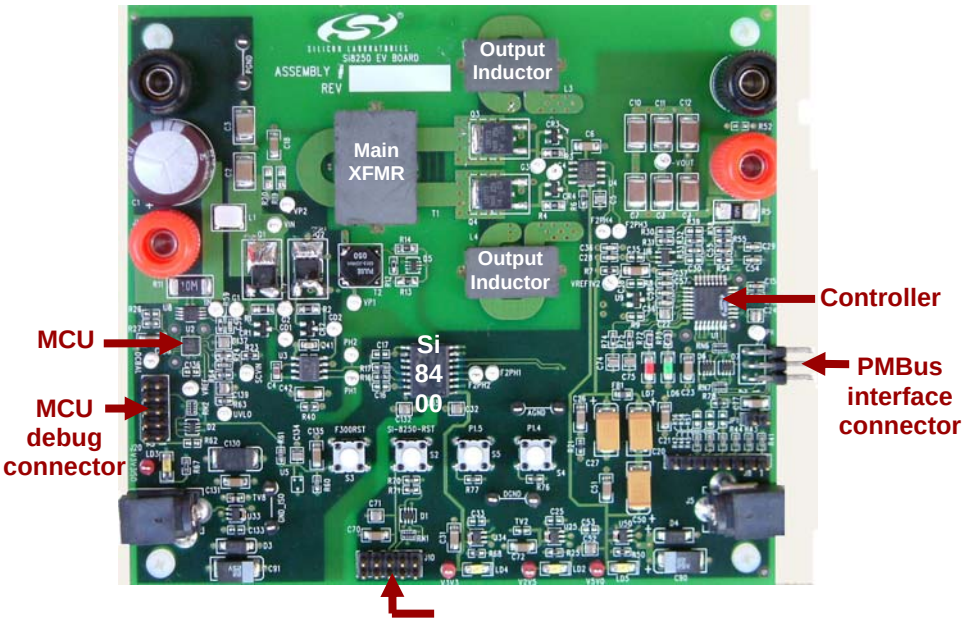


Figure 4-10 Half-bridge with Si8250 demo board

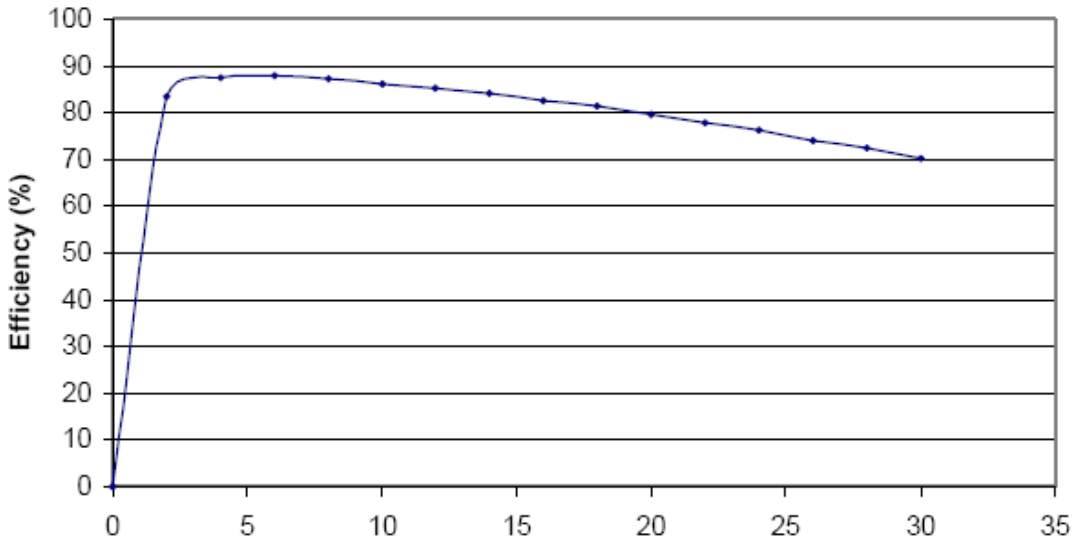


Figure 4-11 Power efficiency curve of Si820 controlled HB converter

4.5.2 Half-bridge power stage design

The design procedures of HB power stage include selecting switching frequency, define range of duty cycle, transformer design, and output filter and components selection such as driver and MOSFETs.

Several factors must be considered when selecting an appropriate switching frequency for a particular application: the size of the converter (limited by the size of magnetic components), the overall losses of magnetic components, and the switching losses of power MOSFETs, the desired efficiency, transient response, and the maximum achievable duty-cycle. The higher the switching frequency is, the higher the required loop bandwidth. (Loop bandwidth is typically chosen at a minimum of the switching frequency divided by 10.) In this particular design, the switching frequency is chosen to be 400 kHz, above which the switching losses tend to dominate the total losses. This

frequency also keeps the overall size of the converter within reason. The primary-side switches of the half bridge are prone to shoot-through. Too short dead times can result in simultaneous conduction of two primary switches, which can degrade the efficiency or even destroy the converter. The maximum duty-cycle selection should incorporate enough margins for dead time between the primary switching phases. The maximum duty-cycle also affects the transformer turns-ratio, which would in turn affect the stress applied to the power components. The maximum duty cycle for this application is 40%.

The primary-to-secondary turns ratio ($n = N_1 / N_2$) of the main transformer should be made as high as possible without exceeding the maximum available duty-cycle at the minimum input voltage and rated load. As turns ratio is increased, the amount of load current reflected into the primary is decreased, which in turn minimizes power losses in the primary MOSFETs. The maximum allowable turn ratio can be calculated with Equation 4-20.

$$D_{MAX} = \frac{2 \cdot V_{out} \cdot n}{V_{in(\min)}} \qquad 4\text{-}20$$

where D_{MAX} is the maximum duty-cycle, $V_{in(\min)}$ is the minimum input voltage specified, and V_{out} is the output voltage. For this application, and given the specified D_{MAX} of 40% and minimum input voltage of 30 V; the calculated transformer turns ratio is 6.

The output LC filter is normally defined based on the required transient response (50 mV) and output voltage ripple (10 mV). To achieve an output voltage regulation

during high slew rate steps with minimum on-board capacitance, the converter must possess fast large-signal transient response. For a properly designed wide bandwidth feedback control, the large transient signal response is mainly determined by the response of the output filter. Decreasing the output filter inductance value can reduce the overshoot/undershoot of the output voltage response. The filter inductance can be reduced by increasing the switching frequency and/or by selecting appropriate converter topology. As a rule of thumb, the overall inductor ripple current should be no more than 20~30% of rated load, and the output inductor value (for each inductor in the current doubler stage) for continuous current mode (CCM) can be calculated using Equation 4-21.

$$V_{out} = \frac{L}{2} \cdot \frac{di}{dt} \qquad 4\text{-}21$$

where L/2 is the equivalent inductance of current doubler secondary topology in this case. The above equation can be re-written with the known parameters (switching frequency and assumed maximum ripple current) as follows:

$$L = \frac{2 \cdot (V_{out} + 2 \cdot V_{fet}) \cdot (1 - D)}{\Delta i \times F_{sw}} \qquad 4\text{-}22$$

Where F_{sw} is the switching frequency, Δi is the maximum allowed current ripple and V_{fet} is the drop across synchronous rectifier. The peak-to-peak current ripple in the

inductor is assumed to be 30% of rated current and the duty-cycle is 40%. From Equation 4-22, the calculated output inductor value is 450 nH.

The requirement of the transient response is the major factor for defining the maximum overall ESR of the output capacitors.

$$ESR = \frac{\Delta V_{transient}}{I_{step}} \qquad 4\text{-}23$$

where $\Delta V_{transient}$ is the maximum allowed deviation from nominal voltage (50 mV) and I_{step} is the 50% load step from 0 to 20 A. From Equation 4-23, calculated maximum allowable ESR is 2.5mΩ. The minimum required output capacitance can be estimated by Equation 4-24 when limiting the output ripple to no more than ΔV_{OUT}.

$$C_o = \frac{1}{\Delta V_{OUT}} \cdot \frac{\Delta i}{8 \times F_{sw}} \qquad 4\text{-}24$$

Where ΔV_{OUT} is the maximum peak-to-peak is ripple (10 mV) and Δi is the maximum peak-to-peak ripple current (30% of rated current). From Equation 4-24, the calculated minimum filter capacitor value is 350 μF. Normally, capacitors used are at least 50% more than the calculated figure, so the chosen value is 600 uF.

4.5.3 HB Converter Loop Design and Implementation

To implement nonlinear control for this HB converter (will be discussed later), we need two compensated loop response corresponding two sets of digital coefficients. One is desired to have bandwidth 35 kHz with large enough phase margin (at least 60^0) to make system has high enough dc gain, and the other one is expected to have higher bandwidth (up to 90 kHz) to achieve fast transient response during transients. The two design cases are discussed below.

In this design, the ADC resolution and sampling frequency are configured to 4mV and 10MHz respectively. DWPM frequency is set at 400 kHz according to the previous calculation.

Case1:

Considering 400 kHz switching frequency, bandwidth $f_c = 40\,KHz$ and at least phase margin 45^0 are desired for steady state regulation. A low frequency zero at 4 KHz is placed to cancel out the phase degrading around the crossover frequency and the second zero at 19 kHz to improve the phase margin. Two poles of low pass filter are put around switching frequency 400 kHz to reduce the switching noise.

The dc gain of power stage from above response can be recognized approximately 15dB. Considering the gain attenuation of DWPM and gain boost of ADC, the total loop gain has been lifted. Then the PID, LPF and composite filter response and the whole open loop response are obtained in the compensator graphs.

Applying digital compensator design procedures discussed in chapter 2(shown in figure 4-12), poles and zeros are placed in s domain first and then with bilinear

transformation simulation achieves z domain poles and zeros. Compared z form compensator transfer function with digital PID compensator structure, related digital coefficients are derived as equation 4-25.

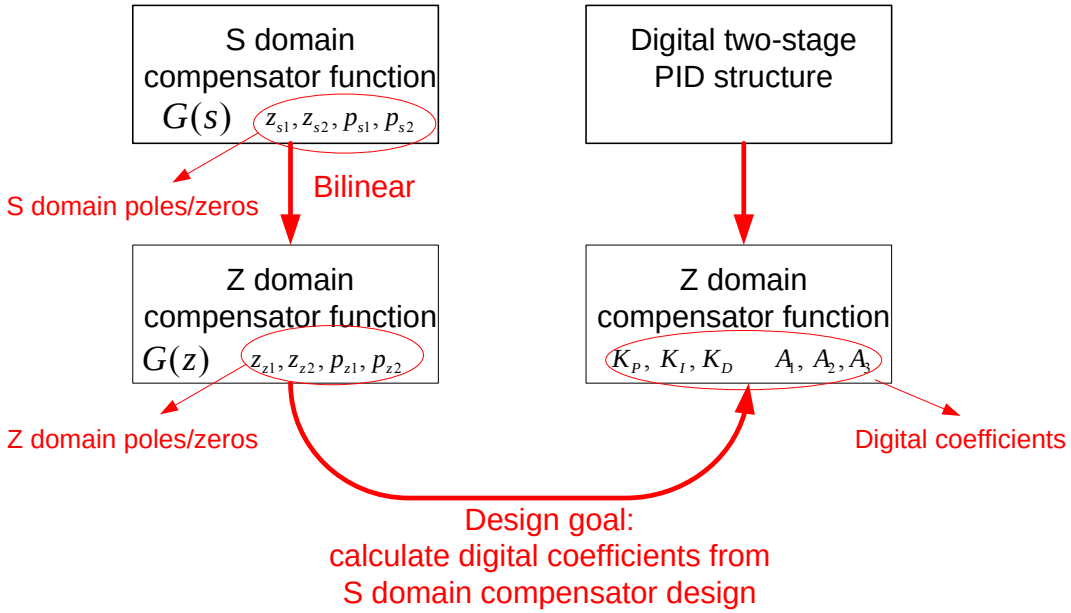


Figure 4-12 Design procedures of digital compensator

$$
\begin{aligned}
kd &= [z(2)\cdot z(1)];\\
kp &= [z(2) + z(1) - 2\cdot z(2)\cdot z(1)];\\
ki &= [1 + z(2)\cdot z(1) - z(2) - z(1)];\\
A_1 &= -p(1) - p(2);\\
A_2 &= p(1)\cdot p(2);
\end{aligned}
\qquad \text{4-25}
$$

Figure 4-13 shows the PID, HB converter power stage and loop gain responses. The dc gain has been improved due to the integrator pole and the system bandwidth is 40

kHz, the phase margin is boosted to around 52^0. Thus system has large dc gain for steady state, desired BW and sufficient phase margin for transient response.

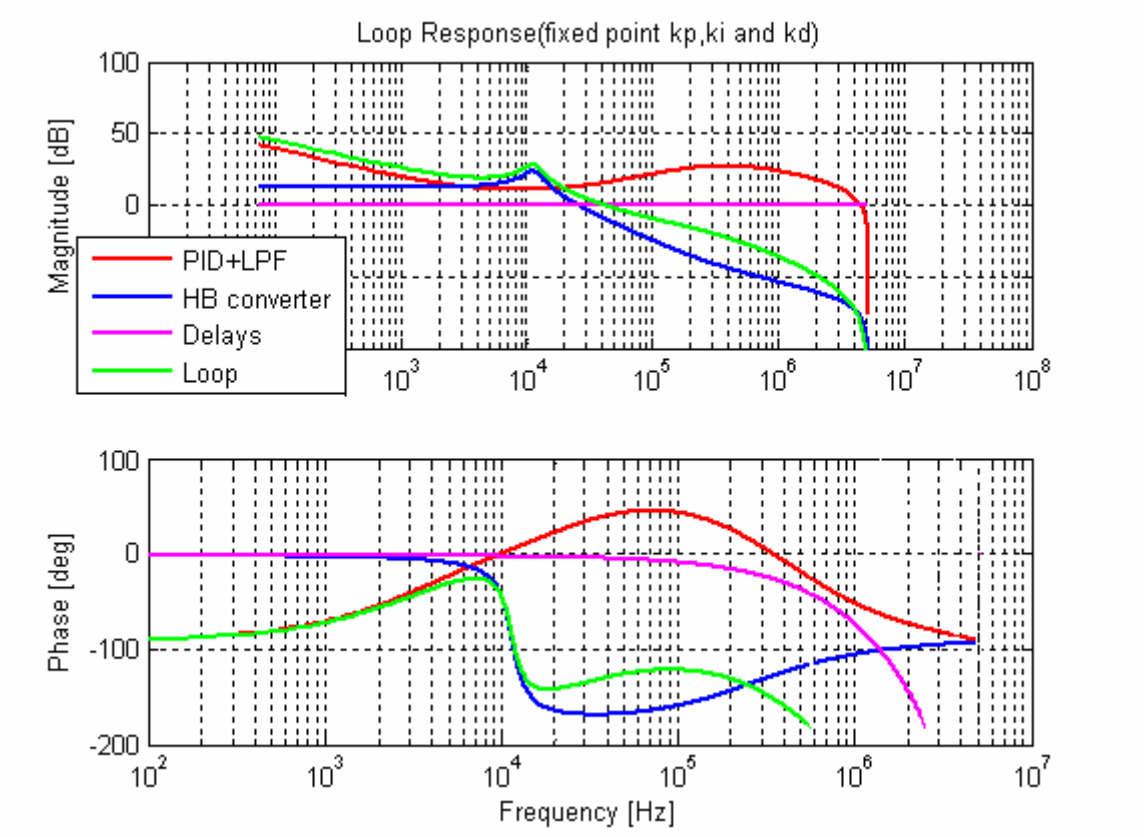


Figure 4-13 PID, HB converter, delay and loop responses

According to above placing of zero and poles, the corresponding digital coefficient codes are generated from Matlab simulation in hexadecimal values as follows:

$$kp = 0x0\mathrm{A}$$
$$ki = 0x01$$
$$kd = 0x27$$
$$a1 = 0x9C$$
$$a2 = 0x4D$$
$$a3 = 0x06$$

Figure 4-14 is the real response measured from network analyzer based on HB target board with those digital PID coefficients. The measured loop gain frequency response shows that the compensated gain bandwidth is 40.7 kHz, and phase margin is 62^0, which almost has 10^0 phase difference compared with the simulation results. The gain and phase differences between design results and real measurement are probably caused by the load condition, parasitic parameters and components temperature deviation.

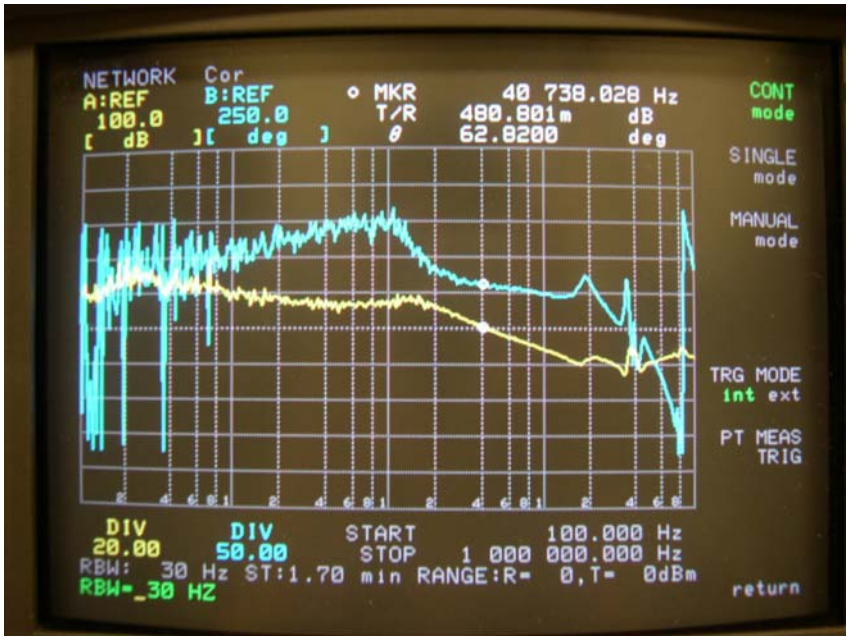


Figure 4-14 Measured HB converter response in case 1

Case 2:

In the case 2 the compensator is desired to have high bandwidth up to 90 KHz to achieve fast transient response. This compensator won't be expected large phase margin since it is supposed to be used to achieve fast transient response only during large-signal transients. This compensator design is based on the same power stage and ADC/DPWM configuration as in Case 1. The two poles are still set up at switching frequency 400 kHz and first zero at 4 kHz and second zero at 25 kHz. The corresponding PID coefficients in hexadecimal values are:

$$kp = 0x17$$
$$ki = 0x01$$
$$kd = 0x3F$$
$$a1 = 0x9C$$
$$a2 = 0x4E$$
$$a3 = 0x18$$

The loop gain frequency response is sketched in Figure 4-15. The loop BW is approximately 90 kHz and the phase margin is 55^0. But with the consideration of power stage switching delay, which is approximately $\frac{90kHz \cdot 180^0}{400kHz \cdot 2} = 20.25^0$, the final phase margin should be around 35^0 in the simulation.

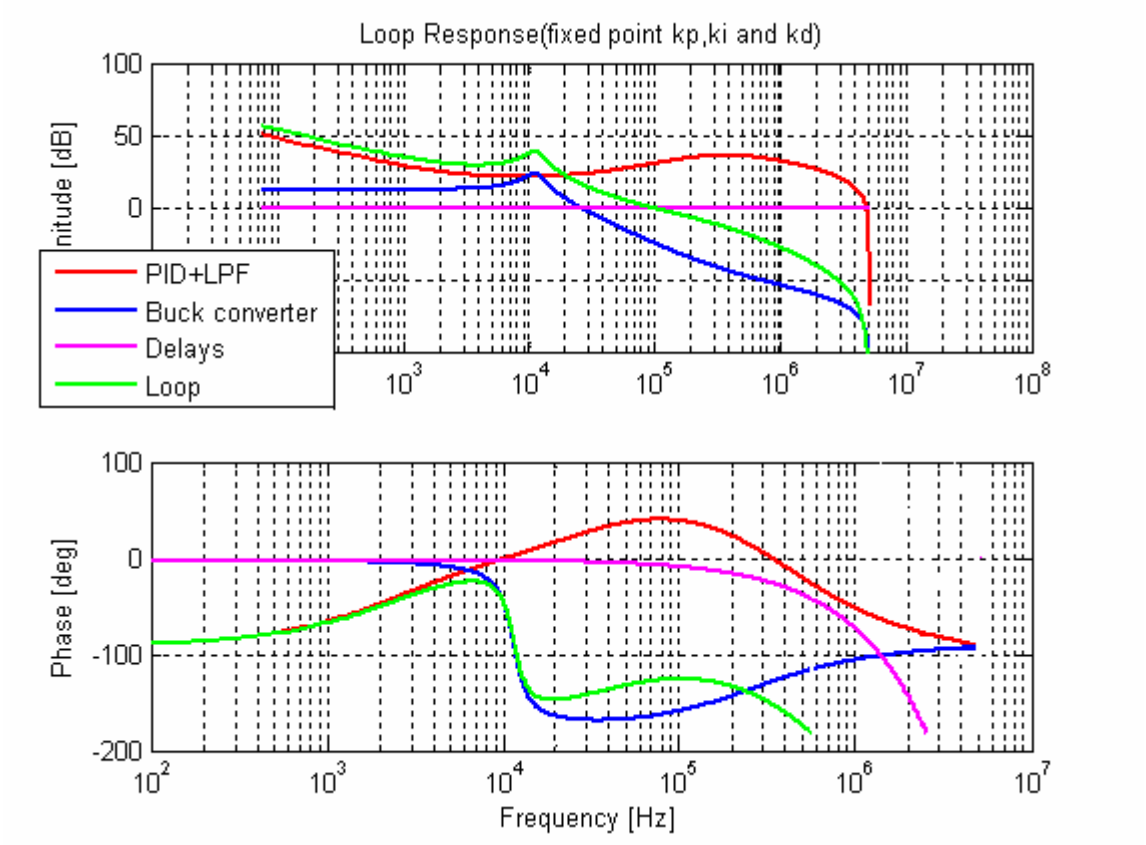


Figure 4-15 PID, HB converter, Delay and loop responses

Figure 4-16 is the frequency response measured from network analyzer, which shows that the BW is 95.5 kHz and phase margin is 30^0. Figure 4-17 shows response measurement setup for Si8250 controlled HB target board with network analyzer HP4195A. An external transformer is used to inject small signal into the loop with a small injection resistor.

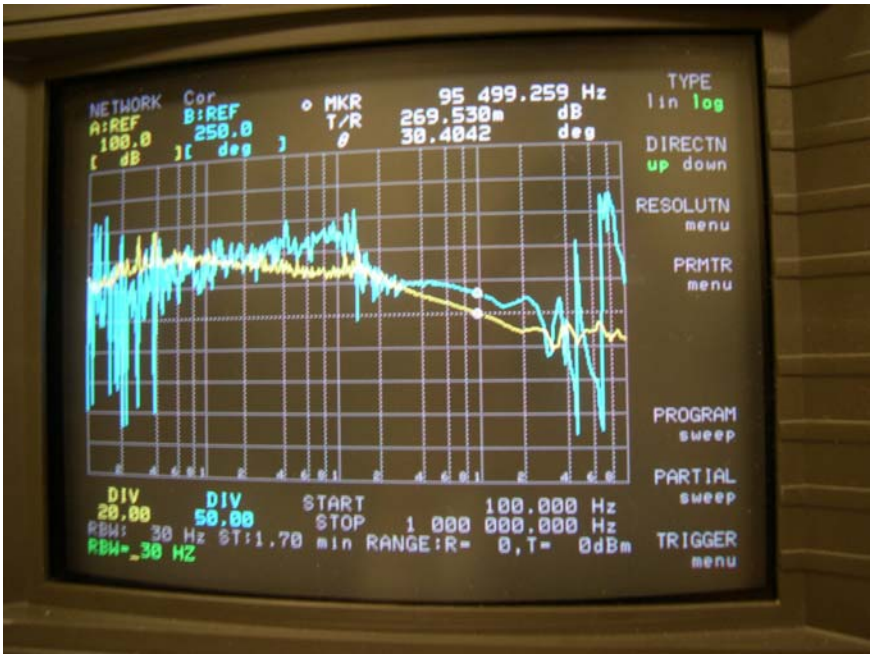


Figure 4-16 Measured response in case 2

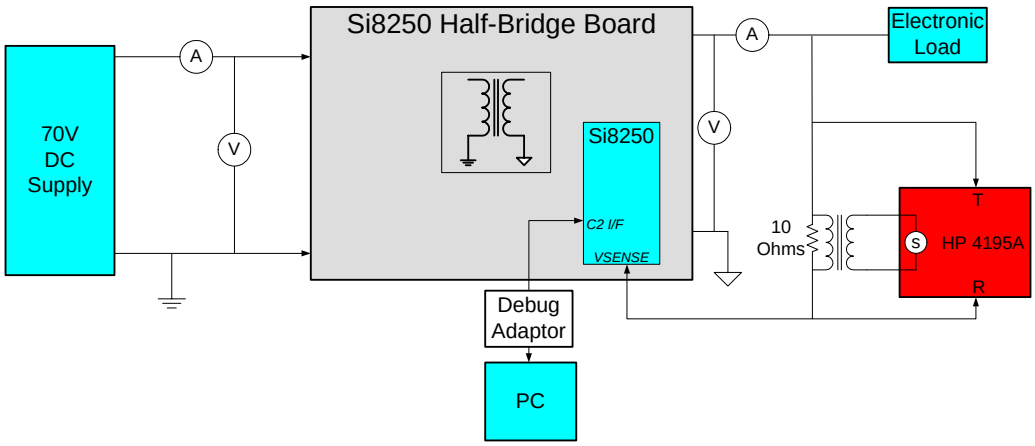


Figure 4-17 Response measurement setup

4.5.4 Transient-triggered nonlinear compensation

Transient-triggered nonlinear control algorithm based on Si8250 has already been presented in Chapter 3. Applying the same concept to the HB dc-dc converter, when load changes and output voltage reaches a low or high threshold, the transient detector detects the occurrence of a transient within a few microseconds and vectors into a transient interrupt service routine (ISR). The interrupt service routine manages to drastically increase the loop bandwidth (case 2) in such a way that system reacts faster to the transients. After the nonlinear algorithm is executed, the system management processor monitors the pattern of the output voltage error signal. Upon detection of instability, the gain of the programmable compensator is reduced and the system returns to regulation with a slower dynamic response but with adequate phase margin coefficients derived in Case 1.

Figure 4-18 shows the transient-triggered nonlinear control processing. And Figure 4-19 and 4-20 show the transient responses with and without nonlinear control algorithm when load changes from 2A to 22A at di/dt=1A/μS.

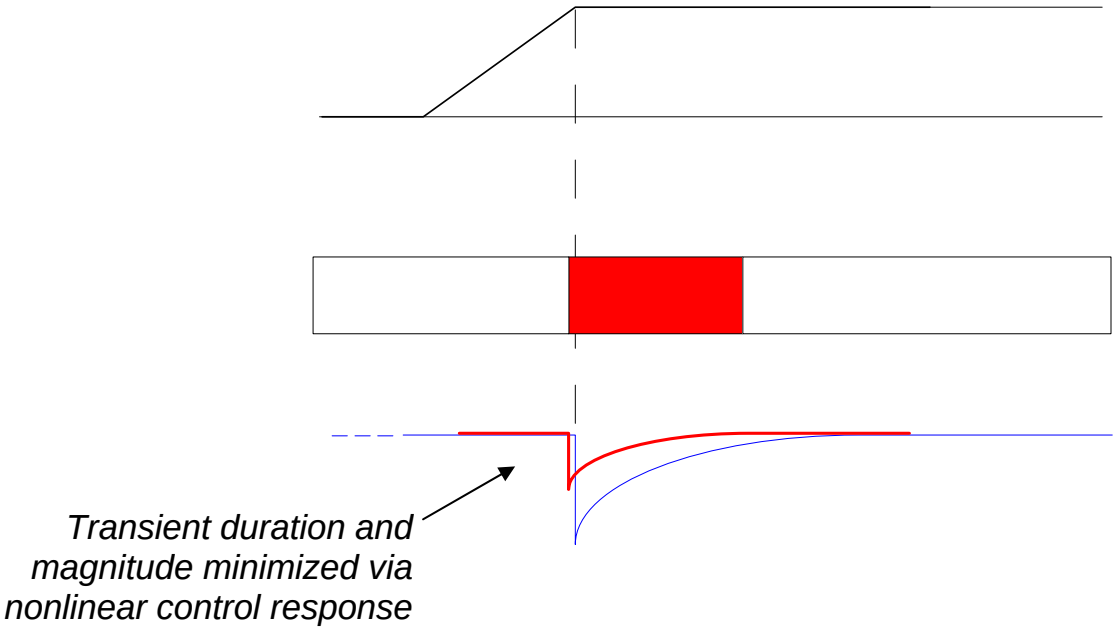


Figure 4-18 Transient with nonlinear control

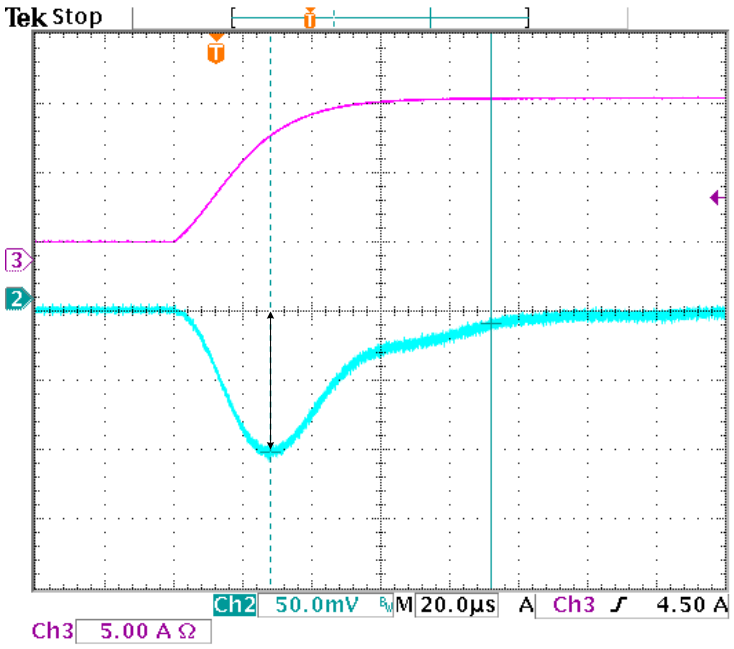


Figure 4-19 Transient response w/o nonlinear control (ΔV = 101mV, settling time = 64µS)

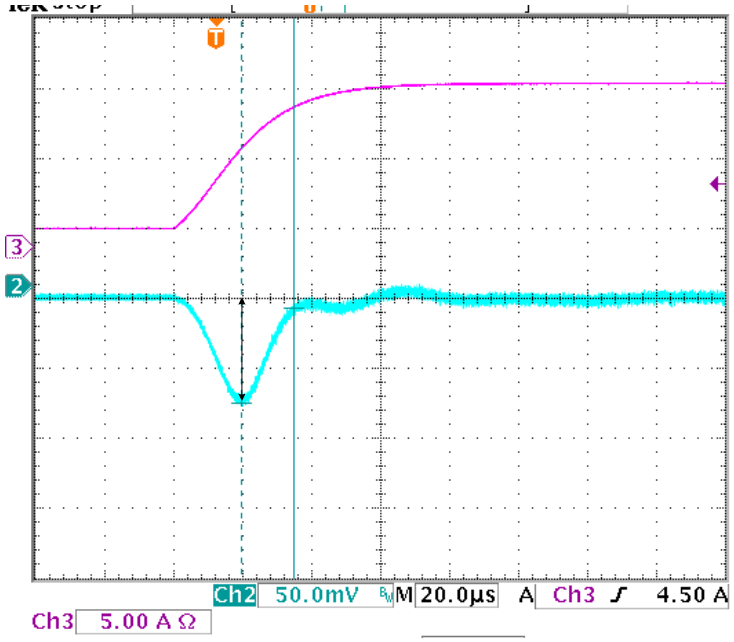


Figure 4-20 Transient response w/ nonlinear control (ΔV = 73mV, settling time = 15µS)

4.6 Summary

Unified steady-state dc model and dynamic small-signal model of the half-bridge dc-dc converters with current doublers are built based on the average model concept. The dc bias is analyzed from the dc solutions of the steady-state dc model. For asymmetrical case, uneven current sharing and dc magnetizing current bias need to be carefully considered when designing the converters. And based on the derived unified small-signal model, the output-to-control transfer functions and the output impedance for both symmetrical and asymmetrical cases are provided. By analyzing the bode plots of the output-to-control transfer functions, the controller design are discussed. Experimental results agree with the system models and analysis results.

Digital controlled half-bridge converter with Si8250 is designed and implemented. The design procedures and key issues from digital compensation perspective are presented. Transient-triggered nonlinear compensation algorithm is implemented based on the simulation feedback loop design. Simulation and experiments are aligned with each other and consequently prove the feasibility of digital controlled high frequency switching dc-dc converters.

5 DIGITALLY ADAPTIVE NONLINEAR CONTROL FOR ASYMETRICAL HALF-BRIDGE FLYBACK-FORWARD CONVERTERS

5.1 Introduction

In isolated dc-dc converters, isolation transformer links primary switching circuitry such as forward, flyback, push pull, half bridge or full bridge topologies with secondary rectifiers such as current doubler, center-tapped full wave or forward half wave rectifiers. Generally, dc-dc converters are named by primary-side topologies. Among them, half bridge is a cost-effective topology for medium power level applications, wherein the primary switches' voltage stress is lower than in flyback, forward and push pull dc-dc converters and the same as in full bridge dc-dc converter. From the complexity aspect, the half-bridge converter is similar to the push-pull and better than the full-bridge converter.

As we mentioned in Chapter 4, there are two conventional control schemes used for the half-bridge topology. One is the conventional symmetric PWM control; the other is the asymmetric (complementary) control [D1, D2]. In a symmetrically controlled half bridge dc-dc converter, the transformer operates at a symmetric and bi-directional condition, and component stresses are evenly distributed in both primary and secondary sides. However, the disadvantage is that the active switches operate at hard switching condition, and the transformer-leakage-inductance-related ringing needs to be damped with a passive snubber that results in degraded conversion efficiency [D3]. By applying complementary gate signals to the two active switches, the dead time between the two

switches is minimized and leakage inductance ringing is eliminated. More important, both the two switches may achieve Zero Voltage Switching (ZVS) [D6, D7]. These features become more desirable with the increase of switching frequency.

Conventionally, for a primary asymmetric half bridge converter, the converter's secondary rectification is either center-tapped rectifier or current doubler rectifier [D1, D2]. However, both the secondary rectification architectures are mismatched with the asymmetric primary side. In the asymmetric half-bridge dc-dc converter with a center-tapped rectifier, transformer secondary is tapped into two separate windings. Since the two windings carry different *r. m. s.* currents that varies with the duty cycle. For example, assuming the filter inductor current I_L is constant and the duty cycle value is D, one of the transformer winding's conduction loss is: $DI_L^2 R_{dc_1}$, the other transformer winding's conduction loss is: $(1-D)I_L^2 R_{dc_2}$. Under wide range of input voltage, the duty cycle variation leads to uneven conduction loss in the two transformer secondary windings, which prevents the transformer from being optimized and well utilized. Current doubler rectifier reduces transformer-winding's terminals from two to one, thus the transformer design is simplified. However, the variable asymmetric duty cycle leads to unequal current sharing between the two filter inductors, which makes the two inductors design hard to optimize since the worst case needs to be considered in the design [D4].

For low-voltage high-power-density dc-dc converters, the transformer secondary conduction loss dominates [D5]. Therefore the design optimization for transformer windings and inductors is crucial. A new topology called asymmetric half-bridge flyback-forward (AHBFF) dc-dc converter was proposed in the paper [D9], wherein forward half-wave rectification structure is utilized as the secondary rectifier. Thus, compared to the

center-tapped rectification, the transformer secondary winding structures is simplified and better transformer window utilization is achieved. Compared with the current doubler rectification, only one inductor is used and the inductor utilization is improved.

In this chapter, the operation mode and dc model analysis of this AHBFF dc-dc converter will be given. Meanwhile, the average small-signal model is derived using the average state-space small signal modeling method. Based on the model, the nonlinear characteristics are investigated and a nonlinear adaptive control is proposed and implemented in the simulation to achieve a unified loop gain and system bandwidth under load and input voltage variations based on a digital PI compensation.

5.2 Converter Description and Analysis

The asymmetrical half-bridge flyback-forward converter topology is shown in Fig. 5-1. The switch S1 and S2 are driven complementary with a short dead time. Basically, there are two principal modes of operation. One is the transformer-charging mode; the other is transformer discharging and forwarding mode. In the first mode, when the switch S2 is on, the transformer magnetizing inductance is charged in the primary, and filter inductor keeps freewheeling in the secondary. In the second mode, magnetizing energy is released to the secondary, and at the same time, the transformer delivers power from the primary to secondary.

5.2.1 DC Bias Analysis

Assume the capacitance C_1, C_2, filter inductance L and magnetizing inductance Lm are sufficiently large and the capacitor voltage ripples and inductor current ripple are negligible compared with the DC bias values at full load. Assuming the on-times of the switch S_1 and S_2 are DT and (1- D) T, respectively. During the on time of the switch S_1, the transformer primary current is $i_p = \frac{I_L}{N} - I_M$. During the on time of the switch S_2, the transformer primary current is: $-i_p = I_M$. According to ample-second balance through a capacitor, the average transformer primary current should be zero: $(\frac{I_L}{N} - I_M)D = I_M(1-D)$. We can further obtain the DC bias of magnetizing current: $I_M = \frac{I_L}{N}D$, which is positively proportional to the load current and duty cycle value D. Likewise, the DC voltage across the transformer should be zero, we can obtain the DC voltage across the capacitor $C_1$and C_2 respectively as follows: $V_{C_1} = DV_{in}$ and $V_{C_2} = (1-D)V_{in}$. Eventually, according *t*o the volt-second of the filter inductor L, the output voltage can be derived as: $V_o = \frac{V_{in}}{N}D(1-D)$.

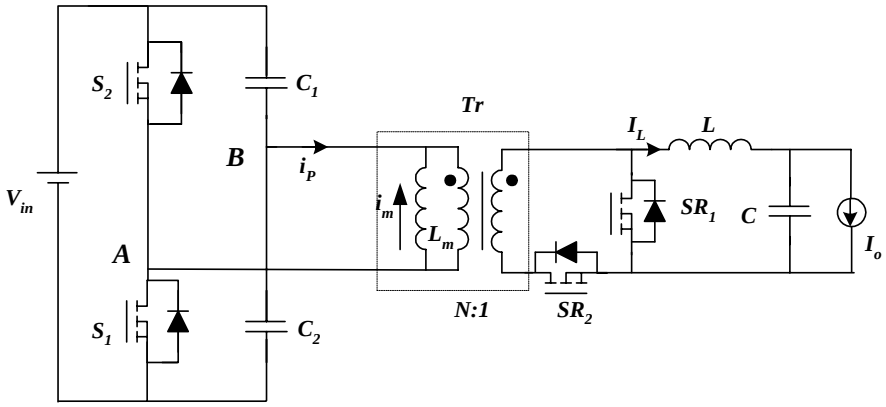


Figure 5-1 Proposed half-bridge flyback-forward converter

5.2.2 Modes of operation

All components are regarded ideal except otherwise indicated. To simplify the analysis, secondary synchronous rectifiers can be simplified as ideal diodes with ideal characteristics. The modes of operation are described as follows (related equations will be included in the final version considering the page limitation of the digest):

Mode 1 ($t< t_1$): During the mode, the switch S_2 is on, transformer magnetizing and leakage inductance are charged by the capacitor C_1. On the secondary, SR_2 is blocked and filter inductor current freewheels through SR_1.

Mode 2 ($t_1 < t < t_2$): At $t=t_1$, the switch S_2 turns off, and the leakage inductance current charges the junction capacitance C_{j2} and discharges C_{j1}. Thereafter the SR_2 start conducting and transformer secondary becomes shorted.

Mode 3 ***($t_2 < t < t_3$):*** At $t=t_2$, the junction capacitance voltage across C_{j1} discharges to zero, and the body diode of the switch S_1 starts carrying current. The leakage inductance current continues decreasing while transformer secondary current i_s keeps increasing.

Mode 4 ***($t_3 < t < t_4$):*** At $t=t_3$, the switch S_1 turns on at zero-voltage switching (ZVS). The leakage inductance current continues being reset through the switch S_1 until it reaches zero, then the leakage inductance current is reversely charged through the switch S_1. The transformer secondary current i_s keep increasing in this mode.

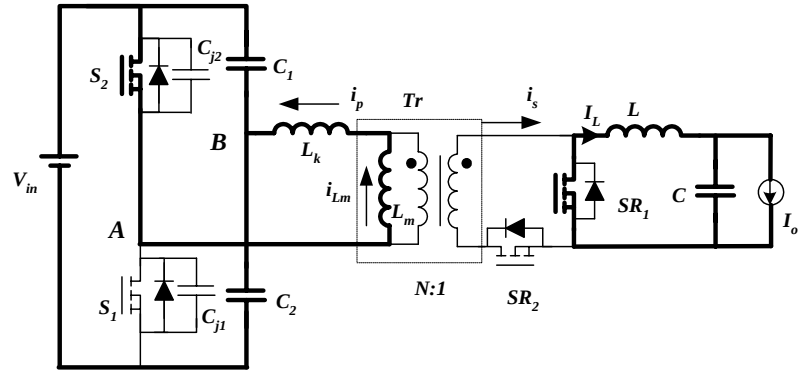
Mode 5 ***($t_4 < t < t_5$):*** At $t=t_4$, the transformer secondary current i_s reaches the filter inductor current, as a result, the SR_1 is blocked. The converter goes into power delivering mode. In the mode, the transformer releases magnetizing energy to the output. At the same time, input power is delivered to output through the transformer.

Mode 6 ***($t_5 < t < t_6$):*** At $t=t_5$, the switch S_1 turns off, and the leakage inductance current charges the junction capacitance C_{j1} and discharges C_{j2}. With the decrease of primary leakage inductance current, SR_1 start conducting and thereafter transformer secondary is shorted.

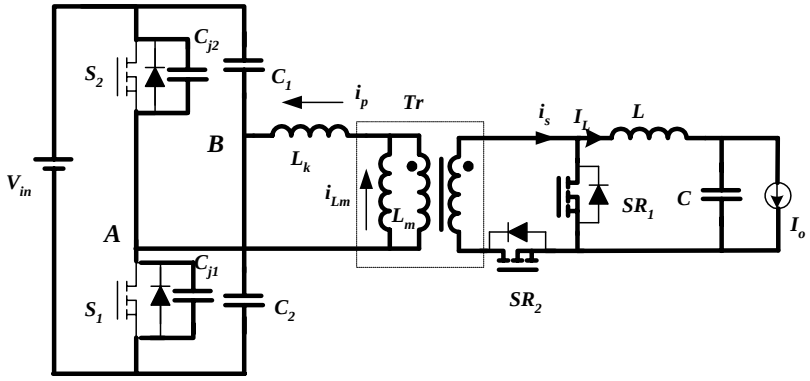
Mode 7 ***($t_6 < t < t_7$):*** At $t=t_6$, the junction capacitance voltage across C_{j2} discharges to zero, and the body diode of the switch S_2 starts carrying current. The leakage inductance current continues decreasing while transformer secondary current i_s keeps decreasing.

Mode 8 ***($t_7 < t < t_8$):*** At $t=t_7$, the switch S_2 turns on at zero-voltage switching (ZVS). The leakage inductance current continues being reset through the switch S_2 until it reaches zero, then the leakage inductance current is reversely charged. During the mode, the transformer secondary keeps shorted. With the increase of leakage inductance current, the transformer secondary current i_s keep decreasing until it reaches zero. At this moment,

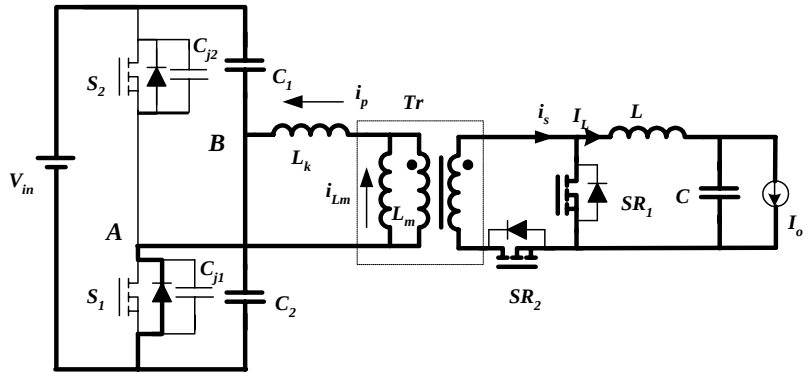
transformer leakage inductance current is equal to magnetizing current. Thereafter, the transformer voltage blocks the SR_2, the converter goes back to Mode 1.



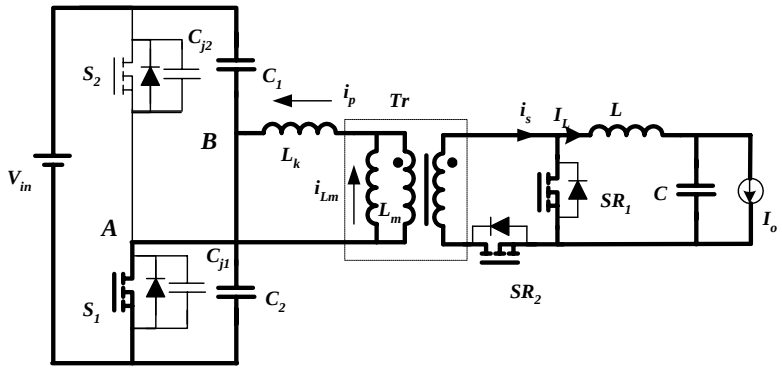
Mode 1



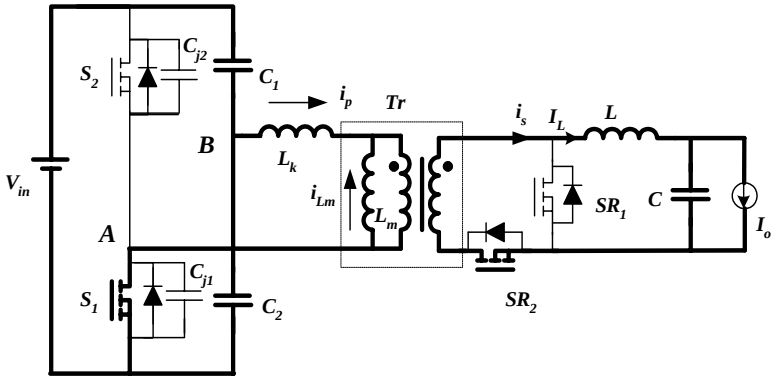
Mode 2



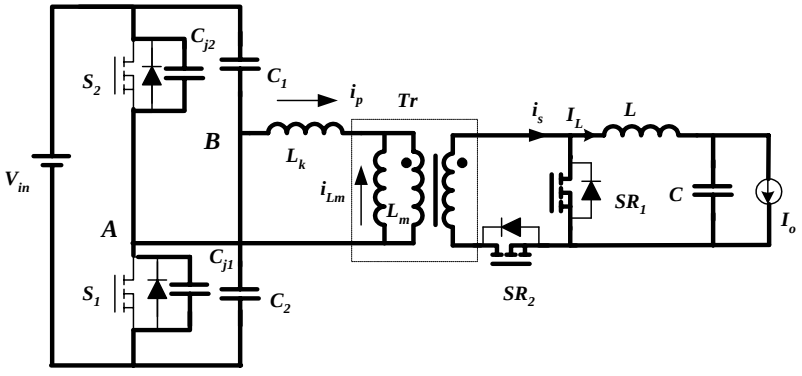
Mode 3



Mode 4



Mode 5



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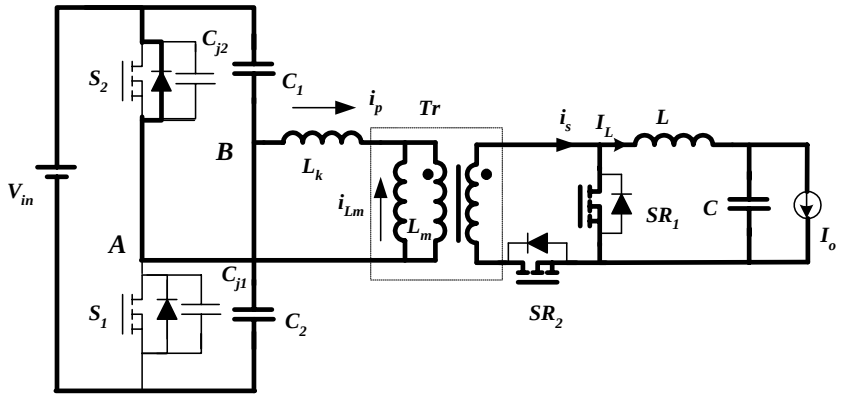
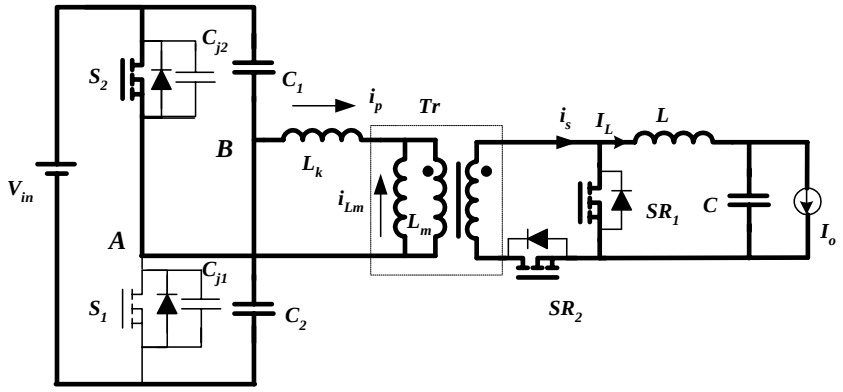


Mode 7



Mode 8

Figure 5-2 Modes of operation

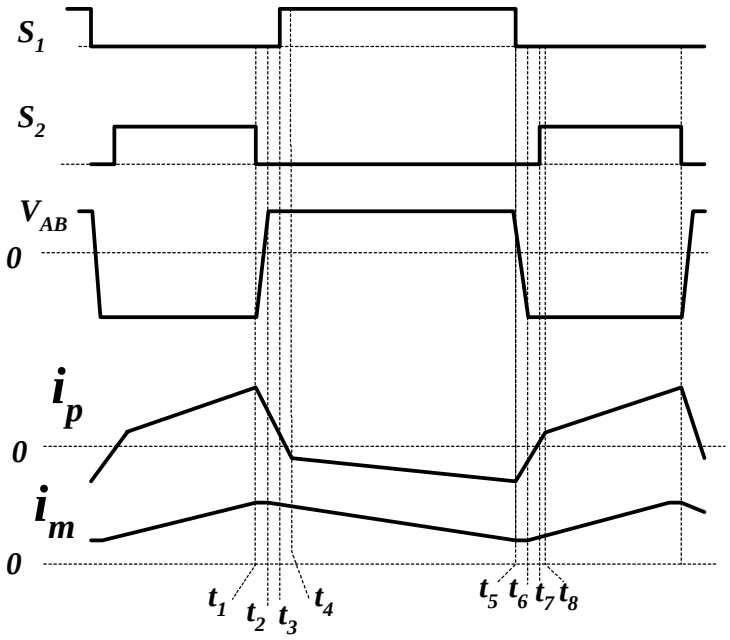


Figure 5-3 Key waveforms of the proposed converter

5.2.3 Features and design Considerations

From the analysis above, it is clear that both the switches achieve ZVS. Moreover, the leakage inductance ringing and related loss are eliminated since the dead time between the two switches is very short. Those are favorable features for dc-dc converters operating high switching frequencies. Compared with active-clamp forward converter, the converter primary voltage stress is reduced and two switches instead of a single switch share the current stress. In addition, the transformer turn ratio is smaller than in forward converter, which leads to lower primary turns for converters with low output

voltage where it is always the case that only one turn is necessary for the transformer secondary winding.

Compared with asymmetric half bridge with a center-tapped rectifier, under a certain design, the transformer turn ratio is same, transformer secondary winding count is reduced from 2 to 1, and thus double copper window area can be used for transformer secondary winding. This is desirable for high current output converters since second conduction loss is significant in the converters. Since the dead time of the converter is minimized, the secondary SRs can be self-driven with transformer windings. Compared with asymmetric half bridge with current doubler rectifier, the converter has simpler rectifier architecture since only an inductor is used, which is desirable for the applications with relatively lower output current requirement.

5.3 Small-Signal Model of Asymmetric HB Flyback Forward Converter

Applying the averaging small-signal modeling technique, the small-signal model of the power stage can be derived [D8]. In a switching cycle, the converter can be denoted using two linear state-space equations, respectively, as the following:

$$\dot{x} = A_m x + B_m u \quad (m = 1,2); \qquad y = Cx + Eu \tag{5-1}$$

So according to the concept of state-space averaging, the unified state-space equation is:

$$\dot{x} = Ax + Bu \qquad y = Cx + Eu \tag{5-2}$$

Where the equivalent matrices are defined by: $A = DA_1 + (1-D)A_2$; $B = DB_1 + (1-D)B_2$, and the DC solution of the unified state-space equation can be obtained by solving the equation $X = -A^{-1}BU$ as follows:

$$
\begin{aligned}
V_{C_1} &= (1-D) * V_{in} \\
I_L &= I_o \\
V_o &= \frac{D(1-D)}{n} V_{in} \\
I_M &= DI_o
\end{aligned}
$$

5-3

The small-signal model of the AHB converter can be derived with perturbing the unified state-space average equation as follows:

$$y = Y + \hat{y} \quad x = X + \hat{x} \quad u = U + \hat{u} \quad d = D + \hat{d} \qquad \text{5-4}$$

Substituting Equation 5-4 into 5-2 and removing the DC bias from the obtained equation and ignoring high-order terms, small-signal model of the AHB converter can be derived as the following:

$$
\begin{aligned}
\hat{x}(s) = {} & (sI - A)^{-1} B\hat{u}(s) + (sI - A)^{-1} * \\
& [\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)]X + \\
& (sI - A)^{-1}[\hat{d}_1(s)(B_1 - B_3) + \hat{d}_2(s)(B_2 - B_3)]U
\end{aligned}
\qquad \text{5-5}
$$

The output-to-control transfer function can be obtained:

$$\frac{\hat{y}(s)}{\hat{d}(s)}\Big|_{\hat{u}(s)=0} = C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U] \qquad 5\text{-}6$$

Considering all the parameters, the output-to-control transfer function is too complicated to fit into page here, but the transfer function can be described as the following form:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)}\Bigg|_{\hat{v}_{in}(s)=0} = \frac{V_{in}(1-2D)}{n}\frac{(b_0 s^3 + b_1 s^2 + b_2 s + 1)}{(a_0 s^4 + a_1 s^3 + a_2 s^2 + a_3 s + 1)} \qquad 5\text{-}7$$

Where a_0~a_4 and b_0~b_3 are constants determined by the converter resistance parameters. It is clear that $\frac{V_{in}(1-2D)}{n}$ is the dc gain of the transfer function. In the following sections, exactly accurate equations derived are used for the bode plots.

5.4 Adaptive Nonlinear Compensation for HB Flyback Forward Converter

5.4.1 Algorithm analysis

From the equation 5-7, the output-to-control transfer function has a dc gain that is a function of input voltage and the duty cycle that represents converter's operating point. For a closed-loop system, the output-to-control transfer function is the representative of the plant. Therefore the dc gain of $\frac{V_{in}(1-2D)}{n}$ in the small-signal output-to-control

transfer function plays an important role in frequency response since it affects the system bandwidth, phase/gain margin resulting various system performance.

Under a certain input voltage, there are a corresponding steady-state duty cycle and a dc gain of output-to-control transfer function. Both of them are nonlinear in term of input voltage as shown in Figure 5-4. From Figure 5-4, it is observed that the small-signal dc gain changes with input voltage.

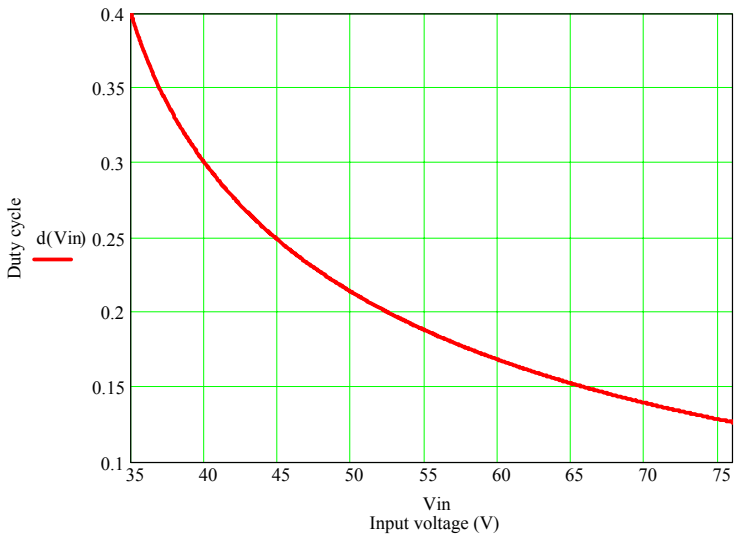
The derived small-signal transfer function under various input voltage is plotted in Figure 5-5 (a), from which it is clearly observed that the gain curve varies with the input voltage. Considering the worst case of input voltage, a PID compensator is designed, and the system loop gain bode plot is plotted in Figure 5-5 (b). It can be observed that the bandwidth changes with input voltage. At high line ($V_{in} = 75V$), the system has higher bandwidth but lower phase margin. In applications with requirement of high bandwidth and fast transient response, those variations of system frequency response become very critical. Compromise has to be made between transient response and system stability in the design.

Considering the loop gain variation, high-line input is the worst case when designing the feedback loop. However, the design could not achieve aggressive bandwidth, phase margin and transient response under nominal input voltage. So the good solution is to compensate the gain and bandwidth adaptively using a feedback loop. In other words, by feed back input voltage and duty cycle, the small-signal DC gain is adjusted to be independent of input voltage line.

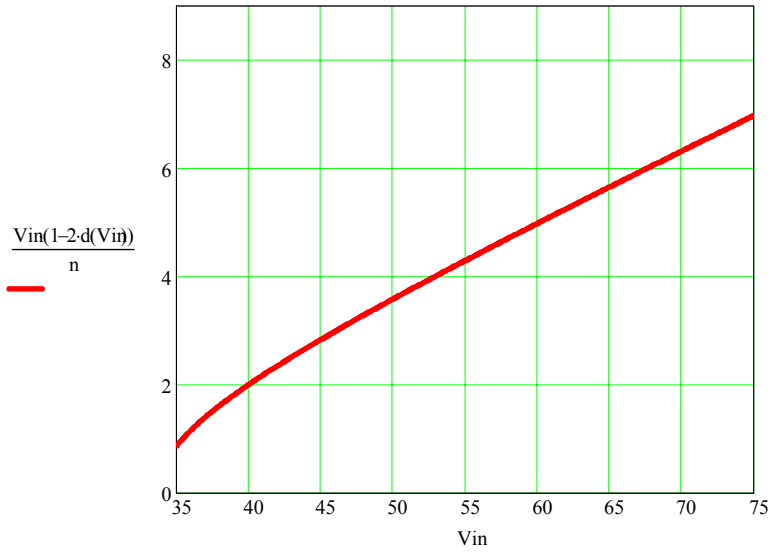
To achieve the constant gain, nonlinear compensation has to be added in the control loop. In the compensator, an adaptive gain factor $\frac{K_0}{V_{in}(1-2D)}$ is added in series with the feed back loop, which adaptively cancels the gain variation from input voltage and duty cycle. The coefficient K_0 is can be designed in nominal condition. With the gain scale factor, the small-signal transfer function in Equation 5-7 is corrected as:

$$\left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{K_0}{n}\frac{(b_0 s^3 + b_1 s^2 + b_2 s + 1)}{(a_0 s^4 + a_1 s^3 + a_2 s^2 + a_3 s + 1)} \qquad 5\text{-}8$$

It is observed that the above equation is independent of input voltage and duty cycle, and thus the plant transfer function can be compensated without considering the input voltage and operating point.



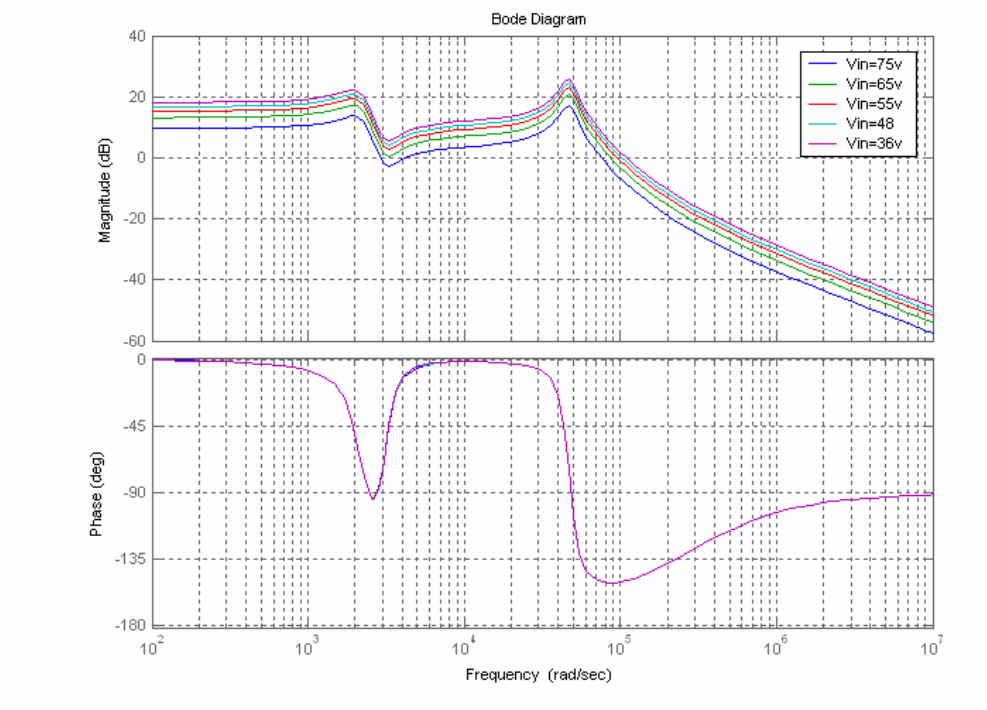
(a) Duty cycle vs. input voltage



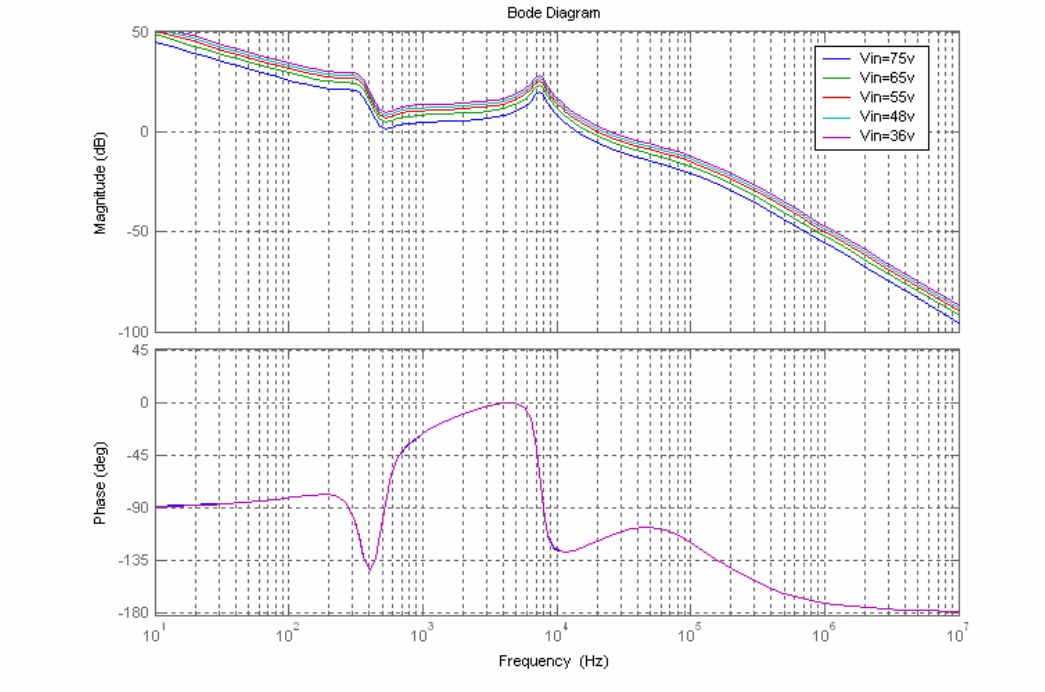
(b) DC gain vs. input voltage

Figure 5-4 Closed-loop steady-state duty cycle and dc gain of small-signal transfer function vs. input voltage

With this concept, the input voltage and duty cycle is fed back to a nonlinear block, which generates a gain scale factor to adaptively compensate the original variable loop gain. The loop gain with the nonlinear gain factor adjustment is plotted in Figure 5-6, where a unified loop gain bode plot is achieved regardless of input voltage change. In other words, theoretically, the system has consistent steady state and dynamic performance under variation of input line and load change.



(a) Bode plot of the output-to-control transfer function under various input voltage (36V~75V)



(b) Bode plot of closed-loop loop gain under various input voltage (36V~75V)

Figure 5-5 Bode plot of the plant and conventional PID controlled loop gain

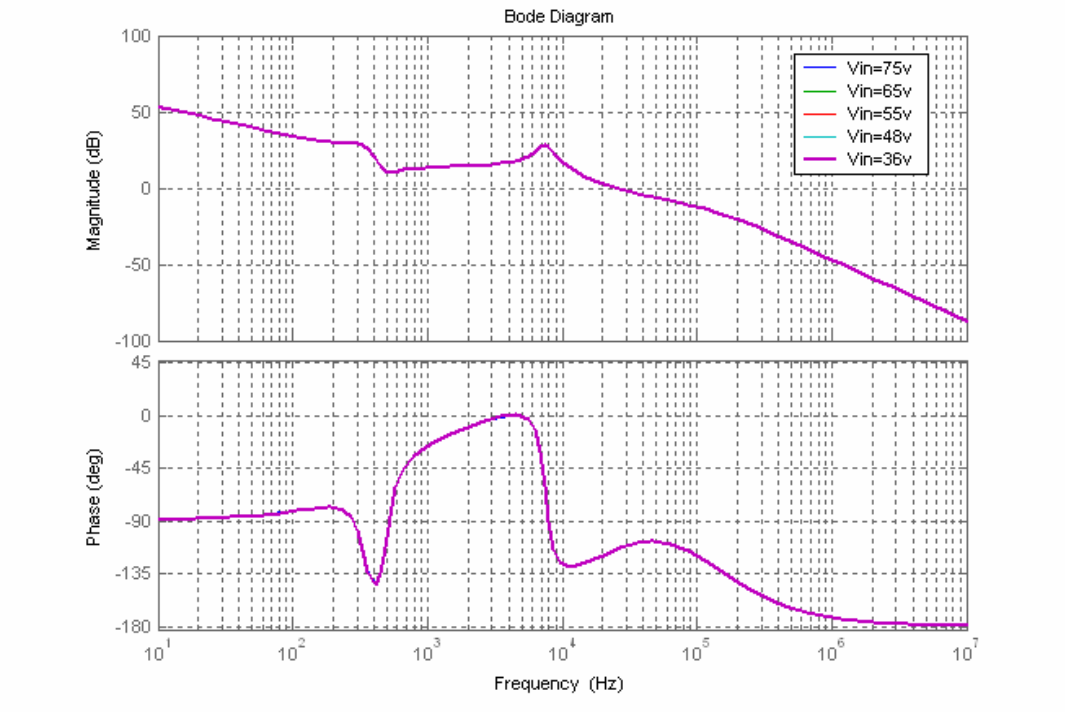


Figure 5-6 Closed-loop frequency response of loop gain with adaptive dc gain adjustment

5.4.2 Simulation Verification

It would be difficult for an analog controller to compensate the small-signal gain variation of AHBFF topology. But digital control features excellent flexibility to implement such kind of schemes. A digital controller with a nonlinear gain adjustment algorithm is simulated based on PSIM software platform. PSIM is powerful software that provides AC sweep while allowing the circuit operating at nonlinear operation.

The simulation schematic is shown in Figure 5-7. Based on the conventional digital PI compensator, a nonlinear loop gain adjustment block is added in the controller. Input voltage and steady-state duty cycle are sensed, sampled and fed/forwarded to the

nonlinear block to generate a gain adjustment factor. The desired gain compensation is calculated in block, which outputs the gain factor $K = \frac{K_0}{V_{in}(1-2D)}$, which is multiplied by the output of the digital PI controller.

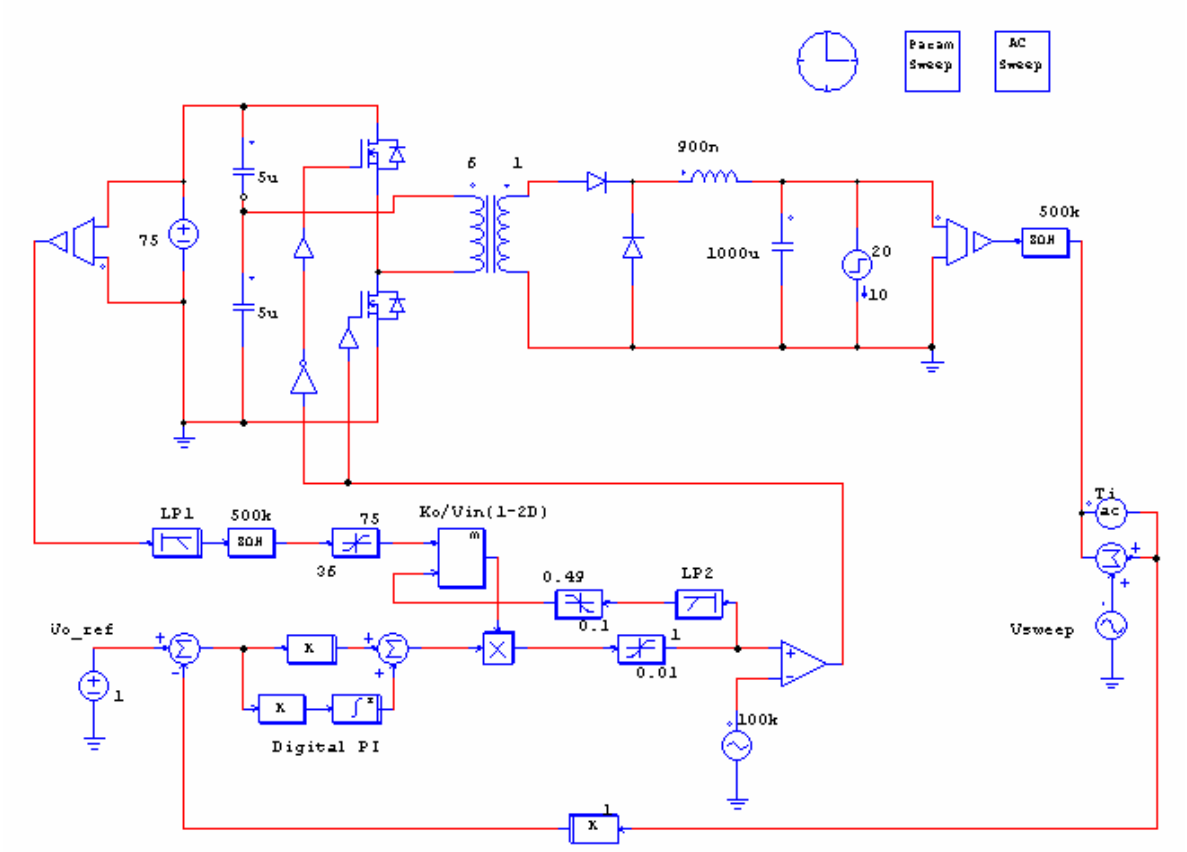


Figure 5-7 Closed-loop AHBFF converter with digital adaptive gain compensation

It should be noted that, two low pass filters must be added in the sense loops to achieve system stability. The gain adjustment loop is allowed to respond relatively slowly compared with the main voltage regulation loop without affecting system dynamic

performance. Therefore, the added algorithm is less expensive in the microprocessor resource utilization.

Based on the simulation schematic, the power train is swept and output-to-control bode plot of the power train is plotted in Figure 5-8, which closely agrees with the previous theoretical analysis result as shown in Figure 5-5(a).

A conventional digital PI compensator is designed with the adaptive dc gain compensation block. The closed-loop frequency responses are shown in Figure 5-9. It is observed that the loop gain and phase margin basically agrees with analysis. The differences come from the low pass filtering of the input voltage and duty cycle sense blocks.

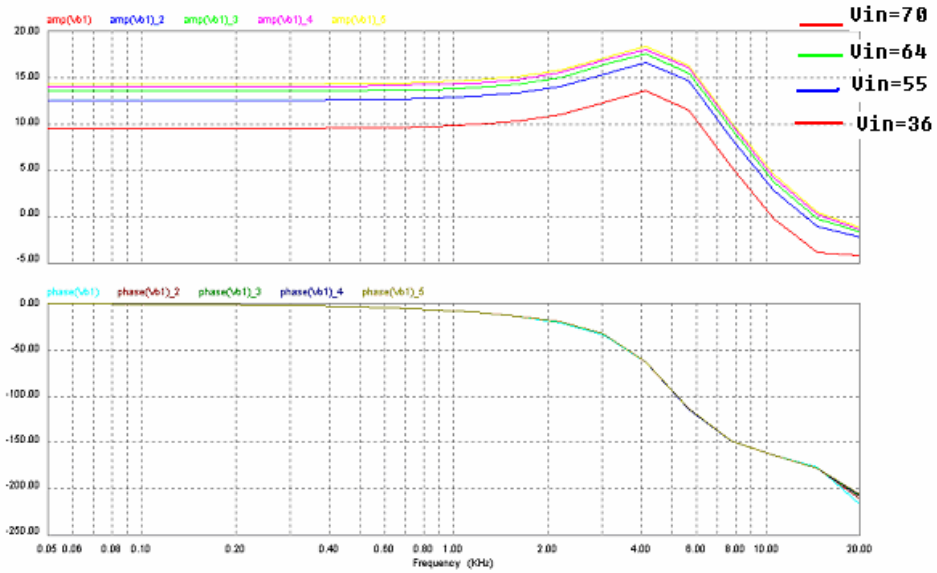


Figure 5-8 Bode plot of the output-to-control transfer function based on AC sweep of power train

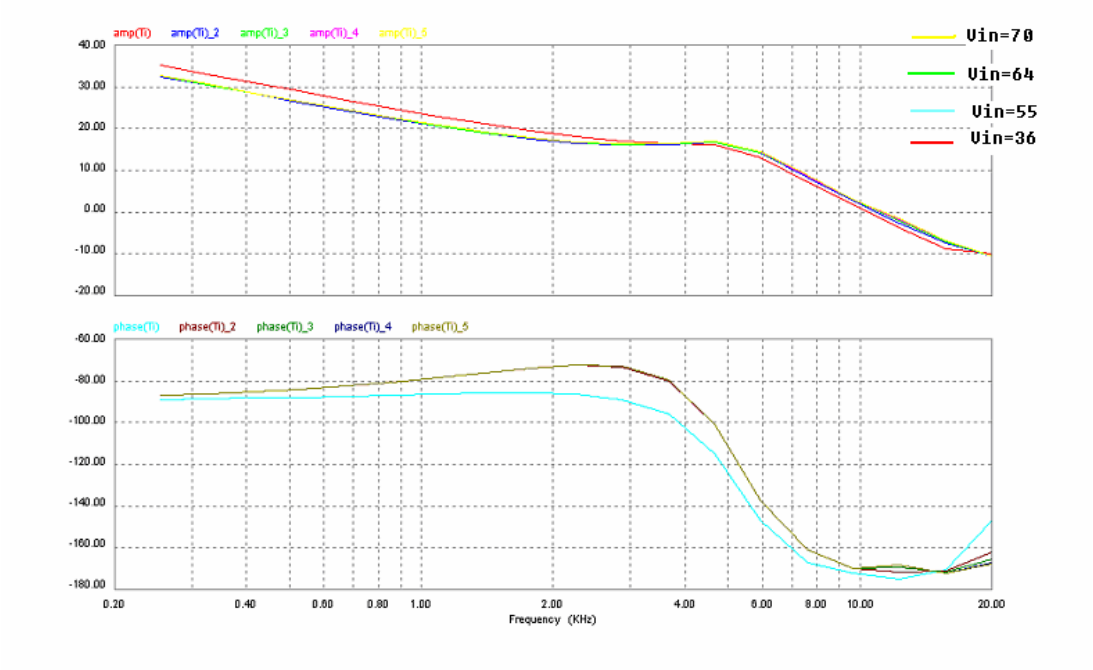


Figure 5-9 Closed-loop bode plot with the proposed control

5.4.3 Experiment Results

A prototype is built with the AHBFF dc-dc topology, and the key specifications are as follows: $V_{in} = 36 \sim 75V$, $V_o = 1V$, $I_{out} = 25A$. TI's TMS320C2812 DSP, which has a 32-bit DSP core delivering 150 MIPS performance, is used to implement the digital controller with a first order digital PI compensator and adaptive gain adjustment algorithm. The prototype and DSP demo board is shown in Figure 5-10.

Digital PI design is based on the continuous time domain transfer function of power stage. Compensator design is derived in continuous time and then mapped to discrete time domain. The corresponding difference equation based on Z-form PI equation is

implemented with DSP firmware. Figure 5-11 shows the flowchart of the control algorithm.

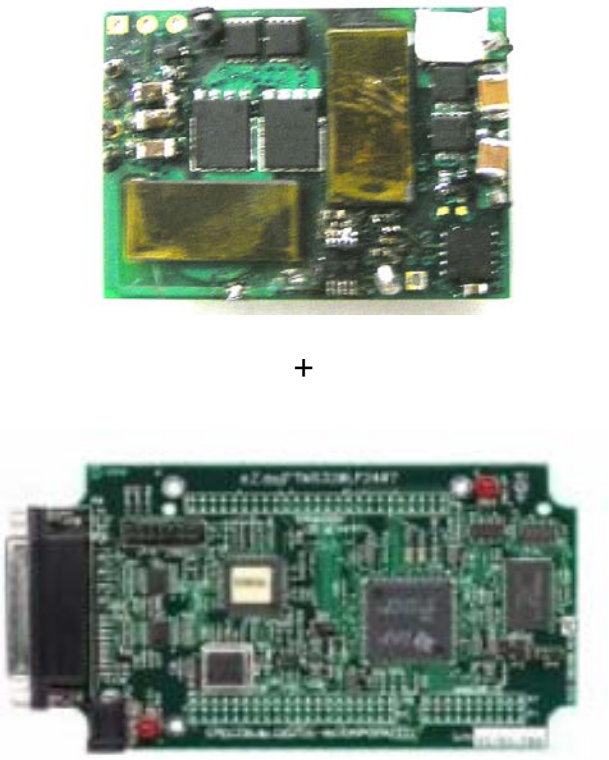


Figure 5-10 Prototype of AHBFF converter and the DSP controller

Figure 5-12 and Figure 5-13 compare the transient response at 75Vin with and without loop gain compensation scheme. It is observed that the voltage response in Figure 5-13 is improved in terms of undershoot voltage and damping effect, because higher phase margin is achieved at high line with the help of the adaptive digital DC gain compensation.

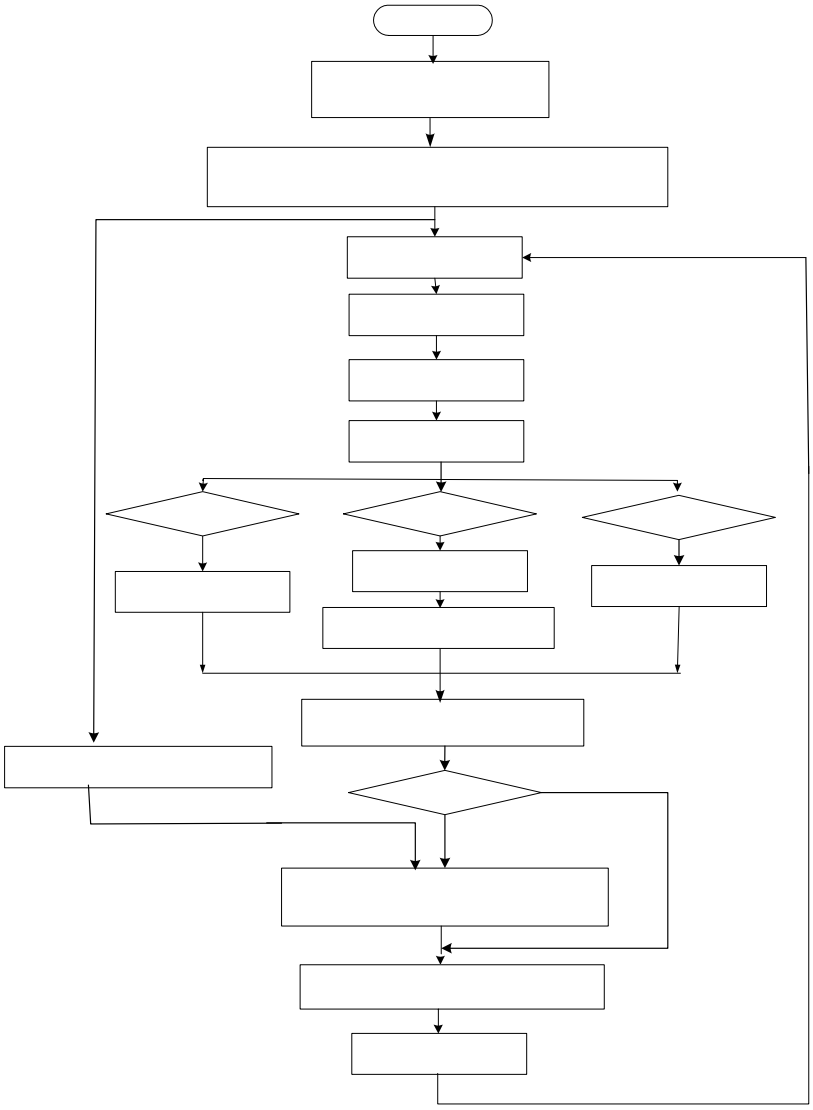


Figure 5-11 Proposed nonlinear compensation flowchart

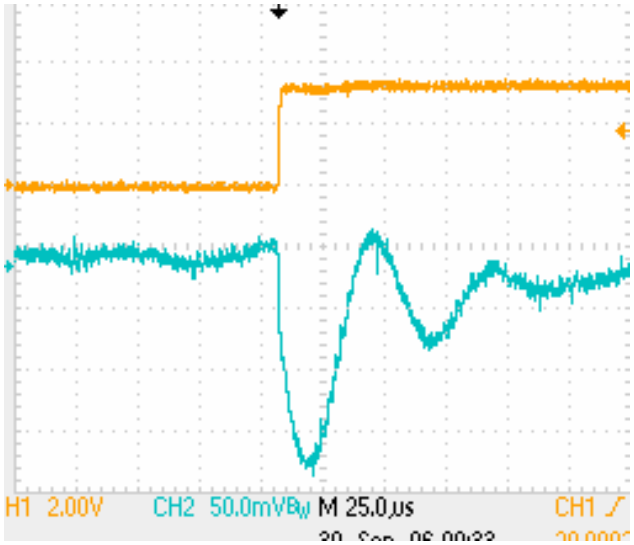


Figure 5-12 Load change transient response at Vin = 75V

(With conventional PI compensator)

(Bottoms trace: output voltage; Top trace: Output current)

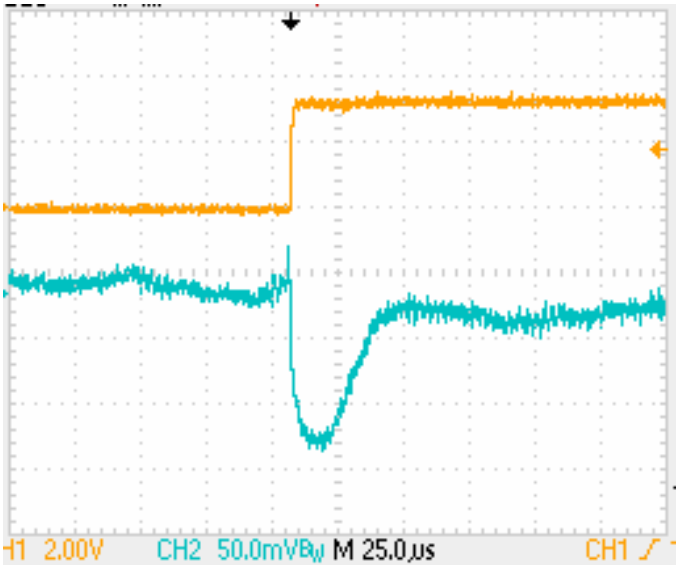


Figure 5-13 Transient response at Vin = 75V

(With the proposed digitally adaptive gain compensation control)

(Bottoms trace: output voltage; Top trace: Output current)

5.5 Summary

Asymmetric Half-Bridge Flyback-Forward converter has been proved favorable for lower output current applications due to its simpler transformer winding structure, better transformer window utilization and better utilization of filter inductor [D9]. The gain variation of this topology results in system performance deviation when input voltage or duty cycle changes. Usually, the gain variation is compensated by feedforward voltage. However, the nonlinearity of gain variation of this AHB topology causes difficulties in compensating for analog design, on the contrary, digital control implementation features excellent nonlinear flexibility in this situation. The simulation and experiment have verified the proposed nonlinear gain compensation scheme and the consequent improvement of the dynamic performance of converters.

6 UNIFIED DIGITAL PWM CONTROL SCHEME FOR HALF-BRIDGE DC-DC CONVERTER

6.1 Introduction

It's been known that soft-switching techniques are the prevailed solution to reduced switching losses, which are intensively investigated in the last two decades. Some of invented techniques, such as active-clamp forward converter and full-bridge phase-shifted converter, have been widely applied to DC-DC isolated DC-DC conversion products. Several techniques for high frequency DC-DC conversion have been proposed to reduce component stresses and switching losses while achieving high power density and improved performance [E1-E11]. Among them, the phase-shifted zero-voltage-switching (ZVS) full bridge [E1-E3] is one of the most attractive techniques since it allows all switches to operate at ZVS by utilizing transformer leakage inductance and MOSFETs' junction capacitance without adding an auxiliary switch. However, the complexity of the full-bridge is almost highest among the conventional topologies due to its large switch count and complicated control and driving. Active-clamp forward topology [E4-E6] is another typical example to successfully realize ZVS for the switches by utilizing the leakage inductance, magnetizing inductance and junction capacitance. However, the topology of the converter is asymmetric and the energy-delivery is unidirectional. In other words, voltage and current stresses are unevenly distributed, which results in the individual switch and rectifier stresses being higher compared to symmetric half-bridge and full-bridge converters. This disadvantage limits power level of

the active-clamp forward topology applications. In addition, DC bias of magnetizing current may exist in the transformer [E5].

As the discussion in previous chapters, Half bridge (HB) dc-dc converter is an good topology for moderate power level applications owing to its cost effectiveness. Symmetric and asymmetric controlled HB converters are two well-known conventional HB DC-DC converters. The main drawback of the symmetric control is that both primary switches of the converter operate at hard switching condition. Moreover, during the off-time period of two switches, the oscillation between the transformer leakage inductance and switch junction capacitance results in energy dissipation and EMI problems. To suppress the ringing, dissipative snubbers are usually applied across switches or transformer primary side.

Asymmetric (complementary) control was proposed to achieve ZVS operation for primary switches [E7-E11]. Two drive signals are complementarily generated and applied to the high-side and low-side switches. Thus, the two switches could turn on at ZVS conditions with the help of transformer leakage inductance. However, asymmetric electrical stress distribution occurs due to the asymmetric duty cycle for the two primary switches. The asymmetry becomes even worse at high input voltage. Therefore, the asymmetric PWM control is not suitable for applications accommodating to wide range of input voltage [E10].

As a solution to reduce the uneven voltage and current stress, a PWM control concept, known as “duty-cycle-shift” (DCS) PWM was proposed in [E12-E13] for HB dc-dc converters. The control scheme achieves ZVS for one of the two switches and eliminates the asymmetric penalties existed in the asymmetric controlled HB dc-dc

converter. The concept of DCS PWM scheme is shifting one of the two symmetric PWM drive pulses close to the other, such that ZVS could be achieved for the lagging switch due to the minimized resonant interval. Unlike the asymmetric control, the pulse width of the drive signals for the two switches keeps equal in the DCS PWM scheme, such that all reciprocal components work at the conditions with even voltage and current stress as the case in the symmetric control scheme.

In this chapter, DCS PWM control concept is improved to a unified digital PWM control scheme, which allows HB dc-dc converters to operate at asymmetric control at low input voltage and the original DCS control at high input voltage, and thus combines the advantages of DCS PWM scheme and asymmetric control. Moreover, the maximum voltage stress across a secondary rectifier is significantly reduced compared with the asymmetric control, such that components with lower voltage ratings can be selected. Mathematical model is established to analyze HB dc-dc converter controlled by the proposed PWM scheme. The proposed scheme is implemented with a digital controller Si8250, and by adaptively changing a modulation coefficient, the control scheme allows a converter to slide from asymmetric control to the original DCS control, or vice versa.

6.2 Proposed Unified PWM Control Concept for Half Bridge DC-DC Converter

6.2.1 Brief Review of PWM Control Schemes for HB Converter

Figure 6-1 shows the half-bridge dc-dc converter with current doubler rectifier. The ideal waveform for the symmetric PWM control is sketched in Figure 6-2 (a). It is observed that the drive signals are symmetrically allocated, and thus the voltage and

current stress are evenly distributed in the circuit. Besides the hard-switching operation, the converter suffers transformer-leakage-inductance ringing during the off-time interval when both switches are off. The energy stored in the transformer leakage inductance may be recycled to primary DC bus through body diodes of MOSFET, however, because of reverse recovery current of body diodes, the oscillation between the transformer leakage inductance and the primary MOSFETs junction capacitance is significant. To suppress the ringing, usually, snubber circuits are necessarily added, but losses dissipated in the snubber become dramatically large, especially at high input current and high switching frequencies.

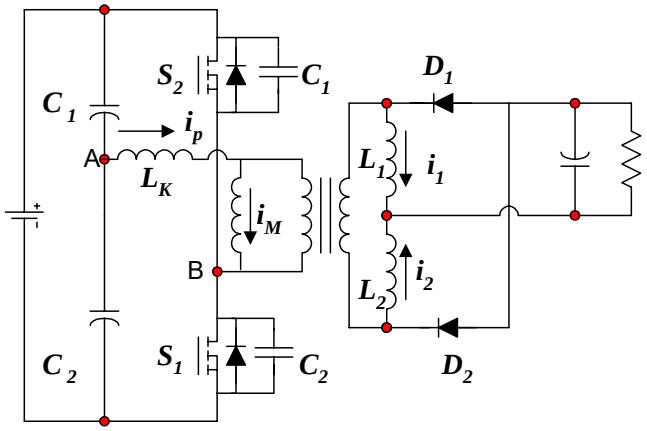


Figure 6-1 Half-bridge DC-DC converter with current doubler rectifier

Figure 6-2(b) shows the key waveforms of the HB dc-dc converter with original DCS PWM control. Based on the symmetric PWM control, S_2 drive signal V_{gs2} is shifted left such that the V_{gs2} rising edge is close to the falling edge of S_1 drive signal V_{gs1}. When S_1 is turned off, the transformer primary current charges the junction capacitance of the switch S_1 and discharges the junction capacitance of the switch S_2. After the voltage across drain-to-source of S_2 drops to zero, the body diode of S_2 conducts to carry the

current. During the body diode conduction period, S_2 may be turned on at zero-voltage switching. No ringing occurs during the transition period. By shifting one of the symmetric PWM driving signals, Zero-Voltage-Switching (ZVS) is achieved for one of the switches without adding extra components and without adding asymmetric penalties of the complementary duty cycle control since pulse width applied to both the switches are identical. This control concept reduces the switching losses and transformer leakage-inductance-related losses. These losses significantly degrade the converter efficiency, especially when operating in high switching frequencies.

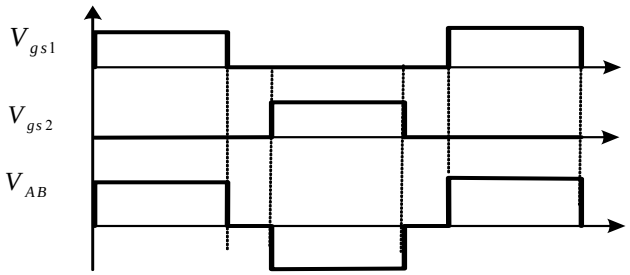


Figure 6-2 (a) Waveforms of conventional symmetric HB dc-dc converter

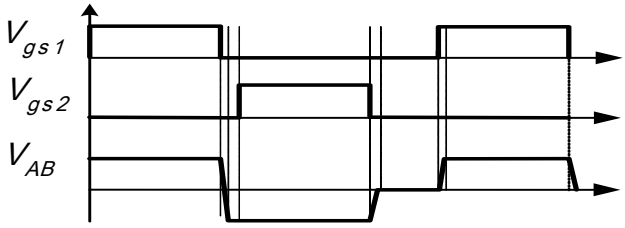


Figure 6-2 (b) Waveforms of DCS HB dc-dc converter

6.2.2 Proposed Unified PWM Control Scheme for HB converter

In the asymmetric half bridge dc-dc converter, the duty cycle of the two main switches are complementary; while in DCS controlled half bridge dc-dc converter, the pulse width of the two drive signals is identical. The advantage and disadvantages of the two control schemes have been discussed above. As matter of fact, further investigation found that the pulse width of the two drive signals could be random providing there is no overlapping between two drive signals (overlapping results in short circuit through the leg). The drive signal waveforms of the proposed unified PWM control scheme is sketched in Figure 6-3, where the drive signals Vgs_1 and Vgs_2 are applied to the switch S_1 and S_2 of the topology shown in Figure 6-1, respectively. The duty cycle of the switch S_1 is defined as D, and the leading edge of the drive signal Vgs_2 follows the falling edge of the drive signal Vgs_1 with a short dead time. The duty cycle of the drive signal Vgs_2 is defined as proportional to that of the drive signal Vgs_1. The duty cycles of the two switches are expressed as follows:

$$D_1 = D \tag{6-1}$$

$$D_2 = \alpha D \qquad (D_2 \le 1 - D) \tag{6-2}$$

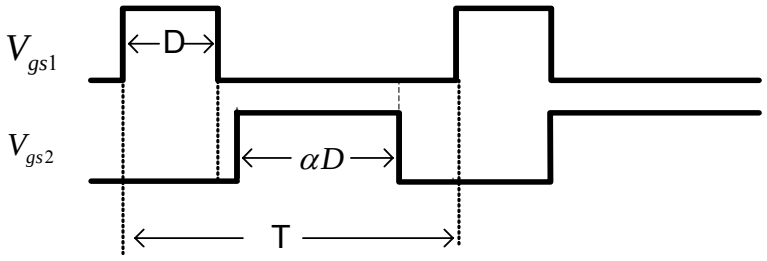


Figure 6-3 Unified PWM control scheme for HB dc-dc converter ($D \le \alpha D \le 1-D$)

The proposed PWM control scheme can be considered as generic scheme since the asymmetric control and DCS control can be derived from this scheme. In the PWM modulation, α is a programmable coefficient. At $\alpha = 1$, the proposed scheme becomes the original DCS control as shown in Figure 6-4. When $\alpha D = 1-D$, the unified control scheme turns into asymmetric control. Although $\alpha D > 1-D$ is not allowed in HB dc-dc converter, in a digital controller, the setup of $\alpha D \ge 1-D$ is allowed providing the controller provides a reset function at the beginning of each cycle, which means that the over-length portion of the pulse V_{gs2} is truncated as shown in Figure 6-5. In this case, the converter automatically slides into asymmetric operation.

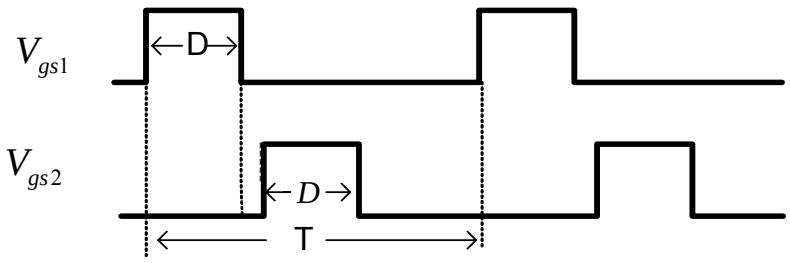


Figure 6-4 Unified PWM control scheme for half-bridge dc-dc converter $(\alpha = 1)$

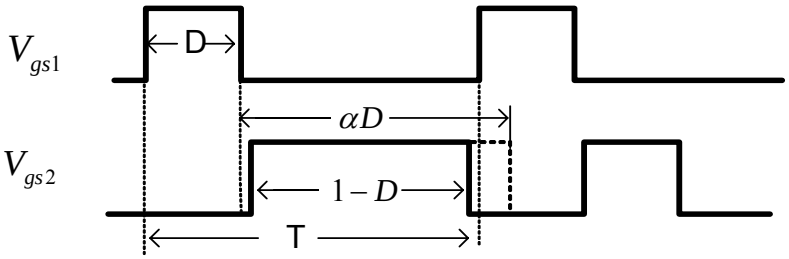


Figure 6-5 Unified PWM control scheme for half-bridge dc-dc converter $(\alpha D \geq 1-D)$

6.2.3 Modes of Operation Analysis

To simplify the analysis of operation, components are considered ideal except as indicated otherwise. The main modes of operation are described as follows, and the corresponding equivalent circuits are shown in Figure 6-6, and the key corresponding waveforms are sketched in Figure 6-7.

Mode 1 $(t < t_1)$: Initially, S_1 is conducting, and the input power is delivered to the output. L_1 is charged, and L_2 freewheels through D_2.

Mode 2 $(t_1 < t < t_2)$: S_1 is turned off at $t = t_1$, causing the primary current i_p to charge C_1 and discharge C_2. During the interval, the reflected secondary inductor current dominates the primary current i_p. Thus, C_2 may be discharged to zero at wide load range, which means wide ZVS range can be achieved for S_2.

Mode 3 $(t_2 < t < t_3)$: When the voltage across C_2 is discharged to zero at $t = t_2$, the body diode of S_2 conducts to carry the current, which provides ZVS condition for switch S_2. During this period, leakage inductance is reset, and secondary current i_1 and i_2 freewheel through D_1 and D_2, respectively.

Mode 4 *(* $t_3 < t < t_4$ *)*: S_2 is turned on with ZVS at $t = t_3$; the primary current decreases to zero and then becomes negative. When the negative peak current is equal to the reflected L_2 current, the diode D_2 is blocked and the converter starts to deliver power to the output. The inductor L_2 is charged, and inductor L_1 current continues to freewheel.

Mode 5 *(* $t_4 < t < t_5$ *)*: S_2 is turned off at $t = t_4$, causing the primary current i_p to charge C_2 and discharge C_1. When the secondary D_1 and D_2 start to freewheel, leakage inductance and junction capacitance of switches S_1 and S_2 start to oscillate on the primary side. During the interval, the body diodes may be involved, which worsen the ringing and results in reverse recovery losses. (The ringing waveforms are not shown in the Figure)

Mode 6 *(* $t_5 < t < t_6$ *)*: The oscillation comes to the end with equal voltage across switches S_1 and S_2. On the secondary side, L_1 and L_2 keep freewheeling. At $t = t_6$, S_1 is turned on again going back to Mode 1.

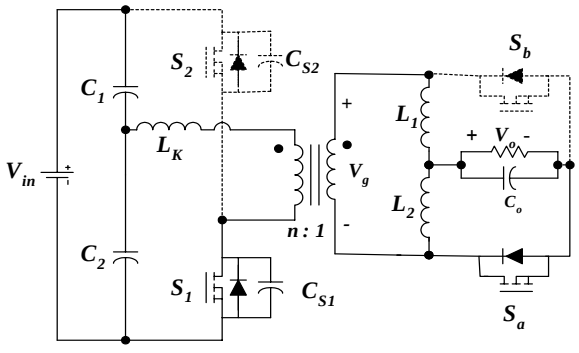


Figure 6-6 (a) Mode 1

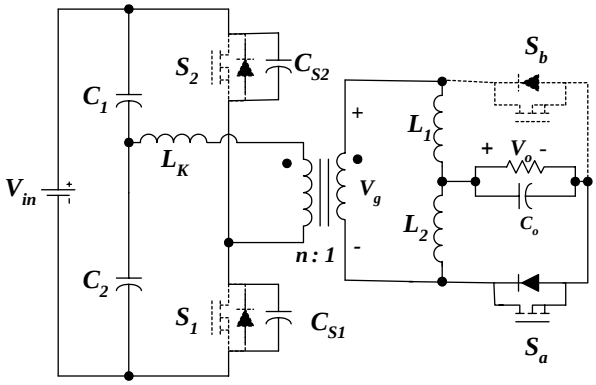


Figure 6-6 (b) Mode 2

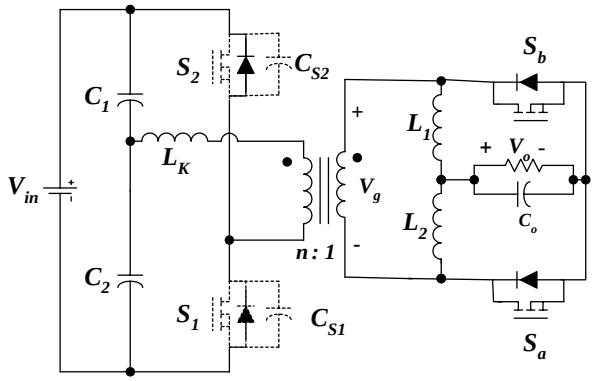


Figure 6-6 (c) Mode 3

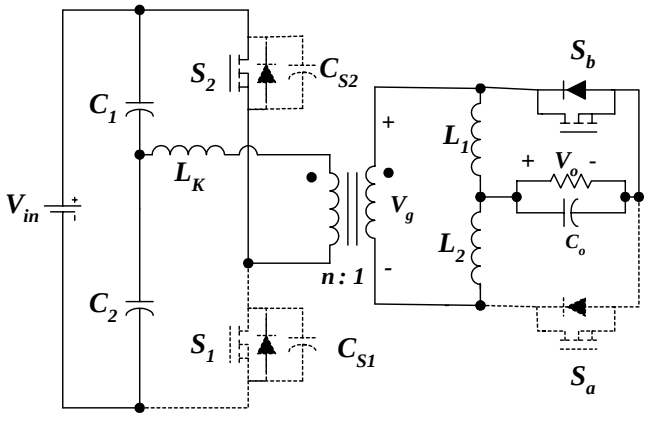


Figure 6-6 (d) Mode 4

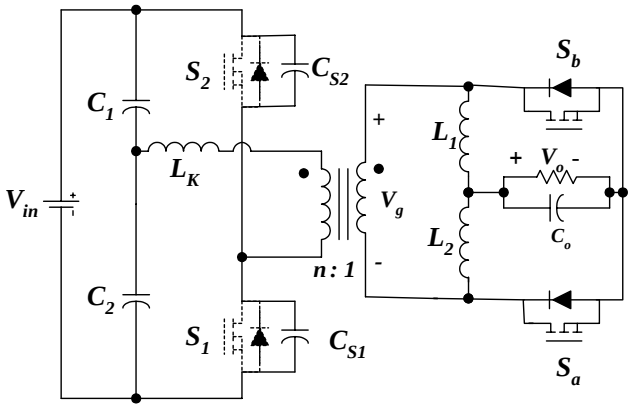


Figure 6-6 (e) Mode 5

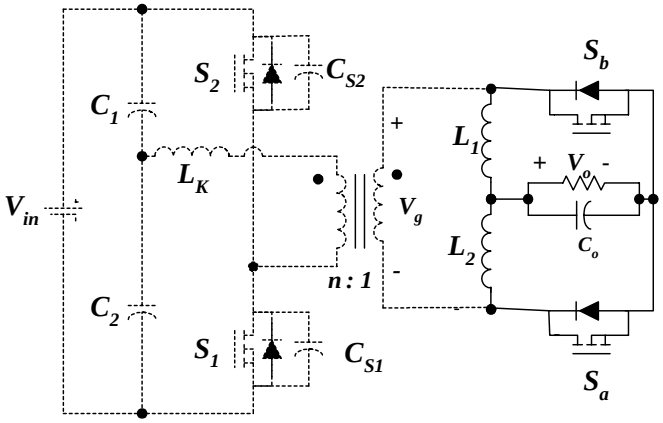


Figure 6-6 (f) Mode 6

Figure 6-6 Key modes of operation

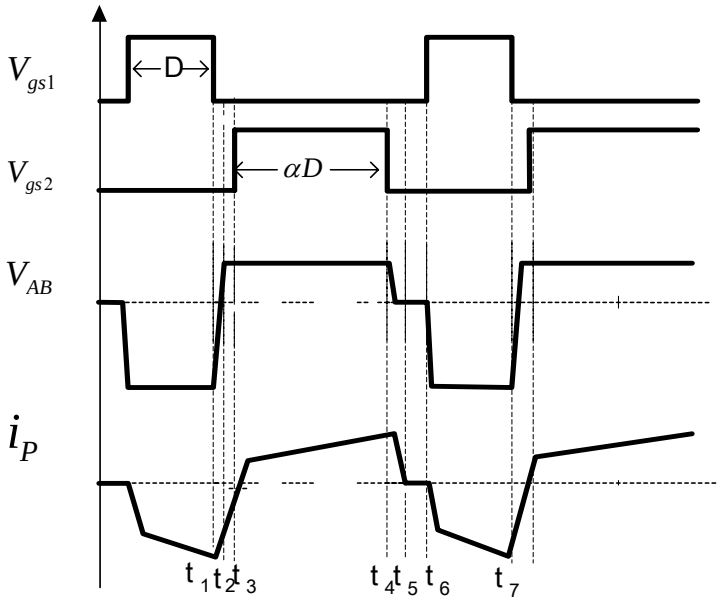


Figure 6-7 Key waveforms of the proposed unified control scheme

6.2.4 Modeling and Analysis of the Proposed PWM Control Scheme

Average modeling method used in [10] can be applied to the analysis. Ignoring the effect of the transformer leakage inductance, the converter has three modes of operation as shown in Figure 6-8(a), (b) and (c).

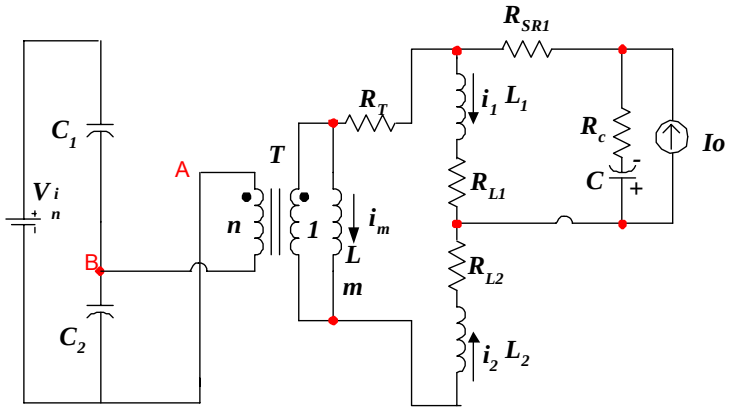


Figure 6-8(a). Switch S_1 is on during D_1T=DT

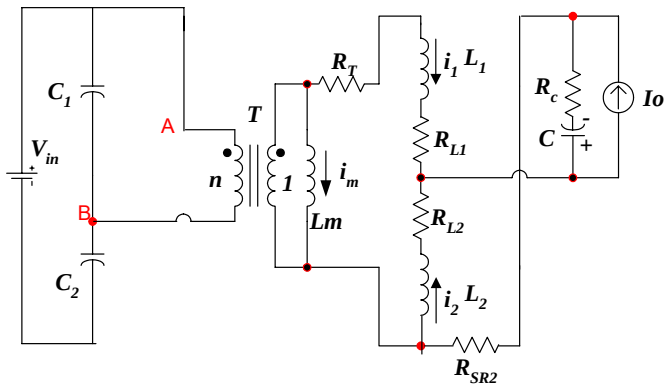


Figure 6-8(b). Switch S_2 is on during $D_2T = \alpha DT$

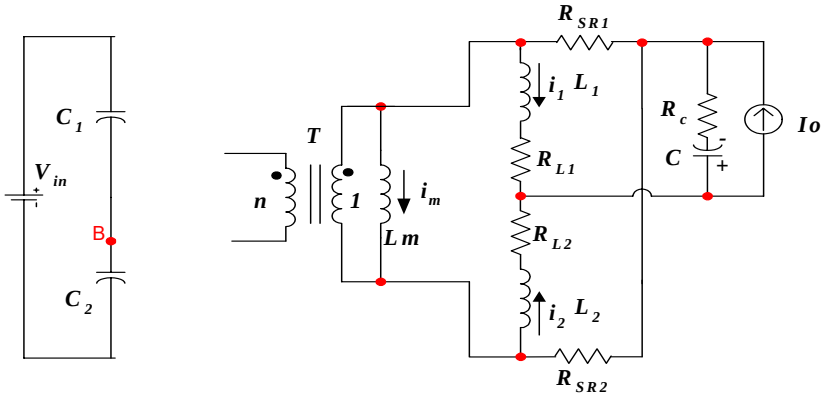


Figure 6-8(c). Both Switch S_1 and S_2 are off

Figure 6-8. Three equivalent circuits

For each mode, the converter can be denoted using a set of linear state-space equations. Corresponding to three modes of operation, three sets of state-space equations are expressed as Equation 6-3, where is the vector of state variables, u is the vector of

independent sources; A_1, B_1, A_2, B_2, A_3 and B_3 are respective system matrices for each of the three switched networks.

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \tag{6-3}$$

The state-space variables are defined as follows:

$$\dot{x} = \left[\frac{dV_{C_1}}{dt} \quad \frac{di_{L_m}}{dt} \quad \frac{di_{L_1}}{dt} \quad \frac{di_{L_2}}{dt} \quad \frac{dV}{dt} \right]^T \tag{6-4}$$

$$x = \left[V_{C_1} \quad i_{L_m} \quad i_{L_1} \quad i_{L_2} \quad V \right]^T ; \; u = \left[V_{in} \quad I_o \right]^T \tag{6-5}$$

A_1, B_1, A_2, B_2, A_3 and B_3 can be derived from modes of operation in Figure 6-8 (a), (b) and (c), respectively. Assuming the duty cycle of the switch S_1 and S_2 are d1 and d2, respectively. The key concept in state-space averaging is the replacement of the above three sets of state-space equations by a single equivalent set [10] A_1

$$\dot{x} = Ax + Bu \tag{6-6}$$

where the equivalent matrices are defined by:

$$A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3 \qquad B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3$$

The steady-state solution, with DC values indicated by capital letters, is obtained by setting $\dot{x} = 0$

$$X = -A^{-1} B U \tag{6-7}$$

Through Equation 6-3 ~ 6-7, the steady-state DC quiescent points can be derived. The voltage across the capacitor C_1 is:

$$V_{C_1} = \frac{1}{1+\alpha} V_{in} \tag{6-8}$$

The voltage across the capacitor C_2 is

$$V_{C_2} = \frac{\alpha}{1+\alpha} V_{in} \tag{6-9}$$

The transformer DC current bias is:

$$I_M = \frac{\frac{\alpha}{1+\alpha} R_{L1} - \frac{1}{1+\alpha} R_{L2}}{R_{Ts} + R_{L1} + R_{L2}} \frac{I_o}{n} \tag{6-10}$$

The average current through inductor L_1 is derived:

$$I_{L1} = \frac{R_{L2} + \frac{\alpha}{1+\alpha} R_{Ts}}{R_{Ts} + R_{L1} + R_{L2}} I_o \tag{6-11}$$

The average current through inductor L_2 is derived:

$$I_{L2} = \frac{R_{L1} + \frac{1}{1+\alpha} R_{Ts}}{R_{Ts} + R_{L1} + R_{L2}} I_o \tag{6-12}$$

where Io is the converter output current.

From Equation (8) through Equation (12), we may conclude:

(1) DC bias is only determined by DC resistance values and control coefficient α, and inductor inductance, transformers magnetizing inductance and filter capacitance have no effect on the DC voltage and current distribution.

(2) It is clear that transformer primary winding DCR, primary-side FETs' on-resistance and secondary-side SRs' on-resistance values have no effect on the DC distribution.

(3) If $\alpha = 1$ is satisfied, symmetric DC distribution can be achieved as: $V_{C_1} = V_{C_2}$; $I_{L_1} = I_{L_2}$ and $I_m = 0$. This is the case of the DCS controlled HB dc-dc converter.

(4) Substituting $\alpha = \frac{1 - D}{D}$ into Equation (8) through (12), the DC bias of asymmetric HB dc-dc converter can be derived.

DC gain of the HB dc-dc converter under the unified PWM control scheme is derived as:

$$\frac{V_{out}}{V_{in}} = \frac{\alpha}{1 + \alpha} \frac{D}{N} \qquad 6\text{-}13$$

Where *N* is transformer turn ratio. Under certain coefficient α, the DC gain is only proportional to the duty cycle, and thus the conventional PWM scheme is applicable to output voltage regulation. When the HB dc-dc converter is controlled under asymmetric scheme, we have $\alpha = \frac{1 - D}{D}$. Substituting this equation into Equation (13), the DC gain of the converter is obtained as:

$$\frac{V_{out}}{V_{in}} = (1 - D) \frac{D}{N} \qquad 6\text{-}14$$

It is clear that the DC gain is a non-linear function of duty cycle D. This non-linearity results in some drawbacks for a converter under this control scheme. For example, for the same range of input voltage deviation, the converter requires wider duty cycle range to regulate output voltage compared to the symmetric control, which makes

the stress distribution even worse at high line input.

6.3 Comparison of Various PWM Control Schemes for HB Converter

As matter of fact, the proposed PWM control scheme is a generic PWM scheme for HB dc-dc converter. By programming the modulation coefficient α , the original DCS and asymmetric control schemes can be derived. Based on the same design and specifications of HB dc-dc converter, comparison between the proposed PWM control, asymmetric control and symmetric control is shown in Table 6-1, where N is the transformer turn ratio, D is the duty cycle of the switch S_1, I_o is the load current, V_{in} is the input voltage, and V_{out} is the output voltage. The filter inductance and output capacitance values are assumed large enough such that the inductor currents and output voltage is regarded as constant current source and voltage source, respectively.

From Table 6-1, it can be observed that DCS HB has the same stress distribution as the symmetric HB, while the proposed PWM controlled HB, asymmetric HB have asymmetric stress distribution, DC bias of the magnetizing current. For the proposed unified PWM control scheme, the voltage and current stress distribution is function of the modulation coefficient α , which determines the degree of stress asymmetry. The transformer DC bias and asymmetric stress distribution exist when $\alpha \neq 1$. However, compared with the original DCS control, the unified PWM control scheme reduces the dead time while the two main switches are off, as result, the transformer leakage ringing duration and loss could be reduced. Particularly, when $(\alpha D \geq 1 - D)$, the HB dc-dc converter turns into complementary operation, and the converter dead time is minimized and transformer ringing is eliminated.

Table 6-1 Comparisons of HB converter under various PWM control schemes

	Unified PWM controlled HB	Symmetric HB	Asymmetric HB	DCS HB
DC gains	$V_{out} = \frac{\alpha}{1+\alpha}\frac{D}{N}V_{in}$	$V_{out}=\frac{DV_{in}}{2N}$	$V_{out}=\frac{D(1-D)V_{in}}{N}$	$V_{out}=\frac{DV_{in}}{2N}$
DC magnetizing current	$I_{DC}=\frac{1}{2}\frac{\alpha-1}{1+\alpha}\frac{I_o}{N}$	$I_{DC}=0$	$I_{DC}=\frac{(1-2D)}{2}I_O$	$I_{DC}=0$
Stresses of switch S_1	$V_{ds1}=V_{in}$	$V_{ds1}=V_{in}$	$V_{ds1}=V_{in}$	$V_{ds1}=V_{in}$
Stresses of switch S_2	$V_{ds2}=V_{in}$	$V_{ds2}=V_{in}$	$V_{ds2}=V_{in}$	$V_{ds2}=V_{in}$
Stresses of rectifier D_1	$V_{D_1} = \frac{1}{1+\alpha}\frac{V_{in}}{N}$	$V_{D1}=\frac{V_{in}}{2N}$	$V_{D1}=\frac{(1-D)V_{in}}{N}$	$V_{D1}=\frac{V_{in}}{2N}$
Stresses of rectifier D_2	$V_{D_2} = \frac{\alpha}{1+\alpha}\frac{V_{in}}{N}$	$V_{D_2}=\frac{V_{in}}{2N}$	$V_{D_2}=\frac{DV_{in}}{N}$	$V_{D_2}=\frac{V_{in}}{2N}$

For a unified PWM control scheme with a certain control coefficient ($\alpha \neq 1$), the converter DC gain is a linear function of duty cycle, and the current and voltage stress is independent of duty cycle. The design is simplified compared with asymmetric control, because in the asymmetric controlled HB converter, the voltage and current stress distribution varies with both the duty cycle and input voltage, which need to be considered in the converter design.

As discussed in sections above, the advantage of the asymmetric half-bridge dc-dc converter is that ZVS can be achieved and the transformer leakage inductance ringing is eliminated. However, the asymmetric voltage and current distribution makes the converter less efficient under broad range of input voltage. Figure 6-9 shows the voltage stress across secondary rectifiers under various control schemes for a certain converter design, where Vin=36V~75V, Vout=1.2V, transformer turn ratio n= 6:1. In the figure, we assume $\alpha = 1$, and the stress traces of V_{D1} and V_{D2} are identical and overlap with those of symmetric control. By increasing the modulation coefficient α, the voltage stress traces of the proposed PWM scheme move towards those of asymmetric HB case. Higher modulation coefficient α, the scheme is closer to the asymmetric HB case, as shown in the figure.

It is also observed that, the maximum voltage stress of V_{D1} occurs at high input voltage. For the proposed PWM scheme and asymmetric control, the high input voltage drives the voltage stress distribution more uneven, which makes the voltage stress even higher compared with the symmetric control scheme. As a result, rectifier component with higher voltage rating needs to select for the diode D_1.

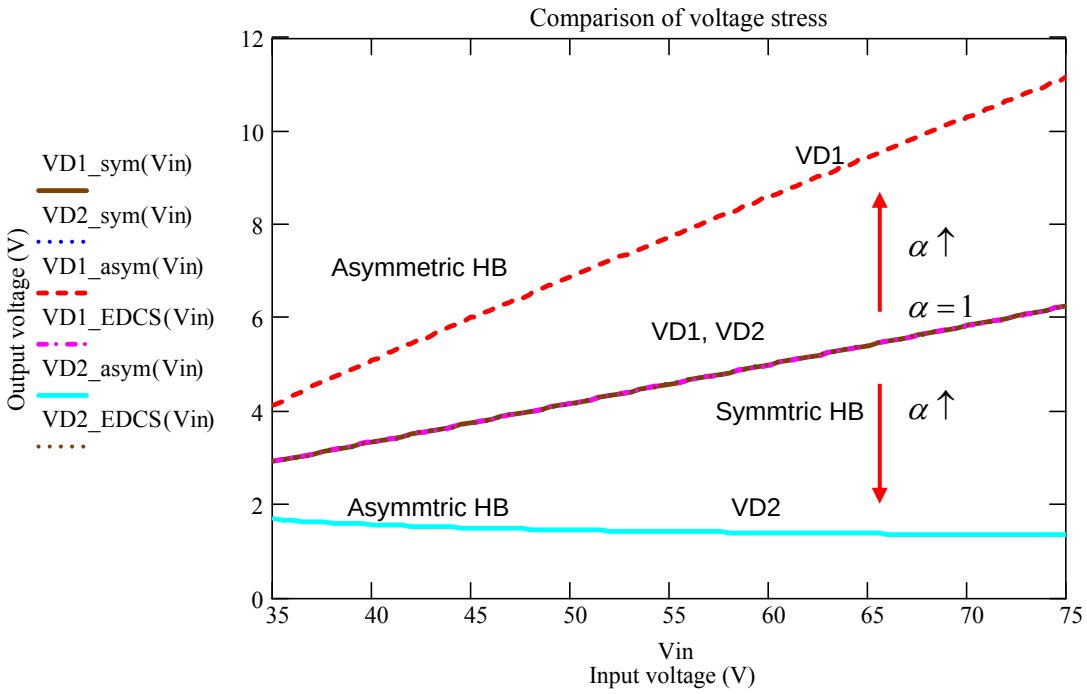


Figure 6-9 Comparison of voltage stress across secondary rectifiers

6.4 Adaptive Unified Digital PWM Control Scheme

6.4.1 Control Scheme Analysis

As we discussed in Section III, the voltage stress across one of the rectifiers are significantly higher than the other at high input voltage. The value of the coefficient α is critical since it controls the asymmetry degrees of stress distribution. At low line input, higher efficient α is favorable because asymmetric operation provides advantages while the rectifier voltage stress is much lower than at high line input. However, at high line, a high efficient α value results in extremely high voltage stress of V_{D1}. If we adaptively adjust the modulation coefficient α according to the input voltage, the voltage stress variation across the secondary rectifiers for the whole range of input voltage can be

controlled within a narrower range. Specifically, at high input voltage, the modulation coefficient α could be minimized ($\alpha = 1$) to eliminate the asymmetry of voltage stress, such that the maximum rectifier voltage stress is minimized. While at low input voltage, modulation coefficient α is increased to allow the converter to operate at asymmetric condition to achieve higher efficiency.

The adaptive modulation coefficient as a function of input voltage is sketched as in Figure 6-10. At low line, the converter operates at point A that corresponds to maximum modulation coefficient α_{max}; while at high line, the converter operates at point B that corresponds to lowest control coefficient. The modulation

$$\alpha(V_{in}) = 1 - \frac{\alpha_{max} - 1}{V_{max} - V_{min}}(V_{in} - V_{max}) \qquad 6\text{-}15$$

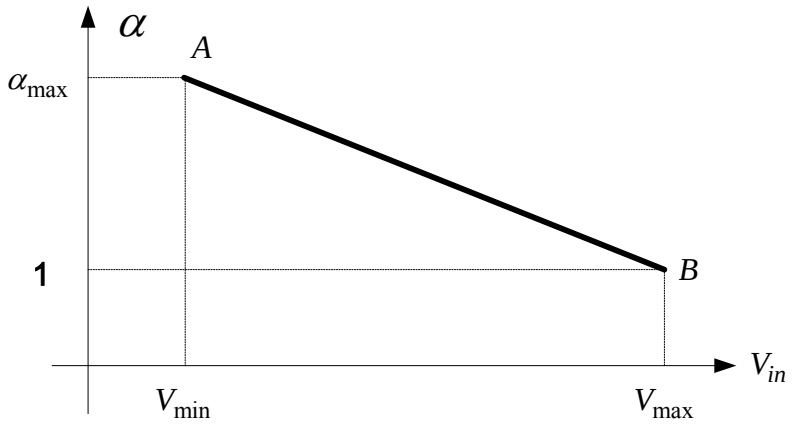


Figure 6-9 Adaptive modulation coefficient v.s. input voltage

Substituting Equation 6-15 into the rectifier voltage stress equations as shown in Table 6-1 obtains the rectifier stresses:

$$V_{D_1}(V_{in}) = \frac{1}{2 - \frac{\alpha_{max} - 1}{V_{max} - V_{min}}(V_{in} - V_{max})} \frac{V_{in}}{N} \quad 6\text{-}16$$

$$V_{D_2}(V_{in}) = \frac{1 - \frac{\alpha_{max} - 1}{V_{max} - V_{min}}(V_{in} - V_{max})}{2 - \frac{\alpha_{max} - 1}{V_{max} - V_{min}}(V_{in} - V_{max})} \frac{V_{in}}{N} \quad 6\text{-}17$$

Considering the same converter design: Vin=36V~75V, Vout=1.2V, transformer turn ration N = 6:1, we have $V_{max} = 75V$, $V_{min} = 36V$, $N = 6$. Assuming the maximum modulation coefficient $\alpha_{max} = 4$, the rectifier stresses expressed as Equation 6-16 and 6-17, are drawn in Figure 6-11 to compare with the asymmetric and symmetric control schemes. In the figure, it is clear that, compared with asymmetric control; the voltage stress difference between two rectifiers is reduced, especially at the range of high input voltage. As a result, the maximum voltage stress of VD1 is significantly reduced. At highest input voltage, the converter operates at the original DCS control and even voltage distribution is achieved.

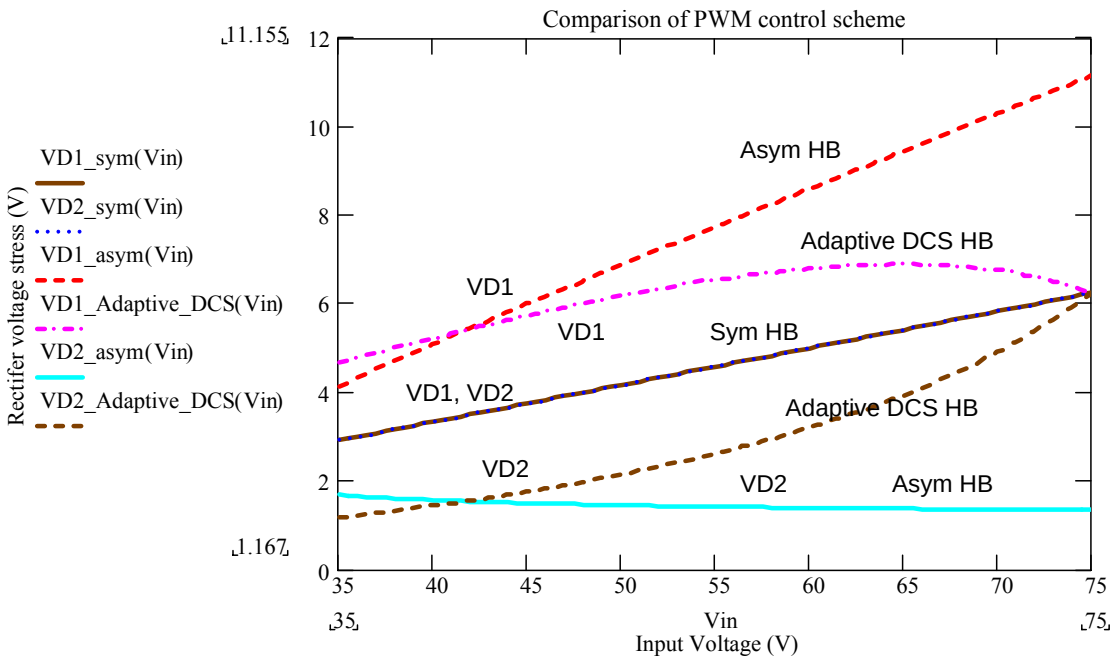


Figure 6-10 Voltage stress comparison of three control schemes

6.4.2 Digital Implementation of the Adaptive PWM Control Scheme

Figure 6-11 shows the block diagram of digital controller Si8250, where the ADC converts output voltage error signal from analog to digital and feeds to digital PID compensator, and the PID compensator forms $u(n)$ fed to the digital PWM (DPWM) block to generate desirable pulse width of drive signals. At the case of $(\alpha D < 1 - D)$, the dive signals for the switch S_1 and S_2 are programmed as shown in Figure 6-13(a). Switching cycle starts at $t = t_1$, the initial states of the two digital signals are set up as "0" in a special function register (SFR). After an absolute time delay, the rising edge of the drive signal V_{s1} is trigged and set as "1". The pulse width of the drive signal depends on *u(n),* which is determined by the output voltage error. After an interval donated by *u(n)*,

the signal V_{s1} falls to "0". At the meanwhile, the trailing edge of the signal V_{s1} triggers the rising edge of the signal V_{s2}. A dead time between the two edges could be programmed to avoid a short circuit across the bridge. The pulse width of the signal V_{s2} is determined by $\alpha\, u\,(n)$, which could be programmed through the SFR.

When the pulse width of $\alpha\, u\,(n)$ is greater than (1-D)T, i.e. $(\alpha D \geq 1-D)$, the digital waveforms are shown in Figure 6-12(b). At $t = t_3$, the drive signal of V_{gs2} is reset to zero. In other words, the drive signal is truncated when this case occurs, and thus the converter turns into operating at asymmetric (complementary) control. In the proposed adaptive digital control scheme, this happens at the band of low input voltage since the modulation coefficient value is increased with the increased input voltage. The reset function provided by the digital controller Si820 perfectly meets the timing needs of the proposed adaptive unified PWM control scheme.

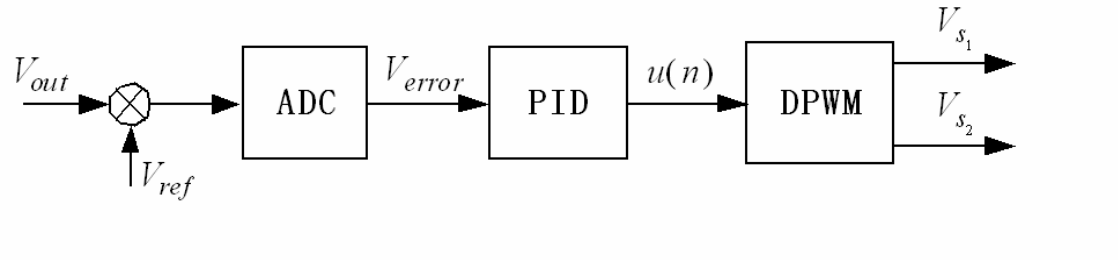
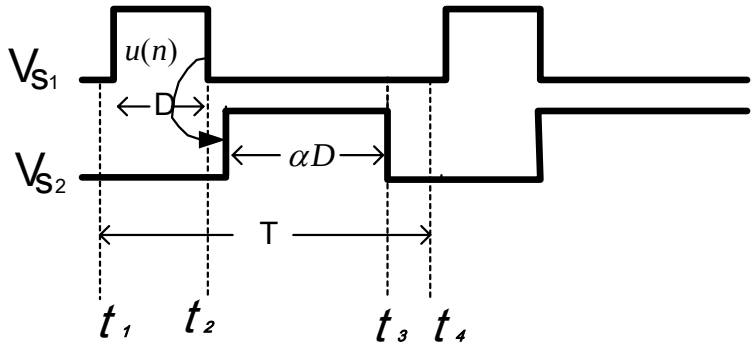
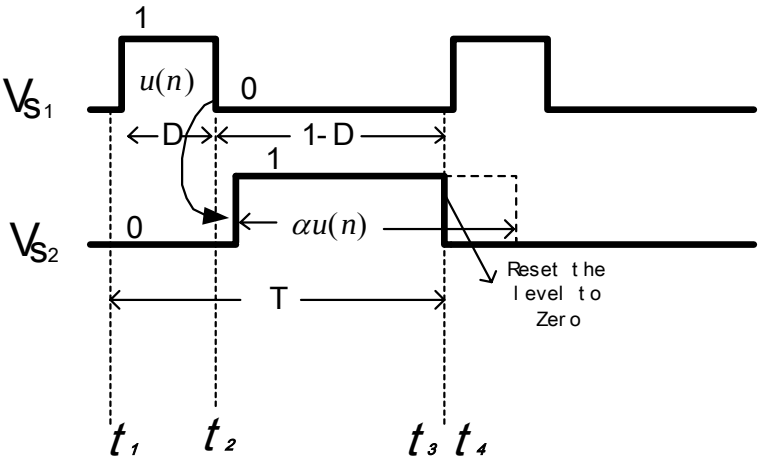


Figure 6-11 Digital PWM implementation based on digital controller Si8250



(a) At the case of $(\alpha D < 1 - D)$



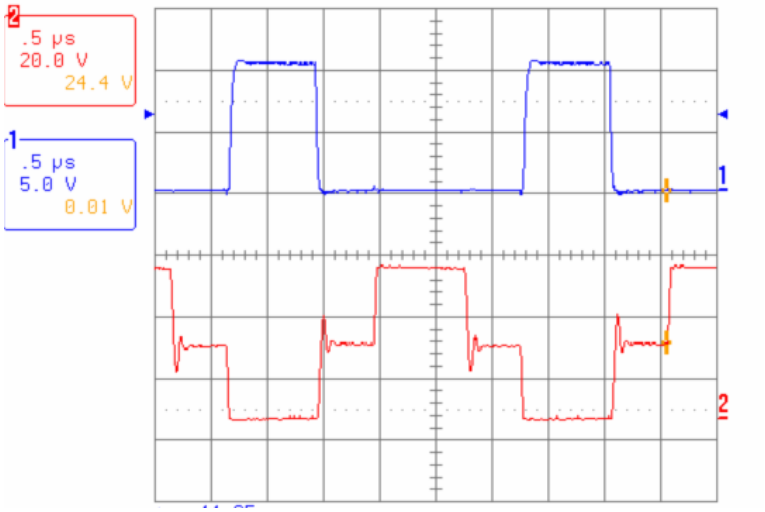
(b) At the case of $(\alpha D \geq 1 - D)$

Figure 6-12 Digital PWM implementation based on digital controller Si8250

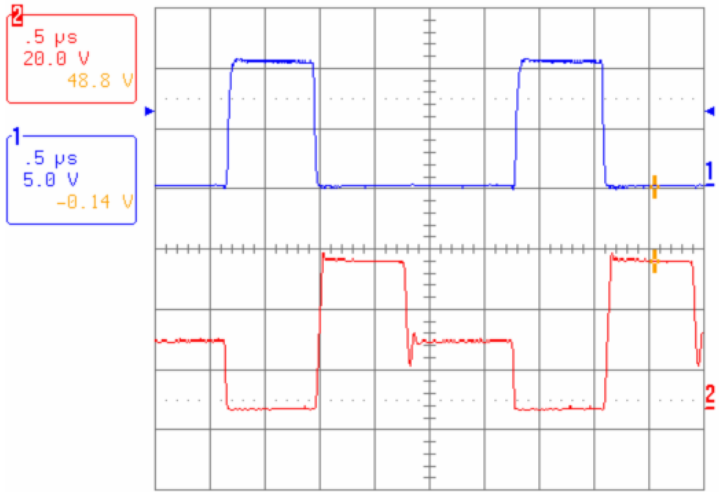
6.5 Experimental Results

The proposed control scheme is verified on a digitally controlled demo board, the specifications are: Vin=36V~75V, Vout=1.2V, Iout=35A, and switching frequency of

400kHz. The demo board was originally designed with symmetric HB dc-dc converter under control of Si8250. Taking advantage of flexibility featured by digital control, the demo board can be used for experimental verification and comparison by just changing algorithm codes in the digital controller. Air gap is added in the transformer to avoid saturation under asymmetric operation. For comparison purpose, symmetric PWM, original DCS PWM and adaptive unified PWM schemes are implemented on the same demo board, respectively. Figure 6-13(a) and (b) show the waveforms of the switch S_1 under the control of symmetric PWM and DCS PWM schemes, respectively. It is observed that the DCS PWM eliminates half of the ringing and provides ZVS conditions for the switch S_2 compared with symmetric PWM scheme.



(a) Symmetric control scheme



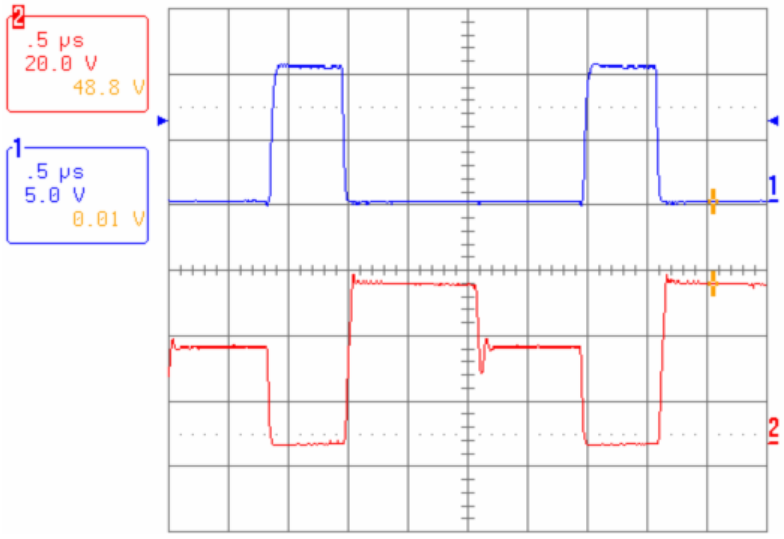
(b) Original DCS control

Figure 6-13 Switch waveforms of the low side switch S_1 under the symmetric control and the original DCS control

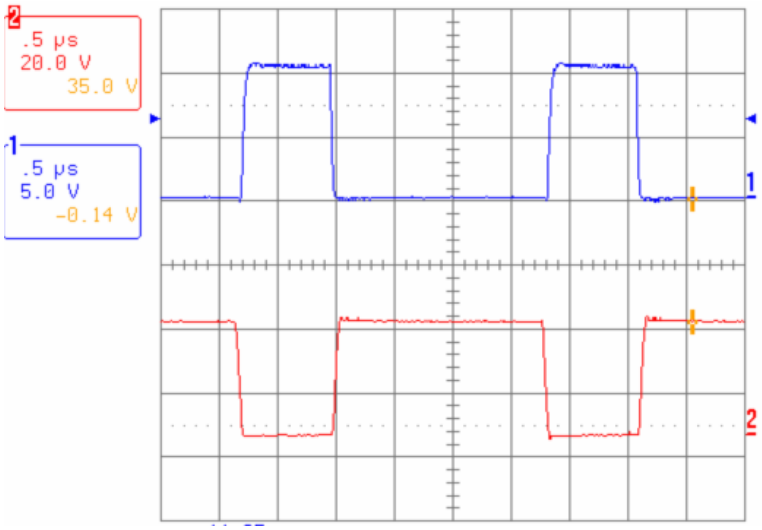
(Top trace: drive signal of Vgs_1; bottom trace: drain-to-source voltage Vds_1)

Applying the proposed adaptive digital PWM scheme to the converter, the waveforms of the switch S_1 at the nominal input voltage 48V is shown in Figure 6-14(a), where asymmetric pulse width for the switch S_1 and S_2 can be clearly observed from the drain-to-source voltage waveform. When the input voltage decreases to 36V, the PWM coefficient α is maximized, and the converter turns into operating at asymmetric PWM condition as analyzed in previous sections. The experimental waveforms are shown in Figure 6-14(b), from which it is clear that the converter operates at asymmetric condition, and the primary transformer ringing is completely eliminated. At this case, with the help of leakage inductance, both switches could achieve ZVS. When the input voltage is increased to 75V, the PWM coefficient α is adaptively minimized to 1, and the converter operates as the original DCS PWM scheme.

The measured efficiency curves are sketched in Figure 6-15. The original DCS PWM scheme improves converter efficiency compared with the symmetric PWM scheme. Compared with the original DCS control, the proposed adaptive PWM scheme improves conversion efficiency at low line input as expected, since ZVS could be achieved and primary leakage-inductance ringing is completely removed.



(a) Vin=48V



(b) Vin=36V

Figure 6-14Waveforms of the low side switch S_1 under the proposed adaptive digital PWM scheme

(Top trace: drive signal of Vgs_1; bottom trace: drain-to-source voltage Vds_1)

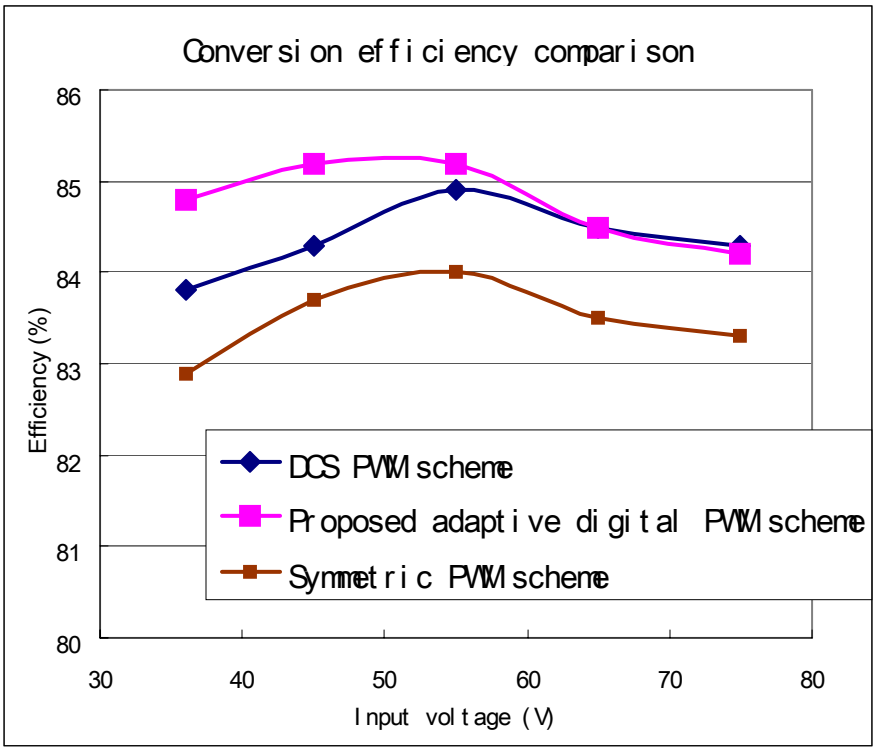


Figure 6-15 Efficiency comparison between the conventional symmetric and DCS PWM schemes and the proposed adaptive digital PWM scheme

6.6 Summary

Based on the original DCS PWM scheme, a unified adaptive digital PWM scheme is proposed for HB dc-dc converters to achieve ZVS for one of the two switches at high line input, and achieve ZVS for both the switches at low line input. In fact, the unified digital PWM scheme extends the original DCS PWM concept to combine the advantages of asymmetric PWM and DCS PWM schemes. Experimental results show that the proposed adaptive digital PWM scheme improves conversion efficiency at low line compared with the original DCS PWM scheme.

7 CONCLUSION

The dissertation explores digital controlled power supply systems with objective of the achieving improvements in converter control schemes, system performance and cost-effectiveness over conventional analog control approaches. Major conclusions achieved are summarized as follows:

Digital controllers, compared with analog controllers, are in a favorable position to provide basic feedback control as well as power management functions with lower cost and great flexibility. Since most power supply products are accomplished in analog and most power design engineers' experience stick with analog world, the key design issues and challenges of digital controlled power deign have to be explored.

Digital redesign is wide-used method of digital controller design, which emphasizes the controller design based on the analog modeling of power converters. With this method, a controller designed in S domain is mapped to digital Z domain. And the limitation and quantization of digital coefficients are some critical issues needed to address. Meanwhile, the limited resolution of ADC and DPWM, calculation error of digital coefficients will significantly impacts the performance of a digital controlled power system.

With a particular design, a digital controlled POL demo prototype, the digital design process has been worked through and some important issues of digital design are addressed. Dynamic or nonlinear control approach corresponding to the system variable situation is also a benefit from digital control. A nonlinear control algorithm trigged by large-signal output voltage transients is accomplished on the POL prototype. The

experimental result shows that digital controller is favorable in implementing advanced control techniques.

In isolated dc-dc converters applications, digital control not only exhibits the capability of dynamic control for system loop, also the flexibility in piecewise control and the switch of PWM modes. A new half-bridge flyback-forward converter topology had been investigated, which has a forward half-wave rectification as the secondary rectifier associated with asymmetric half-bridge converter. This half-bridge converter is favorable since the transformer secondary winding structures is simplified and better transformer window utilization is achieved. However this topology has some intrinsic nonlinear characteristics on system gain variation, therefore, a nonlinear adaptive control has been proposed and implemented to achieve a unified loop gain and system bandwidth under load and input voltage variations based on a digital PI compensation.

DCS (Duty Cycle Shift) PWM control concept is a new concept to reduce the parasitical ringing and maintain the stress balance of components for the applications of half-bridge converters. This concept has been extended to a unified PWM control scheme, which is between asymmetric control and the original DCS control. Corresponding mathematical model was established to analyze a half bridge DC-DC converter under control of the proposed unified PWM scheme. With the digital controller Si8250, by changing the coefficient of the control scheme, the control mode can adaptively slide from one mode to another. The digital control offers this advanced control great flexibility. Experimental results show the performance improvement under control of extended DCS PWM scheme.

Future work of the research on digital controlled dc-dc converter may focus on following aspects.

- Exploring digital applications on high transient response requirement power converters. For example, the multiphase VRM applications require very high power density and high system response speed. Digital controller will provide numbers of excellent features to align with those needs.
- Power management or centralization of power suppliers in some applications
- System dynamic compensation and control according to the variation of environments and parasitical parameters.

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