HIGH SLEW RATE HIGH-EFFICIENCY DC-DC CONVERTER

by

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ABSTRACT

Active transient voltage compensator (ATVC) has been proposed to improve VR transient response at high slew rate load, which engages in transient periods operating in MHZ to inject high slew rate current in step up load and recovers energy in step down load. Main VR operates in low switching frequency mainly providing DC current. Parallel ATVC has largely reduced conduction and switching losses. Parallel ATVC also reduces the number of VR bulk capacitors. Combined linear and adaptive nonlinear control has been proposed to reduce delay times in the actual controller, which injects one nonlinear signal in transient periods and simplifies the linear controller design.

Switching mode current compensator with nonlinear control in secondary side is proposed to eliminate the effect of opotocoupler, which reduces response times and simplifies the linear controller design in isolated DC-DC converters.

A novel control method has been carried out in two-stage isolated DC-DC converter to simplify the control scheme and improve the transient response, allowing for high duty cycle operation and large step-down voltage ratio with high efficiency.

A balancing winding network composed of small power rating components is used to mitigate the double pole-zero effect in complementary-controlled isolated DC-DC converter, which simplifies the linear control design and improves the transient response without delay time.

A parallel post regulator (PPR) is proposed for wide range input isolated DC-DC converter with secondary side control, which provides small part of output power and most of them are handled by unregulated rectifier with high efficiency. PPR is easy to achieve ZVS in primary side both in wide range input and full load range due to 0.5 duty cycle. PPR has reduced

conduction loss and reduced voltage rating in the secondary side due to high turn ratio transformer, resulting in up to 8 percent efficiency improvement in the prototype compared to conventional methods.

To my parents

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CHAPTER ONE: INTRODUCTION

1.1 Background

An unprecedented advancement in semiconductor technology, especially in microprocessors, sets the new level of requirements for power supplies [2-5]. From Intel's initial 4004 to today's Pentium IV, microprocessors have greatly improved their clock frequency by three orders of magnitude through the continuing scaling of Complementary Metal-Oxide-Silicon (CMOS) manufacturing technology from 1.1um in 1986 to 0.09um in 2004. Microprocessor scaling has consistently adhered to Moore's law [8]. By 2006, multi-core CPU processors with more than 279 million transistors on a chip consume more than 100 W. The new scaling technology will drop the core-voltage of high-performance processors down to 1V range, requiring up to 120A current from the voltage regulator.

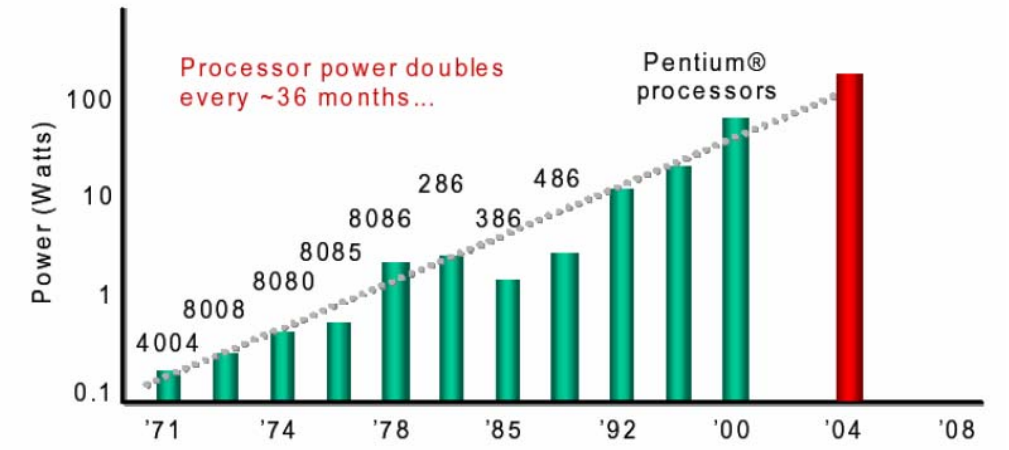


Fig.1.1.1 Historical data on the increased power of Intel CPUs

The electrical power consumed by the CPU is given as

$$P_{CPU} = AV \cdot f \cdot C \cdot V_{CC}^2 \quad (1\text{-}1\text{-}1)$$

Where, AV is the activity factor, f is the clock frequency, C is the lumped capacitance of all the logic gates, and V_{CC} is the CPU core voltage. The scaling of CPU increases the capacitance C, resulting in increased processor power. Fig.1.1.1 shows the historical data on the increase in power for Intel CPUs [1, 6]. It is observed that as the clock speed scales up over time, so does the power dissipation of microprocessors.

The CPU consumes electrical power and eventually turns it into heat. This poses great challenges to CPU thermal management with increasing power consumption [9-10]. The latest mobile processors have implemented special power-saving techniques called PowerNow™ and LongRun™ [11, 12] to try to save power for battery life extension. Accordancing to these technologies, the microprocessor has different modes of operation, i.e., “performance”, “battery” and “automatic”. The idea is to decrease the clock frequency and core voltage in the battery mode, while keeping frequency and voltage higher at performance mode. In the automatic mode, the processor continuously adjusts the clock frequency and voltage according to system demand. That means the microprocessor voltage regulator must be able to change quickly the output voltage on the basis of the control signals from the system or microprocessor.

Another power saving technique, called “Intel Mobile Voltage Positioning” or IMVP, uses the droop-compensation approach usually associated with an extension of the transient window. It also requires the negative core voltage offset for some sleep-mode stages of the microprocessor [3-5]. This approach also extends the battery life, because power dissipation of the microprocessor is inversely proportional to core voltage square.

Fig.1.1.2 shows the roadmap of voltage and current of Intel 32-bit CPUs [6]. Future CPUs will run at sub 1V with an even-tighter voltage tolerance as shown Fig.1.1.2 (a). Meanwhile, Fig.1.1.2 (b) indicates a high current consumption reaching over 120A and fast slew rate of about 400A/μs.

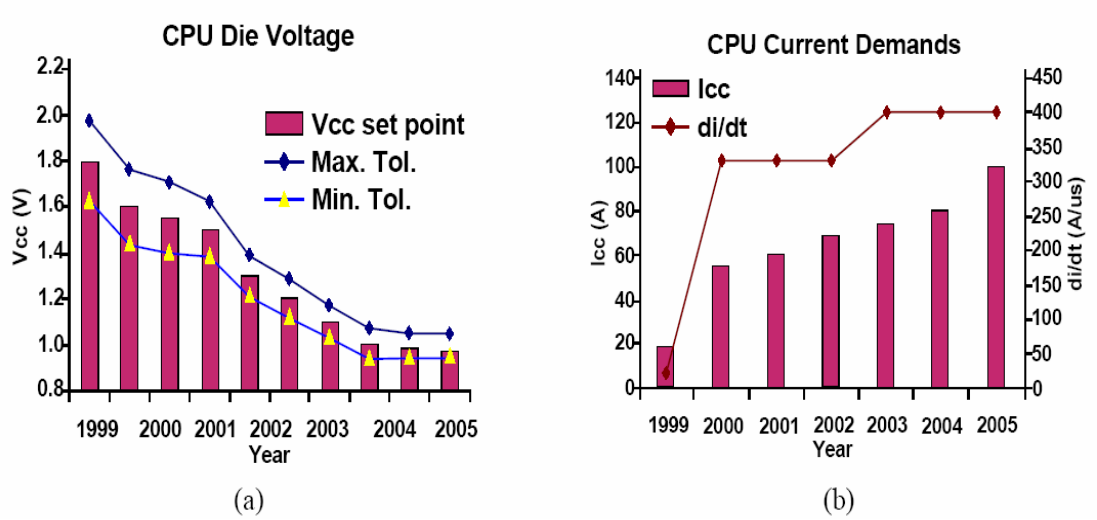


Fig.1.1.2 Intel roadmap of 32-bit CPU (a) CPU die voltage and (b) CPU current demand and current slew rate of VR

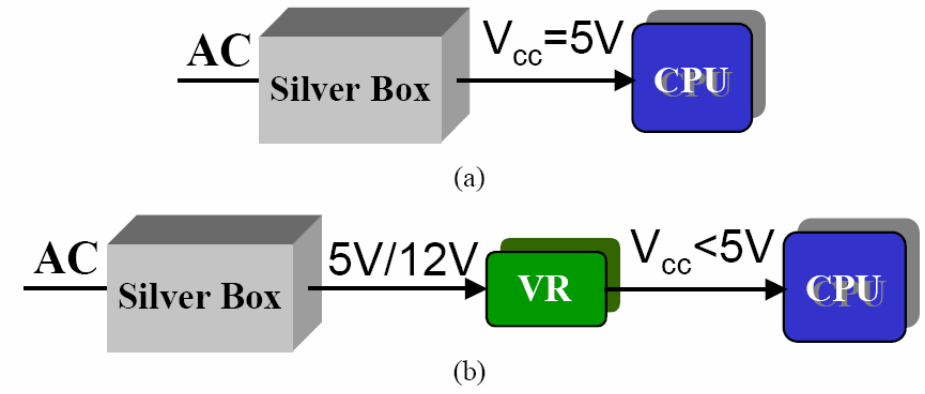


Fig.1.1.3 Power delivery structure: (a) initial CPUs power delivery structure and (b) the current CPU power delivery structure

Fig.1.1.3 (a) shows the initial power delivery architecture for CPUs. The CPU draws power from the 5V output of the silver box directly. However, the parasitic resistance and inductance between silver box and the processor have such a severe impact on the power quality that it is impossible to use the centralized silver box to provide power directly to the high performance CPUs. A dedicated DC-DC converter, the voltage regulator (VR), is placed very close to the processor in order to minimize the parasitic parameters between them. A voltage regulator converts the silver box output voltage to a suitable regulated DC voltage rail to power the CPUs in current power delivery architecture as shown Fig.1.1.3 (b).

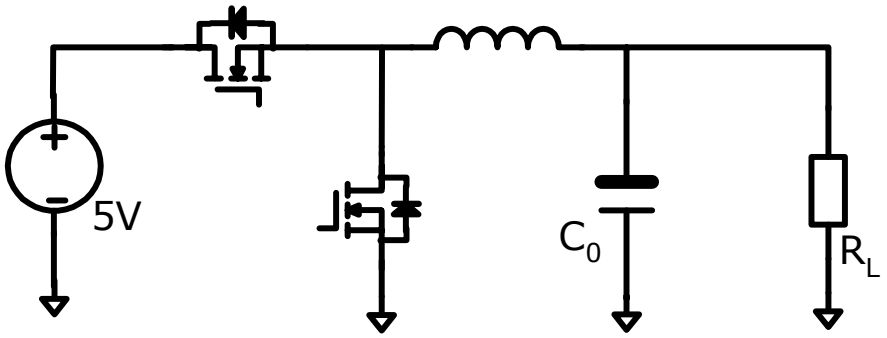


Fig.1.1.4 5V input single phase buck converter

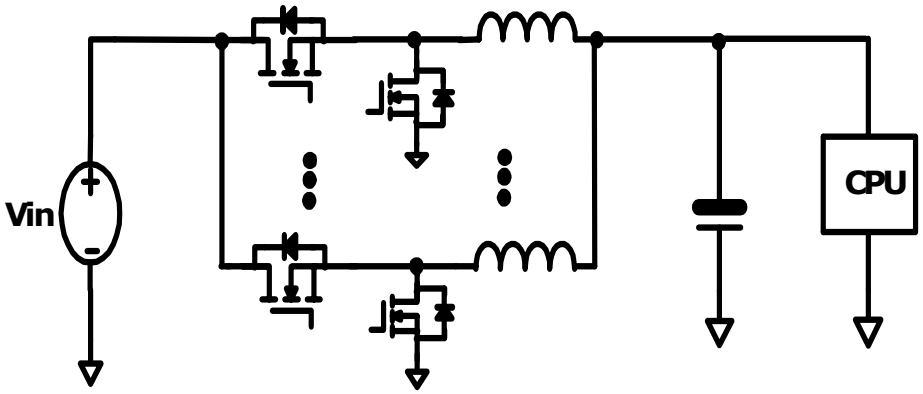


Fig.1.1.5 Multiphase synchronous buck converter

At first, the VR draws power from the 5V output of the silver box by the single-phase buck converter around 2V/20A as shown in Fig.1.1.4. As CPU power increases, a single-phase buck converter cannot meet the requirements because of large current ripples in the filter inductors that increase the conduction and switching losses of FETs, as well as the power losses in the filter inductors.

Therefore, interleaved multiphase synchronous buck converter [23-30], shown in Fig.1.1.5, is presented to improve the efficiency and the transient response, which consists of N identical converters with phase shift of 360/N degree to reduce the output current ripples. Interleaved multiphase operation is important for producing the high currents and low voltages demanded by today's CPUs because it reduces output current ripple and provides better thermal management due to the distributed structure.

For interleaved multiphase buck converter, the output current ripples can be obtained by,

$$\Delta I_L = \frac{V_O}{L_O f_S} \frac{N(D - \frac{m}{N})(\frac{m+1}{N} - D)}{D} \tag{1-1-2}$$

Where, N, Lo and fs are the channel number, the output inductance per channel and the switching frequency, respectively. $m = floor(N \cdot D)$ is the maximum integer that does not exceed the $N \cdot D$. Fig.1.1.6 shows the influence of duty cycle on the output current ripple, which is normalized against the inductor current ripple at zero duty cycle [23].

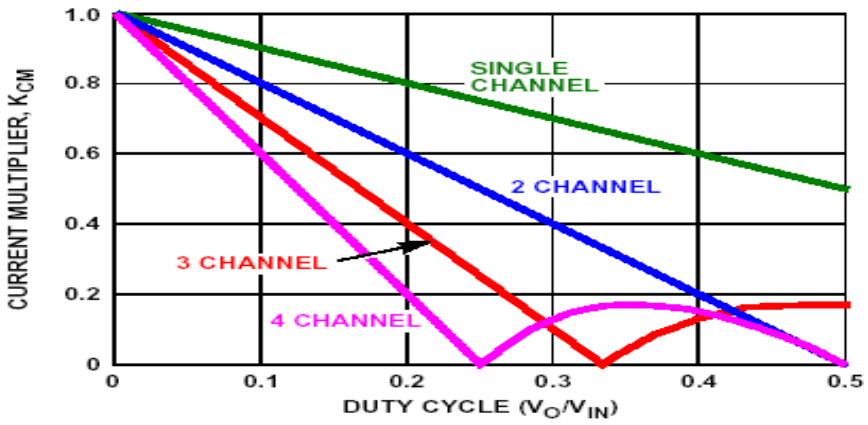


Fig.1.1.6 Influence of duty cycle on the output ripple cancellation

As the power delivered through the VR increases dramatically, the power of the 5V output of the silver box is so high that the distribution loss on the 5V bus is considerable. Hooking the VR to the 5V bus is no longer efficient from the system point of view; therefore, VR input voltage moves to the 12V output of the silver box. In the meantime, more phases are used because higher current is delivered through the VR. Currently, the Intel motherboard adopts a 3~4 phase 12V input interleaved synchronous buck converter, its output voltage is 0.8375~1.6V and the output current is up to 120A in VR10.1 [4].

1.2 Challenge in High Slew Rate VR

Developing an efficient, low cost power delivery system for CPU load is one of the major problems that need to be solved. Another problem relates to the high slew-rate current transients, exceeding 1A/ns through the die when a processor abruptly changes its operating state. Obviously, special packaging, high-frequency decoupling capacitor and fast transient response regulator must be used to keep the core voltage tolerance within the requirement.

The VR current slew rate cannot catch up with that in load current, and the unbalanced current between VR and high slew rate load is provided by the output capacitors until VR supplies full load current. The performance of output bulk and decoupling capacitors play a very important role in output voltage spikes [33, 34, 52]. At the same time, the delay time in the actual controller loop has substantial impact on the voltage spikes [22] [53-63] [67, 68].

1.2.1 Voltage Spikes Estimation in High Slew Rate Load

During high slew rate transient periods, not only ESR and ESL of the output filter and decoupling capacitors have strong impact on the transient response, but also the parasitic inductances and resistances of PCB traces and socket between the VR output terminal and CPU load. In order to simplify the transient voltage spike estimation, only ESR and ESL of capacitors are taken in consideration at first. Fig.1.2.1 shows the equivalent circuit, in which output capacitors are composed of N identical capacitance C with ESR, ESL and VR assumed to be a current source with current ripple and where slew rate is determined by the applied voltage and filter inductance. The worst case for output voltage spikes occurs in step-down load because the buck converter provides higher slew rate current in step-up load than that in step-down load. Therefore, voltage spikes estimation in step-down load has been discussed as an example in this chapter. The influence of parasitic resistance and inductance of PCB traces and socket can be obtained by the same method used in voltage spikes estimation in step-down load.

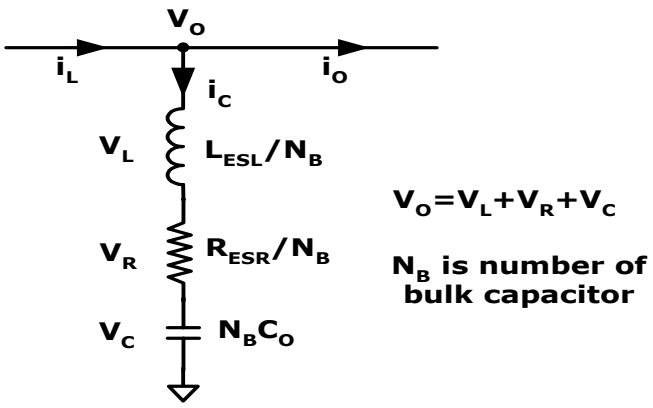


Fig.1.2.1 Simplified circuit for output voltage spikes estimation

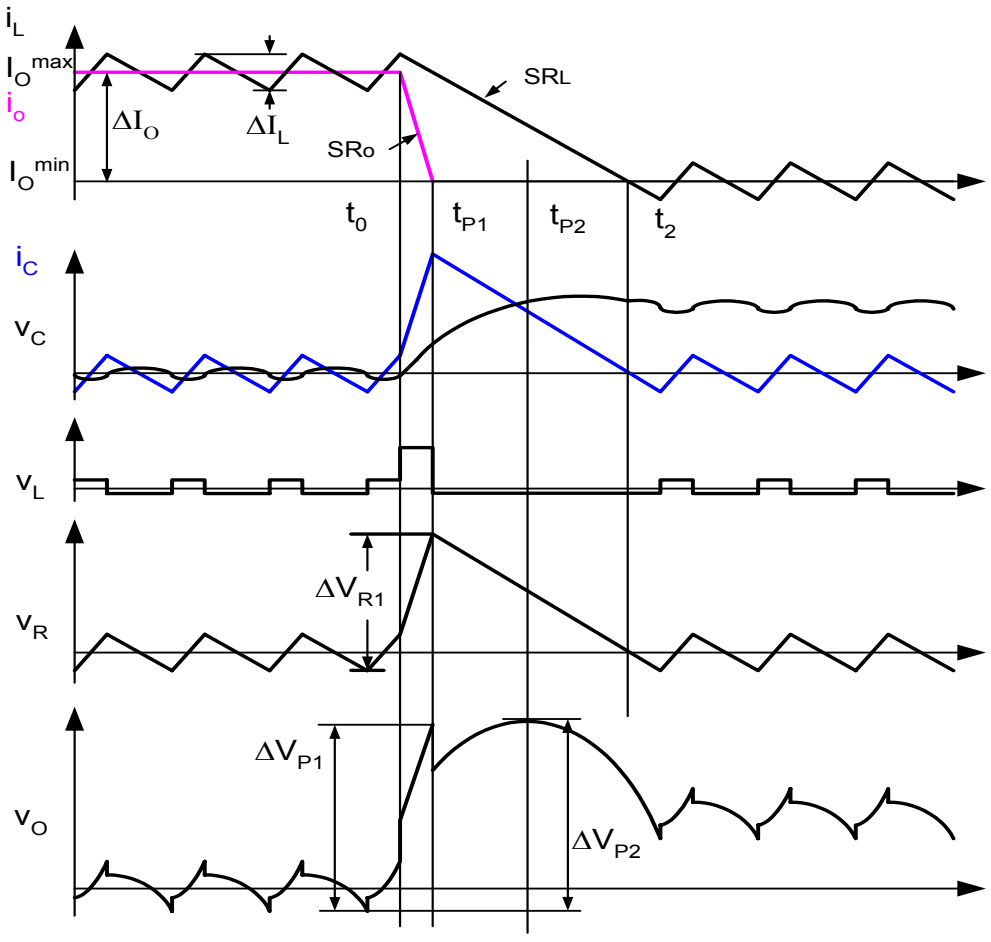


Fig.1.2.2 Output voltage spikes in step-down load with ideal controller

Fig.1.2.2 shows the output voltage transient waveforms in step-down load with ideal controllers that can respond to the transients without any delay time. Two voltage spikes occur, ΔV_{P1} and ΔV_{P2}, during the transient periods. I_L is the VR filter inductor current which slew rate is SR_L. I_O is the load current with SR_0 slew rate.

For the first voltage spike ΔV_{P1} between t_0 and t_{P1},

$$t_{P1}-t_0 = \frac{\Delta I_O}{SR_O} \tag{1-1-3}$$

$$\Delta V_{L1} = \frac{L_{ESL}}{N_B} \cdot SR_O \tag{1-1-4}$$

$$\Delta V_{R1} = \frac{R_{ESR}}{N_B} \cdot (\Delta I_O - \Delta I_O \cdot \frac{SR_L}{SR_O} + \Delta I_L) \tag{1-1-5}$$

$$\Delta V_{C1} = \frac{\Delta I_O}{2 \cdot N_B \cdot C_O \cdot SR_O} \cdot (\Delta I_O - \Delta I_O \cdot \frac{SR_L}{SR_O} + \Delta I_L) \tag{1-1-6}$$

$$\Delta V_{P1} = \frac{1}{N_B} \cdot [(R_{ESR} + \frac{\Delta I_O}{2 \cdot C_O \cdot SR_O}) \cdot (\Delta I_O - \Delta I_O \cdot \frac{SR_L}{SR_O} + \Delta I_L) + L_{ESL} \cdot SR_O] \tag{1-1-7}$$

For the second voltage spike ΔV_{P2} between t_{P1} and t_2

$$\Delta V_{L2} = 0 \tag{1-1-8}$$

$$\Delta V_{P2} = \Delta V_{R2} + \Delta V_{C2} = \frac{R_{ESR}}{N_B} \cdot i_C + \frac{1}{N_B \cdot C_O} \cdot \int_{t1}^{t} i_C \cdot dt + \Delta V_{C1} \tag{1-1-9}$$

$$i_C = \Delta I_O + \frac{\Delta I_L}{2} - SR_L \cdot t \tag{1-1-10}$$

$$\left.\frac{d\Delta V_{P2}}{dt}\right|_{t=t_{P2}} = -\frac{R_{ESR}}{N_B} \cdot SR_L + \frac{1}{N_B \cdot C_O} \cdot (\Delta I_O + \frac{\Delta I_L}{2} - SR_L \cdot t_{P2}) \tag{1-1-11}$$

From the Equation (1-1-11), it is easy to obtain the time t_{P2}-t_0 when the second voltage spike occurs.

$$t_{P2} - t_0 = \frac{\Delta I_O + \Delta I_L / 2}{SR_L} - R_{ESR} \cdot C_O \tag{1-1-12}$$

When the time (t_{P1}-t_0) is less than the time (t_{P1}-t_0), the second voltage spike will dominate; otherwise the first voltage spike dominates. Their Equations are given as

$$\Delta V_{P2}^{1} = \frac{1}{N_B} \cdot [\frac{\Delta I_O}{2 \cdot C_O \cdot SR_L} \cdot (\Delta I_L + \Delta I_O + \frac{\Delta I_L^2}{4\Delta I_O}) - \frac{\Delta I_O^2}{2 \cdot C_O \cdot SR_O}] > \Delta V_{P1} \tag{1-1-13}$$

$$\Delta V_{P2}^{2} = \frac{1}{N_B} \cdot (R_{ESR} + \frac{\Delta I_O}{2 \cdot C_O \cdot SR_O}) \cdot (\Delta I_O - \Delta I_O \cdot \frac{SR_L}{SR_O} + \Delta I_L) < \Delta V_{P1} \tag{1-1-14}$$

From the above analysis, it is clear that the first voltage spike is mainly determined by ESR, ESL, output current slew rate SR_0 and step current ΔI_0; the output filter capacitors have slight capacitive increase because of its short duration. The second voltage spike is mainly determined by the energy stored in filter inductors, bulk capacitance, ESR and step current. ESL has a slight inductive effect on the second voltage spike due to slow slew rate VR current. The delay time in the controller will increase the second voltage spike.

Fig.1.2.3 shows the transient voltage estimation vs. filter inductance. It is clear that the first voltage spike will dominate when filter inductance is small, otherwise the second voltage spike will dominate. Therefore, there are two transient design methods [35]: energy storage-based transient design with large output filter inductance for the second voltage spikes suppression and ESR- and ESL-based transient design with small output filter inductance for the first voltage spike suppression.

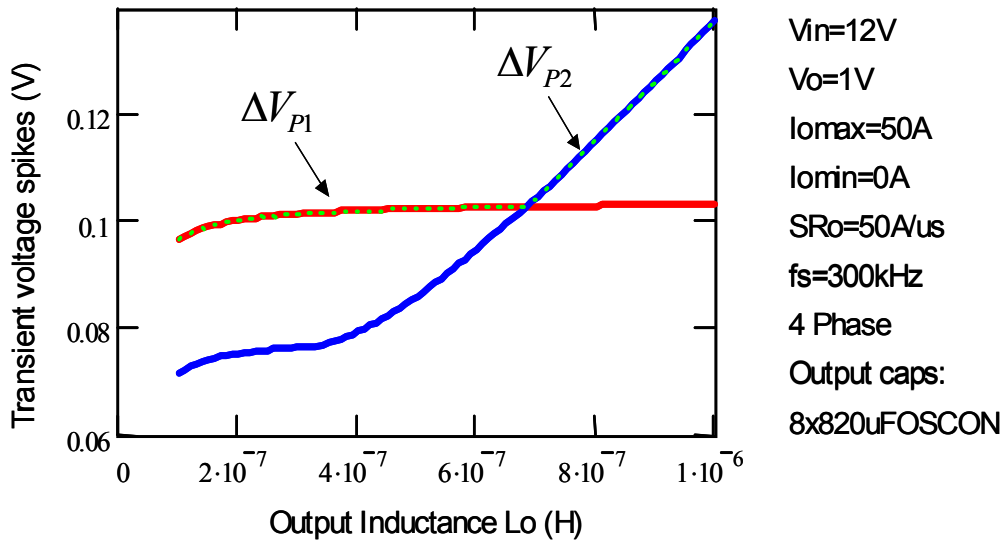


Fig.1.2.3 Voltage spikes estimation vs. output inductance

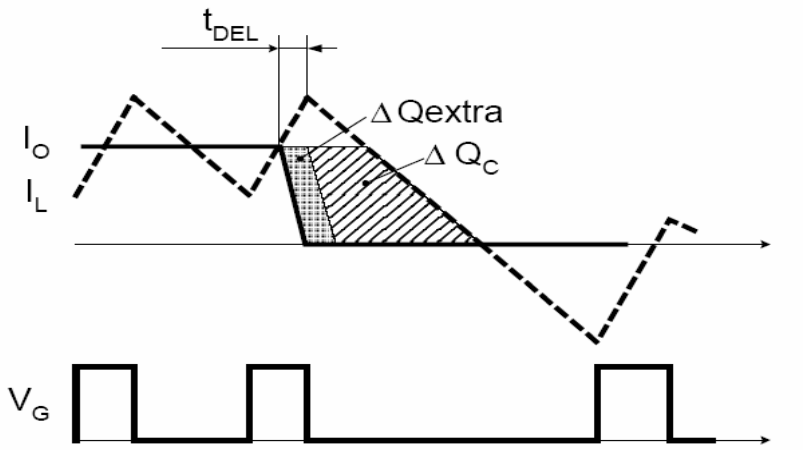


Fig.1.2.4 Delay time t_{DEL} impact on voltage spikes

The ideal controller does not have any delay time and duty cycle restriction so that it can respond to any kind of transient load immediately. In fact, the delay time in actual controller adds more energy to the output capacitor resulting in higher second voltage spike [33, 34].

Fig.1.2.4 shows the delay time t_{DEL} impact on the second voltage spike. The capacitive portion of the output voltage of Co gets the additional rise ΔV_C because the charge ΔQ_C is

delivered to the output capacitor by the filter inductor Lo. The time delay t_{DEL} that any actual controller has adds the extra charge ΔQ_{EXTRA}, which increases the second voltage spike by $\Delta Q_{EXTRA}/Co$. This extra charge can have a significant effect on the transient waveforms, especially in the low output capacitance case, for instance, the ceramic capacitors in a high frequency solution. Also, the controller parameters can significantly affect the voltage spikes and the regulator size.

1.2.2 Challenge in Voltage Regulator

With the rapid development of microprocessors, their power consumption has increased dramatically with low voltage less than 1V, up to 120A high current, up to 10A/ns high slew rate and critical output voltage tolerance requirement [1] [3-5]. The original power delivery architecture to supply the microprocessor from a single channel 5V input voltage regulator (VR) cannot meet these critical requirements any longer. A 12V input interleaved multiphase VR [23-30] becomes the most popular power architecture because of its smaller input and output current ripples and good distributed thermal capability.

The VR current slew rate cannot catch up with the CPU load current slew rate, thus the unbalanced current will be provided by the VR bulk and decoupling capacitors. Therefore, two voltage spikes occur in high slew rate transient loads. The first voltage spike is mainly determined by the ESR and ESL of capacitors and the parasitic resistances and inductances of PCB traces and the socket. The second voltage spike is mainly determined by the energy stored in filter inductance, which is related with controller delay time. A longer delay time exists in the controller and results in a higher second voltage spike.

The effective way to reduce the first voltage spike is the passive method by paralleling more capacitors for smaller equivalent ESR and ESL, which also reduces the second voltage spike. In fact, many Oscon and ceramic capacitors are mounted close to the microprocessor in the current Intel motherboard [4, 5]. VR output impedance can be minimized within a certain frequency range for fast transient response by combining different types of capacitors.

Because of large filter inductance and the delay time in an actual controller, the second voltage will dominate in less than 800A/μs slew rate transient load. However, the passive method has limited improvement on voltage suppression due to the parasitic resistance and inductance of PCB traces and the socket, thus it is not a suitable method for the increasing requirements.

The delay time in LC filter, compensation network and IC propagation delay time will increase the second voltage spike, which is related with the close loop design. High-switching operation improves the transient response by reducing the filter inductance and lessening the LC delay time, but it suffers high-switching loss. Active voltage position (AVP) [14-17] is an attractive control concept to improve the output voltage tolerance as much two times, thus the number of capacitors required for certain voltage tolerance can be reduced. However, AVP cannot achieve constant output impedance (also called load line) in wide frequency rage in an actual design due to an inaccuracy of current sensing and the delay time in linear controller, and it is impossible to eliminate due to the requirement of enough phase and gain margins for converter stability. Therefore, AC load line is always higher than DC load line in most conditions. Moreover, the small-signal model is not effective any longer in large-signal transient.

A two-stage approach [65] is one reported way to improve transient response. The first stage converter operates in a relatively low switching frequency for intermediate voltage bus,

such as 5V. The second stage converter operates in several MHZ with a low inductance (100nH) filter, and it can achieve a high bandwidth for good transient response. But a two-stage approach is a cascade system, and improving its total efficiency is the big challenge for VR design.

Current compensation, or current injection [37-41] [43-45], is another very attractive concept to improve transient response with a small extra converter. It only activates in transient periods to inject high slew rate current in step-up load and absorb energy in step-down load. The current compensators mainly handle the AC current, and then main converter only needs to handle the DC current, thus it can optimize VR efficiency. Unfortunately, linear mode current compensator has a large conduction loss due to high voltage drop and high current stress, and switching mode current compensator also has a high switching loss. Low efficiency in the extra converter is the barrier for the application.

VRM10.1 [4] defines DC-DC converters to meet the power supply requirements of desktop computer system, which has output voltage 0.8375V~1.6000V with VID control code, changing the voltage level by one 12.5mV step, and its current is up to 120A. The following load lines contain DC load line (also called static load line) and AC load line (also called transient load line) as well as maximum and minimum voltage levels.

$$\text{V}_{\text{MAX}} \text{ load line: } V_{CC} = VID - (R_{LL} \cdot I_{CC}) \tag{1-1-15}$$

$$\text{V}_{\text{MIN}} \text{ load line: } V_{CC} = VID - 0.05V - (R_{LL} \cdot I_{CC}) \tag{1-1-16}$$

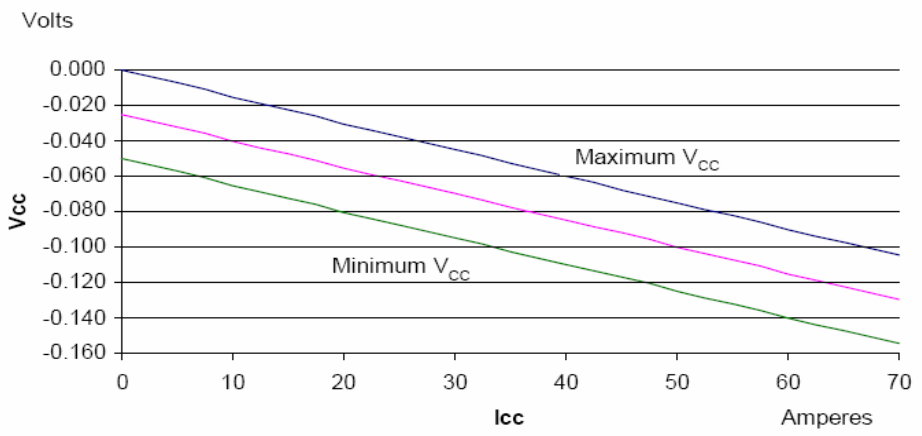


Fig.1.2.5 Intel Pentium 4 processor socket load line

Fig.1.2.5 shows the load lines contain DC and transient droop data as well as maximal and minimal voltage levels. The voltages are measured at the processor-socket Vcc and Vss pins between the voltage regulator and the processor cavity, which are taken between Vcc pin AC14 and Vss pin AC15 [4] in the standard layouts on the Intel desktop motherboard. The slew rate of current change could be several Amps per nanosecond. If not well managed, these current transients may cause the VR output voltage to go outside the regulation band and manifest them as power supply noise that ultimately limits how fast the CPU can operate. This is further compounded by the reduced noise margin in the CMOS logic circuits that result from power supply voltage scaling. While voltage overshoots may cause the CPU reliability to degrade, undershoots may cause malfunctions of the CPU, often resulting in the “blue screen”.

In current desktop and laptop computer systems, the second voltage spike always dominates under 800A /us slew rate load, so optimized close loop design contributes to reducing the delay times for fast transient response. The required socket load line for lumped model of socket 478 [5] is 1.5mΩ, and the required socket load line for lumped model of socket LGA775

[4] is 1.0mΩ, including the impedances of VR, decoupling capacitors and the resistance and inductance of PCB traces and socket.

With the further advancement of processors, the socket load line is trended to be smaller to meet the critical requirement under higher slew rate load. A large number of bulk and ceramic capacitors are mounted close to the processor to suppress the voltage spikes that occupy a lot of space in motherboard, and this is fatal in the future. To extend the close loop bandwidth is a very attractive way to suppress the second voltage spike. Although higher switching frequency operation in VR can reduce the filter inductance and capacitance for better transient response; but it leads to low VR efficiency due to high switching losses.

The preceding discussion has explained the main challenges of VR. They include the need to shrink size, meet stringent requirement on transient response, improve close-loop bandwidth, minimize the response time, reduce heat generated, and to improve efficiency in the entire load range under all input voltage conditions. This dissertation addresses these challenges. It is the goal of this work to find better approaches for future VR than the current approach, which will be problematic under future scenarios. The scope of this work covers VR in desktop computer systems.

1.3 Challenge in the High Slew Rate Isolated DC-DC Converter

In recent years, many efforts have been put into transient response improvement on VR [11, 12] [14-32] [35-69], but few efforts have been put into an isolated DC-DC converter. Although lots of technologies developed in VR can be directly applied into an isolated DC-DC converter, the isolation requirement and less than 10A/μs slew rate current in an isolated DC-DC

converter make it necessary and possible to alleviate the transient voltage spikes. An isolated DC-DC converter close loop bandwidth is mainly limited by the delay times of LC filter, compensation network and IC propagation delay time. Generally the filter LC and compensation network delay times are two key delay times.

Usually, the power transformer is used for power isolation, optocoupler can be used for feedback signal isolation in the primary control and signal transformer can be used for the driving signals isolation, which comes from the secondary controller.

High frequency operation is not an efficient way to improve the transient response in an isolated DC-DC converter due to high power loss in primary voltage, and also, the transformer leakage inductance causes incredible duty loss in the rectifier that increases power loss.

In an isolated DC-DC converter, primary topologies can be a half-bridge, full-bridge, forward, or flyback converter, and secondary rectifiers can be current doubler, full-wave rectifier or single-wave rectifier. Fig.1.3.1 shows the isolated DC-DC converter with primary control, which utilizes the low speed optocoupler in the feedback signal, which has 10~30 kHz bandwidth limitation, and it easily causes converter instability issues and much lower close loop bandwidth in spite of switching frequency operation. Therefore, it is very difficult to improve the transient response in primary control.

Fig.1.3.2 shows the block diagram of isolated DC-DC converter with secondary control, which adopts the signal transformer to isolate the primary side driving signal from the secondary controller, and no optocoupler exists in secondary control. The startup circuit is bulky and costly to supply the secondary controller, otherwise the converter won't work. How to design a simple startup circuit is the big challenge.

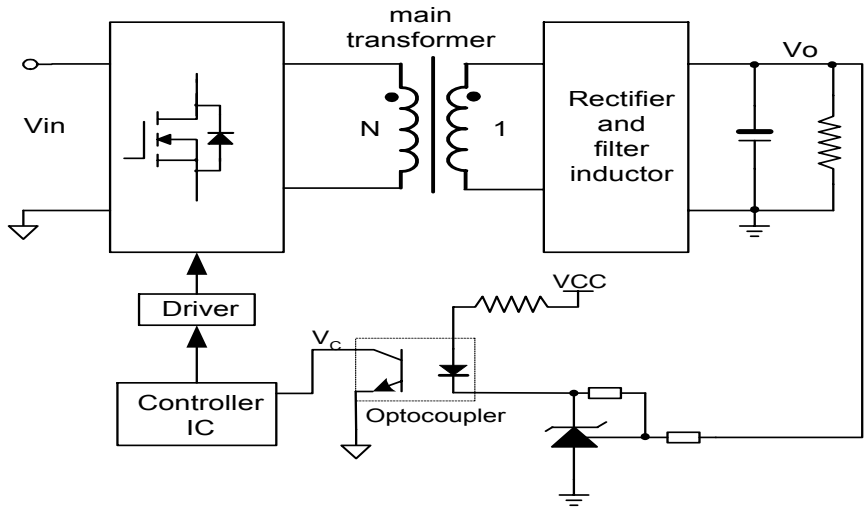


Fig.1.3.1 Isolated DC-DC converter with primary control

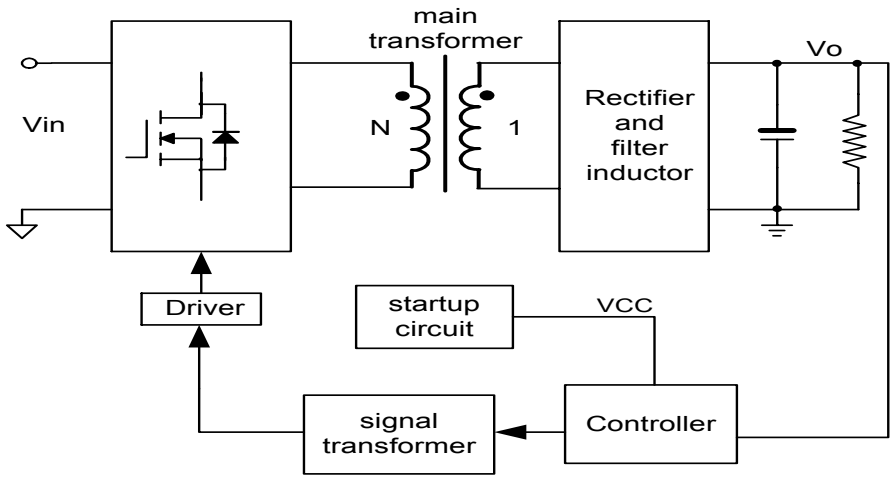


Fig.1.3.2 Isolated DC-DC converter with secondary control

Switching mode current compensator with secondary side control that operates 1MHz has been carried out to remove the optocoupler, which has 10~30 kHz low bandwidth limitation for transient response improvement in isolated DC-DC converter. Experimental results show obvious improvement in transient response, which can be suitable in low current applications.

In the conventional two-stage isolated converter, the first stage converter generates a regulated intermediate voltage bus at a relatively low switching frequency, and the second stage converter can easily achieve soft switching in high frequency operation and high efficiency due to 0.5 duty cycle operation in primary side. But the transient response is mainly determined by the first stage converter, so there is a trade off between the efficiency and transient response. One simple, novel control method is proposed to improve the transient response and efficiency of two-stage isolated converter, which has maximum 0.66 duty cycle in second stage.

In the complementary controlled converter, it can easily achieve soft switching in primary side by utilizing the energy stored in the leakage inductance. However, it introduces the double pole-zero effect composed of the magnetizing inductance and the input capacitors of half-bridge converter, which harms the converter stability, complicates the design of compensation network and deteriorates the transient response. A balancing winding network is proposed to eliminate this double pole-zero effect, which is composed of one small gauge winding, two small diodes and one blocking capacitor. In transient, the energy transfers instantly between the blocking capacitor in balancing winding network and the magnetizing inductance, resulting in the mitigation of the double pole-zero effect. It not only improves the transient response, but also it simplifies the compensation network design.

Conventional post regulators usually have soft switching in primary side, but most of them are in series with secondary main rectifier that introduces extra large conduction loss. In wide range input applications, such as hold up time requirement in server power supplies, the converter suffers large voltage stress in the secondary rectifier because it is designed in low line and operates in high line with small duty cycle, which further decreases the efficiency. Parallel post regulator is the proposed topology to improve the transient response and efficiency for

isolated DC-DC converters, which is in parallel with main rectifier and only delivers small portion of required power, such as 10 percent. Most of the power, 90 percent, is delivered by unregulated main rectifier with very high efficiency. Also it reduces the voltage stress due to the modified transformer turn ratio; furthermore it can adopt flexible control methods. In an experimental prototype, parallel post regulator has up to 8 percent efficiency improvement compared with a conventional half-bridge converter.

The above discussion covers the main challenges of the isolated DC-DC converter. They include the need to reduce the controller delay times, enhance the transient response and improve the power density and efficiency for the entire range and load conditions. It is the goal of this work to find better approaches for the isolated DC-DC converter.

1.4 Dissertation Outline

Chapter 1 introduces the background of this work. First, it briefly introduces VR history with the development of CPUs. Then, the chapter analyzes the output voltage spikes estimation at high slew rate load conditions. Finally, it discusses the main challenges in interleaved VR and also presents the main challenges in the isolated DC-DC converter. The basic reason for the transient voltage spike at high slew current is that the slew rate of converter current is much slower than that of the load current and the existence of delay times in the controller. The discussion shows the first voltage spike is determined by the ESR and ESL of capacitors and the resistance and inductance of PCB traces and socket; the second voltage spike is determined by the energy stored in filter inductors, which is related to the close loop bandwidth determined by the delay times of LC filter, compensation network and IC propagation delay times.

Chapter 2 reviews current technologies for high slew rate VR to improve the transient response. First, it presents the passive method by combining different types of capacitors to reduce output impedance and then summaries their limitations. Second, it discusses the advantages and limitations of existing control technologies to minimize the compensation network delay time and the limitation of current linear control methods. It also analyzes existing active topology methods and active transient current compensators by reducing the filter inductance for fast transient response. Their limitations are also presented. The discussion in Chapter 2 shows that active current injection is an attractive concept for future VR because it only activates in transient, thus the main converter can be optimized for better efficiency, but this concept results in low efficiency in the extra converter. It concludes that the efficiency, fast transient response and smaller delay times in the controller are the main technical barriers and tradeoff always exists between them.

Chapter 3 proposes active transient voltage compensator (ATVC), which injects voltage source instead of current source in prior arts to improve the transient response and efficiency. A turn ratio N:1 transformer is used in ATVC to inject the voltage source into the power distribution path, which benefits the reduced current rating in extra converter by a factor (1+N). Thus, it significantly reduces the conduction and switching losses. At the same time, it injects (1+N) times higher slew rate current than in the conventional current compensation concept based on the same filter inductance. Also, ATVC only engages in transient periods with several MHZ operations for small size. Furthermore, the number of Oscon capacitors required for certain voltage tolerance can be reduced, because the output impedance of VR is the internal impedance of ATVC so that it is easy to control reduced by close loop control.

A new control method, combined linear and adaptive nonlinear control, is proposed to reduce the delay times in ATVC controller for fast transient response in Chapter 3. Conventional linear control has a large delay time because of the requirement of enough phase and gain margins for converter stability. Adaptive nonlinear control with very small delay time only activates in transient periods, which only injects the first nonlinear signal by one shot circuit, thus there is no stability problem in the nonlinear control. It also simplifies the linear controller design. Tested results in VRM9.0 show the delay time of ATVC controller is shortened from 2.4μs to 0.2μs, resulting in great improvement in transient response.

Maxwell 3D magnetic simulations have been carried out in Chapter 3 to optimize the ATVC transformer design based on leakage inductance, turn ratio and core size.

Pspice simulations have been carried in two ATVC topologies: series ATVC and parallel ATVC with different sockets. Then experimental parallel ATVC prototype has been carried out on the Intel motherboard due to its simplicity and smaller power loss. By utilization of ATVC with combined linear and adaptive nonlinear control, the VR AC load line improvement is up to 90 percent of expected load line improvement and up to 25 percent of the total load line including AC and DC load line. The size for ATVC is about $25\times25mm^2$ with custom control IC. The influence of IC propagation delay time and transformer is also addressed, especially in high current, high slew rate transient in this chapter.

Chapter 4 discusses the transient improvement in isolated DC-DC converter. Since the limitation of optocoupler bandwidth is in primary control, switching mode current compensator is proposed in secondary side in the isolated DC-DC converter to eliminate the shortcomings of the optocoupler. The extra converter achieves 250 kHz close loop bandwidth and great transient improvement in tested isolated DC-DC converter prototype.

This chapter also presents a novel control method for the two-stage isolated converter to overcome the bad transient response in conventional control. The novel control improves the transient response and efficiency with simple control; it also has large duty cycle in second stage, high slew rate of DC conversion ratio and large step-down ratio.

Chapter 4 also gives a proposed solution to mitigate the double pole-zero effect in the complementary controlled converter: a balancing winding network. The complementary controlled converter can achieve soft switching operation in primary naturally by utilizing the energy in the transformer leakage inductance. It also introduces the double pole-zero effect composed of the magnetizing inductance and the blocking capacitors, which dramatically harms the stability, complicates the compensation network design and causes bad transient response.

Also this chapter proposes a new topology, parallel post regulator for the high-efficiency wide range input converter. The conventional post regulator is always in series with the main rectifier resulting in extra conduction losses other than its soft switching in primary. In wide range input applications, the converter is designed in low input and operates in high input voltage with small duty cycle, which makes it difficult to achieve soft switching in primary and increases conduction loss and voltage stress on secondary main rectifier leading to efficiency deterioration. Parallel post regulator is in parallel with main rectifier, and it only delivers a small portion of required power, such as 10 percent. Most of the power, 90 percent, is supplied by the unregulated main rectifier with maximum efficiency. The parallel post regulator also reduces the secondary rectifier's voltage stress due to a high transformer turn ratio. In the experimental prototype, parallel post regulator improves efficiency up to 10 percent than that in the conventional half-bridge converter. Also, the secondary side control with trailing edge modulation is discussed to improve the transient response in this chapter.

Chapter 5 summarizes future work on the optimization of main VR and ATVC from a systematic point and also gives some possible ideas for high-switching, high-frequency VR design.

CHAPTER TWO: REVIEW OF TECHNOLOGIES IN HIGH SLEW RATE VR

As discussed in Chapter 1, there are two spikes in VR output voltage at high slew rate transients. The first voltage spike is mainly determined by ESR, ESL of capacitors, which can be minimized by combined different types of capacitors, but it is limited by the parasitic resistance and inductance of PCB traces and socket in the power distribution path [3-5], and it is also limited by the available space in the motherboard.

The second voltage spike contains the capacitive voltage drop mainly determined by the energy stored in VR filter inductors, resistive voltage drop determined by the ESR of capacitors and slight inductive voltage drop due to low slew rate VR current. The delay times in close loop control will increase the second voltage spike, which is mainly determined by LC delay time, compensation network delay time and propagation delay time. Generally, low frequency output impedance is optimized by close loop control, and high frequency output impedance is minimized by combining different types of capacitors, especially ceramic capacitors. Also, high unity gain bandwidth helps reduce the second voltage spike.

2.1 Passive Methods to Reduce Voltage Spikes

In current desktop and laptop computer systems, a large number of different types of capacitors are mounted close to the CPU to suppress the voltage spikes in transient load. Fig.2.1.1 shows the current slew rate distribution in VR system. The highest slew rate current is provided by the die capacitance and packaging capacitance, up to several A/ns, and the decoupling ceramic capacitor handles current slew rate between several hundred to several A/ns. Finally, the VR only needs to handle several hundred A/μs current slew rate load, which makes it

possible to be optimized by close loop control. Different power distribution architecture has different socket output impedance and current slew rate distribution. The target socket output impedance is about 1.5mΩ in SKT478 power distribution model, and the target socket output impedance is about 1mΩ in LGA775 power distribution model, including VR output impedance, parasitic resistance and inductance of PCB traces and socket.

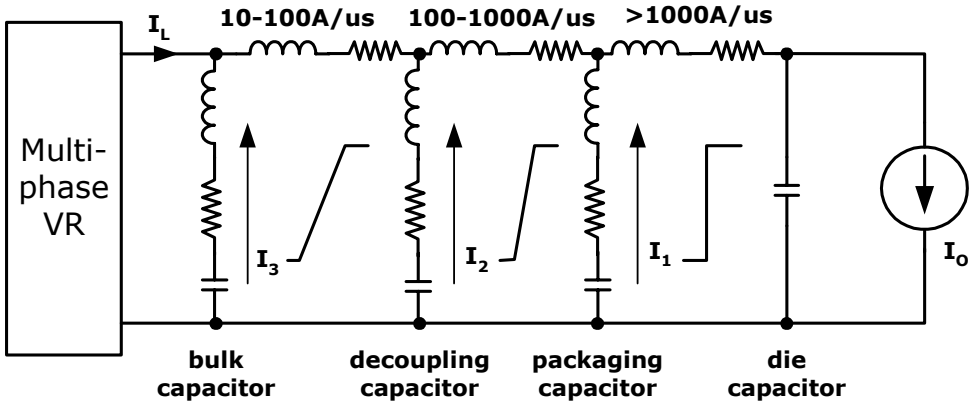
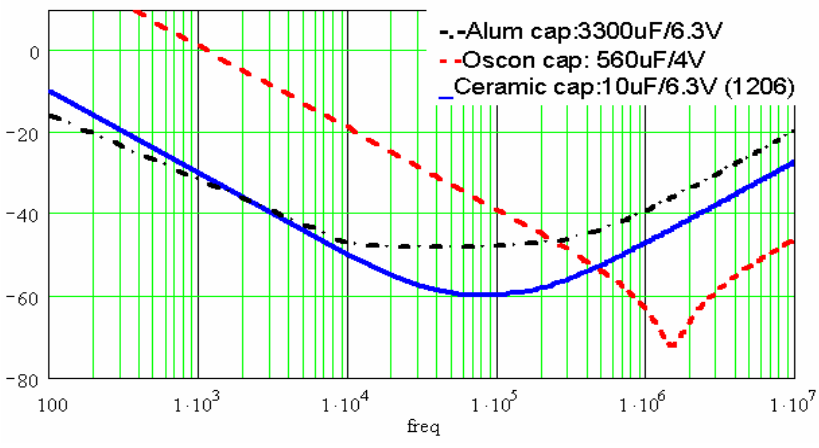
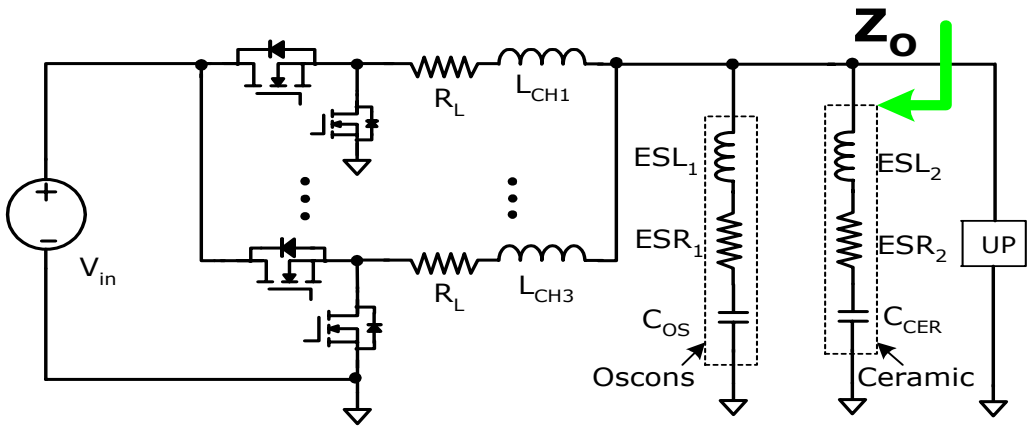


Fig.2.1.1 Current slew rate distribution in the VR system

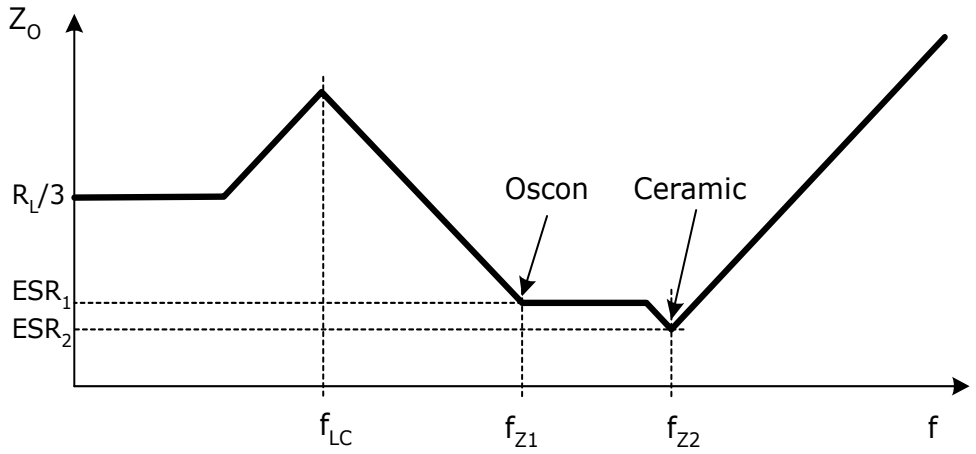
2.1.1 Combination of Different Types of Capacitors



(a)



(b)



(c)

Fig.2.1.2 The output impedance of 3-Ch VR and frequency characteristics of different capacitors: (a) impedance curves of Alum, Oscon and ceramic capacitors, (b) 3-Ch VR, and (c) the asymptotic curve of open loop output impedance

Different types of capacitors have different characteristics. For example, an aluminum capacitor has large capacitance with large ESR and ESL, Oscon capacitor has relatively low ESR and ESL with large capacitance in low voltage rating and ceramic capacitor features lower ESR and ESL than OSCON capacitor with lowest capacitance as shown in Fig.2.1.2 (a).

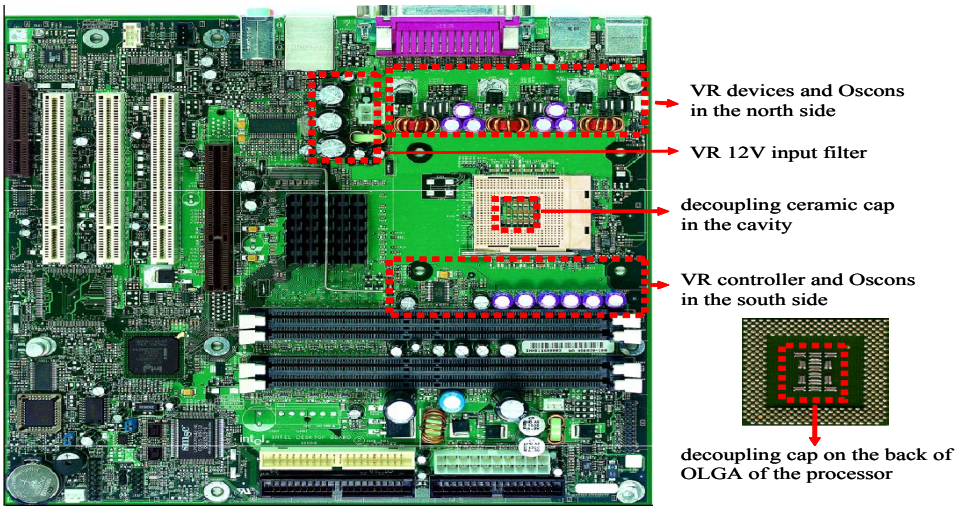
Fig.2.1.2 (a) shows the frequency characteristic of Oscon and ceramic capacitors. Fig.2.1.2 (c) shows the asymptotic curve of open loop output impedance of VR that has three main zeros in the curve. VR filter inductance and Oscon capacitor C_{OS} form the first zero (f_{LC}), ESR_1 and Oscon capacitor C_{OS} form the second zero (f_{Z1}), and ESL_2, ESR_2 and decoupling capacitor C_{CER} form the third one (f_{Z2}) that are in MHZ frequency range. The resonant frequency of Oscon capacitor is the critical design frequency for VR constant output impedance, which can be obtained by the following equation:

$$f_{Z1} = \frac{1}{2\pi \cdot ESR_1 \cdot C_{OS}} \tag{2-1-1}$$

The commonly used capacitors in a desktop motherboard are 560μF/4V Oscon capacitor (6.4nH, 9.28mΩ) and the 10μF/6.3V ceramic capacitor (1.15nH, 3.5mΩ). With a simple calculation, we get f_{Z1} =30.6 kHz. Below f_{LC} , the filter inductor resistance R_L and filter inductance dominate; Oscon capacitance dominates between f_{LC} and f_{Z1} . The VR output impedance can be constant within f_{Z1} by close loop control that will be discussed later. Thus, f_{Z1} is the minimal bandwidth for VR constant output impedance. Then, ESR_1 of Oscon capacitors dominates until the ceramic capacitance takes over at f_{Z2} ; beyond f_{Z2} , ESL_2 of ceramic capacitors dominates. The output impedance between f_{Z1} and f_{Z2} can be minimized with a proper combination of different types of capacitors.

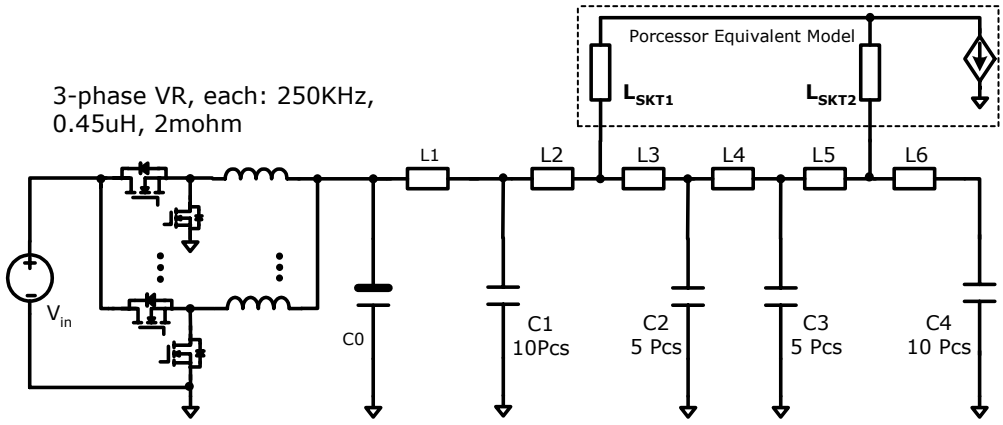
2.1.2 Output Impedance Analysis of Intel Motherboard with SKT478

Fig.2.1.3 (a) shows a 3-Ch interleaved multiphase VR on an Intel motherboard D850MV where VR occupies more than one-third the motherboard space including input, output filter and decoupling capacitors. In order to minimize the influence resistances and inductances of socket and PCB traces, a large number of decoupling ceramic capacitors are located on the back of OLGA of the processor and in the cavity of SKT478.



Intel desktop motherboard D850MV

(a)



(b)

Segment	Resistance	Inductance	Capacitance	ESR (each)	ESL (each)
L1	0.27mΩ	80pH	9 OSCON 560uF	9.28mΩ maximum	6.4nH maximum
L2	0.33mΩ	113pH	3 Al Electrolytic 3300uF	12mΩ maximum	5nH maximum
L3	0.392mΩ	104pH	38 1206 package 10uF	3.5mΩ typical	1.15nH typical
L4	0.196mΩ	52pH			
L5	0.392mΩ	104pH			
L6	0.64mΩ	200pH			

(c)

Fig.2.1.3 Intel desktop motherboard D850MV with SKT478: (a) top view of Intel desktop motherboard D850MV, (b) SKT478 power distribution (PD) model with VR and (c) corresponding parasitic parameters in SKT478 PD model

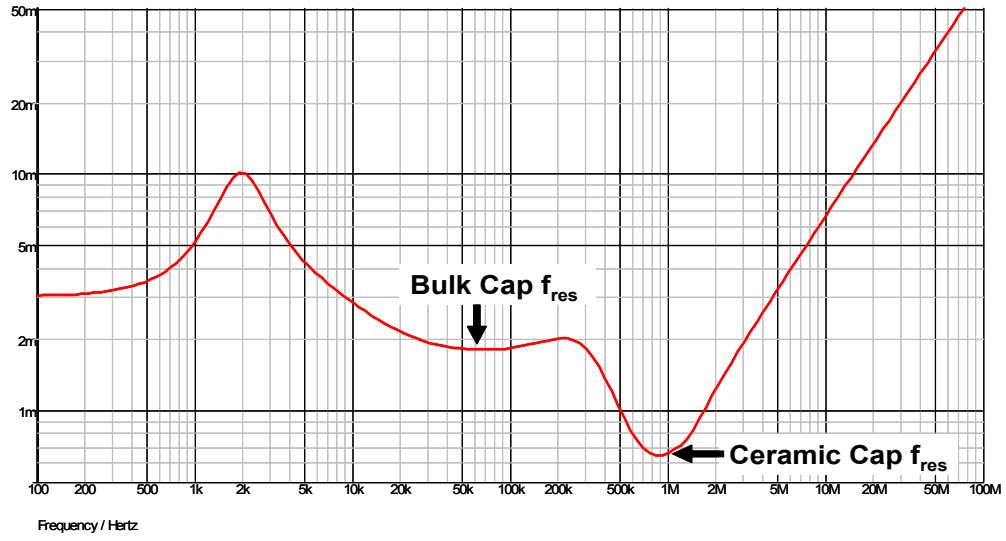


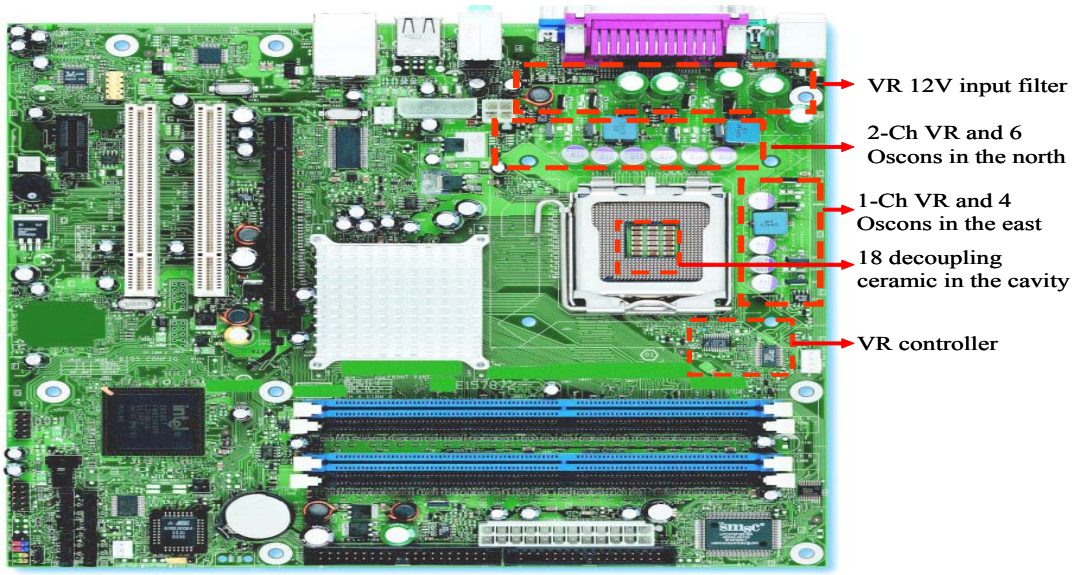
Fig.2.1.4 Output impedance of SKT478 PD model with VR

Fig.2.1.3 (b) shows the lumped SKT478 power distribution model with 3-Ch VR [5], which operates in 250 kHz with 0.45μH, 4mΩ filter inductance per channel. Corresponding parasitic parameters are shown in Fig.2.1.3 (c). Simplis software is used to analyze the output impedance of the SKT478 PD model shown in Fig.2.1.4, which has almost constant open loop

output impedance between 30 kHz and 150 kHz with a combination of different types of capacitors. Also, it is easy to achieve constant output impedance with 30 kHz by active voltage position method or active droop control [14-20].

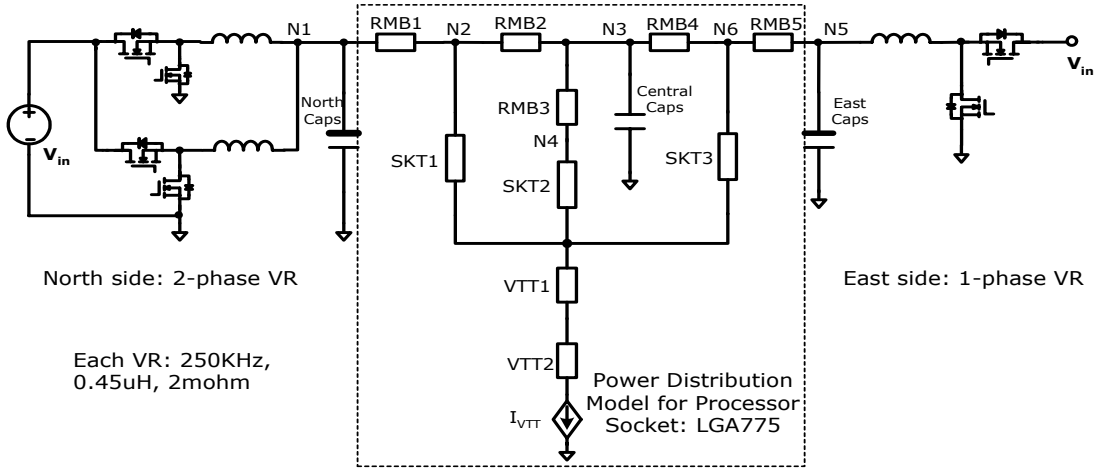
2.1.3 Output Impedance Analysis of Intel Motherboard with LGA775

Fig.2.1.5 (a) shows the Intel desktop motherboard D915GUX with 2-Ch VR on the north side with 6 pieces of 560μF/4V Oscons and 1-Ch VR on the east side with 4 560μF/6.3V Oscons. Eighteen pieces of ceramic capacitors are located in the cavity of LGA775. 3-Ch VR operates in 250 kHz with 0.45μH inductance per channel. Fig.2.1.5 (b) shows the lumped LGA775 power distribution model with 3-Ch VR [4], and the corresponding parasitic parameters, including PCB trace, socket and capacitors, are shown in Fig.2.1.5 (c).



Intel Desktop Motherboard D915GUX

(a)



(b)

Segment	Resistance	Inductance	Segment	Resistance	Inductance
RMB1	0.93mΩ	104pH	VTT1	0.42mΩ	240pH
RMB2	0.85mΩ	88pH	VTT2	0.91mΩ	42pH
RMB3	0.70mΩ	65pH	C0: 3360uF 6 OSCONs	1.0mΩ	560pH
RMB4	0.87mΩ	92pH			
RMB5	0.97mΩ	106pH	C1: 150uF 15 Ceramics	0.16mΩ	54pH
SKT1	0.38mΩ	40pH			
SKT2	1.13mΩ	120pH	C2: 2240uF 4 OSCONs	1.5mΩ	712pH
SKT3	0.29mΩ	30pH			

(c)

Fig.2.1.5 Intel desktop motherboard D915GUX with LGA775: (a) top view of the Intel desktop motherboard D915GUX, (b) LGA775 power distribution model with VR and (c) corresponding parasitic parameters in LGA775 PD model

Fig.2.1.6 shows the output impedance at different testing points: I_{VTT}, N_2 and N_4. N_2 is the tested load line point. Because LGA775 adopts different power distribution architecture other than SKT478, the output impedance at I_{VTT} has almost constant output impedance between 30 kHz and 400 kHz, which is much better than that in SKT478. Therefore, it can achieve better transient response within this free flat bandwidth. Below 30 kHz, it is easy to achieve the constant output impedance by active voltage position method or active droop control [14-20].

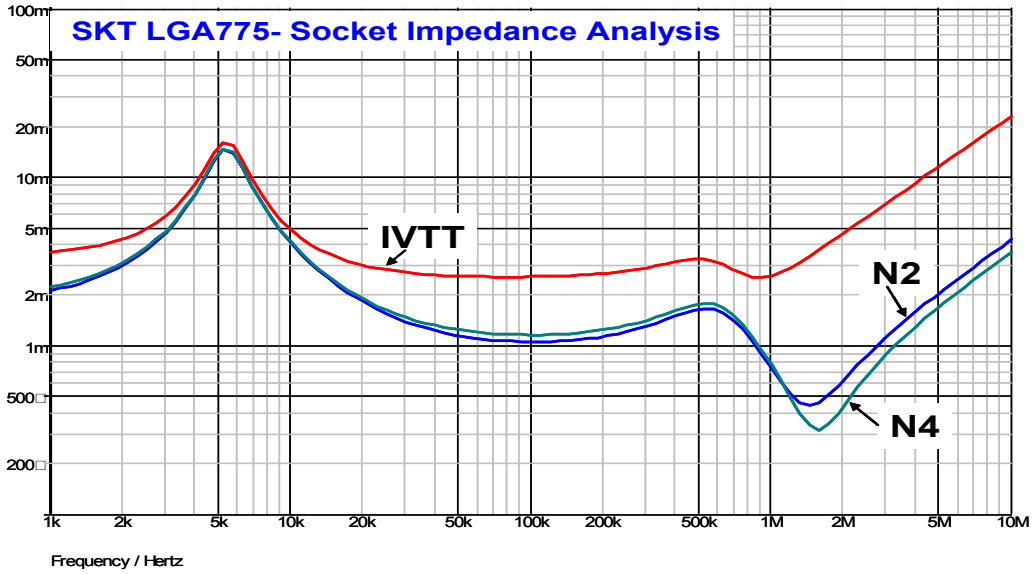


Fig.2.1.6 Output impedance of LGA775 PD model with VR

2.1.4 Limitation of Passive Methods

The Oscon capacitor has good performance in low frequency range, and the ceramic capacitor has better characteristics in MHZ frequency range. With the combination of Oscon and ceramic capacitors, output impedance can be flat, which can minimize the transient voltage spike within the certain frequency range, such as 30~500 kHz in LGA775 PD model, which still needs a large number of Oscon and ceramic capacitors close to processor. However, the socket output impedance cannot be reduced further due to the limitation of the parasitic resistances and inductances of PCB traces and socket, which are determined by the PCB layout and socket.

Fig.2.1.7 shows that the output impedance of N2 only can be 0.7mΩ by paralleling 60 pieces of 560μF/4V Osons on north side and it only achieves about 0.52mΩ by paralleling 100 pieces of 560μF/4V Oscons due to the limitation of parasitic resistance and inductance of PCB

traces and socket. It is obvious that the passive way has the limitation to reduce the output impedance for fast transient response as follows:

1) Oscon capacitor has a large ESR, which determines the number of Oscon capacitors for the required constant output impedance, eventually, yet the capacitance is over-designed.
2) Oscon capacitor has a large ESL, which requires a lot of ceramic capacitors to suppress the first voltage spike and has no more space in cavity for ceramic capacitor.
3) The large size of the Oscon capacitor occupies a large space on the motherboard.
4) The output impedance has limitations due to the parasitic resistance and inductance of PCB traces and socket.

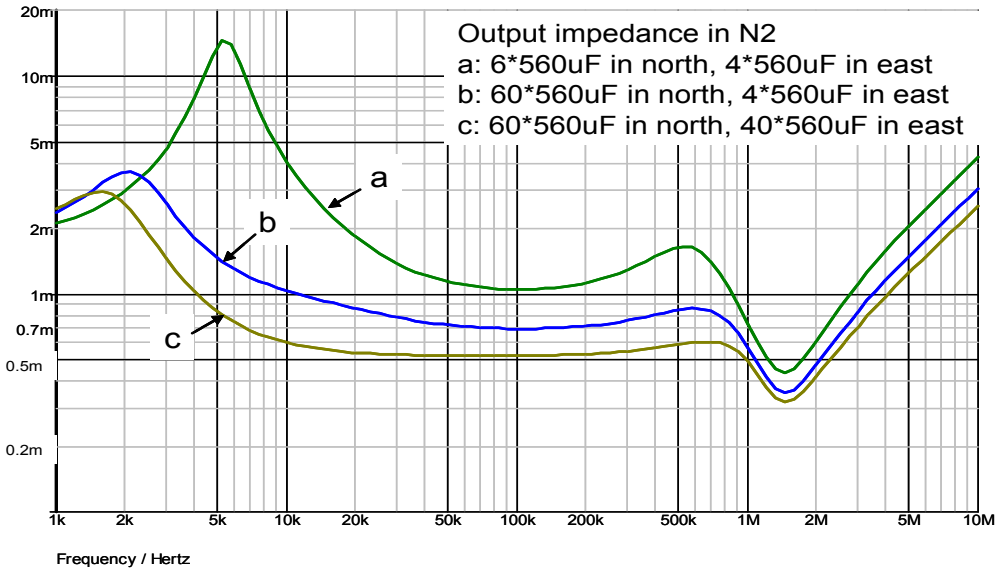


Fig.2.1.7 Output impedance of N2 in LGA775 PD model with increased Oscons

2.2 Existing Control Technologies for High Slew VR and Limitations

In control theory, any switching regulator with feedback loop includes a plant and a compensator. The plant in a switching regulator is its power stage including a low-pass filter. The compensator senses the output voltage and somehow changes the duty cycle of voltage regulator to keep the output voltage within the required window. There are many different disturbances, such as input voltage, temperature, aging and load current that change the output voltage. But for the considered power distribution system with a high-slew-rate transient type of load, the main disturbing factors are the load current and the slew rate of the current transient.

There are a lot of control techniques for interleaved multiphase VR: voltage mode in Fig.2.2.1, peak current mode in Fig.2.2.2, valley current mode control in Fig.2.2.3, average current mode in Fig.2.2.4, hysteretic mode in Fig.2.2.5, and V^2 mode in Fig.2.2.6.

They can be divided into the following two groups:

1.Control techniques that do not sense the load current or its changes directly do not feed-forward or feedback this signal. This is group-control with a “slow” feedback loop, because it senses the disturbance caused by the load current indirectly and uses this signal in the main feedback loop. This group improves the dynamic response by increasing the unity-gain-frequency bandwidth [34] [57-62].

2. The control techniques that do sense the output current transient directly or through the related change of the output voltage use this signal in a fast feedback loop or feed-forward it to improve the transient response. The main examples of this group are hysteretic mode [53] [63] [67, 68] and V^2 mode control [21, 22] [51] techniques. This is group-control with a “fast” feedback loop.

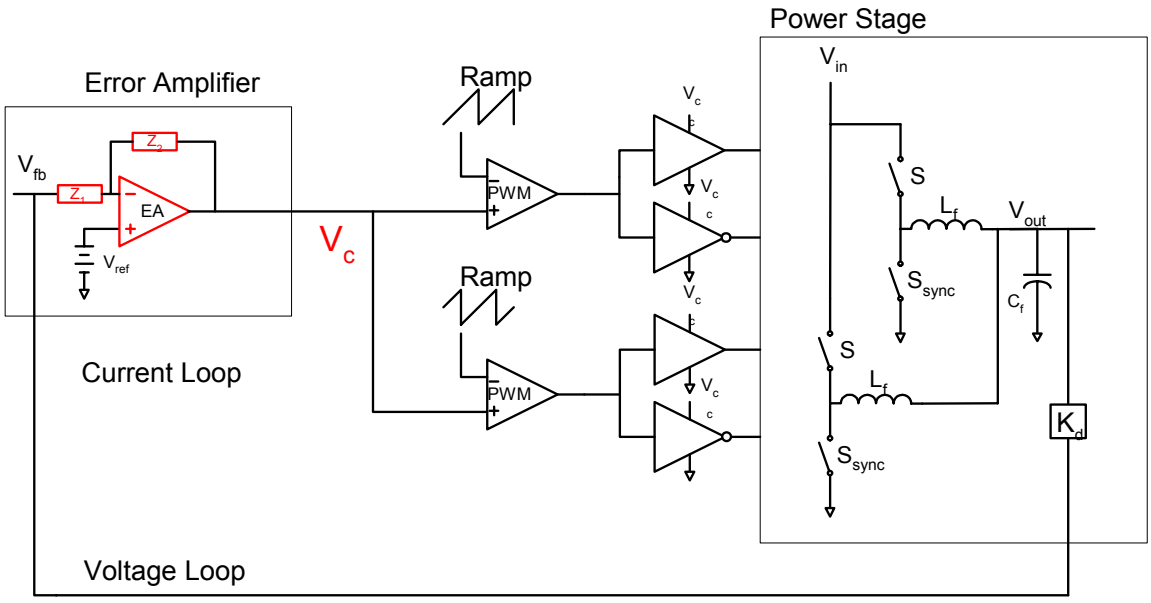


Fig.2.2.1 Voltage mode control

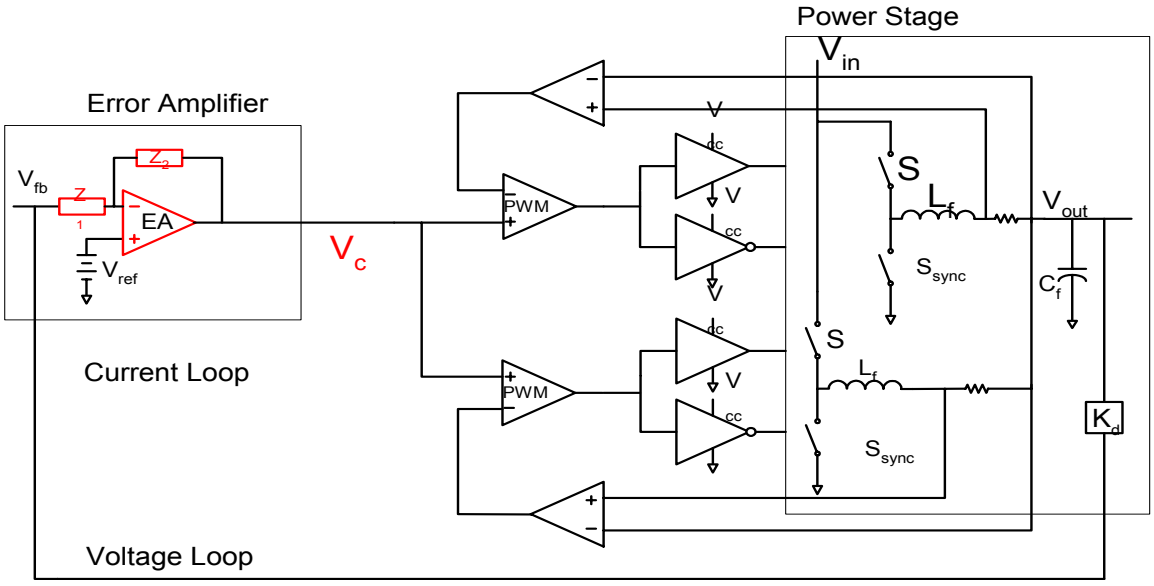


Fig.2.2.2 Peak current mode control

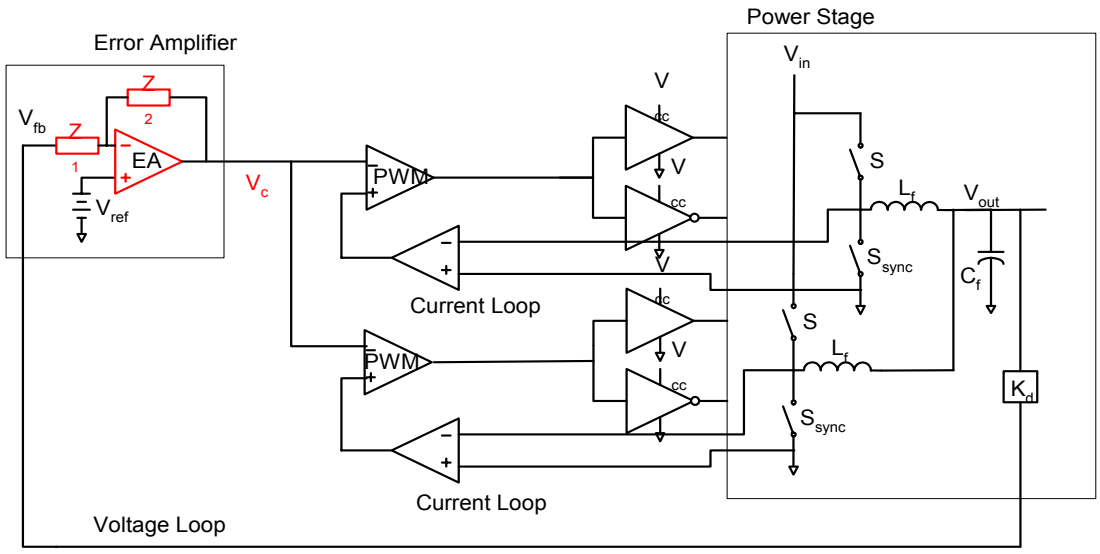


Fig.2.2.3 Valley current control

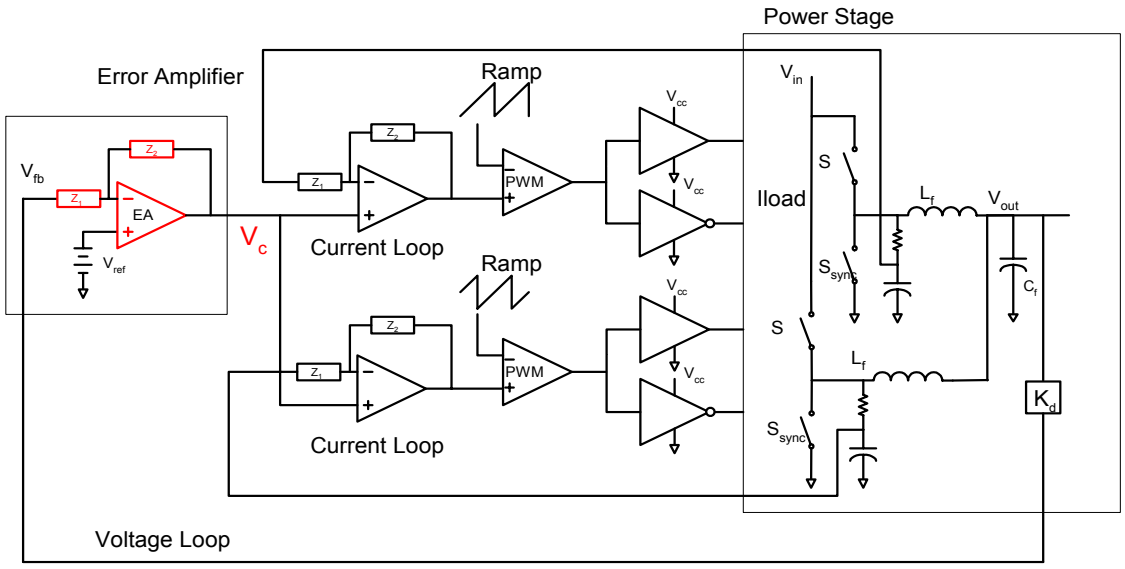


Fig.2.2.4 Average current control

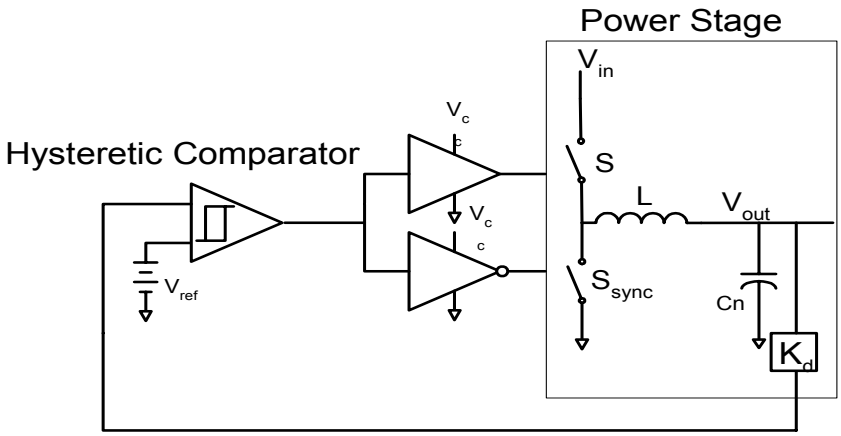


Fig.2.2.5 Hysteretic control

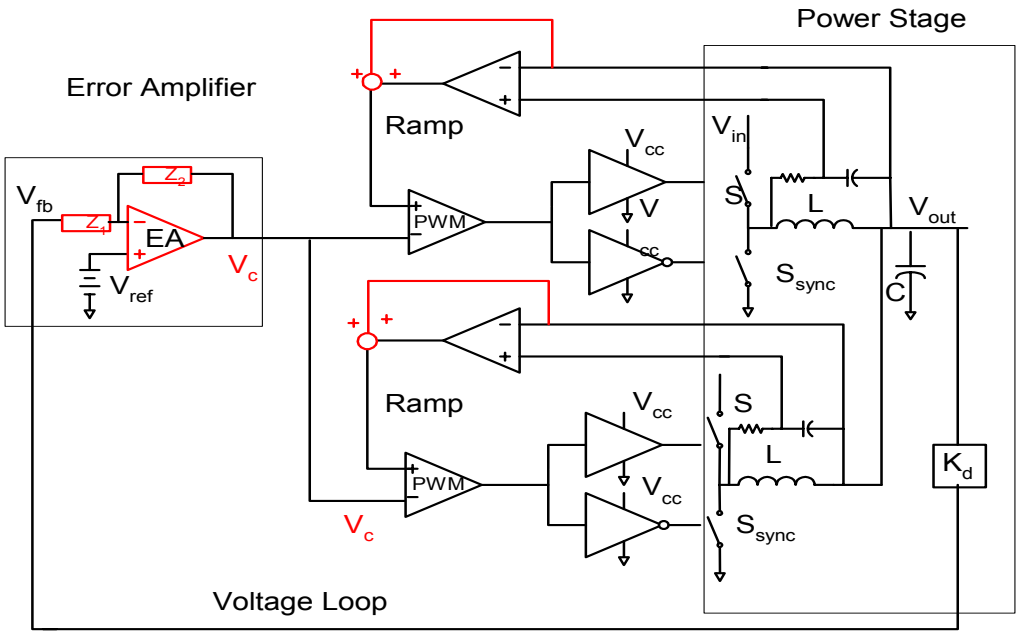


Fig.2.2.6 V^2 control

2.2.1 Control with Slow Feedback Loop

This approach includes the voltage mode control, peak current mode control, valley current mode control and average current mode control, which are very popular in most generic applications. Usually, small signal model is used to design and optimize the large signal transient characteristic by improving the unity-gain bandwidth.

Voltage mode control shown in Fig.2.2.1 is very simple and easily achieves interleaving by shifting ramp phase, but it is very difficult to achieve current sharing between each channel due to no current information.

Current mode current introduces a fast inner current loop to cancel one pole of LC filter, and then simplifies the compensation network design. It has faster transient response than voltage mode control. The peak current mode control in Fig.2.2.2 is carried out by sensing the current signal through the top switch. The disadvantage of the current sensing in the top switch current is so narrow that it is very easy to pick up noise in high frequency operations. The valley current mode control in Fig.2.2.3 can be used in high frequency operation due to the wide current sensing signal of the bottom switch. Fig.2.2.4 shows average current mode that has a much smaller noise by sensing the inductor current.

These control methods do not sense the load current and its changes directly, so there will be a delay time in voltage sensing, which will add more extra energy into filter inductor in step down resulting in higher second transient voltage spike. Vice versa, it increases the voltage drop in step-up load.

2.2.2 Control with Fast Feedback Loop

The hysteretic mode control (also called bang-bang) is the simplest control approach, which has the excellent dynamic characteristics because no compensation network exists in control loop. It reacts on the load-current transient in the switching cycle where the transient occurs. Its transient response time only depends on the delay time in the hysteretic comparator and the drive circuitry. Those delays depend mostly on the selected component performance, thus the hysteretic control is the fastest solution in theory. The other advantage of the hysteretic controller is that its duty cycle covers the entire range from zero to one, which is very important to decrease the recovery time of the output voltage after a load current transient.

The main disadvantage of hysteretic mode control is the sensitivity to noise and variable frequency control. The tight tolerance requirements for the output voltage make it even more difficult to separate the output voltage change caused by a load current transient from noise, especially in a multiphase synchronous buck converter. The switching frequency of hysteretic control can be obtained [68] through:

$$f_S = \frac{V_o \cdot (V_I - V_o) \cdot (ESR - t_{del} / C_o)}{V_I \cdot (V_I \cdot ESR \cdot t_{del} + Hyst \cdot L - ESL \cdot V_I)} \tag{2-2-1}$$

$$ESL \le ESR \cdot t_{del} + Hyst \cdot L \cdot D / V_o \tag{2-2-2}$$

The above two equations show that the switching frequency of hysteretic control strongly depends on ESR, ESL, propagation delay time t_{del} and the hysteretic window Hyst when the ESL meets specific conditions. If it does not meet the conditions, the voltage drop across the ESL during the switching period will exceed the hysteretic window, and then the switching frequency will become too high and uncontrollable due to the parasitic inductance of PCB trace and socket, except for the ESL of capacitors. It becomes even worse in small filter inductance and high slew

rate current conditions. Another shortcoming of hysteretic control is the variable switching frequency, which makes it difficult to design a filter inductor to suppress EMI.

The V^2 mode control also has very fast transient response characteristics by using the output-voltage ripple as the ramp signal of the modulator based on the assumption that the voltage ripple of the output capacitor depends mostly on the ESR, and the part of the ripple caused by the ESL and C_O is negligible. In this case, the ripple is proportional to the inductor current ripple. At the transient, this voltage carries the information about the load-current change directly to the comparator, bypassing the slow main feedback loop. The V^2 mode control actually can be defined as a sort of hysteretic control having the additional error amplifier. This amplifier enables an increase of the hysteretic window of the comparator without degrading the accuracy of the output voltage.

On the other hand, the use of output ripple voltage as the ramp signal causes the stability to depend greatly on the output capacitor parasitic parameters. This dependence is especially problematic when using many high frequency ceramic or film capacitors in parallel as the output filter. The voltage ripple is not exactly proportional to output inductor current, and it has $\pi/2$ out of phase with the output inductor current.

There is another problem related to controllers that sense information about load current by using the output capacitor's ESR: their frequency dependence from the output filter parasitic parameters and its variation related to tolerances and variations of the capacitor characteristics. This problem could be solved [22] but increases the complexity of controller.

2.2.3 Active Voltage Positioning Methods

Any control discussed above allows implementation of the active voltage position or active droop compensation methods to achieve constant VR output impedance.

Constant VR output impedance is used to reduce voltage spikes, which is used to reduce the power loss of CPU by Intel Corp. [3, 4]. If the VR DC load line is equal to its AC load line, then there will be no voltage spike in transient load and the voltage tolerance only depends on output current.

$$V_O = V_{REF} - R_{droop} \cdot \Delta I_O \tag{2-2-3}$$

Fig.2.2.7 shows the active voltage position (AVP) concept [14] [16-20], which means that the DC output voltage of VR is dependent on its load. It is set to the highest level within the specification window at no load condition and to the lowest level by feeding back the current of the output load or filter inductors at full load. This concept increases the output voltage dynamic tolerance by as much as twofold, thus the number of bulk capacitors required to meet the output voltage regulation can be reduced. It also reduces the average power consumption of the CPU in high current, therefore keeping the CPU within its thermal limit. The AVP concept is available in many commercial control ICs.

Fig.2.2.8 shows the AVP implementation circuit. Each channel current signal can be obtained by a different sensing method [67]. The average current is achieved by current averaging block, and it is multiplied by gain K to sum up to the output feedback signal. The output voltage will decrease with the current load when reference voltage is constant. Also, the average current compares with each channel current to modulate slightly the duty cycle for current sharing between each channel.

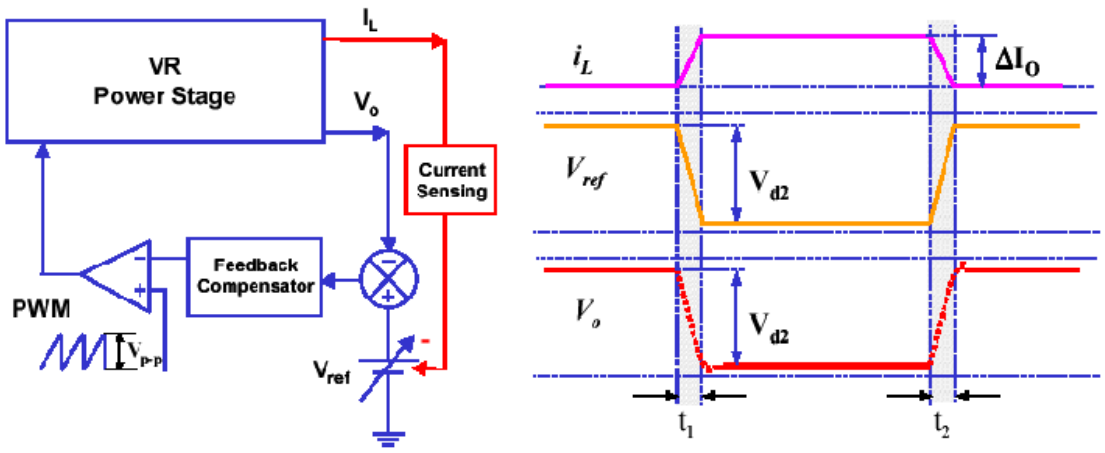


Fig.2.2.7 Active voltage positioning concept

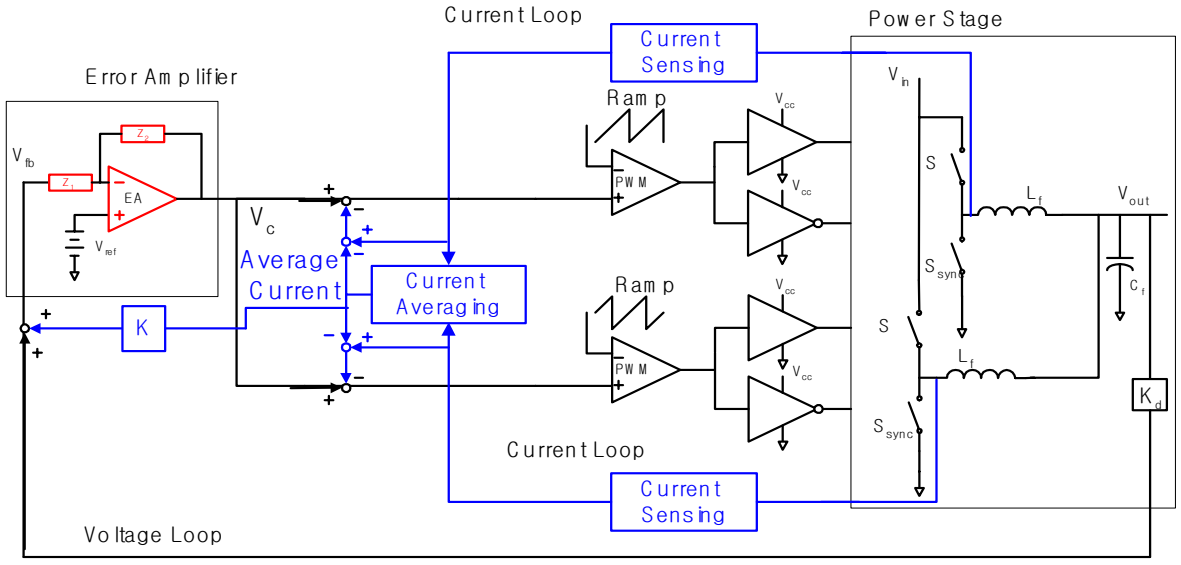


Fig.2.2.8 AVP implementation circuit

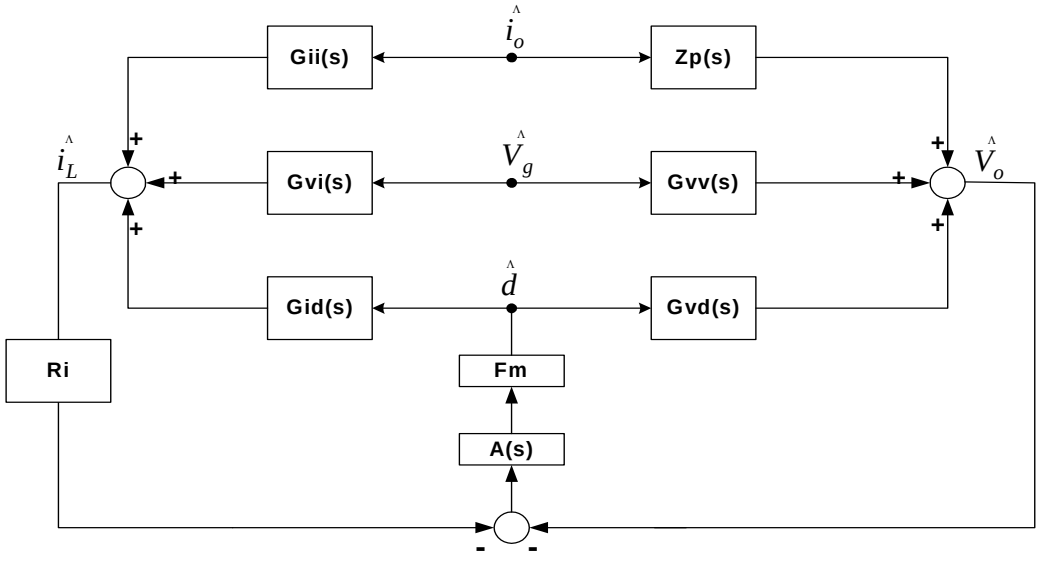


Fig.2.2.9 Small signal blocks of multiphase VR

Small signal model [79-81] is widely used to design the compensator (also called PID control) for stability and transient response optimization. In order to simplify AVP analysis, all the Mosfets and filter inductance in multiphase VR are assumed to be same; R_L contains the Ron of Mosfets and resistance of filter inductors; Lc and Rc are the parasitic parameters of output capacitors. Compensator A(s) for constant output impedance can be obtained through the following steps based on the small signal model of multiphase VR.

$$Z_L(s) = s \cdot L_O / N + R_L / N \tag{2-2-4}$$

$$Z_C(s) = s \cdot L_C + R_C + 1/S \cdot C_O \tag{2-2-5}$$

$$M = \frac{D}{1 + R_L / R_O} \tag{2-2-6}$$

$$G_{id}(s) = \frac{Vin}{Z_L(s) + Z_C(s) // Ro} \tag{2-2-7}$$

$$G_{vd}(s) = \frac{Z_C(s) // Ro}{Z_L(s) + Z_C(s) // Ro} \tag{2-2-8}$$

$$G_{iv}(s) = \frac{M}{Z_L(s) + Z_C(s) // Ro} \tag{2-2-9}$$

$$G_{ii}(s) = \frac{\frac{1}{Z_L(s)}}{\frac{1}{Z_L(s)} + \frac{1}{Z_C(s)} + \frac{1}{Ro}} \tag{2-2-10}$$

$$G_{vv}(s) = \frac{M \cdot (Z_C(s) // Ro)}{Z_L(s) + Z_C(s) // Ro} \tag{2-2-11}$$

$$Zo(s) = \frac{1}{\frac{1}{Z_L(s)} + \frac{1}{Z_C(s)} + \frac{1}{Ro}} \tag{2-2-12}$$

$$T_V(s) = A(s) \cdot F_m \cdot G_{vd} \tag{2-2-13}$$

$$T_i(s) = A(s) \cdot F_m \cdot G_{id} \cdot R_i \tag{2-2-14}$$

$$Z_{OC}(s) = \frac{Zo(s) \cdot (1 + T_i(s)) + T_i(s) \cdot \frac{G_{vd}(s) \cdot G_{ii}(s)}{G_{id}(s)}}{1 + T_i(s) + T_v(s)} \cong R_{droop} \tag{2-2-15}$$

$$A(s) = \omega_i \frac{1 + \frac{s}{\omega_Z}}{s \cdot (1 + \frac{s}{\omega_P})} \tag{2-2-16}$$

The ideal compensator for constant out impedance can be simplified into the applicable compensator [16-20]. As for the design of compensator A(s), one zero ω_Z is placed to compensate for the power stage double pole so that the current loop will be stable with a phase margin of about 90 degrees. A pole ω_P is placed in the high frequency range to filter the

switching noise. It's important to design ω_i large enough so that the current loop has a crossover frequency that is higher than the ESR zero of the output capacitor.

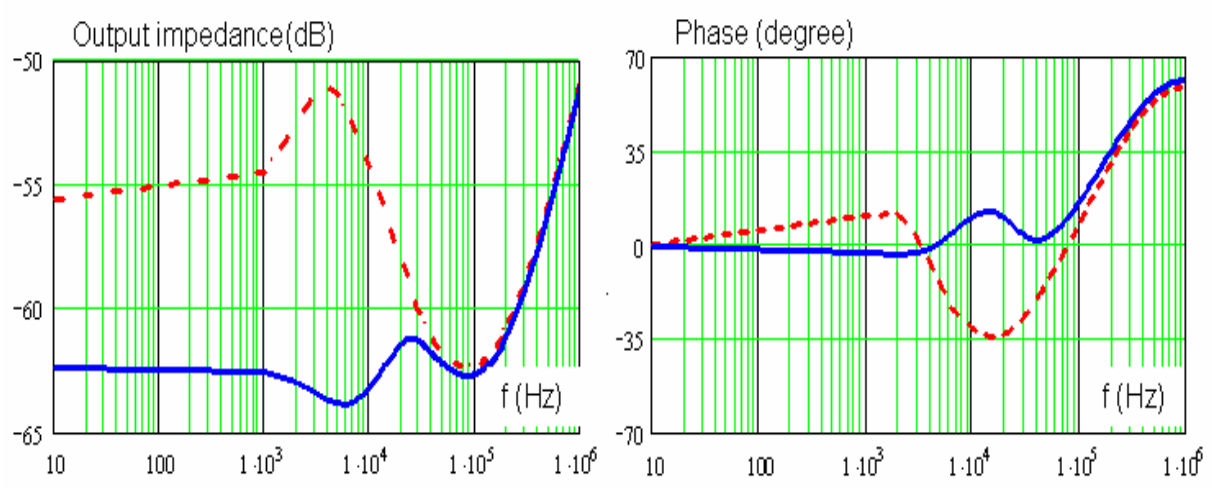


Fig.2.2.10 Output impedance bode plot of a Buck converter

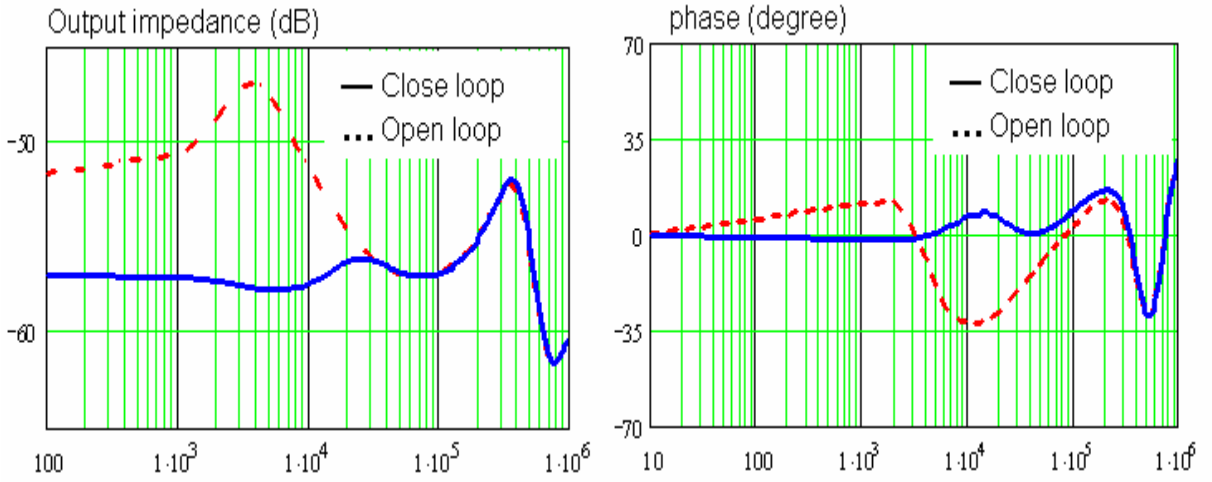


Fig.2.2.11 Socket load line of socket 478

Fig.2.2.10 shows that the 3-Ch VR output impedance and phase curve are almost constant within its 23.5 kHz bandwidth with 9 pieces of Oscons (560μF/4V, 6.4nH ESL, 9.28mΩ ESR), followed by increasing gain and phase due to the influence of the ESL in the Oscon capacitors.

Fig.2.2.11 shows the output impedance of SKT478 PD model for CPU with 3-Ch VR, as shown in Fig.2.1.3. From the load line curve, it is clear that the socket load line is about 1.5mΩ within its 23.5 kHz bandwidth, and also, it is almost flat between 23.5 kHz and 150 kHz because of the combination of different types of capacitors. In high frequency range, the output impedance increases due to the impact of ESL in Oscons.

Fig.2.2.12 shows the output impedance of LGA775 PD model for a processor with 3-Ch VR, as shown in Fig.2.1.5. From the analysis, the socket load line of N2 is about 1mΩ within its 23.5 kHz bandwidth, and it also has almost constant load line between 23.5 kHz and 400 kHz, which is much better than that in the SKT478.

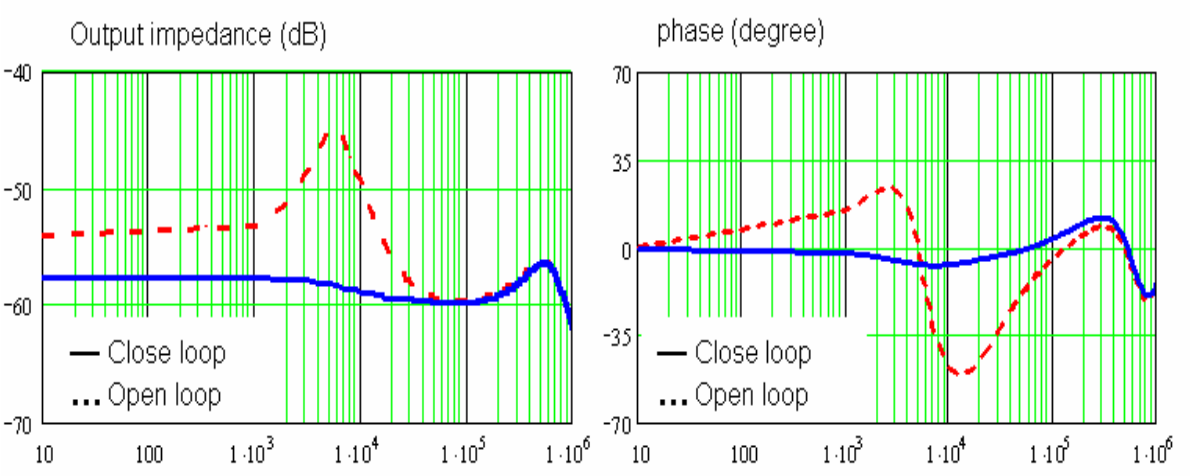


Fig.2.2.12 Socket load line of point N2 in LGA775

If the socket load line is required to be reduced to 1mΩ for socket 478 or 0.7mΩ for LGA775, the VR bandwidth has to be pushed to 500 kHz; thus, the switching frequency should be several MHZ leading to incredible switching loss in the main VR. Therefore, high switching frequency operation in conventional main VR to improve transient response with high bandwidth is not a good solution.

2.2.3 Limitations of Existing Control Methods

The controller designs discussed above are all based on the small signal model [79-81], which cannot describe the large signal transient response very well. Large signal response is mainly limited by filter inductance, dv/dt of error amplifier (EA) and delay time of EA compensation network. The delay time of linear compensation network cannot be eliminated because of the requirement of enough gain and phase margins for converter stability.

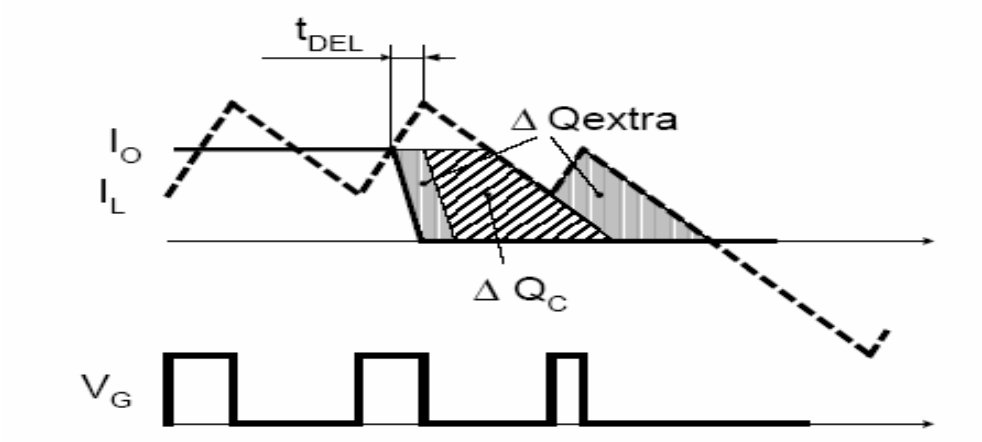


Fig.2.2.13 Impact of delay time in controller on transient

The impact of delay time in actual controller impact on transient is shown in Fig.2.2.13. The capacitive portion of the output voltage V_C gets the additional rise ΔV_C because the charge ΔQ_C is delivered to the output capacitor C_O via the filter inductor L_O. The delay time t_{DEL} in any actual controller adds the extra charge ΔQ_{EXTRA}. This additional charge increases the second voltage spike by,

$$\Delta V_O = \Delta Q_{EXTRA} / C_O = I_{avg} \cdot t_{DEL} / C_O \qquad (2\text{-}2\text{-}17)$$

Usually the current VR controller needs to complete the transient response within at least 2 μs to be ready for the next transient. The limitation of existing control methods at high slew

rate VR is the delay time in any actual control, which can be optimized by increasing the unity gain bandwidth, but it cannot eliminate due to the gain and phase margins for converter stability, which increase the delay time and transient response time.

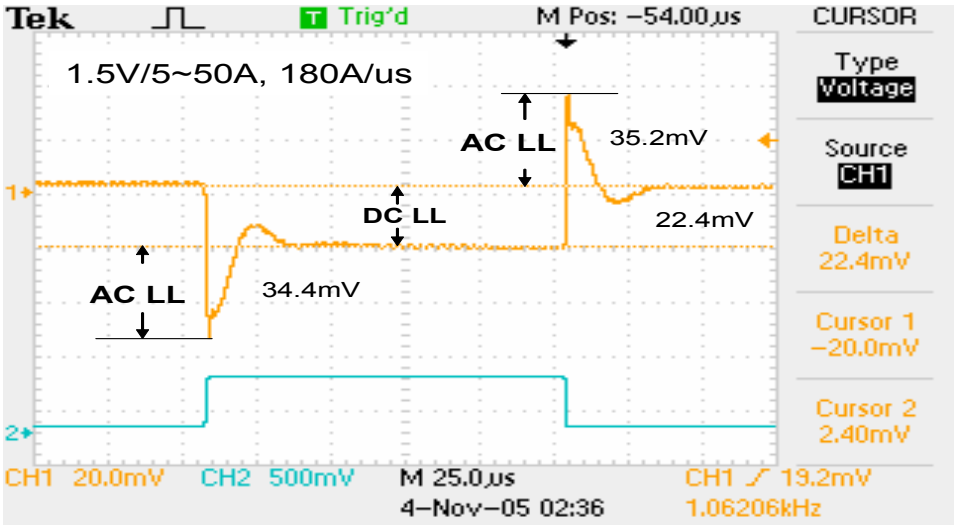


Fig.2.2.14 VR transient waveform at 180A/µs

Fig.2.2.14 shows the tested Intersil Eval ISL6306 transient results @ 1.5Vo/5~50A, 180A/µs, and it is clear that the second voltage spike dominates due to the delay time in the actual controller and large filter inductance for small current ripple. The AC load line is also higher than the DC load line under 800A/µs transient load in most VR designs, so reducing the delay time by optimizing the compensation network to fast transient response or smaller load line is the big challenge in VR design.

All of the linear control methods discussed above have a limitation — delay times for converter stability, and it is impossible to eliminate them. In Chapter 3, combined linear and adaptive nonlinear has been proposed to reduce the delay time and simplify linear controller design, leading to fast transient response.

2.3 Existing Active Topology Methods and Limitations

As discussed in Chapter 1, the basic reason for transient voltage spikes at high slew rate load is low slew rate VR current, and the delay times in actual control deteriorate them. The previous section discussed the existing control methods for fast transient response. This section mainly focuses on the discussion of the existing active topology methods to increase the VR current slew rate by reducing the filter inductance, including coupled inductor [41] [47-50], two-stage approach [64] and active current compensators [37-40] [43-45].

2.3.1 Coupled Inductor in VR

A small inductor allows higher VR current slew rate to improve the transient response. However, small inductor values lead to large ripple current that increases the conduction loss and output capacitor requirement. The multiphase interleaved design avoids this problem because it achieves substantial ripple current cancellation in the output capacitor. This allows smaller inductance without requiring a large output capacitor. However, large current ripples flow through each channel, resulting in higher conduction losses, magnetic losses and higher peak current requirements.

High switching frequency operation is used to reduce the filter inductance and ripple current but it increases the switching and driving losses. Stepping inductance [41] has large filter inductance for small current ripple in steady state. Only small leakage inductance is in transient for high slew rate by the activation of an extra circuit, but large conduction losses in an extra activated circuit are the barriers for applications.

Partial coupled inductor or applying transformer concept to VR has been discussed in the literatures [47-49]. The fully coupled inductor [50] largely reduces the output current ripple and improves the transient response. Fig.2.3.1 shows a two-phase interleaved converter with leakage inductances L1 and L2, an ideal transformer and a single magnetizing inductance L_M.

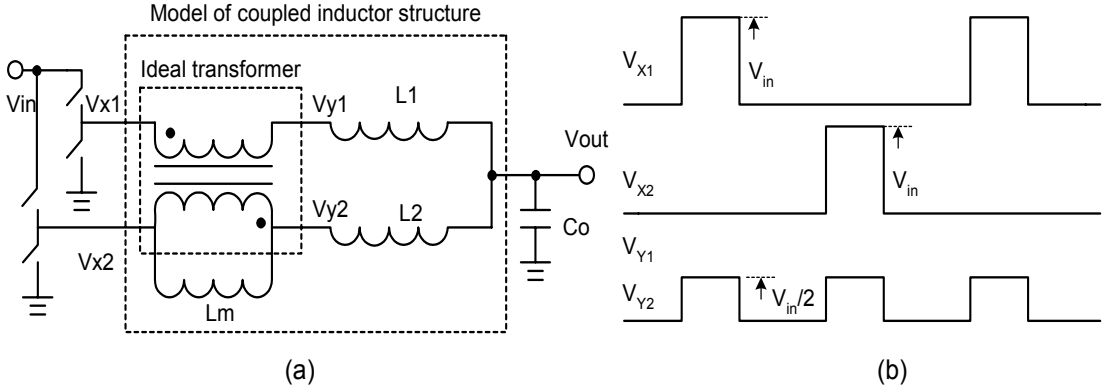


Fig.2.3.1 Fully coupled inductor in VR: (a) two channel VR with coupled inductor, and (b) coupled inductor operation principle

The ideal transformer forces the AC current in two channels to be equal, thus the AC current in two leakage inductance, L1 and L2, are also equal. Fig.2.3.1 (b) shows the operation principle of the fully coupled inductor concept. The voltage labeled Vy1 and Vy2 doubles the switching frequency with half of input voltage Vin, thus it significantly reduces the current ripple in two channels. With the effective duty cycle and the effective frequency doubled, the ratio of ripple current with fully coupling to ripple current without coupling is obtained:

$$\frac{I_{PP,coup}}{I_{PP,uncoup}} = \frac{0.5 - D}{1 - D} \tag{2-3-1}$$

The above equation shows that fully coupled inductor can reduce the current ripple for small magnetic conduction losses with same inductance in each channel, or it requires smaller

inductance and therefore it has fast transient response with the same current ripple in output capacitors. Custom magnetic core shape is required in multiphase VR applications.

2.3.2 Two-Stage Approach

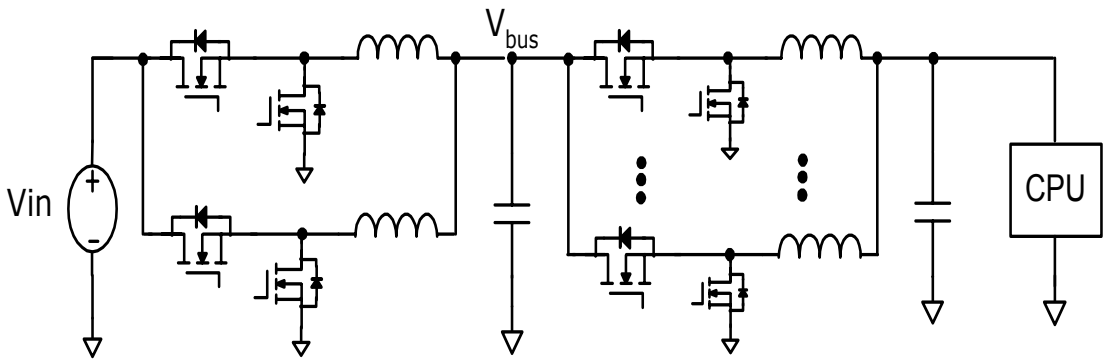


Fig.2.3.2 Two-stage approach

Fig.2.3.2 shows the two-stage approach [64]. The first stage contains 2-Ch interleaved VR operating at 500 kHz with 1.6μHz filter inductance and 30V rating MOSFET. It has a large operating duty cycle and its output voltage is 5V bus; 4-Ch interleaved VR in second stage converter operates in several MHZ with good performance 12V lateral MOSFET and 100nH per phase. It achieves around 320 kHz bandwidth that results in good transient response, and also the two-stage approach achieves higher efficiency than conventional main VR in several MHZ operation. Unfortunately, the two-stage approach is a cascade converter, and improving its total efficiency is the main challenge.

2.4 Existing Active Transient Current Compensator

Fig.2.4.1 shows that the settling time of the actual controller is within at least 2μs and the AC voltage spikes are less than 100mV both in step-up and step-down load in VR10.1 specifications. The second voltage spike contains the DC part determined by AVP design and the AC part related to the energy stored in filter inductors, and the delay times in the actual controller greatly increase the second voltage spike. The power in transient needed to compensate the voltage spike in transient only accounts for 10 percent~20 percent of the total power, and it is a very attractive way to improve transient response by an extra converter to compensate transient power for constant output voltage. Fig.2.4.2 (a) shows a current compensation concept to compensate the second voltage spike by injecting a current source. The extra converter injects the unbalanced current between VR current and load current in step-up load, and absorbs energy in step-down load. There are two implementation circuits: linear mode current compensator [39-40] and switching mode current compensator [37-38] [43-45].

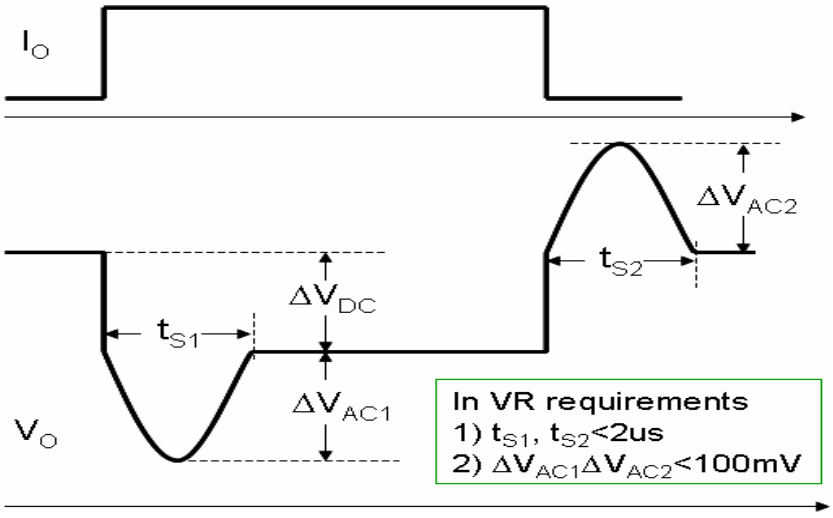
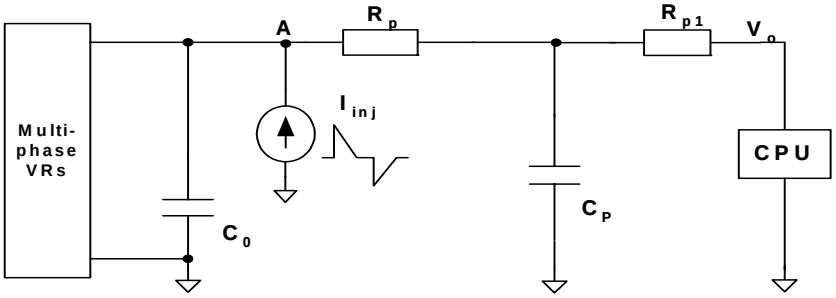
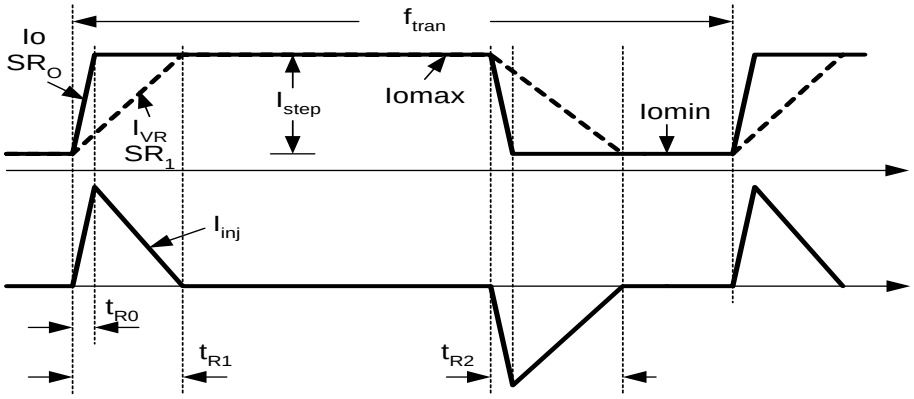


Fig.2.4.1 Transient response waveforms at high slew rate load

Current compensation is used to reduce second voltage spike by an extra converter only engaged in transient periods. It injects the unbalanced current between VR and load current in step-up load and dissipates or recovers extra energy in step-down load by linear mode or switching mode. Linear mode current compensator in Fig.2.4.3 regulates the injected and dissipated energy in linear mode. Switching mode current compensator in Fig.2.4.4 is used to reduce the conduction loss, but it introduces high switching loss. The main VR determines the DC load line and current compensators determine the AC load line, thus main VR can be optimized for better efficiency via switching frequency and filter inductance.



(a)



(b)

Fig.2.4.2 Current compensator concept: (a) simplified current compensator concept, and (b) injected current waveforms of current compensator

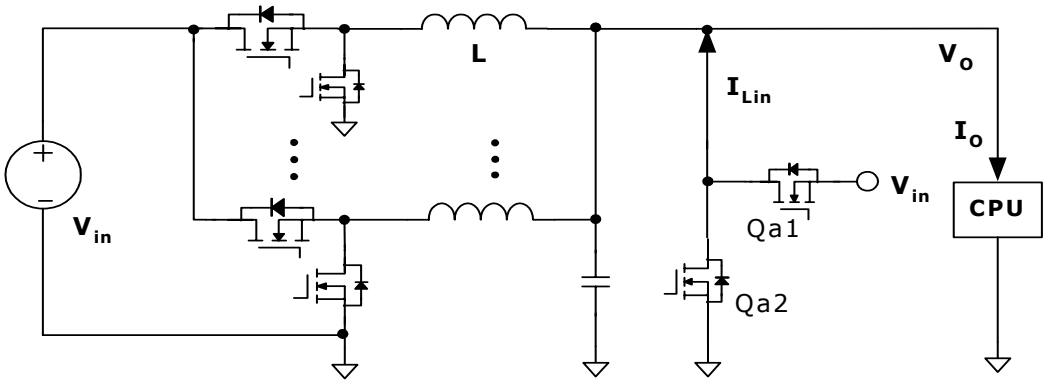


Fig.2.4.3 Linear mode current compensator topology

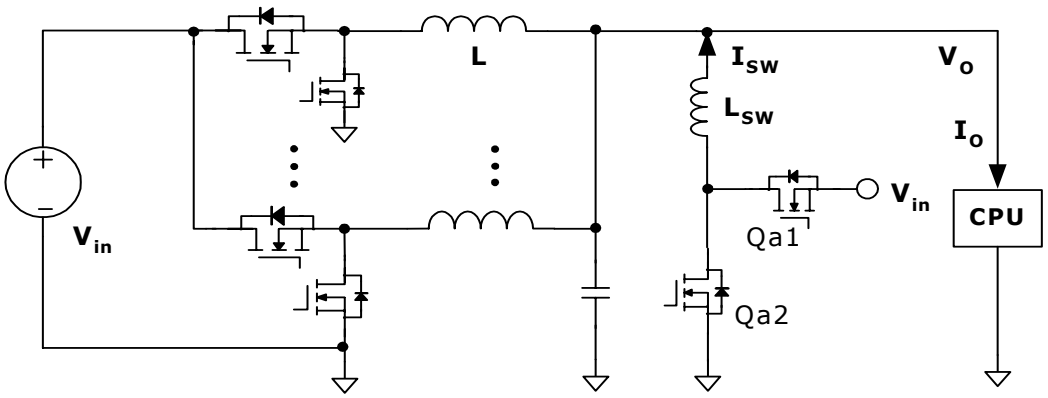


Fig.2.4.4 Switching mode current compensator topology

An extra converter provides most of the unbalanced current, thus linear mode current compensator has large conduction loss due to large voltage drop and current stresses, and the switching mode compensator has small conduction loss but high switching loss.

The injected current waveforms for power loss calculation are as shown in Fig.2.4.2 (b) when the transient load frequency meets $t_{R1} + t_{R2} \le 1/f_{tran}$, and beyond this frequency the extra converter will provide energy to load continuous.

$$T_{RO} = \frac{\Delta I_{step}}{SR_O} \tag{2-4-1}$$

$$T_{R1} = \frac{V_{in} - V_O}{L/N} \tag{2-4-2}$$

$$T_{R2} = \frac{V_O}{L/N} \tag{2-4-3}$$

$$P_{UP} = (V_{in} - V_O) \cdot [\frac{\Delta I_{step}}{2} \cdot (T_{R1} - T_{R0}) \cdot f_{tran}] \tag{2-4-4}$$

$$P_{DWN} = V_O \cdot [\frac{\Delta I_{step}}{2} \cdot (T_{R2} - T_{R0}) \cdot f_{tran}] \tag{2-4-5}$$

$$P_{Linear} = P_{UP} + P_{DWN} \tag{2-4-6}$$

For switching mode current compensator, the power loss contains conduction and switching losses, driving losses of Q_{a1} and Q_{a2}, power loss of filter inductor L_{SW} and the body diode conduction loss of Q_{a2} according to the waveforms in Fig.2.4.2 (b).

$$P_{Q1} = f_{tran} \cdot (t_{R1} - t_{R0}) \cdot R_{on} \cdot \Delta I_{step}^2 \cdot \frac{D}{3} + t_{R1} \cdot f_{tran} \cdot (0.5 \cdot C_{OSS} \cdot V_1^2 \cdot f_S + Q_g \cdot V_g \cdot f_S) \tag{2-4-7}$$

$$P_{Q2} = f_{tran} \cdot (t_{R2} - t_{R0}) \cdot R_{on} \cdot \Delta I_{step}^2 \cdot \frac{1-D}{3} + t_{R2} \cdot f_{tran} \cdot f_S \cdot (Q_g \cdot V_g + V_F \cdot t_b \cdot \frac{\Delta I_{step}}{2}) \tag{2-4-8}$$

$$P_L = f_{tran} \cdot (\int_{t_{R1}+t_{R2}} i_{inj}^2 \cdot R_{LM} \cdot dt + \int_{t_{R1}+t_{R2}} P_{ac} \cdot dt) \tag{2-4-9}$$

$$P_{SW} = P_{Q1} + P_{Q2} + P_L \tag{2-4-10}$$

Where, V_F, t_b, V_g, P_{ac} are voltage drop of body diode of Q_{a2}, conduction time of body diode of Q_{a2}, driving voltage and magnetic power loss, respectively. D=Vo/Vin.

Fig.2.4.5 shows the power loss calculation plots of linear and switching mode current compensators. For linear mode current compensator, it has about 8.6W power loss and about 14W power loss for switching mode current compensator @ 1.1V/100A, f_{tran}=2 kHz and 12V

input for current compensator. Lower input voltage for current compensators helps to reduce lower power loss at the cost of their performances.

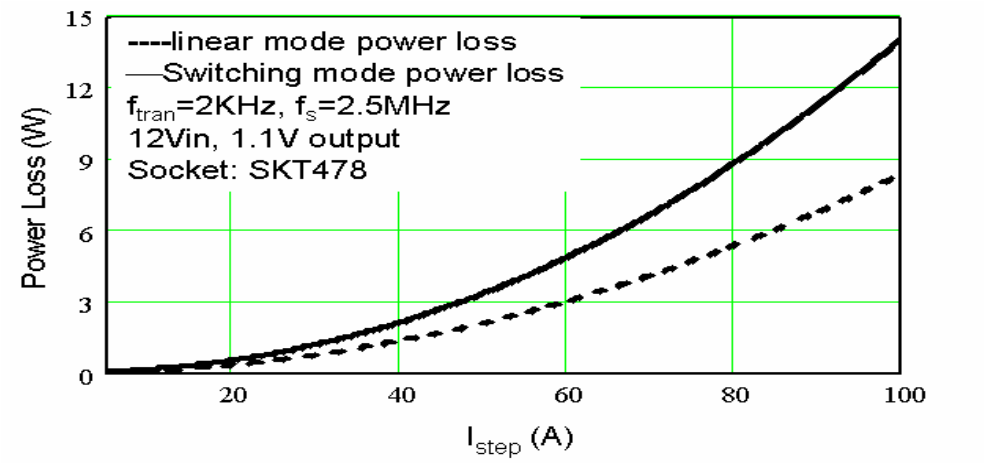


Fig.2.4.5 Power loss estimation of current compensators

The limitation of current compensator is the high conduction loss in linear mode current compensator and high switching loss in the switching mode current compensator. The low efficiency in the extra converter makes it difficult to apply low voltage high current VR.

2.5 Summary

Interleaved multiphase VR is commonly used in desktop and laptop computer systems to power the microprocessor because of small input and output ripples and good distributed thermal capability. In high slew rate transient, main VR current slew rate cannot catch up with the load current slew rate, and then the unbalanced current is provided by bulk and ceramic capacitors. The first voltage spike is mainly determined by ESR and ESL of capacitors. The effective way to reduce the first voltage spikes is to reduce ESR and ESL by paralleling more capacitors. But this

way is always limited by available motherboard space and parasitic resistance and inductance of PCB traces and socket, which is problematic in higher slew rate applications.

The second voltage is determined by the energy stored in filter inductors related to the unity gain bandwidth. The delay time in linear controller can minimize for fast transient response by increasing the unity-gain bandwidth. But it is impossible to get rid of those delay times in the actual controller due to the required gain and phase margins for converter stability.

AVP concept increases the output tolerance as much as twofold and achieves constant output impedance within the close loop bandwidth. In most actual cases, the AC load line is higher than the DC load line due to the delay times in linear controller. The small signal model is not suitable in large signal response design, which is determined by VR filter inductance and EA dv/dt. A novel control is proposed in Chapter 3 for large signal transient.

Another way to improve the transient response is to reduce the equivalent filter inductance for smaller LC delay time. High switching frequency operation leads to small filter inductance, which benefits the high current slew rate and unity-gain bandwidth but deteriorates the efficiency. The two-stage approach utilizes the first stage to generate 5V intermediate bus, and the second stage operates in several MHZ with very small filter inductance with better FOM lateral MOSFETs, and it can improve the second stage efficiency and its bandwidth. However, the two-stage approach is a cascade system thus efficiency improvement is the big challenge.

Current compensation concept is very attractive to improve the transient response by an extra converter, which only injects high slew rate current in step-up load and dissipating energy in linear mode or recovering energy in switching mode current compensators in step-down load. Current compensators only handle the AC current in transient, and main VR handles the DC current; thus, main VR can be optimized for better efficiency. But high conduction loss occurs in

linear mode current compensator due to high voltage drop and high current stresses and high switching loss in switching mode current compensator due to high switching frequency and high current stresses. Low efficiency makes them difficult to apply in low voltage high current VR.

This work focuses on how to improve the VR transient response with high efficiency at high slew rate transient loads, which has following requirements:

1) Novel control method to reduce the delay times in linear controller;

2) High switching frequency operation for higher achievable bandwidth;

3) Minimized extra power loss increase for improved transient response;

4) Simple and easy to implement.

CHAPTER THREE: ACTIVE TRANSIENT VOLTAGE COMPENSATOR

As we know, the VR equivalent inductance determines output current slew rate and transient response. In high slew rate transient load, the first voltage spike is mainly related to the ESR and ESL of capacitors; the second voltage spike is determined by the energy stored in filter inductor. The delay times in VR controller increase the second voltage spike [33, 34].

Faster transient response requires lower output impedance or load line. Constant output impedance is required by Intel [3-6] to reduce the CPU power loss at heavy load. If the VR DC load line is equal to the AC load line, then there will be no voltage spike at any slew rate transient. Constant output impedance may be achieved by active voltage position or active droop compensation methods [17-19].

Using a large number of capacitors in parallel to reduce its ESR and ESL for lower voltage spike is constrained by the available space on the motherboard, and it also has the limitation due to the resistance and inductance of PCB traces and socket. Therefore, this is not a suitable solution for the future higher slew rate requirements.

In a two-stage approach [64], the first stage operates at relatively low frequency for 5V intermediate bus voltage, and the second stage operates in several MHZ with small filter inductance and achieves several hundred kHz close loop bandwidth. All the output filter capacitors are ceramic capacitors due to high frequency operation. Better FOM lateral Mosfets are used in second stage to improve the efficiency in the second stage converter. But a two-stage approach is a cascade system, and improving total efficiency is the main issue.

Conventional current compensators with an extra converter injecting high slew rate current in step-up and recovering energy in switching mode or dissipating energy in linear mode

in step-down load and only activates in transients to handle the AC current. Main VR provides the DC current, but low efficiency is in the extra converter due to the high current stresses.

The main topic in this chapter is how to improve the VR transient response with high efficiency. One proposed concept, active transient voltage compensator, is given in this chapter.

3.1 Proposed Concept of Active Transient Voltage Compensator

Active transient voltage compensator concept (ATVC) is proposed to improve the AC load line by the injecting voltage source instead of current source in conventional current compensators. With the introduction of a transformer in active transient voltage compensator, ATVC reduces the conduction and switching losses obviously, and it also largely increases the injected transient slew rate current compared with conventional current compensators. At the same time, the main VR can achieve better efficiency by optimizing the switching frequency and filter inductance, because it mainly needs to handle the DC current.

3.1.1 Concept of Active Transient Voltage Compensator

Active transient voltage compensator has two implementation options: series ATVC in Fig.3.1.1 and parallel ATVC in Fig.3.1.2. In order to simplify ATVC operation analysis, the main VR is assumed as a current source with output capacitor C_O; C_P is the decoupling capacitors for CPU; R_P is the lumped impedance of PCB traces between C_O and C_P; R_{P1} is the lumped impedance of PCB traces and socket between C_P and CPU and R_{inj} is the equivalent internal impedance of ATVC. Both of them can improve the AC load line with the same operating principle.

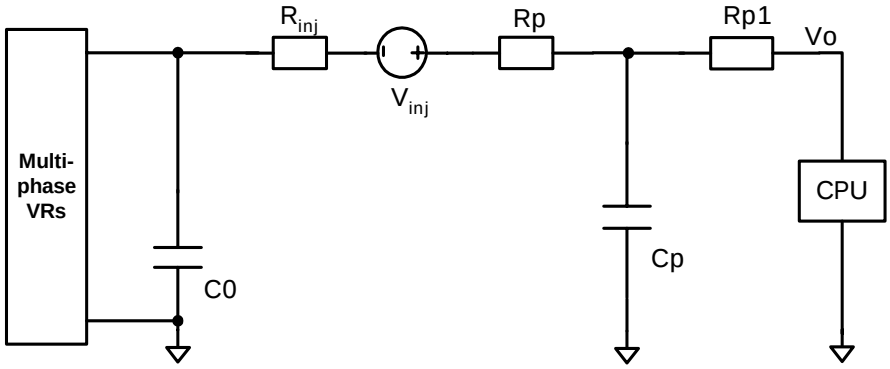


Fig.3.1.1 Concept of series ATVC

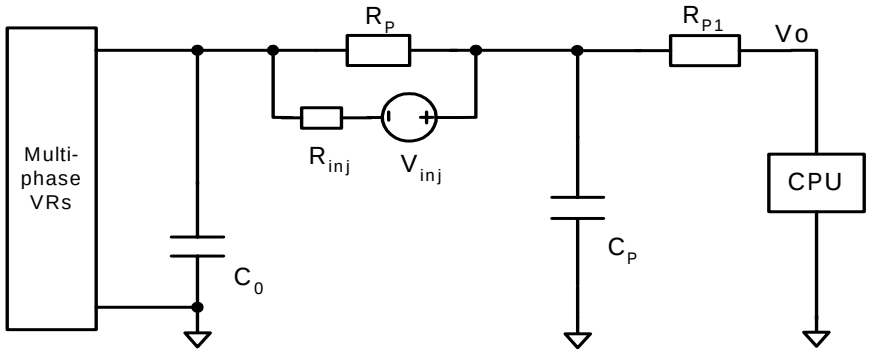


Fig.3.1.2 Concept of parallel ATVC

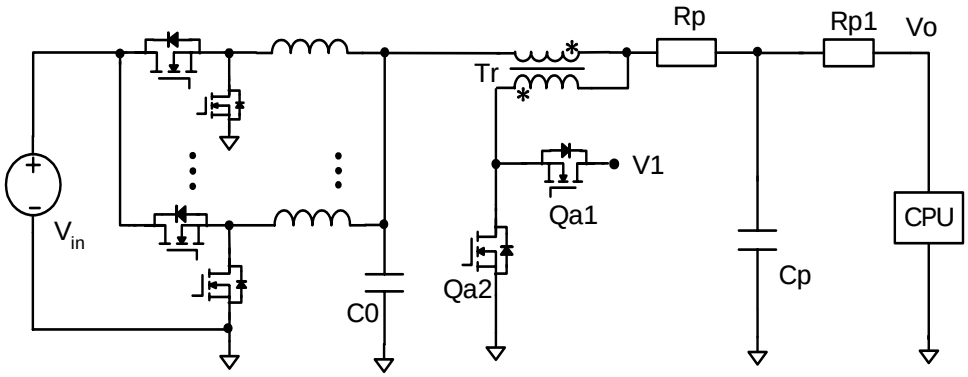


Fig.3.1.3 Series ATVC implementation circuit

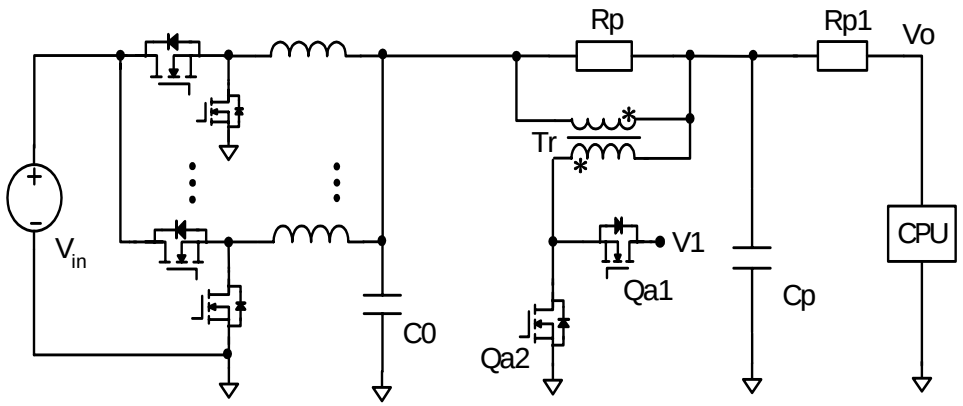


Fig.3.1.4 Parallel ATVC implementation circuit

Series ATVC as shown in Fig.3.1.1 is in series with R_P and carries all the unbalanced current between the load current and the VR current. Thus, it increases the conduction loss in steady state, and it also increases the VR DC load line by R_{inj}.

Parallel ATVC as shown in Fig.3.1.2 is in parallel with R_P and only carries a portion of the unbalanced current that is divided by R_P and R_{LM}, leading to smaller conduction and switching losses. Moreover, parallel ATVC reduces the DC load line by paralleling R_p with R_{inj} in steady state.

ATVC is composed of two switches Qa1, Qa2 and one transformer Tr. The ATVC input voltage V_1 can be any available voltage source. Fig.3.1.3 shows the parallel ATVC implementation circuit that is in parallel with R_P in the output terminal of the multiphase VR. Fig.3.1.4 shows the series ATVC implementation circuit that is in series with R_P in the output terminal of the multiphase VR.

The voltage source is injected by ATVC transformer and filtered by the transformer leakage inductance together with parasitic inductance of PCB traces and socket. ATVC transformer with N: 1 turn ratio is composed of the primary leakage inductor L_{LK2}, secondary

leakage inductor L_{LK1}, the magnetizing inductor L_{LM} and resistance R_{LM} in secondary side. Without specific notices, ATVC is used for the second voltage spike suppression, not for the first spike.

3.1.2 ATVC Operation Analysis

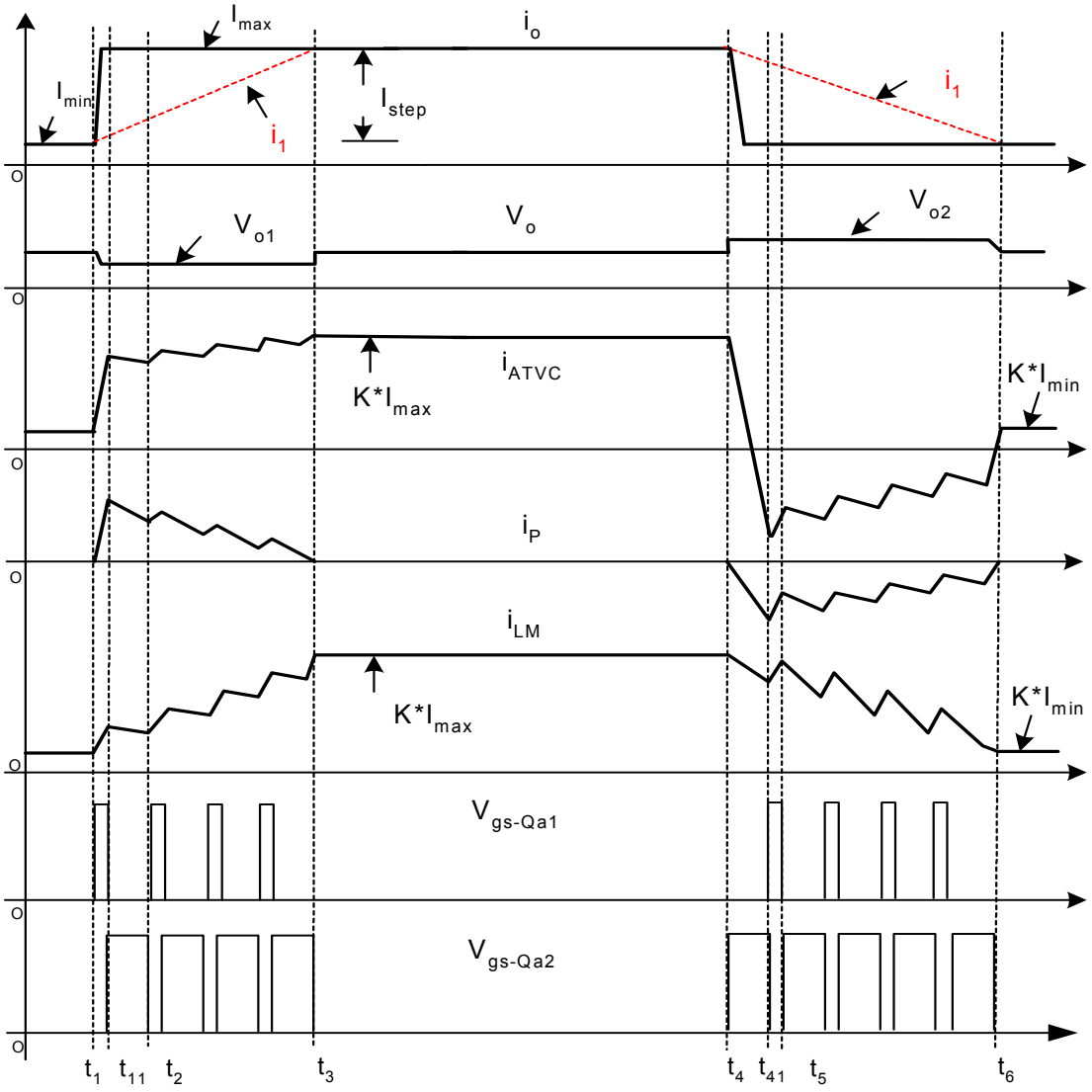
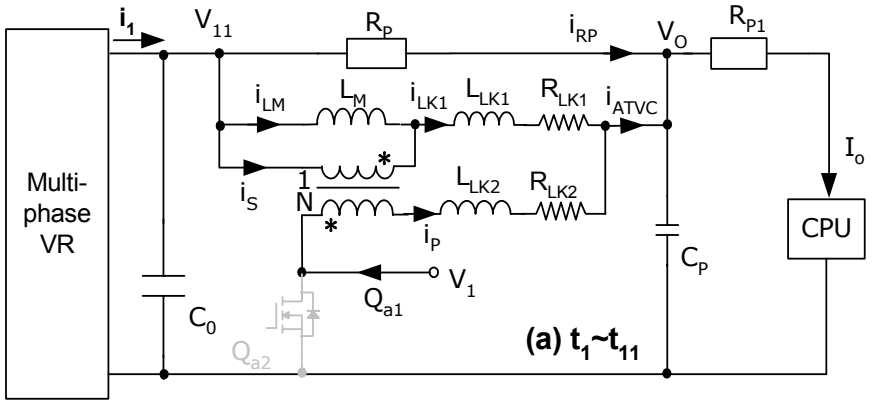
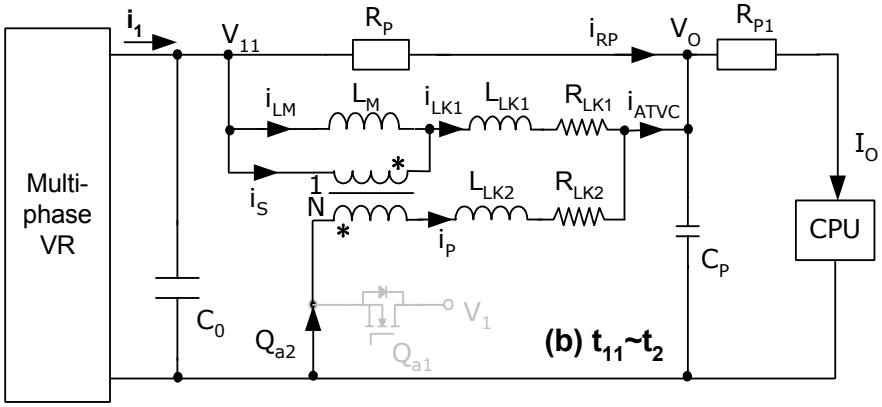


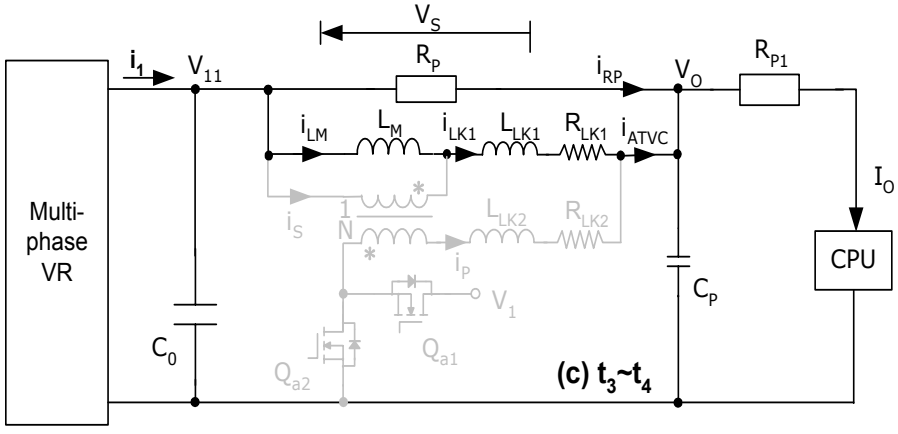
Fig.3.1.5 Operation waveforms of Parallel ATVC



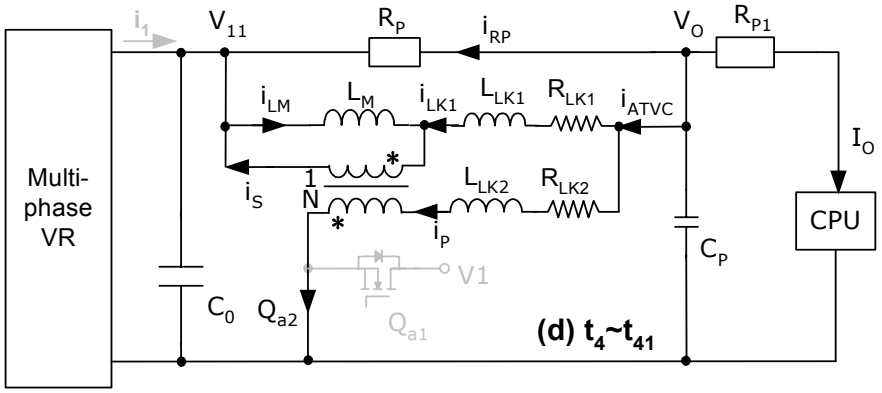
a) Current injection: t_1~t_{11} in step-up load mode



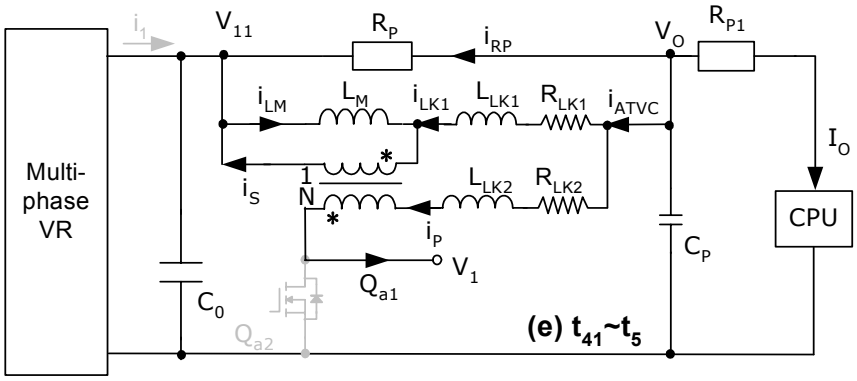
b) Current injection: t_{11}~t_2 in step-up load mode



c) Steady state mode t_3~t_4



d) Energy recovery: t_4~t_{41} in step-down load mode



e) Energy recovery: t_{41}~t_5 in step-down load mode

Fig.3.1.6 Parallel ATVC operation mode analysis

Here, only parallel ATVC is explained as an example. According to the operation waveforms of parallel ATVC, there are three main operation modes: current injection mode (t_1~t_3) in step-up load, steady-state mode (t_3~t_4) and energy recovery mode (t_4~t_6) in step-down load as shown in Fig.3.1.6.

Fig.3.16 (a) and (b) show the step-up load from I_{min} to I_{max}, the output voltage starts to drop when VR current cannot keep up with the output current and the capacitor Co provides the energy. Once the output voltage is lower than the reference voltage in ATVC step-up controller in Fig.3.4.17, ATVC will activate just as a buck converter by controlling Qa1 When Qa1 is on,

high slew rate current is injected into the load. When Qa1 is off, the current freewheels through the body diode of Qa2 or Qa2 in synchronous mode to reduce the conduction loss. In order to keep ATVC in off mode in steady state, the reference voltage in ATVC step-up controller is a little bit lower than VR output voltage, such as 10~15mV less. ATVC keeps injecting high slew rate current until VR provides the total output current $I_{max.}$ Because of small leakage inductance, ATVC current can quickly catch up with output current leading to second voltage spike suppression. Equations (3-1-1)-(3-1-4) govern this stage of operation.

$$\frac{di_{LK2}}{dt} = \frac{V1 - Vo}{N^2 \cdot L_{LK1} + L_{LK2}} \tag{3-1-1}$$

$$\frac{di_{ATVC}}{dt} = (1+N) \cdot \frac{di_{LK2}}{dt} + \frac{di_{LM}}{dt} \tag{3-1-2}$$

$$I_{ATVC} = (1+N) \cdot I_{LK2} + i_{LM} \tag{3-1-3}$$

$$t_{13} = \frac{L_{LM} \cdot K \cdot I_{step}}{V11 - Vo1} \tag{3-1-4}$$

$$K = \frac{R_P}{R_P + R_{LM}} \tag{3-1-5}$$

At the time t_3, magnetizing current I_{LM} reaches $K \cdot I_{\max}$. With the introduction of a transformer, ATVC only needs to handle lower current $K \cdot I_{step} / (1+N)$, thus it largely reduces the conduction and switching losses. Also, it provides the current slew rate (1+N) times higher than that in current compensator based on the same filter inductance.

In steady state mode in Fig.3.1.6 (c), both Q_{a1} and Q_{a2} are in off state and the body diode of Qa2 has to remain in the block state when it meets the following condition,

$$N \cdot V_S < Vo + V_D \tag{3-1-6}$$

Where Vs is the secondary transformer voltage drop, V_D is the on-state voltage drop of the body diode of Qa2. In fact, the voltage drop across R_P in steady state is only several mV, which is very easy to meet the Equation (3-1-6).

Fig.3.1.6 (d) and (e) show the step-down load from I_{max} to I_{min}, and ATVC is activated as a boost converter by controlling Qa2 when the output voltage is higher than the reference voltage in ATVC step-down controller in Fig.3.4.17. The current I_{ATVC} changes from positive to negative current and then recovers extra energy. The reference in ATVC step-down controller has 10~15mV higher than VR output voltage. ATVC keeps energy recovery into V_1 until VR current decreases to I_{min}. Equations in this energy recovery stage are as follows:

$$\frac{di_{LK2}}{dt} = \frac{Vo}{N^2 \cdot L_{LK1} + L_{LK2}} \tag{3-1-7}$$

$$\frac{di_{ATVC}}{dt} = (1+N) \cdot \frac{di_{LK2}}{dt} + \frac{di_{LM}}{dt} \tag{3-1-8}$$

$$I_{ATVC} = (1+N) \cdot I_{LK2} + i_{LM} \tag{3-1-9}$$

$$t_{45} = \frac{L_{LM} \cdot K \cdot I_{step}}{Vo2 - V11} \tag{3-1-10}$$

At the time t_6, the magnetizing current I_{LM} decreases to $K \cdot I_{\min}$. In this mode, I_{ATVC} changes from a positive to a negative value allowing the extra energy stored in VR filter inductors to be recovered into the ATVC input voltage V_1.

ATVC injects high slew rate current in step-up load and recycles extra energy stored in VR filter inductors into its input voltage V_1. The reduced current stress with the introduction of a transformer leads to high ATVC efficiency. At the same time, main VR can achieve better efficiency by optimizing the switching frequency and filter inductance.

Table 3.1.1 shows the current slew rate comparison among three different cases. It is clear that ATVC injects higher current slew rate both in step-up and step-down load. Higher slew rate current in ATVC is injected in step-up load rather than in step-down load because of the different applied voltage both in step-up and step-down load.

Table 3.1.1 Current slew rate comparison

a). 3 Ch VR, 12Vin, 1Vo, L_f=0.45uH, fs=300kHz b). 3 Ch VR, 12Vin, 1Vo, L_f=0.1uH, fs=1.5MHz c). VR same as (a), ATVC: V1=5V, N=2,fs=1.5MHz, L_{LK}=25nH		
Current slew rate Comparison		
	Step-up load	Step-down load
a)	0.073A/ns (VR)	0.0067A/ns (VR)
b)	0.33A/ns (VR)	0.03A/ns (VR)
c)	0.073A/ns (VR) 0.48A/ns (ATVC)	0.0067A/ns (VR) 0.12A/ns (ATVC)

3.1.3 ATVC Power Loss Estimation

ATVC power loss estimation is the main topic in this section, which is similar to the power loss estimation previously discussed in switching mode current compensators.

Series ATVC in socket 478 PD model as shown in Fig.1.3.1, handles the total unbalanced current between main VR and load current. The power losses can be obtained through the following equations when the transient load frequency f_{tran} is less than $1/(t_{R1}+t_{R2})$.

$$D_{tran} = f_{tran} \cdot (t_{R1} + t_{R2}) \tag{3-1-11}$$

$$P_{SW-S} = D_{tran} \cdot [R_{on} \cdot \frac{\Delta I_{step}^2}{3 \cdot (1+N)^2} + f_S \cdot (\frac{C_{OSS} \cdot V_1^2}{2} + 2 \cdot Q_g \cdot V_g + V_F \cdot t_b \cdot \frac{\Delta I_{step}}{2 \cdot (1+N)})] \tag{3-1-12}$$

$$P_{Tr-S-ac} = D_{tran} \cdot (R_{LM} \cdot \frac{N^2 \cdot \Delta I_{step}^2}{3 \cdot (1+N)^2} + P_{ac}) \quad (3\text{-}1\text{-}13)$$

$$P_{Tr-S-dc} = R_{LM} \cdot I_o^2 \quad (3\text{-}1\text{-}14)$$

$$P_{S-478} = P_{SW-S} + P_{Tr-S-ac} + P_{Tr-S-dc} \quad (3\text{-}1\text{-}15)$$

For parallel ATVC in socket 478, it handles a portion of unbalanced current, which is divided by R_P and R_{LM}.

$$P_{P-478} = P_{S-478}(K \cdot \Delta I_{step}) \quad (3\text{-}1\text{-}16)$$

In LGA775, ATVC can locate both on the north side and on the east side. The current on the north side VR is two-thirds of the load current, and the current on the east side VR is only one-third of the load current, thus different locations mean different power losses in ATVC.

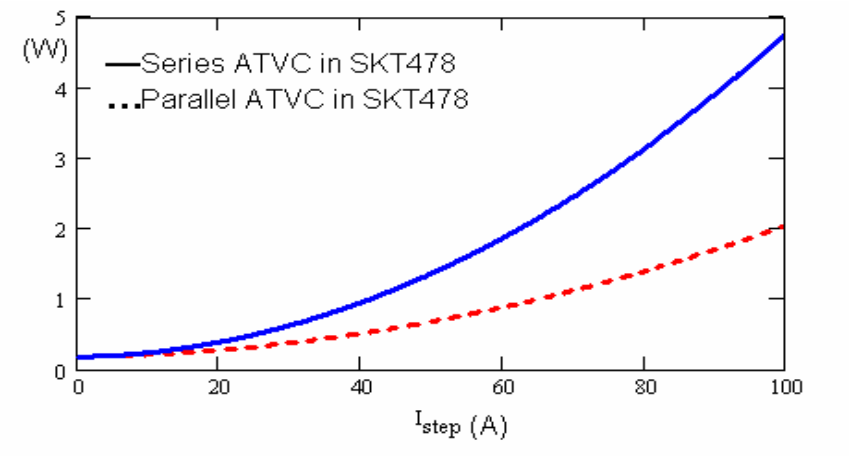
The series ATVC and parallel ATVC power loss estimations in LGA775 are as follows when the transient load frequency f_{tran} is less than $1/(t_{R1}+t_{R2})$.

$$P_{S-775-north} = P_{S-478}(\frac{2}{3} \cdot \Delta I_{step}) \quad (3\text{-}1\text{-}17)$$

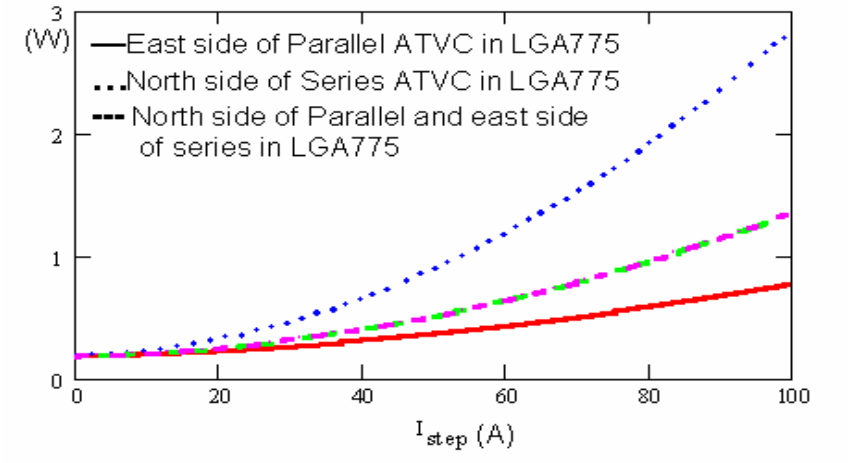
$$P_{P-775-north} = P_{S-478}(\frac{2}{3} \cdot K \cdot \Delta I_{step}) \quad (3\text{-}1\text{-}18)$$

$$P_{S-775-east} = P_{S-478}(\frac{1}{3} \cdot \Delta I_{step}) \quad (3\text{-}1\text{-}19)$$

$$P_{P-775-east} = P_{S-478}(\frac{1}{3} \cdot K \cdot \Delta I_{step}) \quad (3\text{-}1\text{-}20)$$



(a)



(b)

Fig.3.1.7 ATVC power loss estimations: (a) ATVC power loss estimation in socket 478 with K=0.5 and (b) ATVC power loss estimation in LGA775 with K=0.5

From the above analysis, it is clear that ATVC conduction is mainly determined by transformer design. Thus, a different ATVC transformer turn ratio has different ATVC power loss. Fig.3.1.7 (a) shows that parallel ATVC with k=0.5 has about 2W @t 1.1V/100A, f_{tran}=2 kHz and 4.8W in series ATVC in SKT478 PD model based on the 3-Ch main VR in 250 kHz

with 0.45μH filter inductance and 1.1V output voltage, and ATVC at 1.5MHZ with 4:1 transformer.

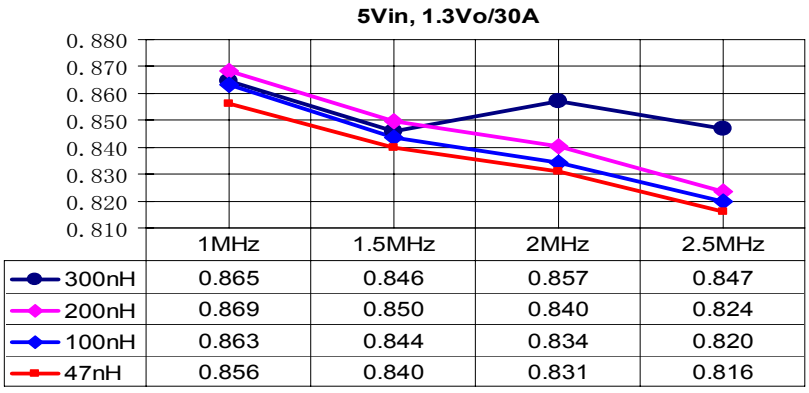
Fig.3.1.7 (b) shows the ATVC power loss estimation in LGA775 PD mode. Parallel ATVC with K=0.5 on the east side VR has less than 1W at 1.1V/100V, f_{tran}=2 kHz, while the series ATVC on the north side has around 2.9W. K mainly depends on the transformer design and resistance of PCB traces.

When the transient load frequency f_{tran} is higher than $1/(t_{R1}+t_{R2})$, ATVC will provide continuous energy leading to the worst case for power loss. The settling time of $t_{R1}+t_{R2}$ is around 4μs in 3-Ch VR in current desktop motherboards. Thus, ATVC operates in CCM when the transient load frequency f_{tran} is greater than 250 kHz.

The ATVC power loss in the worst case can be obtained as follows:

$$P_{Loss-CCM} = V_O \cdot \frac{I_O}{n_{Ch}} \cdot K \cdot (1-\eta_{ATVC}) / \eta_{ATVC} \qquad (3\text{-}1\text{-}21)$$

Where n_{Ch} is the number of VR channel connected with ATVC. K is the current divider ratio between R_P and R_{LM} in steady state. η_{ATVC} is the tested ATVC efficiency in CCM.



	1MHz	1.5MHz	2MHz	2.5MHz
300nH	0.865	0.846	0.857	0.847
200nH	0.869	0.850	0.840	0.824
100nH	0.863	0.844	0.834	0.820
47nH	0.856	0.840	0.831	0.816

Fig.3.1.8 Tested efficiency @ 5Vin, 1.3Vo/30A

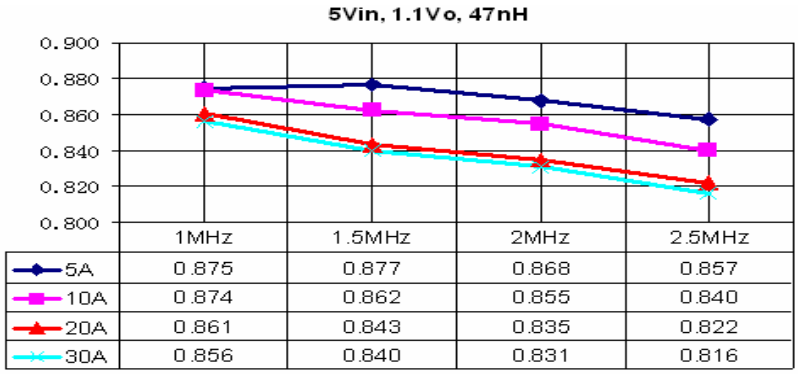


Fig.3.1.9 Tested efficiency @ 5Vin, 1.1Vo, 47nH

Fig.3.1.8 shows the tested efficiency of a one channel synchronous buck converter with different switching frequency and filter inductance @5 V_{in}, 1.3Vo/30A. Tradeoff exists between efficiency and current slew rate. In order to inject high slew rate current in ATVC, 47nH is an achievable value for the transformer leakage inductance.

Fig.3.1.9 shows the tested efficiency of a one channel synchronous buck converter with different switching frequency @ 5Vin, 1.3Vo and 47nH filter inductance. A 1.5MHZ switching frequency is selected from the point of efficiency.

Table 3.1.1 Comparison between prior arts and ATVC

Auxiliary Converter	Prior Arts		UCF Approach	
	Linear Mode	Switching Mode	Series ATVC	Parallel ATVC
Transient Response	Fast	Fast	Fast	Fast
Current Stresses of compensator	Large 100A	Large 100A	Small 100A/(1+N)	Smallest K*100A/(1+N)
Switching Frequency	N/A	High	High	High
Switching Loss	N/A	Medium	Small	Smallest
Conduction Loss	Largest	Small	Small	Smallest
Total Loss	Largest	Medium	Small	Smallest
Implementation	Easy	Easy	Medium	Easy
Component counts**	2*Switch	2*Switch& Inductor	2*Switch& transformer	2*Switch& transformer

Note: 1) I_{step}=100A, N is transformer turn-ratio
2) parallel case second winding shares K*100A in steady state (K<1)
3) different current stress of switches in different auxiliary converter

Table 3.1.1 shows the comparison between prior arts and ATVC. Parallel ATVC has fast transient response with the highest efficiency and smallest current stress among them. Furthermore, it is easy to implement, and it is suitable for low voltage high current VR.

3.2 ATVC Output Impedance Analysis

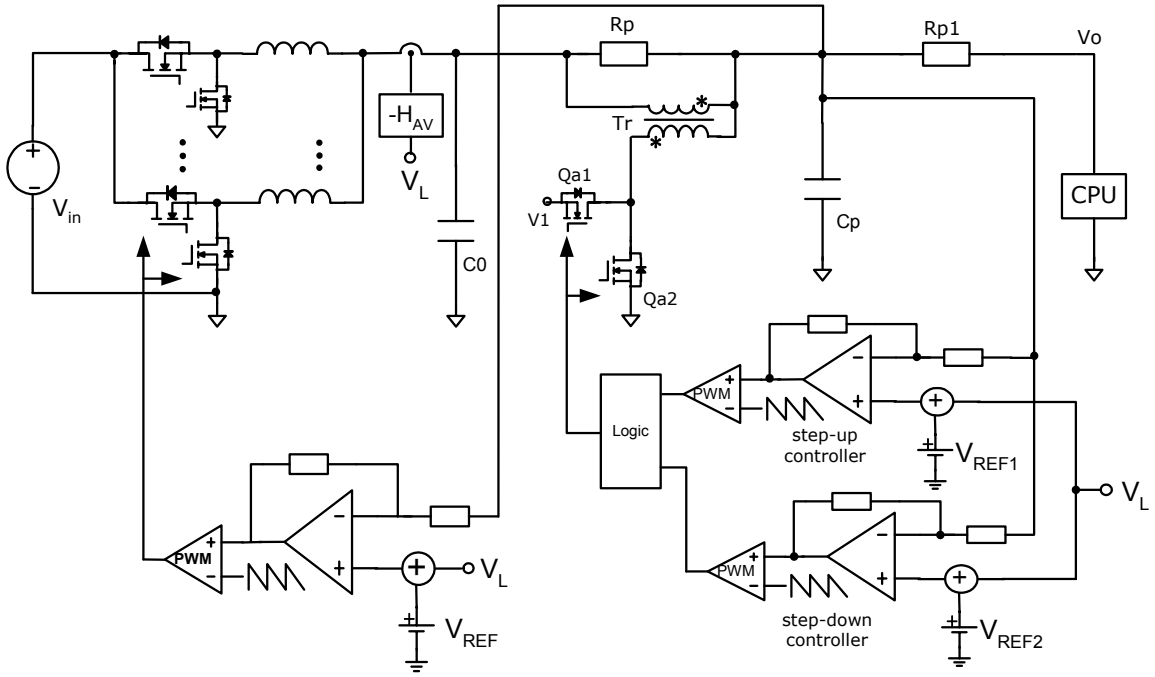


Fig.3.2.1 VR and parallel ATVC controller block diagrams

Fig.3.2.1 shows VR and parallel ATVC control block diagrams, where ATVC contains step-up controller and step-down controller. The logic block is used to keep ATVC off in the steady state and only activate ATVC in transient periods. The V_{REF1} in step-up controller is lower than VR reference voltage V_{REF}, and the V_{REF2} in step-down controller is higher than VR reference voltage V_{REF}.

$$Vref1 < Vref < Vref2 \tag{3-2-1}$$

Fig.3.2.2 shows the equivalent circuit for the output impedance analysis with close-loop controlled VR and series ATVC. Close-loop controlled VR can be assumed to be a voltage source V_{VR} with its close loop output impedance $Z_{OC\text{-}VR}$, which is the internal impedance of ATVC. Z_{ATVC} is the open loop equivalent impedance of ATVC. The output impedance of VR and series ATVC can be analyzed with the following:

$$Z_{O-SKT-S} = (Z_{OC-VRM} + Z_{ATVC} + Z_{RP}) // Z_{CP} \tag{3-2-2}$$

$$Z_{OC-SKT-S} = \frac{Z_{O-SKT-S}}{1 + Ti(s)} \tag{3-2-3}$$

$$Z_{DC-S} = Z_{OC-VR} + Z_{ATVC} + Z_{RP} + Z_{RP} \tag{3-2-4}$$

Ti(s) is the loop gain of ATVC circuit. From Equation (3-2-3), it is clear that the $Z_{OC\text{-}VR}$ has a small impact on output impedance $Z_{OC\text{-}SKT\text{-}S}$ by close loop control. Thus, it allows reducing the number of VR bulk capacitance for certain voltage tolerance. As discussed in Section 2.2, ATVC can also achieve constant output impedance by using AVP method [14] [17-19].

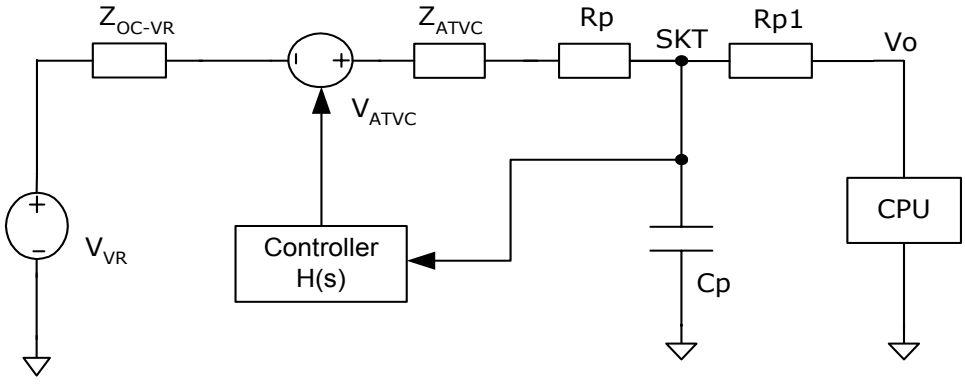


Fig.3.2.2 Equivalent circuit for series ATVC

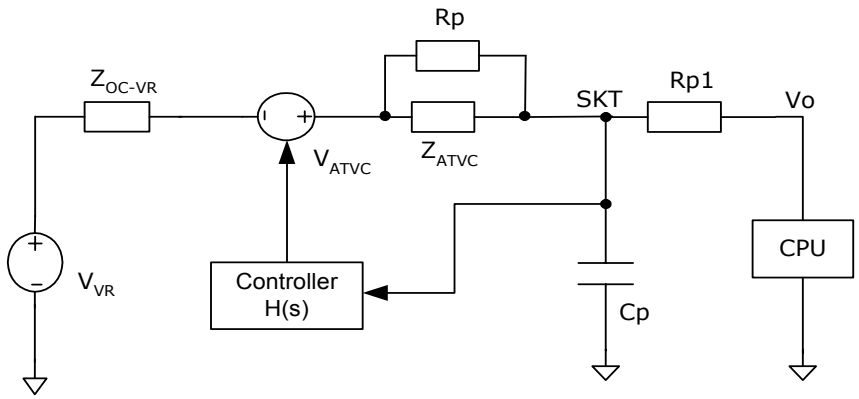


Fig.3.2.3 Equivalent circuit for parallel ATVC

Fig.3.2.3 shows the output impedance analysis circuit of parallel ATVC. The output impedance of parallel ATVC can be obtained as follows,

$$Z_{O-SKT-P} = (Z_{OC-VRM} + Z_{ATVC} // R_{RP}) // Z_{CP} \tag{3-2-5}$$

$$Z_{OC-SKT-P} = \frac{Z_{O-SKT-P}}{1 + Ti(s)} \tag{3-2-6}$$

$$Z_{DC-P} = Z_{OC-VR} + Z_{ATVC} // Z_{RP} + Z_{RP} \tag{3-2-7}$$

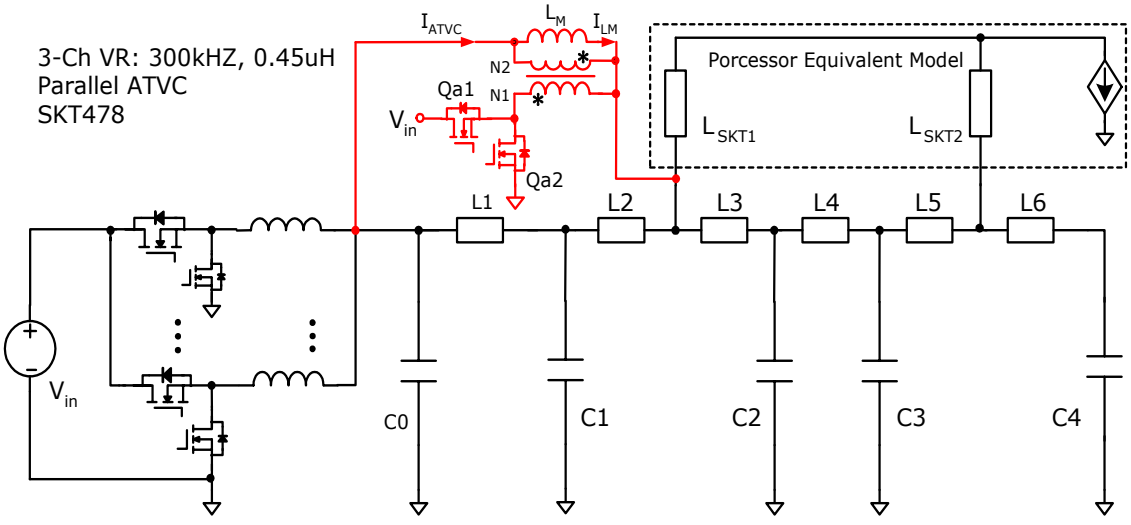


Fig.3.2.4 CPU power distribution model of SKT478 with parallel ATVC

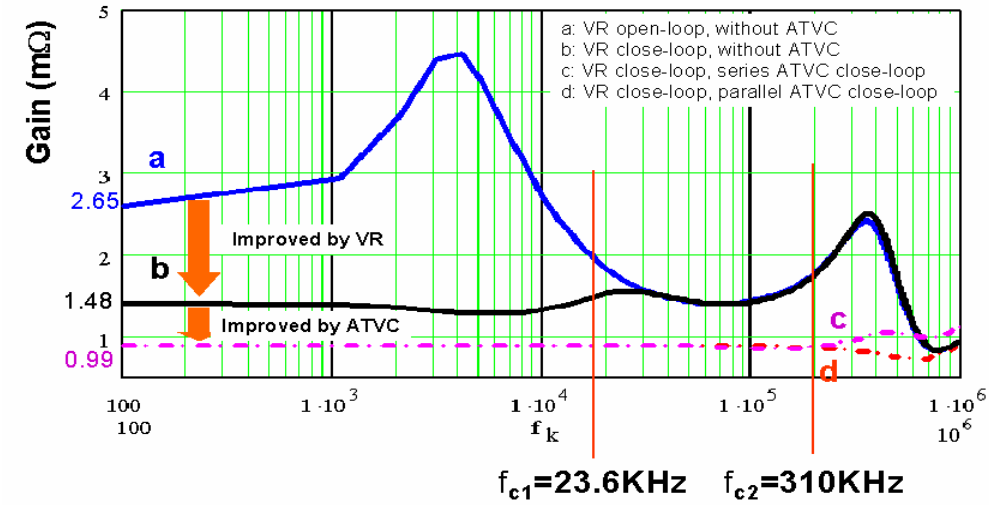


Fig.3.2.5 Socket load line of VR and ATVC in SKT478

Fig.3.2.4 shows parallel ATVC implementation circuit in SKT478 PD model [5]. ATVC is in parallel with L1 and L2 in SKT478 PD model. 3-Ch VR in SKT478 has about 2.65mΩ open loop load line, and it achieves almost constant 1.48 mΩ close loop socket load line within 23.6 kHz bandwidth by using AVP method.

With the introduction of parallel ATVC in SKT478, the close loop socket load line can be reduced to 0.99mΩ within 310 kHz ATVC close-loop bandwidth as shown in Fig.3.2.5.

Fig.3.2.6 shows parallel ATVC in LGA775 PD model [4], which is in parallel with RMB1 on the north side. Main VR has 2.55mΩ open loop socket load line, and it achieves almost constant 1.08mΩ socket load line within 23.6 kHz close loop bandwidth by using AVP method.

With the introduction of parallel ATVC in LGA775, the socket load line can be further reduced to about 0.81mΩ within 310 kHz ATVC close loop bandwidth in Fig.3.2.7.

From the above analysis, we can see that ATVC further reduces the socket load line socket PD model with VR. It also reduces the number of VR bulk capacitors, making ATVC suitable for high slew rate VR for fast transient response.

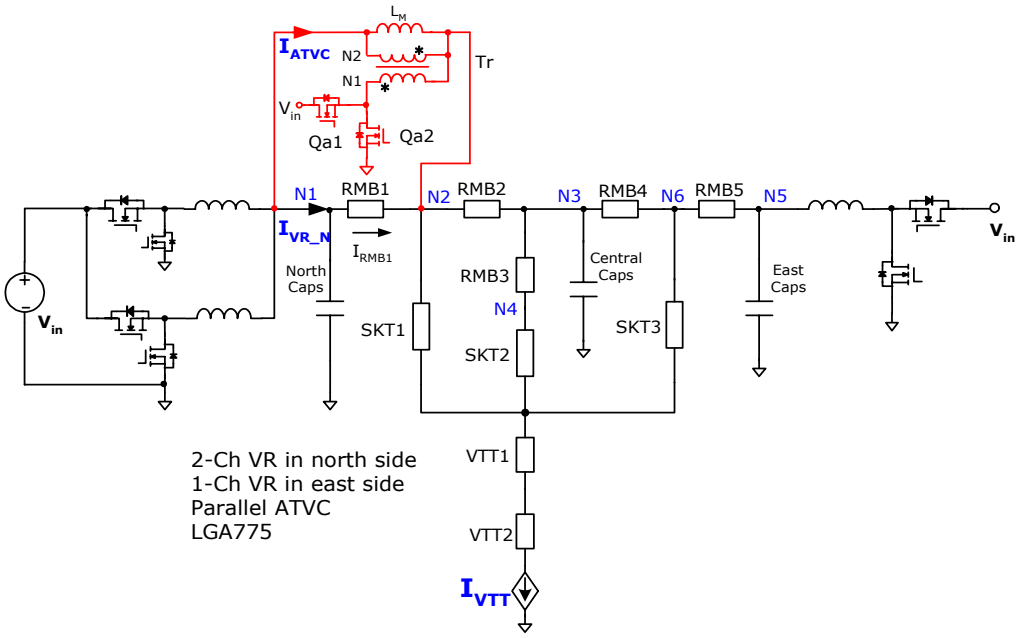


Fig.3.2.6 CPU power distribution mode of LGA775 with parallel ATVC

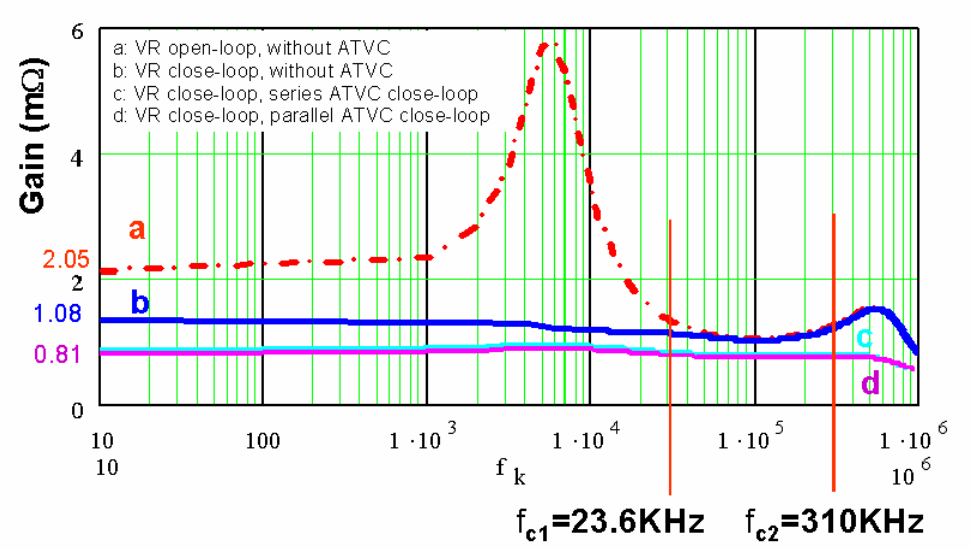


Fig.3.2.7 Load line of N2 with VR and ATVC in LGA775

3.3 ATVC Simulation

The transformer plays a very important role in the ATVC topology for fast transient response. It conducts DC current in steady state, and it acts as a transformer in the transients handling the AC current. The transformer leakage inductance determines the injected current slew rate, and the parasitic resistances determine the conduction loss and injected voltage source. Of course, size of the transformer is another concern in the design. Maxwell 3D transformer simulation has been carried out to optimize the transformer design from the point of injected current slew rate and power loss.

3.3.1 Maxwell 3D Transformer Simulation

Fig.3.3.1 shows the equivalent ATVC transformer model, consisting of R_{LK2}, L_{LK2} in the primary side, R_{LK1}, L_{LK1} in secondary side and the magnetizing inductance L_{LM}, and the turn ratio is N:1. The total transformer leakage inductance acts as the ATVC filter and determines the injected current slew rate. Smaller leakage inductance leads to higher slew rate in injected current but it increases the current ripple. Parasitic resistances in primary and secondary windings result in conduction loss and deterioration of injected voltage source. Different winding arrangement and turn ratio strongly influence the leakage inductance and resistance.

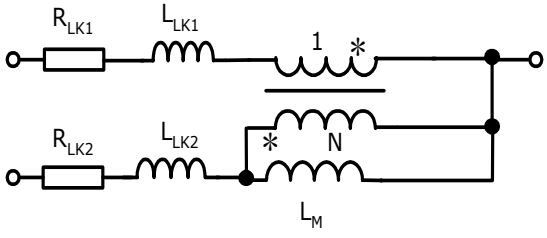


Fig.3.3.1 Equivalent ATVC transformer model

The secondary winding resistance R_{LK1} parallels with R_P in parallel ATVC, which determines the current via the secondary winding in steady state. In Series ATVC, R_{LK1} is in series with R_P in the current path that increases the conduction loss in steady state.

The voltage drop across the primary winding resistance R_{LK2} will decrease the injected voltage source value, which deteriorates the ATVC performance. Also, the transformer turn ratio determines the current rating of Q_{a1} and Q_{a2} in ATVC. A high turn ratio helps to reduce the current rating for low conduction and switching loss and increase the slew rate of injected current. On the contrary, it increases the leakage inductance and primary side winding resistance, which deteriorates the slew rate of injected current. Tradeoff exists between them.

Maxwell 3D magnetic simulations are used to optimize the ATVC transformer design from the current slew rate and power loss with the following parameters and requirements:

1) Switching frequency: 1.5MHZ, 2MHZ, 2.5 MHZ;

2) Transformer turn ratio:1:1, 2:1, 4:1;

3) 4 PCB layer for windings; ER 11/2.5/6, core material: 3F5;

4) Primary leakage inductance: less than 100nH;

5) Low power loss and small size requirement.

We can select the magnetic core size and air gap for inductor with the DC current in steady state and prevent saturation in the transients based on maximum current Imax and Bmax as follows:

$$l_g \geq \frac{N \cdot I_{Max} \cdot \mu_O}{B_{Max}} \tag{3-3-1}$$

$$A_C = \frac{L \cdot l_g}{N^2 \cdot \mu_O} \tag{3-3-2}$$

According to Equations (3-3-1) and (3-3-2), we can determine the minimum air gap according to maximum Imax and Bmax based on the effective area AC of magnetic core 3F35 ER11 with 450mT Bsat.

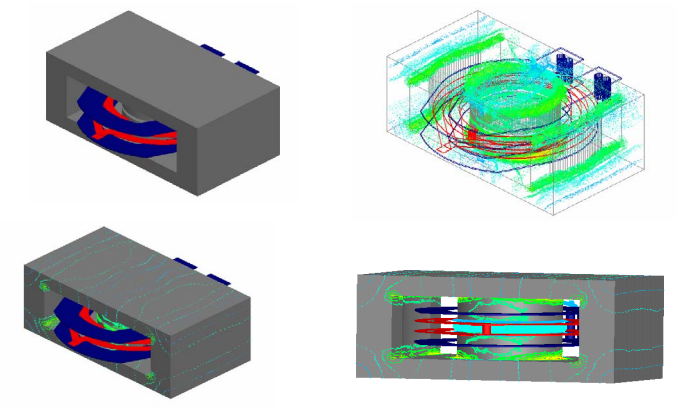


Fig.3.3.2 Maxwell 3D drawing of ATVC transformer

Fig.3.3.2 shows the Maxwell 3D transformer drawing. For 1:1 turn ratio transformer, the winding arrangement is 1P-1S-1P-1S (1P is one turn primary winding, and 1S is one turn secondary winding). For 2:1 turn-ratio transformer, the winding arrangement is 2P-1S-2P-1S, and two layer primary windings are in parallel. For 4:1 turn ratio transformer, the winding arrangement is 2P-1S-2P-1S and two layers are in series to form 4 turn winding.

Table 3.3.1 Maxwell 3D ATVC transformer simulation results

3D simulation: ER11, 1.5MHz, 3F35, 0.2mm air gap, 4-layer PCB planar			
Turn ratio	1:1	2:1	4:1
Lm	55nH	223nH	905nH
L_{LK1}	5.7nH	4.7nH	6.8nH
R_{LK1}	13.7mΩ	13.4mΩ	13mΩ
L_{LK2}	6nH	7.2nH	22nH
R_{LK2}	13.5mΩ	34.4mΩ	164mΩ

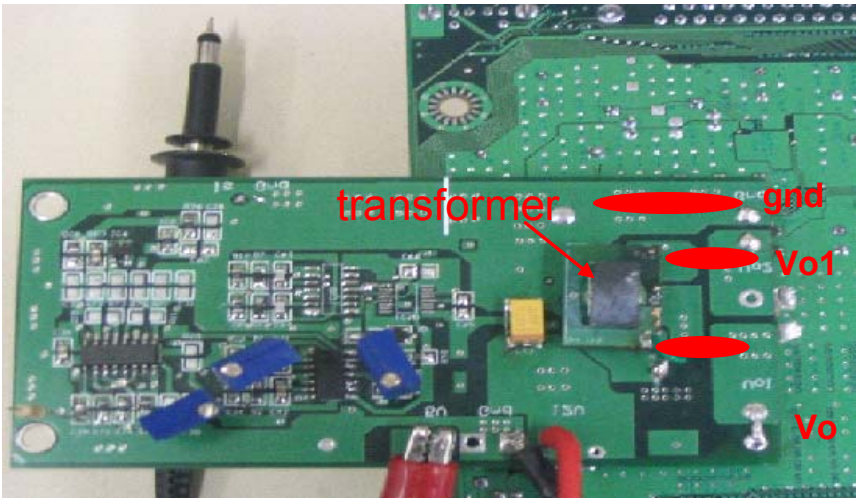


Fig.3.3.3 ATVC prototype on Intel motherboard

Fig.3.3.3 shows the ATVC prototype on an Intel motherboard. There are only three connections between ATVC prototype and Intel motherboard: gnd, Vo1 and Vo.

The parasitic resistance and inductance of PCB traces and socket connection pins have very important roles in the ATVC injected current slew rate and power loss. These parasitic parameters can be optimized by careful PCB layout, more PCB layers and large customized core shape.

The inductance of a via is given by,

$$L = \frac{h}{5} \cdot (1 + \ln \frac{4h}{d}) \quad nH \tag{3-3-3}$$

Where, h is the height of vias in mm, which equals the thickness of the board, and d is the diameter in mm. Several vias in parallel and large vias will yield small inductance.

An approximation for the inductance of a conductor is given by,

$$L = 2 \cdot l \cdot (\ln \frac{4h}{d} - 0.75) \quad nH \tag{3-3-4}$$

Where length l and diameter d are in centimeters.

For the inductance of PCB, traces are given by,

$$L = 2 \cdot l \cdot (\ln \frac{2l}{w} - 0.5 + 0.2235 \frac{w}{l}) \quad nH \tag{3-3-5}$$

Where w is the width of the trace, and l is the length, all in centimeter. Inductance of PCB traces hardly depends on the thickness of the copper. Reducing the length is more effective than width or diameter by a factor of 10.

Fig.3.3.4 shows the equivalent ATVC transformer model including the parasitic resistance and inductance of the PCB traces, vias, connection pins between ATVC prototype and Intel motherboard. It is clear that 2:1 turn ratio transformer has higher resistance and inductance than that in 1:1 turn ratio transformer. Higher turn ratio transformer can reduce the current handled by ATVC, but it has larger leakage inductance and resistance that deteriorates the ATVC performance. The increased ATVC input voltage will improve the ATVC performance. In the ATVC design, there is a trade off between power loss and ATVC performance.

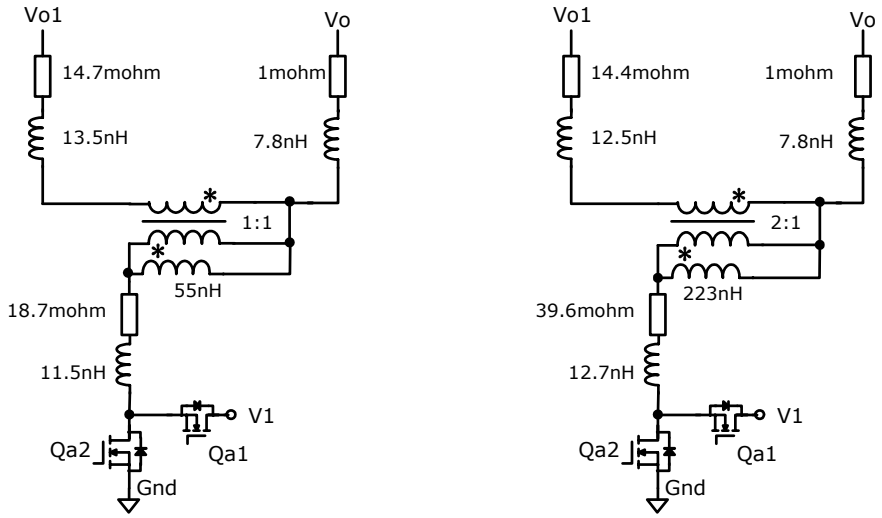


Fig.3.3.4 ATVC transformer model including parasitic components

3.3.2 ATVC Pspice Simulation

Based on the previous analysis, Pspice simulations have been carried out in SKT478 and LGA775 PD models [3-4]. Parallel ATVC is mainly used to suppress the second voltage spike.

Some specifications of ATVC and VR in simulations are as following.

- 3-Ch main VR: 250 kHz, 0.45μH filter inductance, Vin=12V, 1.1V/120A;
- ATVC: 1.5MHZ switching frequency, 5V input voltage;
- ATVC Transformer model in Fig.3.3.4;
- Independent control for main VR and ATVC;
- Two voltage mode controllers in ATVC: step-up controller in step-up load and step-down controller in step-down load.

3.3.2.1 ATVC Simulation in Socket 478

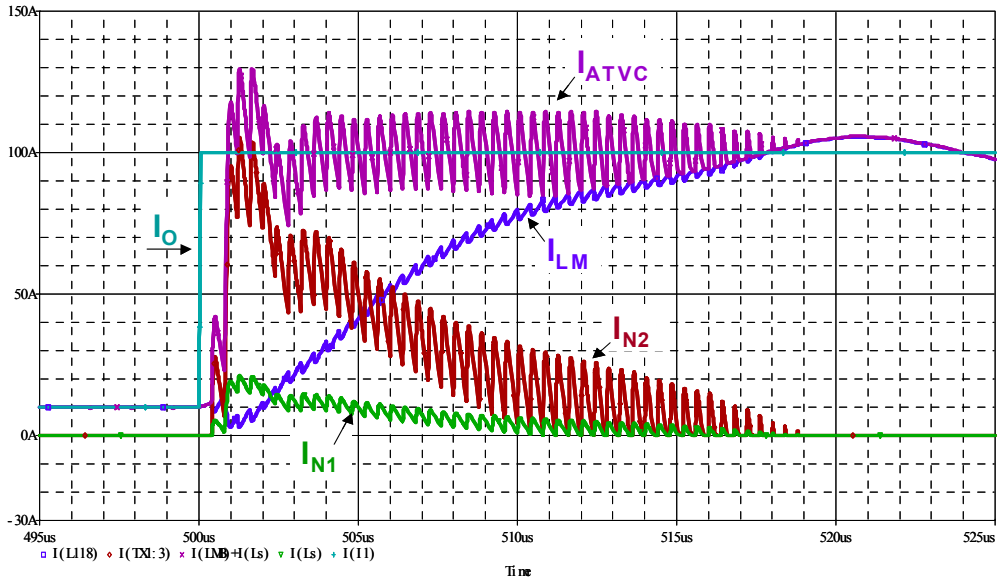


Fig.3.3.5 Parallel AVTC current waveforms in step-up load

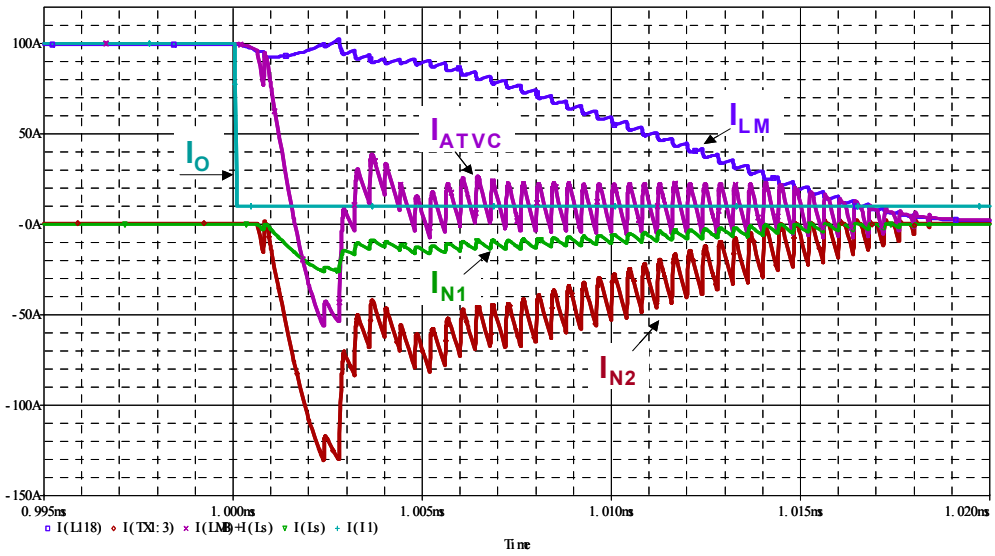


Fig.3.3.6 Parallel AVTC current waveforms in step-down load

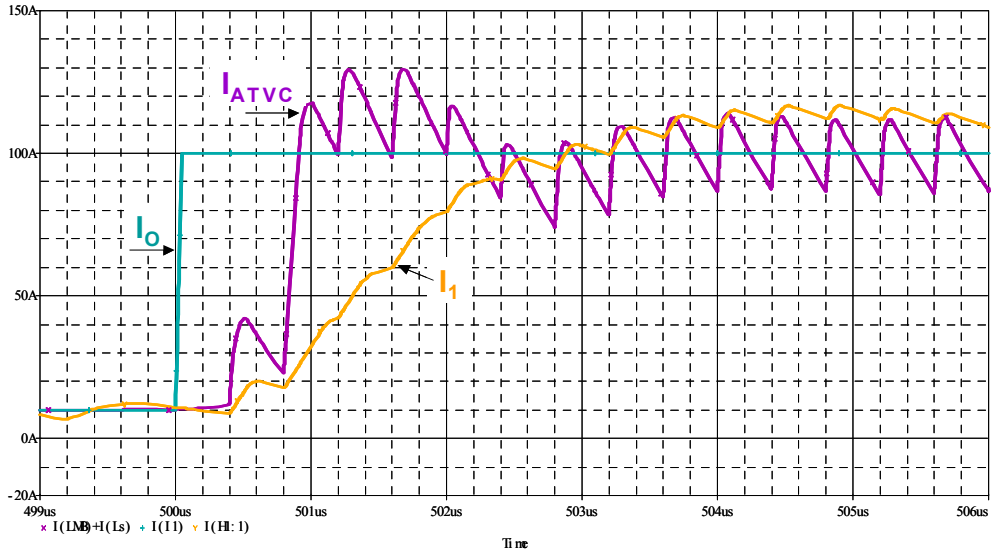


Fig.3.3.7 Parallel ATVC and VR Current in step-up load

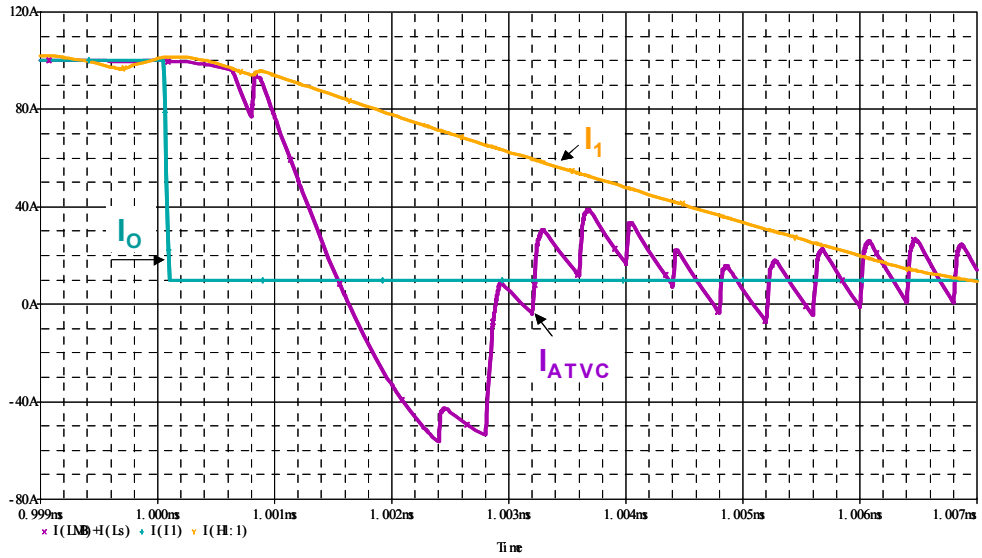


Fig.3.3.8 Parallel ATVC and VR Current in step-down load

SKT478 PD model has about 1.5mΩ socket load line including DC and AC load lines within its close loop bandwidth. ATVC is in parallel with L1 and L2 as shown in Fig.3.2.4. ATVC operates in 1.5MHZ with 4:1 turn ratio transformer.

Fig.3.3.5 shows the key ATVC current waveforms in step-up load 10~100A@95A/μs. The ATVC output current I_{ATVC} can catch up with output current I_O after a very small delay time in the step-up controller. ATVC injects high slew rate current both in primary side and in secondary winding until the magnetizing current I_{LM} reaches the maximum output current 100A.

Fig.3.3.6 shows the key ATVC current waveforms in step-down load 100~10A@95A/μs. It is clear that the part of energy stored in VR filter inductance is recovered into ATVC input voltage V_1 because current changes from positive to negative value until I_{LM} drops to the minimum output current 10A.

Fig.3.3.7 shows the simulated current comparison between main VR current I_1 and ATVC output current I_{ATVC} in step-up load. ATVC provides higher slew rate current injection, 15 times higher than that in the main VR.

Fig.3.3.8 shows the simulated current comparison between main VR current I_1 and ATVC output current in step-down load. ATVC can provide five times higher slew rate current than that in the main VR, and it recycles energy stored in VR filter inductance into input voltage V1, resulting in better ATVC efficiency. Fig.3.3.9 shows the simulated results with VR in SKT478 PD model and parallel ATVC in step-up load. The load line baseline of SKT478 PD model is about 1.5mΩ, and the response time is 1.5μs. With introduction of parallel ATVC, load line is reduced to 1.06 mΩ, which is about 29 percent load line improvement including DC load line improvement, and response time is reduced to 0.3μs.

Fig.3.3.10 shows the simulated results with VR in SKT478 PD model and parallel ATVC in step-down load. The baseline without ATVC is about 1.48 mΩ. Improved socket load line is 1.18 mΩ by utilization of parallel ATVC, about 20 percent improvement.

From the simulation results, we can see that parallel ATVC injects high slew rate in step-up load and recovers energy in step-down load, resulting in AC load line improvement. DC load line improvement mainly depends on the parasitic resistance of one turn secondary winding in transformer design.

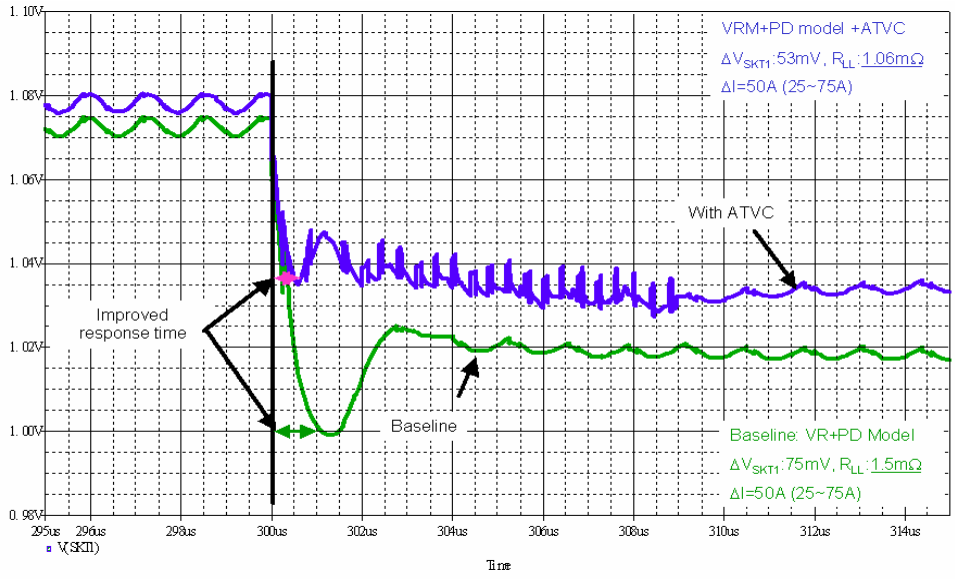


Fig.3.3.9 Parallel ATVC simulation results in step-up load

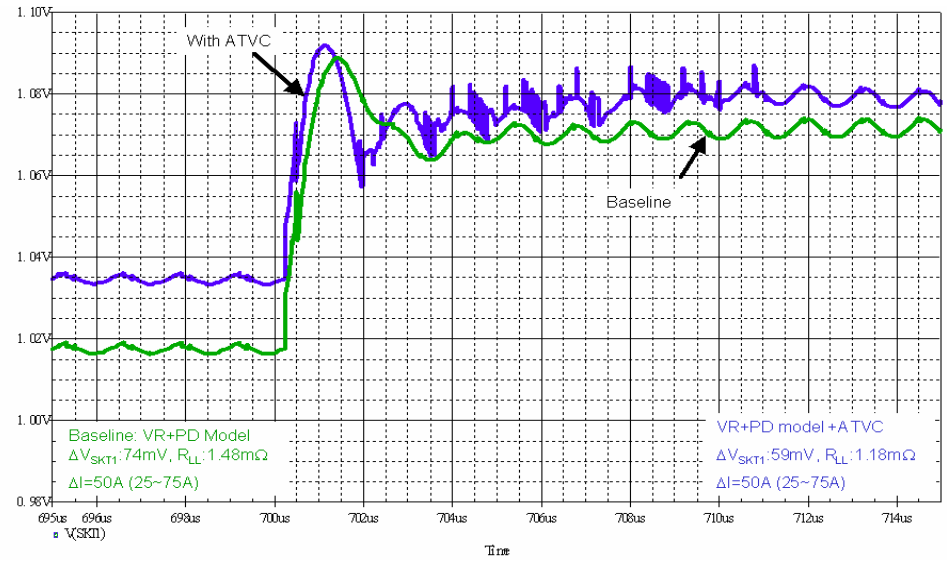


Fig.3.3.10 Parallel ATVC simulation results in step-down load

3.3.2.2 ATVC Simulation in Socket LGA775

Pspice simulation schematics of LGA775 PD model [4] with parallel ATVC is shown in Fig.3.2.6. ATVC is in parallel with RMB1 in the main VR, which operates in 1.5MHZ with 1:1 transformer model in Fig.3.3.6.

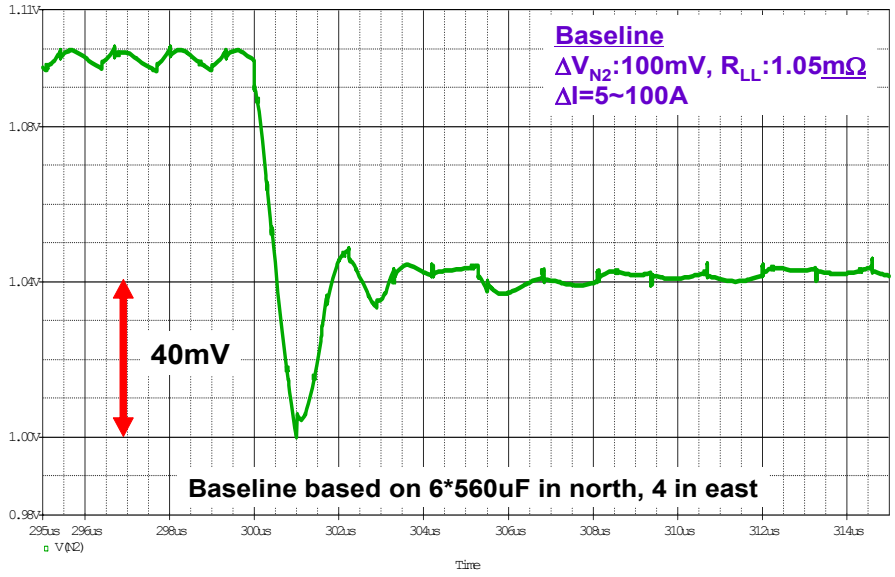


Fig.3.3.11 LGA775 baseline load line in step-up load

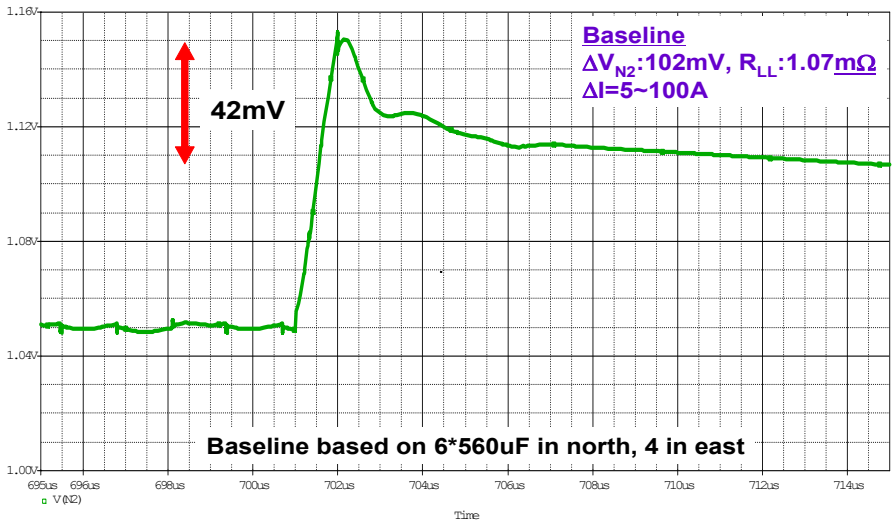


Fig.3.3.12 LGA775 baseline load line in step-down load

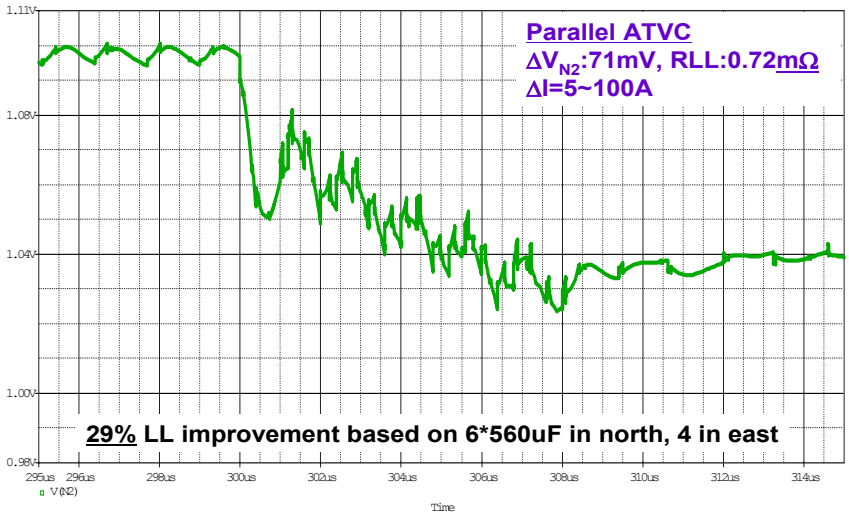


Fig.3.3.13 Improved LGA775 load line with ATVC in step-up load

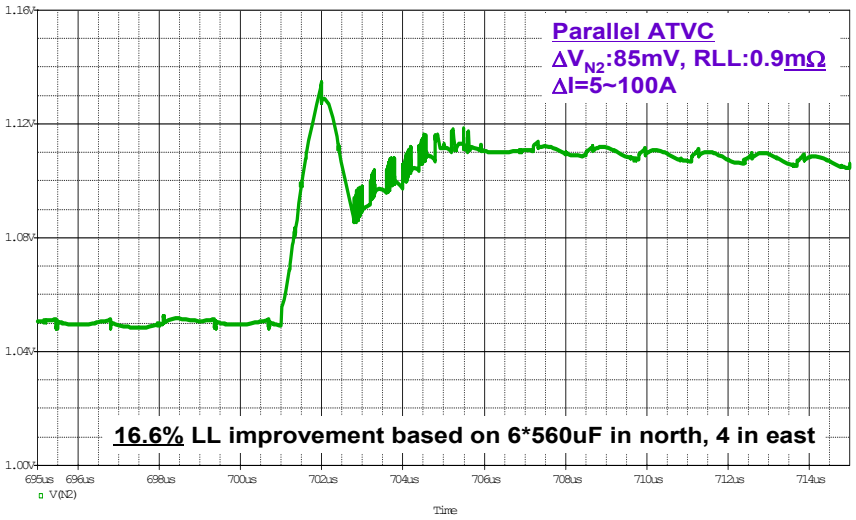


Fig.3.3.14 Improved LGA775 load line with ATVC in step-down load

Fig.3.3.11 shows the baseline load line of LGA775 PD model, which has 1.05mΩ (100mV) in 5~100A, 95A/μs step-up load with 6 Oscons on the north side and 4 Oscons on the east side. In step-up load, the DC load line is about 0.63mΩ (60mV) and the AC load line is about 0.42mΩ (40mV). The expected maximum AC load line improvement in this condition is

about 0.32mΩ (30~34mV) because of 10~15mV voltage difference between the reference voltage in ATVC step-up controller and the main VR output voltage.

Fig.3.3.12 shows the baseline load line of PD model, around 1.07mΩ (102mV) in 100~5A, 95A/μs step-down load. The DC load line is about 0.63mΩ (60mV), and the AC load line is about 0.44mΩ (42mV). The expected maximum AC load line improvement in step down is about 0.34mΩ (32~36mV) because of a 10~15mV voltage difference between the voltage reference in ATVC step-down controller and the main VR output voltage.

Fig.3.3.13 shows the improved load line with ATVC in step-up load. The improved load line is 0.72mΩ, up to 95 percent of expected maximum AC load line improvement and about 29 percent improvement of total load line. Fig.3.3.14 shows the improved AC load line with ATVC in step-down load. The improved load line is 0.9mΩ, up to 50 percent of expected maximum AC load line improvement, or 16.6 percent total load line improvement.

Table 3.3.2 LGA775 Simulation results

Intel LGA775 PD model: 2-Ch in north, 1-Ch in east, 250kHz, 0.45uH,100A/us, 5~100A ATVC: 1:1, 1.5MHz, 5V input				
	Oscon Caps in north and in east side			
	6*4	4*4	3*4	3*3
Step up load	0.75mΩ	0.79mΩ	0.81mΩ	0.83mΩ
Step down load	0.9mΩ	1.02mΩ	1.11mΩ	1.19mΩ
VR load line baseline W/O ATVC: 1.05mΩ in step up load 1.07mΩ in step down load.				

Table 3.3.2 shows the Oscon impact on the parallel ATVC performance. It is clear that the load line improvement in step-up load is better than that in step-down load, because higher slew rate current is injected in step-up rather than in step-down load. Parallel ATVC can still achieve good load line improvement in step-up load with less Oscon capacitor, but the improvement in step down will decrease due to the reduced capacitance and increased ESR.

3.4 Proposed Combination of Linear and Adaptive Nonlinear Control

3.4.1 Background

As previously discussed, the converter transient or large signal response is mainly limited by filter inductance and dv/dt or delay times in linear controller. High switching frequency operation helps the converter to reduce the filter inductance, but it deteriorates converter efficiency. How to design the linear controller to minimize its delay time of the compensation network is very crucial for the second voltage spike suppression. The longer the delay time it has, the worse transient response occurs in transient loads.

Enough gain and phase margins are always required in the conventional linear control for the converter stability, which leads to longer delay time and bad transient response. In transient periods, the error amplifier output (EAO) responds immediately to catch up with the transient load change in an ideal case, so there are no voltage spikes in the output voltage. Actually, the EAO is determined by EA performance and the compensation network design. Thus, it cannot change as quickly as the load changes, and finally the output voltage spikes occur. The transient response can be improved by optimizing the unity gain bandwidth in the linear controller. There

is a trade off between the transient response and converter stability in the design. Usually, high performance and costly EA, such as high product of gain and bandwidth, high dv/dt, are used to reduce the delay time for fast transient response.

Hysteretic control [53, 54] [63] [67, 68] has a very small delay time because it has no compensation network, and the delay time is only determined by the performance of the comparator. When output voltage increases and is larger than the top window reference voltage, it outputs low drive signal, or vice versa, and a high drive signal is generated. The main disadvantage of hysteretic control is the variable switching frequency related with hysteretic window, which makes it difficult to design the converter filter. Not only the parasitic resistance and inductance of PCB traces, but output capacitors and connectors also have strong impact on the hysteretic control, and also are very sensitive to the noises. So the hysteretic control is very difficult for high slew rate applications, such as VR in the desktop motherboard.

Active voltage position method [14-19] is an improved linear control, which increases the output voltage transient tolerance as much as twofold in the voltage regulator, and it can achieve almost constant VR output impedance. In transient periods, the delay times in linear controller increase the second voltage spike, and it is impossible to eliminate the delay time due to the requirement of the converter stability.

With the increasing demand for better dynamic performance under high slew rate output current, smaller delay times in a linear controller are required to improve the transient response. A combination of linear and adaptive nonlinear control is proposed to reduce the delay times for fast transient response, and it simplifies linear controller design.

3.4.2 Concept of Combination of Linear and Nonlinear Control

Fig.3.4.1 and Fig.3.4.2 show conventional linear control block diagram and its main transient waveforms. It is well known that the EA is used to compensate the gain and phase margins for the converter stability by the feedback impedance Z_F and the input impedance Z_{in} in compensation network, whose output (EAO) is compared with saw tooth waveform in PWM generator to regulate duty cycle width for the converter. When the output voltage V_O is larger than reference voltage V_{REF1}, EAO decreases to reduce the duty cycle. When the output voltage is less than reference V_{REF1}, the EAO increases to increase the duty cycle, and finally, the tight output regulation is obtained in the converter.

In step-up load in Fig.3.4.2, the EAO and duty cycle cannot catch up with load change immediately. A voltage drop occurs in step-up load because of the delay time t_{21} in the EAO, and an over voltage spike occurs in step-down load due to the delay time t_{34}. It is impossible to eliminate the delay time in linear control because enough gain and phase margins are required for converter stability. Reducing the delay time is very important for fast transient response.

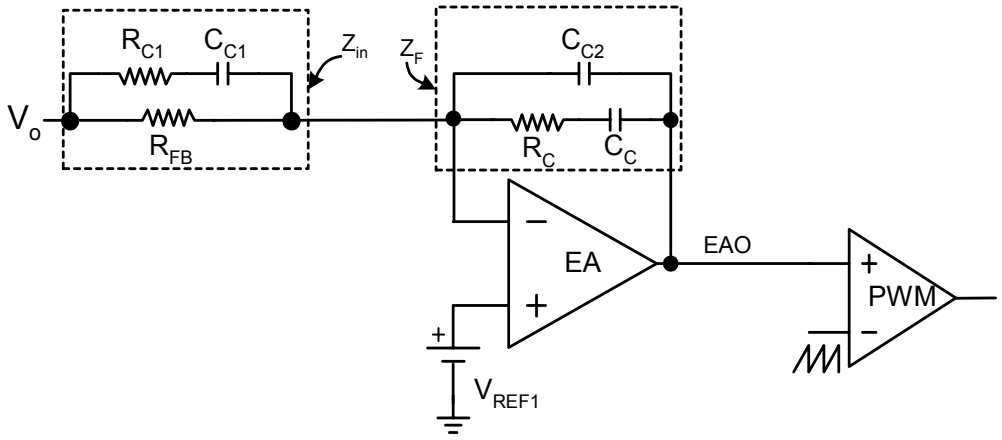


Fig.3.4.1 Conventional linear control block diagram

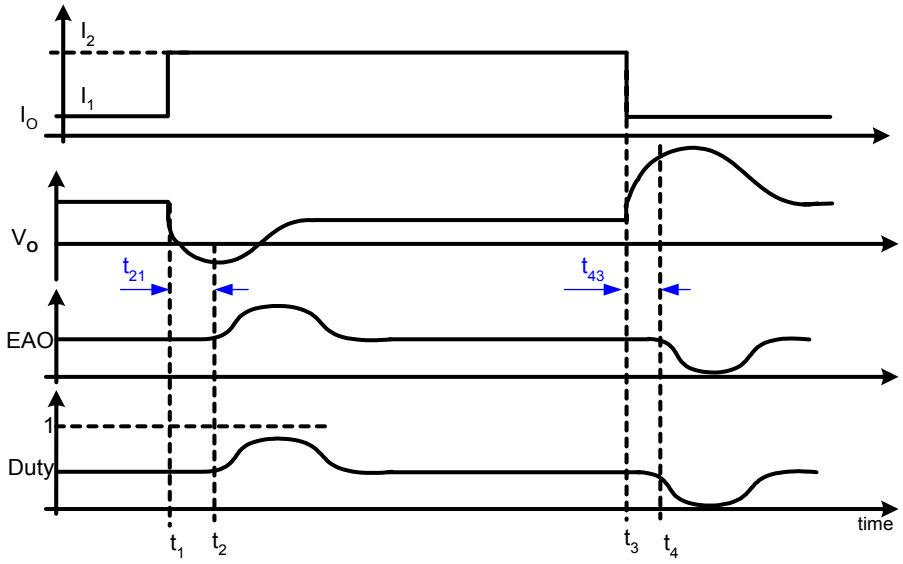


Fig.3.4.2 Conventional linear control transient waveforms

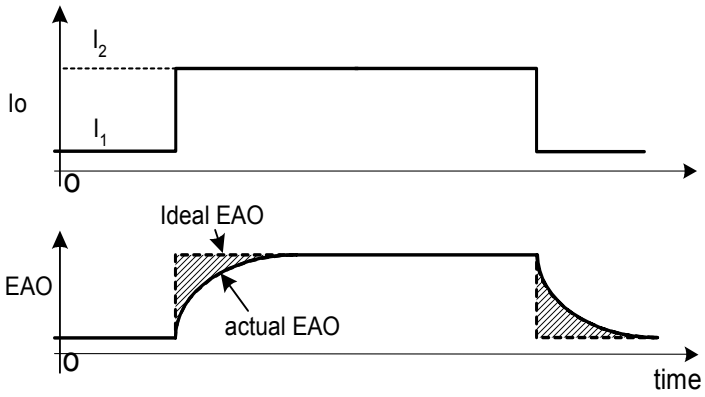


Fig.3.4.3 EAO comparisons in ideal and actual cases

Fig.3.4.3 shows the EAO comparison between the ideal and the actual cases in transient loads. The ideal EAO can respond immediately to the transient loads, and there will not be any transient voltage spikes. The actual EAO rises slowly because of the compensation network and the performance of EA. The shadowed EAO difference increases the extra transient voltage spikes. The larger shadowed area leads to a higher second transient voltage spike.

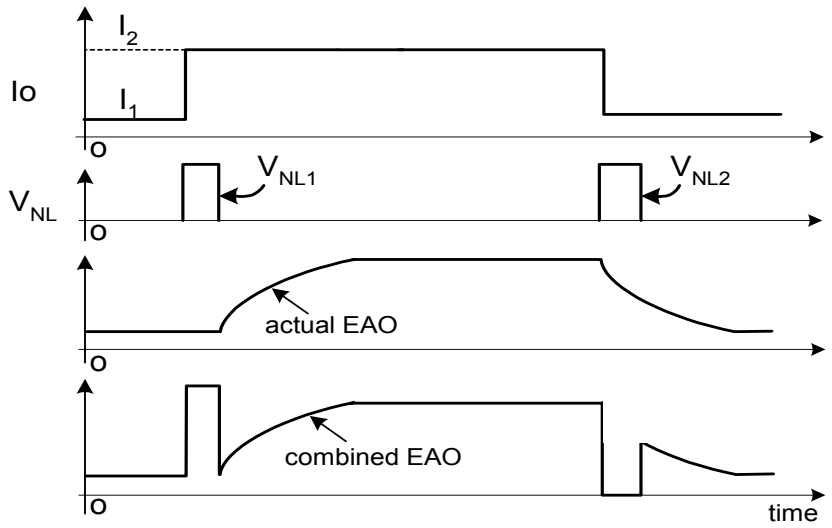


Fig.3.4.4 shows the concept of combined linear and nonlinear control to reduce the delay time for fast transient response. Nonlinear control is activated only in transient periods and generates nonlinear signal V_{NL1} in step-up load and V_{NL2} in step-down load with very small delay time with simple comparators with a hysteretic window. Only the first pulse of the output of nonlinear control V_{NL} is used to sum up the actual EAO of linear control. The area of the first pulse V_{NL1} of the output of nonlinear control approximates the shadowed area between the ideal EAO and actual EAO in step-up load shown in Fig.3.4.3. It is the same for V_{NL2} in the step-down load, and then the EAO of combined linear and nonlinear control is very close to ideal, resulting in a very small delay time and in small transient voltage spikes. Most importantly, there is no stability problem for combined linear and nonlinear control because only one pulse nonlinear control signal is injected. In the steady state, linear control determines the converter duty cycle, while nonlinear control is in standby mode.

Combined linear and nonlinear control reduces delay times, and it also simplifies the linear compensation network design for converter stability by using nonlinear control for the transient response. Fig.3.4.5 shows the implementation circuit of combined linear and nonlinear

control. V_{R11} is the constant reference voltage of comparator C_{m1} in step-up load, which is lower than steady state output voltage, and V_{R21} is the constant reference voltage of comparator C_{m2} in step-down load in nonlinear control, which is higher than steady state output voltage.

Nonlinear control circuit in dash block 300 is composed of two parts: dash block 310 for the step-up load and dash block 320 for step-down load. In the step-up load, the output voltage V_{NL1} of comparator C_{m1} is summed up with the output of linear control by the one-shot circuit and diode D_1 and R_{NL1} when the output voltage Vo is less than the reference voltage V_{R11}. Then, the converter operates at full duty cycle after a very small delay time $t'_{21;}$ thus, it can supply the current as quickly as possible to the load, and vice versa. In step-down load, V_{NL2} is subtracted from the output of linear control by comparator C_{m2}, one-shot circuit, R_2 Q_1 and $R_{NL2.}$ When the output voltage V_O is larger than reference voltage V_{R21}, EAO decreases to zero after very small delay time t'_{43}, and then there is no duty cycle. As a result, the combined linear and nonlinear control reduces the transient voltage spike by reducing response time in transient current.

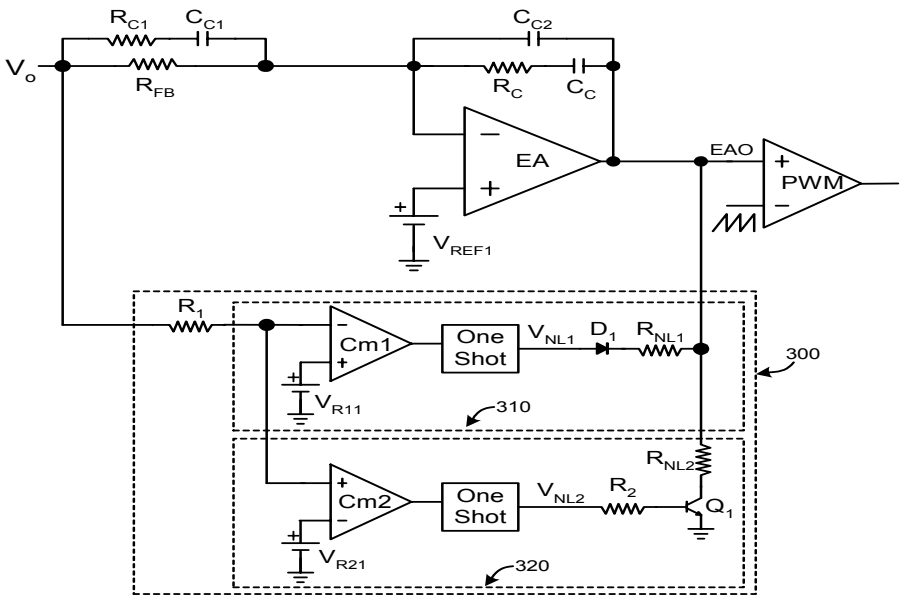


Fig.3.4.5 Implementation of the combined linear and nonlinear control

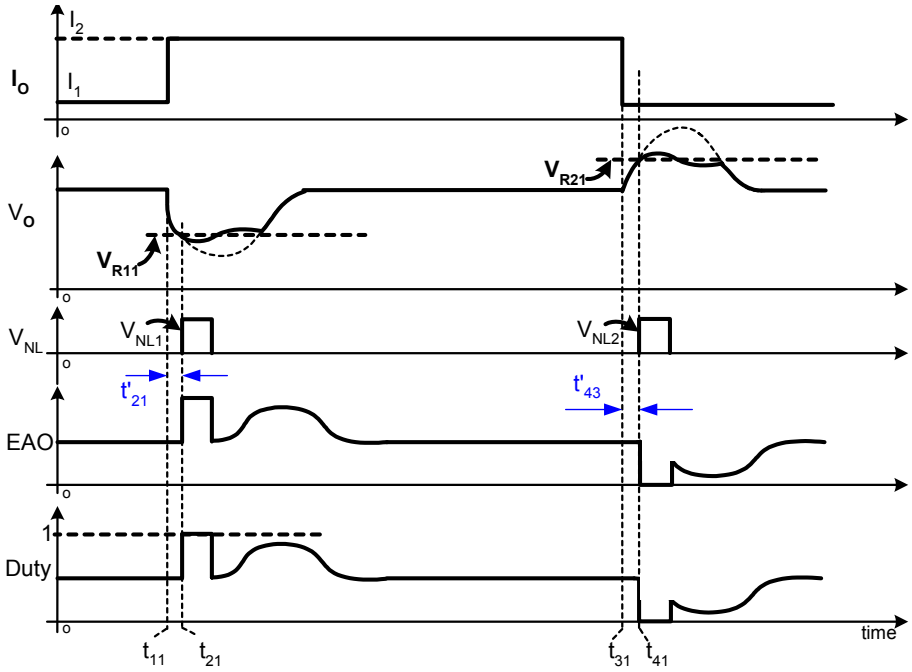


Fig.3.4.6 Key waveforms of combined linear and nonlinear control

In Fig.3.4.6, the delay time of combined linear and nonlinear control is t'_{21} in step-up load and t'_{43} in step-down load, which is mainly determined by the comparator performance and the voltage difference at two input terminals of comparator, the output voltage V_O and the reference voltage. However, in conventional nonlinear control, the voltage difference is about 100mV causing a large delay time.

Small voltage difference leads to small delay time for fast transient response. Fig.3.4.7 shows the adaptive nonlinear control concept that is proposed to reduce the voltage difference further for small delay time. It is clear that adaptive nonlinear control has a much smaller voltage difference, only 10~15mV, leading to delay time reduction with the introduction of a current signal in adaptive nonlinear control instead of over 100mV in conventional nonlinear control.

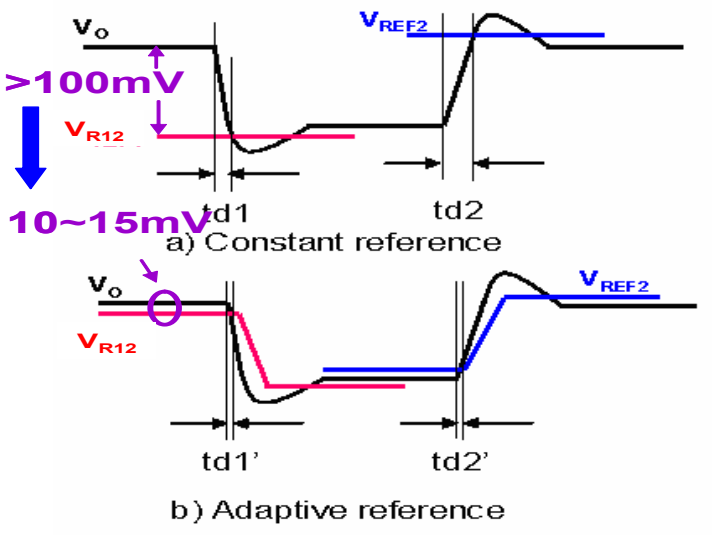


Fig.3.4.7 Concept of adaptive nonlinear control

3.4.3 Concept of Combined Linear and Adaptive Nonlinear Control

Fig.3.4.8 and Fig.3.4.9 show the implementation circuit and key waveforms of combined linear and adaptive nonlinear control. Adaptive nonlinear control is carried out in dash block 400, which is composed of a filter, a transconductance amplifier Gm and a controlled current source. The comparator reference voltages V_{R12} in step-up load and V_{R22} in step-down load in adaptive nonlinear control are shown in the dashed line in Fig.3.4.8, which are dependent on the load current. With the introduction of current signal, the delay time of nonlinear control is reduced from t'_{21} to t''_{21} in step-up load and from t'_{43} to t''_{43} in step-down load because of only 10~15mV difference between the output voltage V_O and the reference voltage V_{R12}, V_{R22} instead of 100mV in conventional nonlinear control. Therefore, the combined linear and adaptive nonlinear control further reduces delay time to reduce the second voltage spike.

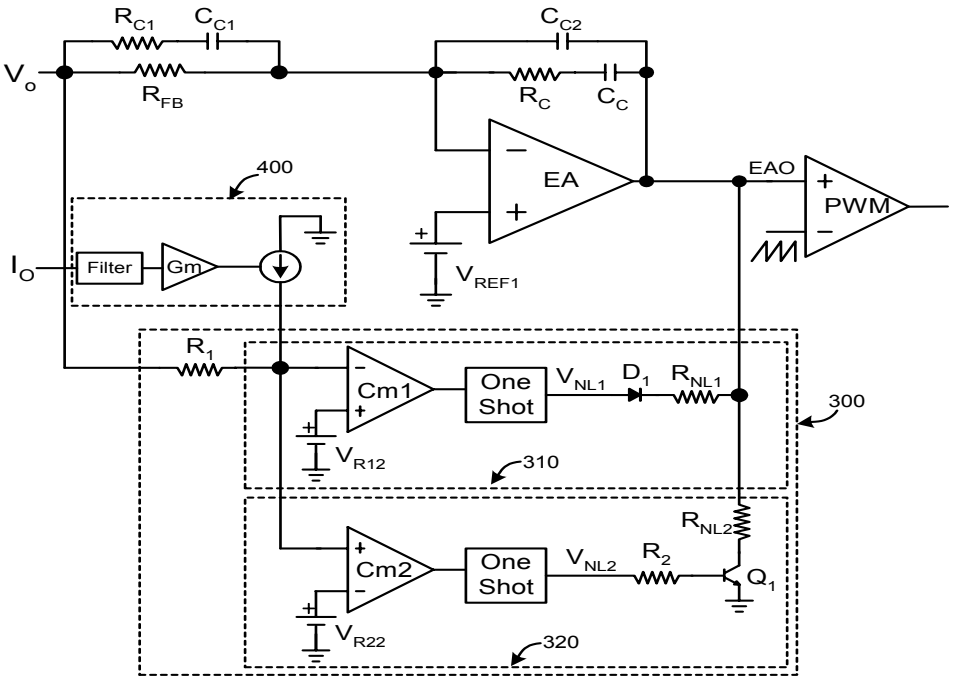


Fig.3.4.8 Implementation of combined linear and adaptive nonlinear control

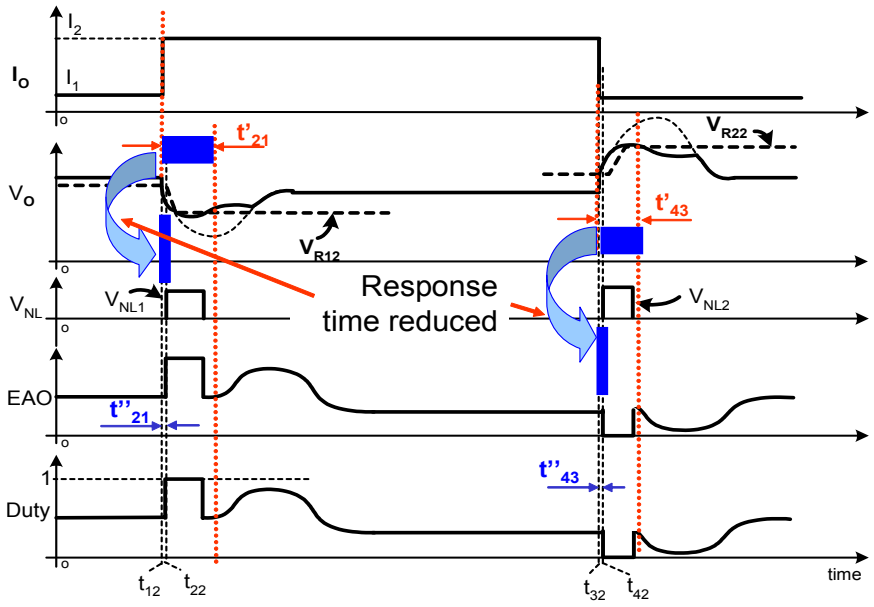


Fig.3.4.9 Key waveforms of combined linear and adaptive nonlinear control

3.4.4 Experimental Verification if Combined Linear and Adaptive Nonlinear Control

An experimental prototype has been carried out to verify combined linear and adaptive nonlinear control. Fig.3.4.10 shows the experimental circuit: 2-Ch VRM9.0 at 300 kHz switching frequency, 2.2μH inductance and ATVC at 1.5 MHZ, 2:1 turn ratio with ER11 core. The operation waveforms of the controller for ATVC are shown in Fig.3.4.9. V_{ga1} is the drive signal of Q_{a1}, and V_{ga2} is the drive signal of Q_{a2} of ATVC. V_{NL1} is the nonlinear control signal in step-up load, and V_{NL2} is the nonlinear control signal in step-down load.

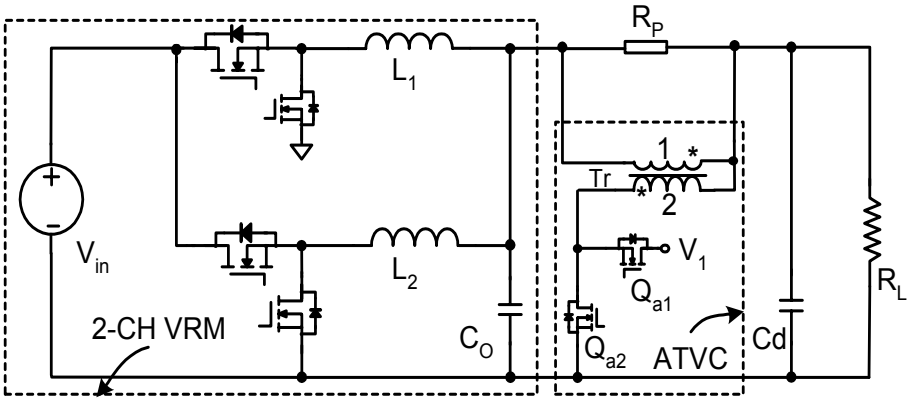


Fig.3.4.10 VRM9.0 Experimental circuit

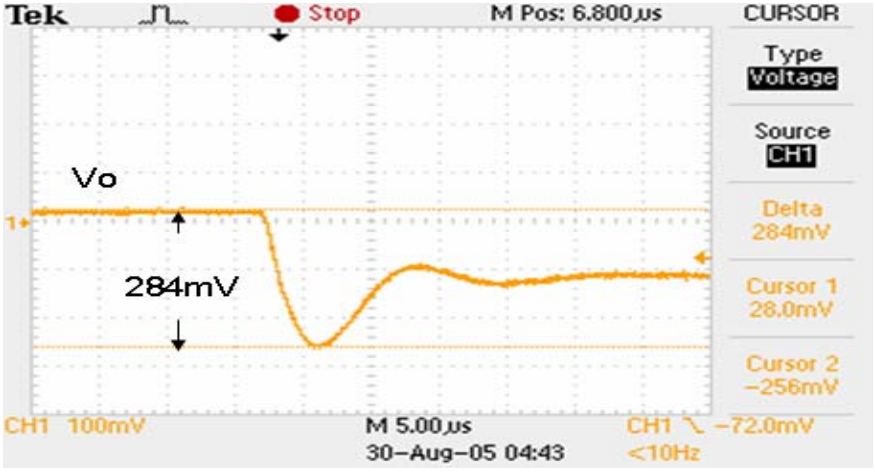


Fig.3.4.11 Output transient waveforms of 2-Ch VRM9.0 in step-up

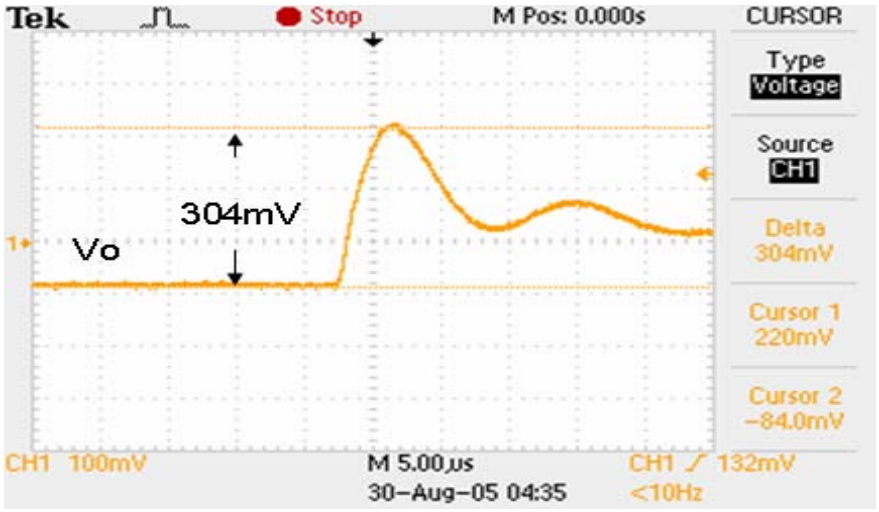


Fig.3.4.12 Output transient waveforms of 2-Ch VRM9.0 in step-down

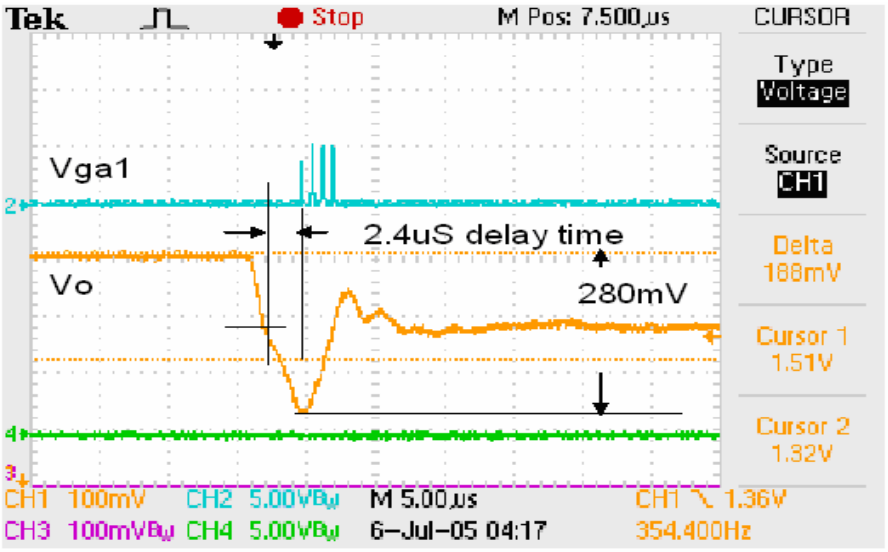


Fig.3.4.13 Transient waveforms with linear and nonlinear in step-up

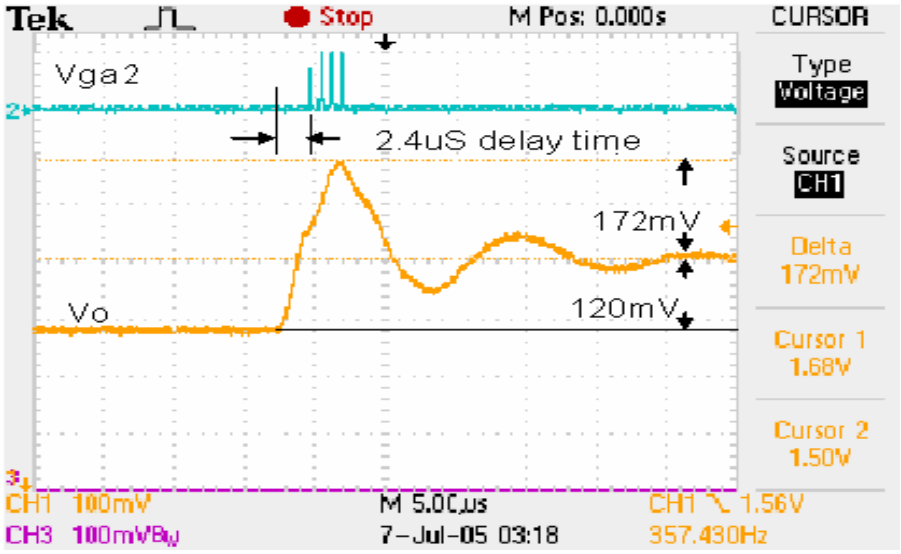


Fig.3.4.14 Transient waveforms with linear and nonlinear in step-down

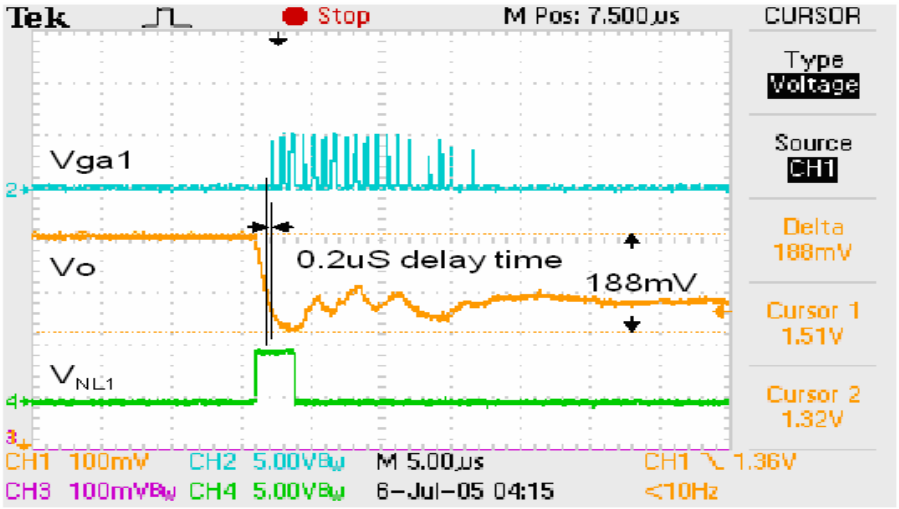


Fig.3.4.15 Transient waveforms with linear and adaptive nonlinear in step-up

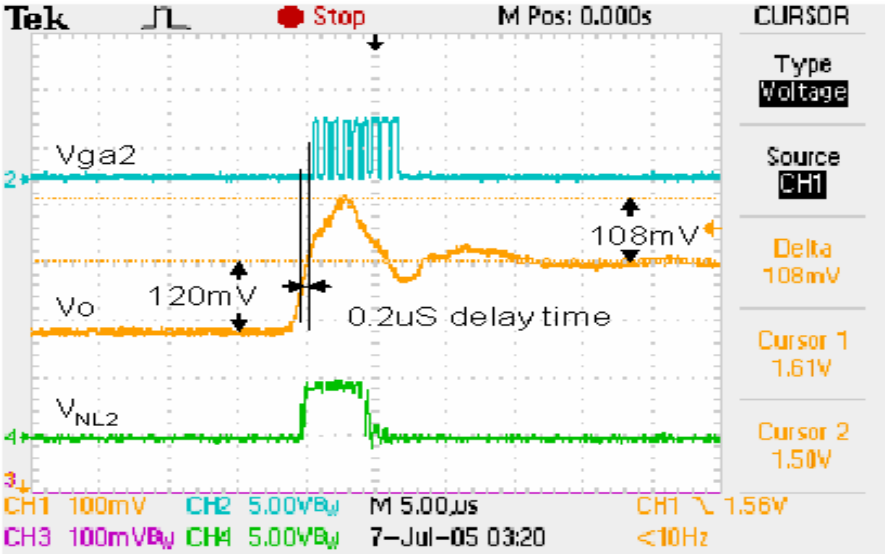


Fig.3.4.16 Transient waveforms with linear and adaptive nonlinear in step-down

Fig.3.4.11 shows the output transient waveforms in step-up load in 2-Ch VRM9.0 without ATVC. It is clear that 284mV voltage drop is in step-up load 0~25A @100A/μs, which has 13.6mΩ load line including 4.8mΩ DC load line.

Fig.3.4.12 shows the output transient waveforms in step-down load in 2-Ch VRM9.0. There is 304mV voltage overshoot in step-down load 25~0A @100A/μs, which has 14mΩ load line including 4.8mΩ DC load line.

Fig.3.4.13 shows the transient waveforms in step-up load 0~25A@100A/μs in 2-Ch VRM9.0 with ATVC that adopts the combined linear and nonlinear control in Fig.3.4.5. From tested waveforms, it has 2.4μs response times in ATVC step-up controller and 280mV voltage drop, 11.2mΩ load line. ATVC has only 4mV improvement due to 2.4μs response times.

Fig.3.4.14 shows the transient waveforms in step-down load 25~0A @100A/μs in 2-Ch VRM9.0 with ATVC that adopts the combined linear and nonlinear control in Fig.3.4.5. It has

about 292mV voltage spike and about 2.4μs response time in ATVC step-down controller. There is only 12mV improvement due to the slow response time. Total load line is about 11.68mΩ.

Fig.3.4.15 shows the transient waveforms in step-up load 0~25A @100A/μs in 2-Ch VRM9.0 with ATVC that utilizes the combined linear and adaptive nonlinear control shown in Fig.3.4.7. It has only 0.2μs response time in ATVC step-up controller. The voltage drop is reduced to 188mV, 33.4 percent improvement, about 7.52mΩ load line in step-up load.

Fig.3.4.16 shows the transient waveforms in step-down load 25~0A @100A/μs in 2-Ch VRM9.0 with ATVC that utilizes the combined linear and adaptive nonlinear control in Fig.3.4.7. It has only 0.2μs response time, and the voltage spike is reduced to 228mV, 25 percent improvement, which has 9.12mΩ load line in step-up load.

Table 3.4 Experimental results of 2-Ch VRM +ATVC

Load line in 2-Ch VR PT8124A with ATVC@ 0~25A, 100A/us					
VRM9.0	dc load line	ac load line			
		Step up	Response time	Step down	Response time
VRM baseline	120mV 4.8mΩ	340mV 13.6mΩ	N/A	350mV 14mΩ	N/A
VRM ATVC+NL&L	120mV 4.8mΩ	280mV 11.2mΩ	2.4us	292mV 11.68mΩ	2.4us
VRM ATVC+ Adaptive NL&L	120mV 4.8mΩ	188mV 7.52mΩ	0.2us	228mV 9.12mΩ	0.2us

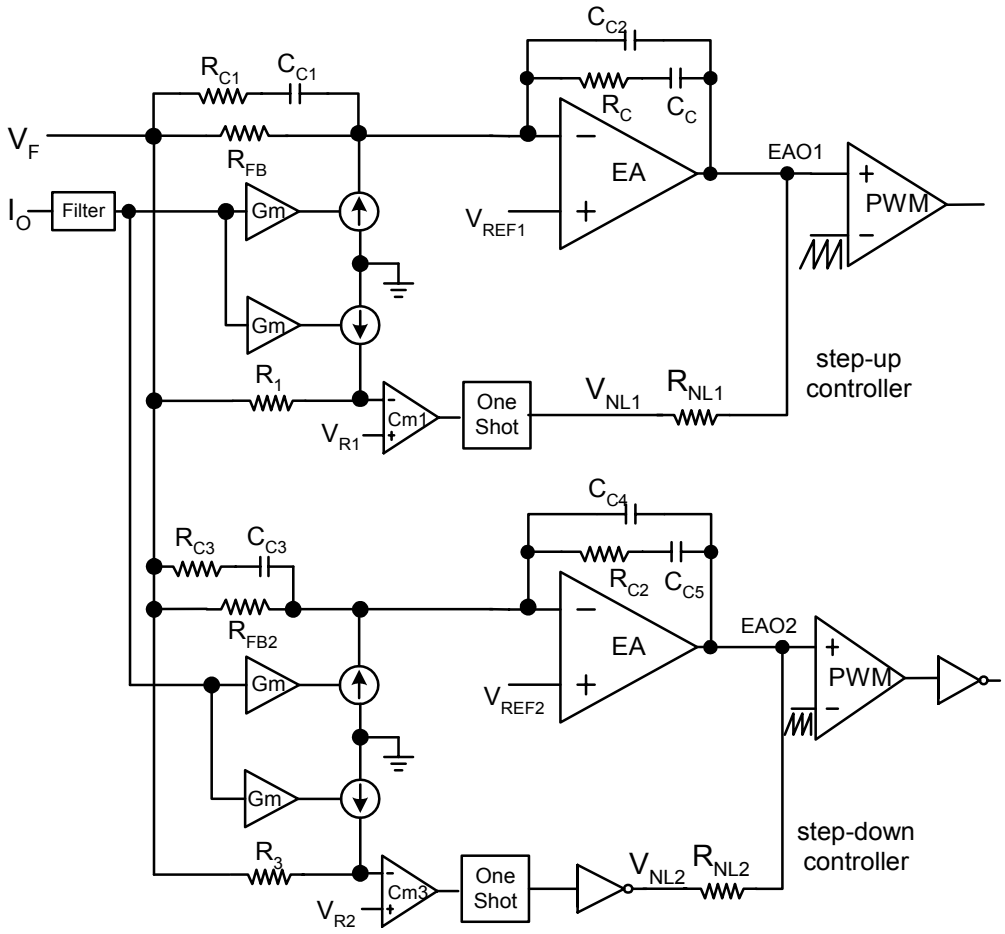


Fig.3.4.17 Control circuit block diagram for the ATVC

Fig.3.4.17 is the combined linear and adaptive nonlinear control for the ATVC to improve the transient response of 3-Ch VR in a desktop motherboard. Dash block 500 is the ATVC step-up controller with adaptive nonlinear control. Dash block 501 is the ATVC step-down controller with adaptive nonlinear control. The current signal Io can be the current signal of VRM filter inductors or the output load current.

3.5 ATVC Experimental Verification

As previously discussed, ATVC is used mainly to suppress the second voltage spike not the first voltage spike. It activates only in transient periods with small leakage inductance in several MHZ operation, which results in high slew rate current injection and high bandwidth for fast transient response. The main VR response time is only about 1~2μs so that the ATVC controller should have a very small delay time to activate from standby mode in steady state to operating mode. The conventional linear PID control method has a large delay time in transient, because it requires enough phase and gain margin for its stability. Combined linear and adaptive nonlinear control for ATVC controllers is used to reduce the delay times for fast transient response shown in Fig.3.4.17. A prototype has been carried out on the Intel desktop motherboard D915Gev to verify the theoretic analysis of ATVC.

Fig.3.5.1 shows the expected ATVC AC improvement definition. The reference in ATVC step-up controller is about 10~15mV less than the output voltage and 10~15mV higher than output voltage in ATVC step-down controller to keep ATVC standby mode in steady state. The definitions of AC load line improvement in transient loads are as follows:

$$\Delta V_1^1 = \Delta V_1 - (10 \sim 15)mV \tag{3-5-1}$$

$$\Delta V_2^1 = \Delta V_2 - (10 \sim 15)mV \tag{3-5-2}$$

$$\Delta V_{LLAC-UP} = (\Delta V^1{}_1 - \Delta V_1^2) / \Delta V^1{}_1 \tag{3-5-3}$$

$$\Delta V_{LLAC-DN} = (\Delta V^1{}_2 - \Delta V_2^2) / \Delta V^1{}_2 \tag{3-5-4}$$

ΔV_1 is the maximum AC voltage spike, and $\Delta V^1{}_1$ is the expected maximum AC voltage spike improvement in step-up load. ΔV_2 is the maximum AC voltage spike, and $\Delta V^1{}_2$ is the expected maximum AC voltage spike improvement in step-down load.

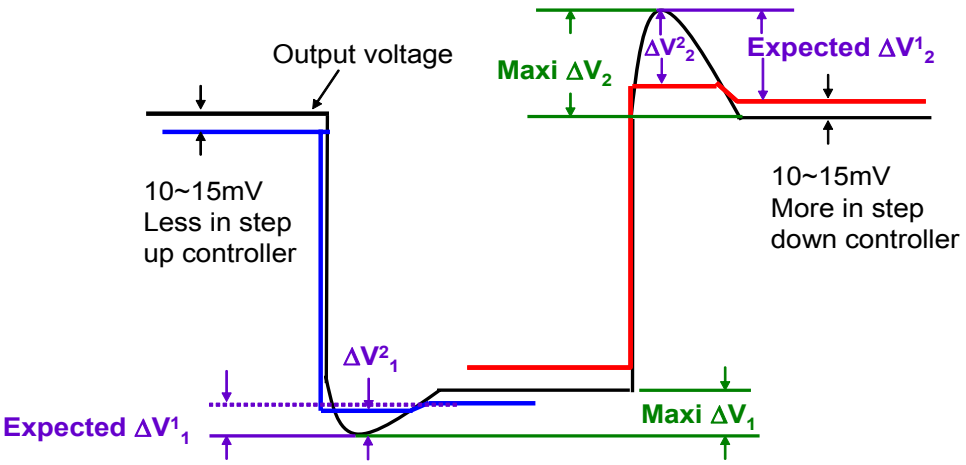


Fig.3.5.1 ATVC AC load line improvement definition

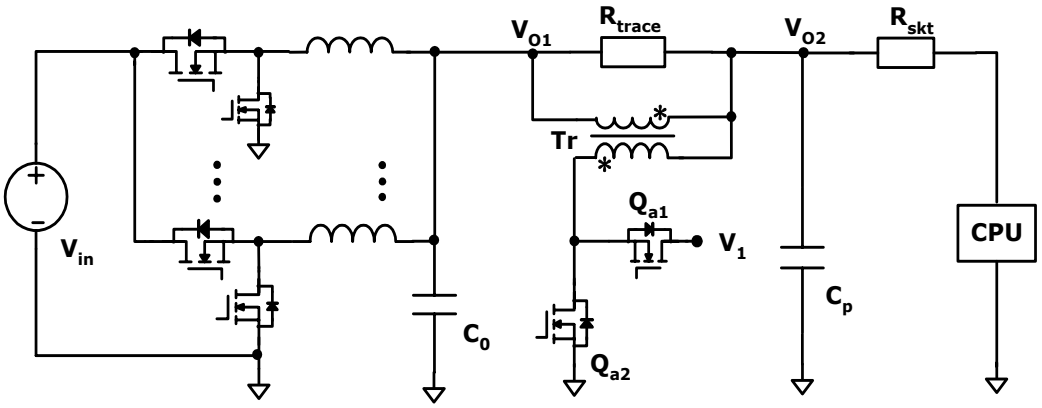


Fig.3.5.2 ATVC implementation circuit with multiphase VR

Fig.3.5.2 shows the ATVC implementation circuit with original 3-Ch VR10.1 on the Intel desktop motherboard D915Gev: 2-Ch VR on the north side with 6 Oscons and 1-Ch VR on the east side with 4 Oscons, 450nH filter inductance per channel. ATVC has been directly in parallel with the motherboard via three connection points: gnd, V_{O1} and V_{O2} as shown in ATVC prototype in Fig.3.5.3. ATVC is mainly used to suppress the second voltage spike, which operates at 1.5MHZ switching frequency and 5V input voltage. ATVC transformer turn ratio is 1:1 with ER11 core. The size of the transformer and two FETs is about 20×20mm^2.

VTT tool [115, 116], shown in Fig.3.5.4, is used to simulate the CPU load with programmable current slew rate (up to 10A/ns), programmable current (up to 120A) and programmable transient load frequency.

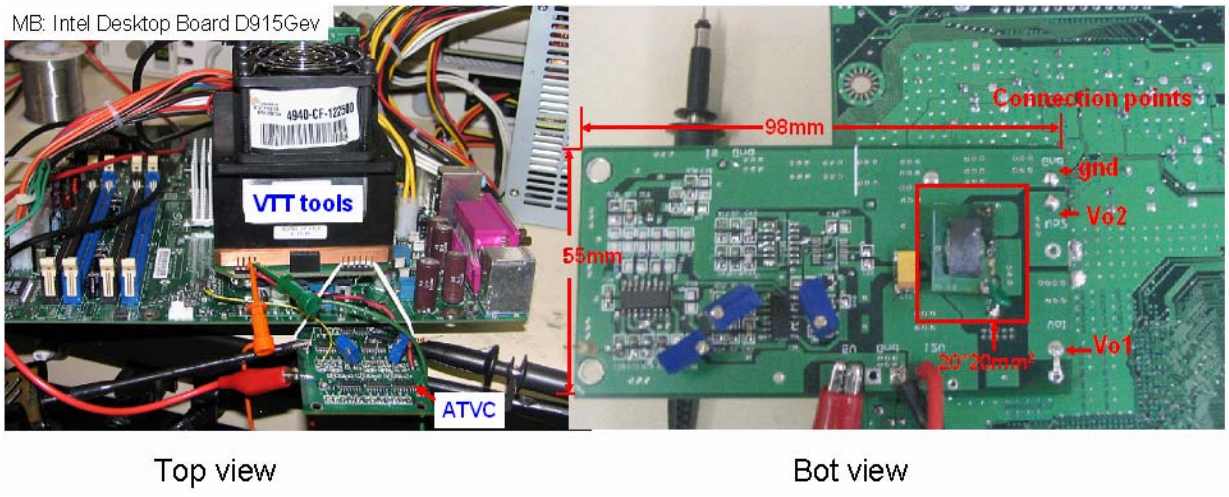


Fig.3.5.3 ATVC experimental prototype setup

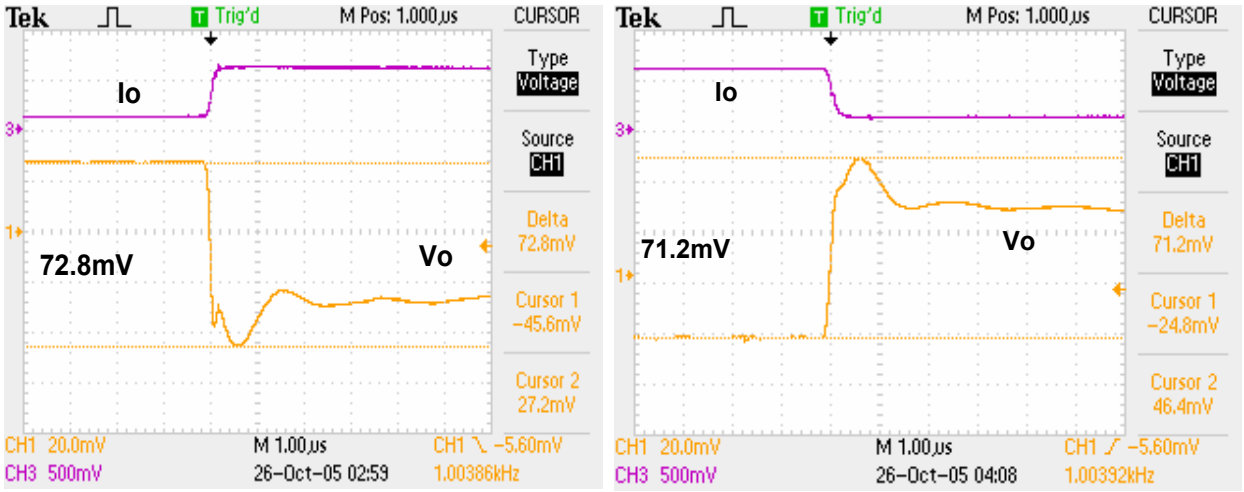


Fig.3.5.4 Baseline transient waveforms @ 5~50A, 550A/µs

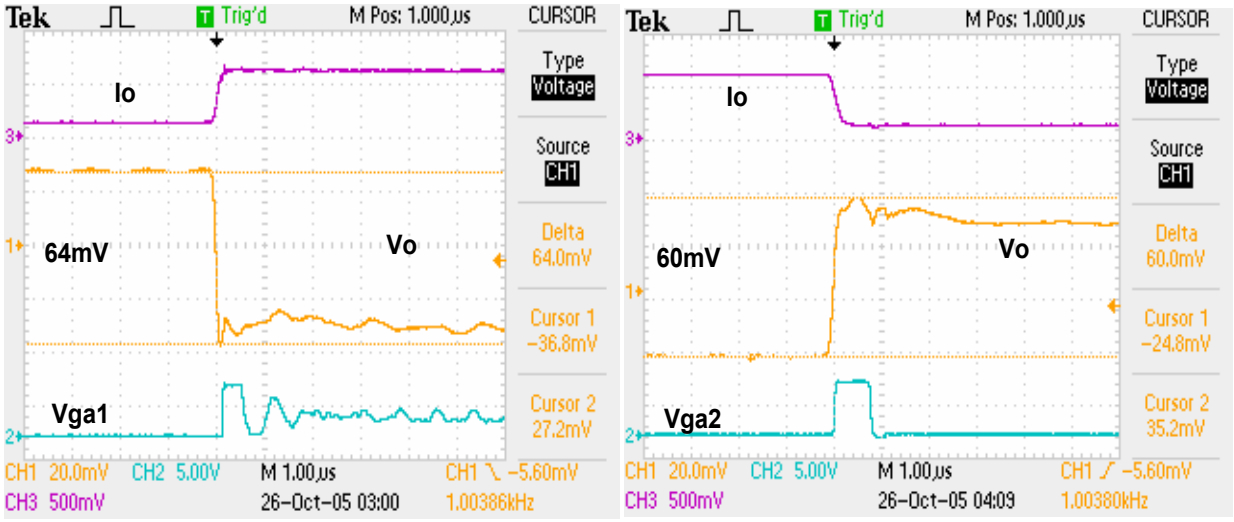


Fig.3.5.5 Improved transient waveforms @ 5~50A, 550A/µs

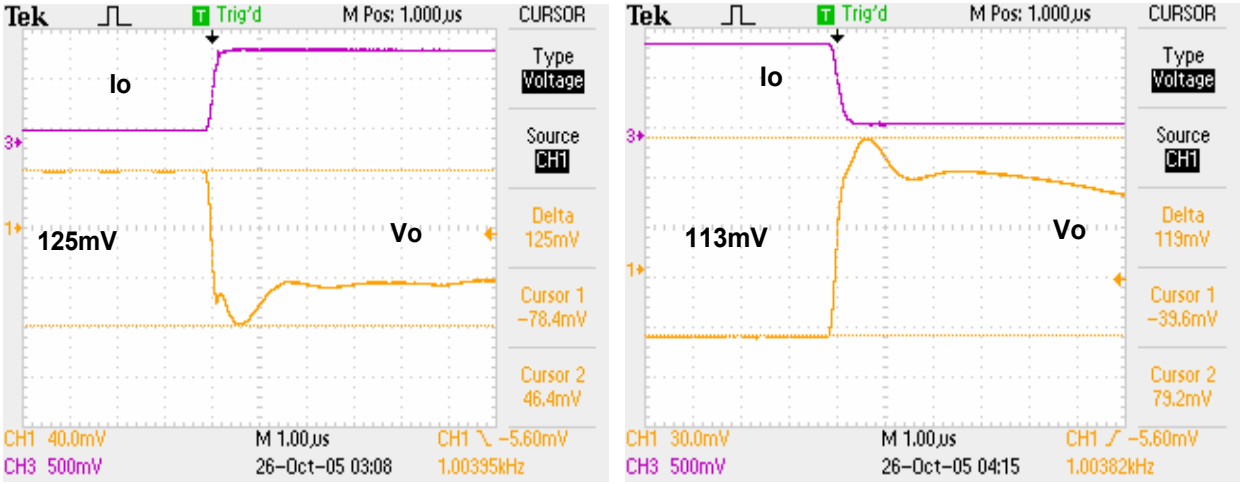


Fig.3.5.6 Baseline transient waveforms @ 5~80A, 550A/µs

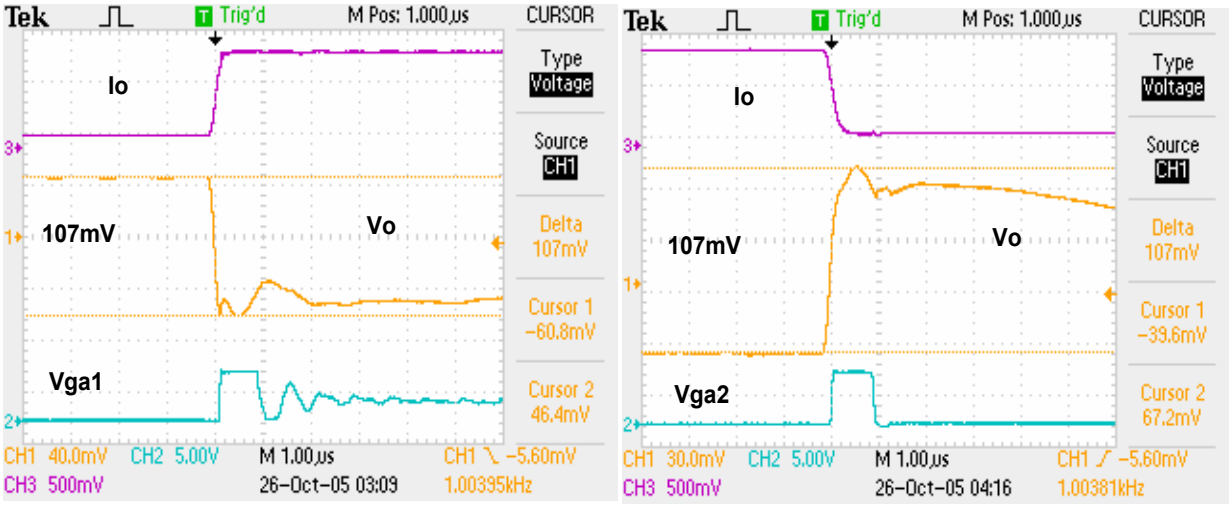


Fig.3.5.7 Improved transient waveforms @ 5~80A, 550A/µs

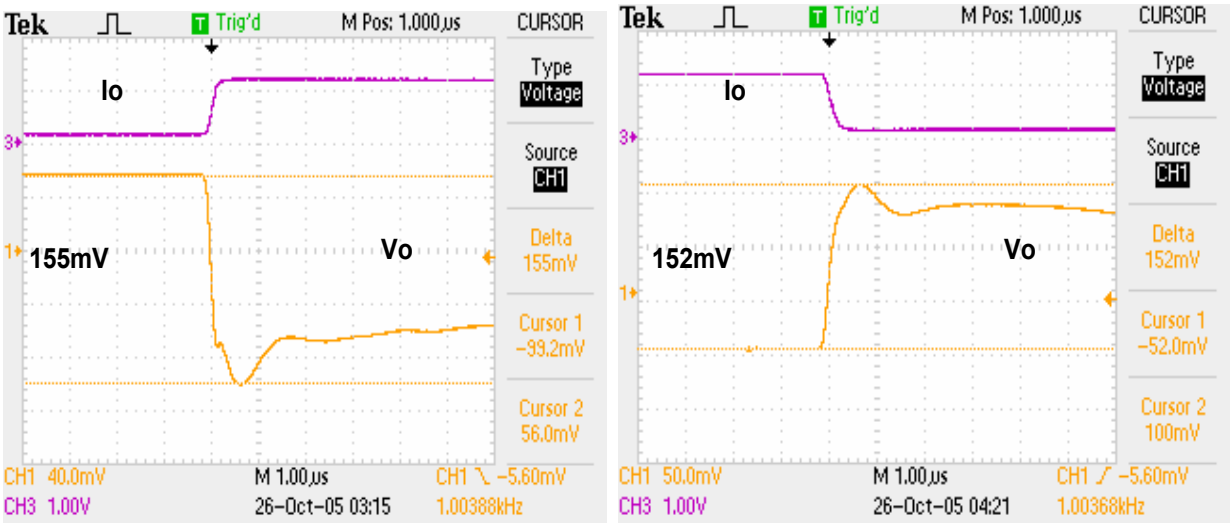


Fig.3.5.8 Baseline transient waveforms @ 5~100A, 550A/µs

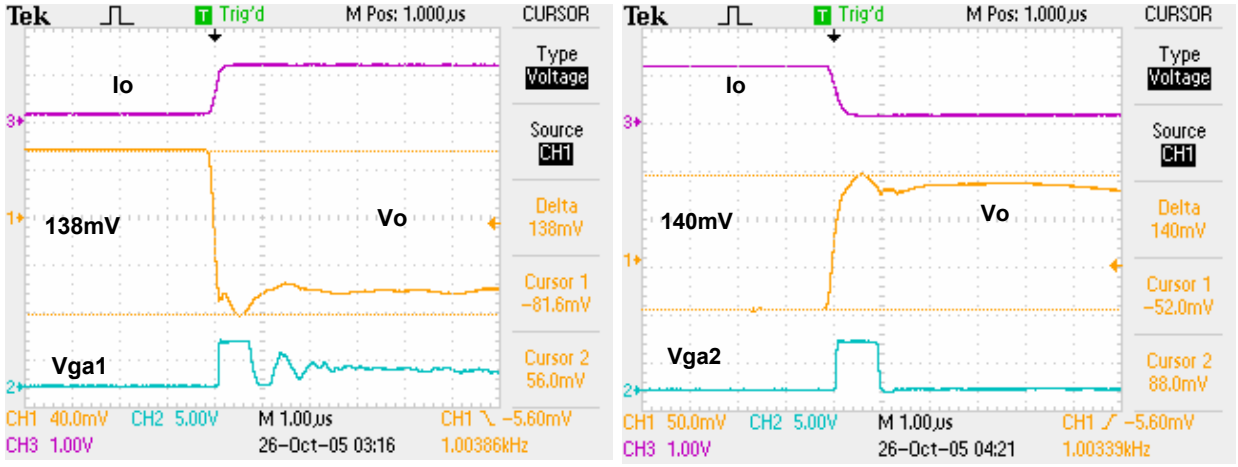


Fig.3.5.9 Improved transient waveforms @ 5~100A, 550A/µs

Fig.3.5.4 shows the baseline 3-Ch VR transient waveforms without ATVC @ 5~50A, 550A/µs with 6 Oscons on the north side and 4 Oscons on the east side. From the waveforms, we can see the second voltage spike dominates at this slew rate transient load. It has 72.8mV voltage drop with 24mV AC voltage drop, and its load line is 1.62mΩ in step-up load. Also, it has 71.2mV voltage spikes in step-down load with 22mV AC voltage spike. It has 1.58mΩ load line.

Fig.3.5.5 shows the improved 3-Ch VR transient waveforms with ATVC @ 5~50A, 550A/µs. The voltage drop is reduced to 64mV (1.42mΩ load line) in step-up load, and the voltage spike is reduced to 60mV (1.33mΩ load line) in step-down load, which accounts for about 64.5 percent of expected AC load line improvement in step-up load and 80.6 percent of expected AC load line improvement in step-down load.

Fig.3.5.6 shows the baseline 3-Ch VR waveforms without ATVC @ 5~80A, 550A/µs with 6 Oscons on the north side and 4 Oscons on the east side. It has 125mV voltage drop with 34mV AC voltage drop, and its load line is 1.67mΩ in step-up load. Also, it has about 113mV (1.59mΩ load line) voltage spikes in step-down load with 29mV AC voltage spike.

Fig.3.5.7 shows the improved 3-Ch VR transient waveforms with ATVC @ 5~80A, 550A/μs. The voltage drop in step-up load is reduced to 107mV, and 107mV (1.43mΩ load line) is in step-down load, which accounts for about 75 percent of expected AC load line improvement in step-up load and 64 percent of expected AC load line improvement in step-down load.

Fig.3.5.8 shows the baseline 3-Ch VR waveforms without ATVC @ 5~100A, 550A/μs with 6 Oscons on the north side and 4 Oscons on the east side. It has about 155mV voltage drop with 39mV AC voltage drop, and its load line is 1.63mΩ in step-up load. Also, it has about 152mV (1.60mΩ load line) voltage spikes in step-down load with 38mV AC voltage spike.

Fig.3.5.9 shows the ATVC improved transient waveforms with @ 5~100A, 550A/μs. The voltage drop in step-up load is reduced to 138mV (1.45mΩ load line) and 140mV (1.47mΩ load line) in step-down load, about 58.1 percent of expected AC load line improvement in step-up load and 44.8 percent of expected AC load line improvement in step-down load.

Table 3.5.1 Tested experimental results of 6×4 Oscons with 1.15mΩ DC load line

VR10.1, VTT Tools, Vo=1.5V, **$R_{LL\text{-}DC}$=1.15mΩ**, ATVC for 2nd voltage spike $R_{LL\text{-}AC}$ improvement ATVC: ER11, **1:1, 5Vin**, 1.5MHz, **6*560uF in north, 4*560uF in east, Intel MB D915Gev**										
Slew rate		5~50A			5A~80A			5A~100A		
		Base	ATVC	Δ_{LLAC}	Base	ATVC	Δ_{LLAC}	Base	ATVC	Δ_{LLAC}
Step up load	180A/us	1.58mΩ	1.33mΩ	80.6%	1.63mΩ	1.33mΩ	**93.7%**	1.57mΩ	1.32mΩ	80.6%
	250A/us	1.58mΩ	1.35mΩ	74.2%	1.63mΩ	1.39mΩ	75%	1.60mΩ	1.37mΩ	74.2%
	550A/us	1.62mΩ	1.42mΩ	64.5%	1.67mΩ	1.43mΩ	75%	1.63mΩ	1.45mΩ	58.1%
Step down load	180A/us	1.53mΩ	1.30mΩ	74.2%	1.51mΩ	1.35mΩ	64%	1.54mΩ	1.39mΩ	51.7%
	250A/us	1.55mΩ	1.32mΩ	74.2%	1.53mΩ	1.36mΩ	68%	1.56mΩ	1.41mΩ	51.7%
	550A/us	1.58mΩ	1.33mΩ	**80.6%**	1.59mΩ	1.43mΩ	64%	1.60mΩ	1.47mΩ	44.8%
Expected LL_{AC} in step up		14mV 0.31mΩ			24mV 0.32mΩ			29mV 0.31mΩ		
Expected LL_{AC} in step down		12mV 0.27mΩ			19mV 0.25mΩ			28mV 0.29mΩ		

Table 3.5.1 shows the VR socket transient load line [17] improvement at different load current step and different slew rate 180A/μs, 250A/μs and 550A/μs. The DC load line is 1.15mΩ with 6 Oscons on the north side and 4 Oscons on the east side with ATVC @ 5Vin and 1:1 transformer on the Intel motherboard D915Gev. The AC load line improvements account for 64 percent of the expected AC load line improvement in step-up loads, and the AC load line improvements are up to 80.6 percent of expected AC load line improvement in step-up loads.

The AC load line improvement is about 0.2~0.25mΩ in 5~50A step-up load (expected 0.31mΩ AC improvement) and 0.18~0.25mΩ in 50~5A step-down load (expected 0.27mΩ AC improvement). The tested AC load line achievement in other different slew rate transient loads takes up most of expected AC load line improvement because 10~15 mV voltage difference is in ATVC controllers in Fig.3.4.17.

Generally, the AC load line improvement in step load is better than that in step-down load because higher slew rate current is injected in step-up load. Also, ATVC has better AC load line improvement at slower slew rate load than in higher slew rate, because the propagation delay time of controller and driver has less impact on ATVC controller response time. Table 3.5.2 shows the 3-Ch VR socket load line improvement with reduced Oscons. The main 3-Ch VR has 1.2mΩ DC load line with 4 Oscons (2 Oscons removed) on the north side and 4 Oscons on the east side. The AC load line improvement is still up to 94.5 percent of the expected AC load line improvement in step-up load, and the AC load line improvements are up to 90.3 percent of the expected AC load line improvement in step-down load.

The AC load line achievement is about 0.27mΩ in 5~50A step-up load (expected 0.36mΩ AC load line improvement) and 0.21~0.28mΩ in 50~5A step-down load (expected

0.31mΩ as load line improvement). Also, the tested AC load line achievement in different slew rate step step currents account for most of the expected AC load line improvement despite the 10~15mV voltage difference in ATVC controller in Fig.3.4.17.

Table 3.5.2 Tested experimental results of 4×4 Oscons with 1.2 mΩ DC load line

VR10.1, VTT Tools, Vo=1.5V, $R_{LL\text{-}DC}$=1.2mΩ, ATVC for 2nd voltage spike $R_{LL\text{-}AC}$ improvement ATVC: ER11, 1:1, 5Vin, 1.5MHz, **4*560uF in north, 4*560uF in east, Intel MB D915Gev**										
Slew rate		5~50A			5A~80A			5A~100A		
		Base	ATVC	Δ_{LLAC}	Base	ATVC	Δ_{LLAC}	Base	ATVC	Δ_{LLAC}
Step up load	180A/us	1.69mΩ	1.42mΩ	75%	1.73mΩ	1.41mΩ	80%	1.75mΩ	1.45mΩ	76.9%
	250A/us	1.71mΩ	1.44mΩ	75%	1.77mΩ	1.44mΩ	82.5%	1.79mΩ	1.42mΩ	94.5%
	550A/us	1.76mΩ	1.48mΩ	77.8%	1.81mΩ	1.53mΩ	70%	1.83mΩ	1.56mΩ	69.2%
	10A/ns	1.8mΩ	1.51mΩ	80.5%	1.84mΩ	1.59mΩ	62.5%	1.87mΩ	1.64mΩ	59%
Step down load	180A/us	1.6mΩ	1.39mΩ	67.7%	1.64mΩ	1.41mΩ	95.8%	1.63mΩ	1.46mΩ	73.9%
	250A/us	1.65mΩ	1.37mΩ	90.3%	1.68mΩ	1.45mΩ	95.8%	1.68mΩ	1.52mΩ	69.6%
	550A/us	1.67mΩ	1.41mΩ	83.9%	1.71mΩ	1.52mΩ	79.1%	1.74mΩ	1.58mΩ	69.6%
	10A/ns	1.69mΩ	1.48mΩ	67.7%	1.75mΩ	1.57mΩ	75%	1.77mΩ	1.65mΩ	47.8%
LL_{AC} in step up	Maxi	26mV 0.58mΩ			40mV 0.53mΩ			46mV 0.48mΩ		
	Expected	16mV 0.36mΩ			30mV 0.4mΩ			36mV 0.39mΩ		
LL_{AC} in step down	Maxi	24mV 0.53mΩ			24mV 0.32mΩ			32mV 0.34mΩ		
	Expected	14mV 0.31mΩ			18mV 0.24mΩ			22mV 0.23mΩ		

Table 3.5.3 shows 3-Ch socket load line tested results with ATVC: 2:1 transformer. 3-Ch VR has 1.44mΩ DC load line with 4 Oscons on the north side and 4 Oscons on the east side. 2:1 turn ratio transformer has large leakage inductance and resistance, which reduce ATVC injected voltage source and deteriorate the AC load line improvement. From the tested results, it is clear that the AC load line improvement is around 0.2mΩ in 7~50A, 0.15mΩ in 7~80A and 0.12mΩ in 7~100A, which is not good compared with 1:1 transformer. With the increasing input voltage from 5V to 10V, the AC load line improvement can achieve 0.3mΩ, over 80 percent of the expected AC load line improvement, but it will increase the ATVC power loss, so there is a trade off between transformer turn ratio and transient response.

Table 3.5.3 Tested experimental results of 4×4 Oscons with 1.44mΩ DC load line

VR10.1, VTT Tools, Vo=1.5V, R_{LL-DC}=1.44mΩ, ATVC for 2nd voltage spike R_{LL-AC} improvement ATVC: ER11, 2:1, 5Vin, 1.5MHz, **4*560uF in north, 4*560uF in east**										
Slew rate		7~50A			7A~80A			7A~100A		
		Base	ATVC	Δ	Base	ATVC	Δ	Base	ATVC	Δ
Step up	250A/us	1.81mΩ	1.62mΩ	40.4%	1.79mΩ	1.64mΩ	34%	1.81mΩ	1.63mΩ	46%
	550A/us	1.84mΩ	1.64mΩ	42.5%	1.89mΩ	1.71mΩ	41%	1.86mΩ	1.74mΩ	30%
	10A/ns	1.86mΩ	1.67mΩ	40.4%	1.9mΩ	1.73mΩ	38.6%	1.89mΩ	1.78mΩ	28%
Step down	250A/us	1.69mΩ	1.51mΩ	78%	1.73mΩ	1.56mΩ	74%	1.72mΩ	1.59mΩ	50%
	550A/us	1.70mΩ	1.56mΩ	60.8%	1.74mΩ	1.64mΩ	43.5%	1.73mΩ	1.68mΩ	19%
	10A/ns	1.73mΩ	1.63mΩ	43.4%	1.77mΩ	1.67mΩ	43.5%	1.75mΩ	1.70mΩ	19%
Expected LL_{AC} in step up		20mV 0.47mΩ			32mV 0.44mΩ			36mV 0.39mΩ		
Expected LL_{AC} in step down		9.6mV 0.23mΩ			16.8mV 0.23mΩ			24mV 0.26mΩ		

7A~100A step up load		Base	ATVC	Δ
ER11, 2:1, 10Vin	250A/us	1.81mΩ	1.48mΩ	85%
	550A/us	1.86mΩ	1.55mΩ	80%
	10A/ns	1.88mΩ	1.58mΩ	77%

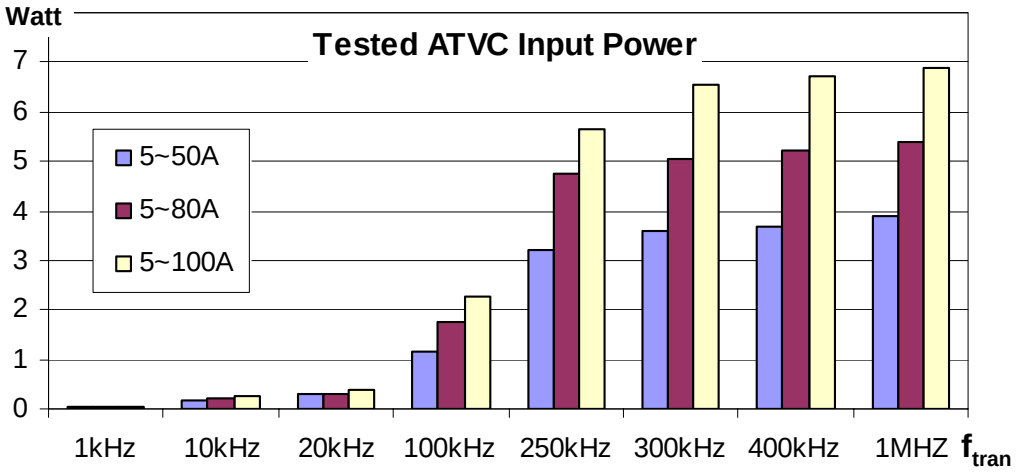


Fig.3.5.10 Tested ATVC input power

Fig.3.5.10 shows tested ATVC input power at different load current step and transient load frequency f_{tran}. From the tested results, the ATVC input power is almost independent on the slew rate, but on the transient load frequency f_{tran}, it is about 7W @ 5~100A, f_{tran}=1 MHZ.

ATVC continuously provides the current to the load when the transient load frequency f_{tran} is higher than 300 kHz.

The main 3-Ch VR in Fig.3.2.7 can achieve around 86~88 percent efficiency in steady state, and it achieves better socket transient load line with very small increased power losses by using ATVC as shown in Fig.3.5.10.

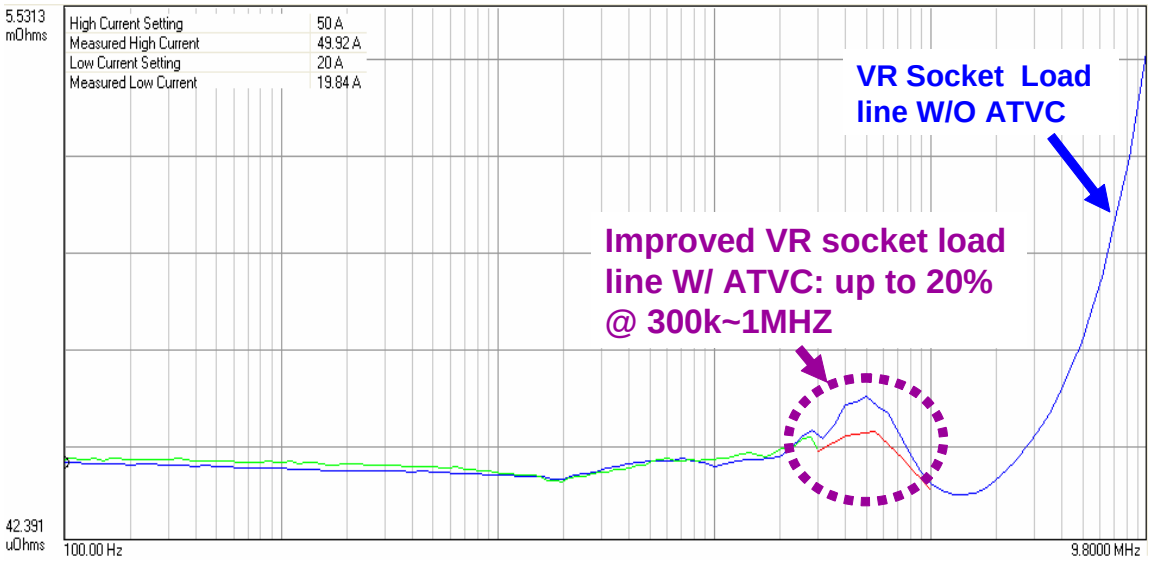


Fig.3.5.11 Tested socket load line improvement of Intel motherboard

Fig.3.5.11 shows the tested socket load line improvement of Intel motherboard D915Gev. It is clear that socket load line is improved by 20% between 300 kHz and 1 MHZ.

Fig.3.5.12 shows the average injected transient voltage by ATVC transformer. The obvious first voltage pulse in transient waveforms is due to the adaptive nonlinear control with small delay time.

Fig.3.5.13 shows that ATVC in CCM has 245 kHz bandwidth with 50^{o}C phase margin with 1.5MHZ, 2:1 transformer.

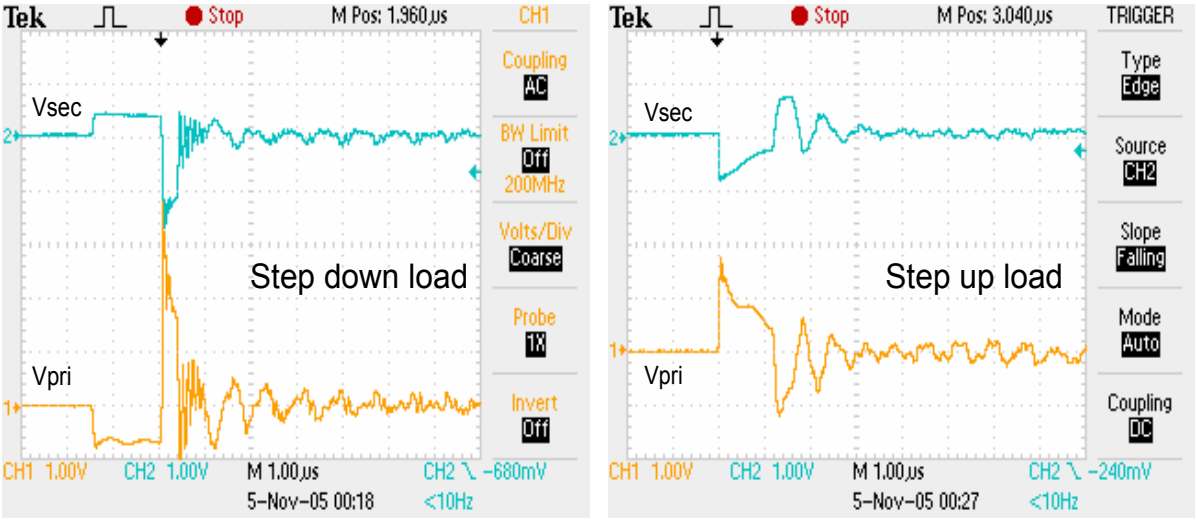


Fig.3.5.12 Average injected transient voltage waveforms

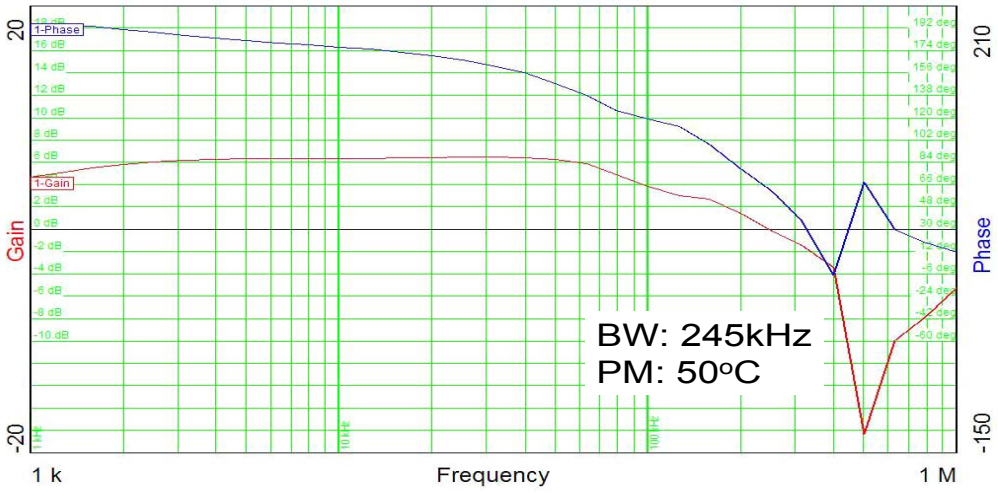


Fig.3.5.13 Tested ATVC bode-plot in CCM

3.6 ATVC Summary

There are two voltage spikes that occur in high slew rate CPU current. The first voltage spike is related with ESR, ESL of filter capacitor and socket and PCB layout. The only way to suppress the first voltage spike is to optimize the combination of different types of parallel capacitors and with careful PCB layout. But motherboard space limits the possibility of adding more capacitors. Fortunately, the second voltage spike that is related to the energy stored in VR filter inductance and close loop design will dominate under 800A/μs. Higher bandwidth contributes to the smaller second voltage spikes. High switching operation in main VR helps to reduce filter inductance for high bandwidth and fast transient response, but it deteriorates the efficiency. The big challenge is to reduce the second voltage spike with small extra power loss in a simple way.

The conventional active current compensator only injects high slew rate current in step-up load and absorbs the voltage overshoot in step-down load by linear mode or switching mode. The problem in current compensators is the high current stresses resulting in high conduction loss in linear mode current compensator or high switching loss in switching mode current compensator, and also, it is very difficult to eliminate the impact of resistance and inductance of PCB layout and socket on voltage spikes.

The two-stage approach regulates the intermediate bus voltage by the first stage converter operating in relative low switching frequency, and the second stage converter operates in several MHZ with small filter inductance to achieve high bandwidth for fast transient response. The challenge for two-stage approach is how to improve the efficiency because it is a cascade system.

Active transient voltage compensator is proposed to reduce the power loss and inject higher slew rate current in step-up load and recover energy in step-down load. ATVC only activates to handle the AC current in transient periods with several MHZ operations to reduce the filter inductance for fast transient response, and the main VR can operate in low switching frequency for better efficiency. With introduction of N: 1 turn ratio transformer, ATVC reduces the current stresses by the factor of 1+N and injects 1+N times higher slew rate than that in conventional current compensators with the same inductance. At the same time, ATVC can eliminate the influence of PCB layout and socket on the output voltage spikes because of its injected voltage source. Furthermore, ATVC can reduce the number of main VR bulk capacitors; because the close loop output impedance of main VR is the internal impedance of ATVC, which can be largely reduced by close loop control.

ATVC transformer design is very important for ATVC performance. The transformer leakage inductance and turn ratio determines the injected current slew rate and the ATVC power losses. Also, the resistance of winding will reduce ATVC injected voltage source due to its voltage drop on the resistance. Maxwell 3D magnetic simulation has been carried out to optimize the transformer design from the power loss, leakage inductance and core size.

Linear compensation network has a large delay time, because it requires enough phase and gain margin for the converter stability, so the transient response is not good as expected. A large delay time in the compensation network and propagation delay will degrade or even kill the ATVC performance. Combined linear and adaptive nonlinear control is proposed to reduce the delay time for fast transient. Adaptive nonlinear control only activates in transient periods to inject one pulse nonlinear signal by one shot circuit with very small delay time, and there is no stability problem in nonlinear control due to one pulse injection. Finally, it simplifies the design

of the linear compensation network design. In VRM9.0 experimental tested results, adaptive nonlinear control reduces the response time from 2.4μs in linear compensation network to 0.2μs with combined linear and adaptive nonlinear control.

In ATVC experimental prototype, it achieves about 0.3mΩ AC load line improvement, which accounts for up to 90 percent of expected AC load line improvement with a small extra power loss in ATVC, which has 1:1 transformer and 5Vin. Generally, the AC load line improvement in step load is better than that in step-down load at load condition, because higher injected current slew rate occurs in step-up load rather than in step-down load. Also, ATVC has better improvement at slower slew rate load because the propagation delay time of the controller and the driver has less impact on the ATVC controller than on higher slew rate condition.

High turn ratio transformer can reduce ATVC current stress, but it has large leakage inductance and resistance, which decrease the injected transient voltage source leading to bad performance. Increasing ATVC input voltage helps to increase the injected transient voltage source; in other words, trade offs are between the ATVC input voltage V1 and different turn ratio transformers.

CHAPTER FOUR: TRASIENT IMPROVEMENT IN ISOLATED DC-DC CONVERTER

As we all know, the converter current slew rate is determined by its equivalent inductance and the applied voltage. The unbalanced current between load and inductor will be provided by filter capacitors. As discussed in Chapter 1, ESR and ESL of filter capacitors play a very important role in the voltage spikes at high slew rate load [53]. Higher output current slew rate results in higher first output voltage spikes, and the second voltage is mainly determined by the energy stored in filter inductor and is limited by control close-loop bandwidth. High switching frequency operation is a very common way to reduce the filter and extend the close-loop bandwidth for higher slew rate current; however, it deteriorates the efficiency sharply.

The first voltage spike is mainly determined by output current slew rate, ESR of filter capacitors and is almost independent on controller design. The simple, direct way to reduce the first transient voltage spike is to parallel more bulk capacitors or combine different capacitors to reduce its ESR, but it is constrained by the size and increasing cost.

In recent years, many efforts have been put into transient improvement [14-51] [63-69], mainly focusing on VRM. Few works are put into wide input range isolated DC-DC converter. For most isolated DC-DC converter commercial products, their current slew rate is always less than 10A/μs so the dominant voltage spike is the second voltage spike, which relates to the bandwidth of the isolated DC-DC converter and is mainly limited by filter LC delay time, compensation network delay time and propagation delay time that includes gate driving delay time, signal sampling delay time and control IC propagation time. Generally, the filter LC and compensation network delay times are the key delay time, and how to reduce those two delay times for fast transient while keeping high efficiency is the main topic in this chapter.

4.1 Proposed Current Injection in Isolated DC-DC Converter

The galvanic isolation is required in isolated DC-DC converter. Usually the power transformer is used for power isolation, and optocoupler is used for signal isolation in the primary side control or signal transformer is used for primary side driving signals isolated from the secondary side control.

Fig.4.1.1 is the general schematics of isolated DC-DC converter with primary side control. The primary topology can be half-bridge, full-bridge, forward, or flyback converters, and secondary rectifier can be current doubler, full-wave rectifier or single-wave rectifier.

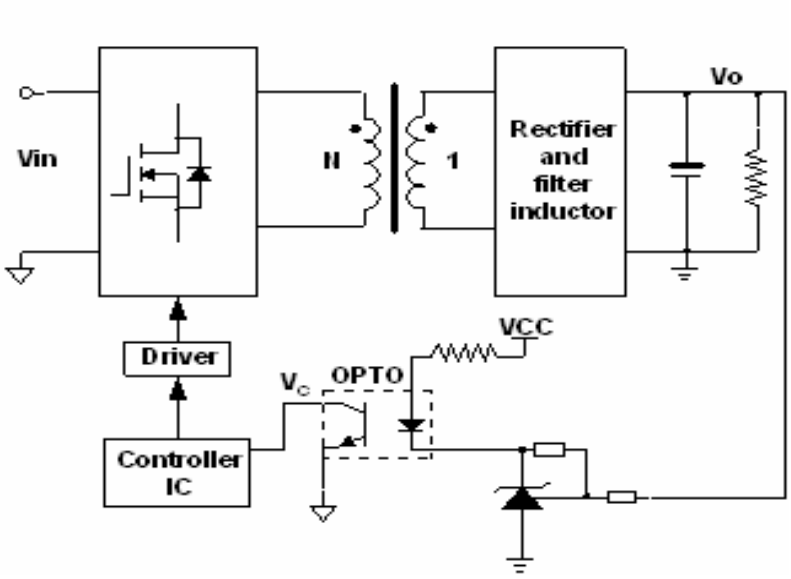


Fig. 4.1.1 Isolated DC-DC converter with primary side control

Fig.4.1.2 shows the performance characteristics of optocoupler. From its frequency characteristic curves, it is clear that it has a low frequency pole, which commonly occurrs around 10~30 kHz. This low frequency pole not only complicates the feedback control loop design, but also slows down the transient response. Moreover, the performance of optocoupler varies with ambient temperature and load current, and enough phase and gain margins should be considered

in different operating environments for converter stability, which deteriorates the transient response.

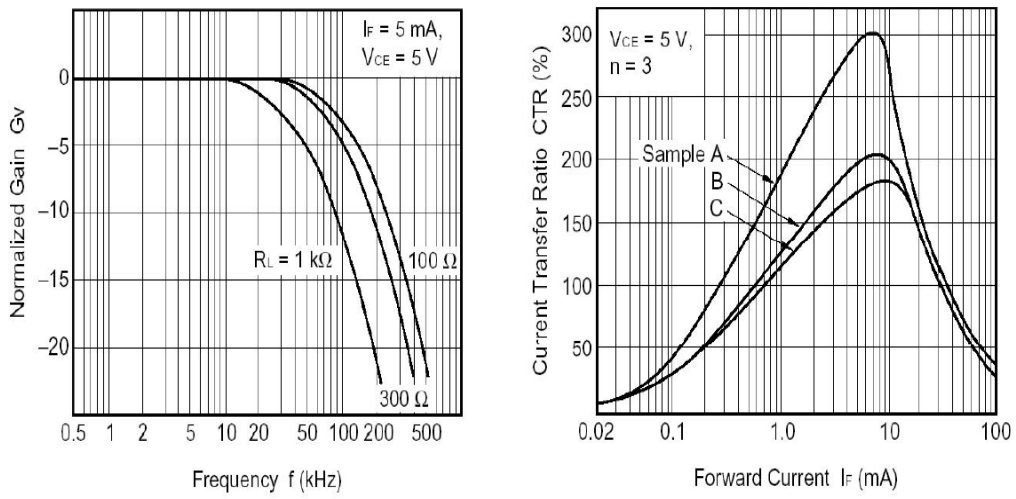


Fig.4.1.2 Optocoupler performance characteristics

Secondary side control can remove the optocoupler, allowing for fast transient response. Unfortunately, it needs an extra startup circuit to power the secondary side controller; otherwise there will be no operation. Startup circuit design is complex and costly [42].

High frequency operation in the main converter usually benefits higher bandwidth for better transient response, but it deteriorates the efficiency. At the same time, leakage inductance of the power transformer causes large duty loss and long current commutation time, especially in high frequency and in wide range input voltage applications. So simply increasing the switching frequency is not a suitable way to improve isolated DC-DC converter transient response.

A switching mode current injection circuit is presented in this section, which is only activated in transient periods by injecting high slew rate current in step-up load and recovering energy in step-down load. The switching mode current injection circuit mainly handles the transient current. Thus, the main converter can be optimized in low switching frequency for

better efficiency. Furthermore, no optocoupler is on the secondary side control for the current injection circuit, which benefits the transient response and close loop design.

4.1.1 Proposed Switching Mode Current Injection Circuit

There are two current injection circuits available on the secondary side to improve transient response: linear mode and switching mode current injection. Fig.4.1.3 shows the power loss estimation of linear mode and switching mode current injection circuit. Linear mode current injection circuit has large conduction loss because of high voltage drop across switches, so it is not suitable for low output voltage or high output current conditions.

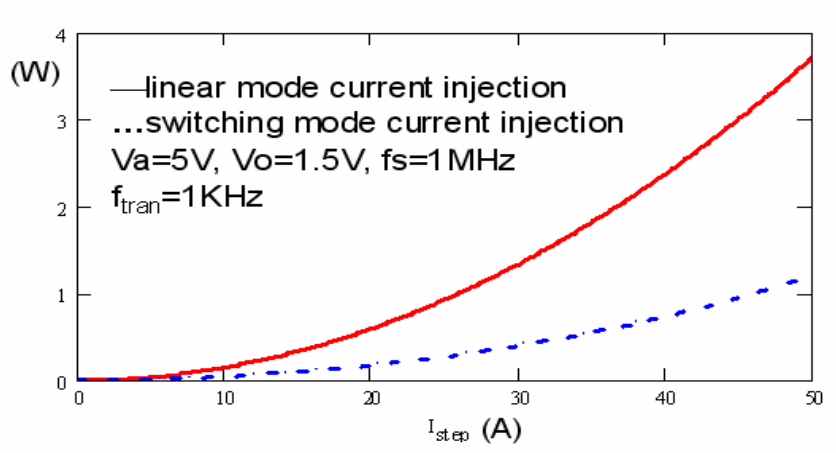


Fig.4.1.3 Linear and switching mode current injection power loss estimation

The proposed isolated DC-DC converter with switching mode current injection circuit as shown in Fig.4.1.4 is composed of a main converter and an extra switching mode current injection circuit operating at several MHZ for small filter inductance.

The voltage mode controller combined with logic circuit is used to keep the switching mode current injection circuit off in steady state and activate only in transient loads. Fig.4.1.5

shows the operation waveforms with switching mode current injection circuit. V_{LT} is the lower threshold voltage in step-up load and V_{HT} is the upper threshold voltage in step-down load.

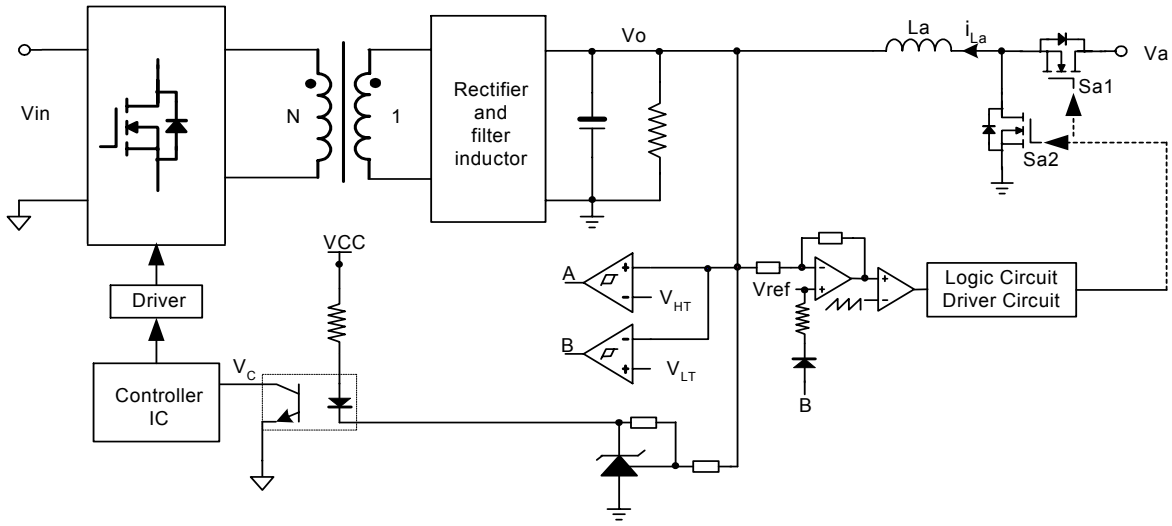


Fig.4.1.4 Isolated DC-DC converter with switching mode current injection circuit

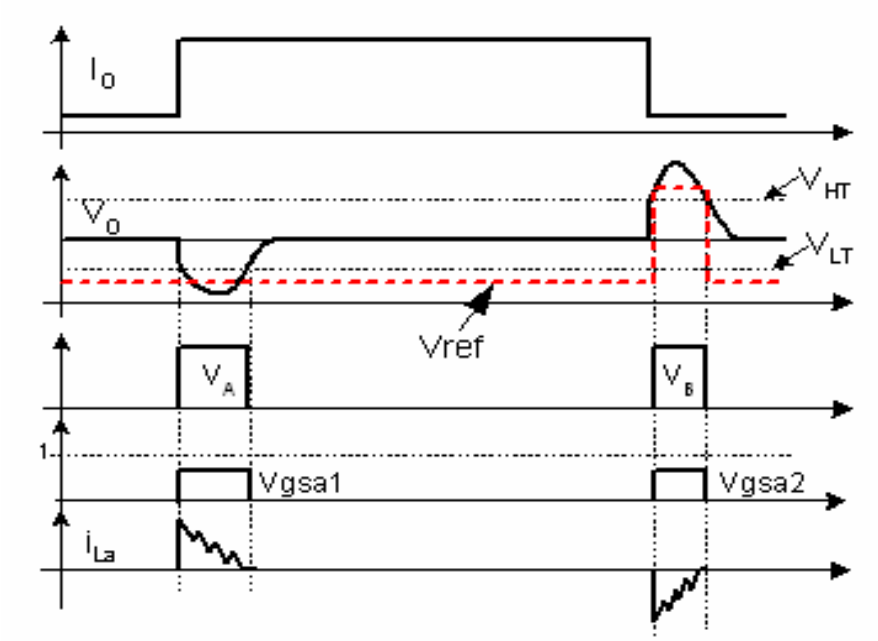


Fig.4.1.5 Operation waveforms with current injection circuit

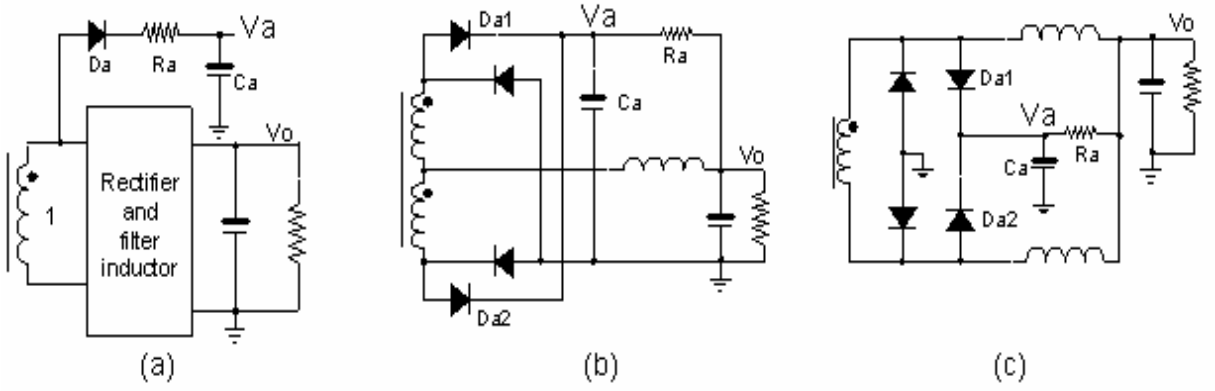


Fig.4.1.6 Three types of circuits for Va in current injection circuit

There are three main modes in the switching mode current injection circuit: step-up load mode, steady-state mode and step-down load mode. Detailed operating waveforms are shown in Fig.4.1.5. In steady-state mode, the switching mode current injection circuit stands by because it blocks the driver signal when logic circuit is V_A=V_B=0. In step-up load mode, the current injection circuit activates as a buck converter by controlling Sa1 to supply higher slew rate current to load until output voltage Vo is back into V_{LT}. Sa2 can be operated in synchronous rectifier for small conduction loss.

$$\frac{di_{La1}}{dt} = \frac{Va - Vo}{La} \tag{4-1-1}$$

In step-down load mode, current injection circuit serves as a boost converter by controlling Sa2 to recover energy to its input voltage Va until output voltage Vo returns back below V_{HT}. Also, Sa1 can be operated in synchronous rectifier for small conduction loss.

$$\frac{di_{La2}}{dt} = \frac{Vo}{La} \tag{4-1-2}$$

From the above equations, it is clear that the current slew rate of the switching mode current injection circuit is determined by its filter inductance. Lower filter inductance in several MHZ operations lead to high current slew rate injection.

In switching mode current injection circuit, input voltage Va can be generated with a secondary side winding or extra winding as shown in Fig.4.1.6 (a). Snubber circuits for full-wave rectifier or current doubler also can used to generate voltage source Va while clamping the voltage of diode rectifiers or synchronous rectifiers in Fig.4.1.6 (b) and (c); it can also come from other kinds of snubbers or circuits on the secondary side.

4.1.2 Experimental Verification

An experimental prototype was carried out to verify the theoretic analysis. The main converter topology is resonant reset forward, 36~75V input, 1.5V/15A output, 300 kHz and output filter inductance, of 1μH.

Fig.4.1.7 shows the Vds and Vgs waveforms of resonant reset forward converter. Switching mode current injection circuit has 1MHZ operation with 100nH filter inductance, and its input voltage Va is shown in Fig.4.1.6 (a), which is about 4V~8V at full range input conditions.

Fig.4.1.8 shows the main converter transient waveforms without current injection circuit @1~10A, 10A/μs, which has 1.23V voltage drop in step-up load and 0.56V voltage spike in step-down load.

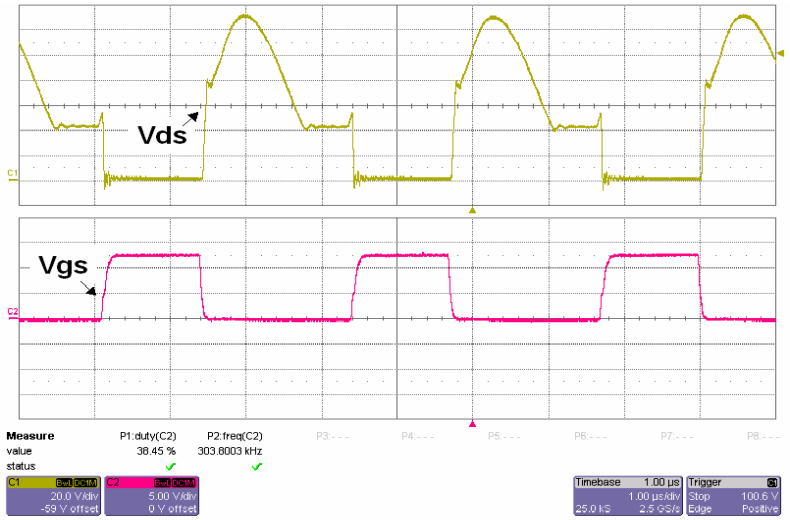


Fig.4.1.7 Vds and Vgs of the resonant reset forward converter

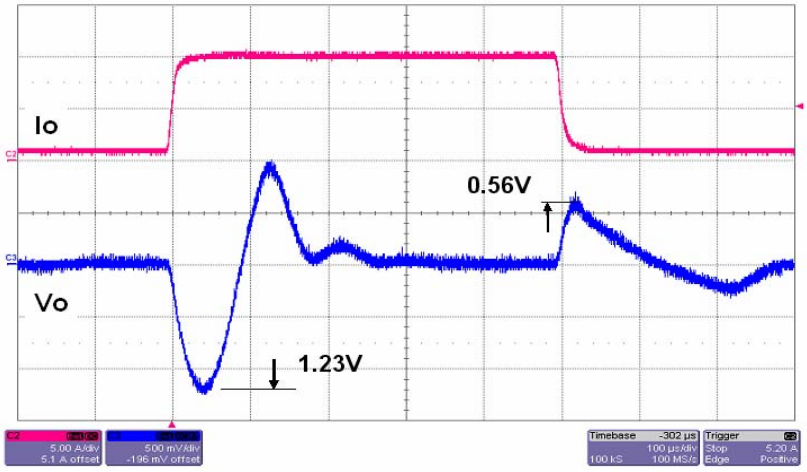


Fig.4.1.8 Output transient response waveform of the isolated DC-DC converter

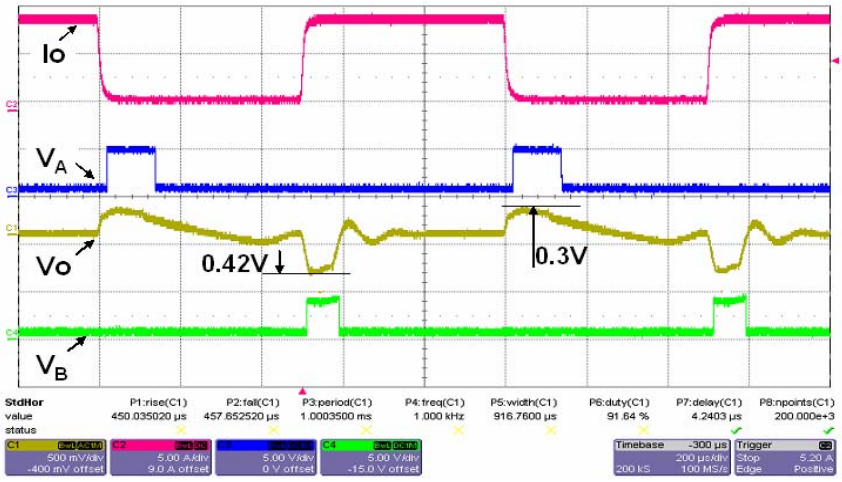


Fig.4.1.9 Improved transient response waveforms with the current injection circuit

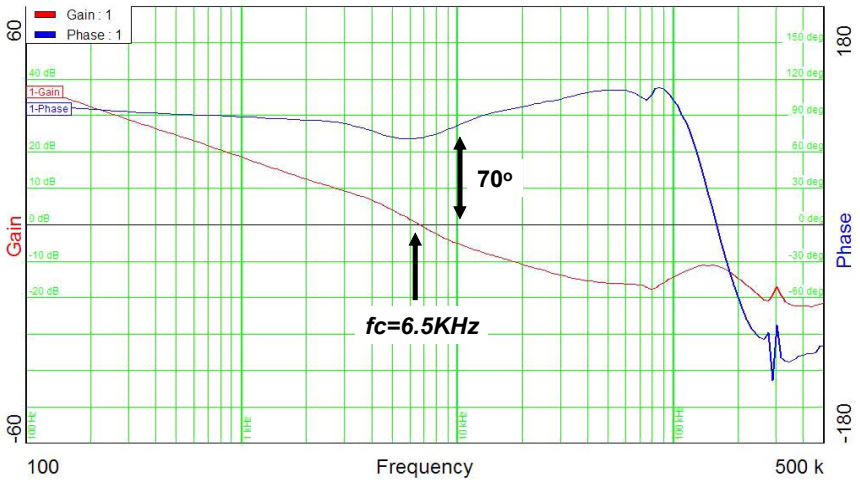


Fig.4.1.10 Main converter close-loop bode-plot

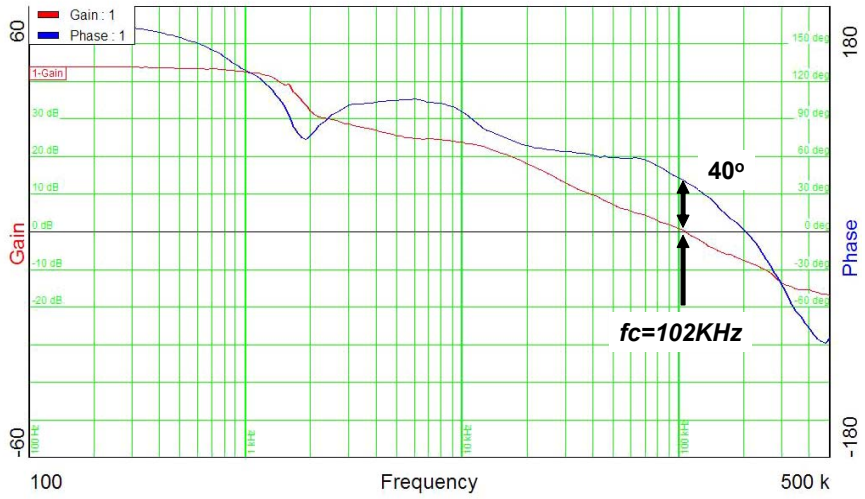


Fig.4.1.11 Close-loop bode-plot of switching mode current injection circuit

Fig.4.1.9 shows the improved transient waveforms in step-up load at the same transient condition, which reduces the voltage from 1.23V to 0.42V in step-up load and from 0.56V to 0.3V in step-down load by using the switching mode current injection circuit.

Fig.4.1.10 shows the close loop bandwidth of the main converter without current injection circuit is around 6.5 kHz with 70^{o} phase margin, and low bandwidth results in bad transient response.

Fig.4.1.11 shows the close loop bandwidth of switching mode current injection circuit in CCM is around 102 kHz with 40^{o} phase margin, which leads to improved transient response.

In the main isolated DC-DC converter, its close loop bandwidth is mainly limited by filter LC, the controller and the optocoupler, and the transient response can improve by optimizing the unity gain bandwidth but has limitations such as optocouple and converter stability requirements. Switching mode current injection circuit in MHZ operation is proposed mainly to handle the transient current in secondary side for better transient response without optocouple in feedback control. At the same time, the main converter can be optimized at

relatively low frequency operation, which only needs to handle the DC current and benefits from efficiency improvement.

4.2 Proposed Novel Control for Isolated Two-Stage Converter

4.2.1 Limitation in Conventional Two-Stage Converter

Fig.4.2.1 shows the conventional isolated two-stage converter with 0.5 duty cycle [74-75]. The first stage synchronous buck converter regulates a constant voltage bus V_b, and the second stage half-bridge converter with fixed 0.5 duty cycle operates just as a DC transformer, which has the following features:

1) Easy ZVS in primary side in second stage due to 0.5 duty cycle operation;
2) Optimized synchronous rectification design with low voltage stress and better FETs;
3) Relatively low frequency operation in first stage for better efficiency.

However, the two-stage converter transient response mainly depends on the close loop bandwidth of the first stage synchronous buck, because the second stage has no capability of voltage regulation. High switching frequency operation in the first stage reduces the output filter for better transient response, but it decreases the total efficiency. There is a tradeoff with efficiency and transient response in a two-stage converter.

The DC gain of conventional two-stage converter with 0.5 duty cycle in CCM is obtained:

$$M = \frac{Vo}{V_{in}} = 0.25nD \tag{4-2-1}$$

$$\frac{dM}{dD} = 0.25n \tag{4-2-2}$$

D is the duty cycle in the first stage converter and n is transformer turn ratio in the second stage converter with 0.5 duty cycle. From Equation (4-2-2), it is clear that the gain slew rate is only related to the transformer turn ratio, which means that fast dynamic response needs a large duty cycle margin. In other words, fast dynamic response requirement in common 36~75V input converters requires a converter operating in small duty ratio, so it has enough duty cycle margin to response the transient load, causing low total efficiency due to increased switching and conduction losses related to small duty cycle [74].

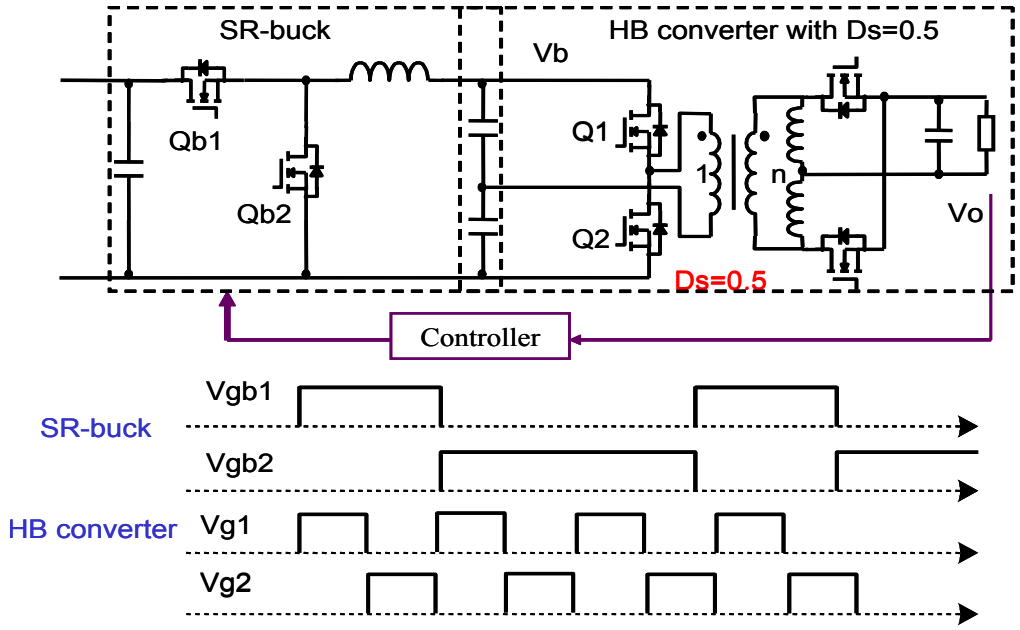


Fig.4.2.1 Synchronous buck and 0.5 duty cycle HB converter

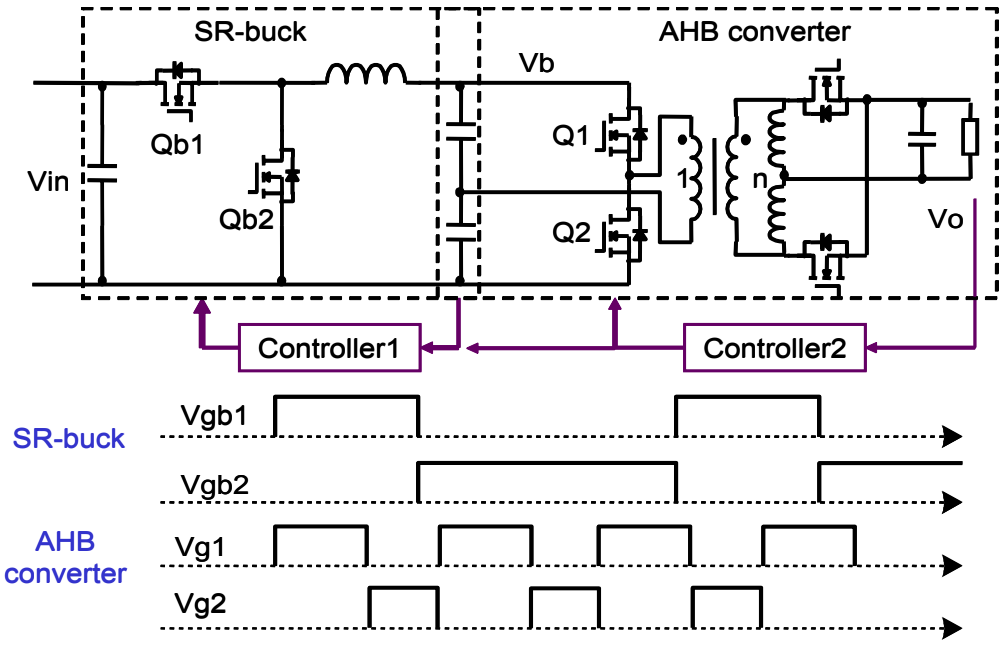


Fig.4.2.2 Synchronous buck and AHB converter

Fig.4.2.2 shows the conventional two-stage DC-DC converter with asymmetrical half-bridge converter (AHB) in second stage [78]. The first stage operates in low switching frequency to roughly regulate the intermediate bus voltage V_b with low bandwidth controller 1. Generally, V_b is selected around 20V so that 30V FETs and small turn ratio transformer can be used in the second stage for simple layout. High switching frequency in second stage AHB converter is used to precisely regulate output voltage V_O with higher bandwidth controller 2. However, the AHB converter operates in large duty cycle, which easily achieves natural ZVS in primary side by using the energy stored in the transformer leakage inductance and parasitic inductance, and it also reduces the output filter.

The DC gain of conventional two-stage DC-DC converter with AHB in CCM is obtained,

$$M = \frac{Vo}{V_{in}} = D_1 D_2 (1 - D_2) n \qquad (4\text{-}2\text{-}1)$$

$$\frac{dM}{dD_2} = D_1(1-2D_2)n \tag{4-2-2}$$

D_1 is the duty cycle of the first stage synchronous buck converter and D_2 is the duty cycle of the second stage AHB converter. The transient response mainly depends on the bandwidth of the second stage AHB converter because the first stage synchronous buck converter operates at low switching frequency for better efficiency. However, the AHB converter has to operate in large duty cycle for better efficiency, which deteriorates the transient response.

From Equations (4-2-1) and (4-2-2), it is clear that the transient response in a conventional two-stage converter with AHB is also limited by the efficiency, which is the same as with the conventional two-stage converter with 0.5 duty cycle.

4.2.2 Novel Control for Two-Stage DC-DC Converter

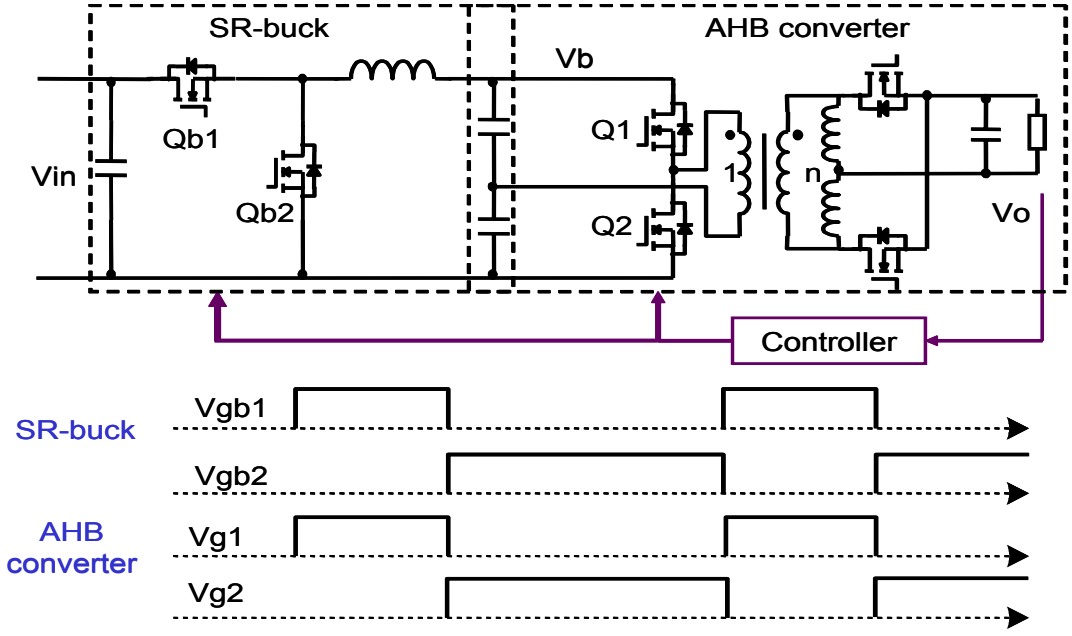


Fig.4.2.3 Proposed novel control for a two-stage DC-DC converter

Unlike conventional control methods in two-stage converters, the novel control has the same driver signal for synchronous buck converter and half-bridge converter, as shown in Fig.4.2.3. Q_{b1} and Q_1 have the same driving signal and Q_{b2} and Q_2 have the same driving signal. Only one simple controller is required for the two-stage DC-DC converter.

The DC gain of the two-stage converter with novel control in CCM is obtained with:

$$M = \frac{Vo}{V_{in}} = nD^2(1-D) \tag{4-2-3}$$

$$\frac{dM}{dD} = nD(2-3D) \tag{4-2-4}$$

We also can easily obtain the maximum duty cycle and DC gain as follows:

$$D_{\max} = 0.66 \tag{4-2-5}$$

$$M_{\max} = \frac{4}{27}n \approx 0.15n \tag{4-2-6}$$

Normalized DC gain of two-stage DC-DC converter with novel control is shown in Fig.4.2.4. The two-stage isolated DC-DC converter with novel control can operate at maximum duty cycle D_{max}, up to 0.66. Therefore, it is suitable for low voltage, high current conditions because of large voltage step-down ratio.

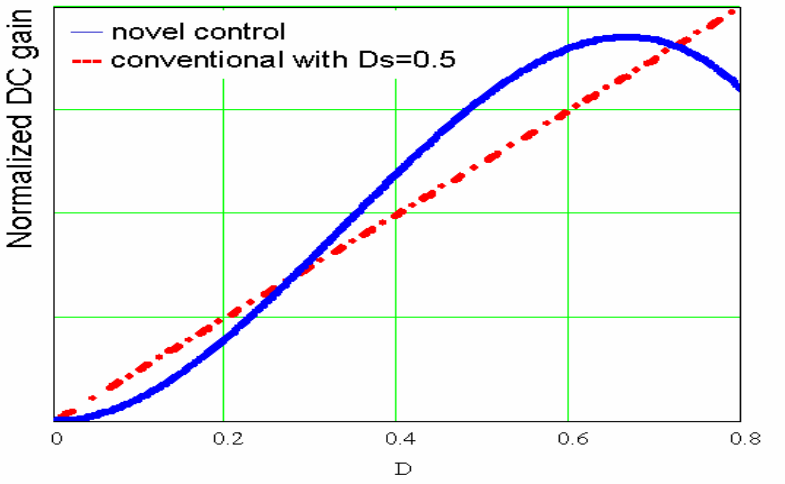


Fig.4.2.4 Normalized gain of a two-stage converter with novel control

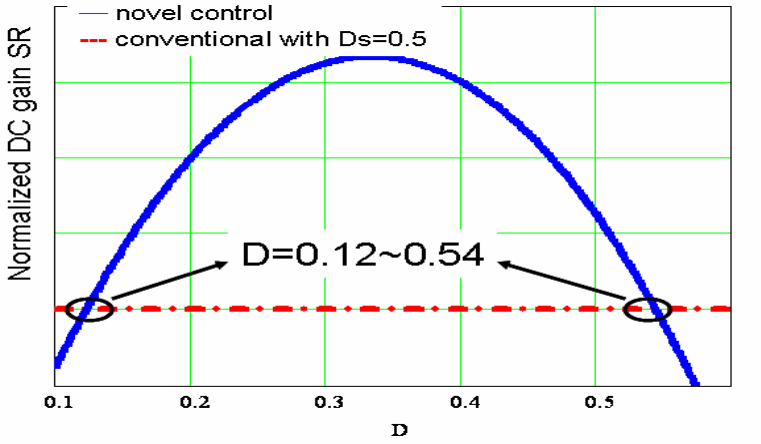


Fig.4.2.5 Normalized gain slew rate of the two-stage converter with novel control

Normalized DC gain slew rate of the two-stage DC-DC converter with novel control method is shown in Fig.4.2.5. It is clear that the slew rate of gain in novel control is greater than in conventional control within D=0.12~0.5, which means that novel control has faster dynamic response than in conventional control at the same switching frequency.

Table 4.2 Two design cases for the two-stage DC-DC converter

36~75V input, 1V/20A output		
	Conventional control	Same control
Transformer turn ratio (n=ns:np)	5:1	4:1
Bus voltage Vb	20V	19~22V
Duty ratio	Buck:0.27~0.55 HB:0.5	0.31~0.54
Gain	0.25nD	$nD^2(1-D)$
Slew rate of gain	0.25n	n(2-3D)
Maximum SR voltage stress	2V	3.5V

Table 4.2 shows the comparison of two-stage DC-DC converter with different controls. Conventional control method has 20V intermediate voltage bus and around 2V maximum voltage stress on the secondary side synchronous rectifier in second stage converter. Novel control has an unfixed intermediate bus voltage, which is about 19~22V at 0.3~0.54 duty cycle. In both cases, 12V FETs can be used for synchronous rectifier in second stage converter.

Fig.4.2.6 shows the experimental topology, AHB converter with two air-gap transformers [82, 83] instead of current doubler, which helps to simplify interconnections between the secondary winding with synchronous rectifier and reduces the conduction loss.

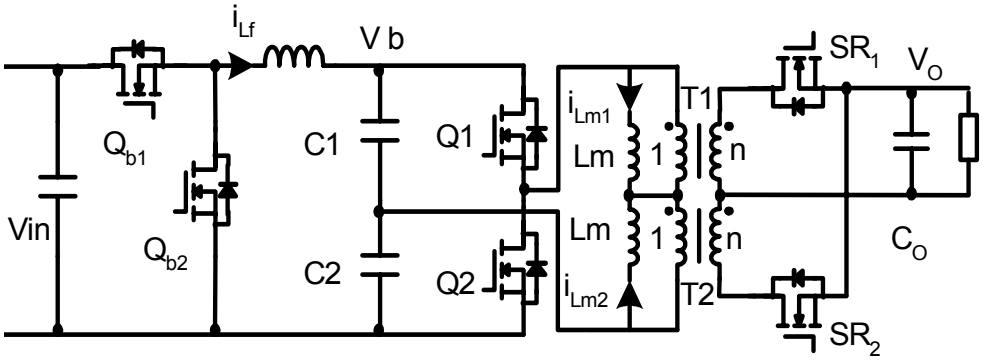


Fig.4.2.6 Two-stage DC-DC converter with two-transformer topology

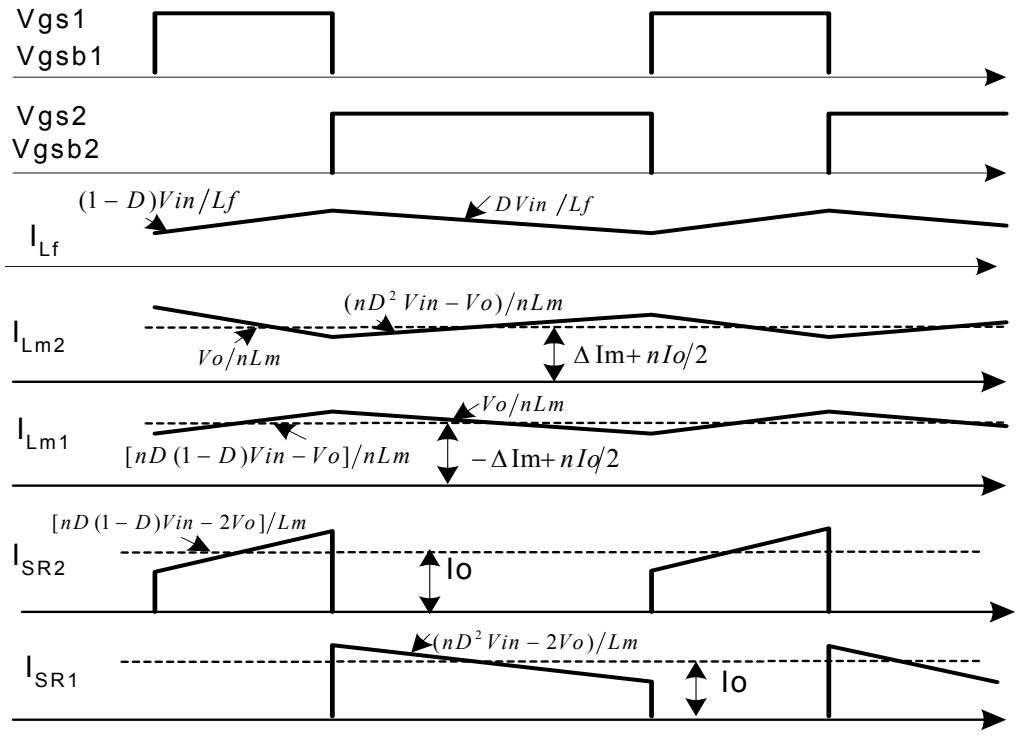


Fig.4.2.7 Key waveforms analysis of experimental prototype

The two-stage DC-DC converter with two-transformers has two main operation modes shown in Fig.4.2.8. In mode 1, Q_1 and Q_{b1} are both on. SR_2 conducts full load current and clamps T_2 primary voltage to Vo/n, while magnetizing inductance Lm1of T_1 acts as a filter inductor to limit the slew rate of input current with half of the output power and i_{Lm2} shares the other half of output power. Their corresponding current slew rates are:

$$\frac{di_{LM1}}{dt} = (nD(1-D)V_{in} - V_O)/nL_{m1} \tag{4-2-7}$$

$$\frac{di_{LM2}}{dt} = -V_O/nL_{m2} \tag{4-2-8}$$

During mode 2, SR_1 conducts when Q_2 and Q_{b2} are on, which clamps T_1 primary voltage to V_O/n. The magnetizing inductance L_{m2} of T_2 acts as a filter inductor to limit the slew rate of input current.

$$\frac{di_{LM2}}{dt} = (nD^2V_{in} - V_O)/nL_{m2} \tag{4-2-9}$$

$$\frac{di_{LM1}}{dt} = -V_O/nL_{m1} \tag{4-2-10}$$

From the above analysis, the two-transformer topology operation is the same as the current-doubler rectification. Due to DC bias current in the transformer, an air gap is required in the transformers to prevent transformer core saturation.

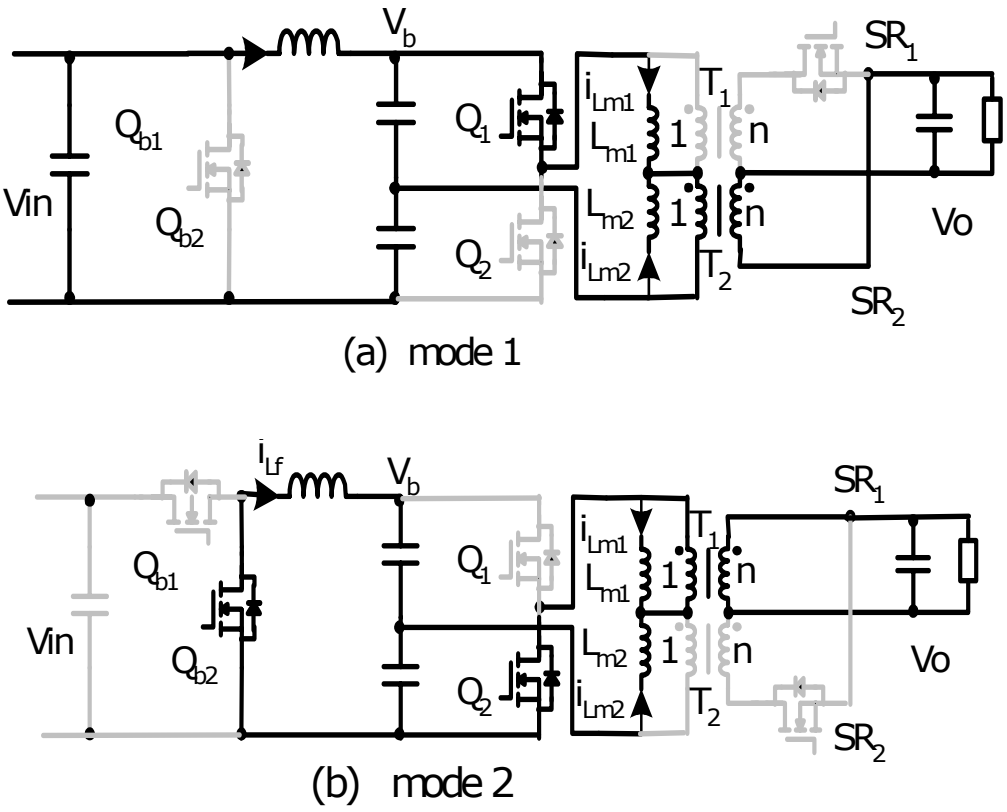


Fig.4.2.8 Operations analysis of experimental prototype

4.2.3 Experimental Prototype

A 36~75V input and output 1V/20A two-stage converter with novel control has been built, and its switching frequency is 150 kHz. Two transformers (EI18, n_S:n_P= 4:1) are integrated into one core using integrated magnetic techniques [84]. And the control IC is UC3842.

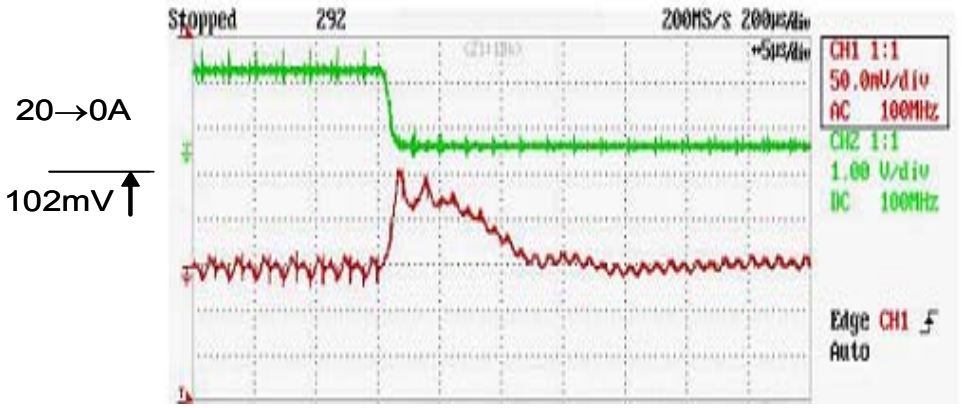


Fig.4.2.9 Output ripple in step-down load @10A/μs

(CH1: 50mV/div, CH2:10A/div, 5μs/div)

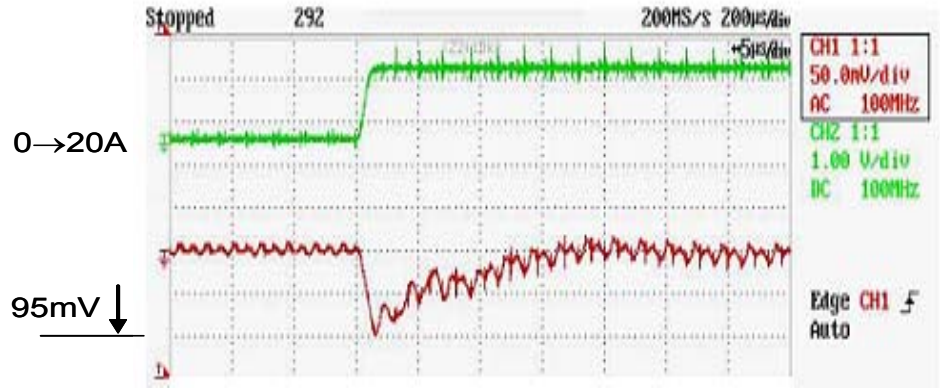


Fig.4.2.10 Output ripple in step-up load @10A/μs

(CH1: 50mV/div, CH2:10A/div, 5μs /div)

About 102mV voltage spike is in step-up load 0~20A and is only 102mV and 95mV in step-down load @10A/μs. The response time in the two-stage converter with novel control is about 15μs, which is much faster compared with 100μs response time in Fig.4.1.8.

Fig.4.2.15 shows the novel control in the second-stage converter used in high input voltage applications. The best advantage here is that two diodes are in place of the two switches discussed in the previous first stage converter, which will reduce switching loss in high frequency operation and simply the first stage converter design. Also, it is a low cost solution, but it increases the voltage stress across Q_2 in second stage converter.

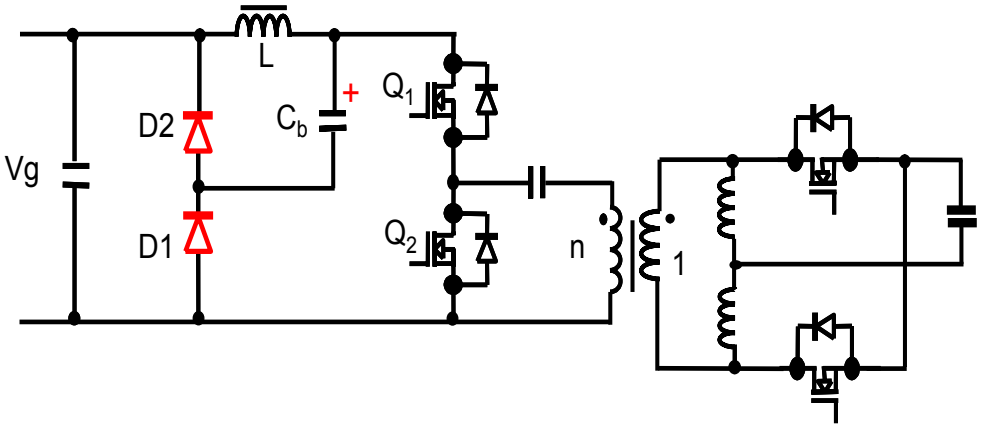


Fig.4.2.15 High voltage application with novel control

A simple novel control method is given to investigate the dynamic response relationship with nonlinear gain instead of conventional linear relationship in the two-stage DC-DC converter, and it has a large voltage step-down ratio, a high gain slew rate and fast dynamic response without pushing the converter into higher frequency operation. Furthermore, proposed novel control in a two-stage converter simplifies the control design and improves transient response. Furthermore, novel control can also be used in high voltage two-stage converter to simplify the circuit.

4.3 Proposed Balancing Winding Network for Complementary Control Converter

Complementary control topologies, including asymmetrical half-bridge converter (AHB), active clamp forward converter (ACF), boost half-bridge converter (BHB) [95] and TTBHB [96] are very attractive in high frequency, high-efficiency converters because of ZVS in the primary side by utilizing the energy stored in leakage inductance by simple control as shown in Fig.4.3.2 and Fig.4.3.3. Also, the output filter can be reduced due to perfect filtered voltage waveforms. Furthermore, self-driven methods also can be easily used for the synchronous rectifier.

Fig.4.3.1 shows the topology of the half-bridge converter with complementary control (HBCC) [87-93]. There is a DC bias magnetizing current I_M in transformer based on the voltage-second balance.

$$I_M = (1-D)\cdot I_{out}\cdot n1 - D\cdot I_{out}\cdot n2 \qquad (4\text{-}3\text{-}1)$$

It is clear that magnetizing current I_M changes with duty ratio D, which shows the double pole-zero effect in HBCC with its corresponding input capacitors, C1 and C2. This is the byproduct of complementary control, double pole-zero effect, which is made up of magnetizing inductance and the corresponding blocking capacitors.

In other topologies, such as ACF, BHB and TTBHB, the principle of double pole-zero effect is the same as HBCC. Therefore HBCC converter is carried out here as an example to analyze double pole-zero effect.

The double pole-zero effect of HBCC converter complicates the design of compensation network and deteriorates the dynamic response. Mitigation of the double pole-zero effect will be helpful to the improvement of HBCC converter transient response.

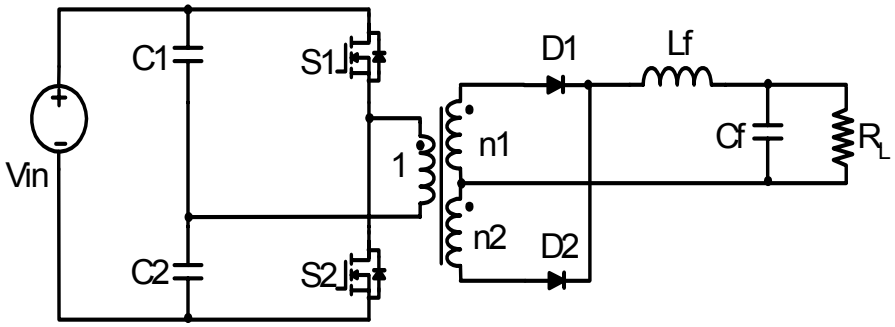


Fig.4.3.1 HBCC converter topology

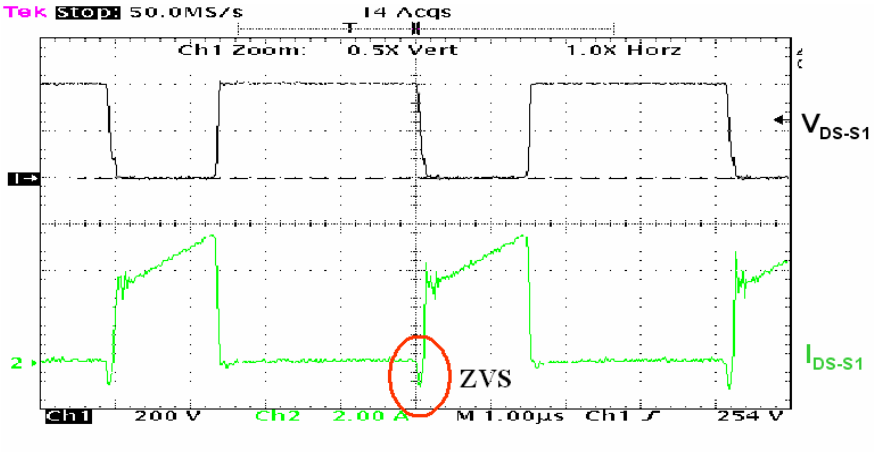


Fig.4.3.2 S1 ZVS in HBCC converter

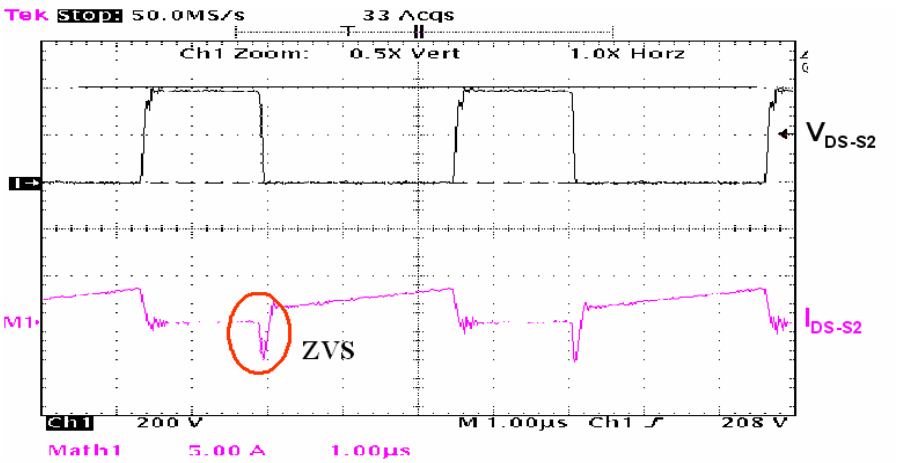


Fig.4.3.3 S2 ZVS waveforms in HBCC converter

4.3.1 Double Pole-Zero Effect in Complementary Controlled Converter

Small signal modeling of HBCC converter has already been done [91] [94]. Fig.4.3.4 shows the equivalent small signal model of the HBCC converter. It is clear that there are two pairs of LC networks in the HBCC converter:

1) An LC network of output filter: L_f and C_f, and its resonant frequency f_F;

2) Another LC network of transformer magnetizing inductance L_M, its corresponding capacitors (C1+C2), and its transformer-capacitive resonant frequency f_{TD}.

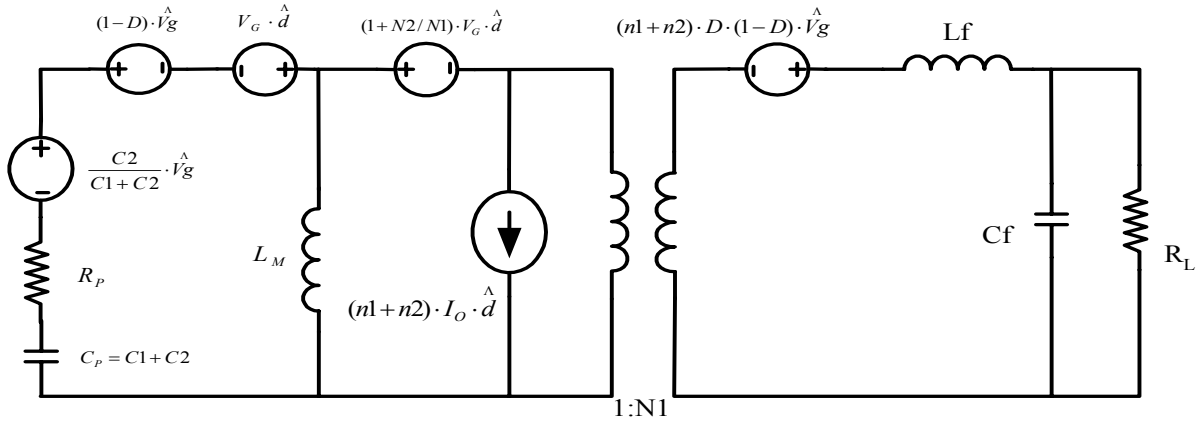


Fig.4.3.4 Small signal modeling of HBCC converter

Table.4.3 Pole and zero of HBCC converter

	f_F-pole	f_{TD}-zero	f_{TD}-pole	Gain
$f_F>f_{TD}$	$\frac{1}{2\pi\sqrt{L_F C_F}}$	$\frac{1}{2\pi\sqrt{L_F C_P}}$	$\frac{\sqrt{\frac{N1+N2}{N1}}}{2\pi\sqrt{L_M C_P}}$	$(N1+N2)\cdot Vin$
$f_F<f_{TD}$*	$\frac{1}{2\pi\sqrt{L_F C_F}}$	$\frac{\sqrt{\frac{N2^2 L_M+L_F}{L_F}}}{2\pi\sqrt{L_M C_P}}$	$\frac{\sqrt{\frac{N1+N2}{N1}}}{2\pi\sqrt{L_M C_P}}$	$\frac{(N1+N2)\cdot Vin}{\frac{N2^2 L_M+L_F}{L_F}}$

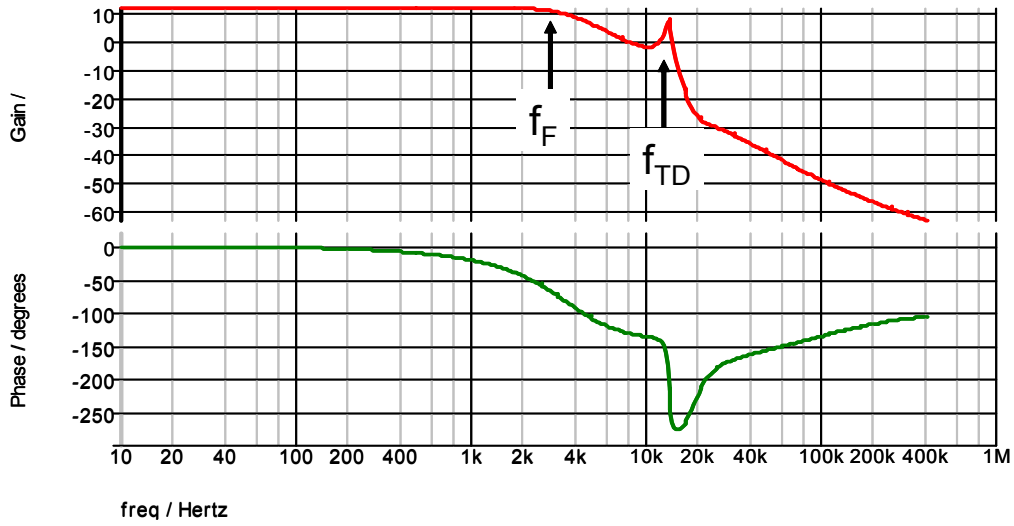


Fig.4.3.5 Bode plot of $\hat{V}_O / \hat{d}$ in the HBCC converter ($f_{TD}>f_F$)

There are two typical cases in HBCC converter design based on the relationship between the output filter resonant frequency f_F and transformer-capacitive resonant frequency f_{TD}, shown in Table 4.3. In most high frequency converters, the transformer-capacitive resonant frequency is always higher than output filter resonant frequency, ($f_{TD}>f_F$).

Fig.4.3.5 shows this phenomenon in bode plot of $\hat{V}_O / \hat{d}$ of the HBCC converter ($f_{TD}>f_F$). At the frequency of f_{TD}, we can see a sharp change in phase and gain, which results in loop instability and poor dynamic response and complicates the compensation network design.

One feed-forward method is used to reduce the effect of double pole-zero effect [92], which reduces the effect of double pole-zero by sensing the middle-point capacitive-divider voltage of the half-bridge converter.

Here, a balancing winding network is proposed to compensate the different voltage between C1 and C2 for mitigation of the double pole-zero effect. And the balancing winding network also can be used in other complementary control converters.

4.3.2 Proposed Balancing Winding Network

As for transient response in HBCC converter, a HBCC converter has to increase duty cycle D to keep tight regulation via close loop control in step-up load, and finally, the voltage across C1 (Vc1) increases and the voltage across C2 (Vc2) decreases into the steady state. However, because of delay times in compensation network and IC propagation time, the duty cycle D cannot immediately catch up with the transient load current, which forces Vc1to decrease and Vc2 to increase; thus, output voltage drops more. After delay times, output voltage starts to go up. Vice versa, output voltage increases in step-up load due to double pole-zero effect.

For example, a small variation of ΔV_{C1} under duty ratio D occurrs in Vc1, and then it will cause corresponding output voltage variation ΔV_O because of the double pole-zero effect as following equation:

$$\Delta V_O = \Delta V_{C1} \cdot [D \cdot n1 - (1-D) \cdot n2] \qquad (4\text{-}3\text{-}2)$$

Fig.4.3.6 shows the proposed balancing winding network, which is composed of a small gauge winding in the transformer, T_{1b}, having the same number of turns as the primary winding, T_{1a}, two small diodes and one capacitor Cb.

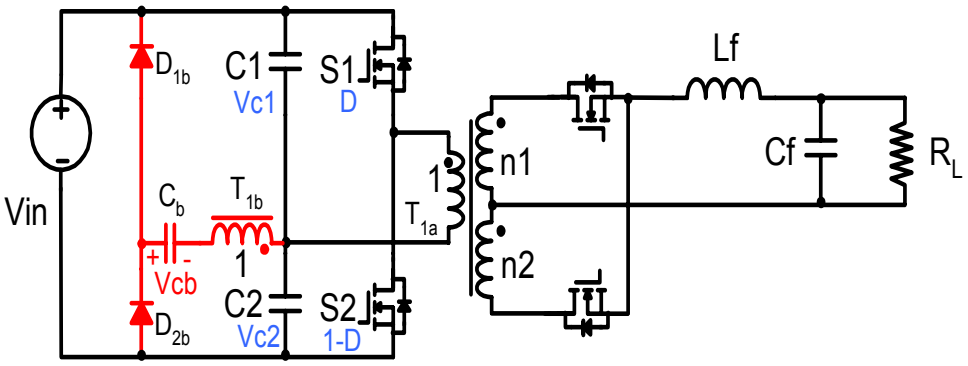


Fig.4.3.6 HBCC converter with balancing winding network

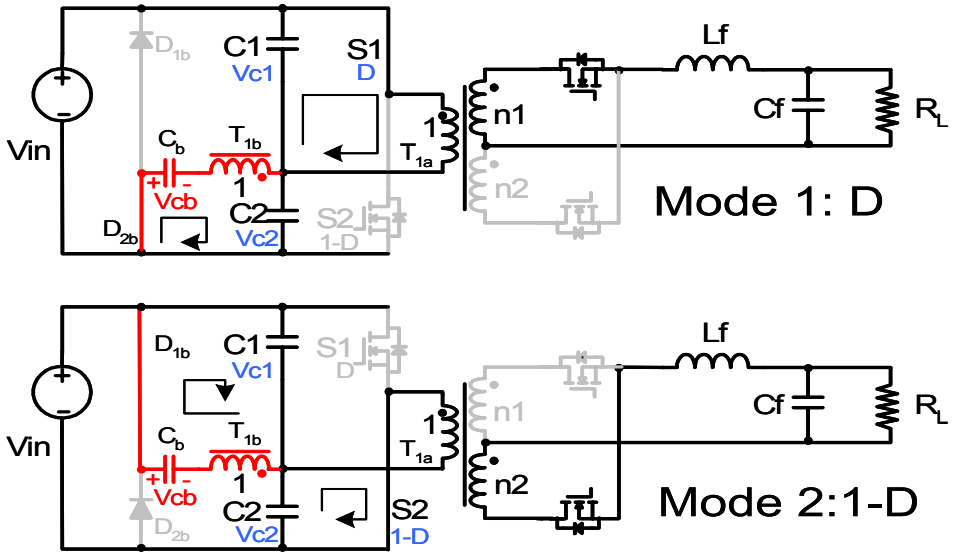


Fig.4.3.7 Operation analysis of HBCC with balancing winding network

Two operating modes of HBCC converter with balancing winding network are shown in Fig.4.3.7. The voltage across C_b is assumed to be a constant voltage source because of small power handling in balancing winding network in steady state. When S1 is on, the unbalanced voltage between C1 and C2 is mitigated through T_{1b}, C_b and D_{2b}. A similar operation exists in mode 2, where unbalanced voltage is mitigated by balancing winding network T_{1b}, C_b and D_{1b}.

In step-up load, the energy stored in capacitor C_b discharges immediately to load through the balancing winding network to compensate the voltage drop caused by the delay times in controller. In step-down load, the extra energy caused by the delay times is absorbed by Cb through the balancing network so that the over voltage spike drops. In other word, capacitor Cb acts as an energy buffer in transient load without any delay times, therefore the double pole-zero effect is mitigated by balancing winding network. Moreover, the audiosusceptibility of the HBCC converter, the effect of input voltage to output voltage, also can be reduced by using balancing winding network.

4.3.3 Simulation and Experiment with Balancing Winding Network

As for HBCC converter with balancing winding network, it is conplicated to carry out small signal modeling analysis because the currents through balancing winding network are discontinuous. Software Simplis is the simplest way to simulate the small signal performance of HBCC with balancing winding network.

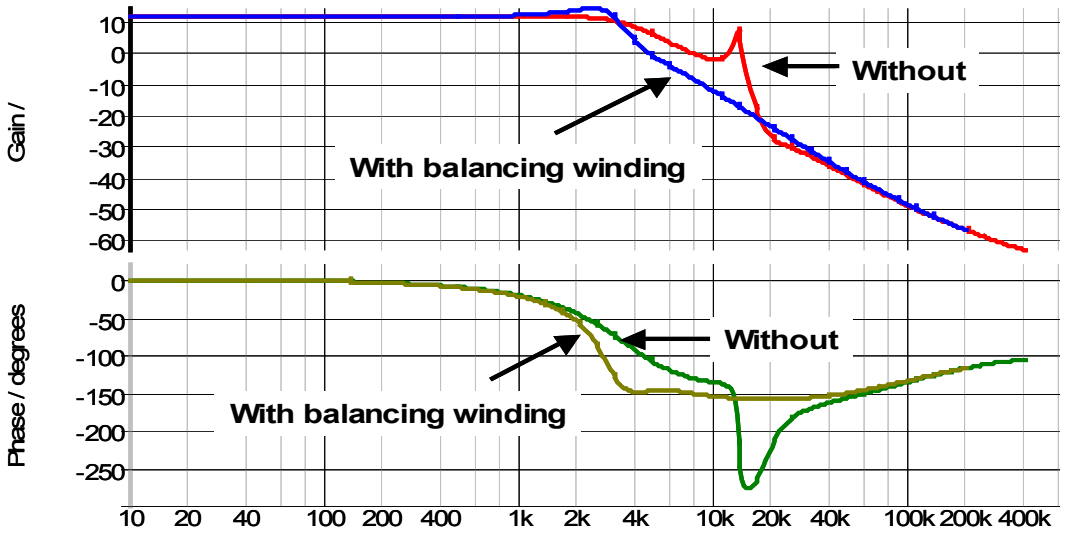


Fig.4.3.8 Comparison of bode plot of $\hat{V}_o / \hat{d}$ in the HBCC converter

From the simulation of HBCC converter with balancing winding network, it is clear that a very slight double pole-zero effect exists in HBCC with balancing winding network, which can be negligible compared to this effect without a balancing winding network as shown in Fig.4.3.8.

Reduced double pole-zero effect of HBCC converter increases the bandwidth and simplifies compensation network design, resulting in good loop stability and good transient response, as the tested bode plot of $\hat{V}_o / \hat{d}$ in experimental prototype in Fig.4.3.9.

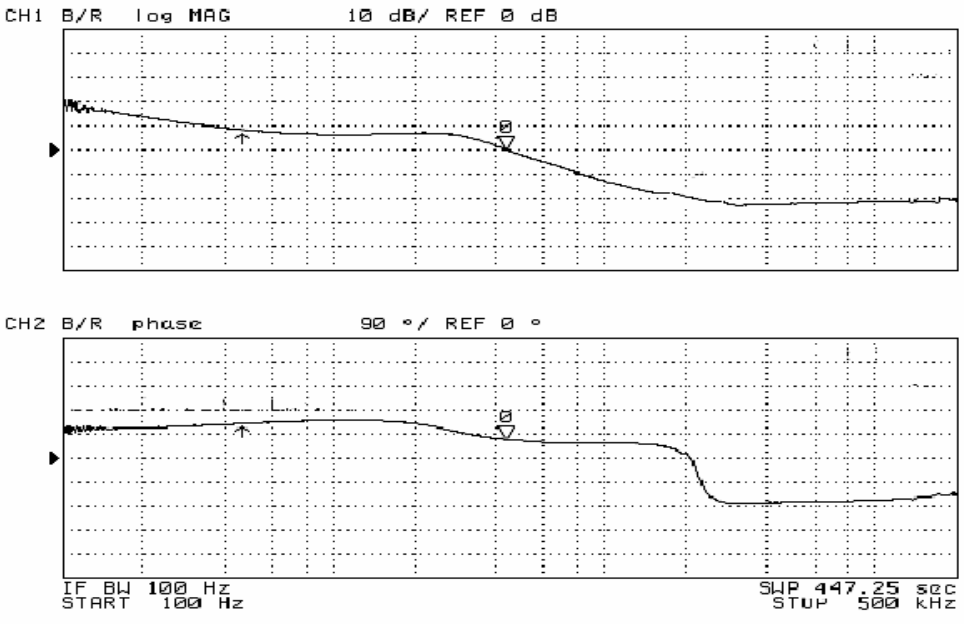


Fig.4.3.9 Experimental Bode Plot with balancing winding network

Balancing winding network is proposed to mitigate the effect of double pole-zero effect in complementary control converters with the following features:

1) It mitigates the double pole-zero effects;

2) It reduces transient voltage spikes;

3) It simplifies the compensation network design and improves dynamic response;

4) Small rating components are needed.

The balancing winding network also can be applied in other complementary control converters, such as BHB converter shown in Fig.4.3.10. The principle of balancing winding network in these converters is the same as in HBCC converter and benefits the transient response and simplifies the compensation network design.

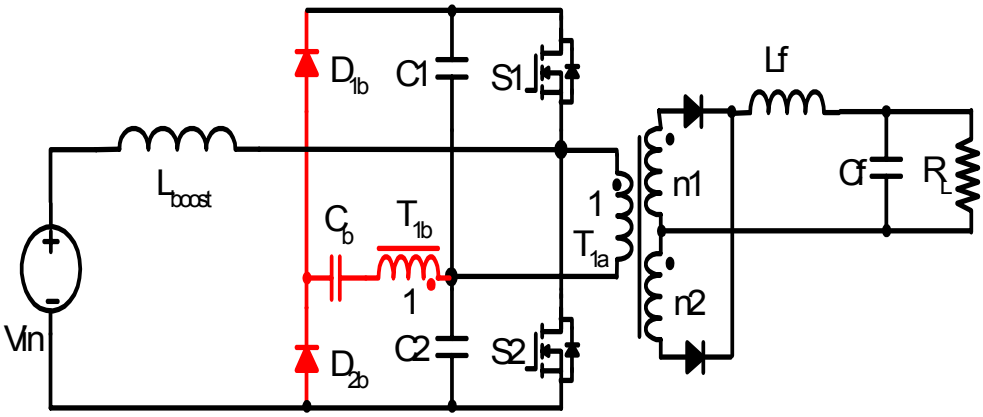


Fig.4.3.10 BHB converter with balancing winding network

4.4 Proposed Parallel Post Regulator for Wide Range Input Converter

Wide input range DC-DC converter is widely used in the distributed power systems (DPS) and server power supplies, which require 20ms hold up time to provide output voltage within regulation after input AC line dropout at full load conditions. Fig.4.4.1 shows the general front-end DC-DC converter design procedure: design at the minimal input voltage V_{inmin} and operation at the maximum input voltage V_{inmax} with very small duty cycle, which makes it very difficult to achieve soft switching in primary side and causes higher voltage stresses in the secondary rectifier. Therefore, bad efficiency is in normal operation in high voltage input. Range winding topology [97] only activates to increase the transformer turn ratio for hold up time when the input DC voltage drops to a certain value. Thus, the converter cab be designed and operates in narrow input voltage range, which leads to better efficiency. Because of the limitation of the close-loop bandwidth, a transient problem appears during range winding activation [98] [106].

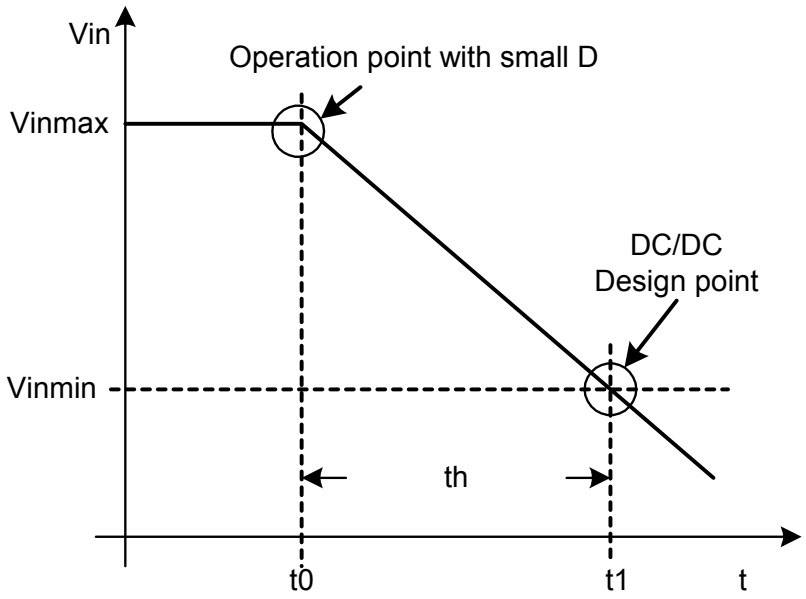


Fig.4.4.1 Wide range input DC-DC converter design

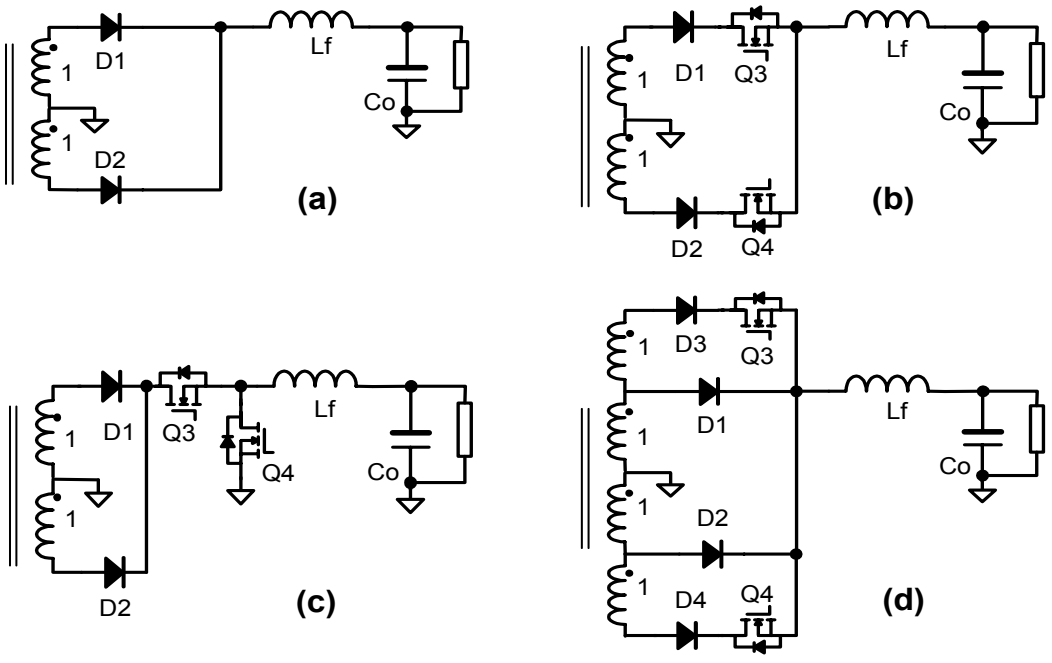


Fig.4.4.2 Different types of secondary side post regulator

Different types of secondary side post regulators (SSPR) [99-101] are shown in Fig.4.4.2, which regulate the output voltage using secondary side control. The primary side can easily achieve ZVS in full range load due to 0.5 duty cycle operation. Main rectifiers are composed of D_1, D_2, L_f and C_O, and post regulators are composed of D_3, D_4, Q_3, and Q_4. In topology (b), Q_3 and Q4 are connected in series with the main rectifiers to control the pulse width for tight output regulation with ZCS, but it introduces large conduction losses, especially in low voltage applications. In topology (c), Q_3 also can achieve ZVS if it turns on or turns off at the intervals of the main rectifiers' current commutation. However, this is a cascade system, and therefore total efficiency is the big challenge. Topology (d) is the combination of topology (a) and (b), and it can reduce the output filter inductance [102] but increases a lot of conduction losses in primary side switches and post regulator due to high current rating when post regulator is activated.

The half bridge converter is commonly-used in low or medium power applications due to its simplicity and small transformer turn ratio. But in wide range input DC-DC converters, the conventional half-bridge converter cannot achieve ZVS in primary side, resulting in high switching losses. Recently, many efforts have been put into a half-bridge converter for soft switching in the primary side [103-105], but it still very difficult to achieve ZVS in full range load and wide range input cases. How to improve the efficiency in high input is very crucial for DPS and server power supplies because they always operate in high input voltage. As previous discussed, secondary side post regulator with half bridge can easily achieve ZVS in primary side in full range loads, but it introduces large extra conduction losses in the series post regulator.

A parallel post regulator (PPR) is proposed to improve efficiency. The concept of parallel post regulator is shown in Fig.4.4.3. Primary side switches operate in D=0.5 so they easily can achieve ZVS in full range load. Most of the power, such as 90 percent, is delivered to the load by

unregulated output voltage V_{O2} that is less than output voltage V_O with very high efficiency η_1. The parallel post regulator only delivers small parts of the power, such as 10 percent, with efficiency η_2 and regulates the output voltage. PPR input voltage V_{O1} is higher than the converter output voltage V_O, and finally, we can get high total efficiency.

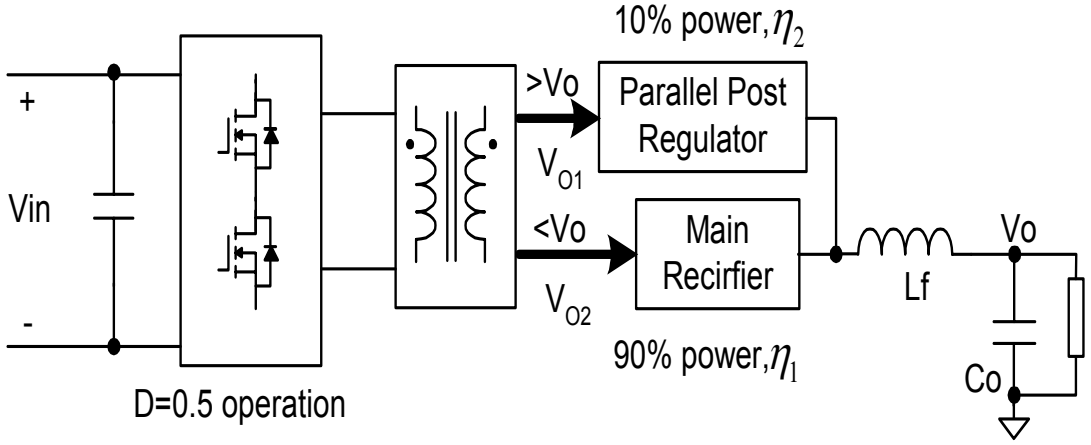


Fig.4.4.3 Concept of parallel post regulator

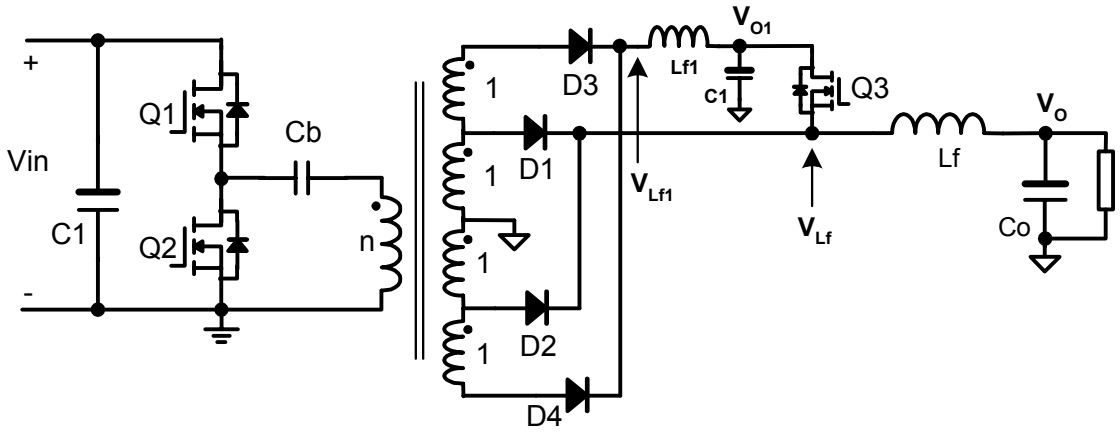


Fig.4.4.4 Implementation circuit of parallel post regulator

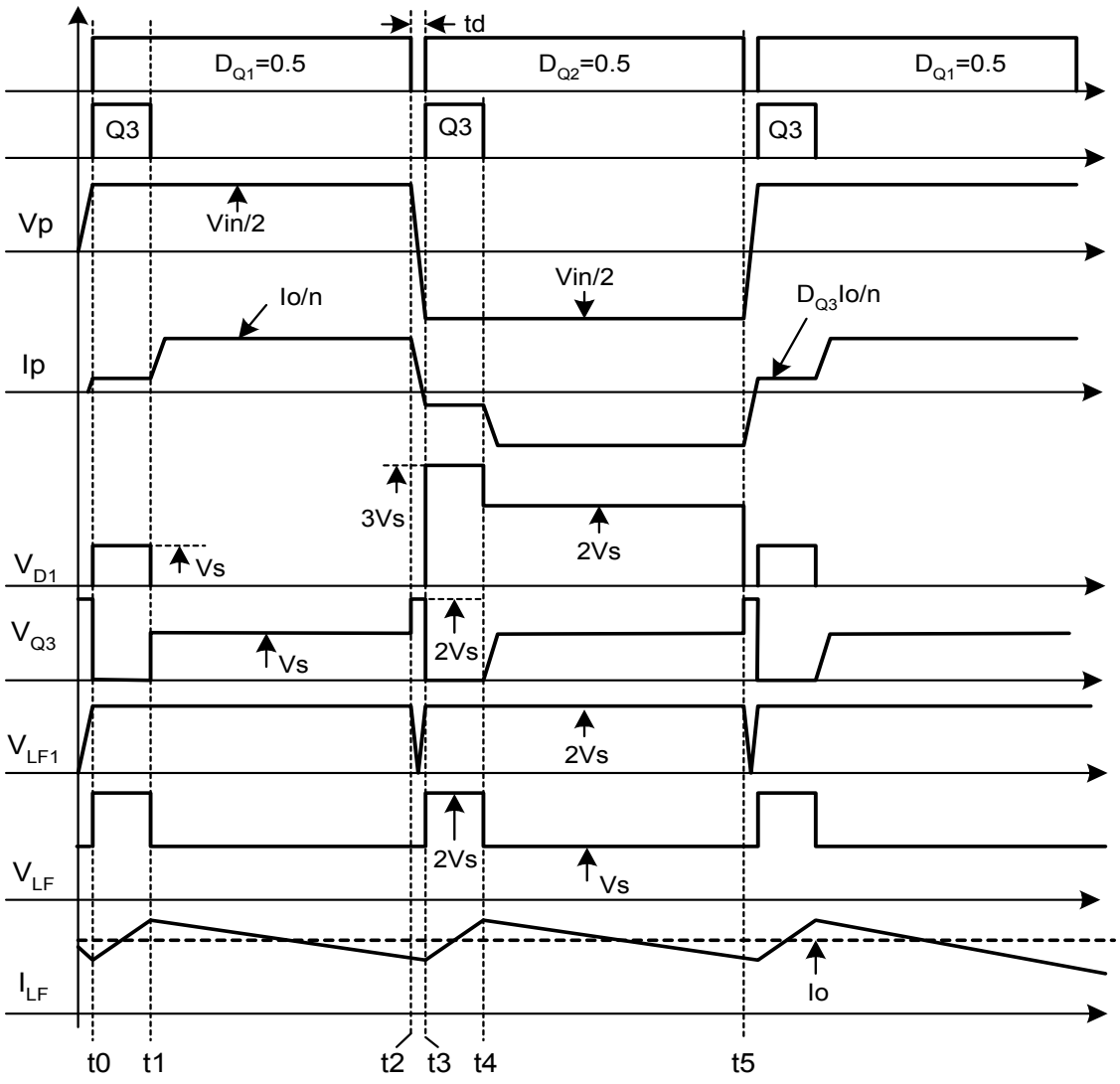


Fig.4.4.5 Key waveforms of parallel post regulator

4.4.1 Proposed Topology: Parallel Post Regulator

Fig.4.4.4 shows the implementation circuit of parallel post regulator with half-bridge converter that simplifies input capacitor into one blocking capacitor C_b, and it operates in D=0.5 with small dead time t_d, resulting in easy ZVS in primary side at full range load. The parallel post

regulator is composed of D_3, D_4, L_{f1}, C_1 and Q_3. Only very small inductance L_{f1} and capacitance C_1 are required because of D=0.5 operation in primary side. The current through D_3 and D_4 are the average current of parallel post regulator. It is clear that parallel post regulator utilizes the main rectifier D_1 and D_2 as its freewheeling diode. The key operation waveforms of parallel post regulator are shown in Fig.4.4.5. V_S is the secondary transformer winding voltage.

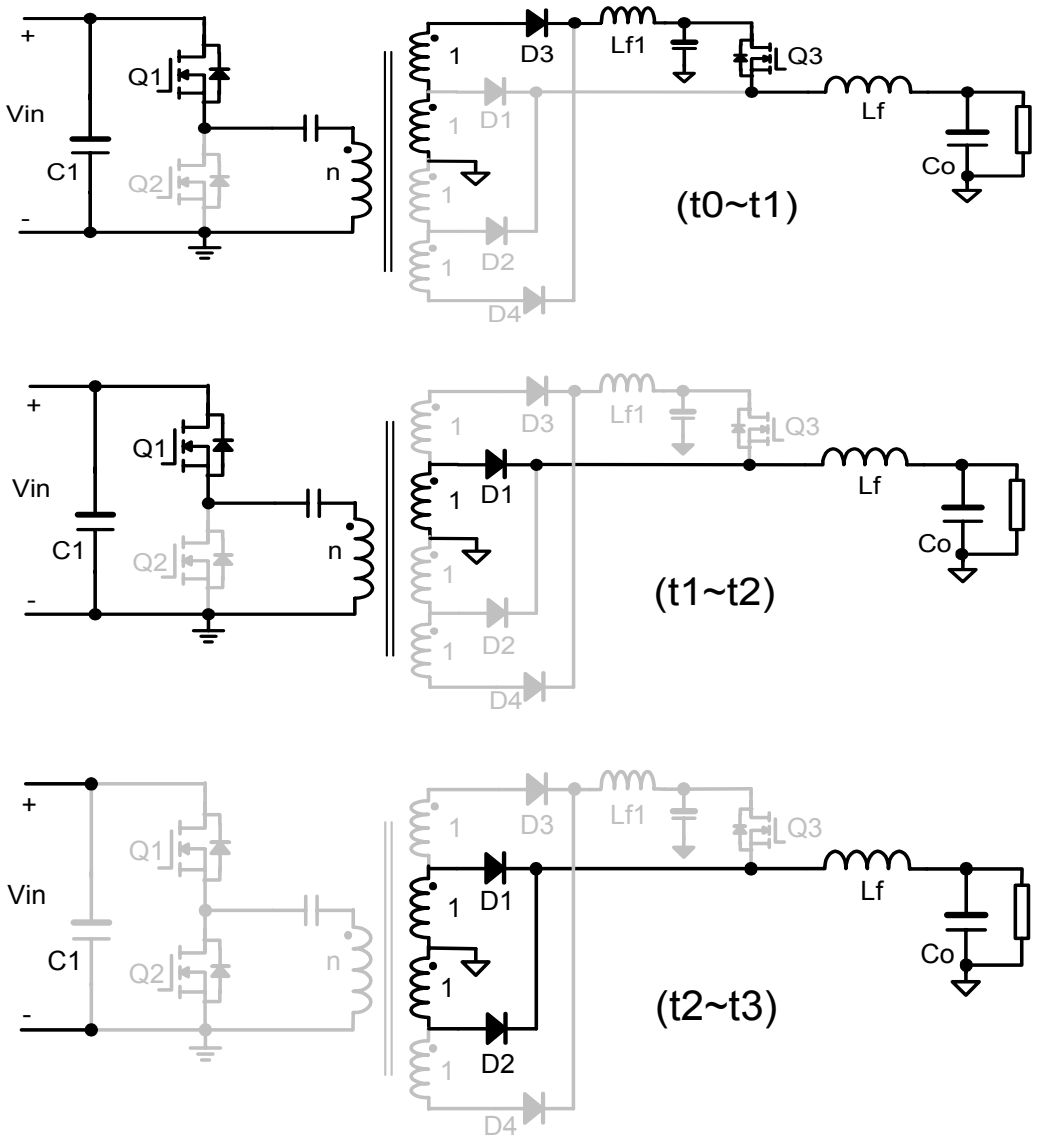


Fig.4.4.6 Detailed PPR operation analysis

4.4.2 PPR Operation Principle Analysis

According to the key waveforms in Fig.4.4.5, there are three main modes of PPR in a half switching period. During t_0~t_1, Q_1 and Q_3 all turn on, main rectifier D_1 and D_2 are in off state. PPR provides the output load current as shown in Fig.4.4.6. D is the duty cycle of Q_3.

$$I_P = 2D \cdot I_O / n \tag{4-4-1}$$

$$V_{D1} = \frac{V_{in}}{2n} \tag{4-4-2}$$

$$V_{D2} = \frac{3V_{in}}{2n} \tag{4-4-3}$$

At the interval t_1, PPR turns off, so the inductor current commutates from Q_3 to D_1. D_1 conducts all the load current within t_1~t_2.

$$I_P = I_O / n \tag{4-4-4}$$

$$V_{D2} = \frac{V_{in}}{n} \tag{4-4-5}$$

$$V_{Q3} = \frac{V_{in}}{2n} \tag{4-4-6}$$

During t_2~t_3, Q_1 turns off, the energy stored in transformer leakage inductor starts to discharge the parasitic capacitors of Q_1 and Q_2 until the body diode of Q_2 conducts, and then Q_2 achieves ZVS. Secondary side rectifiers conduct together to free-wheel the inductor current.

$$V_{Q3} = \frac{V_{in}}{n} \tag{4-4-7}$$

From the volt-second balance in L_f, DC voltage gain in CCM can be obtained:

$$V_O = \frac{V_{in}}{2n}(1 + D) \tag{4-4-8}$$

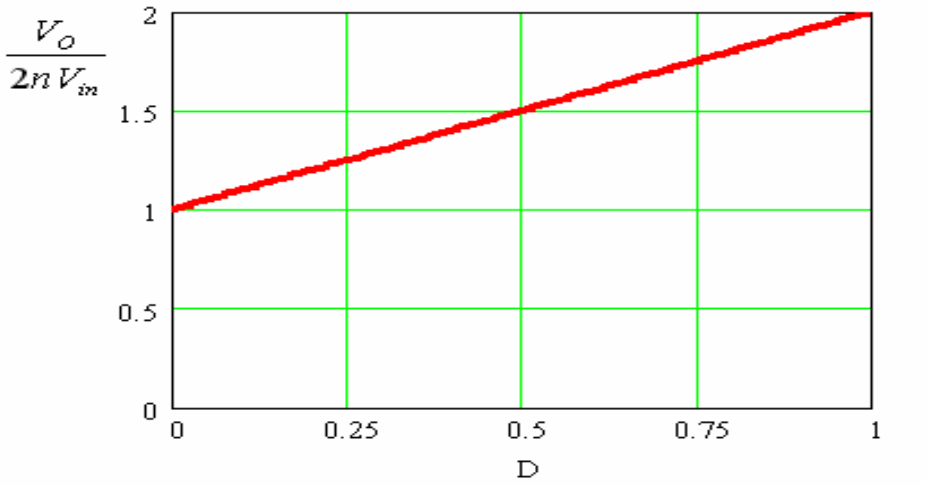


Fig.4.4.7 Normalized DC gain vs. D

From the curve in Fig.4.4.7, it is clear that PPR can operate in two-times the wide range input voltage converters with tight regulated output voltage. Furthermore, the input and output filter requirements are significantly reduced due to perfect filtered waveforms, shown in Fig.4.4.5, suitable for power density improvement.

4.4.3 Flexible Secondary Side Control for PPR

Leading or trailing edge modulation in synchronization with primary side switching frequency can be used in secondary side control to control the pulse width in a post regulator controller [99] [109-110]. Fig.4.4.8 shows the current commutation between half-bridge main rectifiers with Q_3 in PPR. L_{LK1} is the secondary leakage inductance of half-bridge converter, including inductance of PCB trace and transformer, and R_{LK1} is the total resistance. L_{LK2} and R_{LK2} are the total parasitic inductances and resistances in parallel post regulator. We can obtain the current slew rate during current commutations through:

$$V_{O1} - V_{Sec} = (L_{LK2} - L_{LK1})\frac{di_2}{dt} + (R_{LK2} - R_{LK1})i_2 + R_{LK1}I_O \qquad (4\text{-}4\text{-}9)$$

From (4-4-9), it is clear that shortest current commutation time occurs when secondary voltage V_S is equal to zero during the dead time td, resulting in smaller turn-on switching loss in PPR, so trailing edge modulation is adopted in the experiments.

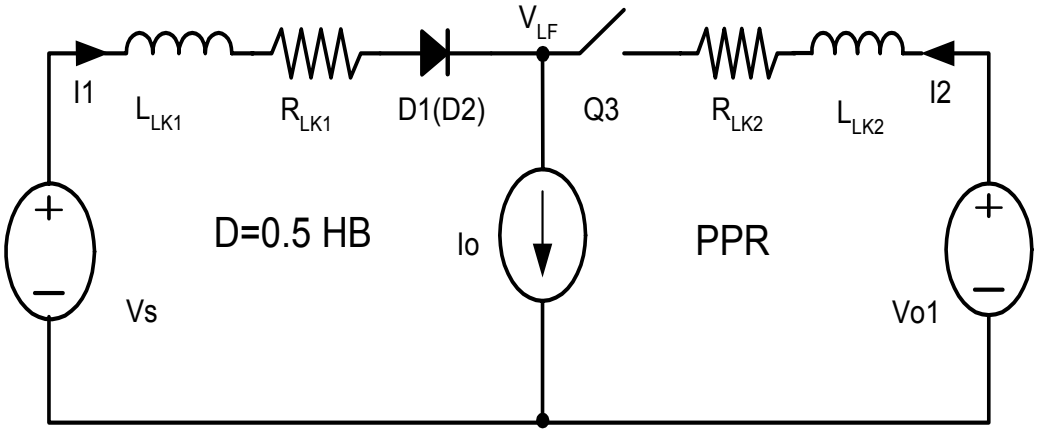


Fig.4.4.8 Current commutation between HB and PPR

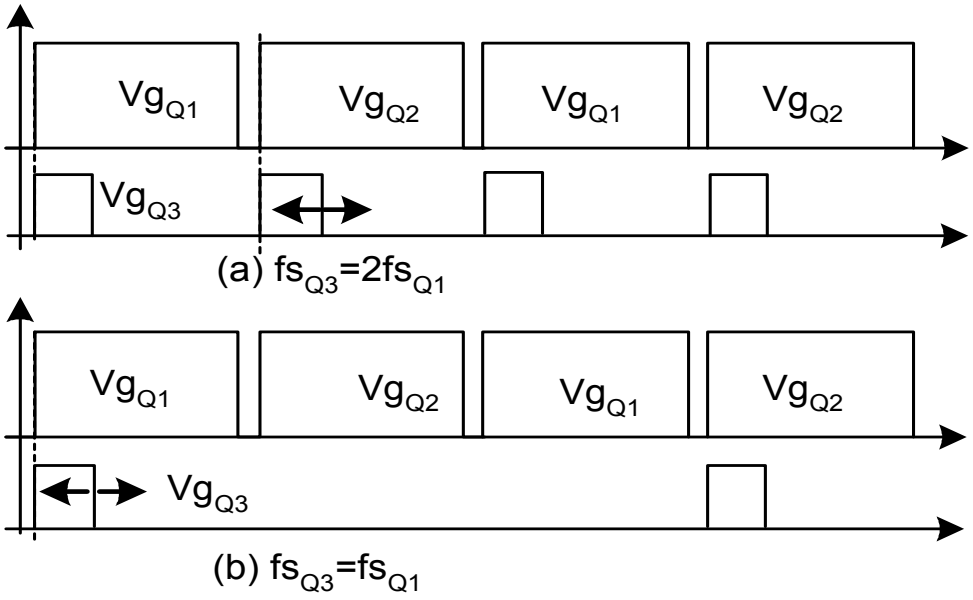


Fig.4.4.9 Flexible control for PPR

Fig.4.4.9 shows two different control methods with trailing edge modulation at different switching frequencies in PPR: $fs_{Q3}=2fs_{Q1}$ and $fs_{Q3}=2fs_{Q1}$. f_{SQ1} is the switching frequency in half-bridge converter, and f_{SQ3} is the switching frequency in PPR.

PPR utilizes the main rectifiers D_1 and D_2 as its freewheeling diodes. Reduced conduction losses are in primary and secondary diode D_3 and D_4 due to small average current handled by PPR, so PPR efficiency η_2 is higher than any of previous post regulators. η_1 is the efficiency of unregulated output voltage in half-bridge converter with main rectifiers. The total efficiency of half-bridge and PPR is as follows:

$$\eta = \frac{\eta_1 \eta_2}{(1-D)\eta_2 + D\eta_1} \tag{4-4-10}$$

Table 4.4 Comparison between conventional HB and PPR

Vin=250~400Vdc, 12Vo, half-bridge topology				
	Turn ratio: n:1:1	Maximum V_{D1}, V_{D2}	Duty cycle	
			250V	400V
Conventional HB	9:1:1	44.4V	$D_{Q1,Q2}$= 0.43	$D_{Q1,Q2}$= 0.245
PPR	18:1:1:1:1	33.3V	$D_{Q1,Q2}$= 0.5 D_{Q3}= 0.73	$D_{Q1,Q2}$= 0.5 D_{Q3}= 0.08
HB: $Vo=D_{Q1}Vin/n$, PPR: $Vo=0.5Vin(1+D_{Q3})/n$				

Table 4.3 shows the comparison between conventional half-bridge converter and PPR. It is clear that PPR has large transformer turn ratio resulting in reduced primary current and reduced voltage stresses across secondary main rectifiers, all of which lead to high efficiency.

4.4.4 Experimental Verification

Based on the previous analysis of PPR, one prototype has been built according to the following specifications and parameters:

Input voltage: 250Vdc~400Vdc;

Output voltage: 12V/40A;

Switching frequency for Q_1 and Q_2: 140 kHz;

Two carried out switching frequencies for Q_3: 140 kHz and 280 kHz;

Primary side Q_1 and Q_2: STP12NM50, 12A/550V, Ron=0.3Ω;

Blocking capacitor C_b: 0.27μF/630V;

Transformer: 18:1:1:1:1, PQ32/30, 3F3;

Main rectifiers D1 and D2: 40CPQ045 each of them, V_f=0.49V;

PPR rectifier D3 and D4: one MUR1020, V_f=1.12V;

Q_3 in PPR: STP80NF06, 80A/60V, Ron=6.5mΩ;

L_{f1} in PPR: 2μH;

L_f in half-bridge converter: 5μH.

Fig.4.4.10 shows primary-side switch ZVS of Q_1 under no load condition and Fig.4.4.11 shows ZVS of Q_1 under 40A load condition. Because of nearly D=0.5 in primary side, it is very easy to achieve ZVS for two switches: Q_1 and Q_2.

Fig.4.4.12 shows the primary transformer voltage and current waveforms. It is clear that the primary current is much smaller in PPR turn-on than that in the main rectifier conduction.

Fig.4.4.13 shows voltage stresses across the main rectifiers D_1 and D_2. The maximum voltage across D_1 occurs when PPR turns on, three times of the secondary transformer voltage.

Fig.4.4.14 shows drive signal and V_{ds} of Q_3 in PPR and the filter current I_{Lf1} with 12V/20A. Very small current ripple exists in the current I_{Lf1} because of D=0.5 operation in the primary side. Maximum V_{ds} occurs at intervals of current commutations.

Fig.4.4.15 shows rectified voltage waveforms and filter inductor current with $fs_{Q3}=fs_{Q1}$, 12V/20A. Fig.4.4.16 shows secondary side rectified voltage and transformer primary voltage and current waveforms with $fs_{Q3}=2fs_{Q1}$, 12V/20A.

Fig.4.4.17 shows the experimental efficiency of half-bridge converter with PPR tested at 400Vdc input. Eff1 is the efficiency of unregulated output voltage without PPR; Eff2 is the efficiency of half-bridge converter and PPR with $fs_{Q3}=fs_{Q1;}$ Eff3 is the efficiency of half-bridge converter and PPR with $fs_{Q3}=2fs_{Q1}$; and Eff4 is the baseline efficiency of half-bridge converter with regulated 12V output voltage. Efficiency of the half-bridge converter and PPR with $fs_{Q3}=fs_{Q1}$ is higher than 90.5 percent from 10A to 40A load current, about 7 percent ~ 8 percent higher than a conventional half-bridge converter.

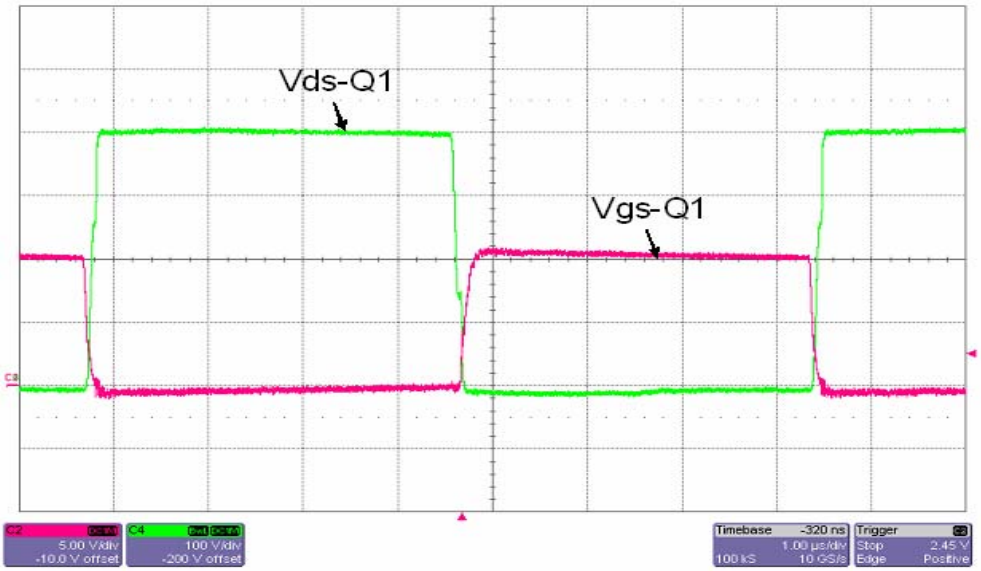


Fig.4.4.10 Q_1 ZVS waveforms @ no load

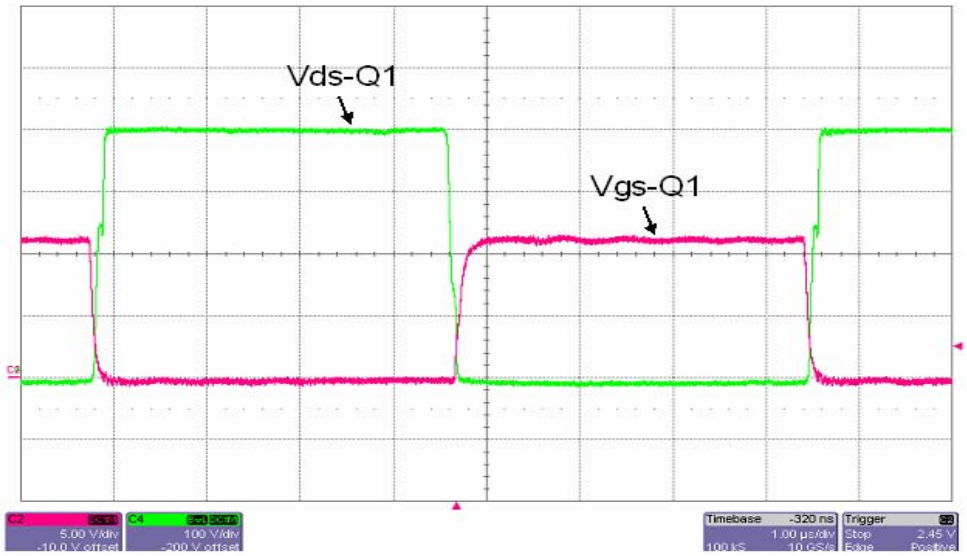


Fig.4.4.11 Q_1 ZVS waveforms @ 40A

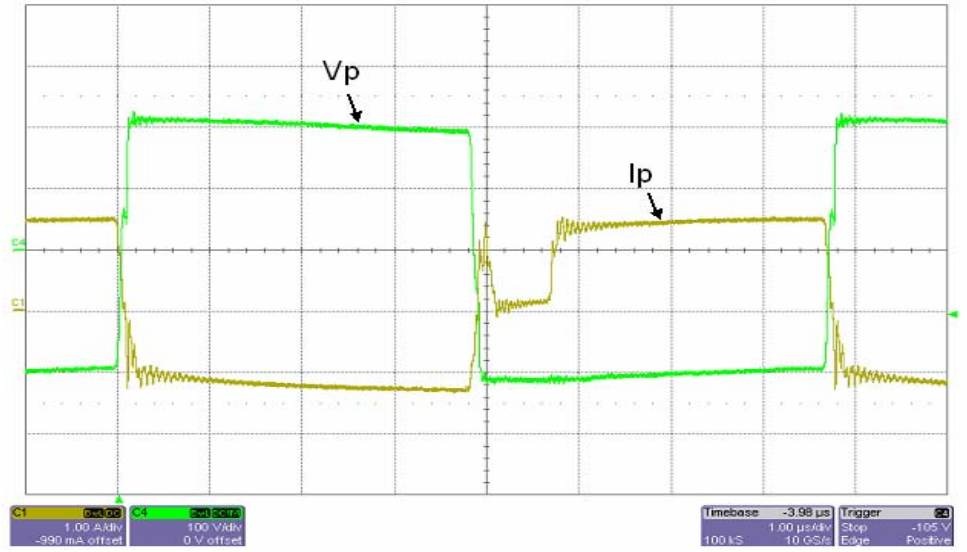


Fig.4.4.12 Primary transformer voltage and current waveforms

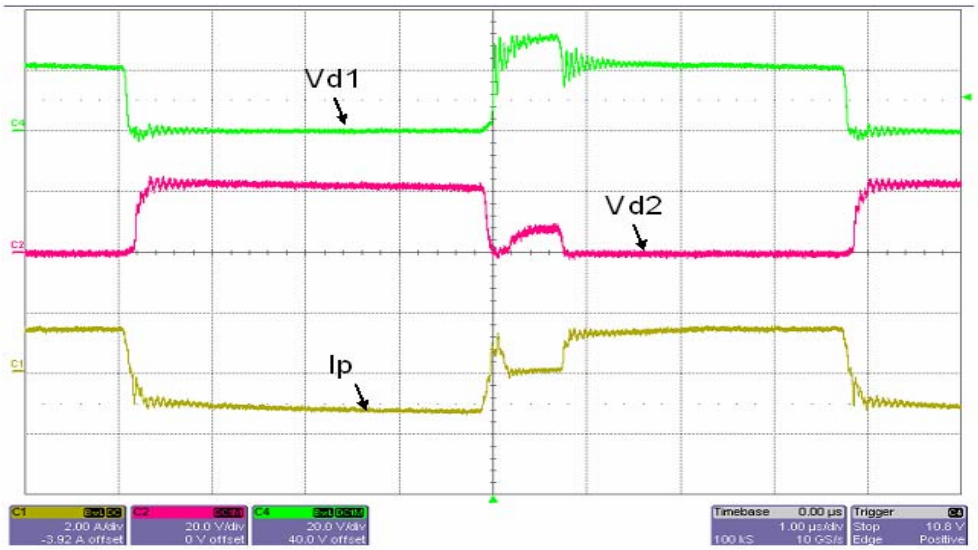


Fig.4.4.13 Voltage waveforms of secondary main rectifiers

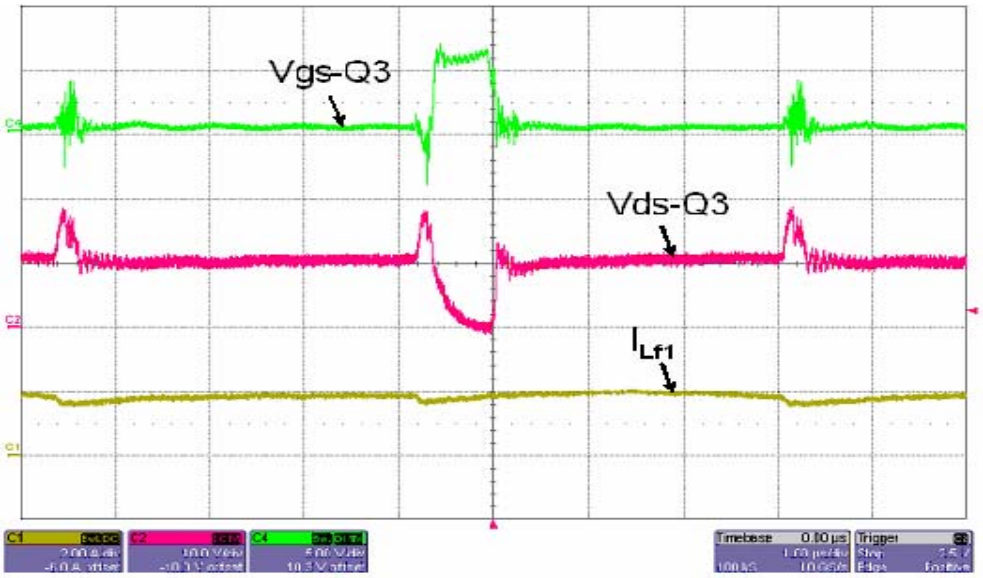


Fig.4.4.14 Voltage waveforms of Q_3 and current I_{Lf1}

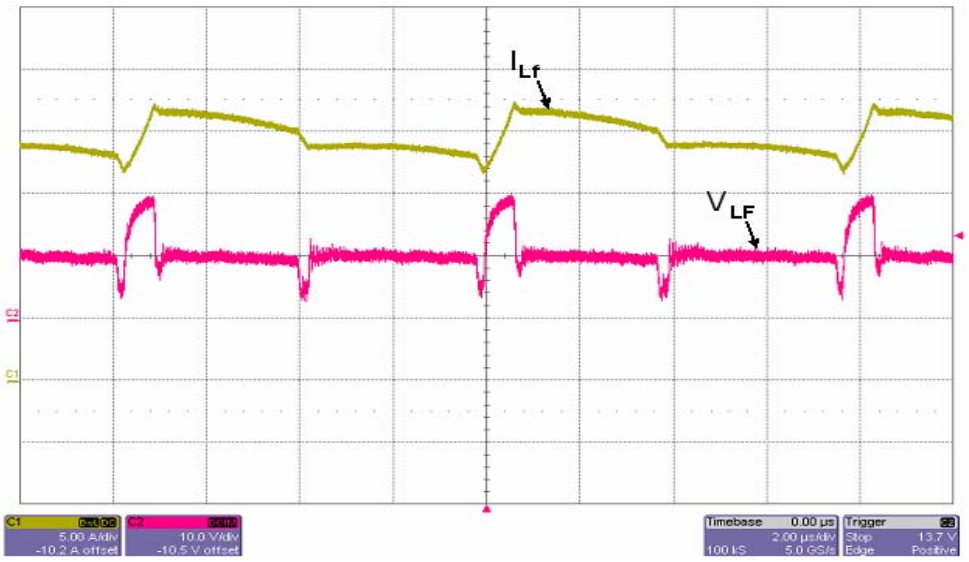


Fig.4.4.15 Waveforms of rectified voltage and filter current

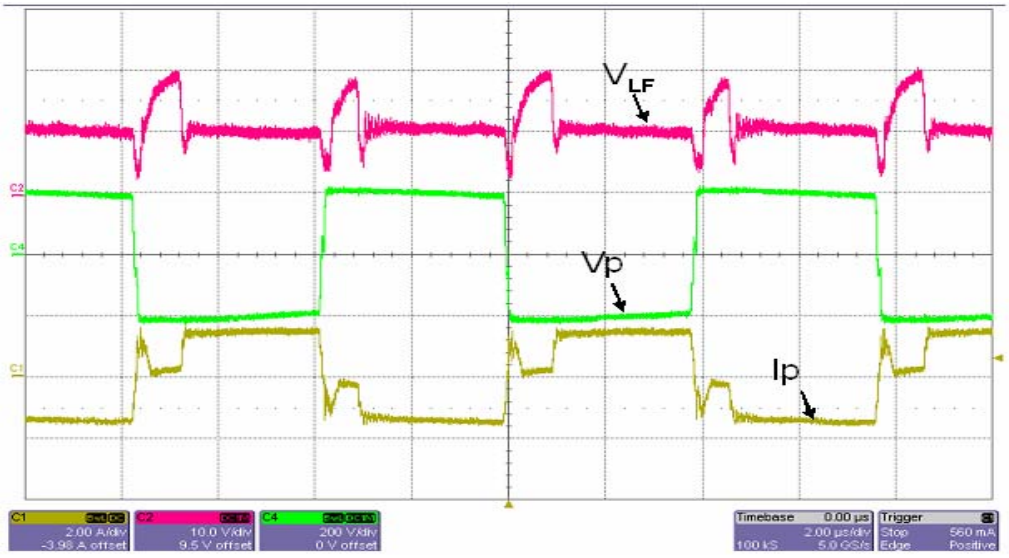
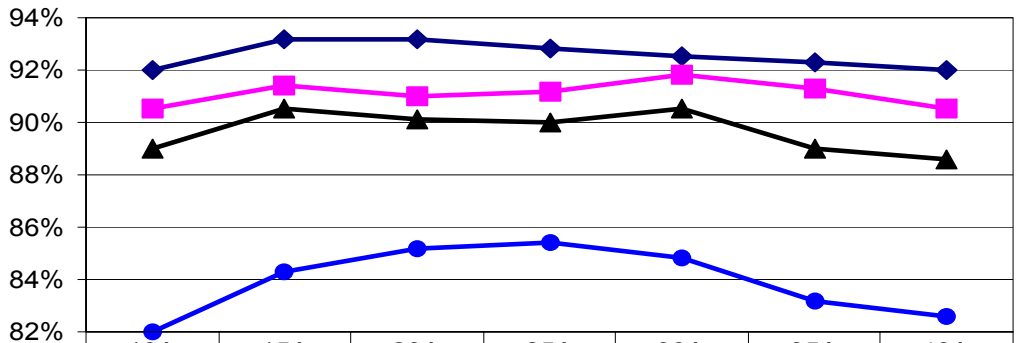


Fig.4.4.16 Current and voltage waveforms @ $f_{Q3}=2f_{Q1}$



	10A	15A	20A	25A	30A	35A	40A
Eff1	92%	93.20%	93.20%	92.80%	92.50%	92.3%	92.0%
Eff2	90.50%	91.40%	91%	91.20%	91.80%	91.30%	90.50%
Eff3	89%	90.50%	90.10%	90%	90.50%	89%	88.60%
Eff4	82%	84.30%	85.20%	85.40%	84.80%	83.20%	82.60%

Fig.4.4.17 Tested efficiency of PPR and HB converter

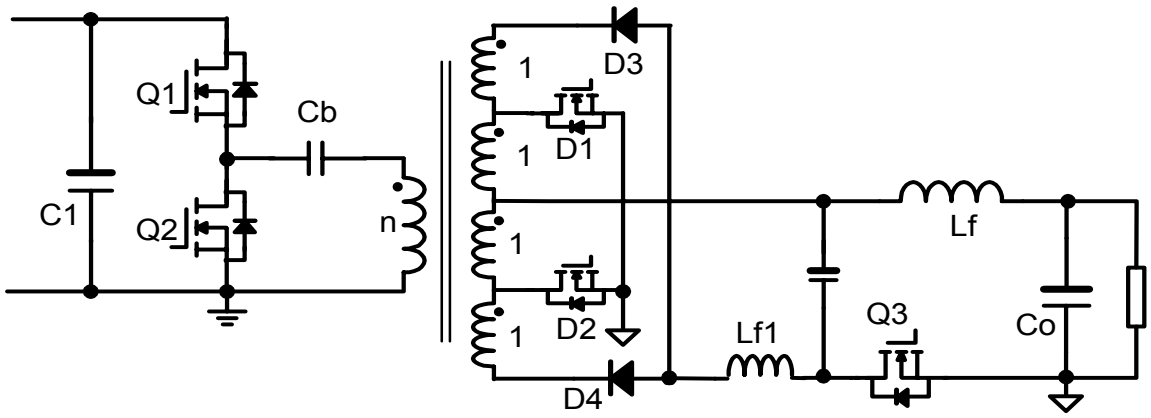


Fig.4.4.18 Synchronous rectifiers with PPR

Parallel post regulator with synchronous rectifier in secondary side in the half-bridge converter is shown in Fig.4.4.18.

A high-efficiency PPR for wide range input DC-DC converter has been proposed. The primary side switches in the half-bridge converter can achieve ZVS in full range load due to D=0.5 in primary side. Trailing edge modulation in secondary side control has been presented for fast current commutation between half-bridge converter and PPR, resulting in smaller

switching loss of Q3. The main rectifiers D1 and D2 have lower voltage stresses than the conventional half-bridge converter. PPR has higher efficiency than in the previous post regulators because of low conduction losses in the rectifiers D3 and D4 and primary side switches. Also, small input and output filters are required due to the perfect filtered waveforms. The PPR is very suitable for DPS and server power supplies for holdup time requirement.

4.5 Summary

An isolated DC-DC converter also has two main voltage spikes at high slew rate load with the same scenario as VR. The first voltage spike is mainly determined by ESR and ESL of filter capacitors and is almost independent of the close-loop bandwidth. The second voltage spike is determined by the energy stored in the filter inductor related to the close-loop bandwidth that is determined by three main delay times: filter LC, compensation network and propagation delay time. Fortunately, in isolated DC-DC converter the slew rate is only up to 10A/μs, and thus, the second voltage spike dominates, not the first voltage spike. How to optimize the close-loop bandwidth or reduce three main delay times is an effective way for fast transient response in the isolated DC-DC converter.

High switching frequency operation reduces the filter LC for high bandwidth and fast transient response. But high switching frequency causes high switching losses and large duty cycle loss due to the transformer leakage inductance, resulting in low efficiency. Therefore, high switching frequency operation for fast transient response is not an effective way from the point of converter efficiency.

Primary side control is commonly-used in the isolated DC-DC converter, but the close-loop bandwidth is limited by the 10~30 kHz pole of the optocoupler in the feedback loop. A switching mode current injection circuit is presented to inject high slew rate current in step-up load and to recover energy in step-down load to improve isolated DC-DC transient response. The switching mode current injection circuit has high bandwidth with small filter inductance with several MHZ and no optocoupler, which only activates in the transient period handling the AC current. The main converter can operate in low switching frequency handling the DC current.

A two-stage converter regulates the bus voltage in the first stage converter at low switching frequency, and the second stage converter operates in high frequency with large duty cycle, resulting in improved transient response and good efficiency. But the bandwidth of the two-stage converter is limited by the first stage converter with low switching frequency. A novel control method is proposed to improve the transient without pushing the converter into high switching frequency operation.

The complementary control converter can easily achieve ZVS in primary side and reduce the filter inductance for good transient response. But it introduces the double pole-zero effect, which complicates the compensation network design and decreases the stability and transient response. A balancing winding network is proposed to mitigate the double pole–zero effect, which will simplify the compensation network design and also improve the transient response. Moreover, the balancing winding network can be applied in other complementary control converters.

Conventional secondary side post regulators have attractive features such as ZVS in primary side and secondary side control without optocoupler in feedback loop. But conventional post regulators have large increased conduction losses because the post regulators are in series

structure, and also, it increases voltage stresses on the main rectifier, especially in a wide range input converter. A parallel post regulator is proposed to reduce the conduction loss and voltage stress of the main rectifier for better efficiency. Also, it reduces the input and output filters due to a perfect filtered waveforms. At the same time, a parallel post regulator has good transient response due to a flexible secondary side control and a small filter inductance.

CHAPTER FIVE: SUMMARY AND FUTURE WORK

5.1 Summary of High Slew Rate VR

The interleaved multiphase VR is commonly used in desktop and laptop computer systems to supply the microprocessor because of smaller input and output current ripples and good thermal capability. The new generations of microprocessors demand even lower core voltage, about 0.8375~1.6V with tighter regulation, while drawing substantially higher current up to 120A and high slew rate up to 10A/ns. Because the VR current slew rate cannot catch up with the load current slew rate, the unbalanced current between them will be provided by the filter and decoupling capacitors, and then two voltage spikes occur at high slew rate transient load. The first voltage spike is determined by ESR, ESL of capacitors, the parasitic resistance and inductance of PCB traces and socket as well. The second voltage spike is mainly determined by energy stored in filter inductors related with the unity gain bandwidth of the controller. How to design VR with good efficiency, fast transient response and small ripple is the big challenge.

The effective way to reduce their ESRs and ESLs is to parallel more capacitors. By combining different types of capacitors, the output impedance or load line can be optimized within certain frequency between the Oscon resonant frequency and the ceramic capacitor resonant frequency. Below the Oscon capacitor resonant frequency, it is easy to achieve the constant output impedance by active voltage position method. But for future higher slew rate and lower load line requirement, paralleling more capacitors close to the microprocessor is not a suitable solution due to the limitation of available space on the motherboard and the influence of parasitic resistance and inductance of PCB traces and socket.

The second voltage spike is caused by discharging the energy stored in filter inductors to output filter capacitors. More energy stored in filter inductors leads to a higher second voltage spike. Delay times of LC filters, compensation network and propagation delay time in actual controller increase the second voltage spike a lot. The effective way to reduce the second voltage spike is to reduce the filter inductance and the three main delay times in an actual controller. High switching frequency operation results in low filter inductance for high VR current slew rate. Also, it helps reduce delay times of LC filters and the compensation network for fast transient response, but high switching operation also causes low efficiency due to high switching losses.

A two-stage approach is reported in the literature for fast transient response. The first stage converter composed of two interleaved VR operates in relatively low switching frequency to generate 5V intermediate voltage bus with increased duty cycle, which has about 95 percent ~ 97 percent high efficiency at full load. The second stage converter with 4 interleaved VR operates in several MHZ with 100nH filter inductance per channel and ceramic capacitors. Because of low input voltage, better FOM lateral FETs can be used with about 0.2 duty cycle. This stage efficiency still can be up to 84 percent and the unity gain bandwidth is about 320 kHz for fast transient response. Total efficiency is the obstacle, because the two-stage approach is a cascade system. Improving the VR transient response and keeping high efficiency is the big challenge in the VR design.

AVP is a good solution to make full use of the output voltage tolerance as much as two times as conventional control methods, and thus, the number of bulk capacitors required to meet the output voltage regulation can be reduced. AVP can achieve constant output impedance within the close loop bandwidth, which means no voltage spikes will occur in transient load. In fact, AVP cannot get constant output impedance because of inaccurate current sensing and delay

times in the controller. In most VR designs, the AC load line is always higher than the DC load line. The transient response only can be optimized by improving the unity gain bandwidth, but it is impossible to reduce delay times in the controller due to the stability requirement.

Current compensator or current injection method is another reported way to improve transient response, which only activates in transient to inject high slew rate current in step-up load and absorb extra energy in step-down load by an extra converter. In other words, the current compensator mainly handles the AC current, and the main converter mainly handles DC current. Therefore, it is possible to optimize the efficiency and transient separately. There are two main circuits to implement current compensators: linear mode and switching mode current compensators, which should provide the whole unbalanced current between the VR current and load current, leading to high current stress in the extra converter. Thus, the linear mode current compensator has a large conduction loss, and the switching mode current compensator has a large switching loss. Low efficiency in the extra converter is the main barrier for applications.

Active transient voltage compensator (ATVC) is proposed to inject voltage source instead of current source in current compensator methods. ATVC also activates only in transient periods to inject high slew rate current in step-up load and recover energy in step-down load. It mainly handles the AC current, and main VR mainly handles the DC current same as do the current compensators. The difference between ATVC and the current compensators is the introduction of an ATVC transformer used to inject a voltage source. Thus, the current handled by ATVC is only 1/(1+N) of that in the current compensators, which significantly decreases ATVC switching and conduction losses. Also, ATVC has (1+N) higher slew rate current than that in the current compensator based on the same filter inductance. Furthermore, it reduces the VR output impedance impact on the output voltage because main VR is the internal loop of

ATVC circuit, so that VR output impedance can easily be suppressed by close loop control, which means that less Oscon capacitors are needed for certain transient requirements.

The delay times in a conventional linear controller based on small signal model are very difficult to eliminate due to the requirement of gain and phase margins for converter stability. A novel control method has been proposed and carried out: combined linear control and adaptive nonlinear control. Adaptive nonlinear control only activates in transient with a very small delay time generated by a hysteretic comparator. There are only 10~15mV difference at two input terminals of the hysteretic comparator. The nonlinear signal generated by hysteretic comparator is injected into conventional linear control by one shot circuit so that no stability problem exists in adaptive nonlinear control. The experimental VRM9.0 tested results show that it reduces the delay time from 2.4μs to 0.2μs.

ATVC prototype has been carried out on the Intel motherboard, which has a size of about $25\times25mm^2$ with customer control IC. By utilization of ATVC and combined linear and adaptive nonlinear control, the VR AC load line improvement is up to 90 percent of the expected AC load line improvement, and up to 25 percent of the total load line including AC and DC load line.

With the development of CPU, VR design changes from simple objective high efficiency in the beginning to multiple requirements, such as high efficiency, fast transient response, high power density and low cost. Some of them are contradictive to each other, such as high efficiency and fast transient response. How to optimize VR design with both high efficiency and fast transient response is the challenge and is also a good opportunity for us. ATVC is a good solution in this direction.

5.2 Summary of Transient Improvement in Isolated DC-DC Converter

Many efforts have been put into VR transient response improvement, but few efforts have been put into isolated DC-DC converter. Although many technologies developed in VR can be used directly into isolated DC-DC converter, special requirements on the isolated DC-DC converter are the galvanic isolation and less than 10A/μs output current slew rate. Thus, many opportunities can be explored to optimize the transient response in the isolated DC-DC converter.

First, in a DC-DC converter, primary side control is the most popular way to use an optocoupler to isolate the feedback signal. Unfortunately, the optocoupler has around 10~30 kHz low bandwidth limitation, which deteriorates the transient response. Switching mode current injection circuit has been studied in the secondary side of the converter, which has fast transient response because of low filter inductance in high frequency and no optocoupler in control loop. In an experimental prototype, switching mode current injection circuit has up to 250 kHz bandwidth and has great transient response. In fact, this approach is suitable for low current, not for high current because of high current stress.

Second, a simple novel control is proposed for a two-stage isolated DC-DC converter to improve the transient response. In the conventional control for a two-stage converter, the first stage converter generates an intermediate voltage bus at relatively low switching frequency and the second stage converter can operate at large duty cycle or 0.5 duty cycle for good efficiency and small magnetic size by using two independent controllers. Therefore, the transient response is mainly determined by a low bandwidth converter, such as the first stage converter, which has a unity gain bandwidth that is limited by the large LC and low switching frequency. There are always tradeoffs between the efficiency and transient response. The novel control method

utilizes only one control IC to regulate both the first stage and the second stage converter, which increases the total DC gain and extends the maximum duty cycle to 0.66 in second stage converter, thus it can benefit both the transient response and efficiency.

Third, complementary controlled converter can easily achieve soft switching in primary side by utilizing the energy stored in the leakage inductance, leading to high efficiency and high frequency operation. But it introduces the double pole-zero effect composed of the magnetizing inductance and the equivalent blocking capacitor in the converter. Double pole-zero effect harms the stability, complicates the design of the linear controller design and deteriorates the transient response. A balancing winding network has been proposed to eliminate the double pole-zero effect, which is composed of one winding same turn as primary winding, two small diodes and one blocking capacitor. In steady state, the unbalanced voltage between two input capacitors in HBCC converter can be balanced by the balancing winding network. In transient loads, the blocking capacitor in the balancing winding network acts as an energy buffer to provide or absorb unbalanced energy between the converter and load without any delay time. Therefore, it can reduce the delay time effect in the actual controller and mitigate the double pole-zero effect, which simplifies the compensation network design and improves the transient response.

Fourth, a parallel post regulator is proposed for high efficiency and high transient response isolated DC-DC converter with secondary side control, which has advantages, such as no optocoupler and fast transient response. Most of the conventional post regulators have soft switching capability in primary side due to 0.5 duty cycle operation, but they are in series with the secondary side main rectifier causing large conduction loss, especially in wide range input applications such as server power for hold up time requirement. This is because the converter operates at high input voltage at low efficiency with low input voltage design, which leads to

difficult ZVS in primary side and high voltage rating both in the main rectifier and the post regulator. Parallel post regulator only handles a small portion of output power; most of them are handled by the unregulated main rectifier with very high efficiency, so it is easy to achieve high efficiency for the total system. It also can reduce the secondary side voltage rating in the rectifier and post regulator due to high turn ratio transformer. In an experimental prototype, parallel post regulator has up to 8 percent improvement compared with a conventional half-bridge converter.

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