ENTIRE LOAD EFFICIENCY AND DYNAMIC PERFORMANCE IMPROVEMENTS FOR DC-DC CONVERTERS

by

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To my parents

ABSTRACT

Demands for DC-DC converters are continuously increasing for the application in many areas such as telecommunications, cellular telephones, networking products, notebook and desktop computers, industrial instrumentation, and automotive electronics. These areas are continually being upgraded with regard to their specifications and power requirements; this puts the emphasis on power electronics and power management. DC-DC converters are able to supply energy at high standards and specifications, which leads DC-DC converters to be continually upgraded in order to fulfill other application requirements such as efficiency, dynamic performance, thermo, noise and size.

The scope of this work can be summarized into three main aspects for DC-DC power converters. The first aspect is soft switching topologies to improve conversion efficiency for On-Board Converters or Point of load (POL) converters (chapters 2, 3); the second aspect is load adaptive control techniques to improve all load efficiency for battery powered DC-DC converters that are applied to mobile devices (chapters 4, 5); and the third aspect is dynamic performance control techniques to improve load transient in voltage regulators (chapters 6, 7). Topologies and control techniques for DC-DC converters are presented after reviewing loads powering requirements and steady-state and transients design challenges.

Following is a quick overview of the presented topologies and control techniques that sum up the work of this research:

- In chapter 2, Active Resonant Tank (ART) cells are presented to achieve Zero-Voltage-Switching (ZVS) and eliminate body-diode conduction and its reverse recovery in dc-dc converters with Synchronous Rectifiers (SRs). ART cells extend the benefits of utilizing SRs to higher voltage applications, since switching losses tend to be more significant in higher voltage ratings SRs because they have worse parasitic. The concept of current injection in ART cells is generally introduced and detailed analyses are provided based on a buck converter. Experimental results show that efficiency improvement is achieved due to the reduced switching loss, body diode's conduction, and reverse-recovery loss.

- In chapter 3, LCC ZVS Buck Converter with Synchronous Rectifier is presented. The concept of the LCC ZVS buck converter topology introduces an inductive load in the bridge leg and changes the switching commutation mechanism of the SR to achieve Zero-Voltage-Switching (ZVS) and eliminate body-diode conduction and its reverse. Compared with the conventional SR buck converter, reverse-recovery-related switching and ringing loss are eliminated; compared with QSW buck converter, the output current ripple is significantly reduced and the output capacitance is dramatically reduced.

- In chapter 4, load Adaptive Control for Improved Light Load Efficiency and Performance of Voltage Regulator (VR) is presented. Analytical studies of VR losses and voltage ripple deviation are presented and discussed, yielding to proposed control technique, namely "Pulse Sliding**" (PSL) control technique, which results in improved VR conversion efficiency with low and controlled voltage ripple and improved dynamic

response. The presented control method achieves the advantages of both variable frequency and fixed frequency controls and eliminates their disadvantages by utilizing information obtained from the inductor peak current, compensation error signal and output capacitor current, resulting in an optimum non-linear switching frequency modulation. PSL is compared with other control methods by both analyses and experiments.

- In chapter 5, a load adaptive voltage regulator that achieves high efficiency extended to light and heavy load regions is presented. It is named as "Adaptive FET Modulation" (AFM) since multiple FETs with different specifications are paralleled; the number of driven FETs and their gate driving voltage are adaptive to load current. The capability of adaptive modulation of FETs' parasitic charges and resistances along with adaptive gate driving voltage allows achieving the best FET optimization for wide load range. AFM operates at fixed switching frequency for almost the whole load range, so it has no affect on the conventional buck operation and its dynamic performance, in addition to having simple implementation.

- In chapter 6, the discussion centers upon a control method that dynamically modulates the PWM ramp signal peak during DCM or Mode Hoping operation with inverse relationship to the compensator error signal, as a result modulate the PWM modulator gain to minimize the required error signal change during load transient, so that the

compensator reaches steady state faster and lower output voltage deviation during load transient is achieved.

- In chapter 7, an approach to significantly limit the voltage overshoot and undershoot during load transient and reduces the number of capacitors, without compromising on the efficiency, cost or size of the dc/dc converter. It allows optimization of power stage efficiency for the dc operation with less concern of dynamic performance, while an additional switching circuit; that utilizes the output capacitor current to rapidly detect load transient; is activated during load step up to deliver the shortage charge to the output capacitor, and to pull out the extra charge from the output capacitor during load step down. Therefore, lower voltage deviation is achieved during load transient.

- Finally, the work is summarized and concluded, and references are listed

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CHAPTER 1: INTRODUCTION

Demands on DC-DC converters are continuously increasing to be applied in many areas such as telecommunications, cellular telephones, networking products, notebook and desktop computers, industrial instrumentation, and automotive electronics. DC-DC converters must be able to supply energy at high standards and specifications, which forces DC-DC converters to a continuous improvement to be able to fulfill other applications requirements pertaining to efficiency, dynamic performance, thermo, noise and size.

DC-DC converters are mostly required to be physically small; this requires the increase of switching frequency since high switching frequency permits capacitors and magnetic components to have smaller size; also, faster switching frequency has the benefit of better dynamic performance for faster response. The issue that rises up when increasing the switching frequency is the efficiency since switching frequency and efficiency are inversely proportional. On the other hand, converters with smaller sizes face thermal issues especially at high currents due to increased conduction losses. Given that power losses transform to heat, it is more challenging to dissipate this heat out of converters with smaller sizes; the temperature rise caused by poor heat flow degrades device performance and therefore the converter's efficiency.

In order for a power converter to operate at high switching frequency while maintaining good performance, high efficiency, and acceptable temperature, it is essential to investigate where and how energy is lost inside the power converter. Mainly, losses in power converters are divided into switching losses and conduction losses.

Switching losses are due to electrical charges lost in the process of turning on and off the switching devices; they are basically the energy lost in charging and discharging the FET's gate capacitor, or what are called driving losses: energy losses associated with the FET's junction capacitor, reverse recovery losses of diodes, or FET's body diode and other switching losses caused by the switching devices parasitics. These kinds of losses get more significant at higher frequencies. In order to reduce such losses, many techniques can be applied to recover the energy stored in the MOSFET's gate capacitor. In addition to applying soft switching where switching devices can switch at zero voltage or zero current, soft switching also lowers EMI noise and speeds the turn on speed and lower the gate drive power in some cases due to the absence of Miller's effect.

Conduction losses are due to the energy flow through components and switching devices. They are basically the energy lost in the components resistance: the switches' on-resistance and diodes or MOSFET's body diode voltage drop. These kinds of losses get more significant in high-current applications. In order to reduce conduction losses, energy must be processed through the least possible number of components with avoidance of circulating energy; components and switching devices should be selected to have the least resistance and voltage drop. In addition, converter parameters such as inductor value, switching frequency, and the input-to-output voltage ratio should be designed properly that considers current ripple and its rms, since conduction losses are directly related to rms current value.

Understanding the causes behind each loss, it is possible to reduce the type of losses that can be dominantly affecting the converter's efficiency. For example, in order to improve efficiency at heavy loads, it is beneficial to reduce conduction losses even at the expense of increased switching losses since conduction losses dominate the total power loss ate heavy load. On the other hand, if light load efficiency improvement is desired, it is beneficial to reduce switching losses even at the expense of increased conduction losses since switching losses dominates the total power losses at light loads.

Power requirements vary from one application to another. In mobile applications, the main concern is to extend the battery life, such applications draw light power most of the time. Therefore, it is essential to improve the light load efficiency for converters applied in battery powers devices. Load adaptive schemes can be used to adapt power delivery to different load demands [61, 62]. This could be done by adjusting control parameters or by modifying the hardware/components structure of the power stage, or both. While in other applications such as telecommunications, converters have higher input voltages, compared to mobile applications, and are required to deliver higher currents. Thus, it is necessary to reduce power losses at heavy load in order to limit the temperature rise. Applying soft switching to such applications is desired since switching losses are more significant at higher input voltages [63-65]; also, FETs' parasitics tend to be worse for higher voltage rating FETs.

Demanding high power applications, such as fast processors and pulsed loads, require new levels of performance from dc-dc converters. The requirements of high slew rate of load current with minimal output voltage deviation along with high conversion efficiency, small size and low cost, are all contradicting requirements for the dc-dc converter design. Literature includes many approaches to significantly limit the voltage overshoot and undershoot during load transient and reduce the number of capacitors, without compromising on the efficiency, cost, or size of the dc-dc converter.

Following are literature reviews and brief introductions of proposed soft switching topologies, load adaptive control techniques, and dynamic performance improvement methods.

1.1 Soft switching topologies

1.1.1 Literature review of soft switching topologies

With demanding powering requirements of fast transient response and high power density, the converters' switching frequencies keep increasing resulting in increased switching loss. Recently, soft-switching techniques drew a lot of attention in reducing switching loss and EMI noises. Among them, particularly, zero voltage switching (ZVS) techniques are desirable for MOSFET-type switches. ZVS multi-resonant converters (MRCs) technique utilizes all major parasitic of the power stages and all semiconductor devices in MRC operate with ZVS [1], which substantially reduces the switching losses and noise. Quasi-resonant converters (QRCs) were introduced to overcome the disadvantages of conventional PWM converters operating at high

switching frequency by achieving ZVS for the active switch and zero current switching (ZCS) for the rectifier diode [2,11]. However, the switches in both QRCs and MRCs have to withstand high voltage stress or high current stress [12, 14], which restricts the applications of those resonant converters. By reducing the filter inductance in the conventional PWM converters, ZVS quasi-square-wave (QSW) technique offers ZVS for both the active and passive switches without increasing the switches' voltage stress [3, 4, 13]. However, QSW converters suffer high current stress in components, as a result, conduction losses are greatly increased, and active switches turn off at high currents. In [5-6], a similar concept of QSW is presented with an LC cell in parallel with the active switch or rectifier diode. The cell consists of a small inductor Lr in series with a large capacitor Cc, and the cell's high inductor current ripple is utilized to achieve ZVS turn-on for the active switch. However, the current ripple in the cell's inductor Lr is more than twice that of the one in the filter inductor, and the associated conduction and turn-off loss increase is significant.

To facilitate ZVS while preserving the advantages of the PWM technique, hybrid topologies incorporate PWM technique and resonant converters in order to minimize circulating energy and corresponding conduction loss and switching loss. Adding an auxiliary switch across the resonant converter in a ZVS-QRC derives ZVS-PWM converter, which can be considered as hybrid circuits of ZVS-QRCs and PWM converters [9], wherein ZVS is achieved for the power switch and the converter operates at a constant switching frequency. However, the power switch suffers from a high voltage stress that is proportional to the load range. Compared with ZVS-PWM converter, zero-voltage-transition PWM (ZVT-PWM) converters [10, 12] are more

desirable since soft switching is achieved without increasing switch voltage and current stress. By adding an auxiliary shunt network to discharge switch junction capacitance and shift the rectifier diode current, ZVS is achieved for switch and reverse recovery of rectifier diode is attenuated.

1.1.2 Proposed soft switching topologies

1.1.2.1 Active Resonant Tank (ART) for zero-voltage-switching DC-DC converters with synchronous rectifiers

Active Resonant Tank (ART) cells are to achieve Zero-Voltage-Switching (ZVS) and eliminate body-diode conduction and its reverse recovery in dc-dc converters with Synchronous Rectifiers (SRs). During transition of the switches, SRs' parasitic body diodes unavoidably carry load current, which decreases conversion efficiency because voltage drop across body diodes is much higher than that across SRs. In addition, reverse recovery of the body diodes leads to increased switching losses and Electromagnetic Interference (EMI). Even so, in low-output-voltage dc-dc converters, SRs are widely utilized to reduce rectifier conduction loss and improve converter efficiency since the saved conduction losses overcome the switching losses. However, in higher voltage applications, which require the higher voltage rating FETs or SRs, the benefits of utilizing SRs are limited since switching losses tend to be more significant. This is so because SRs with higher voltage ratings have worse parasitic, and conduction losses appear to be less since the current is less for the same power level. With the proposed cells of active resonant tank, the body diodes are never involved during switching transition, and thus body diode conduction

loss is saved, and reverse-recovery-related switching loss and ringing are eliminated, in addition to achieving zero voltage switching (ZVS) for the active or main switch. The resonant tank cells consist of a network including LC resonant tank and an active switch. Basically, prior to the turn-off of the SR, the energy stored in the tank capacitor is released through the resonant inductor to reverse the current in the SR to avoid body diode conduction and eliminate recovery loss, and then discharge the main switch junction capacitance, so that the main switch turns on at ZVS. During the following interval, the resonant tank cell recharges in a resonant manner. Since energy communication occurs only during switching transition, conduction loss dissipated in the resonant tank is limited. Moreover, the auxiliary active switch turns on at ZCS and turns off at ZVS and the SRs operate at ZVS. The concept of ART cells is introduced in a general manner, and detailed analyses are provided based on a buck converter, and experimental results show that efficiency improvement is achieved due to the reduced switching loss, conduction of the body diode and reverse-recovery loss.

1.1.2.2 LCC ZVS buck converter with synchronous rectifier

The motivation is the same as that for the ART converter discussed above, which is the limitation of SR usage in high voltage applications due the increased switching losses. This differs from the ART since it has no additional switch which makes it a passive cell instead of an active cell or tank.

The concept of the LCC ZVS buck converter topology is introducing an inductive load in the bridge leg and changing the switching commutation mechanism of the low-side SR switch. In

other words, in the conventional buck converter with SR, the SR operates at capacitive load. When the SR turns off, the current flows through the body diode; as a result, the reverse recovery of the body diode occurs with the turn-on of the high-side switch. While in the proposed converter, the SR turns off at inductive load, and the inductive current will not flow through the body diode of the SR. Moreover, the inductive current is utilized to discharge the junction capacitance and achieve ZVS for the high-side switch. Therefore, compared with the conventional SR buck converter, reverse-recovery-related switching and ringing loss is eliminated; and compared with QSW buck converter, the output current ripple is significantly reduced and the output capacitance is dramatically reduced. A prototype was built to compare the conventional Buck converter, QSW buck converter, and the proposed LCC ZVS buck converter. The experimental test shows that the proposed converter is advantageous over the conventional buck converter at high switching frequency, where the switching loss dominates the total power loss. The experimental test results also show that the LCC buck converter is advantageous over QSW converter in current and output voltage ripples and efficiency in wide range of switching frequency; it also has half the input current di/dt compared to the QSW converter.

1.2 All load efficiency improvement control techniques

1.2.1 Literature review of all load efficiency improvement techniques

Unlike many Voltage Regulator (VR) applications where achieving high efficiency toward the full load is the most important factor—even at the expense of low efficiency under light load—

high efficiency at all load conditions including light load is required in other applications such as those that are battery-powered and have constrains in energy consumption [17-20]. For such applications, this becomes even more important when the load power consumption is dynamically varied with applications or usage conditions such as DSP (Digital Signal Processor) and ICs (Integrated Circuits) in portable computers and handheld devices. On the other hand, other applications target achieving maximum efficiency at heavy load with less concern of light load efficiency in order to minimize the generated heat inside the converter [20].

Figure 1.1 shows a power consumption of an Intel Centrino® Mobile Technology based system under different usage or application conditions [23] as an example. As can be noted, both the CPU power and platform power drawn from the power delivery or VR vary rapidly and frequently with time as usage conditions or applications change. This load/power variation covers a wide load range including light loads. Moreover, as DSPs and the platform become more power managed (by software or hardware), the percentage of time during which a specific VR or power delivery operates at lighter loads becomes larger. Therefore, platform power delivery efficiency at all load levels including lighter loads is very important for extended energy savings and battery life.

Power conversion structure, parameters, components and control are usually selected and optimized to: 1) peak efficiency at specific load or power level, at the expense of lower efficiency at other load levels, 2) to satisfy performance requirements such as steady-state ripple and transient deviation specifications, and 3) to reduce size and cost. To improve efficiency and

performance, load adaptive schemes can be used to adapt power delivery to different load demands. For example, this could be done by adjusting the control or control parameters of the power stage, by adjusting the hardware/components structure of the power stage, or by adjusting both. The objective is always to achieve the best possible power conversion efficiency with the best possible steady-state and dynamic performance over wide load range, which should meet load requirements and demands with minimum size and cost.

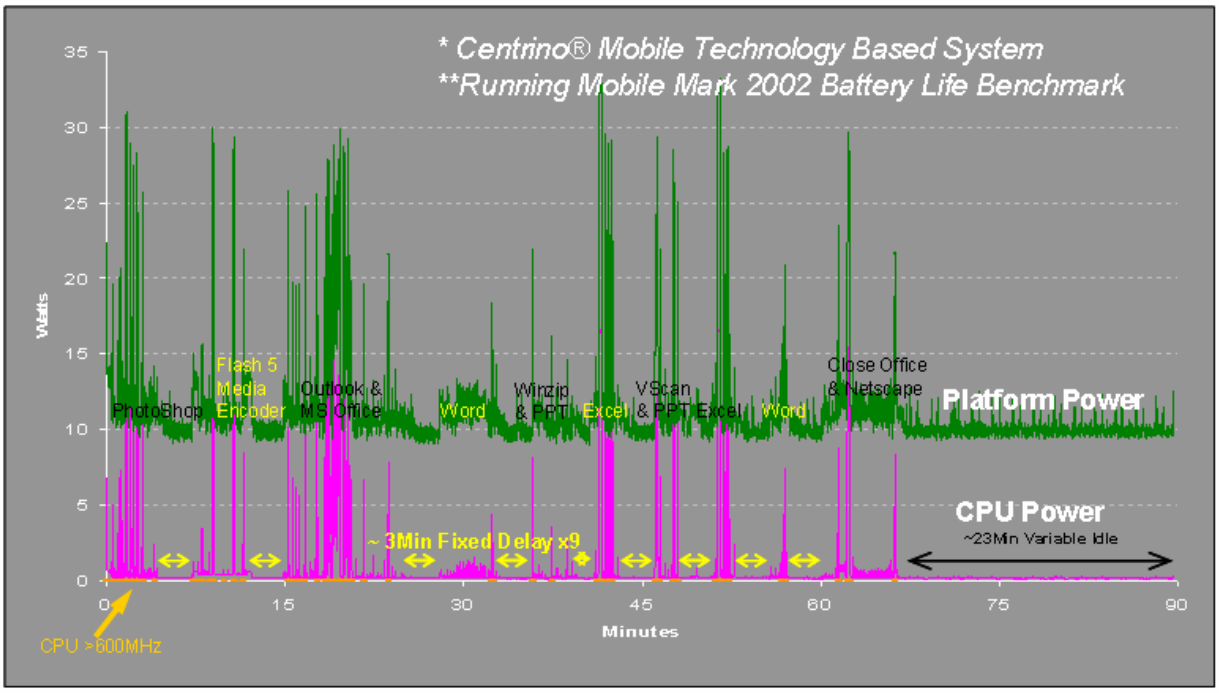
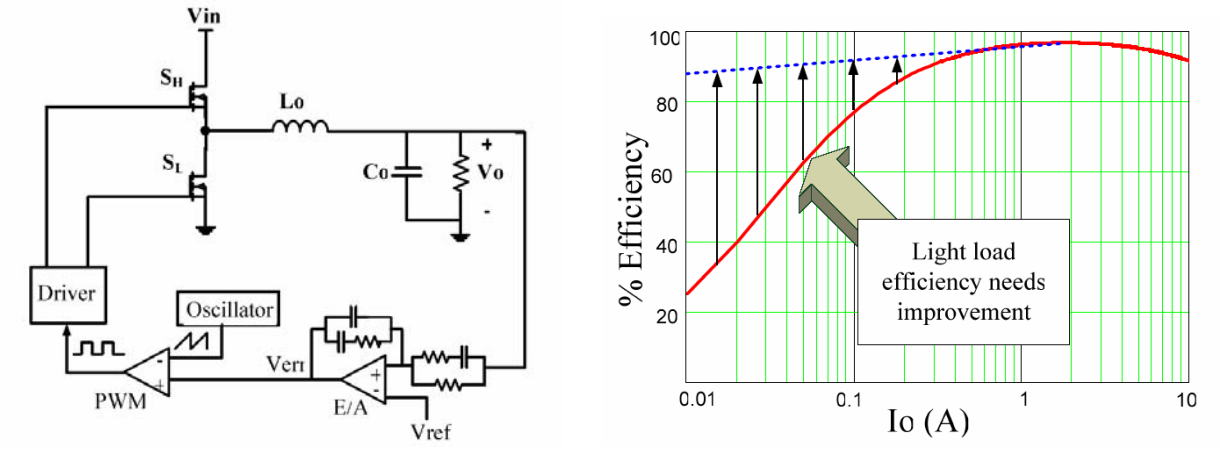


Fig. 1. 1: *Example of Power Consumption Benchmark of an Intel Centrino® Mobile Technology based system under different usage and applications conditions: Top Curve for Platform Power and Bottom Curve for CPU Power.*

Figure 1.2 shows an example of a typical buck VR and efficiency curve. In order to "flatten" such efficiency curve or improve light load efficiency, several techniques can be applied such as

Mode-Hopping and Pulse Skipping [17, 18, 28, 29, 35]. In Mode-Hopping technique (MH), the DC-DC Buck VR operates in both synchronous and asynchronous modes. It operates in synchronous mode at CCM (Continuous Conduction Mode) under medium to heavy load demands, where the inductor current does not reach zero or below. It operates in asynchronous mode at DCM (Discontinuous Conduction Mode) under light load demands, where the inductor current starts approaching the zero amperes point, to mainly reduce conduction losses [20, 29]. While in Pulse-Skipping or variable switching frequency technique, the VR switching frequency is lowered as the load becomes smaller in order to reduce switching and driving losses. This can be implemented by using hysteretic control or variable frequency PWM control [21, 31]. Both techniques result in efficiency improvement especially under light loads. However, they also cause an increase in output voltage ripple and possibly impact the dynamic and steady-state performances of the VR [33, 34], which are important for ICs operation performance, especially for those that are highly integrated and operate under a low normal voltage level. In [22], the gate drive voltage dynamically scales relative to load current, so that gate drive loss is reduced at light load. Efficiency improvement due to this technique is limited since there are other switching losses that degrade light load efficiency besides driving losses.



(a) *(b)*

Fig. 1. 2: (a) Buck VR and (b) Typical buck VR and efficiency curve.

In [46], a multiphase buck converter technique with non-uniform current sharing and phase-picking was proposed, which also improves light load efficiencies. However, multiphase buck topology is more favorable in high current applications. In low power applications that do not require more than one phase and that are area constrained, it is preferred to process power through a single phase and optimize the design for a wide range of load current.

Another way to improve light load in interleaved multi-phase buck is through what is called the "baby buck" [26], a small phase that is optimized for low power is activated only at light load conditions.

In a tapped inductor buck [27], the duty ratio is extended mainly to reduce peak current, which reduces turn off losses. But the leakage inductance of the tapped inductor causes a severe voltage spike across switching devices. And the energy trapped in the leakage inductance is also

dissipated in each switching cycle and generates large power losses. Many techniques are used to solve the voltage spike problem and recover the leakage inductance energy. But these techniques require additional parts or more complicated magnetic design, which takes away the simplicity feature of a buck regulator.

1.2.2 Proposed load adaptive techniques for all load efficiency improvement

1.2.2.1 On load adaptive control of voltage regulators for power managed loads: control schemes to improve converter efficiency and performance

Efficiency improvement, especially at light load currents, is important in many applications including those that are battery powered and have energy consumption constraints. However, controlled steady-state and dynamic performance should be maintained while improving efficiency. An analytical study of VR losses and voltage ripple deviation is presented and discussed, yielding to a proposed control technique, namely "Pulse Sliding**" (PSL) control technique, which results in an improved VR conversion efficiency with low and controlled voltage ripple and improved dynamic response. The proposed control method achieves the advantages of both variable frequency and fixed frequency controls and eliminates their disadvantages by utilizing information obtained from the inductor peak current, compensation error signal and output capacitor current, resulting in an optimum non-linear switching frequency modulation. PSL is compared to other control methods by both analyses and experiments. Experimental results highly agree with theoretical analyses.

1.2.2.2 Adaptive FET modulation for voltage regulator efficiency improvement

A load adaptive voltage regulator that achieves high efficiency extended to light and heavy load regions is named "Adaptive FET Modulation" (AFM). Since multiple FETs with different specifications are paralleled, the number of driven FETs and their gate driving voltage is adaptive to load current. The capability of adaptive modulation of FETs' parasitic charges and resistances along with adaptive gate driving voltage allow achievement of the best FET optimization for wide load range. AFM operates at fixed switching frequency for almost the whole load range, so it has no effect on the conventional buck operation and its dynamic performance, in addition to having simple implementation. Concept, design, analyses and experimental results of the AFM are presented.

1.3 Dynamic performance improvement methods

1.3.1 Literature review of dynamic performance improvement methods

With the continuous upgrades of CPU's, challenges keep rising for voltage regulators to meet the power requirements, such as the low output voltage, high current with high slew rate, and high efficiency with high power density and good thermal performance. Some of these requirements contradict each other, such as the high slew rate and high efficiency. A high slew rate needs small filter inductance, but this leads to high current ripple which increases the conduction and switching losses. Interleaved multiphase VR can reduce the input and output current ripples and it has good distributed thermal capability which is commonly used in desktop and laptop

computer system to power the CPU [48]. In high slew transient, the VR current cannot catch up with load current immediately: the unbalanced current will be provided by filter and decoupling capacitors; thus, two transient voltage spikes occur in the VR output voltage [46]. The first voltage spike is determined by ESR, ESL of capacitors, and the second voltage spike is mainly determined by the energy stored in filter inductors related to the close-loop bandwidth [46, 47]. In order to reduce the transient voltage spikes, typically a large number of capacitors are mounted close to the processor on the motherboard for lower ESRs, ESLs. Unfortunately, the available space on the motherboard makes it difficult to add more capacitors for the increasing slew rate. Furthermore, increased motherboard capacitors have limited effect on the voltage spike suppression due to the existence of resistance and inductance of PCB traces and socket [46, 48]. The effective way to reduce the second voltage spike is to reduce the delay times in controller, especially in large signal transients. There are three main delay times in VRs: LC filter, compensation network, and the IC propagation delay times. How to reduce those delay times in a simple way is a challenge and needs a tradeoff between fast transient response and high efficiency.

The barrier of output VR current slew rate is determined by the VR equivalent inductance and its applied voltage. High switching frequency operation helps to reduce its LC filter for high bandwidth, but it introduces higher switching loss. Recently many other efforts have been put into the VRs to improve the transient response by reducing the output impedance or load line [49-56, 59, 60].

1.3.2 Proposed dynamic performance improvement methods

1.3.2.1 Dynamic PWM ramp signal to improve load transient in DCM and Mode-Hoping operation

The requirement of high slew rate of load current with minimal output voltage deviation is challenging. In case of load transient in CCM operation, the duty ratio is almost constant over the load current range; it slightly changes to compensate the extra losses and keep output voltage regulation. While in DCM and Mode Hoping operation, duty ratio varies significantly in case of load transient, the control loop is required to update the compensation error signal, consequently, the duty ratio, as load current varies. Since it takes longer time for the compensator to reach the steady state in cases of large duty cycle variation (DCM operation), the output voltage deviation during load transient is drastically increased when operating in DCM compared to CCM operation. Proposed is a new control method that dynamically modulates the PWM ramp signal peak, which in turn modulates the PWM modulator gain, to minimize the required error signal change during load transient, so that the compensator reaches steady state faster. Therefore, lower output voltage deviation during load transient can be achieved.

1.3.2.2 Transient response improvement in DC-DC converters using output capacitor current for faster transient detection

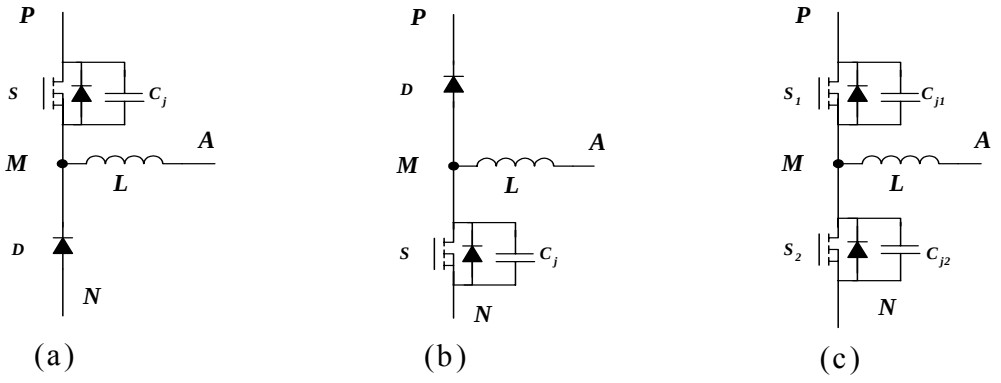
Proposed is a new approach to significantly limit the voltage overshoot and undershoot during load transient and reduce the number of capacitors without compromising on the efficiency, cost

or size of the dc-dc converter. It allows optimization of the power stage efficiency for the dc operation with less concern of dynamic performance, while an additional switching circuit; that utilizes the output capacitor current to rapidly detect load transient, is activated during load step up to deliver the shortage charge to the output capacitor, and to pull out the extra charge from the output capacitor during load step down. Therefore, lower voltage deviation is achieved during load transient.

CHAPTER 2: ACTIVE RESONANT TANK (ART) FOR ZERO-VOLTAGE-SWITCHING DC-DC CONVERTERS WITH SYNCHRONOUS RECTIFIERS

2.1 General concept

Buck, boost, and buck-boost dc-dc converters are the most common non-isolated dc-dc converters. Each converter is composed of a 3-terminal cell as shown in Fig. 2.1, wherein Fig. 2.1 (a) shows a cell with a diode rectifier for Buck and Buck-Boost converters, where Cj is MOSFET's junction capacitance. Figure 2.1 (b) shows a cell for Boost converter with diode rectifier. Replacing the rectifier diode by an SR in the three basic dc-dc converters, a common cell is derived as shown in Fig. 2.1(c). For Buck and Buck-Boost converters, MOSFET S1 functions as an active switch and MOSFET S2 functions as a SR, and vice versa for the Boost converter,



(a) Buck and Buck-Boost's cell (b) Boost's cell (c) Common cell with a SR

Fig. 2. 1: Cells in non-isolated dc-dc converters

Reviewing the principle of switching commutation in a conventional dc-dc converter with a SR, the active switch operates at hard switching, while SR operates at ZVS turn-on. Buck converter cell is shown in Fig. 2.2 with the current injection cell excluded, and the associated key waveforms are shown in Fig. 2.3(a) assuming switches are ideal and the inductance current is constant. When Switch S1 turns off, inductor current charges junction capacitance C_{j1} and discharges junction capacitance C_{jSR} until voltage across C_{jSR} reaches zero, and the body diode Db_SR conducts current; after that SR turns on with ZVS and inductor current freewheels through SR. Freewheeling mode ends up with the turn-off of the SR forcing inductor current to shift from SR to its body diode Db_SR. Then Switch S1 turns on with the junction capacitance C_{j1} discharging through S1. Due to the SR's body-diode reverse-recovery current, the active switch S1 suffers from extra turn-on loss and the SR's body diode suffers from hard turn-off loss. In short, in the Buck converter, active switch S1 operates at undesirable conditions due to hard turn-on; the SR operates at ZVS turn-on, but the body diode's reverse recovery leads to extra switching loss and EMI problems. Because the body diodes' reverses-recovery characteristic becomes worse with increase of MOSFETs' voltage rating, SR's applications are still limited to low voltage range.

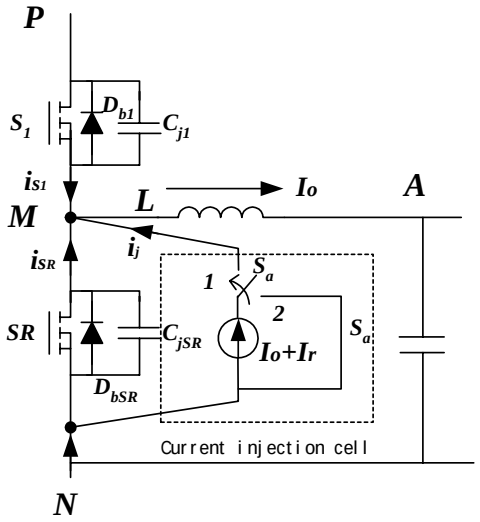


Fig. 2. 2: Concept of current injection cell in a Buck converter

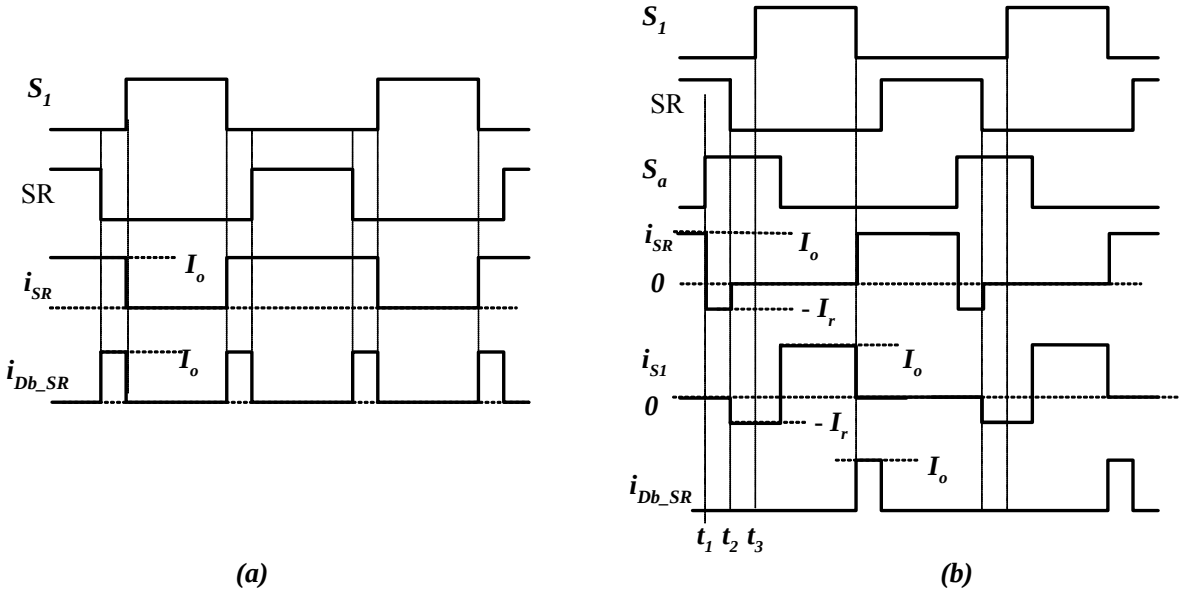


Fig. 2. 3: Key Concept of current injection cell

2.2 Current injection cell to achieve zero-voltage-switching (ZVS)

From the analyses of switching operation in Buck converter, we observe that the SR's turn-on and Switch S_1's turn-off are desirable, while the SR's turn-off and Switch S_1's turn-on are undesirable due to S_1's hard turn-on and reverse-recovery of the SR's body diode. The ideal switching operation is: all switches of the body diodes conduct prior to turn-on of the switches, and all switches turn off with inductive load instead of capacitive load. In other words, to avoid hard turn-off of the body diode, the current commutation sequence must be from a switch to the body diode of the other switch instead of from a body diode of a switch to the other switch.

As shown in Fig. 2.2, a current injection cell is placed in parallel with the SR to help Buck converter to achieve an ideal switching commutation discussed above. Switch Sa is turned "on" at Position "1" to inject current I_r+I_o in the converter. The key waveforms are given in Fig. 2.3(b) assuming switches are ideal and the inductance current is constant. Basically, the cell is utilized to ensure the SR turns off at inductive load and its body diode is not involved in during the turn-off interval. During freewheeling mode while $t < t_1$, SR carries freewheeling current: $i_{SR}(t) = I_o$. At $t = t_1$, the cell is activated and a current is injected into the node M, where the equation $i_{SR} + i_j = I_o$ is satisfied, forcing SR current to reverse with $i_{SR}(t_1) = -I_r$. At $t = t_2$, SR turns off and current I_r charges the junction capacitance C_{jSR} and discharges C_{j1}, and eventually the body diode D_{b1} is involved to carry current I_r. At $t = t_3$, Switch S1 turns on at ZVS. During the interval $t_1 < t < t_3$, SR's body diode never conducts, thus the body diode reverse recovery loss is eliminated; moreover, the active switch S_1 achieves ZVS with the help of current injection cell.

Therefore, both the SR and the active switch operate at ZVS conditions, and the converter operates at desirable conditions.

2.3 Implementation of the current injection cell with (ART)

Fig. 2.4 shows two candidate circuits consisting of a LC tank and an active switch. Assuming the resonant capacitor Cr is pre-charged to $2V_{PN}$ and SR is on to carry freewheeling current I_o. With the turn-on of the active switch S, the capacitor Cr starts to charge the resonant inductor Lr as a resonant manner through the switch SR. Ignoring the power loss during the resonance, the current in the resonant inductor Lr is given by:

$$i_{Lr}(t) = \frac{2V_{PN}}{L_r\omega_o}\sin(\omega_o t) \qquad \left(0 \le t \le \frac{\pi}{2\omega_o}\right) \qquad \textit{Eq. 2. 1}$$

The resonant capacitor voltage is given by:

$$v_{cr}(t) = 2V_{PN}\cos(\omega_o t) \qquad \left(0 \le t \le \frac{\pi}{2\omega_o}\right) \qquad \textit{Eq. 2. 2}$$

where $\omega_o = \frac{1}{\sqrt{L_r C_r}}$, the resonance ends with resonant capacitor voltage reaches zero: $V_{Cr}= 0$, and the resonant current reaches its maximum as:

$$I_j = I_{L_r \max} = \frac{2V_{PN}}{Z_0} \qquad \textit{Eq. 2. 3}$$

Where the circuit characteristic impedance, Z_0, defined as:

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \qquad \textit{Eq. 2. 4}$$

After that, resonant inductor current freewheels through the diode D in the ART cell. If the injected current is larger than output current, $I_j > I_o$, the SR current is reversed during the freewheeling duration of the resonant inductor, $I_{SR} = I_o - I_j$. Later on, SR turns off, the additional inductor energy is utilized to charge the junction capacitance C_{jSR} and discharge C_{j1}. Therefore, the additional inductor energy must be at least equal to the energy stored in C_{jSR} and C_{j1} for the body diode of switch S_1 to conduct and for the switch S_1 to turn on at ZVS, this condition implies the following:

$$\frac{1}{2}L_r(I_j - I_o)^2 \geq \frac{1}{2}(C_{jSR} + C_{j1})V_{PN}{}^2 \qquad \textit{Eq. 2. 5}$$

With the turn-on of the switch S_1, the node M is connected to a voltage source, the inductor current decreases to zero and becomes negative, then the resonant capacitor starts charging in a resonant manner. During the capacitor-charging period, the cell switch S turns off at ZVS. The resonance ends with inductor current going back to zero and the capacitor voltage reaches $2V_{PN}$. It should be noted that the cell switch is activated only during the current commutation interval from the SR to S_1.

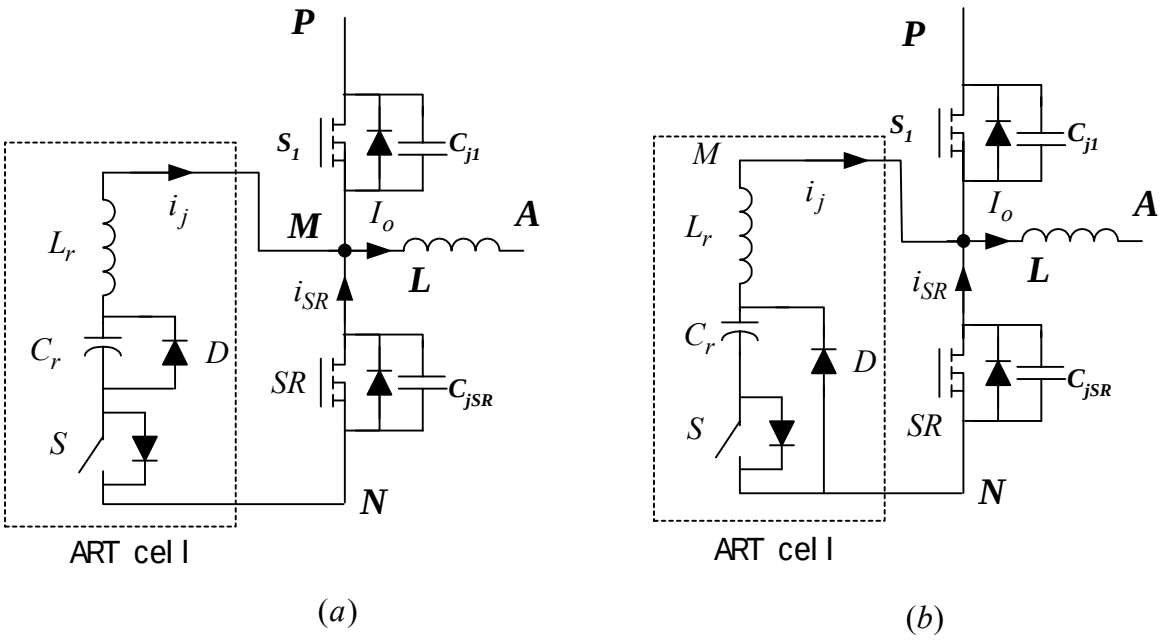


Fig. 2. 4: Active resonant tank (ART) cells

2.4 Modes of operation analyses

The ART cell can be applied to common bridge cells of non-isolated converters. Since the cell's principle of operation is similar in different topologies, this section presents detailed analyses of the SR Buck converter with the ART cell as an example, as shown in Fig. 2.5. The ART switch is implemented using a P-channel MOSFET that requires a negative gate driving voltage.

To simplify the analyses of operation, components are considered ideal except otherwise indicated. The output filter inductance is assumed large enough and the inductor current is constant in all the modes. The main equivalent circuits for main operation modes are shown in

Fig. 2.6 and the key waveforms are shown in Fig, 2.7; it should be noted that the time scale in Fig. 2.7 is magnified during the transition period between switches S1 and SR in order to clarify the modes of operation of the presented ART cell. The modes of operation are described as follows:

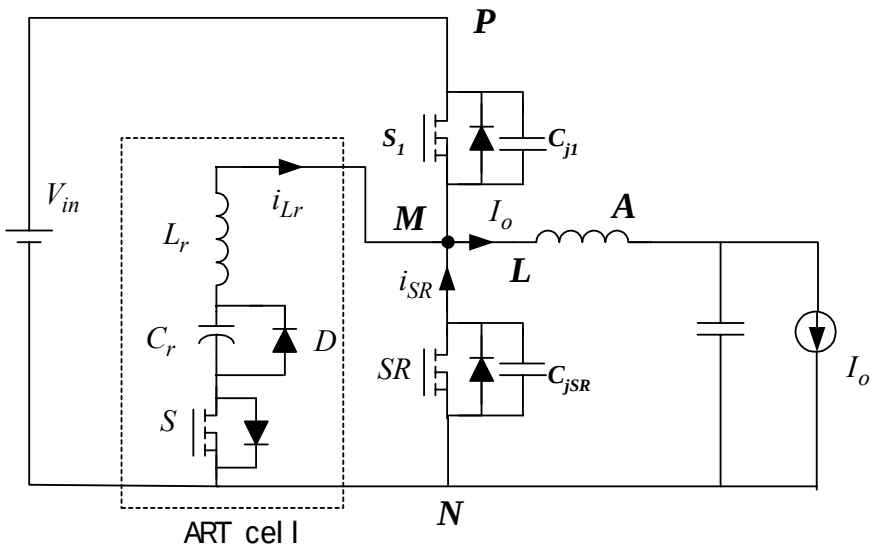


Fig. 2. 5: Buck converter with ART cell

Mode 1 (t_0<t< t_1): The resonant capacitor Cr was pre-charged with $v_{Cr}(t_0) = 2Vin$, and the filter inductor L freewheels through the SR. This mode starts with turn-on of the switch S at t=t_0, where the inductor current $i_j(t_0) = 0$. Cr charges Lr at resonant manner; the associated voltage and current are given by:

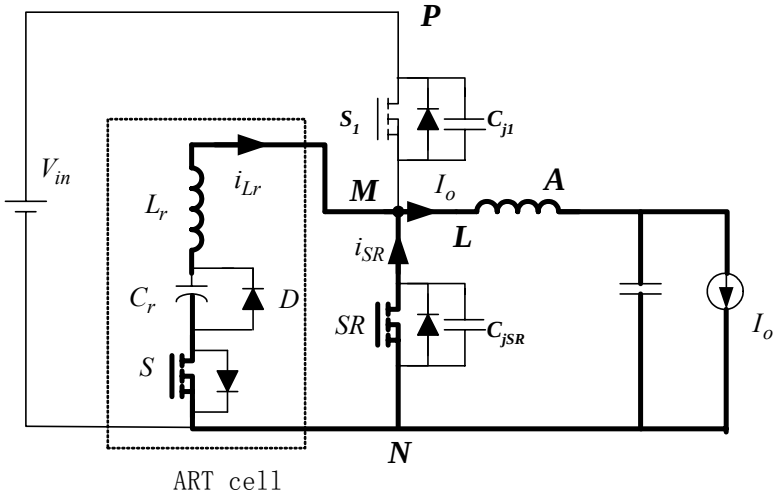
$$i_{Lr}(t) = \frac{2V_{in}}{L_r\omega_o}\sin(\omega_o t) \qquad \left(0 \le t \le \frac{\pi}{2\omega_o}\right) \qquad \text{Eq. 2. 6}$$

$$v_{Cr}(t) = 2V_{in}\cos(\omega_o t) \qquad \left(0 \le t \le \frac{\pi}{2\omega_o}\right) \qquad \textit{Eq. 2. 7}$$

Where $\omega_o = \frac{1}{\sqrt{L_r C_r}}$

The mode ends at $t = t_1 = \frac{\pi}{2\omega_o}$ with the capacitor voltage discharged to zero, and the resonant current reaching maximum value:

$$i_{Lr}(t_1) = \frac{2V_{in}}{\omega_o L_r} \qquad \textit{Eq. 2. 8}$$

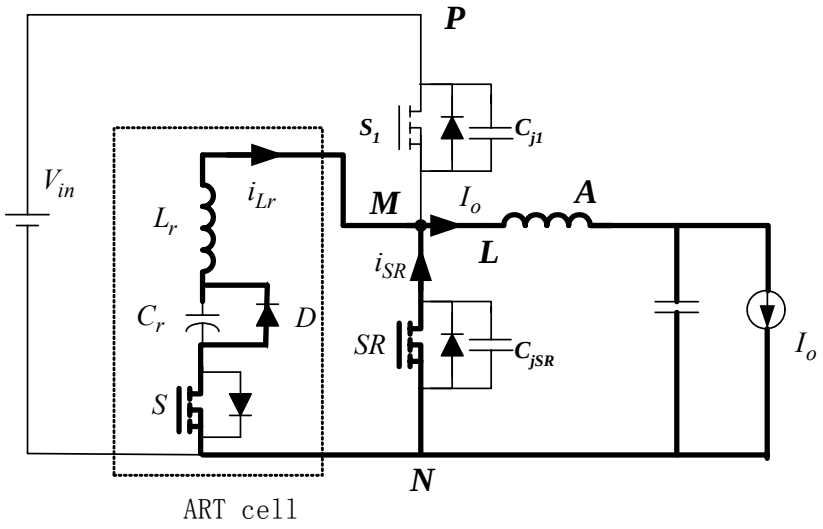


< Mode 1 >

Fig.2.6 a

Mode 2 (t₁<t< t₂): With the resonant capacitor Cr voltage reaching zero, the diode D in the cell carries current, and the inductor is trapped in the short-circuit loop. Assuming the inductor

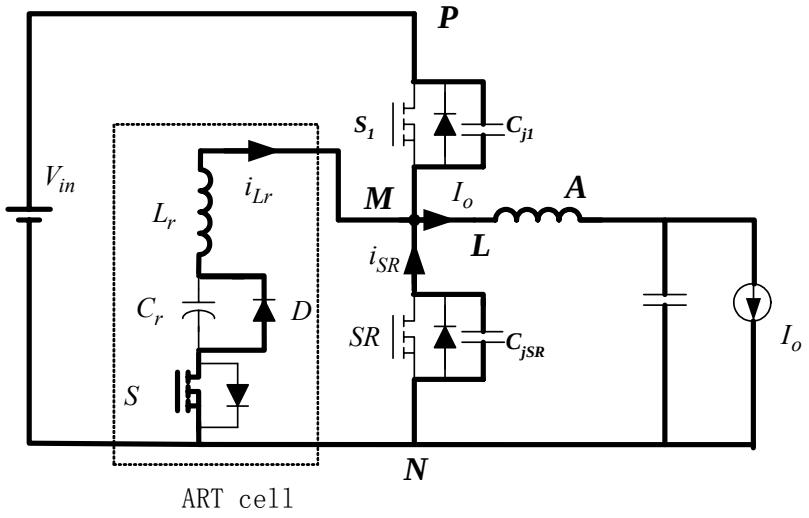
current value $i_{Lr}(t_1) > I_o$, the SR current is reversed with the value of $(i_{Lr}(t_1) - I_o)$. As a matter of fact, inductor L freewheels through the ART cell during this mode.



< Mode 2 >

Fig.2.6 b

Mode 3 (t2<t< t3): SR turns off at t = t2, and the inductor current previously flowing through the SR charges the junction capacitance C_{jSR} and discharges C_{j1} until the switch of the S1 body diode conducts in Mode 4.



< Mode 3 >

Fig.2.6 c

Mode 4 (t_3<t< t_4): When the junction capacitance voltage across the switch S_1 is discharged to zero t = t_3, body diode conducts to carry current. To ensure body-diode conduction, the following estimated condition should be satisfied:

$$\frac{1}{2}L_r\left(\frac{2V_{in}}{\omega_o L_r}-I_o(t_2)\right)^2 \geq \frac{1}{2}(C_{jSR}+C_{j1})V_{in}{}^2 \qquad \textit{Eq. 2. 9}$$

The inductor current at t_3 satisfy:

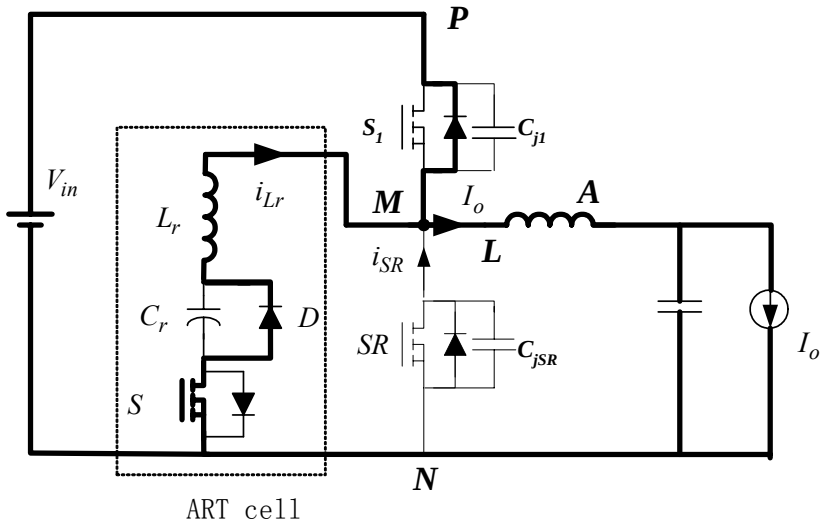
$$\frac{1}{2}L_r\left(\frac{2V_{in}}{\omega_o L_r}-i_{Lr}(t_3)\right)^2 = \frac{1}{2}(C_{jSR}+C_{j1})V_{in}{}^2 \qquad \textit{Eq. 2. 10}$$

Solving Equation (2.10) obtains the inductor current at t_3:

$$i_{Lr}(t_3) = \frac{2V_{in}}{\omega_o L_r} - V_{in}\sqrt{\frac{C_{jSR}+C_{j1}}{L_r}} \qquad \textit{Eq. 2. 11}$$

According to Equation (2.9), there is shown $i_{Lr}(t_3) \geq I_o$. During this mode, through the body diode of the switch S_1, the resonant inductor current i_{Lr} resets towards a steady-state value of I_o. The inductor current resets as the following slew rate:

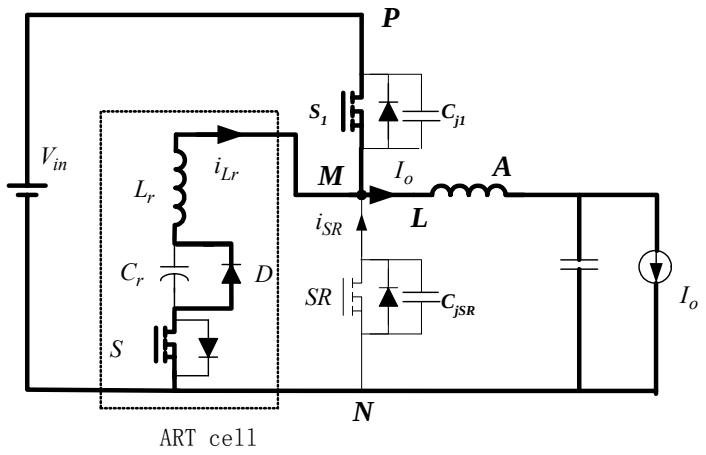
$$\frac{di_{Lr}(t)}{dt} = \frac{V_{in}}{L_r} \qquad (t_3 \leq t \leq t_4) \qquad \textit{Eq. 2. 12}$$



< Mode 4 >

Fig.2.6 d

Mode 5 (t_4<t< t_5): At t = t_4, the switch S_1 turns on at ZVS. The resonant inductor current continues to decrease with the slew rate in Equation (2.12). When the resonant inductor current decreases to output filter inductor current I_o, the current in the switch S_1 reverses the direction and becomes positive. After that, the S_1 current increases and the resonant inductor current decreases with the same slew rate as in Equation (2.12).



< Mode 5 >

Fig.2.6 e

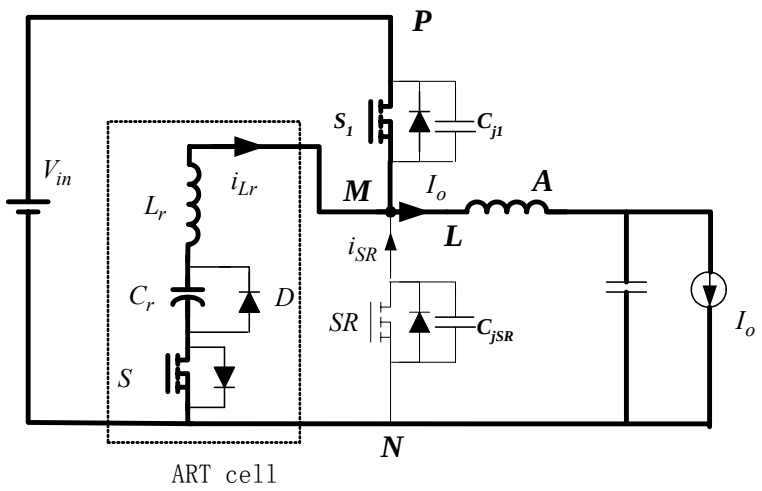
Mode 6 ***($t_5 < t < t_6$):*** When the switch S_1 current increases to the filter inductor current I_o, the resonant inductor current reverses the direction and becomes negative, then the diode D is blocked, and the resonant capacitor Cr is involved in a resonance. The ART tank is charged in a resonant manner, and the resonant inductor current is given by:

$$i_{Lr}(t) = \frac{-V_{in}}{L_r \omega_o} \sin \omega_o (t - t_5) \qquad (t_5 \le t \le t_5 + \frac{\pi}{\omega_o}) \qquad \textit{Eq. 2. 13}$$

The resonant capacitor voltage is given by:

$$v_{Cr}(t) = V_{in}(1 - \cos \omega_o (t - t_5)) \qquad (t_5 \le t \le t_5 + \frac{\pi}{\omega_o}) \qquad \textit{Eq. 2. 14}$$

where $\omega_o = \frac{1}{\sqrt{L_r C_r}}$.

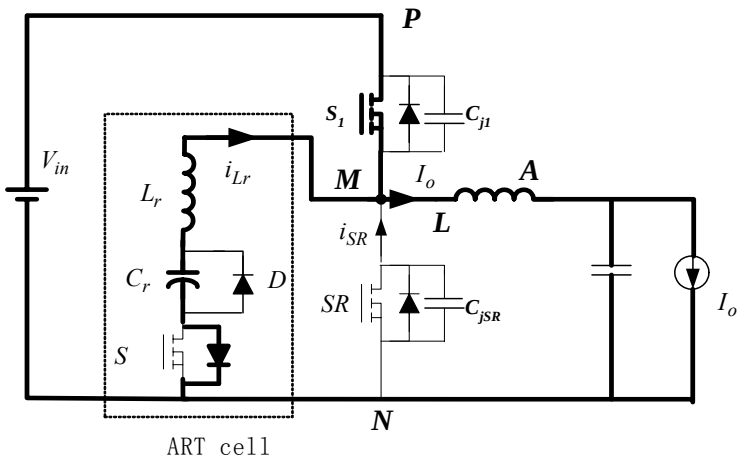


< Mode 6 >

Fig.2.6 f

Mode 7 ($t_6 < t < t_7$): The ART cell's switch S turns off at ZVS and the carried resonant current shifts to its body diode and the resonance continues as described in Equations (2.13) and (2.14) in Mode 6. The sinusoidal resonant current rises to the peak and then decreases towards zero. The resonance ceases with the capacitor voltage reaching the peak ($v_{Cr}(t_7) = 2V_{in}$) and the inductor current reaches zero ($i_r(t_7) = 0$). The total duration of time in Mode 6 and 7 is determined by the parameters of the ART.

$$\Delta T = t_7 - t_5 = \pi\sqrt{L_r C_r} \qquad \textit{Eq. 2. 15}$$

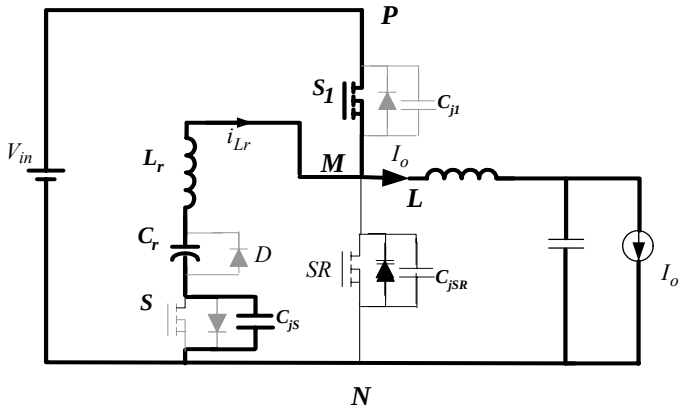


< Mode 7 >

Fig.2.6 g

Mode 8 ***($t_7 < t < t_8$):*** At t=t_7, the voltage across the resonant capacitor reaches $2V_{in}$, and the resonant inductor current becomes zero. After that, the circuit goes into damped ringing caused by the involvement of the switch S junction capacitor. When body diode of switch S was conducting in mode 7, the junction capacitor of switch S was not charged; at the beginning of mode 8, the body diode stops conducting and the junction capacitor of switch S is charged towards a steady-state voltage level Vin. This forms a resonant circuit composed of the input voltage Vin, resonant inductor Lr, resonant capacitor C_r and the junction capacitor of the switch S, all in series as shown in Fig. 2.6(h). Considering the capacitance value of the capacitor Cr is much greater than that of the junction capacitor C_{js}, the resonant inductor Lr and the junction capacitor C_{js} determine the resonant manner; the resonant frequency is estimated by:

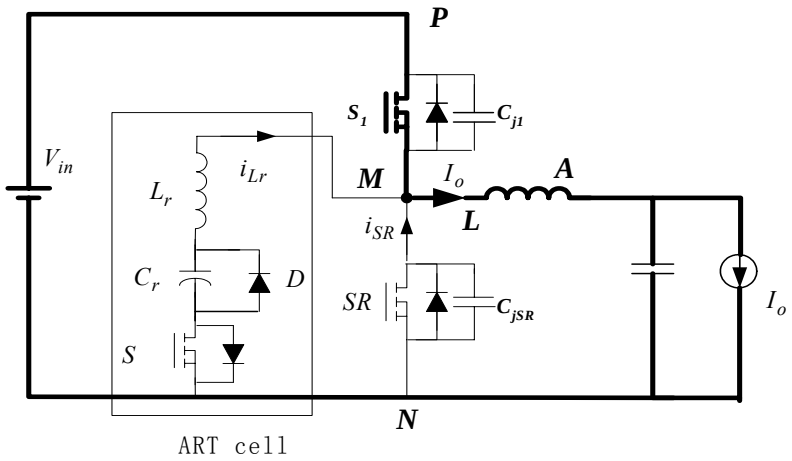
$$\omega_r = \frac{1}{\sqrt{L_r C_{js}}} \qquad \textit{Eq. 2. 16}$$



< Mode 8 >

Fig.2.6 h

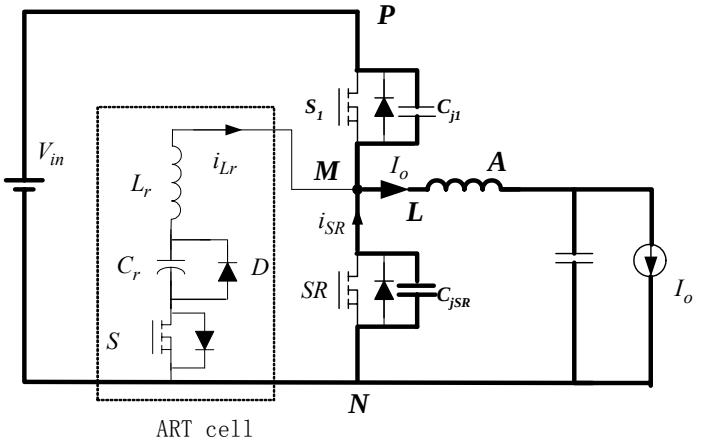
***Mode 9 (t_8< t < t_9)**:* The ringing is dampened by the equivalent resistance along the path of the resonant loop. At t = t_8, the ART cell is naturally inactive and separated from the converter. In this mode, the output filter is charged and the input power is delivered to the output.



< Mode 9 >

Fig.2.6 i

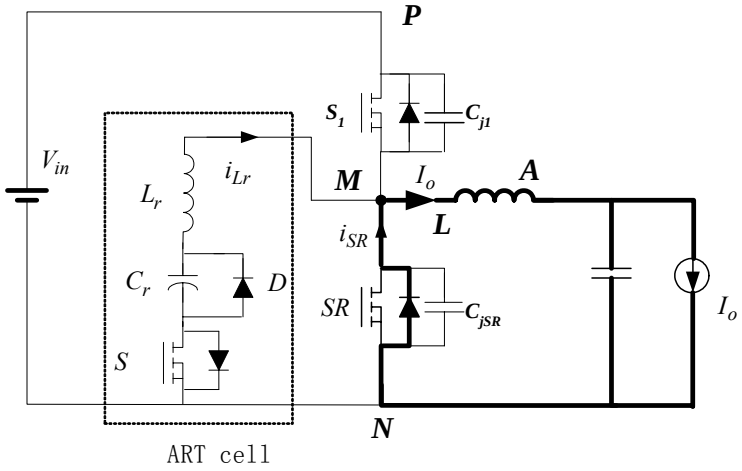
Mode 10 ($t_9 < t < t_{10}$): At t = t_9, the switch S_1 turns off, the filter inductor charges the junction capacitance C_{j1} and discharges $C_{jSR.}$



< Mode 10 >

Fig.2.6 j

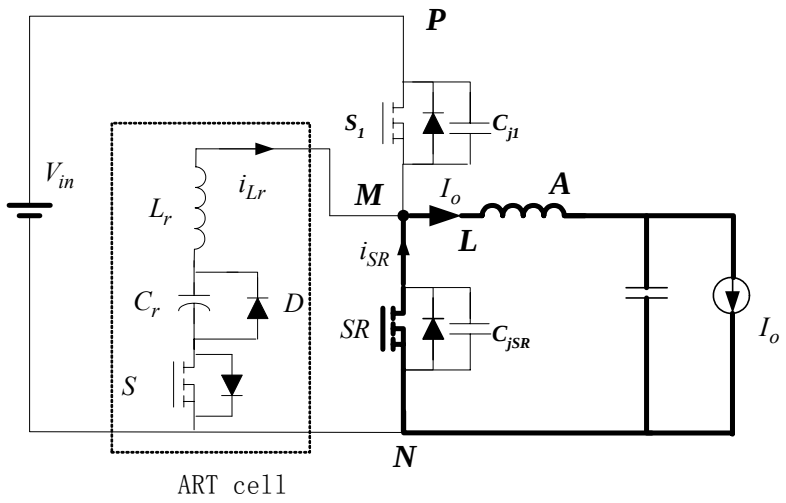
Mode 11 ($t_{10} < t < t_{11}$): When the junction capacitance voltage reaches zero, the SR body diode conducts carrying the output inductor current, which provides ZVS turn-on condition for the SR.



< Mode 11 >

Fig.2.6 k

Mode 12 ***($t_{11} < t < t_0+T$):*** During the body-diode conduction interval, the SR turns on at ZVS, and the converter enters into inductor freewheeling mode. With the turn-on of the switch S, the converter goes back to Mode 1.



< Mode 12 >

Fig.2.6 l

Fig. 2. 6: Equivalent circuits of modes of operation

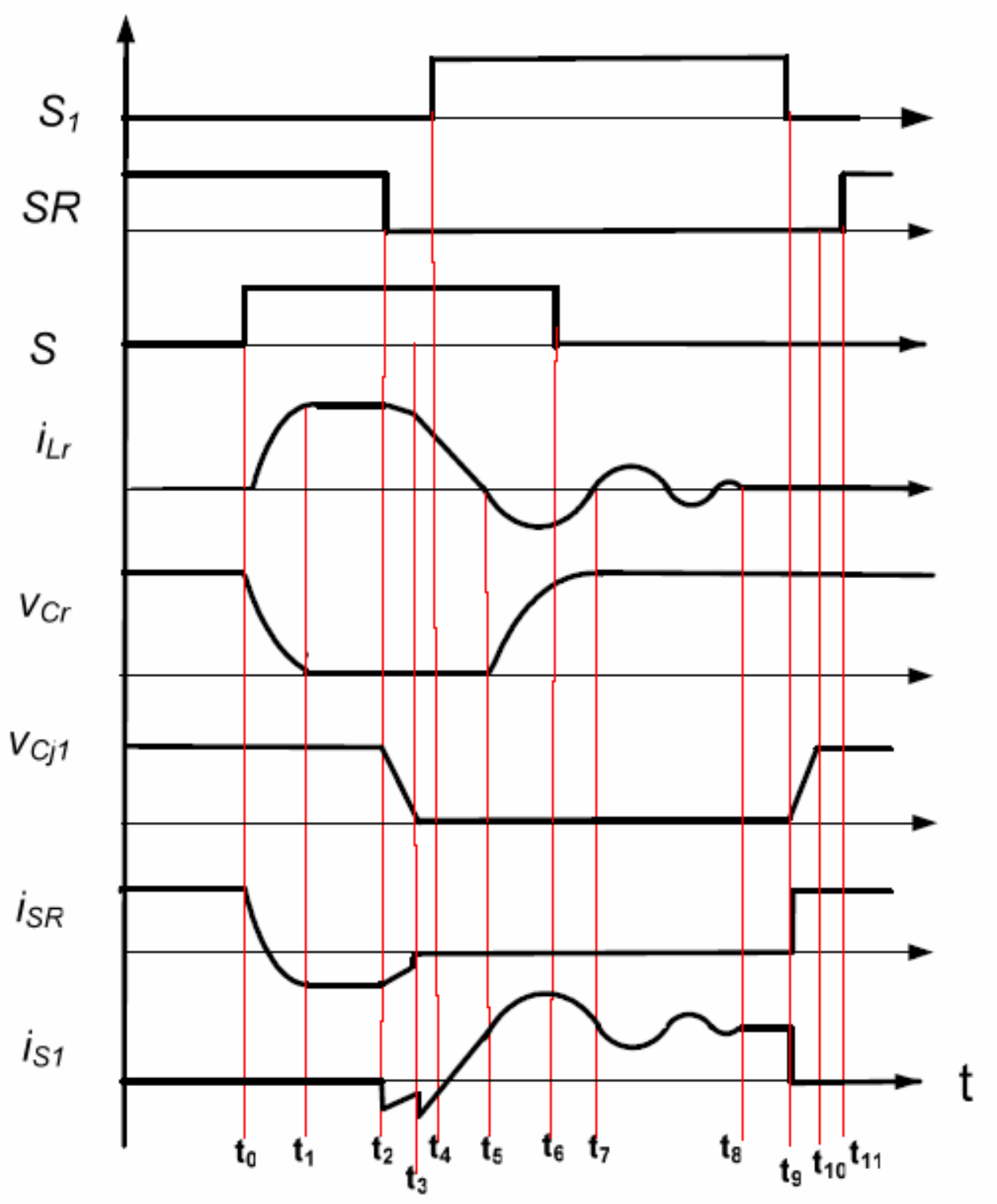


Fig. 2. 7: Key waveforms for Buck converter with ART cell

2.5 Features and design considerations

As discussed above, by adding an ART cell in parallel with synchronous rectifiers in non-isolated dc-dc converters, the SR's body diode conduction and the related reverse recovery are eliminated, and the ART cell energy is released for the active switch to turn on at ZVS. In addition, the ART cell's auxiliary switch S turns on at ZCS and turns off at ZVS; thus, the related switching loss is minimized. Since the ART cell is activated only during the switching transition, the conduction loss in the cell is limited.

The presented topology is advantageous especially for high voltage synchronous rectifiers. Generally, the synchronous rectification is limited to applications with low voltage ratings of MOSFETs (usually below 150V) because the SR's body-diode reverse recovery becomes more significant with the increase of MOSFET voltage ratings. In the meanwhile, with ever-decreasing on-resistance of MOSFETs, conduction loss can be dramatically reduced with synchronous rectifiers replacing Schottky or ultra-fast-recovery diodes in high-voltage rectification applications. The presented ART cell provides a solution to the problem and allows high-voltage MOSFETs to be used as SRs since reverse recovery and related loss are eliminated.

The resonant inductance L_r and capacitance C_r values determine the time constant of the ART resonant tank. To ensure the body diode is not conducting at its worst, that of full load and low-

line input, the ART cell must store and release sufficient energy. According to Equation (2.9), the resonant inductor peak current satisfies if

$$i_{Lr,pk} = i_{Lr}(t_2) > I_o(t_2) \qquad \textit{Eq. 2. 17}$$

The body diode conduction can be avoided when the SR turns off and the active switch S_1 could probably achieve ZVS. In an engineering design, output filter inductance is finite, and the output current ripple is necessary considered. At $t = t_2$, the output filter inductor current almost reaches the low peak, and the full load current is:

$$I_{o,\max} = I_o(t_2) + \frac{\Delta I_o}{2} \qquad \textit{Eq. 2. 18}$$

Where ΔI_o is the output inductor current ripple. Approximately, the ART cell is designed to make the resonant inductor peak current satisfy $i_{Lr,pk} = I_{o,\max}$, the condition of Equation (2.17) is satisfied, and thus body diode conduction is eliminated and Switch S1 has a good chance to achieve ZVS. The resonant inductor peak current can be obtained and designed as equal to full load current:

$$i_{Lr,pk} = 2V_{in,\min}\sqrt{\frac{C_r}{L_r}} = I_{o,\max} \qquad \textit{Eq. 2. 19}$$

Where $V_{in,\min}$ is the low-line input voltage. As described in Mode 7, during the time while the ART cell is being recharged, the auxiliary switch S turns off at ZVS. To secure the auxiliary switch S has sufficient time to turn off with ZVS during the cell-recharging period, the ART cell's recharging period of time has to be sufficiently long. Meanwhile, the recharging time should be limited to reduce conduction loss of the cell. According to Equation (2.15), the ART

recharging time is determined by the cell's parameters. We assume the required time for recharging is T_d , the cell parameters satisfy:

$$\pi\sqrt{L_r C_r} = T_d \qquad \textit{Eq. 2. 20}$$

By solving Equation (2.18) and (2.19), the ART cell parameters are designed as follows:

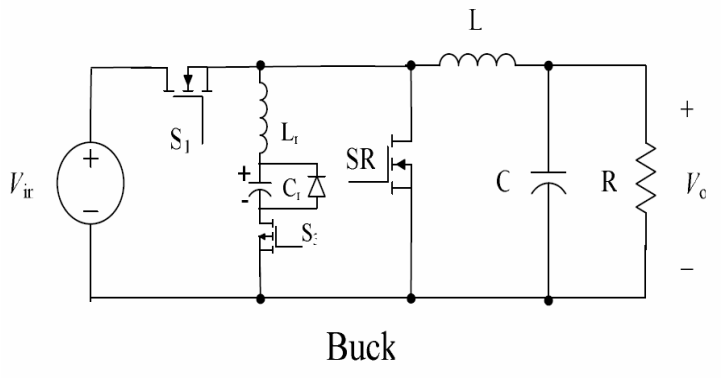
$$L_r = \frac{2V_{in,\min} T_d}{\pi I_{o,\max}} \qquad \textit{Eq. 2. 21}$$

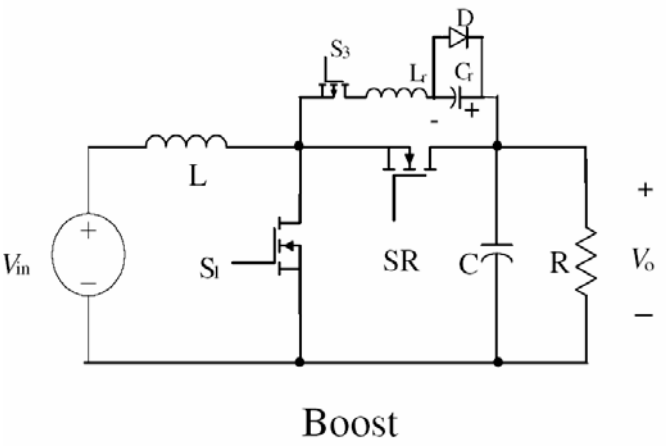
$$C_r = \frac{T_d I_{o,\max}}{2\pi V_{in,\min}} \qquad \textit{Eq. 2. 22}$$

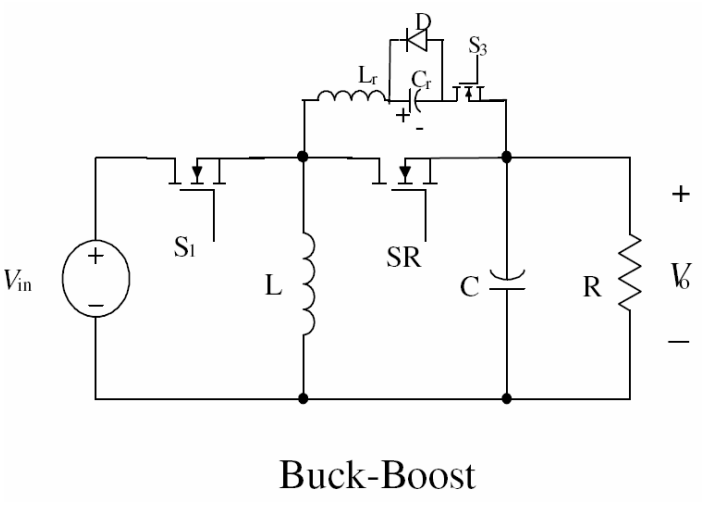
If Lr was selected to be 1.5uH, then Td can be calculated from Equation (2.21) to be 147ns and then Cr can be calculated from Equation (2.22) to be 1.46nF. In the experiment, Cr was increased to be 2nF so that the resonant current peak is increased to assure achieving ZVS for switch S1, $i_{Lr,pk}$ was calculated as in Equation (2.19) to become 3.5A, which agrees with experimental waveform shown in Fig. 2.9(b). Increasing Cr to 2nF also increases Td which can be calculated as in Eq, and (2.20) to become 172ns, which agrees with experimental waveform shown in Fig. 2.9(b), increasing the Td duration assures turning off switch S at zero voltage and ease the tuning of the experiment.

2.6 Topology derivation

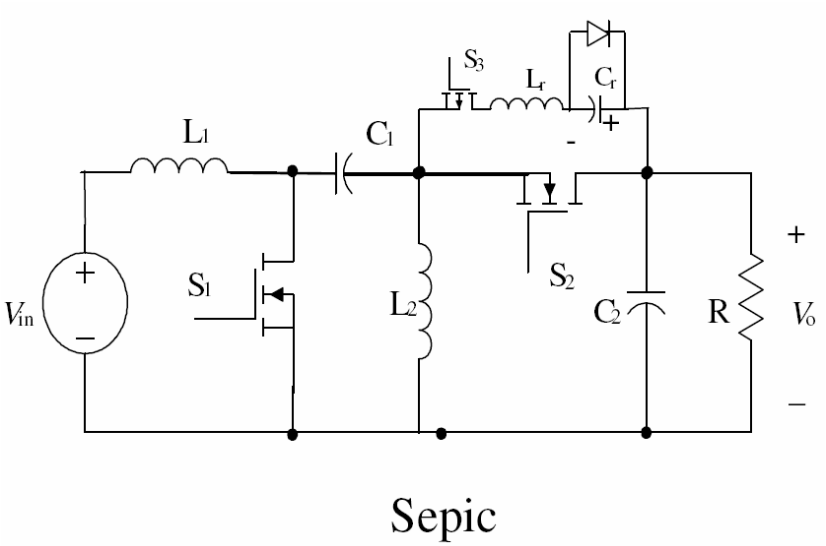
ART concept can be generally applied to non-isolated dc-dc converters where synchronous rectifiers are utilized by connecting the ART cell with SRs in parallel. Figure 2.8 shows the six basic non-isolated dc-dc converters with synchronous rectifiers connected in parallel with the ART cell. The ART cells' principle of operation is similar to the one in the buck converter. Understanding this concept, ART cell can even be expanded to isolated dc-dc topologies such as forward, flyback, half-bridge, full-bridge and push-pull.







Buck-Boost



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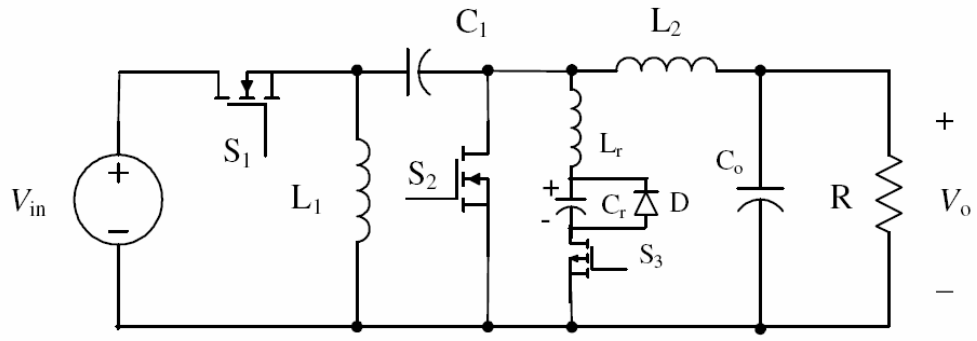


Zeta

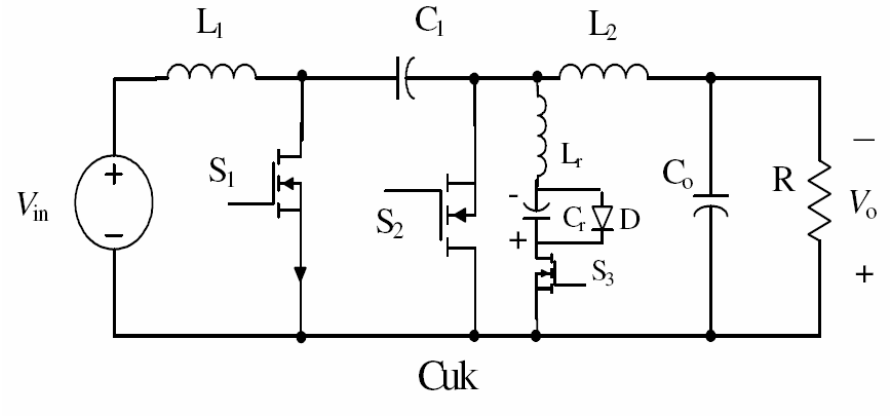


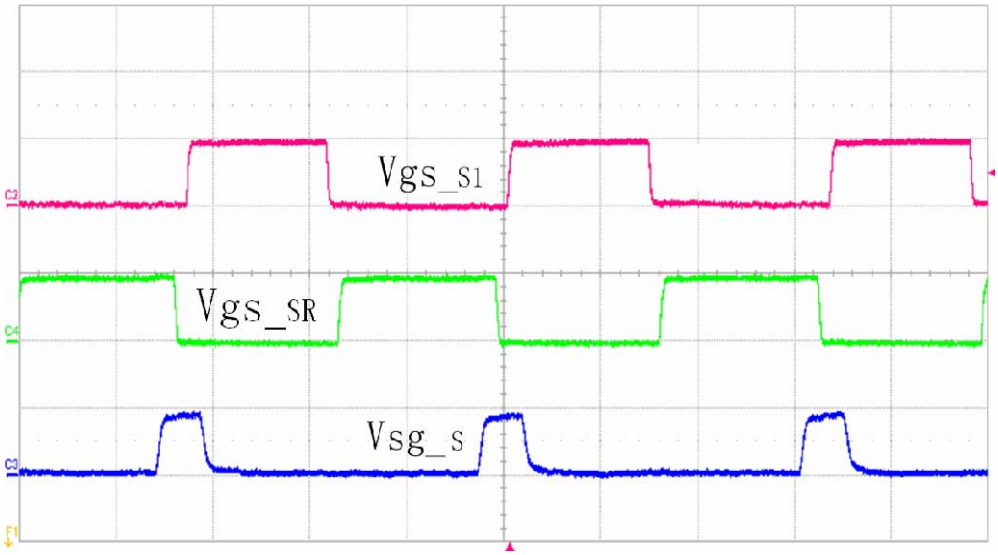
Fig. 2. 8: ART concept applied to main non-isolated dc-dc converter topologies

2.7 Experimental results

A prototype is built to verify the presented topology with the specification of Vin= 48V, Vout= 32V, Iout = 0 ~ 3A, switching frequency: 300kHz. N-channel MOSFET Si7454DP is selected as S1 and SR switches, and P-channel MOSFET Si7439DP is selected as the auxiliary switch S. Output filter inductance is L= 88uH, the ART cell's resonant inductance Lr= 1.5uH, and resonant capacitance Cr= 2nF. According to the design Equation (2.19), the resonant peak current is about 3.5A, which means the converter can operate under ZVS condition with output current up to 3.5A. Substituting the resonant parameters into Equation (2.20), the resonant recharging time is 172nS, which provides switch S enough time to turn off while having limited conduction loss in the ART cell.

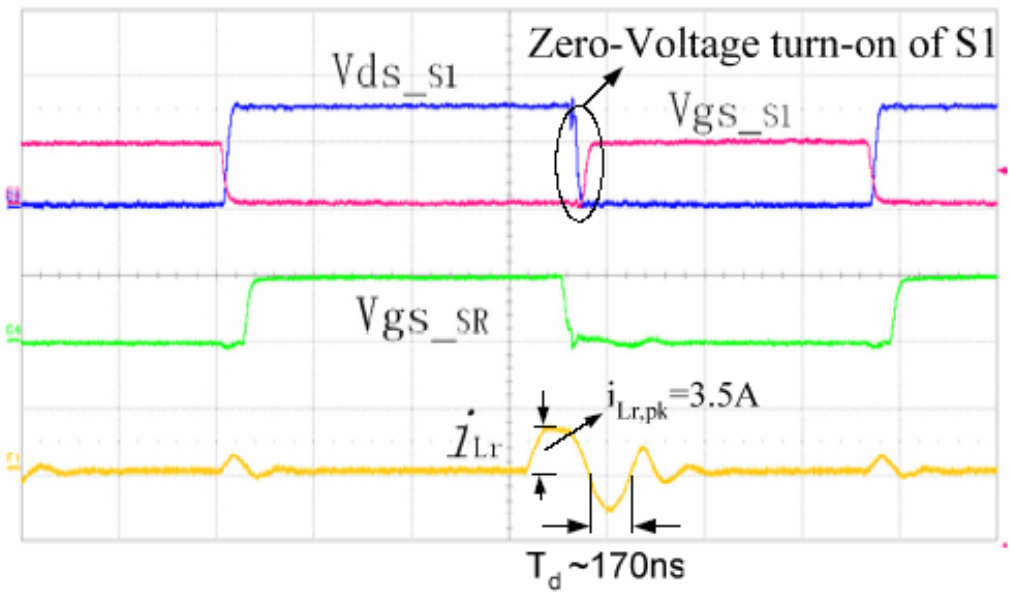
Figure 2.9 shows experimental waveforms. From Figure 2.9(a), it can be shown that the auxiliary switch S is activated during the switching transition of Switch S1 and SR. From Figure 2.9(b), it

is clear that ZVS is achieved for Switch S1 when SR is turned off. In Figure 2.9(c), it is shown that SR turns off when SR current goes negative; therefore, the SR body diode is not involved and the reverse recovery problem is solved. Figure 2.9(d) shows soft-switching waveforms of Switch S. When S is turned on, the current slowly rises due to the resonant inductor, so the turn-on loss is limited. When Switch S turns off, the body diode conducts and the switch has no turn-off loss. Figure 2.9(e) shows waveforms of the resonant capacitor Cr, and it is observed that the capacitor voltage is discharged to zero and recharged during the transition. All waveforms agree with the analyses in Section III. Because of the advantage of the presented ART cell, the converter operates at 300kHZ with fairly good efficiency (driving loss is included). For comparison purposes, convectional buck converter is tested by removing the ART cell and the efficiencies are shown in Fig. 2.10. Compared with conventional buck converter, the ART converter efficiency is improved up to 2%.



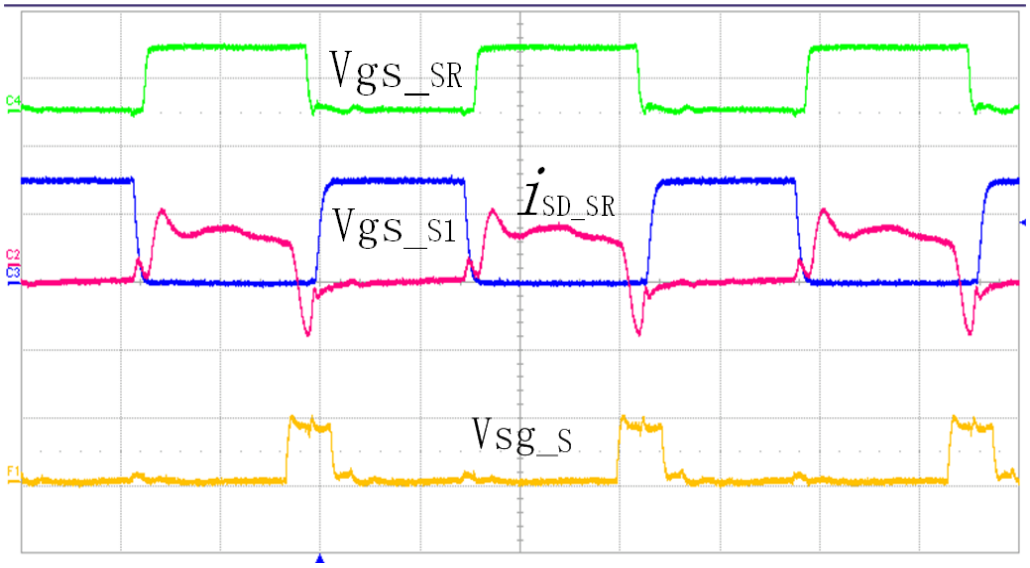
(a). Gate voltage waveforms

(Voltages: 10V/div; Time: 1uS/div)



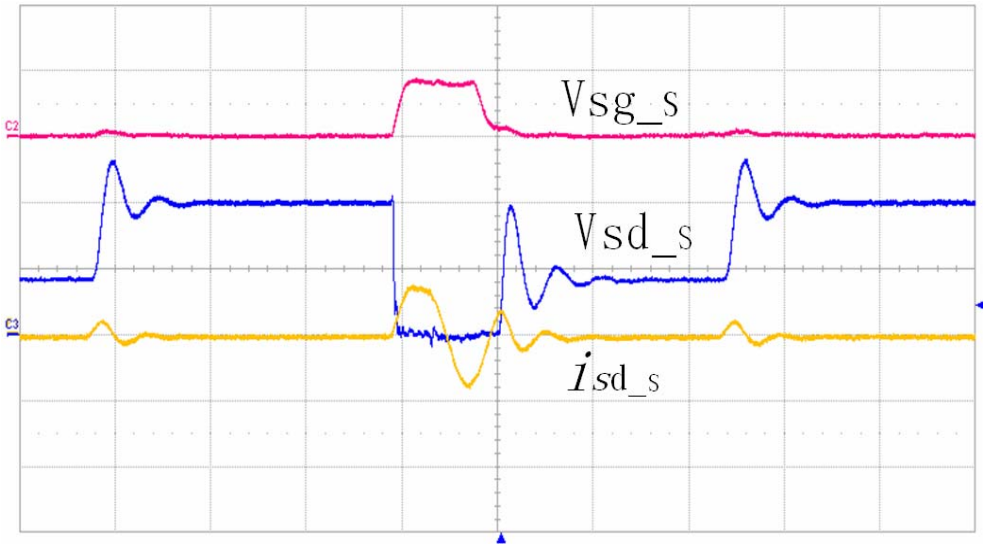
(b). ZVS waveforms of the switch S1

(Voltages: 10V/div; Current i_{Lr}: 5A/div; Time: 500nS/div)



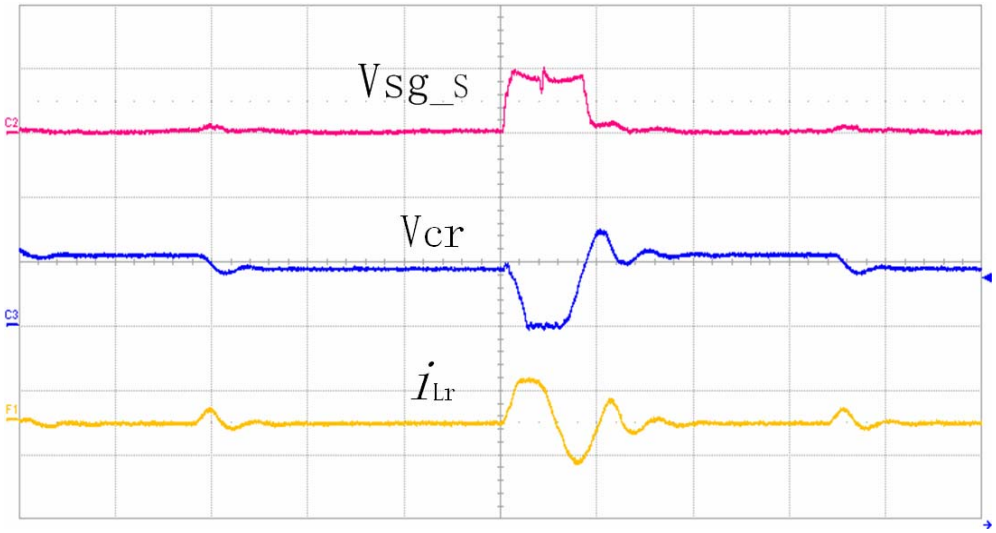
(c). Current and voltage waveforms of the SR

(Voltages: 10V/div; Current i_{Lr}: 5A/div; Time: 1uS/div)



(d). Soft-switching waveforms of the auxiliary switch S

(Vsg: 10V/div; Vsd: 50V/div; isd: 5A/div; Time: 500nS/div)



(e). Waveforms of the capacitor Cs

(Vsg: 10V/div; Vcr: 100V/div; i_{Lr}: 5A/div; Time: 500nS/div)

Fig. 2. 9: Experimental waveforms

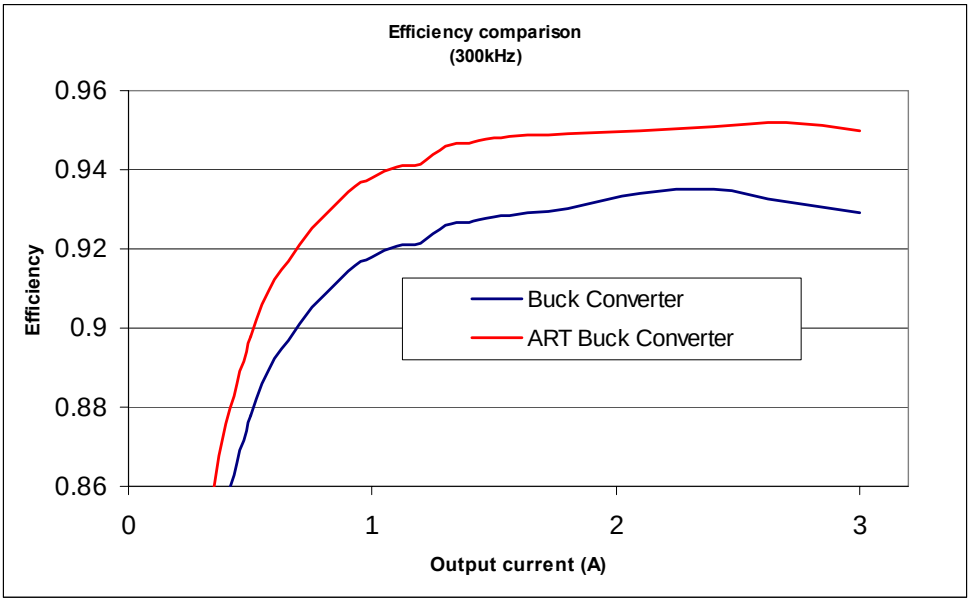


Fig. 2. 10: Efficiency comparison

2.8 Conclusion

The concept of Active Resonant Tank (ART) and a general method for applying the ART cell to non-isolated topologies was introduced. A high-frequency high-efficiency ART buck converter was introduced as an example, in which an active resonant tank is connected in parallel with SR to achieve Zero-Voltage-Switching (ZVS) for the active switch and to eliminate SR-related body-diode conduction and reverse recovery problems.

The ART can be applied to Intermediate Bus Converters (IBC) or to front stages of Point of Load converters (POL). Such applications convert power with high input voltages, and their physical size is limited; this requires high switching frequency. In such conditions, the ART cell improves the SRs' performance and improves the conversion efficiency due to the reduced switching loss and reverse-recovery loss and noise compared to conventional hard-switching buck converter. Moreover, the ART conduction losses are limited since it is activated for a short period during switching time, and the auxiliary switch of the ART cell turns on at ZCS and turns of at ZVS; therefore, the switching losses associated with the auxiliary switch are negligible.

However, the ART cell has some drawbacks, such as: the resonant components must be designed carefully, taking into consideration full load current and maximum line voltage conditions in order to be able to achieve soft switching for all conditions, which make it more difficult to optimize, and adds some complexity compared to the simple conventional buck. Additionally, it requires an additional switch and other components.

CHAPTER 3: LCC ZVS BUCK CONVERTER WITH SYNCHRONOUS RECTIFIER

3.1 General concept

The concept of the LCC Buck converter introduces an inductive load in the bridge leg and changes the switching commutation mechanism of the low-side SR switch. In other words, in the conventional buck converter with SR, the SR operates at capacitive load. When the SR turns off, the current flows through the body diode; as a result, the body diode's reverse recovery occurs with the turn-on of the high-side switch. While in the LCC buck converter, the SR turns off at inductive load, and the inductive current will not flow through the SR's body diode. Moreover, the inductive current is utilized to discharge the junction capacitance and achieve ZVS for the high-side switch. Therefore, compared with the conventional SR buck converter, reverse-recovery-related switching and ringing loss is eliminated; compared with QSW buck converter, the output current ripple is significantly reduced and the output capacitance is dramatically reduced. A prototype is built to compare the conventional Buck converter, QSW converter, and the LCC ZVS buck converter. The experimental test shows that the presented converter is advantageous over the conventional buck converter at high switching frequency, where the switching loss dominates the total power loss. The experimental test results also show that the presented converter is advantageous over QSW converter in current and output voltage ripples and efficiency in wide ranges of switching frequency; it also has half the input current di/dt of the QSW converter.

3.2 Converter description and modes of operation

The presented LCC buck converter is shown in Fig. 3.1 and the corresponding waveforms are shown in Fig. 3.2, where S_2 functions as the synchronous rectifier and S_1 and S_2 are complementarily driven. L_2, C_1, and C_2 are the additional cells to the conventional Buck converter. Capacitance of C_1 and C_2 is sufficiently large so that the inductor L_2 current is regarded as triangle waveform.

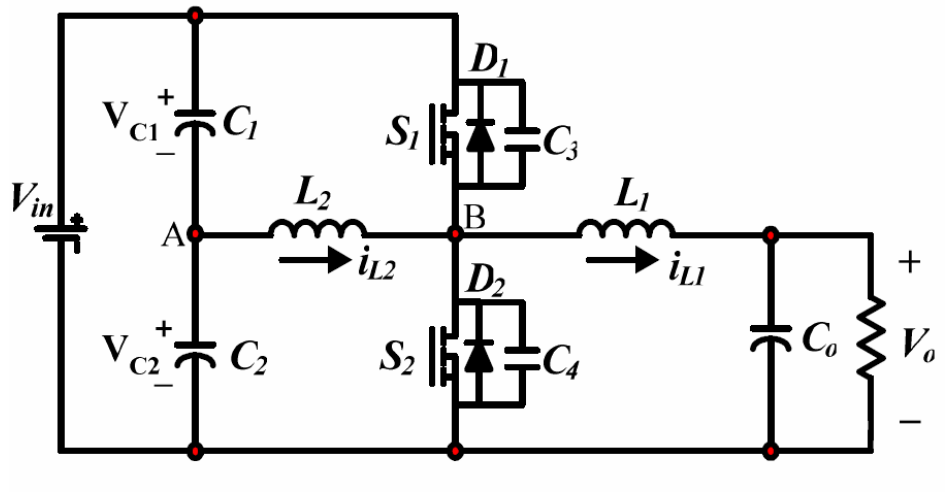


Fig 3. 1: LCC ZVS buck converter

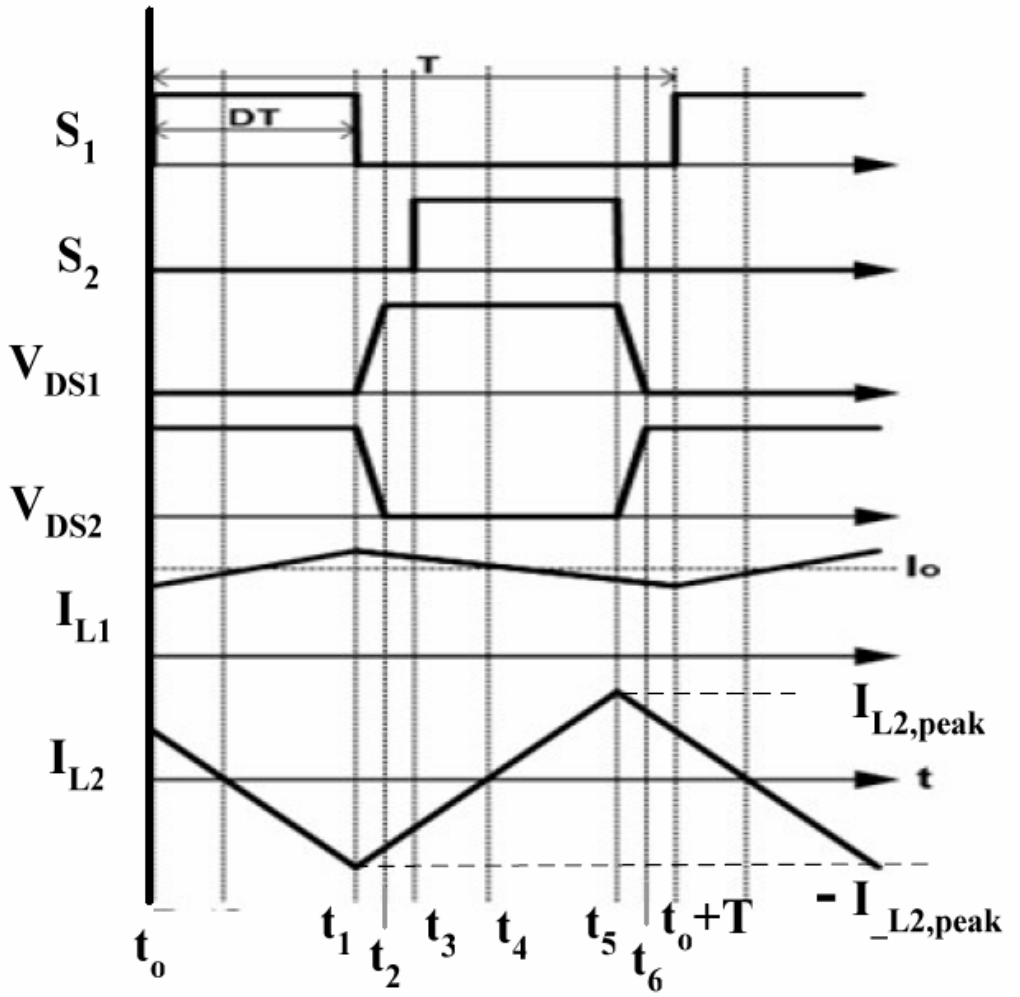


Fig 3. 2: Key waveforms

All components are regarded ideal except otherwise indicated. Capacitors C_1 and C_2 are large enough so that their voltages are considered to be constant. The modes of operation are shown in Fig. 3.3 and described as follows:

Mode 1 (t_0<t< t_1)

During the mode, the switch S_1 is on, the inductor L_1 charges according to Eq. 3.1, and input power is being delivered to the output. Capacitor C_1 voltage discharges inductor L_2 as shown in Eq. 3.2.

$$i_{L1}(t) = \frac{V_{in} - V_o}{L_1}(t - t_o) + I_{L1}(t_o) \qquad \textit{Eq. 3. 1}$$

$$i_{L2}(t) = \frac{-V_{C1}}{L_2}(t - t_o) + I_{L2}(t_o) \qquad \textit{Eq. 3. 2}$$

Mode 2 (t_1 < t < t_2)

At t=t_1, the switch S_1 turns off, and both inductors L_1 and L_2 discharge the junction capacitance C_4 and charge the junction capacitance C_3.

Mode 3 (t_2 < t < t_3)

At t=t_2, the junction capacitance voltage across C_4 discharges to zero, and the body diode D_2 starts carrying current.

Mode 4 (t_3 < t < t_5)

At t=t_3, the switch S_2 turns on at zero-voltage switching (ZVS). L_1 discharges as shown in Eq. 3.3, and capacitor C_2 voltage charges inductor L_2 as shown in Eq. 3.4. At t = t_4, the inductor L_2 reverses current direction and keeps charging. When the current in inductor L_2 is higher than in the inductor L_1, the drain-to-source current through the switch S_2 gets reversed (becomes positive) and continues increasing.

$$i_{L1}(t) = \frac{-V_o}{L_1}(t - t_1) + I_{L1}(t_1) \qquad \textit{Eq. 3. 3}$$

$$i_{L2}(t) = \frac{V_{C2}}{L_2}(t - t_1) + I_{L2}(t_1) \qquad \textit{Eq. 3. 4}$$

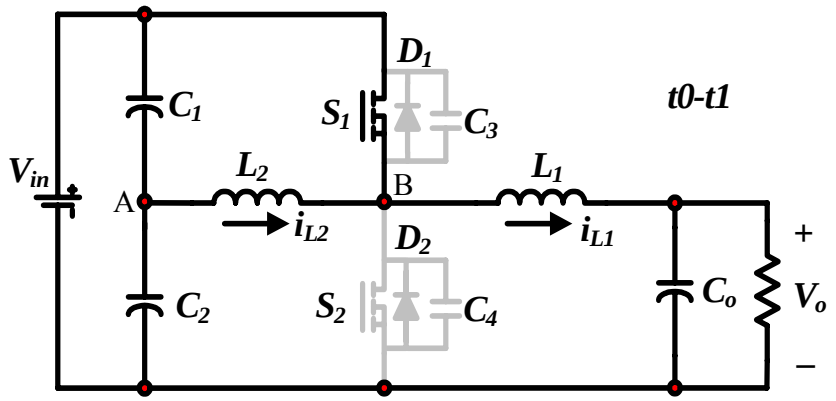
Mode 5 ($t_5 < t < t_6$)

At $t=t_5$, the switch S_2 turns off. Because the current in the inductor L_2 is higher than in the inductor L_1, no current will be flowing through the body diode of switch S_2, the current difference will charge the junction capacitance C_4 and discharge C_3.

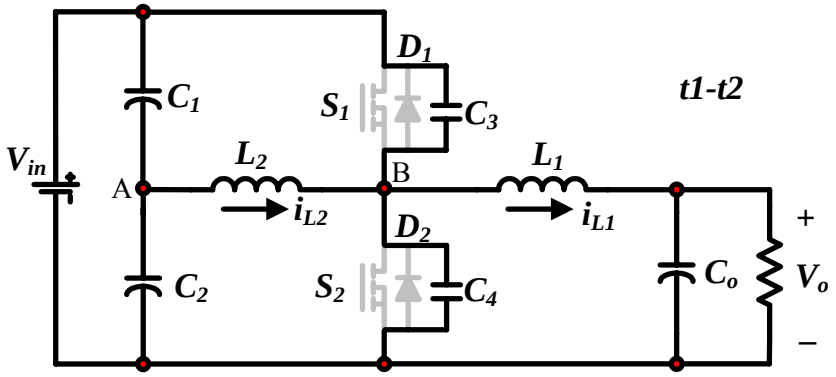
Mode 6 ($t_6 < t < t_o+T$)

At $t=t_6$, the junction capacitance voltage across C_3 discharges to zero, and the body diode D_1 of the switch S_1 starts carrying current.

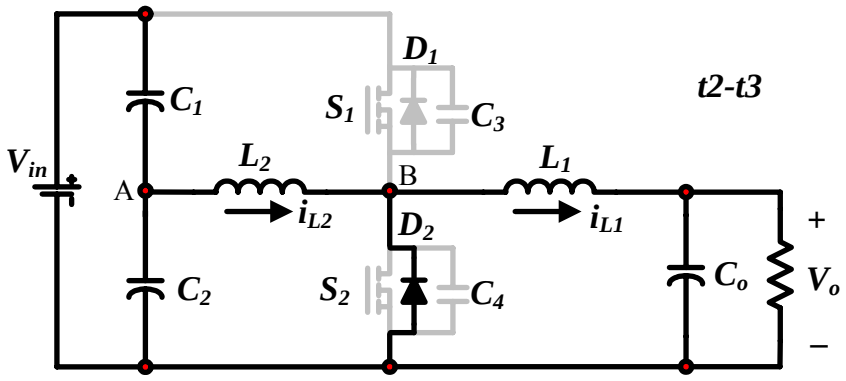
At $t= t_o+T$, a new switching cycle begins when S_1 turns on at zero-voltage switching (ZVS) and with no reverse recovery.



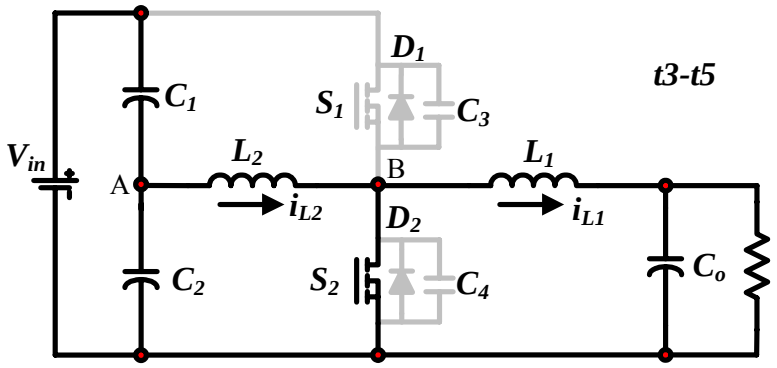
Mode 1



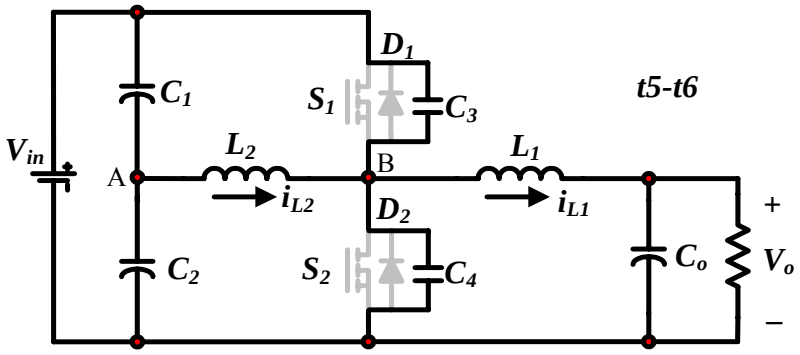
Mode 2



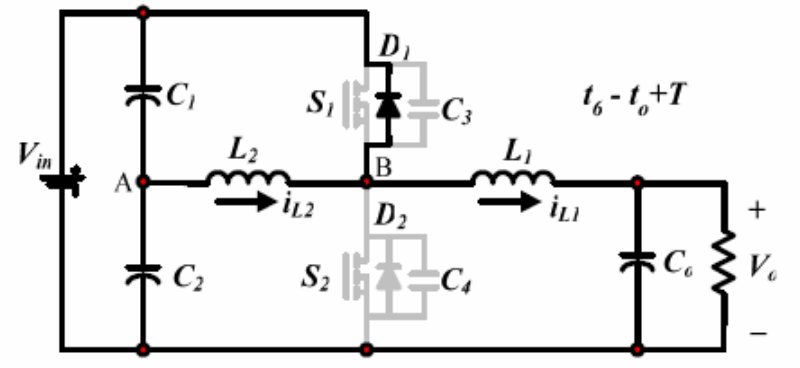
Mode 3



Mode 4



Mode 5



Mode 6

Fig 3. 3: Modes of operation

From the analyses above, it is clear that the body diode of the SR does not conduct when the SR turns off, and both the switches S_1 and S_2 can achieve ZVS. This is favorable for high switching frequency applications, where switching loss (including reverse-recovery loss) dominates. Compared with the conventional buck converter, the penalty of the presented converter is the increased conduction loss in the switches and auxiliary circuits. Fortunately, the extra conduction loss will not increase with the switching frequency. Therefore, when the switching frequency reaches a certain range, the saved switching and reverse-recovery loss increases and becomes compatible with the extra conduction loss, and then the presented topology starts being favorable over the conventional Buck converter. It should be noted that the higher the voltage rating of SR MOSFET, the worse the recovery characteristic of its body diode. This means that conventional buck will suffer more switching losses in high voltage applications.

3.3 Losses and ripple analyses

In this section, losses and voltage and current ripples will be analyzed with the purpose of comparing the LCC buck converter with the conventional and QSW buck converters.

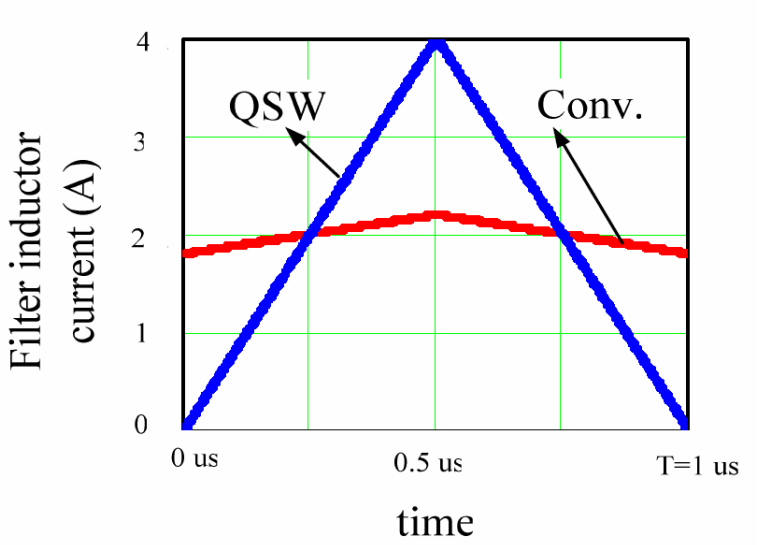
In conventional buck the inductor current ripple is much lower than that of QSW buck, which has the advantage of lower output voltage ripple so that less output capacitance is required; also, lower input current ripple means lower current di/dt drawn from the input source. In addition, the AC current rms (that is due to the current ripple) is less which makes it more efficient than QSW,

especially at light and mid load ranges. This clearly states that QSW buck has higher conduction losses than conventional buck. On the other hand, when high switching frequency is required, the conventional buck will suffer high switching losses and reverse recovery noise. The QSW buck high current ripple can guarantee reversing current direction in the filter inductor before switching transition to eliminate reverse recovery losses and noise, and achieve ZVS for the high side switch. At high switching frequencies, the saved switching losses in QSW will overcome the added conduction losses, meaning higher efficiency. But the QSW buck's high current ripple causes high output voltage ripple, so more output capacitance is required. Pertaining to the LCC buck, it saves the same switching losses the QSW buck does, and it has the same output voltage ripple as in the conventional buck. The proposed converter holds a current ripple that is required for achieving soft switching, just as in QSW buck, but it is contained in the LCC cell, meaning that the high current ripple does not reach the output side, and the filter inductor value is designed as in the conventional buck. Another benefit is that the high capacitor C_1 in the LCC cell offers a contribution in reducing the input current di/dt to half compared to QSW buck.

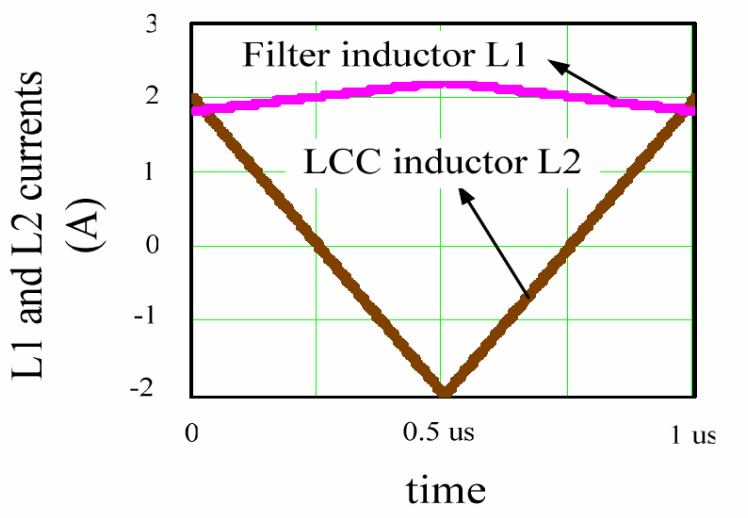
Current through switches in the LCC buck is similar to the QSW buck, but input and output currents are different, and their rms is lower which saves some conduction losses in the capacitors ESR. It should be noted that LCC cell components do not require large values, so their added conduction losses are accepted and affordable judged against their benefits.

Following are several plots of current waveforms along with rms currents for the three converters to support above discussions. Analyses were based on an example of the same specifications as

in experimental section, V_{in}=48V, V_{out}=24V, I_{out}=2A, f=1MHz, C_1=C_2=2uF, L_2=3uH. Filter inductor (L1) is 27uH for the conventional buck and 3uH for the QSW buck. Figure 3.4(a) is a plot of inductor current versus time for conventional and QSW buck, the difference in current ripples is obvious for the two cases; Fig. 3.4(b) shows the current versus time for the LCC buck converter in the filter inductor L_1 and the LCC cell inductor L_2; it is clear that filter inductor ripple is similar to that in the conventional buck, and the current ripple in inductor L_2 has a zero average, unlike the QSW buck.



(a)

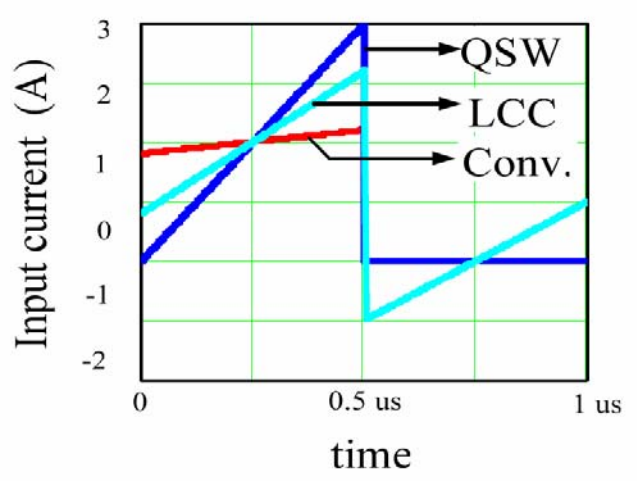


(b)

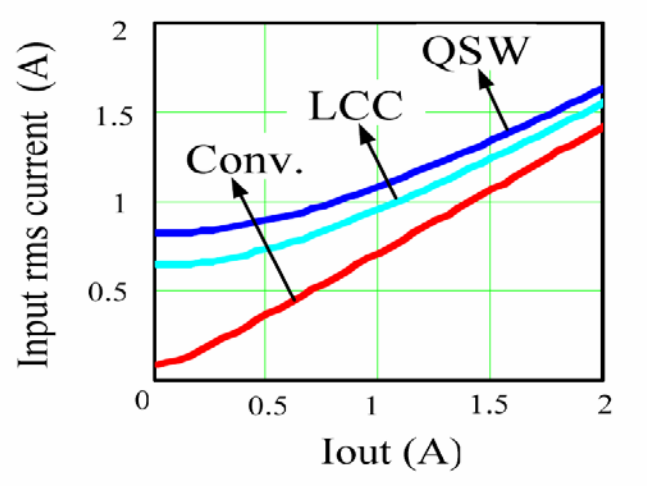
Fig 3. 4: (a) current waveforms for QSW and conventional buck converters.

(b) current waveforms for LCC buck.

As mentioned above, input currents for the three converters are different, and input current rms is different, too. Fig. 3.5(a) shows input current versus time waveforms for the three converters, it is clear that the LCC buck converter's input current di/dt is half compared to QSW buck, fig. 3.5(b) is a plot of input rms current versus output current for the three converters; it shows that the LCC buck converter has lower input rms current than QSW buck.



(a)



(b)

Fig 3. 5: (a) Input current waveforms for the three converters. (b) Input rms current vs. output current for the three converters.

3.4 Design considerations

In order for the LCC buck converter to achieve soft switching, peak current in inductor L_2 must reach full load current. L_2 peak current is dependent on the input voltage, so L_2 inductance must be designed with consideration of input voltage variation. If a close look is given to the LCC cell with both switches S_1 and S_2, it can be seen that they form a buck-boost converter with C_1 being input capacitor, C_2 being output capacitor, L_2 filter inductor, S_1 is the main switch and S_2 is the synchronous rectifier. Notice that $V_{c1} + V_{c2} = V_{in}$, a simplified circuit is shown in Fig. 3.6.

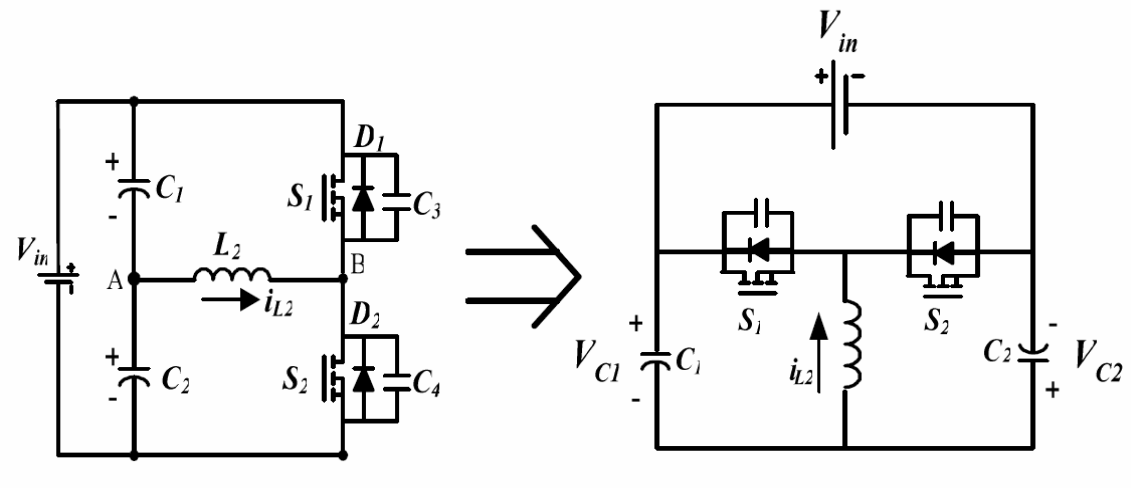


Fig 3. 6: Simplified circuit of LCC cell forming a buck-boost converter

Voltages across capacitors C_1 and C_2 are expresses in Eqs. 3.5 and 3.6, respectively.

$$V_{C1} = (1 - D)V_{in} \qquad \textit{Eq. 3. 5}$$

$$V_{C2} = DV_{in} \qquad \textit{Eq. 3. 6}$$

The peak current in inductor L2 is expressed in Eq. 3.7.

$$I_{L2\ peak} = \frac{V_o}{2\ L_2}\ (1-\frac{V_o}{V_{in}})\ T \qquad \textit{Eq. 3. 7}$$

Fig. 3.7 shows a plot of inductor L_2 peak current versus input voltage. It is clear that peak current is directly related to the input voltage. For applications where input voltage is varied, designing inductor L_2 value must take into consideration the case of minimum input voltage and full load current, so that L_2 inductor current reaches the filter inductor current value, and be able to reverse the SR current direction in order to prevent body diode conduction and reverse recovery, and discharge the junction capacitance of the high switch and achieve ZVS.

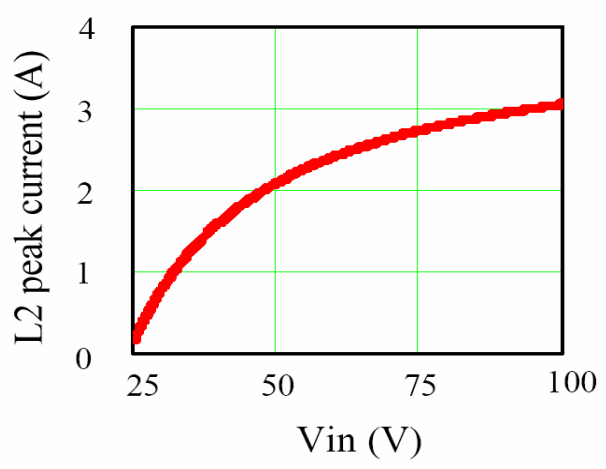


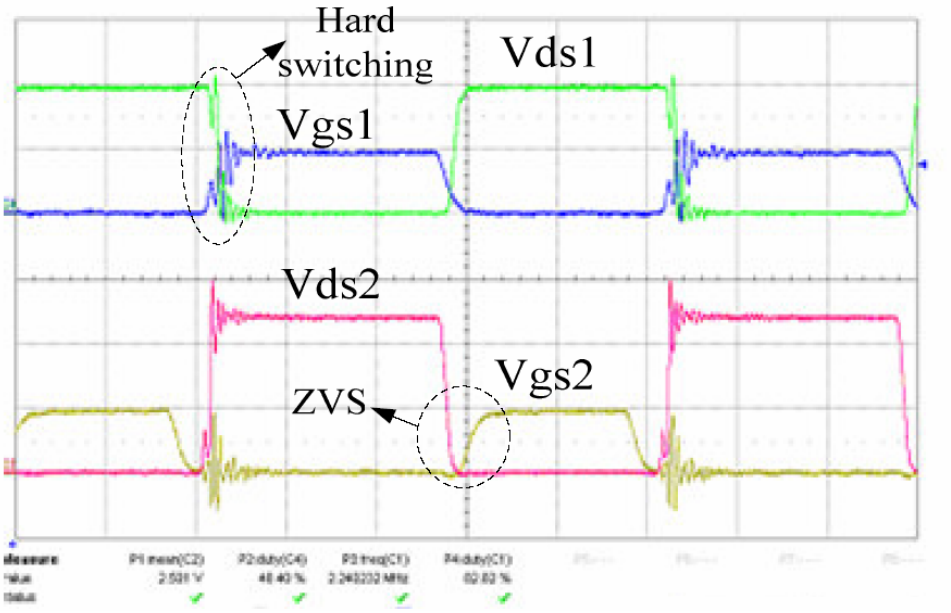
Fig 3. 7: Inductor L2 peak current vs. Input voltage

3.5 Experimental results

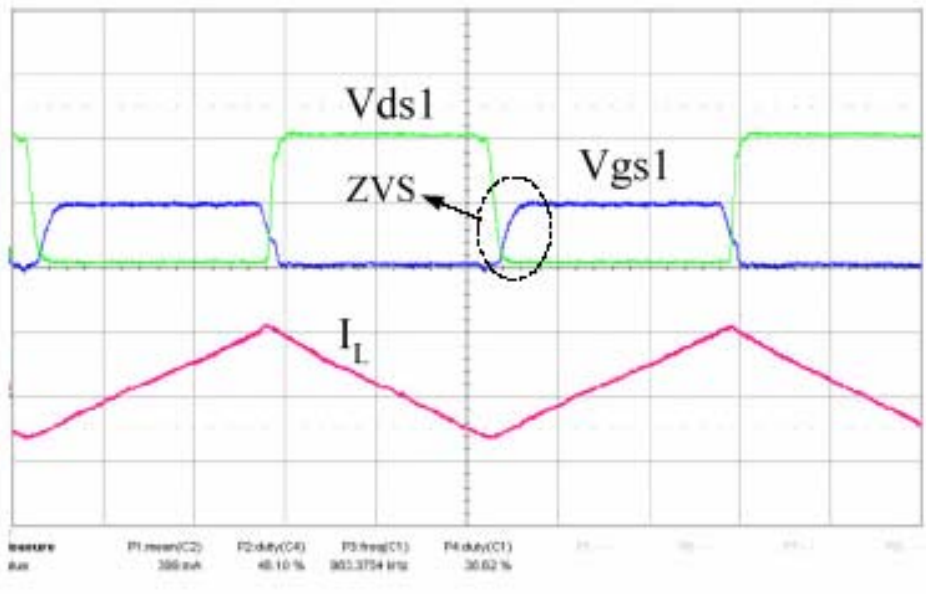
To evaluate the LCC buck converter, a prototype is built with the following specification: V_{in}=48V, V_{out}=24V, I_{out}=2A, f=1MHz. With this input voltage, there are two options for the selection of the freewheeling rectifier: Schottky diode or the synchronous rectifier. For example, with the Schottkey diode MBR10100 (100V@10A), the forward voltage drop is 0.8V, and the conduction loss is 0.8*2*0.5=1W; if a SR Si7456 (Rdson=25m Ohm) is used, the conduction loss is less than 0.1W. For this application, without considering the body-diode conduction and reverse recovery loss, SR is advantageous over Schottky diode. Unfortunately, the reverse recovery for 100V MOSFETs becomes a problem when operating at high switching frequency. The presented topology provides a solution to this application by eliminating reverse-recovery loss and thus allows the converter to operate at an extremely high switching frequency.

Selecting MOSFETs Si7456 as the high-side and low-side switches, three cases are tested on the built prototype: Conventional buck with SR, QSW buck converter and the LCC ZVS buck converter. Fig. 3.8(a) shows the waveforms of the two switches in the conventional Buck converter; it is observed that the reverse-recovery related ringing is very severe and high-side switch S1 operates at hard switching. In order to test the QSW buck converter, the filter inductance value has been reduced from 27uH to 3uH, the high-side switch achieves ZVS as shown in Fig. 3.8(b), and the ringing has been eliminated, but output voltage ripple was almost 9 times greater compared to the conventional. Based on the conventional buck converter, LCC cell (C_1=C_2=2uF, L_2=3uH) is applied and experimental waveforms are shown in Fig. 3.9. It is clearly

observed that both the high-side and low-side switches achieve ZVS and switching waveforms are very clean.

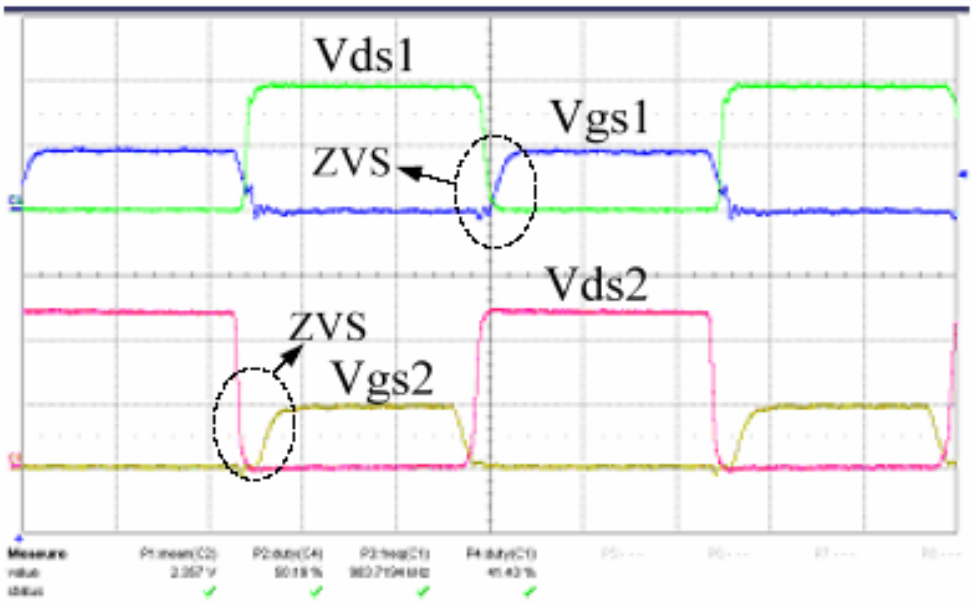


(a) Conventional buck converter

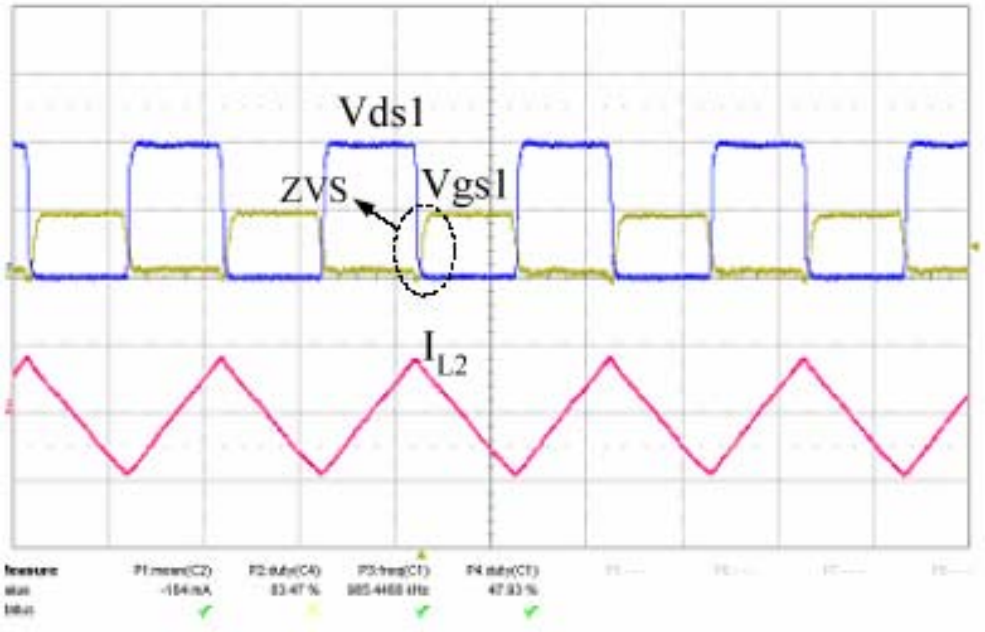


(b) QSW buck converter

Fig 3. 8: Waveform of the conventional buck converter and QSW buck converter at 1 MHz



(a)



(b)

Fig 3. 9: Waveforms of the presented LCC ZVS buck converter at 1MHz.

To demonstrate that the LCC buck converter is beneficial at high switching frequency, the conversion efficiency at 1MHz is measured and compared as shown in Fig. 3.10. It is clear that the improvement in efficiency is up virtually 3 percent compared to the conventional Buck converter, and is up 1.8 percent compared with QSW case.

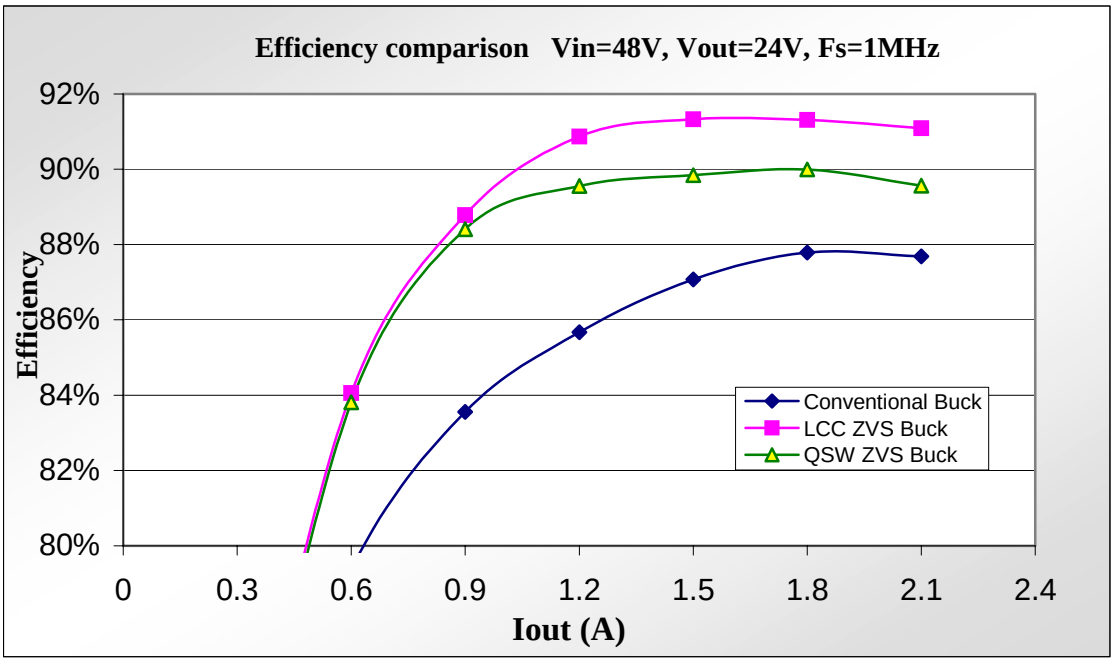


Fig 3. 10: Efficiency comparison at 1MHz

3.6 Conclusion

LCC ZVS Buck converter was presented to achieve Zero-Voltage-Switching (ZVS) and eliminate body-diode conduction and hard-switching reverse recovery in the conventional Buck converter with Synchronous Rectifiers (SRs). The LCC converter is advantageous over the QSW converter since it is capable of saving the same switching losses without increasing the output current ripple; resultantly, less output capacitance is required. Also, it has half the input current ripple of the QSW converter. Experimental results show that the LCC converter is a competitive topology for the SR applications with high voltage and high switching frequency.

The LCC buck converter can be applied to Intermediate Bus Converters (IBC) or to front stages of Point of Load converters (POL). Such applications convert power with high input voltages, and their physical size is limited, which require high switching frequency. In such conditions, the LCC buck can improve the SRs' performance and improve the conversion efficiency due to the reduced switching loss and reverse-recovery loss and noise compared to conventional hard-switching buck converter. Moreover, its design is simple and requires no additional switches, unlike the ART cell discussed in the previous chapter.

Alternatively, it has some drawbacks, such as: the LCC network conducts current throughout the whole switching period; as a result, its conduction losses are not negligible as in the ART cell. Thus, it is favorable over the conventional buck only at high switching frequencies where the saved switching losses overcome the additional conduction losses. Moreover, the LCC inductor L2 must be designed taking into consideration full load current and minimum line voltage

conditions in order to be able to achieve soft switching for all conditions, which makes it more difficult to optimize. Furthermore, since L2 peak current is a function of the input voltage, the LCC buck is not a good candidate for applications with wide input voltage range.

CHAPTER 4: ON LOAD ADAPTIVE CONTROL OF VOLTAGE REGULATORS FOR POWER MANAGED LOADS: CONTROL SCHEMES TO IMPROVE CONVERTER EFFICIENCY AND PERFORMANCE

4.1 VR Power Losses Study

4.1.1 Quick overview on VR losses sources

The conduction loss is one type of VR power loss. It is the result of parasitic resistances of the components such as the switch R_{DS-ON}, the capacitors ESR, the Inductor DCR, and the sense and traces resistances. This loss is a function of the load current and the *rms* value of the VR currents (function of current ripple) which is controlled by several factors including the switching frequency, the inductor value, and the input-to-output voltage ratio. The hard-switching loss is another type of VR power loss as a result of the voltage-current overlap period during switching. It is a function of the switching frequency and the parasitic capacitance of a switch. The reverse recovery loss is another type of power loss. It is a function of the switching frequency and the switch reverse recovery charge in addition to the voltage applied across the switch. The gate drive loss in the VR is a function of the switching frequency, the gate drive voltage, and switch gate charge. Other losses in the VR include inductor/magnetic components core losses, leakage currents, and standby losses.

Theoretical analyses and plots that illustrate detailed VR power losses can be obtained using common power loss equations which can be found, and they are available in the literature such

as those presented in [18]. Tables 4.1 and 4.2 show most of these equations. These equations were programmed into MathCAD® files to obtain the plots presented.

Table 4. 1: Conduction Losses for Buck VR

	CCM	DCM
High Side Switch (PMOS): P_{q1}	$\frac{(I_p^2 + I_p I_v + I_v^2)\cdot D \cdot R_{on}}{3}$	$\frac{I_p^2 \cdot D1 \cdot R_{on}}{3}$
Low Side Switch (NMOS): P_{q2}	$\frac{(I_p^2 + I_p I_v + I_v^2)\cdot (1-D) \cdot R_{on}}{3}$	$\frac{I_p^2 \cdot D2 \cdot R_{on}}{3}$
Winding Resistance: P_{wr}	$\frac{(I_p^2 + I_p I_v + I_v^2)\cdot R_l}{3}$	$\frac{I_p^2 \cdot (D1+D2) \cdot R_l}{3}$
Capacitor esr: P_{esr}	$\frac{1}{3}\left(\frac{Ip - Iv}{2}\right)^2 \cdot R_c$	$\frac{Vin \cdot Rc \cdot D1}{Vo \cdot Ip}\cdot[\frac{Io^3+(Ip-Io)^3}{3} + Ip \cdot Io \cdot (\frac{Ip}{2} - Io)]$
Sensing Resistor: P_{sen}	$\frac{(I_p^2 + I_p I_v + I_v^2)\cdot (1-D) \cdot R_s}{3}$	$\frac{I_p^2 \cdot D2 \cdot R_s}{3}$

Where: Ron is the on resistance of MOSFET, Rl is the winding resistance, Rc is capacitor esr, Rs is the sensing resistance

Table 4. 2: Switching Losses, Gate Drive Losses and Core Losses for Buck VR

	CCM	DCM
Capacitive Turn On: $P_{turn-on}$	$\frac{2}{3}(C_{oss\_p} + C_{oss\_n})\cdot V_{in}^2 \cdot f_s$	$\frac{2}{3}[C_{oss\_p} \cdot (V_{in} - V_o)^2 + C_{oss\_n} \cdot V_{in}^2] \cdot f_s$
Turn off Overlapping: P_{over}	$\frac{1}{4} V_{in} \cdot (I_p \cdot t_{f\_p} + I_v \cdot t_{f\_n}) \cdot f_s$	$\frac{1}{4} V_{in} \cdot I_p \cdot t_{f\_p} \cdot f_s$
Gate Drive Loss: P_{gate}	$C_{iss\_p} + C_{iss\_n}) \cdot V_{gs}^2 \cdot f_s$	$(C_{iss\_p} + C_{iss\_n}) \cdot V_{gs}^2 \cdot f_s$
Core Loss: P_{core}	$k \cdot I_p{}^2 \cdot f_s$	$k \cdot I_p{}^2 \cdot f_s$

Where: C_{oss-p} is high side P-MOSFET C_{oss}, t_{f-p} is the turn off time of high side P-MOSFET.
C_{oss-n} is low side N-MOSFET C_{oss}, t_{f-n} is the turn off time of low side N-MOSFET.

4.1.2 Power loss effects as a function of the load

VR power loss effects become more significant as a load becomes lighter because they become a larger portion of the overall power drawn from a source and a larger portion of the output power, which greatly degrades the VR efficiency. One important reason for this is the loss due to the hard-switching and gate drive (function of the switching frequency) which do not scale much with the load. Fig. 4.1 shows an example of how driving and switching power loss of buck converter tend to have a higher portion of the input power as load becomes lighter when running at fixed switching frequency in CCM mode. These losses can be reduced by modulating frequency as a function of the load current [20]. Also, it can be noticed that at light load and even at no load condition, conduction losses have some percentage of the input power; this is due to the rms value caused by the current ripple, unlike in DCM operation, where the *rms* current decreases at lighter loads, and goes to zero at no load. This explains the benefit of Mode-Hopping (MH) [20] technique especially when using small inductor value—which is the desired case when considering size and dynamic behavior.

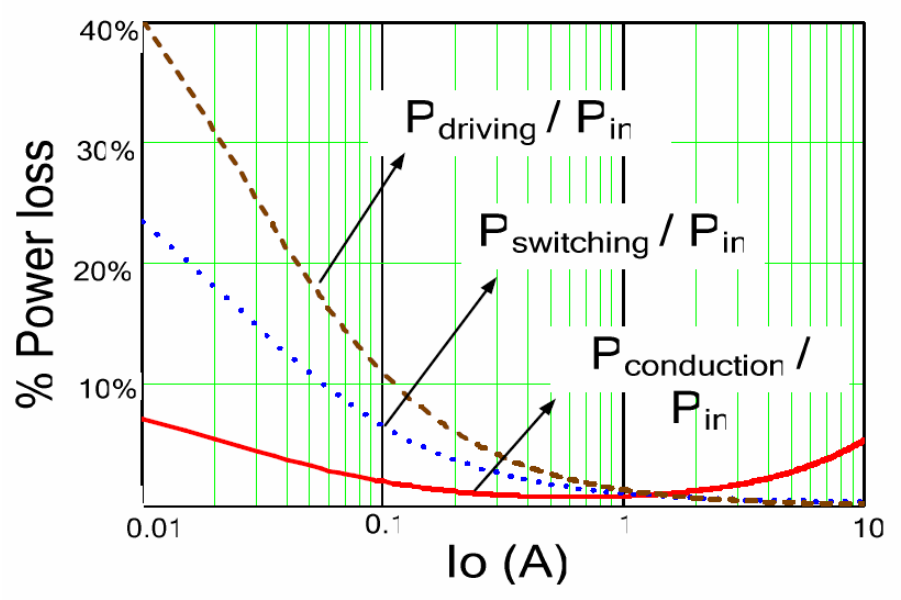


Fig.4. 1: *Power Losses normalized to input power*

4.2 Studies on light load efficiency improvement techniques

As mentioned earlier, Mode-Hopping (MH) and variable switching frequency are techniques used to improve light load efficiency [20]. In this section, the advantages and disadvantages of such techniques are briefly discussed, which then lead to presented control method.

The discussion will be based on the following buck VR design, for example, and not for limitation:

$V_{in} = 5V$, $V_o = 3.3V$, $L_o = 1\mu H$, $C_o = 50\mu F$ (only), and $f_{sw} = 500kHz$. In the analyses, the switch specifications for IRF7821 are used for the active FET and the synchronous FET. The

resistances DCR, R_{sense} and ESR are taken to be equal to $4m\Omega$, $10m\Omega$ and $1m\Omega$, respectively. It must be noted that the observations made next are not necessarily limited to this example case.

4.2.1 Mode-Hopping effect

Operating in DCM mode once the inductor current reaches zero will result in some efficiency improvement mainly because of: 1) Lower conduction losses, especially when operating deeply in DCM (very light load) since negative current represents circulating energy that is not delivered to the load. Therefore, ripple current and *rms* currents are reduced 2) Zero current turn-on of the active switch occurs because the switching cycle starts with a zero current in the output inductor, and 3) Reverse recovery loss is eliminated in DCM since the synchronous FET's body diode will not carry any load current at the end of the switching cycle which will prevent current commutation between the body diode and the active switch. No reverse recovery implies less switching noise in the converter. Fig. 4.2 shows the VR power loss percentages while operating at fixed frequency PWM with MH; upon comparison with the losses shown in Fig. 4.1, it shows how conduction losses go to zero as load current goes to zero.

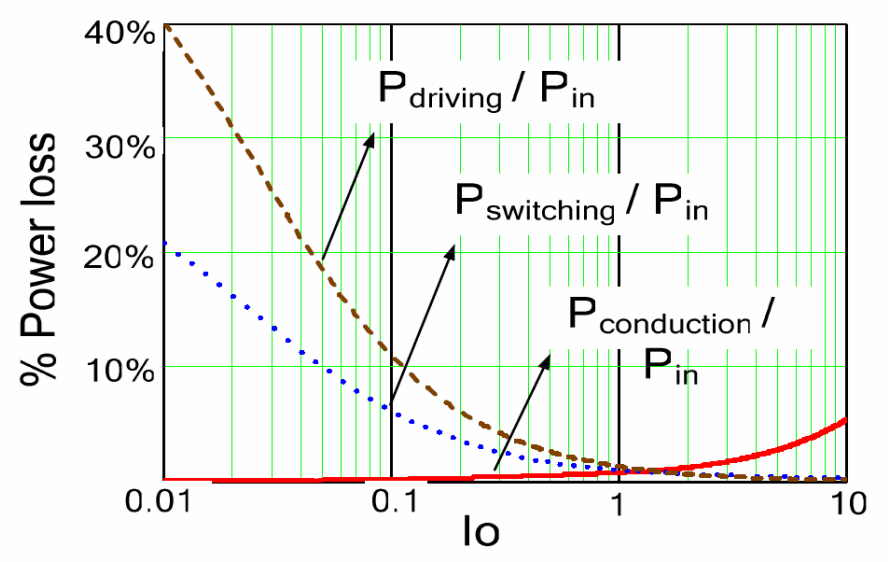


Fig.4. 2: *Power Losses normalized to input power at fixed switching frequency with MH technique*

4.2.2 Linear variable frequency effect

Decreasing the switching frequency will significantly improve efficiency at lighter loads, since hard switching losses and driving losses are reduced with frequency reduction [30, 31]. It is known that the compensation error signal, Verr (or duty cycle), decreases in DCM as load current becomes lighter. Figure 4.3(a) shows linear frequency modulation based on the compensator error signal.

Linear frequency modulation can be expressed as in Eq. 4.1:

$$f_{DCM,Linear}(Io) = f_{CCM} \cdot \frac{I_o}{I_{o.crit}} \qquad \textit{Eq. 4. 1}$$

Where ,

$f_{DCM,Linear}(I_o)$: is the DCM switching frequency in linear frequency modulation, and it is a function of I_o .

f_{CCM} : is the CCM switching frequency.

$I_{o.crit}$: is the critical or boundary current between CCM and DCM, and it is expressed as:

$$I_{o.crit} = \frac{V_o\,(V_{in} - V_o)}{2\,L_o V_{in}\,f_{CCM}} \qquad \textit{Eq. 4. 2}$$

Duty cycle in DCM in linear frequency modulation is a function of I_o , and is given by,

$$D_{DCM,\,Linear}(I_o) = \sqrt{\frac{2 \cdot I_o \cdot V_o \cdot L_o \cdot f_{DCM,\,Linear}(I_o)}{V_{in} \cdot (V_{in} - V_o)}} \qquad \textit{Eq. 4. 3}$$

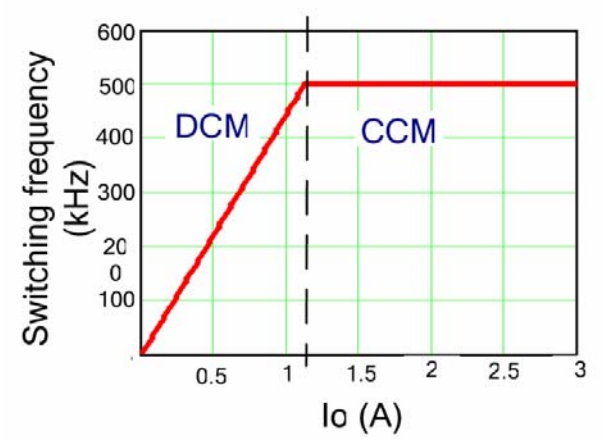
By substituting Eqs. 4.1 and 4.2 into Eq. 4.3, the duty cycle D_{DCM} in DCM can be expressed in terms of the CCM switching frequency as a function of load current as:

$$D_{DCM,\,Linear}(I_o) = \frac{2 \cdot I_o \cdot L_o \cdot f_{CCM}}{(V_{in} - V_o)} \qquad \textit{Eq. 4. 4}$$

Figure 4.3(b) shows power loss percentages when linearly modulating frequency based on the error signal. It shows how switching and driving losses consume a smaller portion of the input power as load current gets lighter. In other words, they scale with the load current. One important issue to be considered in the frequency reduction technique is that, if MH is not applied, the current ripple in the converter will significantly increase as frequency is reduced. For example, if frequency is reduced from 500 kHz to 50 kHz, the current ripple will be increased by

a factor of ten, which leads to higher conduction losses that might offset the savings in switching and driving losses. Therefore, it is important to apply MH when reducing switching frequency.

To have a better evaluation of each technique benefit, efficiency comparison between fixed frequency CCM, fixed frequency MH, and linear frequency modulation with MH is shown in Fig. 4.4. It is obvious that the frequency reduction at light load notably elevates the efficiency, and as mentioned before, this much of an improvement would not occur without being coupled with the MH technique.



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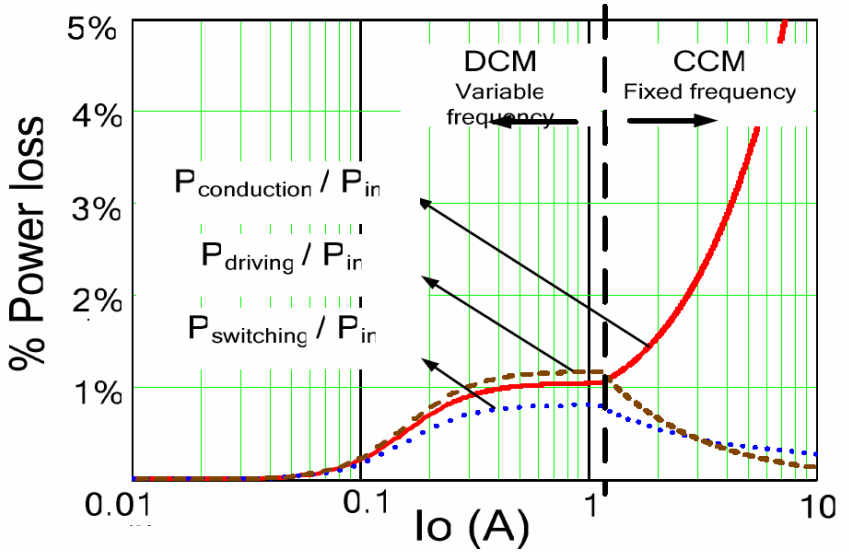


(b)

Fig.4. 3: (a) Switching frequency vs. load current when frequency varies linearly based on the compensation error signal. (b) Power Losses normalized to input power with linear frequency variation and MH techniques.

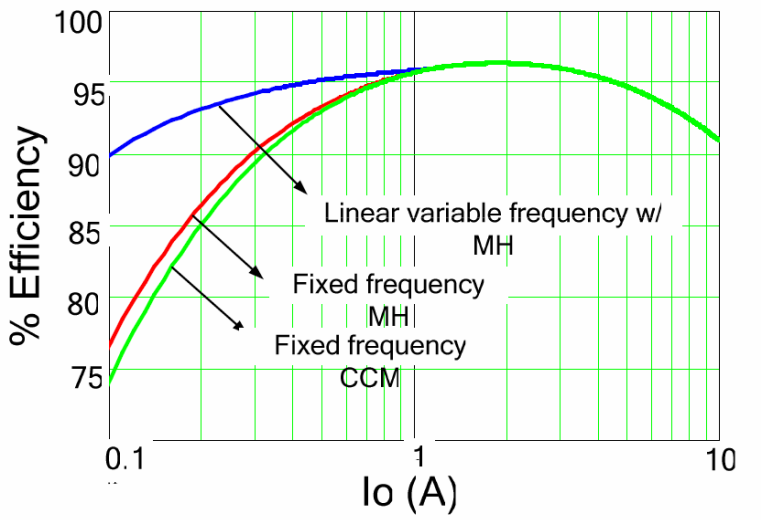


Fig.4. 4: *Efficiency vs. Load Current Comparison for fixed frequency CCM operation, fixed frequency MH and linear variable frequency with MH.*

A very important issue to be considered when modulating frequency is its effect on output voltage ripple. Detailed analyses on voltage ripple in terms of load current and switching frequency and the trade off between efficiency and voltage ripple will be discussed in the next section. A sequence of MathCAD® analyses and plots lead to optimal performance considering efficiency and voltage ripple, which lead to the proposed control technique.

4.3 Output voltage ripple analyses

In general, output voltage ripple is a function of 1) inductor current ripple 2) load current 3) inductor current continuity 4) switching frequency, and 5) output capacitance. Since MH and variable frequency techniques influence the operation of the converter in terms of frequency, current ripple and inductor current continuity, it is essential to investigate voltage ripple for both

techniques with the purpose of revealing the most favorable control technique for modulating frequency taking into account voltage ripple and efficiency. In other words, the objective is to find how the switching frequency should be modulated to achieve the desired efficiency and maintain controlled voltage ripple with the same or reduced output capacitance. In order to proceed with the voltage ripple analyses, the general voltage ripple formulas for CCM and DCM, regardless of frequency modulation, are reviewed.

The output voltage ripple in CCM is given by:

$$\Delta V_{o,\,CCM} = \frac{(1 - D_{CCM}) \cdot V_o}{8 \cdot L_o \cdot C_o \cdot f^2} \qquad \textit{Eq. 4. 5}$$

The output voltage ripple in DCM is a function of I_o, and can be expressed as:

$$\Delta V_{o,\,DCM}(I_o) = \frac{D_1(I_o) \cdot (I_{L\max.DCM}(I_o) - I_o)^2}{2 \cdot C_o \cdot I_{L\max.DCM}(I_o) \cdot f} \qquad \textit{Eq. 4. 6}$$

Where,

$I_{L\max.DCM}(I_o)$ is a function of I_o, and is given by,

$$I_{L\max.DCM}(I_o) = \frac{(V_{in} - V_o) \cdot D_{DCM}(I_o)}{L_o \cdot f}$$

D_{CCM} is the duty ratio in CCM, and is given by,

$$D_{CCM} = \frac{V_o}{V_{in}}$$

D_{DCM} is the duty ratio in DCM, and is given by,

$$D_{DCM} = \sqrt{\frac{2 \cdot I_o \cdot V_o \cdot L_o \cdot f}{V_{in} \cdot (V_{in} - V_o)}}$$

And,

$$D_1(I_o) = \sqrt{\frac{2 \cdot I_o \cdot V_{in} \cdot L_o \cdot f}{V_o \cdot (V_{in} - V_o)}} \qquad in \quad DCM$$

$D_1(I_o)$: is the ratio between the time at which the inductor current reaches zero starting from the beginning of the switching cycle, and the switching period.

Note that f is the switching frequency regardless of frequency variation.

Eq. 4.5 and Eq. 4.6 are valid as long as the capacitor ripple is dominant over ESR ripple, which is the case in the example design.

Based on Eq. 4.5 and Eq. 4.6, Fig. 4.5 shows plots of voltage ripple versus load current for a) fixed frequency CCM operation b) fixed frequency MH, and c) linear variable frequency with MH. It is apparent that CCM has constant voltage ripple for all load currents. In constant frequency MH, voltage ripple decreases when operating in DCM. When linear modulation of frequency is used, the voltage ripple increases as load current decreases, which is not acceptable in many applications. Therefore, the switching frequency must be varied in a way that maintains low and controlled voltage ripple. It will be shown next that in order to achieve improved conversion efficiency while maintaining steady-state performance, frequency should be varied based on a non-linear function of load current.

Figure 4.6(a) shows a 3D surface plot of output voltage ripple vs. frequency vs. load current in DCM load range. It shows that for any specific load current value, the frequency can be set to a certain value to obtain the desired voltage ripple; reducing frequency beneath that value will increase ripple magnitude. For simpler visualization, one can observe Fig. 4.6(b), which shows output voltage ripple versus frequency under different load currents. This plot facilitates finding the switching frequency value at which the voltage ripple equals the desired value for any load, which is set here to be equal to the CCM output voltage ripple value.

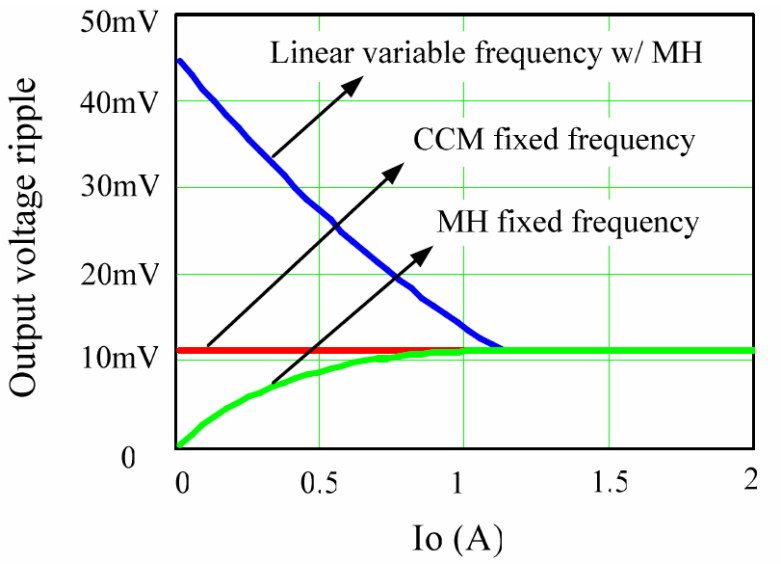
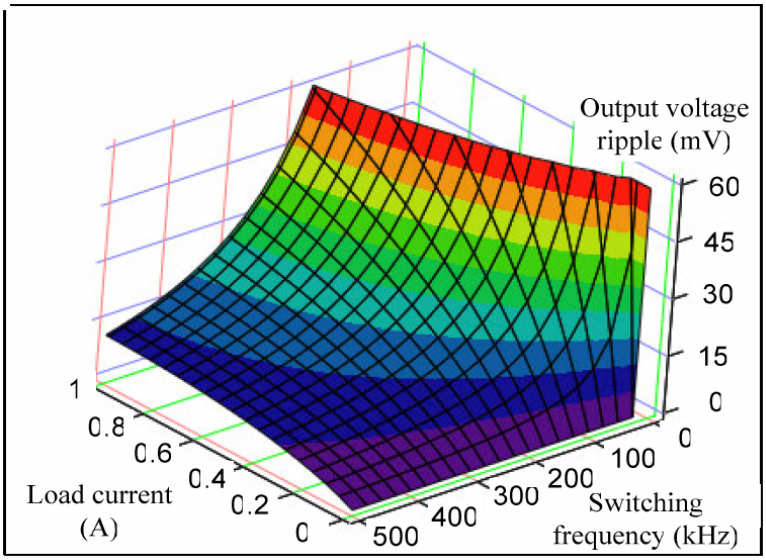
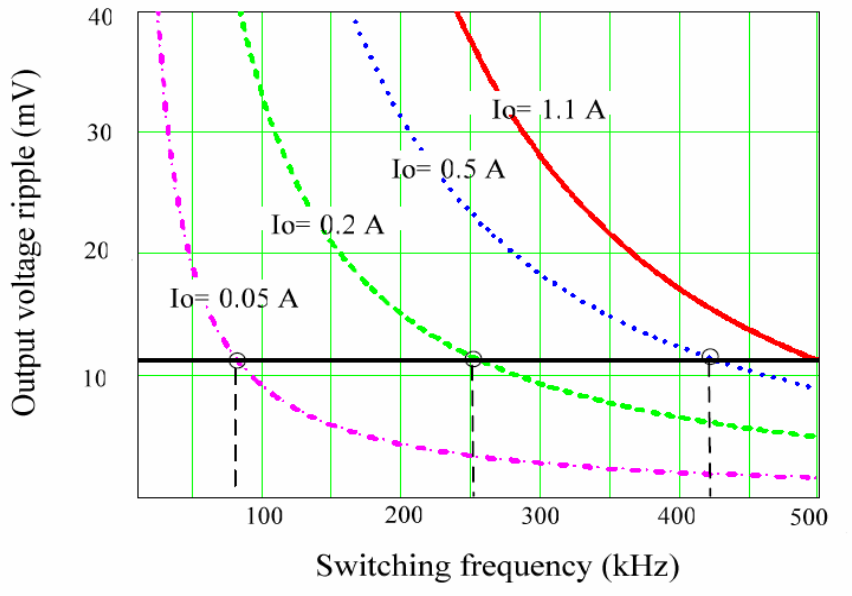


Fig.4. 5: *Output voltage ripple vs. output current for CCM operation, MH and linear variable frequency with MH.*



(a)



(b)

Fig.4. 6: (a) 3D surface plot of voltage ripples vs. frequency vs. load current in DCM load range, and (b) Voltage ripple vs. frequency for different values of load current

A scan through the switching frequency range for each load current value to find the switching frequency value that guarantees an output voltage ripple equal to that in CCM can be performed. Fig. 4.7 shows a plot of switching frequency versus load current as a result of such a scan. It clearly shows that non-linear switching frequency modulation is required for constant output voltage ripple.

Figure 4.8 shows a plot of inductor peak current versus load current for switching frequency varying non-linearly based on a desired fixed voltage ripple which is set to be equal to CCM ripple, i.e., the peak inductor current that results from modulating the switching frequency as in Fig. 4.7 in order to maintain controlled output voltage ripple. This non-linear switching frequency modulation results in a linear peak inductor current. Therefore, it can be concluded that in order to improve conversion efficiency while maintaining controlled output voltage ripple, the peak inductor current should vary linearly with the load current in DCM mode. This is achieved by non-linearly varying the switching frequency.

The conclusion drawn in the previous paragraph is the main motivation of the first part of the presented control method. The aim is to non-linearly reduce frequency at light loads to improve efficiency and maintain desired voltage ripple at the same time. This is realized by controlling the inductor peak current.

Certainly, there is a trade off between converter efficiency and voltage ripple. The trade off can be depicted by comparing the switching frequency at a certain load current for the two cases of linear and non-linear frequency modulation. Conversely, controlled voltage ripple is achieved.

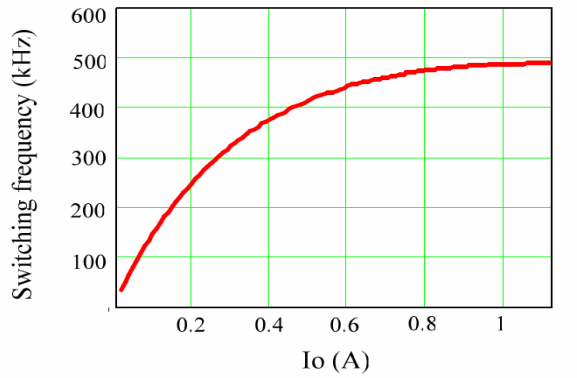


Fig.4. 7: Switching frequency required for fixed voltage ripple vs. Load current

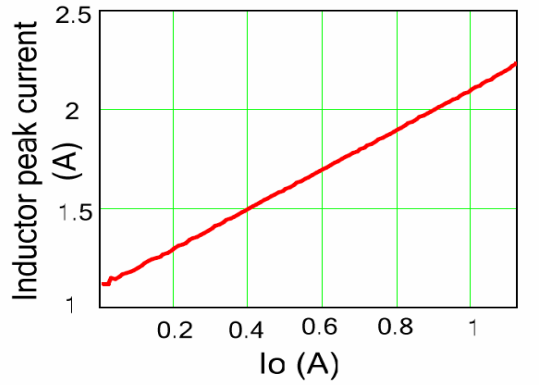


Fig.4. 8: *Inductor peak current vs. load current for switching frequency varying non-linearly for fixed voltage ripple equal to CCM ripple*

The non-linear switching frequency required for a constant output voltage ripple in DCM equal to the CCM ripple can be derived by equating Eq. 4.5 and Eq. 4.6, as follows:

$$\frac{D_{1,DCM,non-Linear}(I_o)\cdot(I_{L\max.DCM,non-Linear}(I_o)-I_o)^2}{2\cdot C_o\cdot I_{L\max.DCM,non-Linear}(I_o)\cdot f_{DCM,non-Linear}(I_o)}=\frac{(1-D)\cdot V_o}{8\cdot L_o\cdot C_o\cdot {f_{CCM}}^2} \qquad \textit{Eq. 4. 7}$$

Where:

$f_{DCM,non-Linear}(I_o)$: is the DCM non-linear switching frequency as function of load current that guarantees constant voltage ripple at DCM equal to CCM ripple.

And,

$$D_{1,non-Linear}(I_o)=\sqrt{\frac{2\cdot I_o\cdot V_{in}\cdot L_o\cdot f_{DCM,non-Linear}(I_o)}{V_o\cdot(V_{in}-V_o)}}$$

$$I_{L\max.DCM,non-Linear}(I_o)=\frac{(V_{in}-V_o)\cdot D_{DCM,non-Linear}(I_o)}{L_o\cdot f_{DCM,non-Linear}(I_o)}$$

From Eq. 4.7, $f_{DCM,non-Linear}(I_o)$ is obtained as follows:

$$f_{DCM,non-Linear}(I_o)=\frac{4\cdot L_o\cdot V_{in}\cdot D_{1,non-Linear}(I_o)\cdot(I_{L\max.DCM,non-Linear}(I_o)-I_o)^2\quad {f_{CCM}}^2}{I_{L\max.DCM,non-Linear}(I_o)\cdot(V_{in}-V_o)\cdot V_o} \qquad \textit{Eq. 4. 8}$$

Plotting switching $f_{DCM,non-Linear}(I_o)$ versus Io yields the same plot shown in Fig. 4.7.

It is also possible to derive the duty cycle $D_{DCM,non-Linear}(I_o)$ as a function of load current at non-linear modulation, as shown in Eq. 4.9,

$$D_{DCM,non-Linear}(I_o)=\frac{2\cdot L_o\cdot f_{CCM}\cdot(I_{L\max.DCM,non-Linear}(I_o)-I_o)}{V_{in}-V_o}\sqrt{\frac{2\cdot I_o\cdot D_{1,non-Linear}(I_o)}{I_{L\max.DCM,non-Linear}(I_o)}} \qquad \textit{Eq. 4. 9}$$

It is now possible to plot duty cycle as a function of load current for fixed frequency with MH, linear frequency modulation with MH, and non-linear frequency modulation with MH as shown in Fig. 4.9. Note that the duty cycle represents the compensator error signal. As shown in Fig. 4.9, the duty cycle at non-linear modulation falls between the other two curves, and it is related to error signal and switching frequency. It can be concluded that non-linear modulation combines the improved efficiency as in linear modulation with controlled voltage ripple as in fixed frequency.

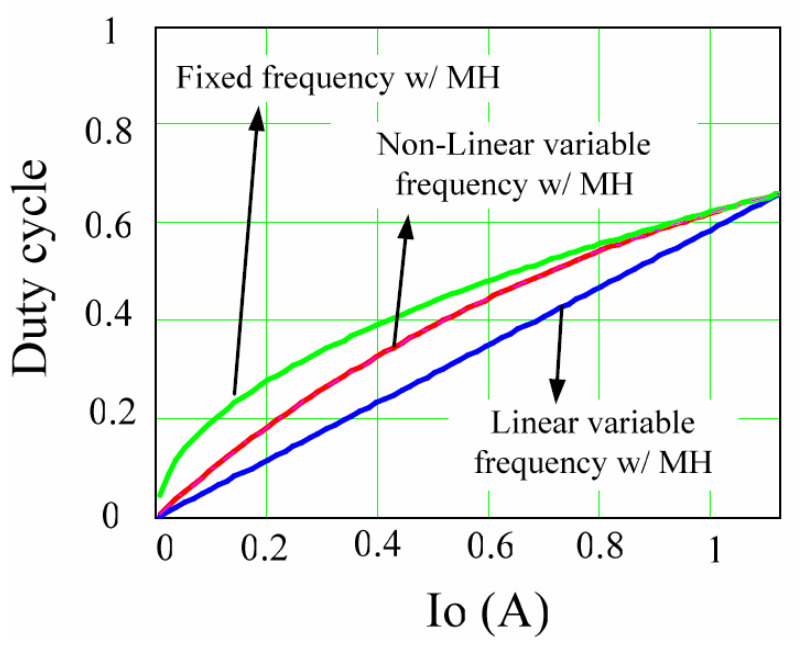


Fig.4. 9: *Duty cycle in DCM vs. Load Current.*

It is the designer's call to judge how much efficiency needs to be traded off with output voltage ripple. It is dependant upon the output voltage ripple requirements and the allowed space and cost of the converter output capacitors. One can allow some more voltage ripple relaxation for the sake of gaining higher efficiency. Figure 4.10 shows efficiency versus load current when

modulating frequency linearly, non-linearly to maintain output voltage ripple in DCM equal to the CCM ripple, and non-linearly to maintain output voltage ripple in DCM equal to twice the CCM ripple.

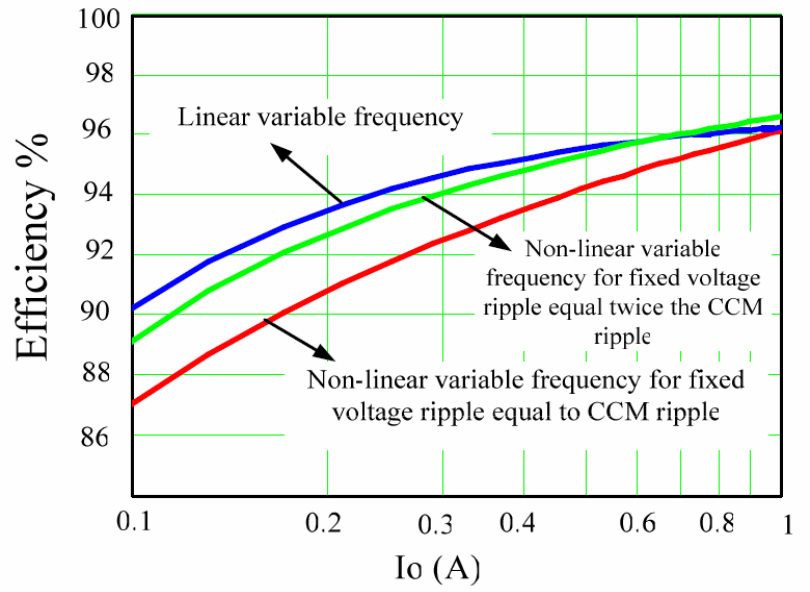


Fig.4. 10: *Efficiency vs. Load current comparison between linear frequency modulation, non-linear frequency modulation for fixed output voltage ripple equal to CCM ripple, and non-linear frequency modulation for fixed output voltage ripple equal to twice the CCM ripple.*

4.4 Pulse-Sliding technique (PSL)

In this section, a non-linear variable frequency technique, namely Pulse-Sliding (PSL), is presented to improve the VR efficiency at lighter loads while maintaining low and controlled steady-state voltage ripple and good dynamic response without adding large output capacitance. In another words, the objective of this section is to present techniques that result in significant efficiency improvement at light loads compared with the fixed frequency case, with low and well

controlled voltage ripple, achieving the advantages of both variable frequency and fixed frequency modes and eliminating their disadvantages.

Figure 4.11 shows the PSL control flowchart and an example of analog implementation circuitry (can be also implemented with digital controller). S_{Li} and S_{Hi} are the synchronous complementary PWM control signals generated by the PWM generator while S_{LF} and S_{HF} are the final PWM control signals that will drive the buck VR low-side and high-side switches, respectively. Note that Fig. 4.11 is for demonstration of operation only, and that the actual circuit in the implementation may vary.

The inductor current is sensed to detect when it tries to go below zero using comparator comp #1. It will go output high and reset SR #1 to force DCM mode by forcing S_{LF} to go low. SR #1 is set again at the next switching cycle by the OR gate. SR #2 generates the high-side switch control S_{HF} ; it is set by S_{Hi} and reset by an AND gate output that will go high if both comp #2 output is high and SR #3 is set. Comp #2 output will go high if the inductor current peak exceeded certain maximum value $V_{L\max-DCM}$ in DCM and SR #3 will be set only when comp #1 output is high, which means that the present mode is DCM. Therefore, the peak current limit will be only active in DCM mode to maintain certain output voltage ripple. There are two schemes for setting the peak current limit: it can be either a constant value or it can be dynamically varying relative to the compensator error signal; both methods will be discussed later in this section. SR #3 will be reset each time SR #1 is set by S_{Li} or by the AND gate

output. The reason is whenever SR #2 is reset in DCM to force S_{HF} to go low and prevent inductor peak current from exceeding the limit, SR #1 should be set to provide a path for the inductor current.

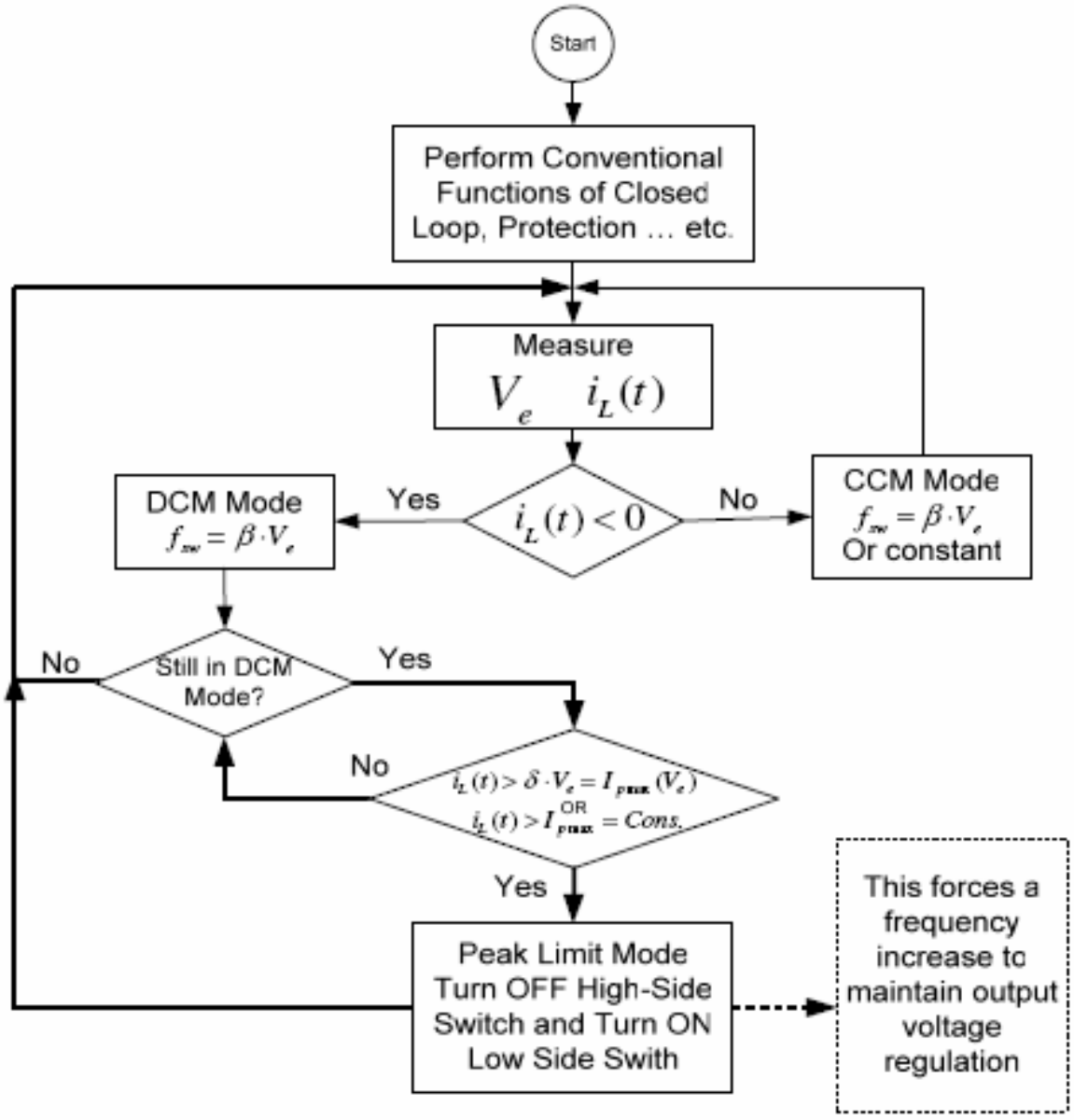
S_{Li} and S_{Hi}, generated by the PWM generator will have switching frequency in both CCM and DCM modes based on the VCO synchronization signal. The VCO input voltage is controlled by voltage signal proportional to the PWM compensator error signal ($\beta \cdot V_e$). Notice that $\beta \cdot V_e$ is proportional to the duty-cycle, which is almost a fixed value in CCM and drops linearly as the VR goes to DCM.

As mentioned above, there are two proposed methods of limiting the peak current in DCM, which are as follows:

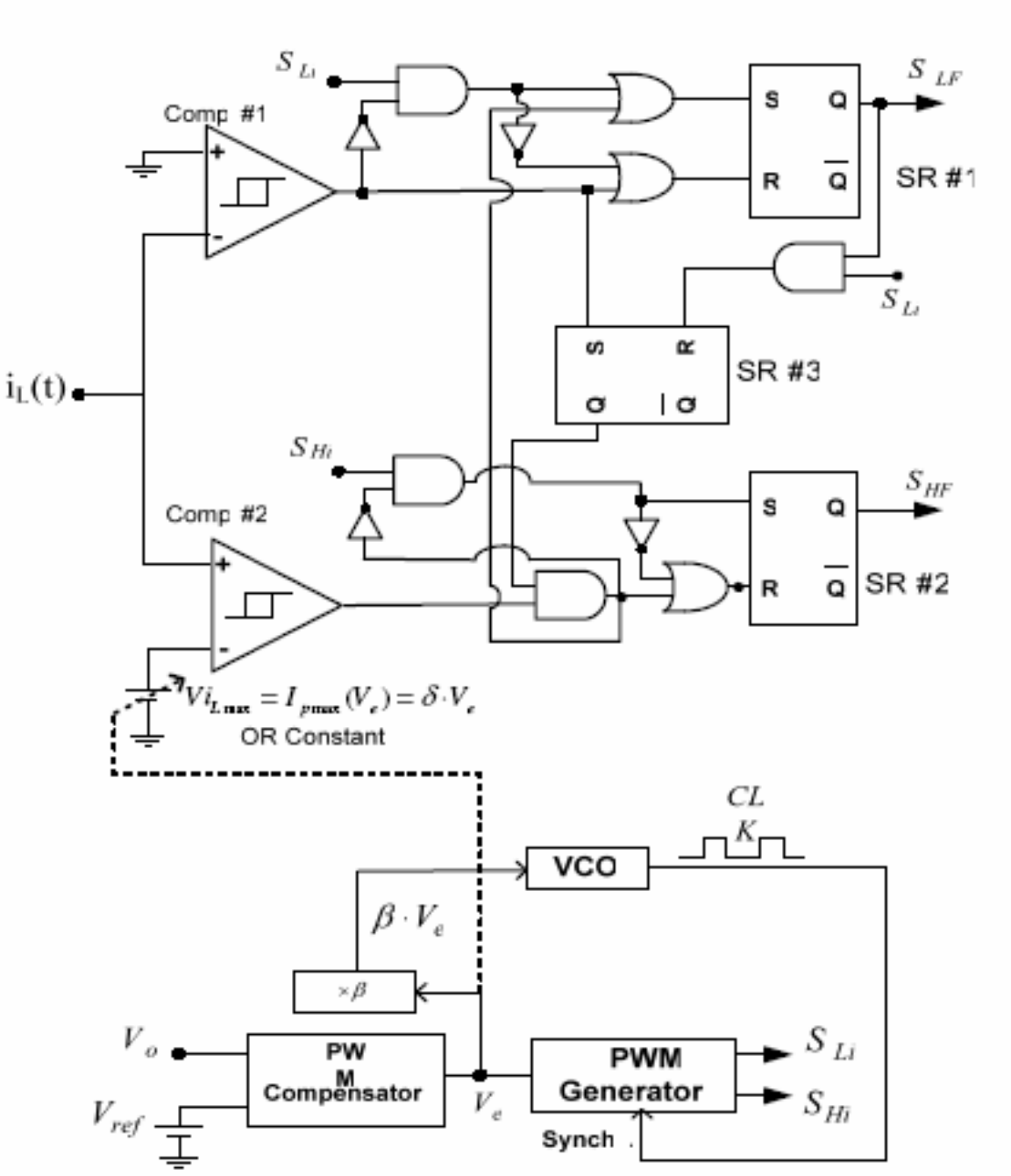
4.4.1 PSL with fixed current peak limiting (FPSL):

The first method is to set the peak current limit ($V_{L\max-DCM}$) to a predetermined fixed value. This method has the advantage of simplicity, but it does not provide the optimal situation regarding voltage ripple and efficiency. The reason is that the peak current limit will be a fixed value that is being determined by considering the worst case condition of voltage ripple which is at very light load current. Therefore, higher load current in DCM is forced to obey this limit that will be smaller than the limit required for that load current to achieve the voltage ripple designed for very light load situations. Moreover, since higher current in DCM will have limited peak

current as in a very light load, the VR is forced to increase frequency at higher currents to maintain output voltage regulation, causing lower VR efficiency improvement.



(a)



(b)

Fig.4. 11: (a) PSL Controller Flowchart and (b) Implementation Example

Figure 4.12 shows the voltage ripple versus load current for an example of setting the peak current to a constant value designed to assure that the very light load voltage ripple is equal to twice the CCM voltage ripple (FPSL). It shows that voltage ripple at very light load satisfies the desired value. It also shows how voltage ripple at higher current in DCM will have a much lower voltage ripple that may be unnecessary. Analyses demonstrate that in such case at high currents in DCM, switching frequency will go up to 1MHz (twice CCM switching frequency) as load varies in order to sustain regulated output voltage.

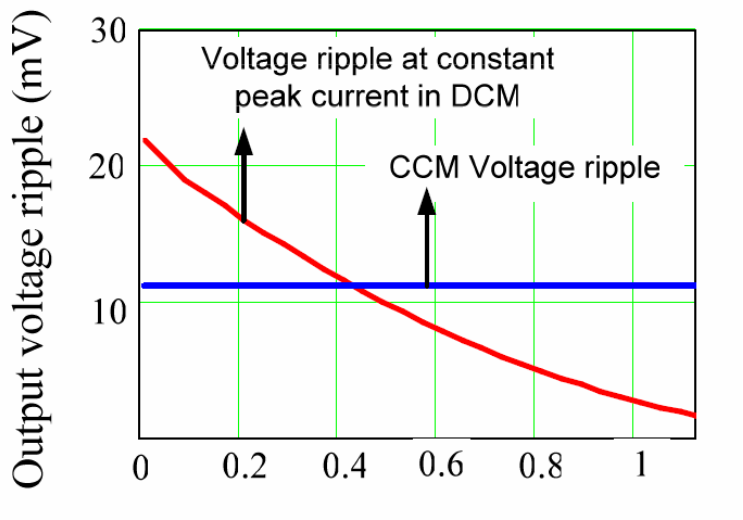


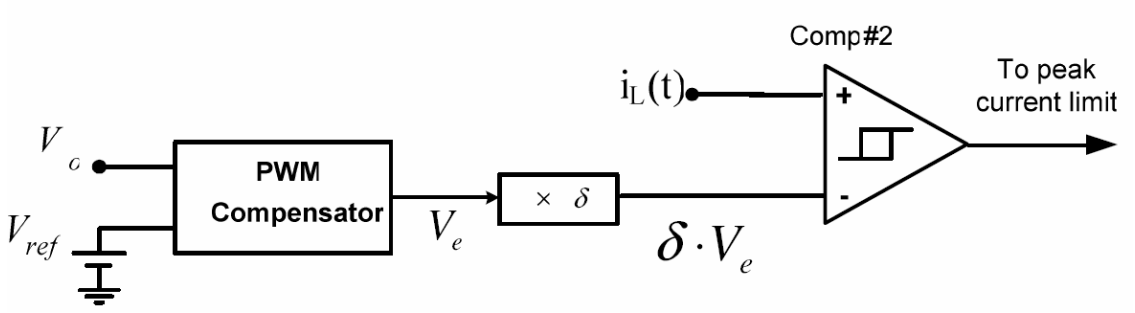
Fig.4. 12: Voltage ripple vs. load current for the case of setting the peak current limit to a constant value that assures a voltage ripple at very light load equal to twice the CCM voltage ripple.

4.4.2 PSL with dynamic current peak limiting (DPSL):

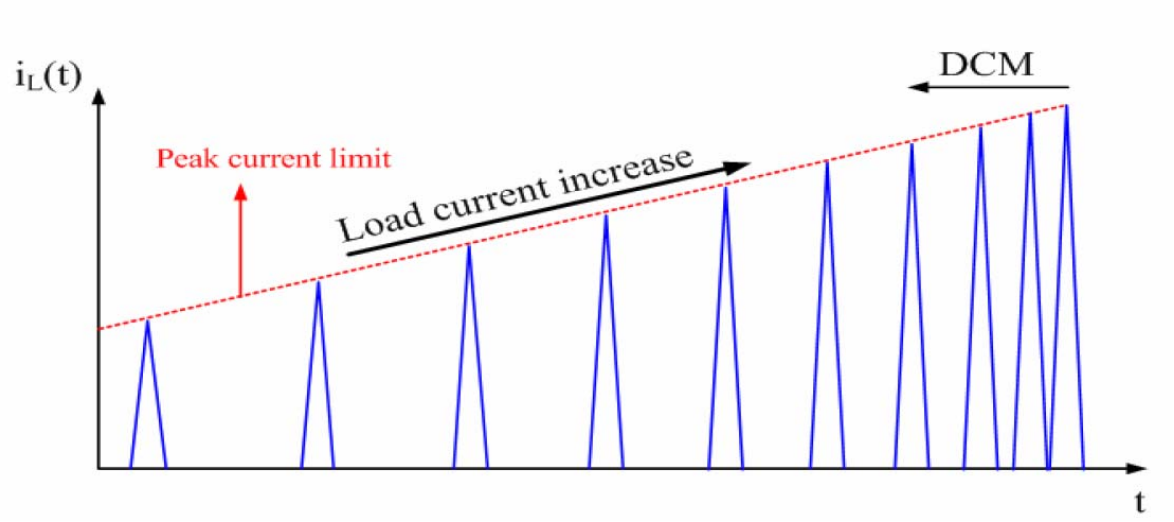
Observing the behavior of the first method of setting the peak current limit to a constant value leads to the second method. In the second method, the peak current limit is dynamically adapted

to load current or compensation error signal. In the previous discussion it was stated that frequency must vary non-linearly relative to load current to maintain a fixed voltage ripple and Fig. 4.8 showed a linear relationship of peak current versus load current given a fixed voltage ripple. This method indirectly suggests varying switching frequency non-linearly with load current by limiting the peak current to a dynamically changing value that is linearly related to load current as in Fig. 4.8. In other words, limiting the peak current linearly relative to load current is the second proposed method to force switching frequency to vary non-linearly in order to achieve a fixed voltage ripple over the load current range. Unlike the first method of setting constant peak current limit, this method guarantees fixed voltage for all load currents without increasing switching frequency significantly. Therefore, higher VR efficiency is gained while achieving a fixed voltage ripple.

Knowing that the compensator error signal has a linear relation with the load current when operating in DCM, the second method of adjusting the peak current limit dynamically, DPSL, as load current changes can be implemented by feeding a voltage signal proportional to the compensator error signal ($\delta \cdot V_e$) to comp #2. Figure 4.13(a) shows a simplified implementation of peak current limit based on compensator error signal, while Fig. 4.13(b) shows the inductor current versus time while load current is varying. It shows that peak current is more peak limited at light load in order to ensure controlled output voltage ripple.



(a)



(b)

Fig.4. 13: (a) Implementation of peak current limit based on compensator error signal. (b) Inductor current vs. time as load current varies.

The discussion above stated that the DPSL is better optimized and more efficient than FPSL with extra required circuitry. Figure 4.14 shows an efficiency comparison for both methods, FPSL and DPSL, in the case of fixing voltage ripple to twice the CCM ripple.

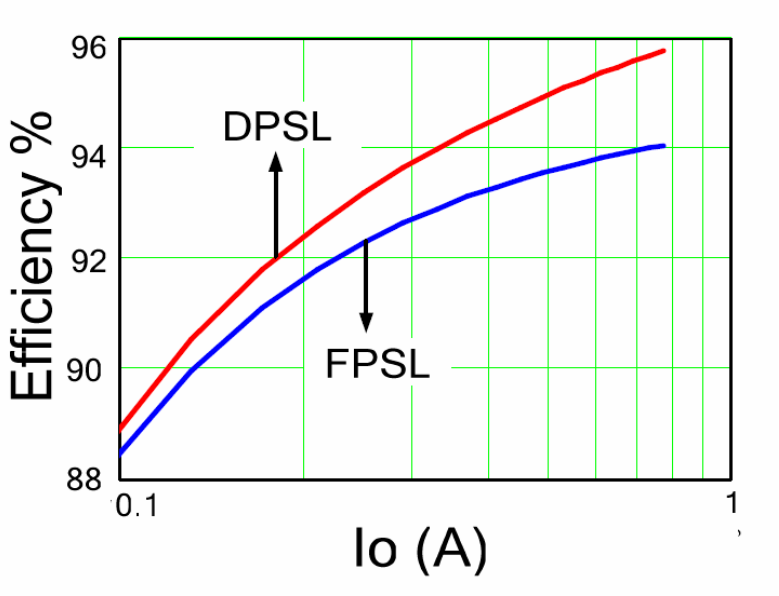


Fig.4. 14: Efficiency comparison between FPSL and DPSL methods.

4.5 Input voltage feed forward to compensate for switching frequency drift at variable line voltages

As shown in Fig. 4.11(b), switching frequency is modulated as a function of the compensator error signal ($\beta \cdot V_e$), and the peak limit of the inductor current is a function of the compensator error signal ($\delta \cdot V_e$). Since V_e is a function of the input voltage, the switching frequency and peak limit will also vary with the input voltage. For example, if input voltage is increased, the error signal V_e will decrease so that the duty cycle gets smaller in order to maintain regulated output voltage; therefore, the switching frequency will be lowered. This suggests feed forwarding the input voltage to the VCO in order to eliminate the switching frequency and peak limit dependency on the input voltage, aiming to maintain switching frequency modulation level

almost constant as line voltage changes. To do so, β and δ could be designed to be variable as a function of the input voltage.

Figure 4.15 shows a plot of the modulation ramp signal generated by the controller modulator. From this plot a formula of the error signal V_e as a function of duty cycle, offsets voltage of the ramp signal V_{offset}. The ramp signal peak-to-peak voltage V_{p-p} can be derived as given by Eq. 4.10:

$$V_e = D \cdot V_{p-p} + V_{offset} \qquad \textit{Eq. 4. 10}$$

During CCM operation, the duty cycle is $D = V_o / V_{in}$, so V_e in CCM is obtained as given in Eq. 4.11:

$$V_e = \frac{V_o \cdot V_{p-p}}{V_{in}} + V_{offset} \qquad \textit{Eq. 4. 11}$$

It is apparent from Eq. 4.11 that error signal V_e is dependent on input voltage; this means that switching frequency will inversely scale with the input voltage variation. Therefore, a signal should be extracted from the error signal V_e that is related to load current and independent of input voltage, so that the input voltage variation will not have an affect on the switching frequency or on the dynamically adjusted peak current limit of the DPSL.

There are two methods to extract such a signal. The first is simple to implement, but it is only capable of minimizing the input voltage effect on switching frequency instead of canceling it.

This method is shown in Fig. 4.16(a). The ramp signal offset voltage V_{offset} is first subtracted from the error signal V_e; the V_{offset} value can be found in the controller datasheet, or it can be extracted experimentally for more accurate processing. Then a signal proportional to the input voltage ($k \cdot V_{in}$) is added. These two steps of subtracting and summing can be easily implemented utilizing a simple Op-Amp circuit.

From Eq. 4.10, the best way of eliminating the input voltage from the equation is to use a multiplying function. This leads to the second method, which is shown in Fig. 4.16(b). The ramp signal offset voltage V_{offset} is first subtracted from the error signal V_e as in the first method, and then the result is multiplied by the input voltage. The result in CCM will be $V_o \cdot V_{p-p}$, which is a constant value regardless of the input voltage. Doing so will eliminate the input voltage effect on the switching frequency, and frequency modulation will be the same for all input voltages. Similarly, the new extracted signal will eliminate the peak current limit dependency on the input voltage.

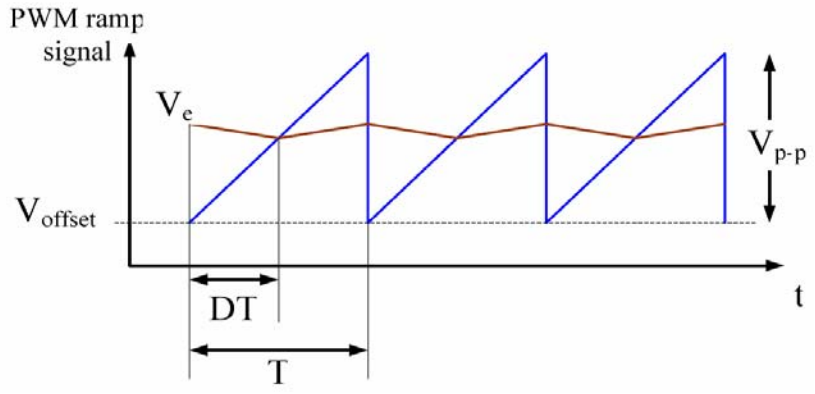
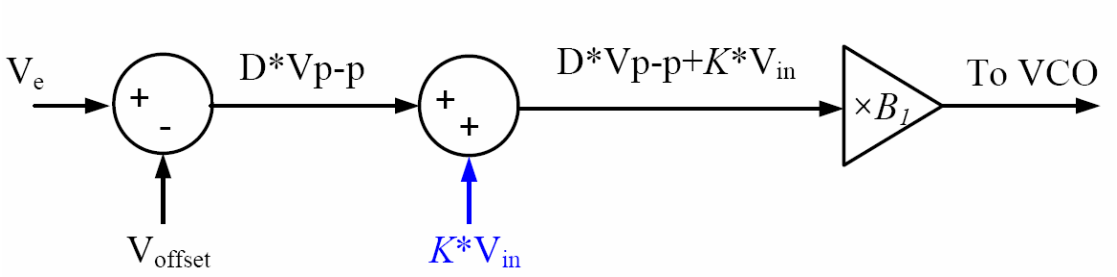
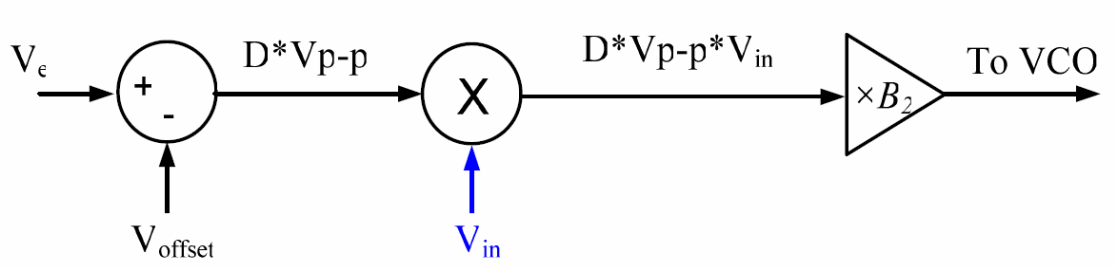


Fig.4. 15: PWM Modulation and Ramp Signal



(a)



(b)

Fig.4. 16: Two methods of input voltage feed forward to eliminate frequency modulation and peak inductor limit dependency on the input voltage.

4.6 Frequency modulation effect on the transient response

Loads such as processors appear to be variable loads for the VR; their power consumption dynamically varies with applications or usage conditions. Therefore, the VR must be capable of delivering such varying power levels to the load with fast dynamic performance, i.e., with fast stable loop and low or controlled dynamic voltage deviation.

The main concern regarding load current transient is when the load rapidly switches to lower or higher levels of power consumption; it takes time for the VR control loop and the VR inductor to

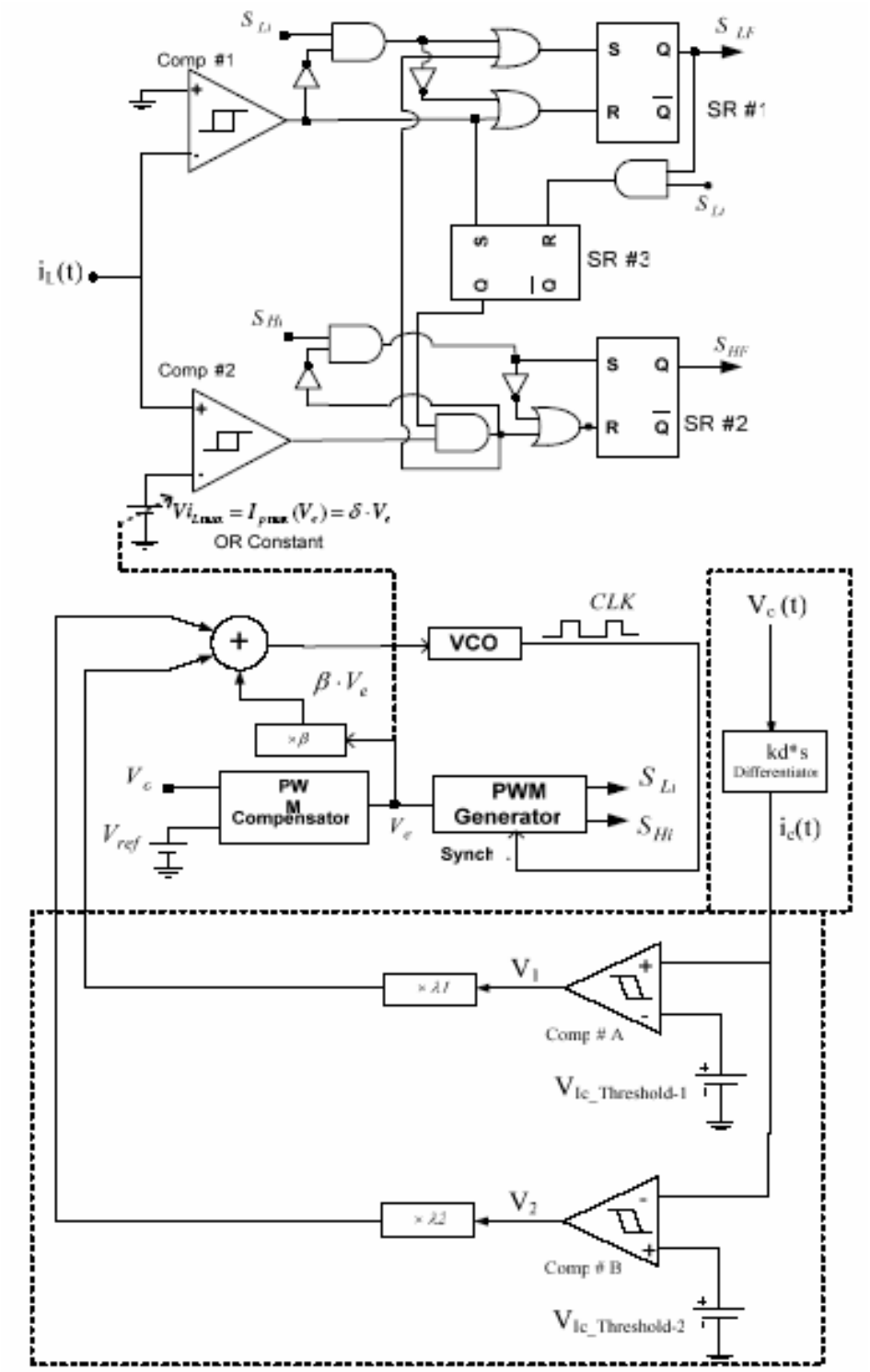
adapt to the new power level. The inductor will try to modify the amount of its stored energy to keep up with the new load condition. However, the nature of an inductor is to resist its current change (d_i/d_t) [44]. How fast an inductor can follow up with the new energy state depends on the inductance value—the smaller its value, the faster its response to a load transient. When load transient occurs, until inductor energy reaches steady state, the difference between the energy drawn by the load and the energy supplied by the VR is supplied by the output. A transient in the output capacitor current will cause a voltage undershoot in case of step-up load transient or a voltage overshoot in case of a step-down load transient. The amount of voltage overshoot or undershoot is determined by many parameters such as filter inductance, output capacitance, closed loop speed, switching frequency, load transient step, and slew rate [32-34]. Switching frequency is a means of how fast a VR updates its state in terms of duty cycle and inductor current to follow load transient. Therefore, modulating switching frequency during load transient will influence the VR dynamic performance [33]. With frequency modulated VR, and especially in the case of load step-down transient where the frequency is reduced when stepping to lighter load, the VR transient response is slowed, meaning longer settling time and larger output voltage deviation.

Figure 4.17 shows the presented PSL method with a new proposed part added to it for eliminating the effect of frequency reduction on transient response. When a load transient occurs, a signal is fed to the VCO, so that the switching frequency is set to be equal to the normal CCM operation frequency or higher during the transient state, and once the transient is completed, the VCO is allowed to reduce its output frequency based on the load current. The signal sent to the

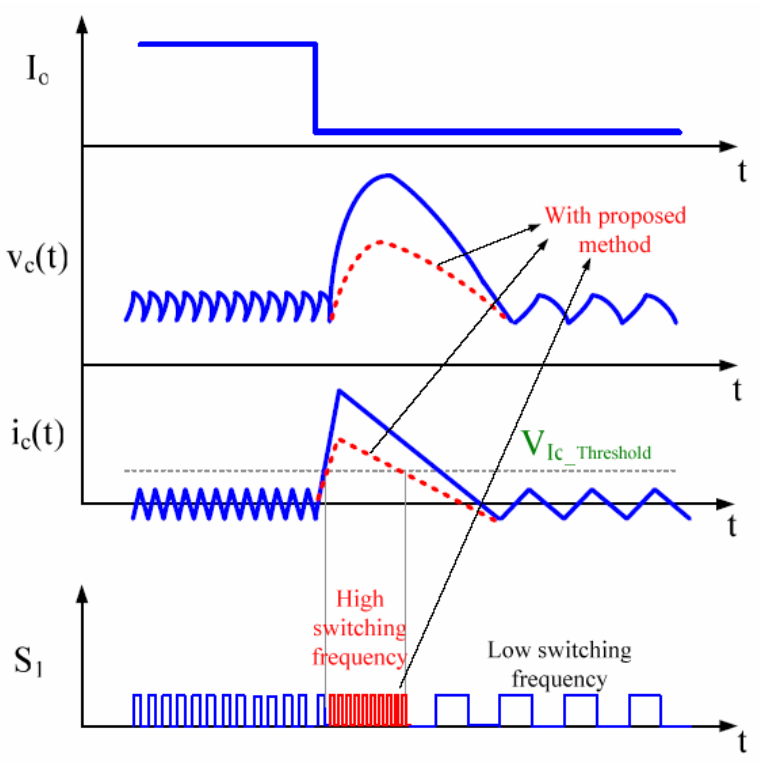
VCO is generated by comparing the capacitor current signal to a threshold value. During transients, capacitor current will step beyond that threshold, and when transient state is completed it will go back to its steady state (zero average). Capacitor current could be sensed by differentiating its voltage ($i_c=C*dv_c/dt$). Figure 4.17(a) shows the implementation of the proposed method and Fig. 4.17(b) shows waveforms of output capacitor voltage, capacitor current, and higher FET's gate-source voltage during a step-down load transient. When a load step down occurs, the capacitor current will overshoot beyond the threshold, the switching frequency will be forced to increase to the normal CCM frequency to speed up VR response; once the capacitor current returns to steady state, the switching frequency will be allowed to adapt to the load current.

Capacitor current is a preferred way of indicating transient condition since it is a lossless method for detecting the load step, its average current equals to zero at steady state, and the absence of DC component in the capacitor current facilitates using a fixed threshold for detecting transient conditions [24].

This method guarantees response to load transient conditions with fixed high switching frequency in order for the VR to change its power level as fast as possible with low voltage spikes and a short settling time. Moreover, it has the potential to reduce the required output capacitance to meet dynamic requirements, and therefore, reduce the size and cost of the VR.


Comp #1
Comp #2
SR #1
SR #2
SR #3
S
R
Q
$i_L(t)$
$Vi_{L\max} = I_{p\max}(V_e) = \delta \cdot V_e$
OR Constant
CLK
VCO
$\beta \cdot V_e$
$\times\beta$
V_c
V_{ref}
PW M Compensator
V_e
PWM Generator
Synch
S_{Li}
S_{Hi}
$V_c(t)$
kd*s Differentiator
$i_c(t)$
$\times\lambda 1$
V_1
Comp # A
$V_{Ic\_Threshold-1}$
$\times\lambda 2$
V_2
Comp # B
$V_{Ic\_Threshold-2}$

(a)



(b)

Fig.4. 17: (a) Implementation of transient improvement for PSL method and (b) output capacitor's voltage and current waveforms associated with step-down load transient

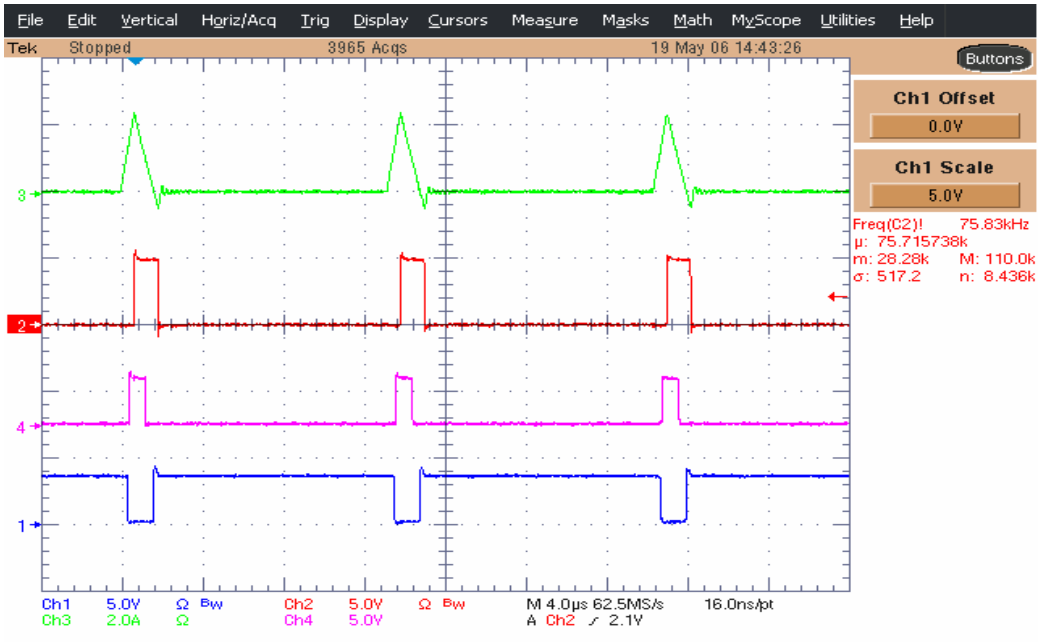
4.7 Experimental results

To evaluate the presented PSL control techniques and to make a comparison with other techniques reviewed earlier in this paper, a prototype was built with the following specifications: *Vin= 5V~12V, Vo= 3.3V, Lo= 1uH, Co= 50uF* , *ESR=* $1m\Omega$, and *IRF7821* [25] is selected for both low and high FETs. In this section, a comparison between the other control techniques discussed earlier and the presented PSL technique is made considering inductor current ripple in

DCM, output voltage ripple, frequency variation, conversion efficiency, and dynamic response. As will be shown next, results clearly verify the conceptual analyses and trends discussed in the earlier sections.

4.7.1 PSL logic circuit operation experimental results

The PSL logic circuit receives input PWM signals from the conventional closed loop controller and outputs modified PWM signals to FETs' gates based on the sensed inductor current and output voltage information. Figure 4.18 shows experimental waveforms when load current is light. When the inductor current reaches the peak current limit, comparator # 2, as shown in Fig. 4.11(b), will output logic high signal to turn off the higher FET and turn on the lower FET. The Inductor current will start to discharge until it reaches zero where comparator # 1 will output high signal to turn off the lower FET.



Waveforms from top to bottom are: Inductor current, lower FET's gate-source voltage, comparator # 2 output, and comparator # 1 output

Fig.4. 18: PSL logic circuit operation experimental waveforms

4.7.2 Peak current limit experimental results

The PSL control is implemented by feeding the error signal to the current limiting circuit as in Fig. 4.13(a). Figure 4.19 shows a plot of the inductor peak current versus load current obtained from the experimental prototype. It can be seen that in linear frequency variation control the peak current is fixed. Having a fixed current ripple while reducing switching frequency will indisputably cause increased output voltage ripple according to Eq. 4.6. However, in the presented PSL control, peak current is directly related to load current, so that current ripple is

lowered at reduced switching frequencies to maintain constant and controlled output voltage ripple.

Figure 4.19 shows good agreement with the theoretical plot shown in Fig. 4.8.

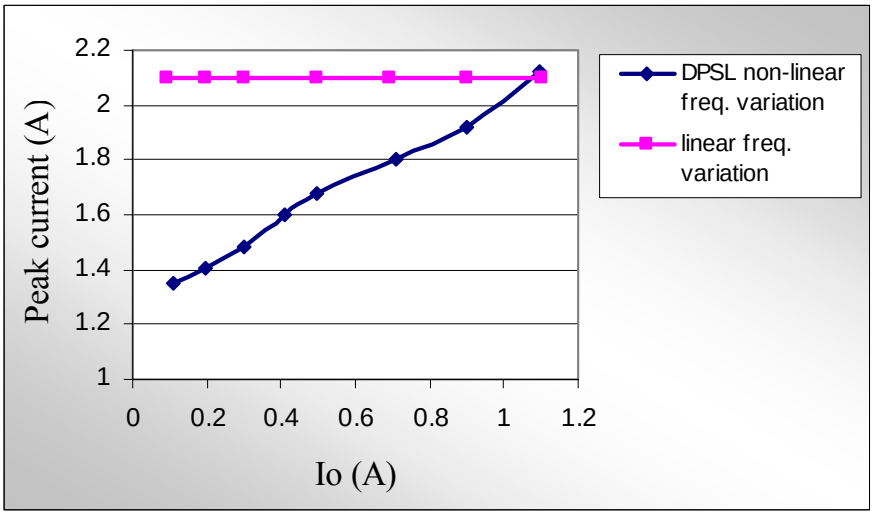
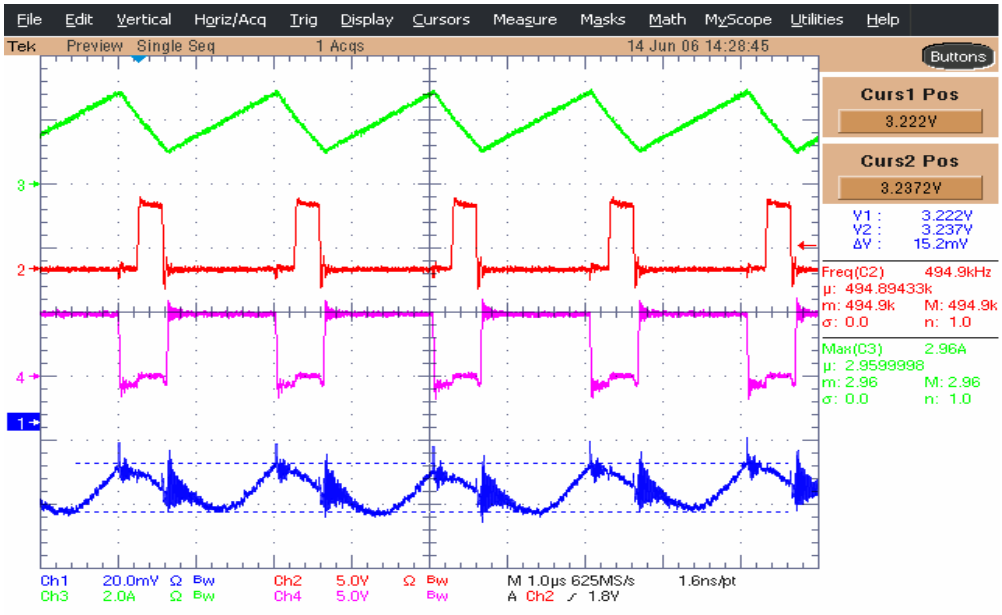


Fig.4. 19: *A plot of the inductor peak current vs. load current measured from the experimental prototype.*

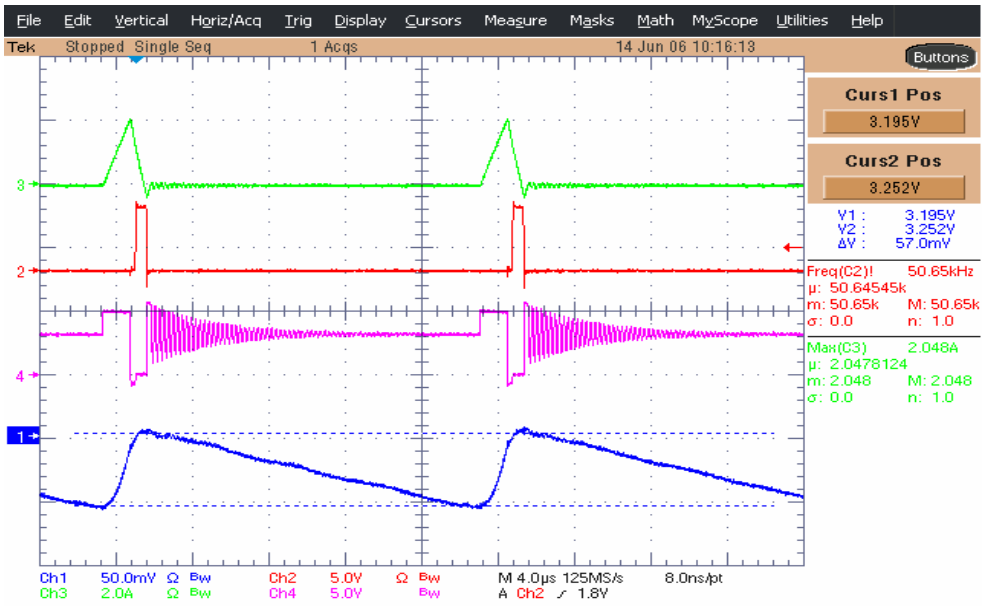
4.7.3 Output voltage ripple experimental results

A major benefit of the PSL control method is to limit output voltage ripple while still achieving improved efficiency at lighter load currents. The PSL control is implemented to guarantee output voltage ripple equal to the CCM voltage ripple. (As mentioned earlier, it can also be set to any other value.) Figure 4.20 shows some experimental waveforms at different loads. Figure 4.20(a) depicts CCM operation at Io=2A; the cursors in the figure show that the output voltage ripple is 15 mV. Figure 4.20(b) captures Io=100mA with linear frequency variation in DCM; the cursors in the waveform show the output voltage ripple is 57 mV, which is higher than CCM voltage

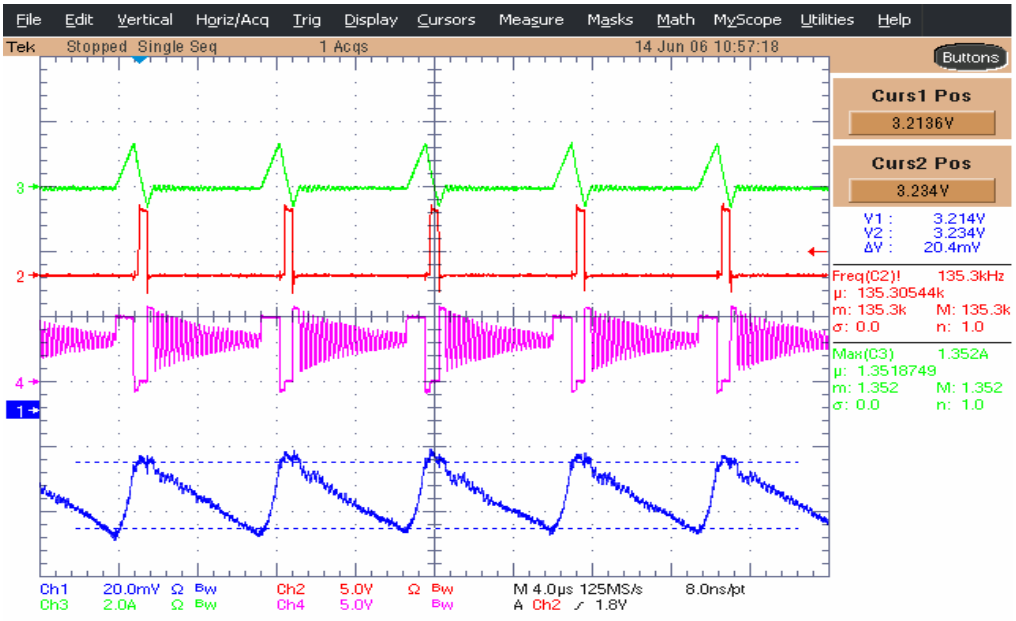
ripple. Figure 4.20(c) captures Io=100mA with the presented PSL control; the cursors in the waveform show the output voltage ripple was brought down to approximate CCM voltage ripple and equal to 20 mV.



(a)



(b)



(c)

Waveforms from top to bottom: inductor current, lower FET's gate-source voltage (Vgs), lower FET's drain-source voltage (Vds), and output voltage ripple

Fig.4. 20: *Experimental Waveforms at Different Loads: (a) CCM at Io=2A, (b) DCM at Io=100mA with linear frequency variation (c) DCM at Io=100mA with PSL non-linear frequency variation.*

A plot of output voltage ripples versus load current for fixed frequency with MH, linear frequency variation with MH, and presented PSL with MH obtained from the experimental prototype, is shown in Fig. 4.21. It can be observed that in conventional linear frequency variation, the output voltage ripple increases at light load, where the presented PSL maintains constant output voltage ripple over the whole load range.

Figure 4.21 shows high agreement with the theoretical plot shown in Fig. 4.5.

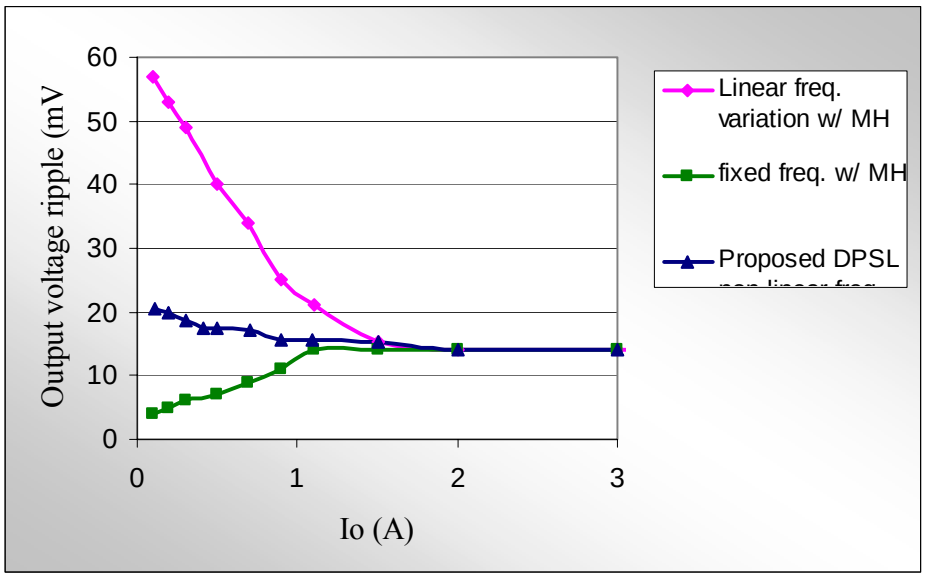


Fig.4. 21: Output voltage ripple vs. output current comparison obtained from experimental prototype

4.7.4 Frequency variation experimental results

As mentioned earlier, the presented PSL drives switching frequency to be non-linearly modulated due to peak current limiting. Figure 4.22 shows how frequency varies over load current range for linear frequency variation control and the presented PSL control (from experimental measurements).

Figure 4.22 shows high agreement with theoretical plot shown in Fig. 4.7.

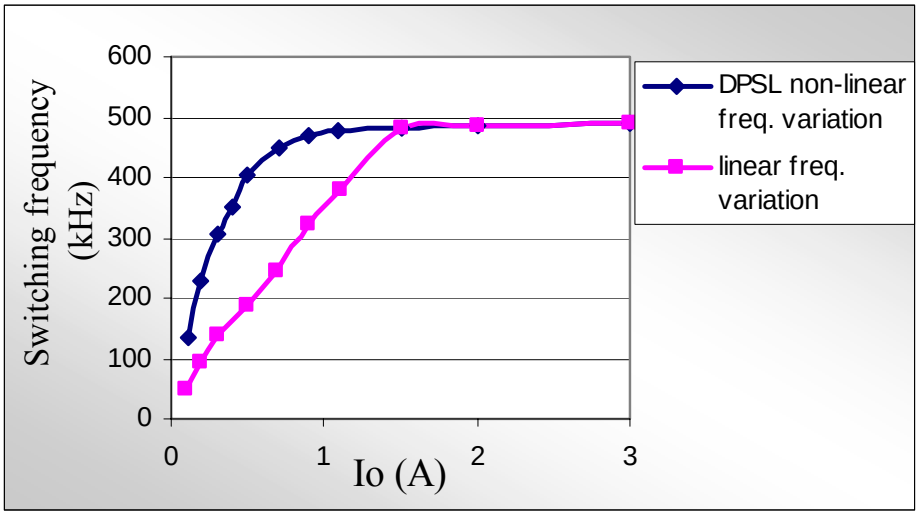


Fig.4. 22: *Switching frequency vs. load current for linear frequency variation control and the presented PSL control.*

4.7.5 Efficiency experimental results

Efficiency was measured from the experimental prototype for three cases: fixed frequency with MH, linear frequency variation, and presented PSL control. PSL assures good performance in terms of controlled output voltage ripple and improved dynamic response while improving conversion efficiency compared with fixed frequency operation with possible slight efficiency drop compared to linear frequency variation control that degrades steady state and dynamic performance. As shown in Fig. 4.23, the presented technique results in significantly improved efficiency at light loads compared with the fixed frequency case, with lower and well controlled voltage ripple, achieving the advantages of variable frequency and fixed frequency modes and eliminating their disadvantages.

Efficiency curves of Fig. 4.23 show high agreement with the theoretical plot shown in Fig.4.10. It may be advantageous to note again that in Fig. 4.23 the DPSL output voltage ripple in DCM was strictly limited to be equal to the CCM ripple. If, for example, twice the CCM ripple is allowed in DCM, the efficiency at light loads will be further improved.

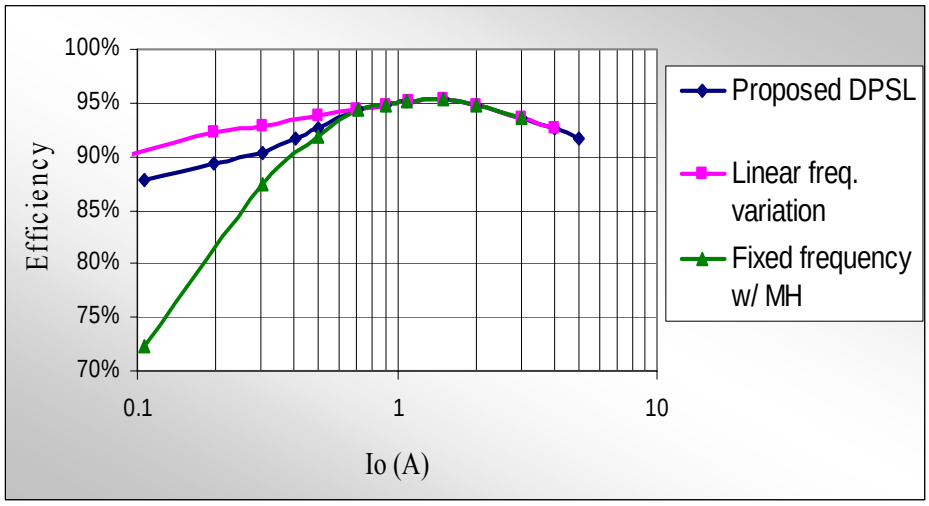


Fig.4. 23: Efficiency comparison between DPSL and the other techniques

Figure 4.24 shows DPSL efficiency for different input voltages. It must be noted that because the input voltage is forwarded to the VCO as discussed earlier, switching frequency was almost fixed while changing the input voltage.

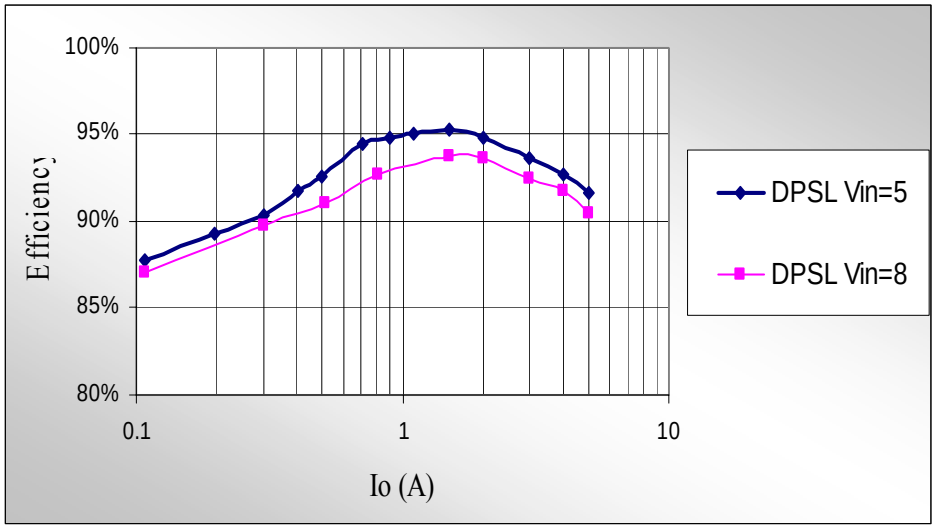


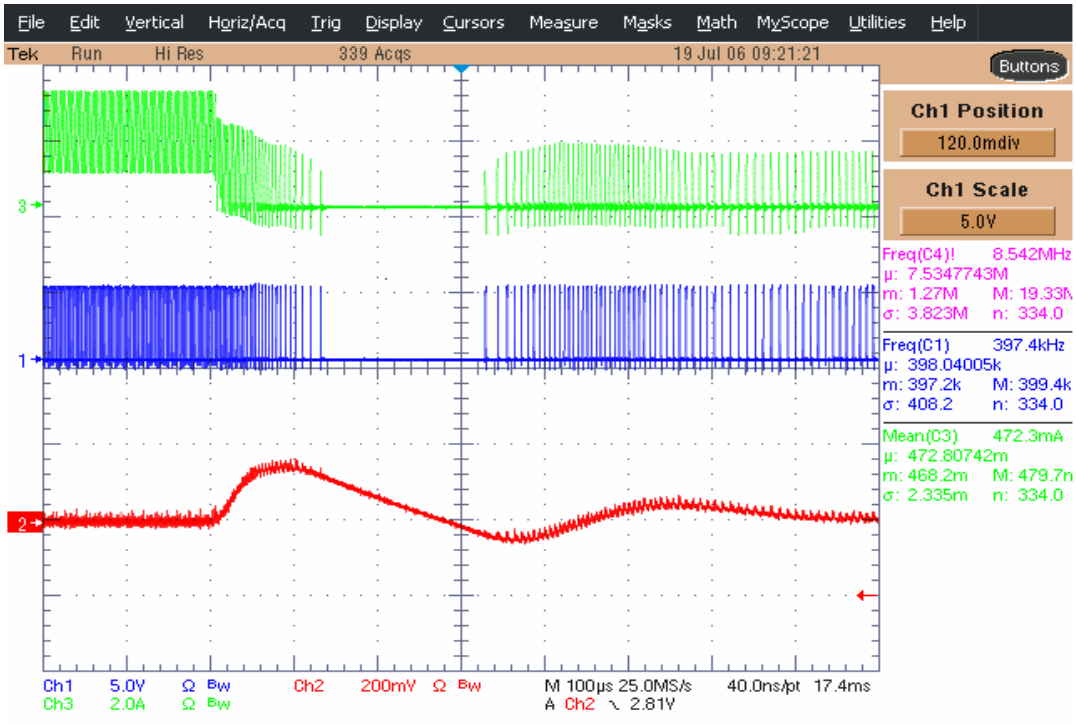
Fig.4. 24: DPSL efficiency for different input voltages

4.7.6 Transient response experimental results

The PSL method results in operating at higher switching frequency because of the peak inductor current tracking, especially at the load region where the load transitions from CCM to DCM and vise versa (0.6A~1A in the example of this paper). This fact alone suggests that there is a potential of improved dynamic response using the PSL method compared with the conventional linear variable frequency method. In addition, Fig. 4.17(a) shows an added technique to the PSL (compared with Fig. 4.11(b)) that further improves the dynamic response.

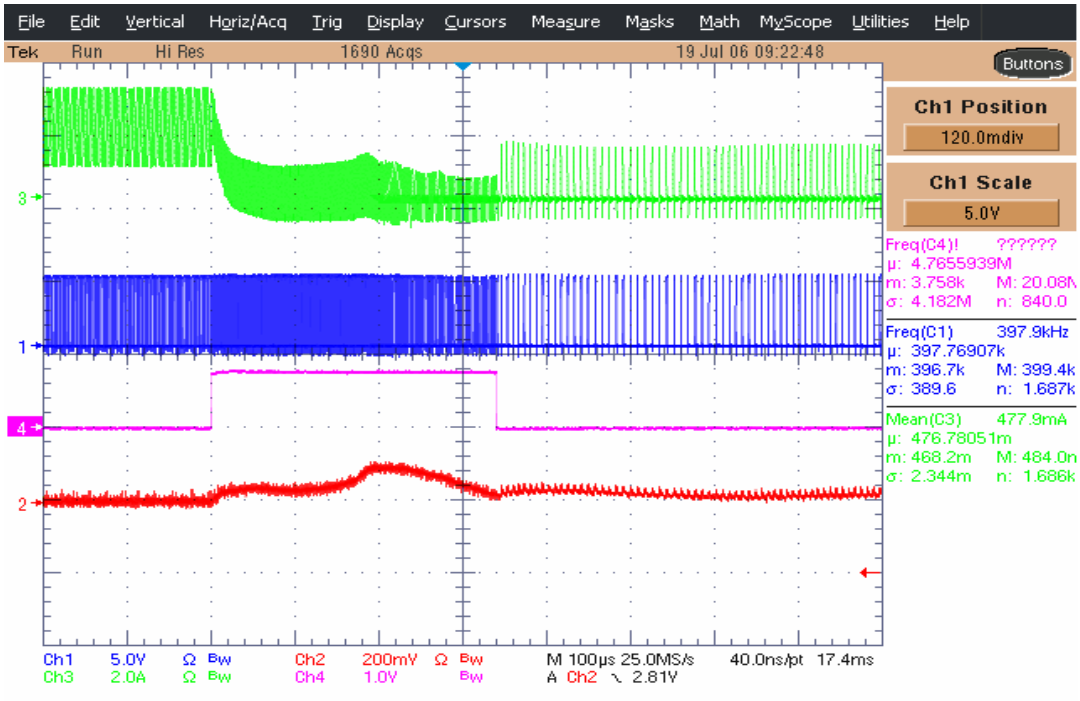
Figure 4.25 shows waveforms for load step down transient before and after applying the transient improvement method. Figure 4.25(a) clearly shows that switching was reduced during transient and overshoot was 150mV. Conversely, Fig. 4.25(b) shows how the transient improvement

method of Fig. 4.17 forces the frequency to increase during transient to speed up the response in order to reduce the overshoot to 80mV and to reduce the settling time.



(a)

Waveforms from top to bottom: inductor current, lower FET's gate-source voltage (Vgs), and output voltage



(b)

Waveforms from top to bottom: Inductors current, lower FET's gate-source voltage (Vgs), signal commanding VCO to increase switching frequency, and output voltage

Fig.4. 25: (a) Load step down transient (2A-0.1A) without applying transient improvement method. (b) Load step down transient (2A-0.1A) with applying transient improvement method

4.7.7 Closed loop Bode-Plots

Figure 4.26 shows the closed loop bode-plots of the PSL VR; it shows that magnitude crosses the zero-dB point at a cross-over frequency of 76 kHz (~15% of switching frequency) and the phase

margin is 36 degrees. This high control loop bandwidth improves transient response while maintaining the stability of the converter.

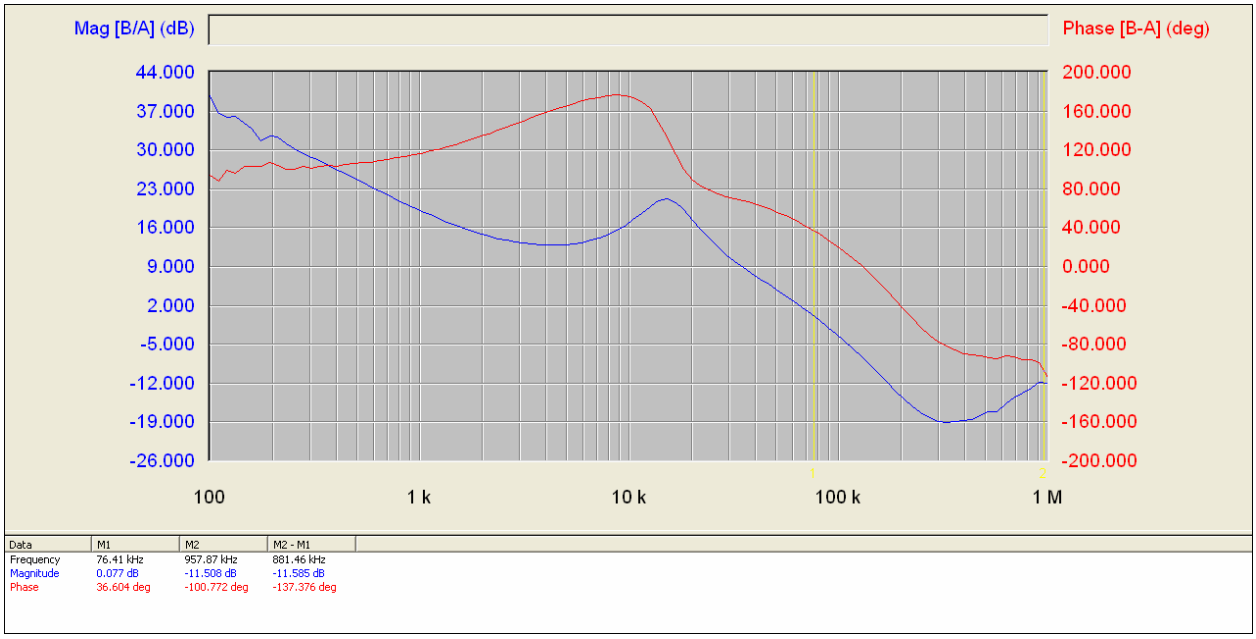


Fig.4. 26: Closed loop Bode-plots of the PSL VR

Figure 4.27 shows a picture of the prototype that was used to verify the presented PSL concept and to obtain the experimental results presented above.

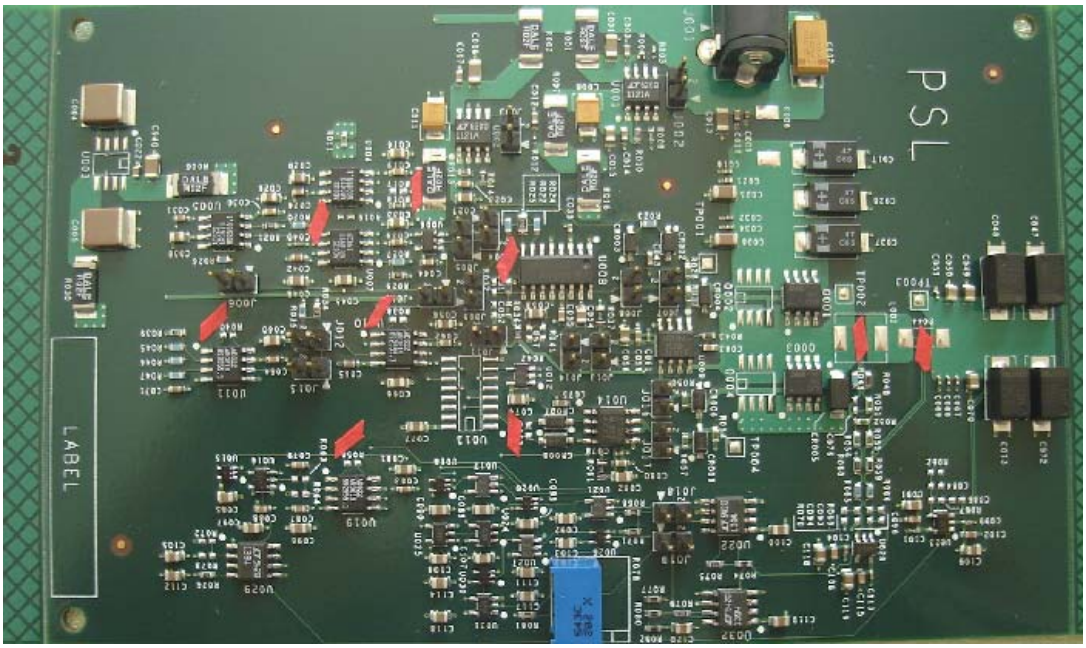


Fig.4. 27: Picture of the experimental prototype

4.8 Conclusion

Analyses and design of VR efficiency and performance considering light load conditions were discussed. A review of several techniques along with their power loss analyses curves for a design example was presented. A load adaptive control scheme with non-linear variable frequency and peak current tracking, namely Pulse-Sliding - PSL, was presented. It was demonstrated that with the PSL scheme, VR efficiency under a light load can be improved while maintaining controlled steady-state ripple and improving dynamic performance. Moreover, the presented method achieves higher efficiency and better performance with much less output capacitance, which reduces size and cost. Concept, analyses results, and experimental verification were presented and discussed. The theoretical and experimental results showed that

with non-linear variable switching frequency of the proposed PSL, conversion efficiency is improved, steady state and dynamic performance are improved, and required output capacitance reduction is achieved. Advantages from both variable frequency and fixed frequency controls are achieved and their disadvantages are eliminated with the presented controller.

The PSL controller provides more flexibility and dynamics to the operation of battery powered voltage regulators. The main advantages are to extend the battery life of mobile applications by improving light load efficiency, and at the same time to maintain controlled steady state and dynamic performances by reducing frequency at light load in a non-linear manner. It must be noted that the additional components and logic gates that were shown in the PSL controller (Fig. 4.11) can be integrated, which means that no area or cost will be compromised.

The drawback of the PSL controller is the additional design complexity of the control and the power stage. The latches and logic gates propagation delays must be taken into consideration. Otherwise, the voltage regulator will not achieve the optimized efficiency, and such delays might cause an overlap between the high side and low side switches in the power stage, which causes a short circuit.

CHAPTER 5: ANALYSES AND DESIGN OF ADAPTIVE FET MODULATION FOR VOLTAGE REGULATOR EFFICIENCY IMPROVEMENT

A conventional design of a buck regulator considers a specific range of load current, with no concern of lower or higher load ranges. Applications such as battery powered portable devices concern high efficiency at all load ranges and especially at the light load range since they operate in that range for most of the time [17, 18]. Other applications that mostly concern thermal issues consider achieving higher efficiency at higher load currents in order to lower the dissipated watts inside the regulator, therefore, lowering the generated heat [20].

Presented is a load adaptive voltage regulator that achieves high efficiency extended to light and heavy load regions. The presented method is named "Adaptive FET Modulation" (AFM) since multiple FETs with different specifications are paralleled such that the number of driven FETs and their respective gate driving voltage are adaptive to load current. The capability of adaptive modulation of FETs' parasitic charges and resistances along with adaptive gate driving voltage allows for the best FET optimization over a wide load range. AFM operates at a fixed switching frequency for almost the whole load range; therefore, it has no influence on the conventional buck operation and its dynamic performance and is simple to implement.

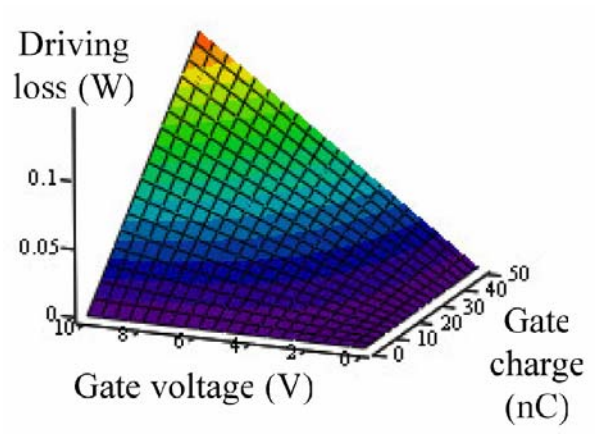
5.1 Concept of AFM

A large portion of losses in voltage regulators is dominated by FET's parasitics. One major parasitic is a FET's gate input capacitance [43]. A certain amount of charge *(Qg)* is required to charge that gate capacitance in order for the FET to turn on. Since $Qg=C*V$, it is clear that in order to drive FETs with higher voltages, more driving charges are required and more driving power is lost. This power loss can be expressed as $P_{driving}=Vg*Qg*f$. A surface plot of this driving loss as a function of gate voltage and gate charge for a given fixed frequency is shown in Fig. 5.1(a). Figure 5.1(b) shows a typical plot of gate charge versus gate voltage for an FET [25, 43]. It is clear from Fig. 5.1(a) that in order to reduce driving loss, FETs with a lower gate charge are preferred and gate drive voltage should be reduced. It is also clear from Fig. 5.1(b) that gate charge has a direct relationship with the gate voltage. Therefore, it can be concluded that driving loss for a given FET is related to the square of gate voltage, or $P_{driving}= Ci*Vg^2*f$, where *Ci* is the gate input capacitance. Figure 5.1(c) shows a surface plot of driving loss as a function of gate voltage and gate input capacitance for a given fixed frequency; it also shows the relation between driving loss and the square of the gate voltage. So for a given FET, if gate voltage is cut to half, its driving loss will be reduced to 25%.

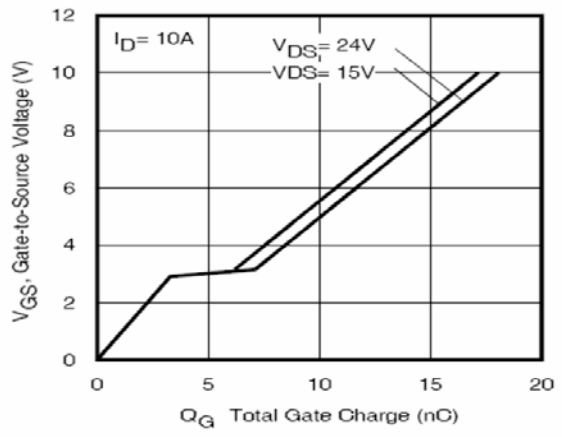
Based on the above discussion, and since driving loss at light load is dominant [43], it is preferred to apply FETs with small gate charges in that region. And for a certain selected FET, reducing gate voltage will further reduce the driving loss.

Another major FET's parasitic is the drain-source resistance *(Rds)*; this causes the FET's conduction loss. Conduction loss in an FET can be expressed as $P_{cond}=Irms^2*Rds$. Figure 5.2(a) shows a surface plot of conduction losses of an FET as a function of the FET's rms current and resistance, and Fig. 5.2(b) show a typical plot of an FET's resistance as a function of the gate voltage [25]. It is clear from Fig. 5.2(a) that in order to reduce conduction loss, it is preferred to apply FETs with small resistance value; it is also clear from Fig. 5.2(b) that an FET's resistance is inversely related to the gate voltage. Therefore, for a certain selected FET, its resistance can be further reduced by driving the gate with higher voltage.

Based on the above discussion, and since conduction losses at heavy load are dominant, it is preferred to apply FETs with small resistance in that region. And for a certain selected FET, increasing gate voltage will further reduce the FET's resistance, and therefore, reduce its conduction loss.



(a)



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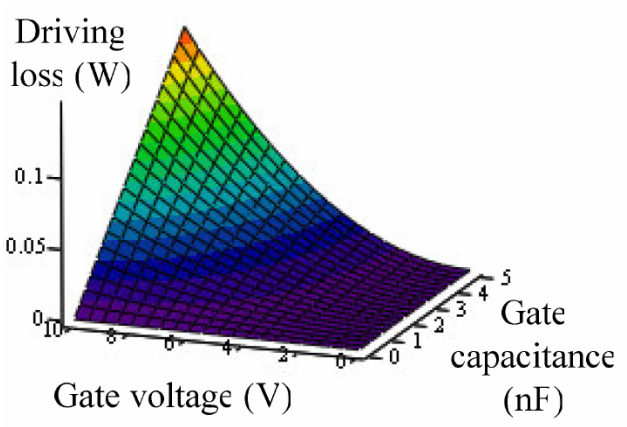
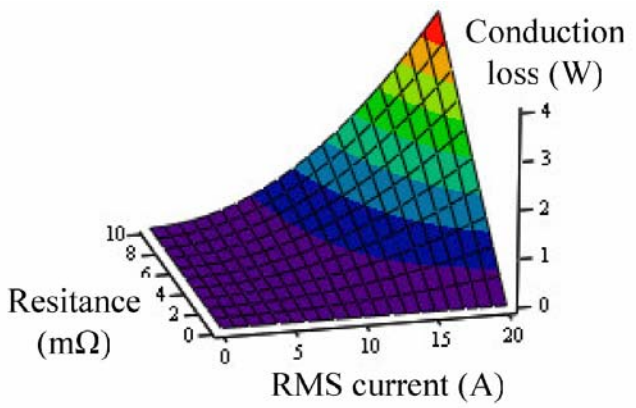
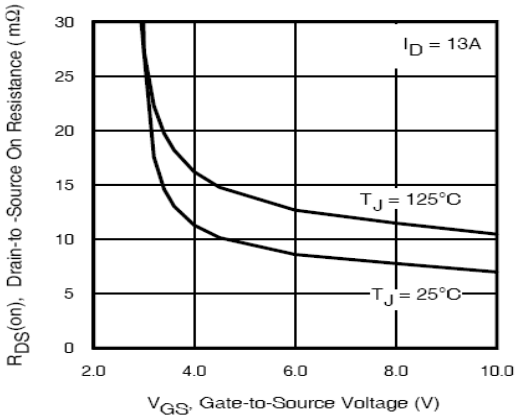


(c)

Fig. 5. 1: (a) Driving loss vs. Gate voltage vs. Gate charge. (b) Gate charge vs. Gate voltage. c) Driving loss vs. Gate voltage vs. Gate capacitance



(a)



(b)

Fig. 5. 2: (a) Conduction loss vs. RMS current vs. FET resistance (b) FET resistance vs. gate voltage.

Unfortunately, there is no single FET that can provide low *Rds* (for low conduction loss) and low *Qg* (for low driving loss) at once; it is either low resistance *(Rds)* or low gate charge *(Qg)*. This

limitation is due to the Figure of Merit (FOM) of today's devices, which makes it difficult for a conventional voltage regulator design to achieve high efficiency at a wide range of load current. Figure 5.3 shows a bar type chart that includes several FETs with different specifications [25, 36-42]; it clearly shows that FETs with high resistance have low gate charge, and vice versa.

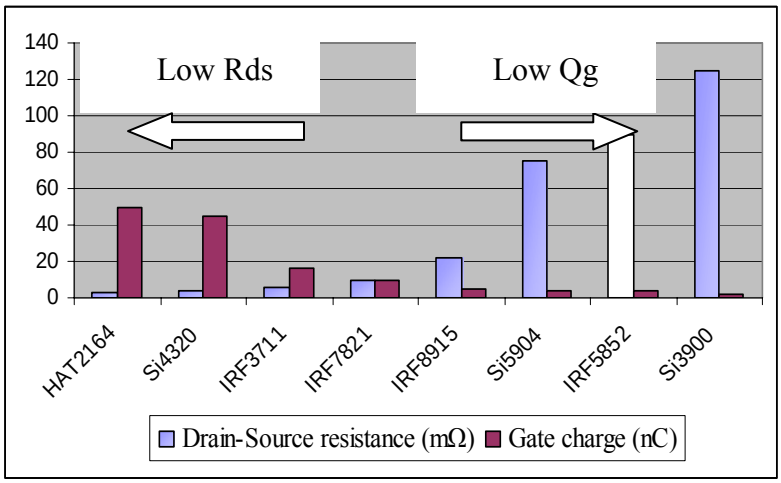


Fig. 5. 3: *Several FETs' gate charge and resistance specifications*

Discussion in this paper will be referring to FETs with low *Rds* as big FETs, since they are more capable to carry high current. FET's with high *Rds* will be referred to as small FETs. And FETs with moderate values of *Rds* and *Qg* will be referred to as medium FET. Discussion also will be based on dividing load range into three regions: light load, medium load, and heavy load regions.

The concept of AFM is to parallel multi FETs with different specifications; the number of driven FETs and their gate drive voltage is adaptive to load current.

- At light load condition, only small FETs are driven, and their gate voltage is low. Consequently, the voltage regulator operates under light load conditions with optimal small FETs specifications, as shown in Fig. 5.4.

- At mid load condition, medium FETs are driven with medium gate voltage to take most of the current off the small FETs. As a result, the voltage regulator operates under mid load condition with optimal equivalent FETs specifications that result from parallel small FETs and medium FETs, as shown in Fig. 5.4.

- At heavy load conditions, big FETs are driven with high gate voltage to take most of the current off the small and medium FETs. Consequently, the voltage regulator operates under heavy load condition with optimal equivalent FETs specifications that result from parallel small, medium, and big FETs, as shown in Fig. 5.4.

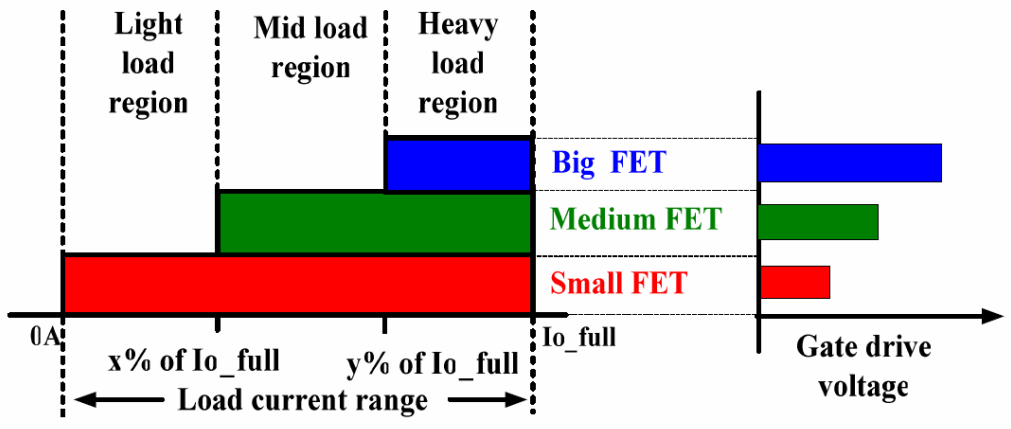


Fig. 5. 4: *Operational concept of proposed AFM*

5.2 Loss analyses

Analyses are based on the following design specifications, for example and not for limitation:

$V_{in} = 8V$, $V_o = 1.5V$, $L_o = 3.3 \ \mu H$, $C_o = 670\,\mu F$, and $f_{sw} = 300\,kHz$.

Specifications of FETs used in the analyses are shown in Table 5.1.

Table 5. 1: FETs specifications

	FET #	Rds (mΩ)	Qg (nQ)	Gate drive voltage
Small FETs	Si3900	125	1.2@Vgs=3V	3V
Medium FETs	IRF7821	10	10@Vgs=5V	5V
Big FETs	HAT2165	2.5	50@Vgs=7V	7V

As discussed earlier, it is possible to optimize a voltage regulator design for a limited range of load current. The proposed method aims to achieve high design optimization for a wider range by analyzing power losses in different regions of load current. Figure 5.5 shows an example of power losses normalized by the input power for a conventional design; it is clear that driving losses dominate the light load and conduction losses dominate the heavy load.

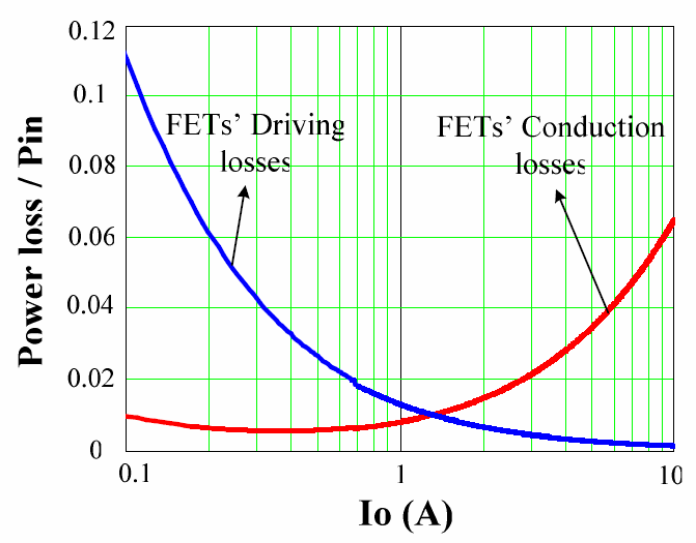


Fig. 5. 5: *Power losses normalized by the input power for a conventional design*

Figure 5.6 explains how the equivalent FETs' specifications change when changing the number of active FETS. Turning on and off parallel FETs is a way to modulate the equivalent resistance and gate charge. Note that the equivalent output charge (Qoss), equivalent switch charge (Qsw), and reverse recovery (Qrr) do not modulate by changing the number of active FETs, since FETs are connected in parallel, regardless of being driven or not. Therefore, proposed AFM does not modulate FETs' parasitic charges that cause switching losses. This means that small FETs will have switching losses caused by the sum of the three FETs' (small, medium, and big) parasitic charges, which limit the efficiency improvement at very light loads. But such effect by losses can be reduced by applying the mode hoping technique (MH), where at light load the converter operates in DCM. MH not only reduces the conduction loss that is caused by current ripple, but it also eliminates reverse recovery loss when operating in DCM. Hence, losses of the small FET at light load are reduced. Moreover, for further efficiency improvement at very light load,

switching frequency can be stepped down to a lower value in order to reduce frequency related losses. It must be noted that frequency reduction in this case is only done at very light load and frequency is stepped down to a constant value; which is different from frequency variation or pulse skipping techniques. It does not affect dynamic performance, since the voltage regulator operates at the nominal constant frequency for over 95% of the load range.

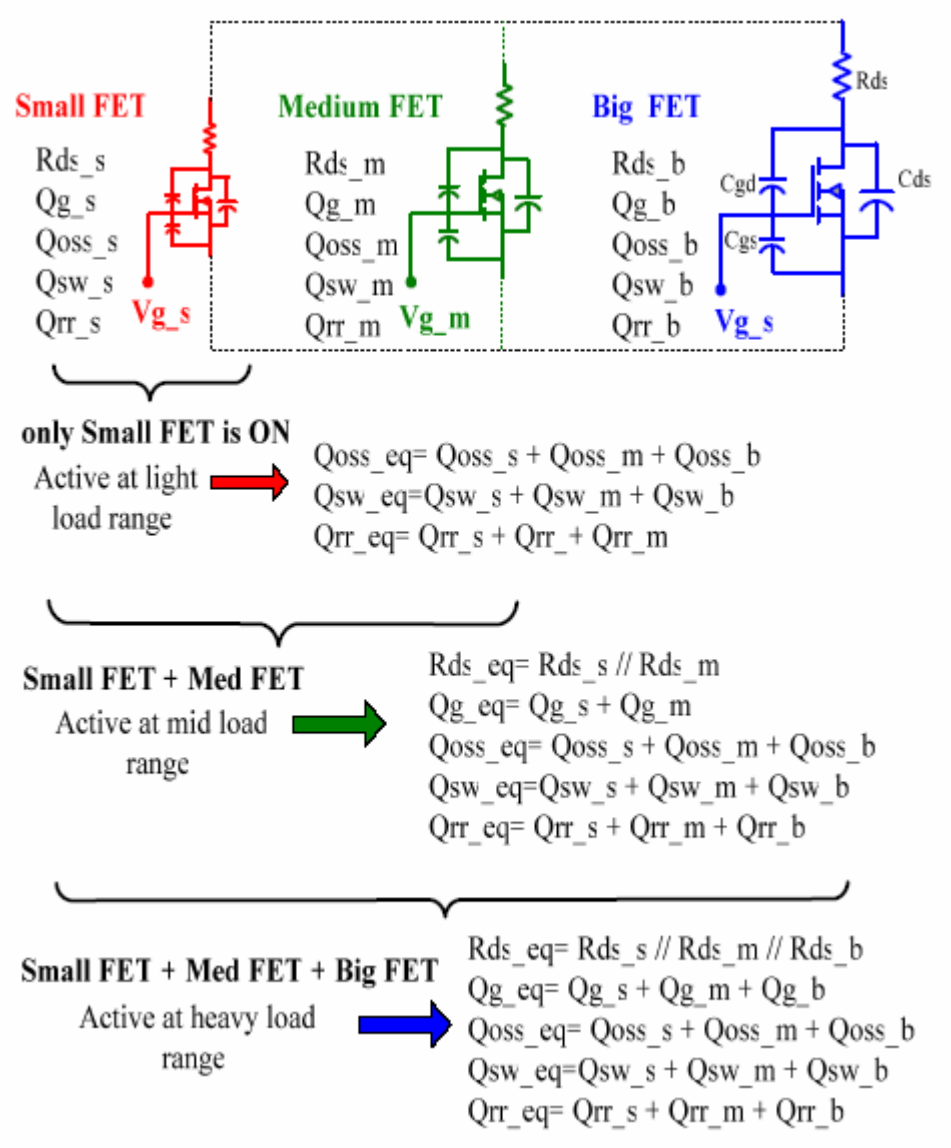
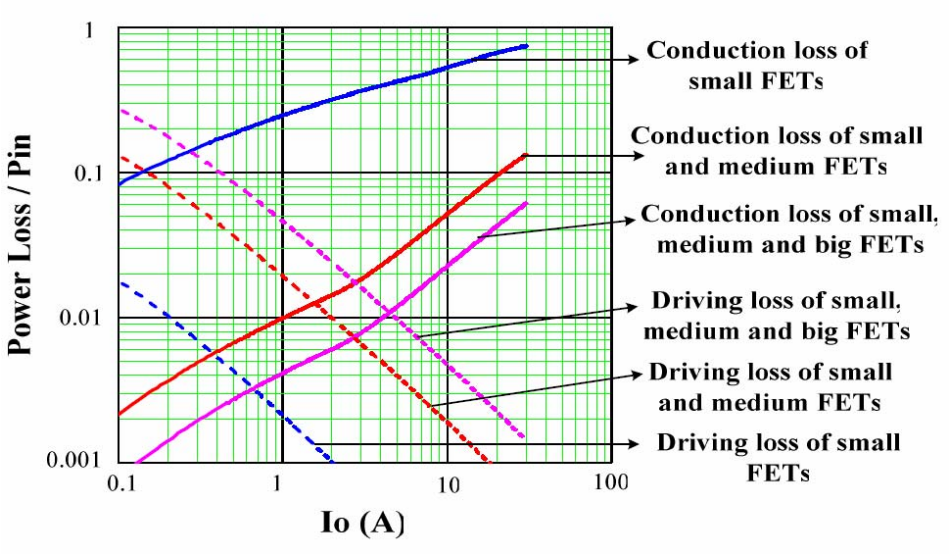
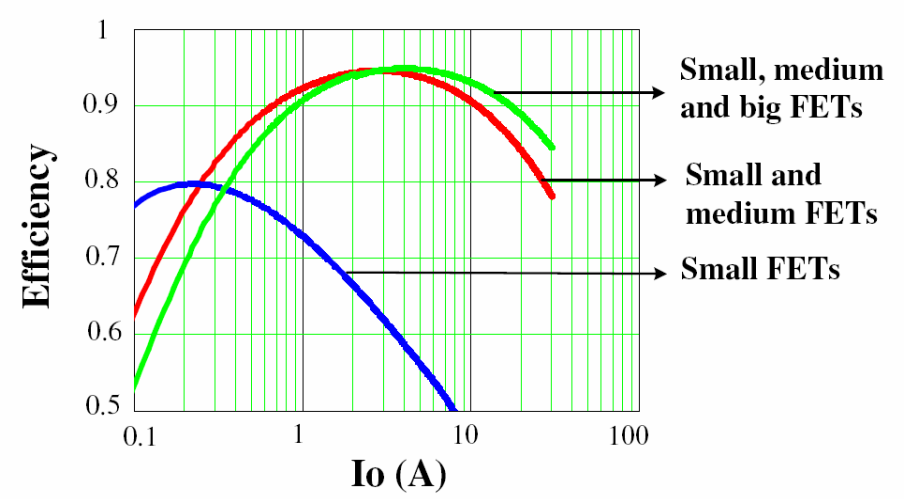


Fig. 5. 6: *Equivalent parallel FETs' specifications*

The proposed converter has different FETs with different specifications, and each combination of driven parallel FETs has different power loss curves. Figure 5.7(a) shows a plot of conduction and driving losses normalized to input power for the three cases of: (1) only small FETs are on, (2) small and medium FETs are on, and (3) small, medium, and big FETs are on. It is clear that small FETs consume the least driving power. And when small, medium, and big FETs are all driven, their combinations have the least conduction losses. Figure 5.7(b) shows the calculated efficiency curves for the three cases. It is obvious that each curve can achieve the best efficiency in some load current range, and the envelop curve of the three curves would be the proposed AFM efficiency curve.



(a)



(b)

Fig. 5. 7: (a) Conduction and driving losses normalized to input power

(b) Calculated efficiency curves

5.3 AFM implementation

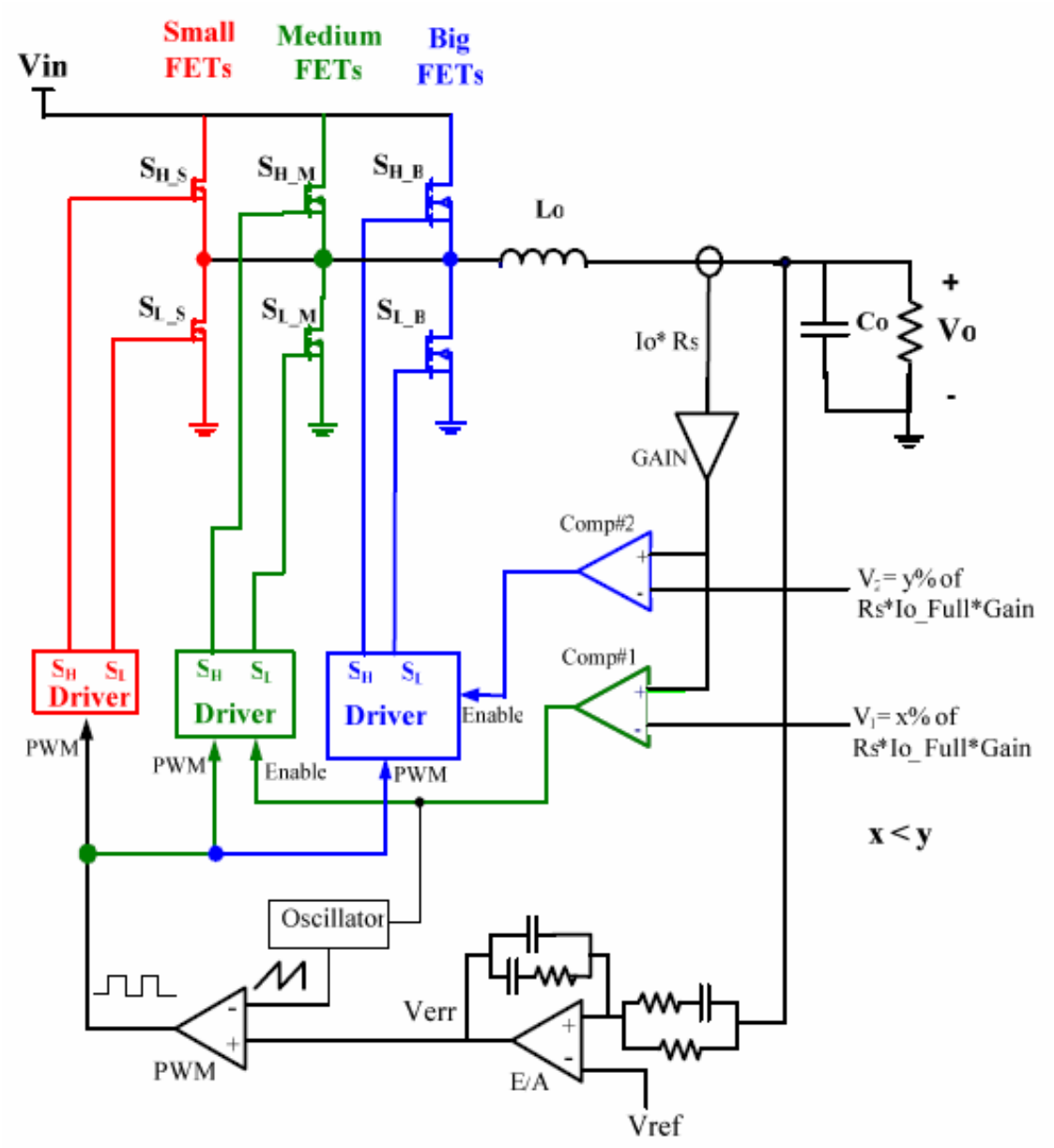
The proposed AFM achieves good performance for a wide load current range, and its simple design makes it easy to implement. Figure 5.8(a) shows the basic implementation of the proposed method. Basically, it is a conventional buck with multiple FETs in parallel with different specifications, the inductor current is sensed, the voltage across the sense resistor is amplified and compared to two predetermined thresholds, V1 and V2. Each threshold is a voltage value representing a certain percentage of full load current. The V1 threshold sets the current boundary between light load and mid load regions, and V2 threshold sets the current boundary between mid load and heavy load regions.

Figure 5.8(b) illustrates the operational waveforms of the proposed converter assuming that the load current is increasing from zero to full load. This operation will be described in the following paragraphs:

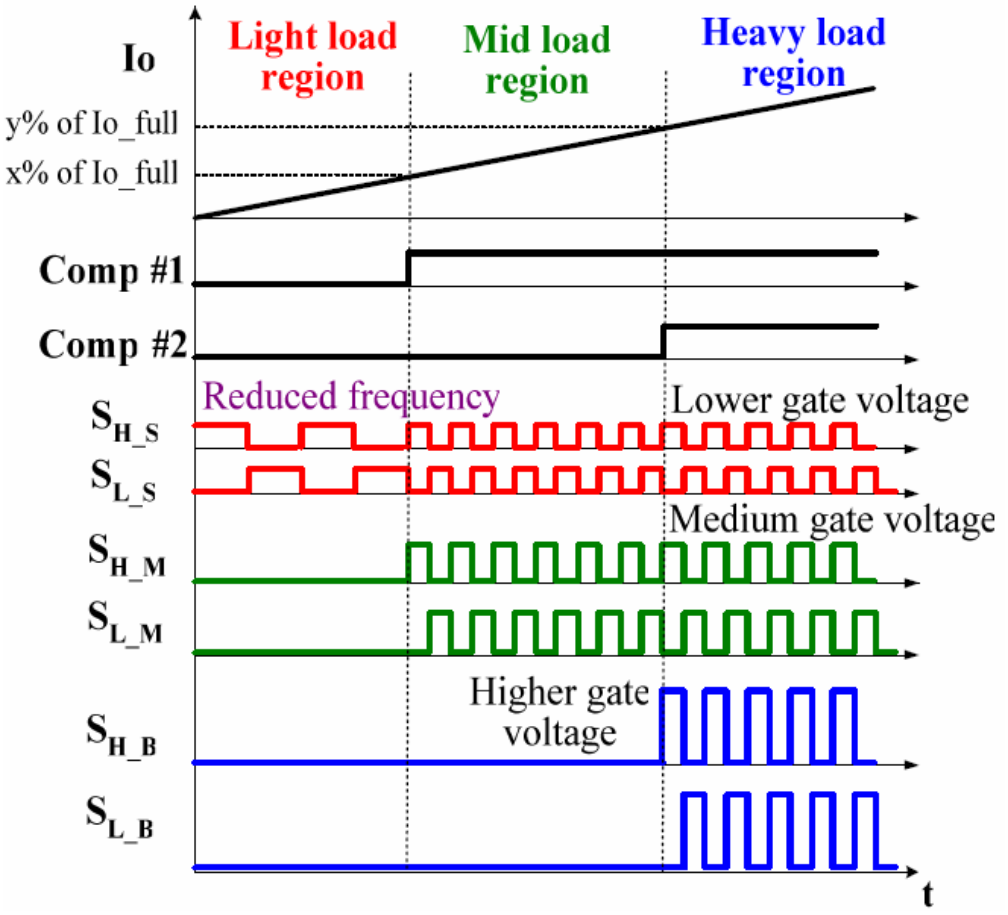
- Under light load conditions, the sensed current voltage signal is below threshold V1, both Comp #1 and Comp #2 outputs are low. Therefore, only small FETs are driven and their gate voltage is low. As a result, the voltage regulator operates under light load condition with optimized performance. As for a further efficiency improvement, the switching frequency is stepped down at light load. Frequency reduction at low current offers a good contribution in minimizing switching losses.

- At mid load condition, the sensed current voltage will be higher than V1 threshold but lower than V2; Comp #1 will output high and Comp #2 will output low. Therefore, medium FETs will become involved, and their gate voltage will increase; hence, the voltage regulator operates under mid load condition with optimized equivalent FETs specifications that result from parallel small FETs and medium FETs.

- At heavy load conditions, the sensed current voltage will be higher than V1 and V2, and Comp #1 and Comp #2 will output high. The big FETs will also be utilized, and their gate voltage is further increased so that the voltage regulator operates under the heavy load condition with optimized equivalent FETs specifications that result from parallel small, medium, and big FETs.


Vin
Small FETs
Medium FETs
Big FETs
SH_S
SH_M
SH_B
SL_S
SL_M
SL_B
Lo
Co
+
Vo
-
Io* Rs
GAIN
Comp#2
Comp#1
Vz= y% of Rs*Io_Full*Gain
Vl= x% of Rs*Io_Full*Gain
x < y
SH SL Driver
Enable
PWM
Oscillator
Verr
E/A
Vref

(a)



(b)

Fig. 5. 8: (a) basic implementation of proposed AFM.

(b) Operational waveforms of the proposed AFM.

5.4 Design considerations

Voltage regulators usually have dynamic load with fast transient. One important design issue for the proposed AFM is to prevent over loading the small FETs in case of step up load transient, especially since small FETs tend to have lower current ratings.

Because of the current sense delay and the driver delay, there is a time delay between the time at which the inductor current is equal to the current threshold and the time at which the medium FETs are driven. During this time delay, the inductor current will ramp up to a value that is higher than the threshold current. If this new current value is higher than the small FET's current rating, then there is a problem. The difference between the threshold current and the inductor current at the time when medium FETs are driven depends on the time delay, input and output voltages, and the inductor value. Design must assure that inductor current does not exceed the small FETs current rating before medium FETs are driven. See Fig. 5.9.

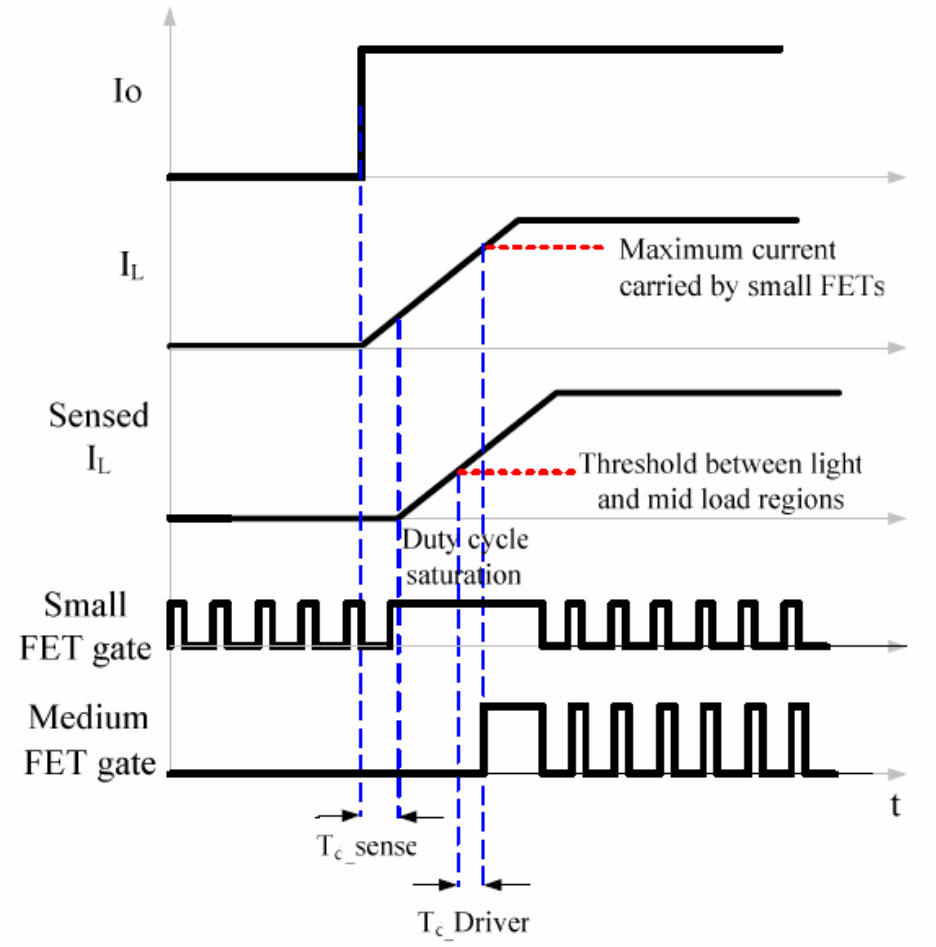


Fig. 5. 9: *Safe operation design consideration at step up load*

In case of typical inductor values, the inductor current will ramp to a slightly higher current than the threshold current during the time delay period, so that medium FETs will be driven before the small FETs gets over loaded. See Fig. 5.10.

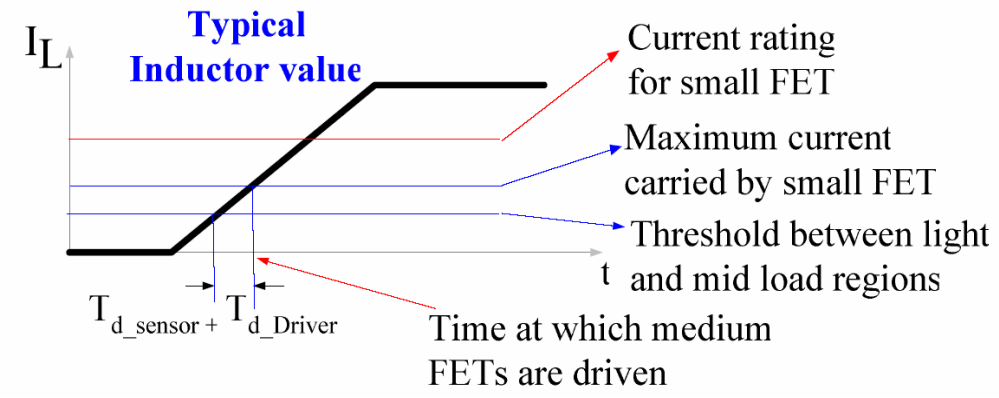


Fig. 5. 10: Typical inductor value case

However, in case of very small inductor values, the inductor current will ramp to a much higher current than the threshold current during the time delay period, so that medium FETs will be driven at a current that is much higher than the small FETs' current rating, and small FETs gets over loaded. See Fig. 5.11.

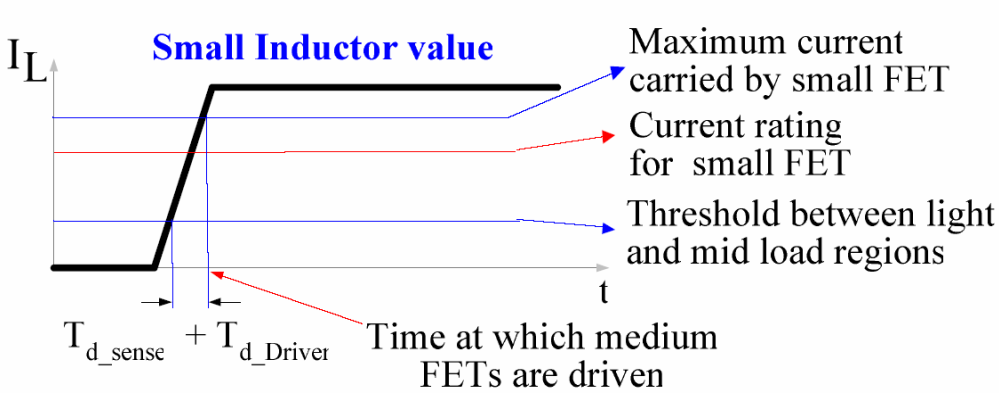


Fig. 5. 11: Small inductor value case

Analyses of such issues consider parameters such as: inductor value, current sense and driver delays, and input and output voltages. Based on these parameters, it is possible to assess the

maximum current flowing through the small FETs before the medium FETs become involved and carry most of the current. For safe operation, the design must take into account the worst case scenario, which is: load current is at the boundary between light and mid load regions before transient occurs, and load transient is assumed to cause duty cycle saturation. Based on the discussion above, the maximum current that flows throughout the small FETs can be derived as shown in Eq. 5.1.

$$I_{FET,S\_MAX} = \frac{V_{in} - V_o}{L} t_{DELAY,TOTAL} + I_{BOUNDARY} \qquad Eq.5.1$$

Based on Eq. 5.1, it is possible to find the minimum inductance value that assures safe operation, as shown in Eq. 5.2.

$$L_{\min} = \frac{V_{in} - V_o}{I_{SMALL\ FET\ RATING} - I_{BOUNDARY}} \ t_{DELAY,\ TOTAL} \qquad Eq.5.2$$

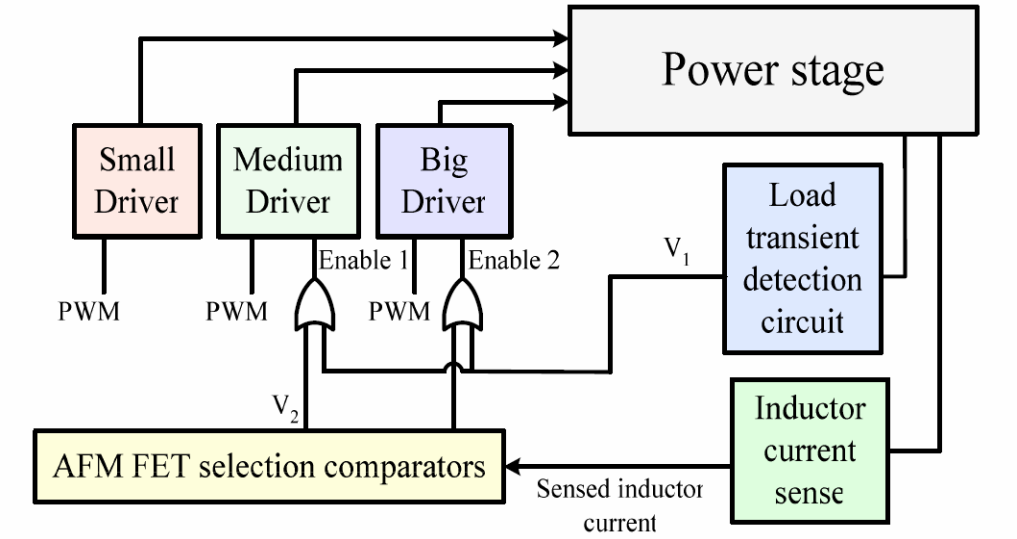
- Solution for cases with small inductor value:

As shown in Fig. 5.11, operation safety becomes critical at smaller inductor values. Hence, a solution must be applied to prevent such risky situations. The following is a solution for this issue.

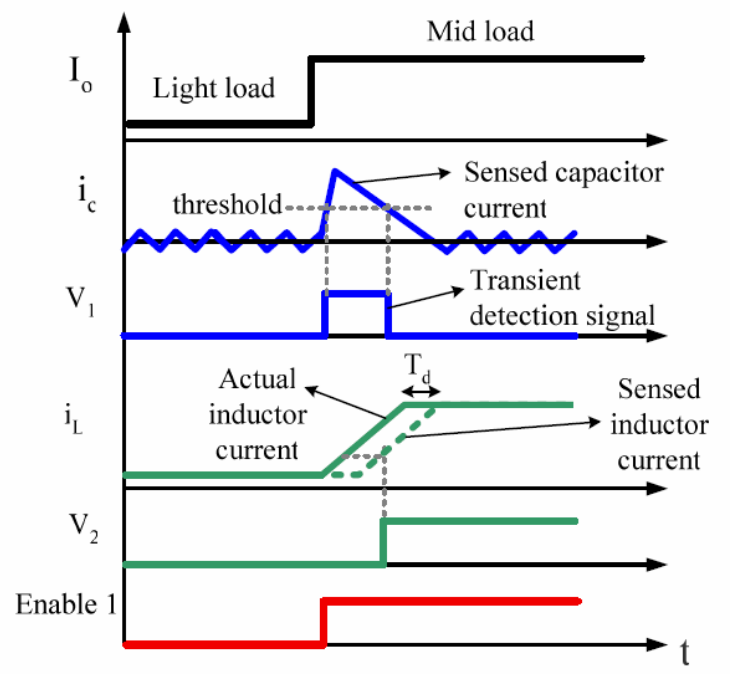
Load transient can be detected either by sensing the output capacitor current by differentiating its voltage, or simply by detecting the output voltage transient spike. A transient detection signal can be used to turn on all FETs during the transient times. When transient is completed, the state of medium and big FETs is decided by steady state inductor current. In other words, the state of

medium and big FETs is decided by inductor current in steady state, and by the transient detection signal during transient to assure safe operation.

Figure 5.12 (a) shows the basic implementation for the solution discussed above. Basically, during load step up, the OR gate output enables the driver when a transient is detected by the transient detection circuit; this covers the time delay period caused by the current sense in order to assure safe operation. After transient is completed, the driver enabled signal is determined by the sensed inductor current. Figure 5.12 (b) shows waveforms demonstrating an example of load step up from light to mid load using capacitor current method to detect load transient. It shows how V1 signal contributes to enabling the driver during transient period, and how V2 signal contributes to enable the driver during steady state.



(a)



(b)

Fig. 5. 12: *(a) Implementation of the proposed safe operation circuit for low inductor value case*

(b) Waveforms of the proposed circuit

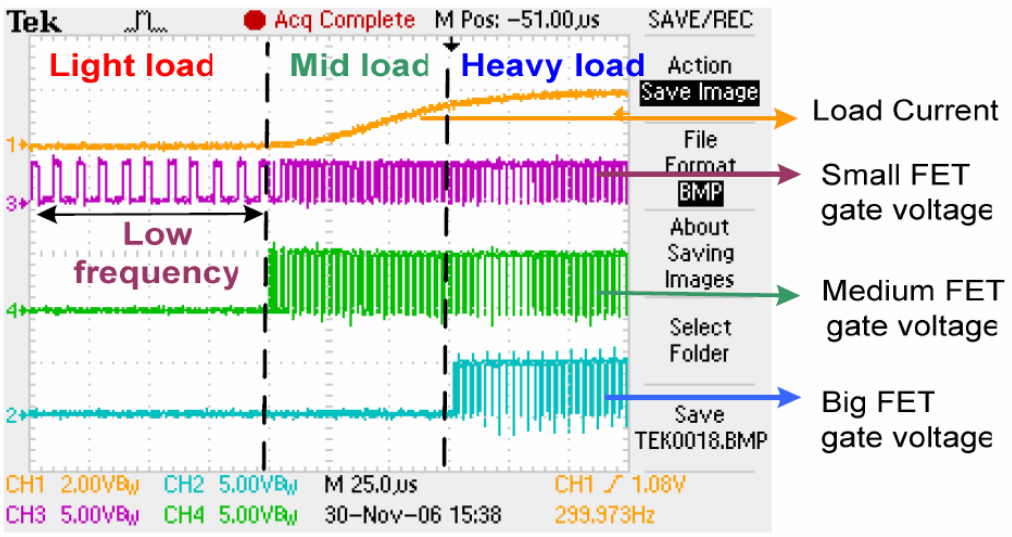
5.5 Experimental results

A prototype was built to validate the proposed concept. The Experiment is based on the following specifications: *Vin= 8 V, Vo= 1.5 V, fs= 300 kHz, L=3.3 uH, Si3900* as small FETs, *IRF7821* as medium FETs, and *HAT2165* as big FTEs. The light load region was defined to range from 0-450mA, the medium load region was defined to range from 450mA-3.5A, and heavy load was defined to range from 3.5A-10A.

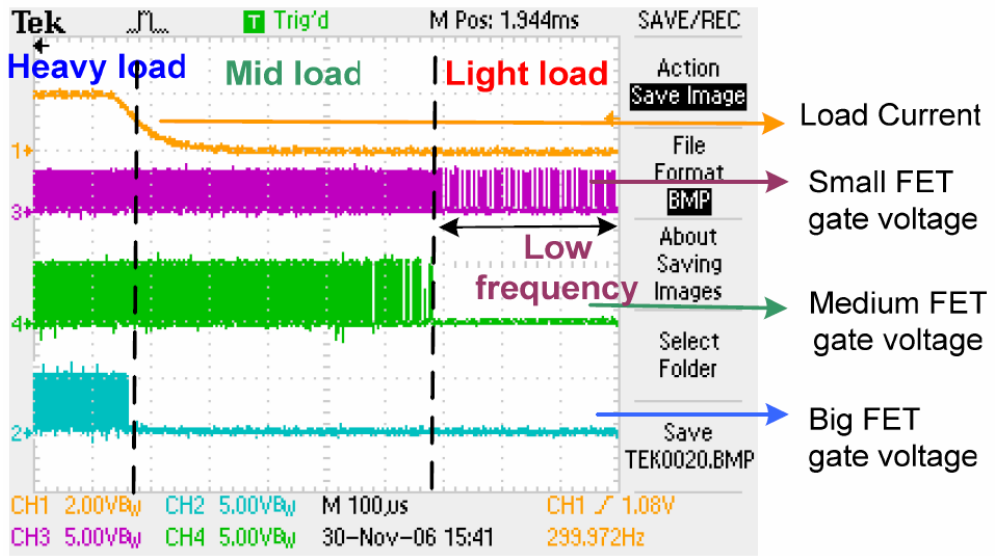
Figure 5.13(a) shows experimental waveforms as load step from light load region to mid load region to heavy load region (0-5A load step). These waveforms can be easily compared to Fig. 5.8(b) in section IV; it shows that at light load, only small FETs are driven and switching frequency is low (100kHz). As load current rises to reach the mid load region, medium FETs are driven with a higher gate voltage and switching frequency is increased to the nominal value (300kHz). As load current rises to reach the heavy load region, big FETs are driven and switching frequency is still fixed to the nominal value (300kHz).

Figure 5.13(b) shows experimental waveforms as load step from heavy load region to mid load region to light load region (5-0A load step). It shows the other side of the operation discussed above regarding Fig. 14(a).

Figure 5.13(c) shows experimental waveforms as load step up and down. It shows how FETs are driven based on load current.


Tek
Acq Complete
M Pos: -51.00µs
SAVE/REC
Light load
Mid load
Heavy load
Action
Save Image
Load Current
File Format
BMP
Small FET gate voltage
Low frequency
About Saving Images
Medium FET gate voltage
Select Folder
Save TEK0018.BMP
Big FET gate voltage
CH1 2.00V
CH2 5.00V
M 25.0µs
CH1 1.08V
CH3 5.00V
CH4 5.00V
30-Nov-06 15:38
299.973Hz

(a)


Tek
Trig'd
M Pos: 1.944ms
SAVE/REC
Heavy load
Mid load
Light load
Action
Save Image
Load Current
File Format
BMP
Small FET gate voltage
Low frequency
About Saving Images
Medium FET gate voltage
Select Folder
Save TEK0020.BMP
Big FET gate voltage
CH1 2.00V
CH2 5.00V
M 100µs
CH1 1.08V
CH3 5.00V
CH4 5.00V
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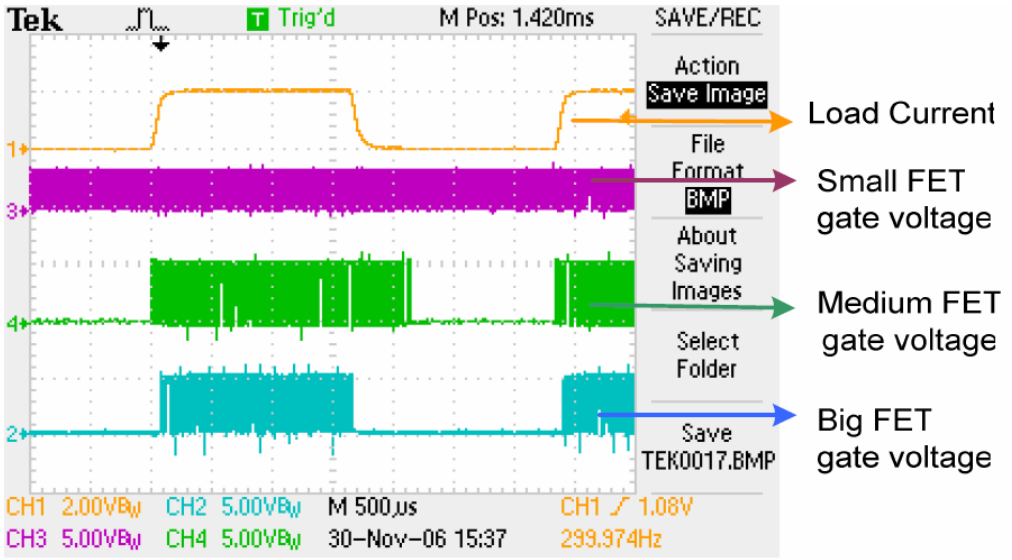
299.972Hz

(b)



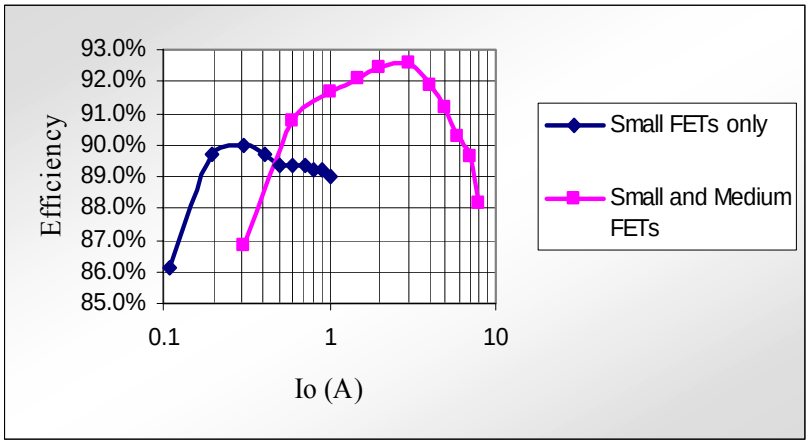
(c)

Fig. 5. 13: Experimental waveforms of the proposed AFM operation.

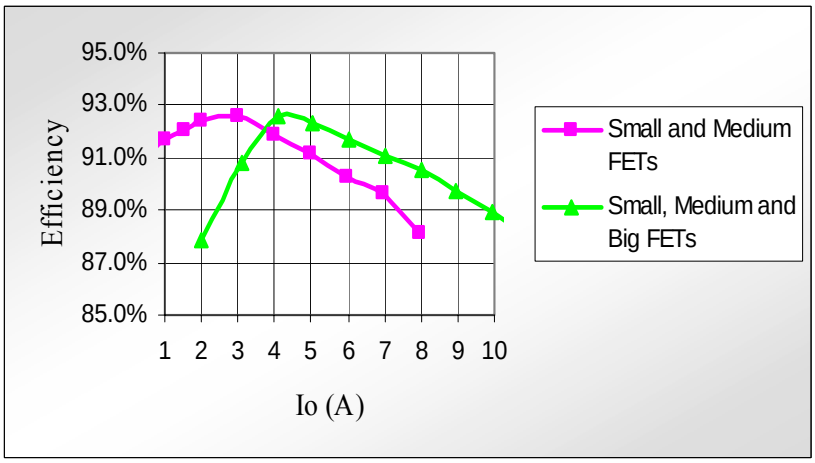
(a) 0-5A load step (b) 5-0A load step (c) 0-5-0A load step

Figure 5.14(a) shows the efficiency comparison when only small FETs are on and when small and medium FETs are on. The results show that small FETs have better performance under light load, and the combination of small and medium FETs have better performance at mid load. Figure 5.14(b) shows the efficiency comparison between small and medium FETs when they are on, and when small, medium, and big FETs are on. It is clear that the combination of small, medium, and big FETs have better performance at heavy load. The resulting maximum efficiency would be the envelopment of the three efficiency curves. Efficiency is shown in two separate plots for simplicity to illustrate the improvement in each load range. It must be noted that the proposed converter operates at a fixed switching frequency for a majority of the whole

load range so that dynamic performance will not be affected, and frequency is stepped down under only very light loads.



(a)



(b)

Fig. 5. 14: (a) Efficiency comparison between small and medium FETs.

(b) Efficiency comparison between medium and big FETs.

Figure 5.15 shows a picture of the prototype that was used to verify the proposed concept and to obtain the experimental results presented above.

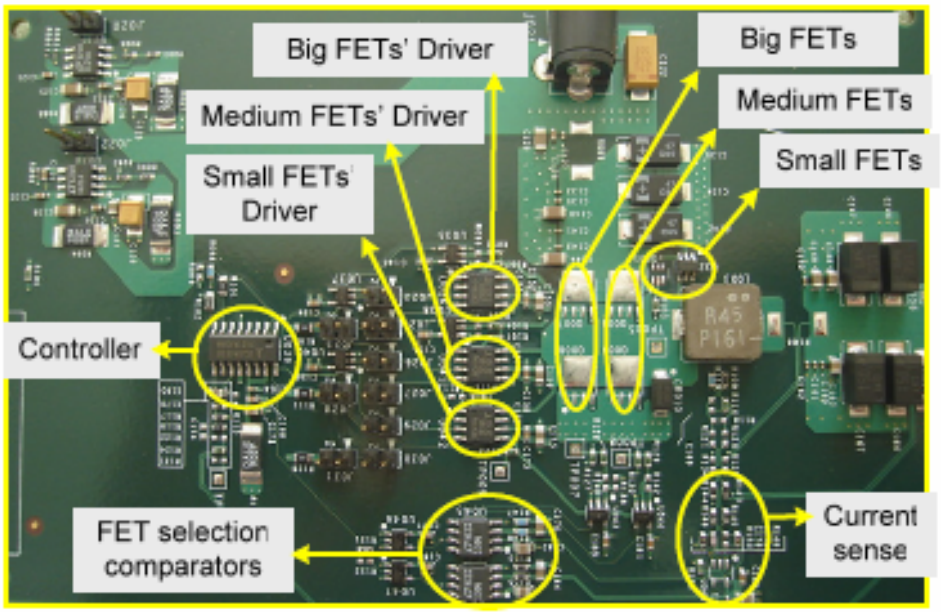


*Fig. 5. 15***:** *Picture of the experimental prototype*

5.6 Conclusion

A load adaptive voltage regulator that achieves high efficiency extended to light load and heavy load regions is presented. The AFM is capable of adaptive modulation of FETs' parasitic charges and resistances along with adaptive gate driving voltage in order to achieve the best FET optimization for a wide load range. The concept, design, analyses and experimental results of the AFM were presented.

The main advantage of the AFM is to extend the battery life of mobile applications by improving light load efficiency, and extend the high efficiency to heavy load regions to reduce the generated heat inside the converter. The AFM feature preferred over the PSL controller discussed in the previous chapter pertains to the heavy load conditions. Moreover, it operates at fixed frequency, which makes it simpler and its design much easier in comparison to the PSL. It should be noted that the multiple FETs and the multiple drivers are intended to be integrated in the real application. Therefore, cost and area will not be increased.

The drawback of the AFM converter is that its light load efficiency improvement is limited compared to the PSL controller because it only reduces driving losses at light load, while switching losses still degrade the efficiency since it operates at fixed switching frequency.

CHAPTER 6: DYNAMIC PWM RAMP SIGNAL TO IMPROVE LOAD TRANSIENT IN DCM AND MODE HOPING OPERATION

In case of load transient in CCM operation, the duty ratio is almost constant over the load current range; it slightly changes to compensate the extra losses and to keep output voltage regulation. While in DCM and Mode Hoping operation, duty ratio varies significantly in case of load transient. The control loop is required to update the compensation error signal; consequently, the duty ratio as load current varies. Since it takes a longer time for the compensator to reach the steady state in cases of large duty cycle variation (DCM operation), the output voltage deviation during load transient is drastically increased when operating in DCM compared to CCM operation. Presented is a control method that dynamically modulates the PWM ramp signal peak; this will modulate the PWM modulator gain to minimize the required error signal change during load transient, so that the compensator reaches steady state faster. Therefore, lower output voltage deviation during load transient can be achieved.

6.1 Principle of operation

Proposed is a new control method that dynamically modulates the PWM ramp signal peak, which will modulate the PWM modulator gain to minimize the required error signal change during load transient, so that the compensator reaches steady state faster. The PWM ramp signal peak is modulated with inverse relationship to the compensation error signal, since error signal in DCM is directly related to load current. The principle is to speed up the duty ratio required change during load transient with the help of the PWM ramp signal, and not by the compensator

error signal by itself. Figure 6.1 illustrates the operation during load transient for the conventional constant ramp signal peak and for the proposed dynamic ramp signal peak; it demonstrates how duty cycle can reach steady state faster when applying the proposed control method. As load steps up, the error signal increase causes the ramp signal peak to decrease; as a result, duty ratio can reach steady state with less error signal deviation and in shorter time. The opposite scenario occurs in case of load step down.

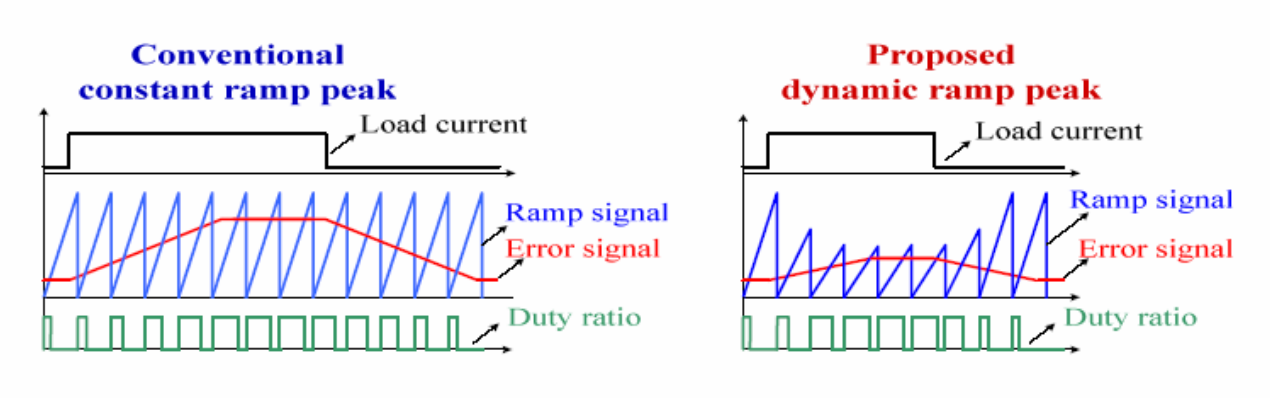


Fig. 6. 1: PWM for the conventional constant ramp signal peak and for the proposed dynamic ramp signal peak during load transient

6.2 Implementation

Figure 6.2 reveals the basic implementation of the proposed control method. Simply, the oscillator outputs a ramp signal with a peak proportional to its input ($V_p = \alpha \cdot V_1$). As shown in the figure, the V_1 voltage is obtained by the difference between a constant voltage (Vcc) and a voltage proportional to the error signal voltage (β*Verr). At light load, the error signal voltage is low; therefore, the V_1 voltage is high and the ramp signal peak (V_p) is high, and the PWM

modulator gain is low. As load current increases, the error signal voltage increases; consequently, the V_1 voltage decreases and the ramp signal peak (V_p) decreases, and the PWM modulator gain increases. The implementation of the oscillator is also shown in Fig. 6.2.

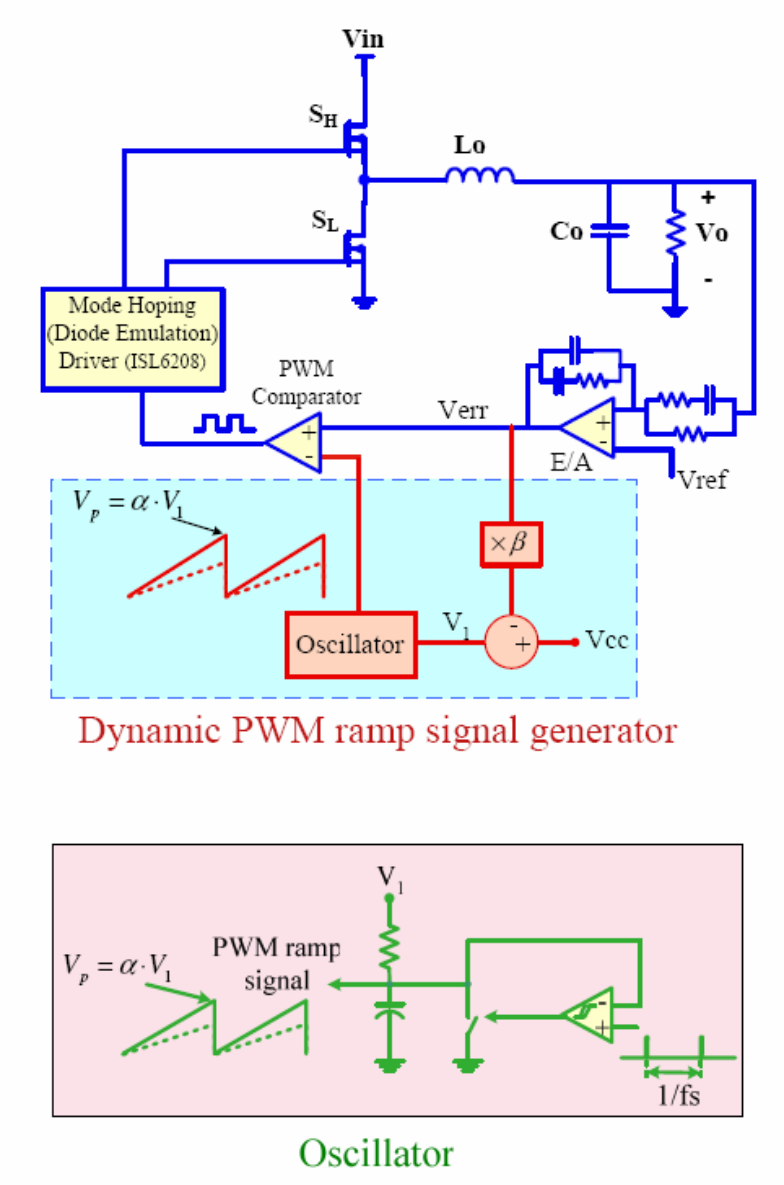


Fig. 6. 2: Implementation of the proposed control method

6.3 Theoretical proof of load transient improvement

In order to verify the proposed control method benefit, the error signal change (ΔVe) caused by a certain load transient in DCM should be investigated and compared with that of the conventional constant ramp. The aim behind this proposed control method is to minimize the ΔVe caused by load transient.

In a conventional constant ramp, the duty ratio can be expressed as in Eq. 6.1,

$$\frac{V_e}{V_{p\_f}} = D \qquad \textit{Eq. 6. 1}$$

where, Ve is the error signal and Vp_f is the fixed ramp signal peak.

When load transient occurs, the duty ratio has to change by ΔD; similarly, the error signal has to change by ΔVe, and Eq. 6.2 has to satisfy the steady state operation after load transient.

$$\frac{V_e + \Delta V_{e\_f}}{V_{p\_f}} = D + \Delta D \qquad \textit{Eq. 6. 2}$$

where ΔV_{e_f} is the error signal change for the conventional fixed ramp control.

Substituting Eq. 6.1 with Eq. 6.2, the error signal change ΔVe for the conventional fixed ramp is obtained as shown in Eq. 6.3.

$$\Delta V_{e\_f} = V_e \cdot \frac{\Delta D}{D} \qquad \textit{Eq. 6. 3}$$

By repeating the above steps for the proposed dynamic ramp control, the duty ratio can be expressed as in Eq. 6.4.

$$\frac{V_e}{V_{p\_d}} = \frac{V_e}{V_{p\_f} - \beta \cdot V_e} = D \qquad \textit{Eq. 6. 4}$$

where, Vp_d is the dynamic ramp signal peak.

When load transient occurs, the duty ratio has to change by ΔD; similarly, the error signal has to change by ΔVe, and Eq. 6.5 has to satisfy the steady state operation after load transient.

$$\frac{V_e + \Delta V_{e\_d}}{V_{p\_f} - \beta \cdot (V_e + \Delta V_{e\_d})} = D + \Delta D \qquad \textit{Eq. 6. 5}$$

where, ΔV_{e_d} is the error signal change for the proposed dynamic ramp.

Substituting Eq. 6.4 with Eq. 6.5, the error signal change ΔVe for the proposed dynamic ramp is obtained as in Eq. 6.6.

$$\Delta V_{e\_d} = \frac{\Delta D}{D} \cdot V_e \cdot \frac{V_{p\_f} - \beta \cdot V_e}{V_{p\_f} + \beta \cdot V_e \cdot \frac{\Delta D}{D}} \qquad \text{Eq. 6. 6}$$

Using Eq. 6.3, Eq. 6.6 can be rewritten as shown in Eq. 6.7.

$$\Delta V_{e\_d} = \Delta V_{e\_f} \cdot \frac{V_{p\_f} - \beta \cdot V_e}{V_{p\_f} + \beta \cdot V_e \cdot \frac{\Delta D}{D}} \qquad \text{Eq. 6. 7}$$

Since $\frac{V_{p\_f} - \beta \cdot V_e}{V_{p\_f} + \beta \cdot V_e \cdot \frac{\Delta D}{D}} < 1$, then $\Delta V_{e\_d} < \Delta V_{e\_f}$, meaning that the proposed dynamic ramp control allows duty ratio to reach its steady state after load transient occurrence with less error signal deviation, resulting in faster response and less output voltage deviation.

Note that Eq. 6.3 is a special case of Eq. 6.6 where $\beta = 0$, since $\beta = 0$ signifies that the error signal is not fed to the oscillator and does not affect the ramp signal peak.

6.4 *Control loop analyses*

The basic blocks of a closed loop buck regulator are shown in Fig. 6.3. The gain equations of the blocks are available in books and in the literature [57, 58], and are expressed as in Eq. 6.8 and Eqs. 6.8 (a-d).

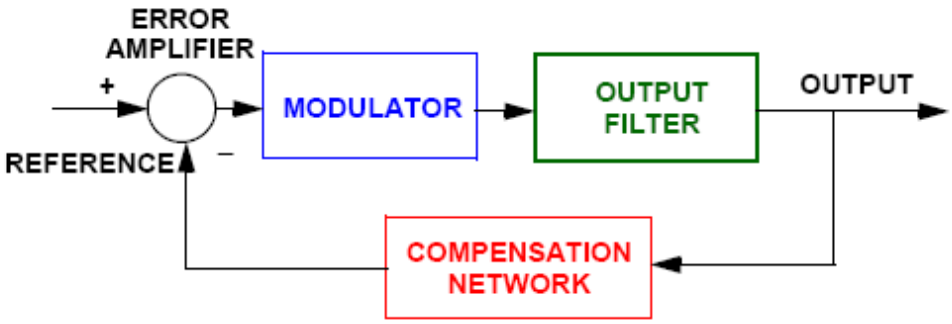


Fig. 6. 3: Basic blocks of Buck regulator

$$G_{SYSTEM} = G_{MODULATOR} \cdot G_{COMPENSATOR} \cdot G_{FILTER} \qquad \text{Eq. 6. 8}$$

where,

$$G_{MODULATOR} = \frac{V_{in}}{V_{OSC}}, \qquad \text{Eq. 6. 8a}$$

V_{OSC} is the PWM ramp signal peak-peak voltage

$$G_{COMPENSATOR\_TYPE\ III} = K \cdot \frac{(1+s/\omega_{Z1}) \cdot (1+s/\omega_{Z2})}{s \cdot (1+s/\omega_{P1}) \cdot (1+s/\omega_{P2})} \qquad \text{Eq. 6. 8b}$$

$$G_{FILTER\_CCM} = \frac{1+s \cdot ESR \cdot C}{1+s \cdot (ESR+DCR) \cdot C + s^2 \cdot L \cdot C} \qquad \text{Eq. 6. 8c}$$

$$G_{FILTER\_DCM} = H_d \frac{1+s/s_{Z1}}{(1+s/s_{P1})(1+s/s_{P2})} \qquad \text{Eq. 6. 8d}$$

where,

$$H_d = \frac{2 \cdot V_o}{D_{DCM}} \cdot \frac{(1 - D_{DCM})}{(2 - D_{DCM})}, \quad s_{Z1} = \frac{1}{ESR \cdot C}, \quad s_{P1} = \frac{I_o}{V_o \cdot C} \cdot \frac{2 - M}{1 - M}, \quad s_{P2} = 2 \cdot f_s \cdot \left(\frac{M}{D_{DCM}} \right)^2$$

$$M = \frac{V_o}{V_{in}}, \quad D_{DCM} = \sqrt{\frac{2 \cdot I_o \cdot L \cdot f_s}{V_o (1 - M)}} \cdot M$$

From Eqs. 6.8 and 6.8a, it is clear that the closed loop gain can be modulated by modulating the PWM ramp signal peak, consequently, the PWM modulator gain. During step-up load transient, it is desired to increase the loop gain. And during step-down load transient, the loop gain should be decreased so that duty ratio can reach steady state faster. This can be achieved by modulating the ramp signal peak with an inverse relationship to the compensator error signal, which is related to load current.

Figure 6.4 shows a plot of the PWM modulator gain as a function of the ramp signal peak for an input voltage of 5V. It demonstrates that decreasing the ramp signal peak increases the modulator gain, and thus increases the close loop gain. By using Eqs. 6.8 and 6.8(a-d), the loop gain and phase bode-plots can be obtained for CCM and DCM at different load currents and different ramp peak values. Figure 6.5 shows a comparison between the bode plots of a closed loop buck regulator for fixed ramp peak control and the proposed dynamic ramp peak control; it is clear that the proposed control lowers the gain in DCM compared to those with fixed ramp peak control, but it has no effect on the phase. This feature of adjustable gain speeds the error signal and duty ratio response to load transient. Thus, the output voltage will have less deviation.

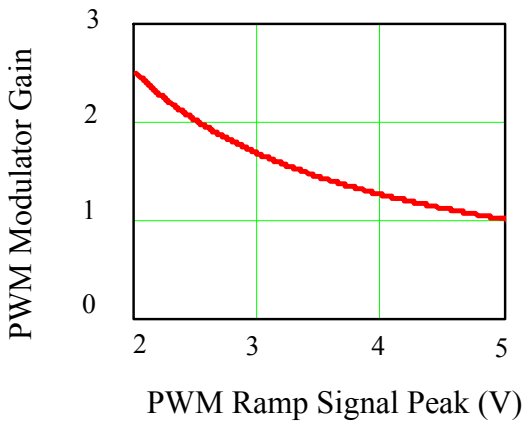


Fig. 6. 4: *PWM modulator gain vs. ramp signal peak, and closed loop buck regulator Bode-Plots for different PWM ramp signal peaks*

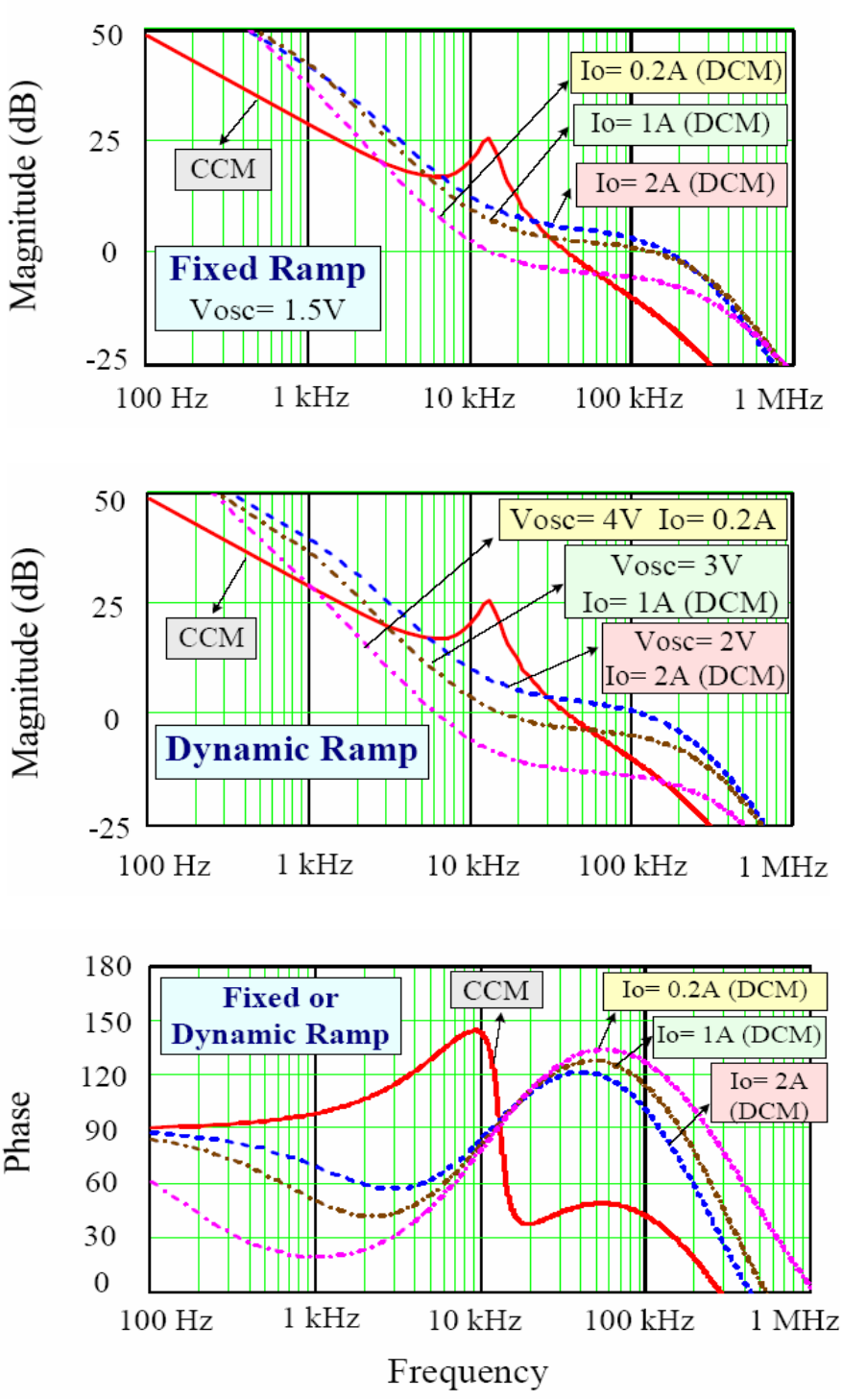


Fig. 6. 5: Comparison between the bode plots of a closed loop buck regulator for fixed ramp peak control and the proposed dynamic ramp peak control

6.5 Experimental results

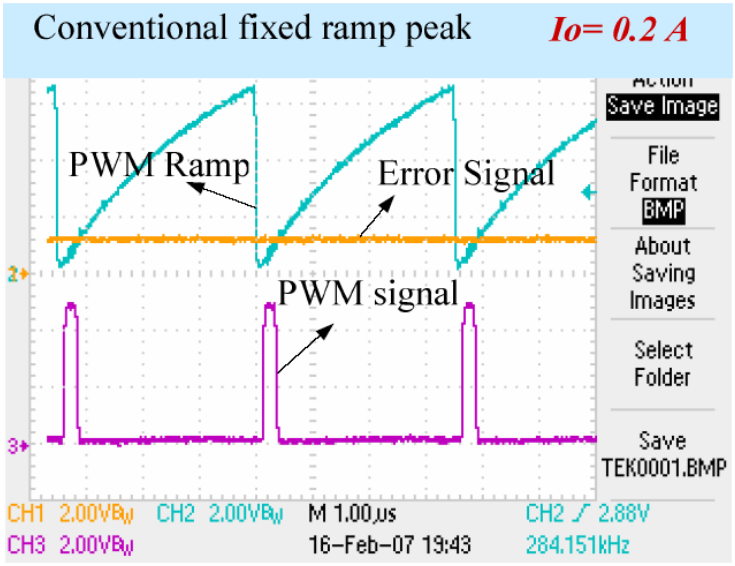
A prototype was built to verify the proposed control method with the following specifications: Vin= 5V, Vo=1.5V, f= 300kHz, Lo= 0.5uH, Co= 300uF. It revealed significant transient response improvement.

Figure 6.6 shows waveforms for the conventional fixed ramp peak control; Fig 6.6(a) shows that at low current in DCM (0.2 A), the duty ratio is small and consequently the error signal is also small. While at higher current in DCM (2A) as shown in Fig. 6.6(b), the duty ratio increases significantly and therefore the error signal must increase significantly. Figure 6.6(c) shows waveforms during load transient (0.2-2-0.2A load step) for a conventional fixed ramp control; it is clear that stepping current in DCM requires significant duty ratio change, consequently, significant error signal change (~1.6V). As a result, it takes a longer time for the error signal to reach steady state. It is clear from the figure that the output voltage has a deviation of (~ 350mV).

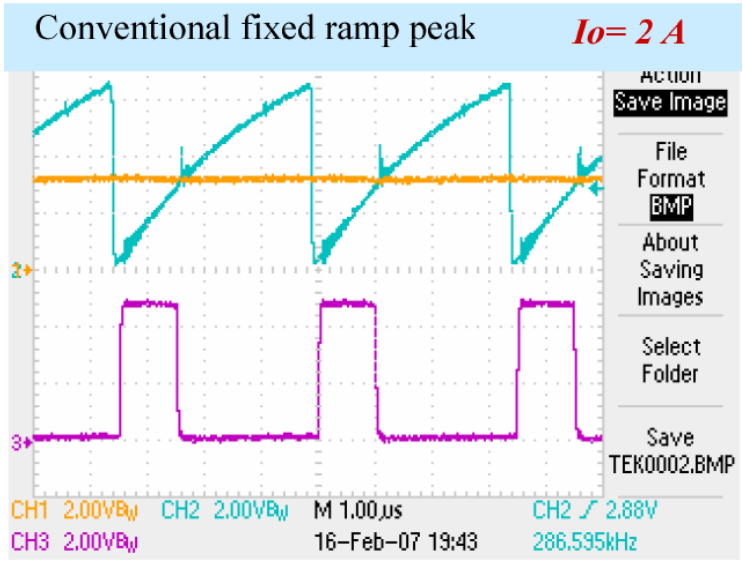
Conversely, Fig. 6.7 shows waveforms for the proposed dynamic ramp peak control; Fig 6.7(a) shows that at low current in DCM (0.2 A), the duty ratio is small. While at higher current in DCM (2A) as shown in Fig. 6.7(b), the duty ratio increases significantly but the error signal increases slightly due to lowering the ramp peak. Figure 6.7(c) shows waveforms during load transient (0.2-2-0.2A load step) for proposed dynamic ramp control; it is clear that when stepping current in DCM, the required significant duty ratio change can be achieved by slight error signal change (~80mV) with the help of the dynamic ramp peak. As a result, it takes a shorter time for

the error signal to reach steady state. It is clear from the figure that the output voltage deviation has been extensively reduced to become (~ 100mV).

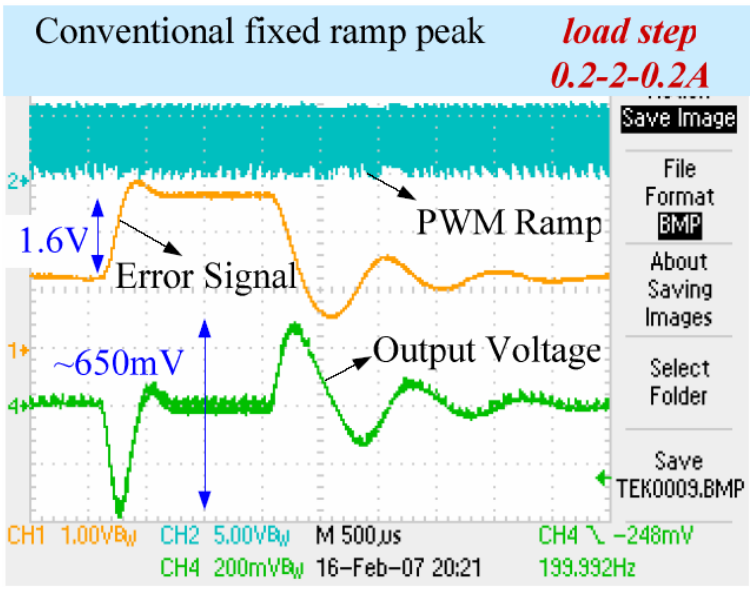
It must be noted that in the waveforms below (Figs. 6. 6 and 6.7), the PWM signal does not go low at the exact time of intersection between the ramp signal and the error signal. This is because the ramp signal has an offset of (+0.7V) inside the PWM controller prior to being fed to the negative input terminal of the PWM comparator.



(a)

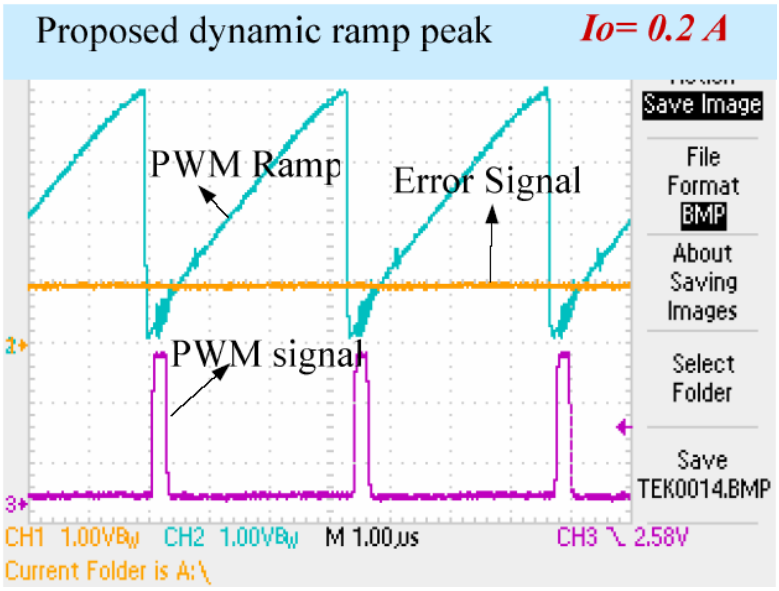


(b)

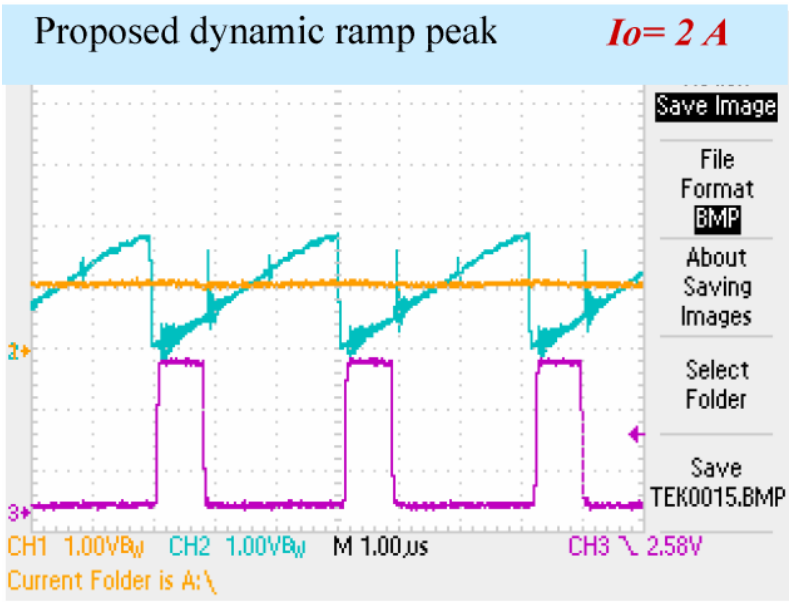


(c)

Fig. 6. 6: Conventional fixed ramp peak control waveforms.


Proposed dynamic ramp peak
Io= 0.2 A
PWM Ramp
Error Signal
PWM signal
Save Image
File Format BMP
About Saving Images
Select Folder
Save TEK0014.BMP
CH1 1.00V
CH2 1.00V
M 1.00µs
CH3 2.58V
Current Folder is A:\

(a)


Proposed dynamic ramp peak
Io= 2 A
Save Image
File Format BMP
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Select Folder
Save TEK0015.BMP
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CH2 1.00V
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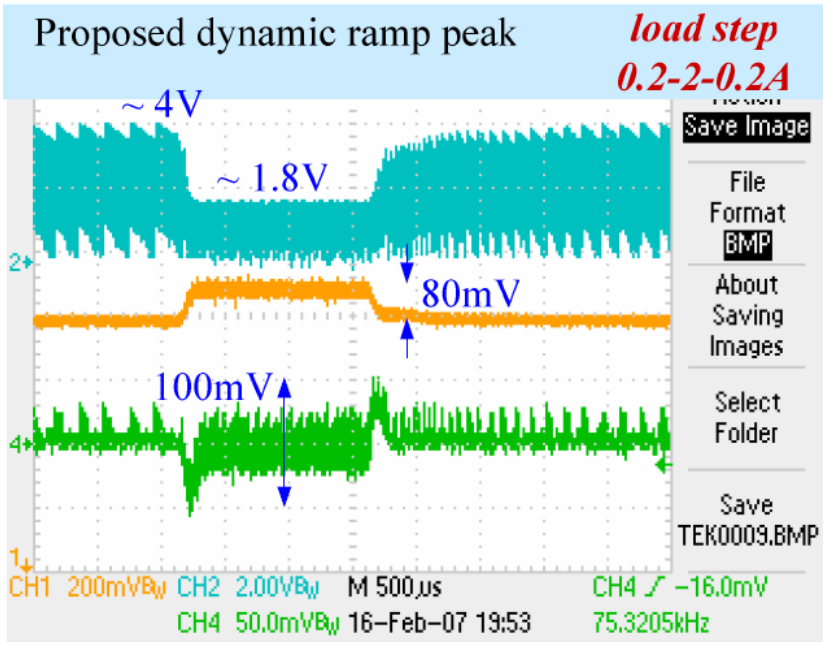
CH3 2.58V
Current Folder is A:\

(b)



(c)

Fig. 6. 7: Proposed dynamic ramp peak control waveforms.

6.6 Conclusion

A control method was presented to improve transient response in DCM and Mode Hoping operation, where duty ratio varies significantly with load current variation. The presented control dynamically modulates the PWM ramp signal peak based on the error signal so that the control loop gain is dynamically modulated, allowing duty ratio to reach steady state faster. Therefore, lower output voltage deviation is achieved during load transient. Principle of operation, analyses, implementation, and experimental results were presented. Experimental results revealed significant load transient improvement compared to fixed ramp peak control.

The presented control method can be easily applied to switching regulators (controllers) in order to offer a solution to the increased load transient voltage deviation caused by the DCM operation. Its simple design makes it a practical method. Moreover, the dynamic PWM ramp can be integrated within the controller ICs with no additional cost or size.

CHAPTER 7: TRANSIENT RESPONSE IMPROVEMENT IN DC-DC CONVERTERS USING OUTPUT CAPACITOR CURRENT FOR FASTER TRANSIENT DETECTION

Presented is an approach to significantly limit the voltage overshoot and undershoot during load transient and reduce the number of capacitors, without compromising on the efficiency, cost or size of the dc-dc converter. It will allow for the optimization of the power stage efficiency for the dc operation with less concern of dynamic performance, while an additional switching circuit that utilizes the output capacitor current to detect load transient is activated during load step up to deliver the shortage charge to the output capacitor; also, the extra charge from the output capacitor will be extracted during load step down. Therefore, lower voltage deviation is achieved during load transient. The principle of operation and experimental results are presented.

7.1 Principle of operation and implementation

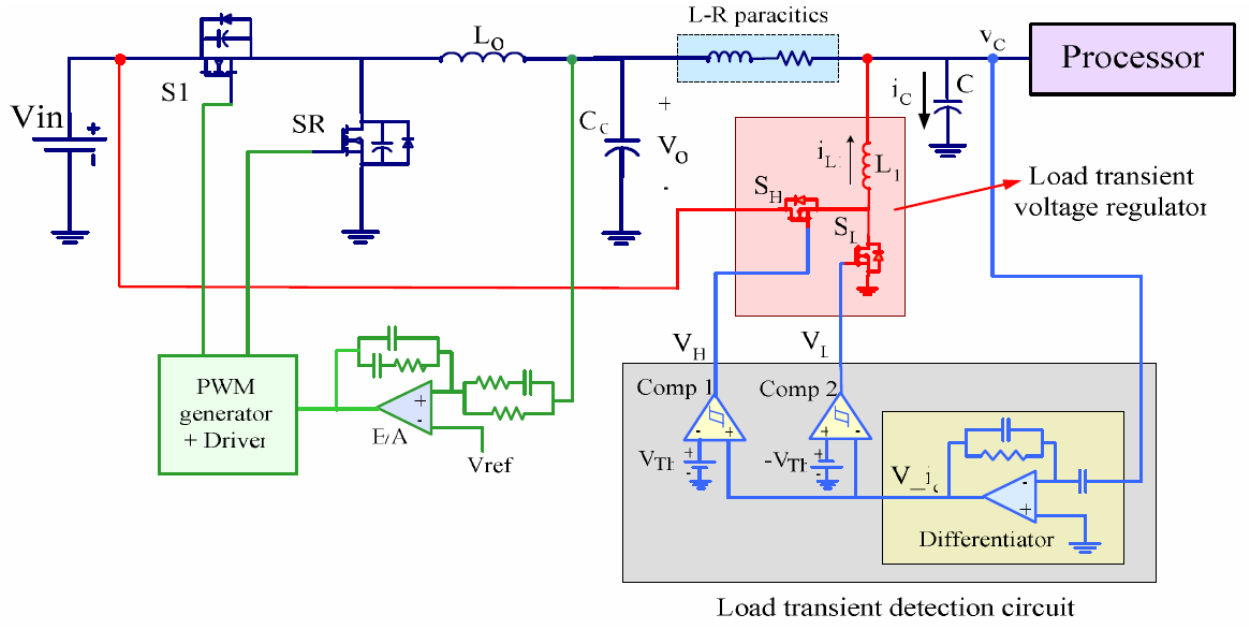
Figure 7.1 shows the proposed converter and its key waveforms. A conventional synchronous buck converter with a conventional control loop is used to deliver the dc power to the load (Processor). The power stage can be well optimized to have high efficiency, unlike other methods, where the filter inductor is lowered and switching frequency is increased to achieve fast transient response and maintain the transient voltage deviation within the limits. In addition, the number of output capacitance can be less, since there is no need to store a big charge in the capacitors to supply the transient load. The transient load is supplied by the load transient voltage regulator as shown in the figure; the two switches (S_H and S_L) and the inductor (L_1) can supply the step-up load transient to suppress undershoot and pull out the excess inductor current during

step-down load transient to suppress overshoot. Since the capacitor current represents the difference between the filter inductor current and the load current, when a step-up load transient occurs, the filter inductor current needs some time to rise to the load current value; meanwhile, the capacitor current will have to supply the load with the shortage current. This will cause a negative current spike in the output capacitance as shown in Fig. 7.1. However, when a step-down load transient occurs, the capacitor will have to store the excess inductor current until it reaches steady state, and this will cause a positive spike in the capacitor current as shown in Fig 7.1. In this proposed converter, the capacitor's negative spike is used to indicate load step-up transient, and the positive spike is used to indicate load step-down transient. The capacitor current used for transient detection is obtained by differentiating the capacitor voltage, since i_c= C dv_c/dt, the output of the differentiator are voltage spikes that represent the inverted current spikes, the voltage spikes are compared to pre-set threshold voltages to sense transient.

At step-up load transient, the differentiator outputs a positive voltage spike. When the spike exceeds the positive threshold (V_{Th}), the comparator (Comp1) outputs a high signal that turns on the high switch (S_H), allowing fast current delivery from input to the load through inductor L_l which has a small inductance value in order to provide high slew rate current. This stops the capacitor current spike to exceed a certain limit that is determined by the V_{Th} ; thus, the output voltage will not have an undershoot and will be clamped to a certain value determined by the V_{Th}.

Alternately, when a load step-down transient occurs, the differentiator outputs a negative voltage spike. When the spike goes below the negative threshold ($-V_{Th}$), the comparator (Comp2) outputs a high signal that turns on the low switch (S_L), allowing fast current pull from output to input through inductor L_1. This prevents the capacitor current spike from going below a certain limit that is determined by the $-V_{Th}$; therefore, the output voltage will not have an overshoot and will be clamped to a certain value determined by the $-V_{Th}$.

It is shown in Fig. 7.1 that the load transient regulator is connected directly to the input of the processor and placed nearby, so that the delivered or pulled out power does not pass through the line R-L parasitics that slow down the transient current. It is possible to integrate the transient regulator inside future generations of processors. It is also shown in the figure that the input voltage node of the processor is being used for transient detection instead of the power stage output voltage node, since it can provide earlier indication of load transient.



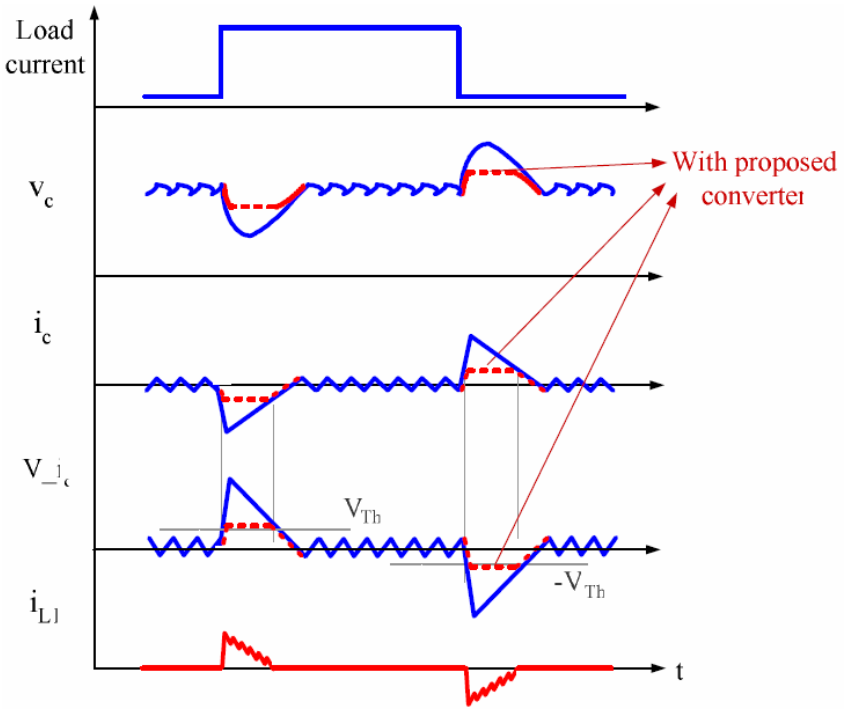


Fig 7. 1: Proposed converter implementation and key waveforms

7.2 Experimental results

To evaluate the presented concept, a prototype was built with the following specification: V_{in}= 5 V, V_{out}= 1.5 V, I_{out}= 0-10A, f= 300 kHz, Lo= 1uH, L1= 100nH, and output capacitance= 200uF. Mosfet HAT2165 was used for the S1, SR, SH and SL. Figure 7.2 shows a load step-up transient (0 to 10 A step) before and after applying the proposed converter; it is clear that after applying the transient regulator, the output voltage undershoot was reduced from 250mV to 120mV. Figure 7.3 shows a load step-down transient (10 to 0 A step) before and after applying the proposed converter; it is apparent that after applying the transient regulator, the output voltage overshoot was reduced from 350mV to 80mV. Figure 7.4 shows the overall improvement of output voltage deviation during load transient (0-10-0 A load step) when applying the proposed converter; voltage deviation was reduced from 600mV to 200mV.

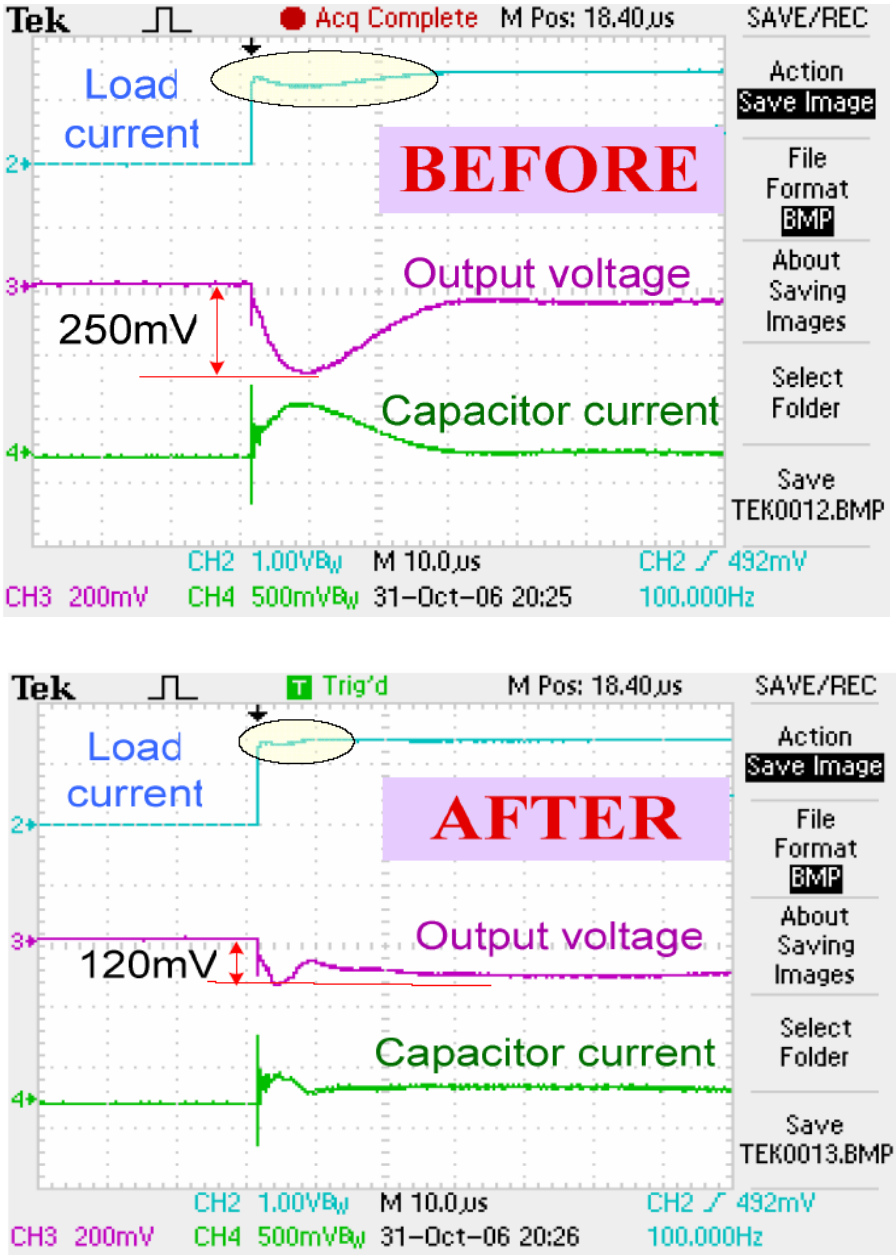


Fig 7. 2: Load step-up transient (0A - 10A step) before and after applying the proposed converter.

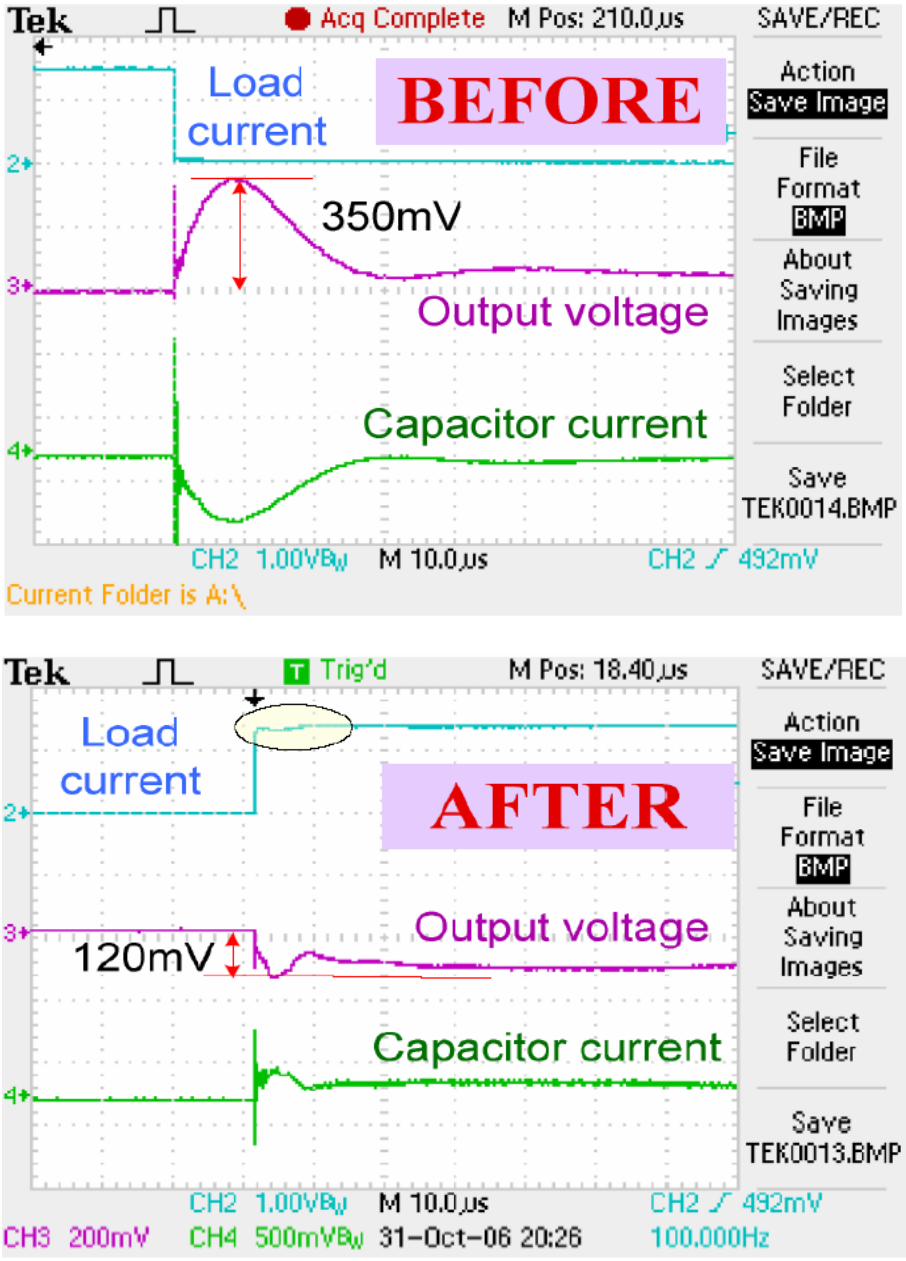


Fig 7. 3: Load step-down transient (10A - 0A step) before and after applying the proposed converter.

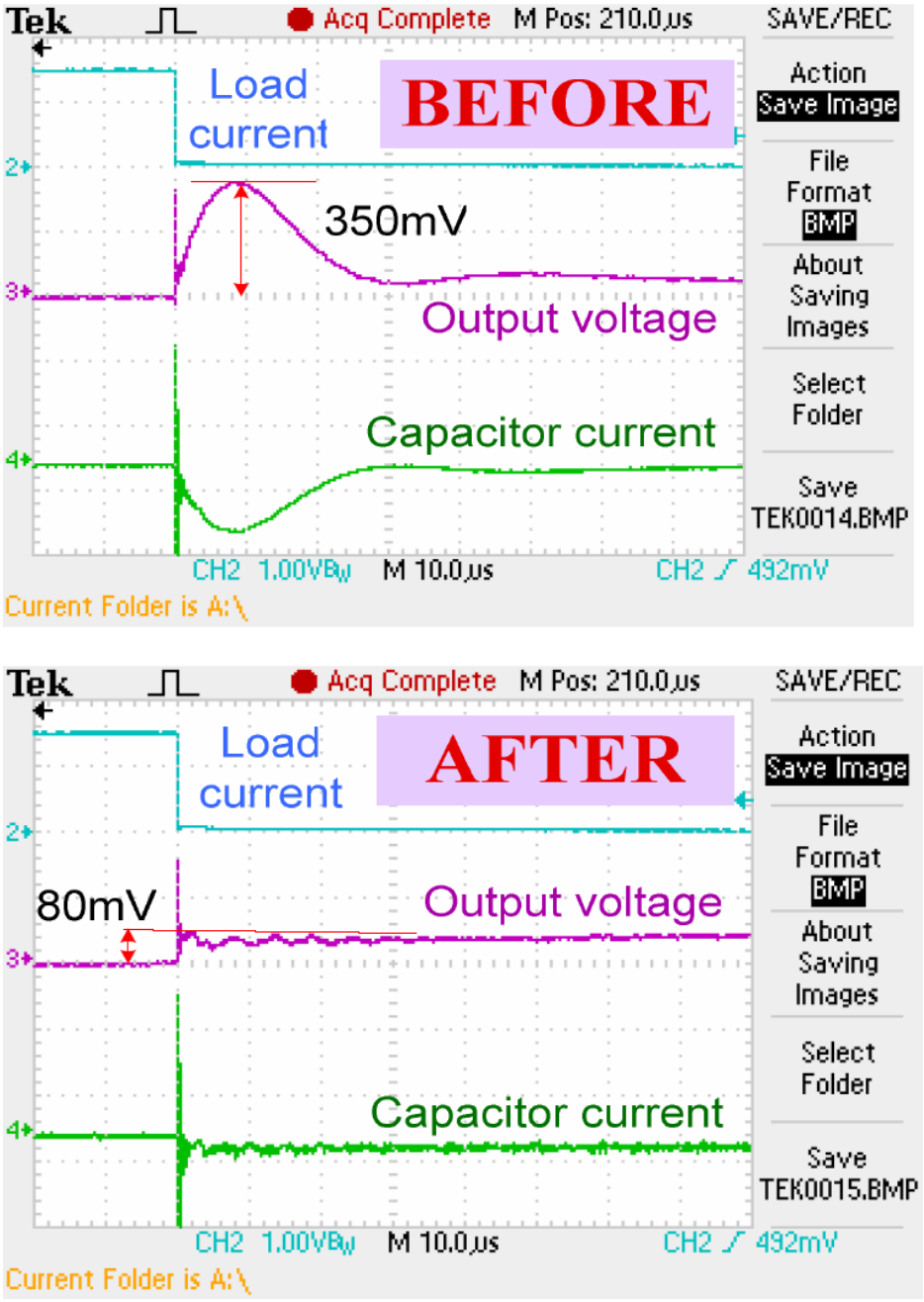


Fig 7. 4: Load transient (0A - 10A - 0A) before and after applying the proposed converter.

7.3 Conclusion

A load transient voltage regulator is activated only during load transient to deliver power to the load during step-up transient to reduce voltage undershoot and to pull out the extra power during step-down transient to reduce voltage overshoot. Load transient is detected by sensing the output capacitor current. The presented circuit transient response was improved without sacrificing efficiency, size, or cost. Results of the experiment verified the principle of operations and showed significant improvement in transient response.

The presented circuit can be applied to voltage regulators supplying fast dynamic load such as CPUs or DSPs; it allows the main power stage design to be optimized for high efficiency with less concern of dynamic performance, since the presented circuit is able to regulate the output voltage during load transient times.

The drawback of the presented circuit is that its efficiency is low compared to the main power stage efficiency. Therefore, in cases of high repetitive loads, the presented circuit will be activated more frequently, which degrades the overall efficiency of the system.

CHAPTER 8: SUMMARY AND FUTURE RESEARCH WORK

8.1 Summary

The area of power electronics is notably expanding to influence the rapidly advancing markets. Power converters must meet the state of the art technologies in order to be able to keep up with the high standards and specifications of power applications. Future power converters tend to have smaller sizes and higher power requirements. Therefore, the research in the area of improving the performance of DC-DC power converters is highly appreciated.

This research work has focused on soft switching topologies for efficiency improvement, adaptive control techniques for improving all load efficiency of battery powered applications, and techniques to improve load transient and reduce the output voltage deviation.

In chapter 2, the concept of Active Resonant Tank (ART) and a general method for applying the ART cell to non-isolated topologies were introduced. A high-frequency, high-efficiency ART buck converter was introduced as an example, in which an active resonant tank is connected in parallel with SR to achieve Zero-Voltage-Switching (ZVS) for the active switch and to eliminate SR-related body-diode conduction and reverse recovery problems. Experimental results are very close to the theoretical analyses. High efficiency at high switching frequency is achieved due to the reduced switching loss and reverse-recovery loss compared to the conventional hard-switching buck converter.

In chapter 3, the LCC ZVS Buck converter was presented to achieve Zero-Voltage-Switching (ZVS) and eliminate body-diode conduction and hard-switching reverse recovery in the conventional Buck converter with Synchronous Rectifiers (SRs). The presented converter is advantageous over the QSW converter since it is capable of saving the same switching losses without increasing the output current ripple and therefore less output capacitance is required; it also has half the input current ripple of the QSW converter. Experimental results show that the presented converter is significantly advantageous for high switching frequency. The presented converter is a competitive topology for the SR applications with high voltage and high switching frequency.

In chapter 4, analyses and design of VR efficiency and performance considering lighter load conditions were discussed. Review of several techniques along with their power loss analyses curves for a design example was presented. Moreover, a load adaptive control scheme with non-linear variable frequency and peak current tracking, namely Pulse-Sliding, was proposed to improve VR light load efficiency while maintaining good steady-state performance. Concept, analyses, and experimental results of the presented scheme were presented.

In chapter 5, a load adaptive voltage regulator that achieves high efficiency extended to light load and heavy load regions was introduced. The presented AFM is capable of adaptive modulation of FETs' parasitic charges and resistances along with adaptive gate driving voltage in order to achieve FET optimization for wide load range. The concept, design, analyses and experimental results of the AFM converter were presented.

In chapter 6, a control method was introduced to improve transient response in DCM and Mode Hoping operation, where duty ratio varies significantly with load current variation. The presented control dynamically modulates the PWM ramp signal peak based on the error signal so that the control loop gain is dynamically modulated, allowing duty ratio to reach steady state faster. Therefore, lower output voltage deviation is achieved during load transient. Principle of operation, analyses, implementation and experimental results were presented. Experimental results showed significant load transient improvement compared to fixed ramp peak control.

In chapter 7, a load transient voltage regulator that uses output capacitor current to sense load transient was introduced. The presented circuit delivers power to the load during step-up transient to reduce voltage undershoot, and it also pulls out the extra power during step-down transient to reduce voltage overshoot. Transient response was improved without sacrificing efficiency, size, or cost. Experimental results verified the principle of operations and showed significant improvement in load transient response.

8.2 Future research work

At the end of each chapter, a conclusion was provided, including the application of the presented concept, in addition to the benefits and drawbacks of that concept. Future research work intends to improve the performance of the presented ideas and to eliminate or minimize their disadvantages.

In chapter 2, the ART cell presented the current injection to achieve soft switching in high voltage high frequency applications. Future work would concern expanding this cell to isolated topologies and figure its benefits on Point of Load converters with high currents and low output voltages.

In chapter 3, the LCC converter achieves soft switching in high voltage high frequency applications. The drawback of this converter is that the L2 inductor carries a current ripple that is fixed regardless of the load current, which becomes less efficient at light load and mid load regions. Future work would concern adapting the L2 current ripple to load current, so that at lower load conditions the current ripple is reduced to what is just enough to achieve the soft switching in order to minimize the conduction losses in the LCC network

In chapter 4, the PSL controller was presented to improve light load efficiency by modulating switching frequency in a non-linear manner in order to maintain controlled output voltage ripple.

Future work would concern implementing logic gates of the controller digitally, which can provide more design flexibility.

In chapter 5, the AFM converter was presented in order to extend the high efficiency to light and heavy load regions. Future work would concern implementing it in multiphase converters along with the PSL discussed in chapter 4, which can offer higher optimization to the light load efficiency. Merging the AFM converters with the PSL controller will significantly reduce switching related losses at light loads.

In chapter 6, the dynamic PWM ramp control was presented to improve load transient in DCM operation. Future work would concern improving this concept and making it more robust and optimized in order to make it a good candidate in future controllers.

In chapter 7, a load transient regulator was presented as a means to supply the load during transient times in order to limit the output voltage deviation during transient. Future work would concern the analyses of its performance with high repetitive loads with high transient frequencies and comparing its performance to the conventional methods of improving the dynamic performance such as increasing switching frequency and lowering the converter's output impedance.

In addition to the intended future work for the chapters outlined in this dissertation, the author of this paper intends to extend research work that will investigate new control techniques to

improve the power management in converters and power systems with the emphasis on digital power techniques. The author also plans to investigate resonant converters and develop new control techniques, seeking ways to highlight the advantages of the resonance operation such as soft switching and minimizing the drawbacks such as control complexity.

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