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DYNAMIC MODELING OF PWM AND SINGLE-SWITCH SINGLE-STAGE POWER FACTOR CORRECTION CONVERTERS

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ABSTRACT

The concept of averaging has been used extensively in the modeling of power electronic circuits to overcome their inherent time-variant nature. Among various methods, the PWM switch modeling approach is most widely accepted in the study of closed-loop stability and transient response because of its accuracy and simplicity. However, a non-ideal PWM switch model considering conduction losses is not available except for converters operating in continuous conduction mode (CCM) and under small ripple conditions. Modeling of conduction losses under large ripple conditions has not been reported in the open literature, especially when the converter operates in discontinuous conduction mode (DCM). In this dissertation, new models are developed to include conduction losses in the non-ideal PWM switch model under CCM and DCM conditions. The developed model is verified through two converter examples and the effect of conduction losses on the steady state and dynamic responses of the converter is also studied.

Another major constraint of the PWM switch modeling approach is that it heavily relies on finding the three-terminal PWM switch. This requirement severely limits its application in modeling single-switch single-stage power factor correction (PFC) converters, where more complex topological structures and switching actions are often encountered. In this work, we developed a new modeling approach which extends the

PWM switch concept by identifying the charging and discharging voltages applied to the inductors. The new method can be easily applied to derive large-signal models for a large group of PFC converters and the procedure is elaborated through a specific example. Finally, analytical results regarding harmonic contents and power factors of various PWM converters in PFC applications are also presented here.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

Modeling of switched-mode DC/DC converters is a very important research area in power electronics. The need for dynamic models of the power stage lies in fact that the DC/DC converter goes through different circuit topologies within each switching period, depending on its operation modes. The overall response of all state variables with respect to external disturbances needs to be predicted such that this response could be controlled and minimized through properly designed control circuits. The purpose of the feedback loop is to remedy any undesirable dynamic nature and to optimize the overall performance of the power regulator. Once the model or the transfer function of the power stage is found, sophisticated control theory can be applied to design the controllers characterized in terms of the concepts such as loop gain, bandwidth and stability margins.

The quality of power supply systems is evaluated from its voltage magnitude, frequency and waveform. In early stages, power systems were subjected only to some inconsistent transient disturbances such as breaker operation, load change and equipment fault, etc., as well as the effects of transformer nonlinearity. Voltage and current distortions were generally very small. During normal operation, power engineers were mainly concerned about providing a voltage with stable magnitude and frequency. Power

quality were maintained at a satisfactory level through improvement of the transmission and distribution network, improvement of the equipment design and manufacturing as well as reactive power management and balancing on the busbars.

1.1 Origin of Harmonics

The origin of harmonics can be traced back to the beginning of this century when mercury arc rectifiers emerged and found wide applications in electrochemical industry and high voltage direct current (HVDC) transmission in the 1930s. Since then, power system safe operation has encountered a new challenge: harmonics. Nonlinear loads, such as rectifiers, absorb non-sinusoidal current which is rich in high frequency components-harmonic currents, when connected to the ac line. These harmonic currents generate harmonic voltages when flowing through system impedance. They are superimposed on the fundamental voltage and subsequently distorted the bus voltage waveform.

The first noticeable effect of the consistent harmonic disturbances was on the communications systems because of their electromagnetic interference (EMI) with adjacent communication lines [1, 5]. Since the mid-60s, harmonic problem has gradually attracted attention in the power engineering and is now becoming a pressing issue mainly because of the following reasons:

1) Increased use of high power semiconductor switching components in energy conversion and motor drives such as in rolling mill machines, electric arc furnaces, HVDC, traction systems, etc. Loads with nonlinear characteristics such as rectifiers

have gradually constituted the major portion of electrical loads in most of the power systems.

2) High power rectifier loads usually dissipate large amount of reactive power during their normal operation, resulting in voltage fluctuation and excessive energy loss on the transmission lines. To improve system power factor and voltage regulation, shunt capacitors are used to provide the reactive power compensation. However, in a harmonic environment, these capacitors will resonant with system impedance at certain harmonic frequencies and cause greater voltage distortion, causing more serious harmonic pollution in power systems.

Most of the electrical equipment has been designed and manufactured to operate efficiently assuming ideal sinusoidal environment. In a polluted system, however, its operation may be deviated from the designed normal conditions. In additional to telephone interference, power system harmonics are found to be the major threat to the safe operation of the power systems. Some of their influences are [1-7]:

1) Affect the smooth operation of motors because of the presence of additional torque generated by the negative sequence harmonic currents.
2) Results in excessive heating in transformers and motors by increasing magnetic core losses.
3) Generate abnormal audible noises and mechanical vibration of the transformers and motors.
4) Cause malfunction of protection relays.
5) Accelerate aging of insulating media.

6) Increase instrument error.

7) Overloading shunt capacitor banks.

In view of the proliferation of the power electronic equipment connected to the utility grid, some national and international harmonic standards have been developed to limit harmonic current injection or to limit the harmonic voltages at the point of common coupling (PCC) [7-10] to protect power system safe operation. The two that draw most attention are the recommended IEEE 519-1992 [8] and the IEC 1000 family [9]. Table 1-1 shows the voltage distortion limits set by the standard IEEE 519. The underlined consideration of the standard is to prevent harmonic currents generated by nonlinear loads from interfere with other customers. In other words, the electric utility and the user of electric equipment are both responsible for improving the power quality. IEC 1000-3-2 classifies power electronics equipment with a maximum input current less than or equal to 16A per phase into four categories. Among those the harmonic limits of the class D received the most attention since most of the switch-mode power conversion systems fall into this category. It also has a profound impact to the power electronics industry as it set the harmonic emission level for individual power equipment. Table 1-2 shows the harmonic current limits of this class and Fig. 1-1 gives a graphic presentation of the second column on maximum harmonic current per watt that can be generated by electric equipment. The IEC 1000 standard, once approved by the European Standardization Committee for Electrical Products, will be enforced by law in Europe in January 2001.

Table 1-1. IEEE 519 voltage distortion limits

Bus voltage at PCC	Individual voltage distortion (%)	Total voltage distortion THD (%)
69kV and below	3.0	5.0
69.001kV through 161kV	1.5	2.5
161.001kV and above	1.0	1.5

Table 1-2. IEC 1000-3-2 harmonic current limits for class D electric equipment

Harmonic order, n	Maximum permissible harmonic current per watt, mA/W	Maximum permissible harmonic current, A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.4
11	0.35	0.33
13≤n≤39, odd harmonics	3.85/n	Refer to class A

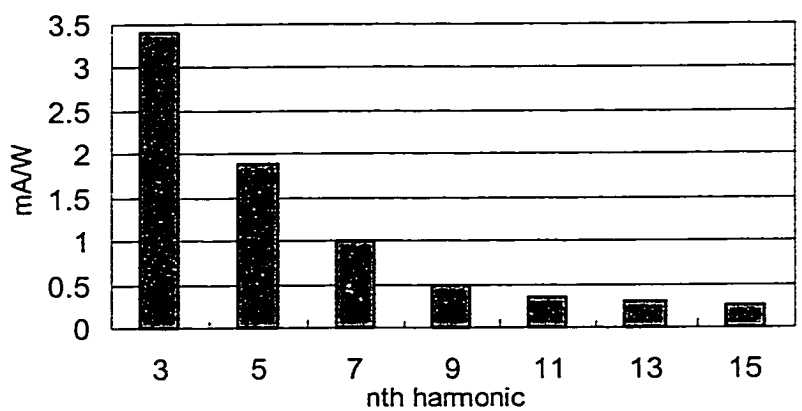


Fig. 1-1. Maximum permissible harmonic current per watt for class D electric equipment.

Solution for harmonic reduction and power quality improvement can be achieved by installing harmonic compensation equipment beside the rectifier loads or by modifying conversion topologies as well as developing new conversion techniques.

The purpose of installing harmonic compensation equipment is to provide an alternate path for harmonic currents generated by the nonlinear loads to prevent them from flowing into the power systems. The following approaches have been proven to be very successful in the past several decades [11-17].

1) Installing harmonic filter banks: to avoid resonance between reactive power compensation capacitors and system impedance at some harmonic frequencies, a carefully designed reactor is inserted into the capacitor branches such that the inductor-capacitor tuned to particular frequencies to provide a low impedance path to bypass one or more harmonic currents. The method is very effective for balanced systems where load variation is moderate.
2) In systems where the load is subjected to large changes such as with the rolling mill machine, a Static Var Compensator (SVC) can be installed. The SVC contains a filter bank which is responsible for filtering out the harmonic currents and a reactive power regulator to compensate for variations in reactive power consumed by the load.
3) Time-domain reactive power compensation: also called active filtering. This method is based on the theory that the distorted current absorbed by a nonlinear load can be decomposed into two perpendicular components: active component and reactive component. The active component has the same shape and is in phase with the supplying voltage. Its magnitude is determined by the active power of the load.

Active filters eliminate harmonic currents by injecting a controlled current into the system with its magnitude equals that of the reactive component of the load current but has a 180° phase difference.

Active filtering is becoming a viable alternative solution to SVC since it achieves both harmonic elimination and reactive power compensation at the same time. It is also insensitive to changes in system and load operation conditions.

In addition to relying on external equipment and devices to prevent harmonic currents from polluting power systems, harmonic problem can also be alleviated effectively by minimizing harmonic current being generated. The traditional three-phase six pulse phase-controlled rectifier contains 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, ..., harmonic currents with magnitude of 1/5, 1/7, 1/11, 1/13, 1/17, ..., with respected to the fundamental current component for each harmonic current. By combining two six pulse rectifiers with 30° phase shift in between, a three phase twelve pulse phase-controlled rectifier is obtained, with which the 5^{th}, 7^{th}, 17^{th}, ..., harmonic currents can be significantly reduced, leaving only the smaller 11^{th}, 13^{th}, ..., harmonic currents present in the line current [2, 18].

It is noted that harmonic currents generated by many nonlinear loads including the six and twelve pulse rectifiers are in the frequency range of 2kHz. An alternative approach to perform power conversion from ac to dc is to utilize power electronic high frequency switching converters for input current shaping. This technique is called *active power factor correction* (PFC). The essence of this technique is to move the low

frequency harmonic current components to much higher frequency range (>50kHz) where they are much easier to handle. Advantages of PFC technique include:

1) The bulk and heavy line frequency transformer is ruled out.
2) The line current of the PFC converter is in phase with the line voltage, no reactive power compensation needed.

AC/DC power conversion circuits from low to medium power level for computers, television sets, communication systems, etc., contribute a large portion of power electronics applications because of the huge quantities involved. Switched-mode PFC power supplies are rapidly replacing earlier linear power supplies across the full spectrum of these applications. This dissertation is devoted to the analysis and modeling of the PFC converters.

1.2 Single-Switch Single-Stage PFC Converters

Figure 1-2 shows a block diagram for the PFC converter configuration. The front-end converter performs ac to dc conversion as well as line current shaping to obtain unity power factor. It serves as the interface between the line and the output stage converter which provides the required dc power to the load.

Most of the switched-mode DC/DC converters can be directly utilized as the PFC converter by incorporating a full bridge diode rectifier at their input. Figure 1-3 shows three basic DC/DC converter topologies. However, it should be noted that they present different input characteristics. For example, except in some special cases, the Buck converter and its derivations are not quite suited for power factor correction as they draw

zero current from the line when the instantaneous input voltage is lower than the output voltage, exhibiting a dead zone in their input *v-i* characteristics [19-23].

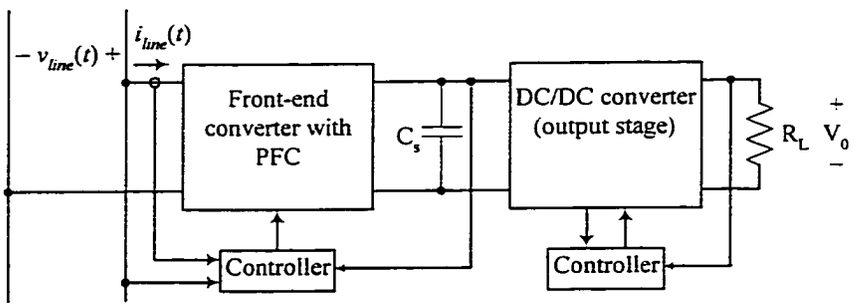
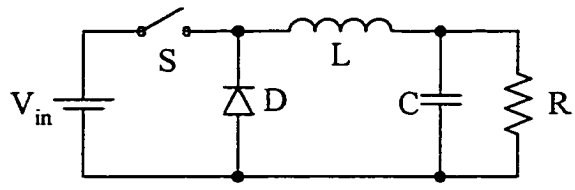
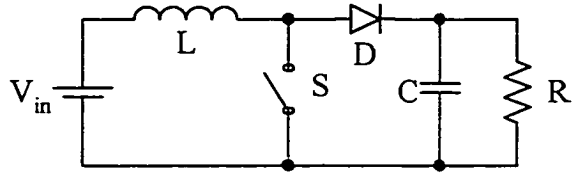


Fig. 1-2. The PFC converter block diagram.

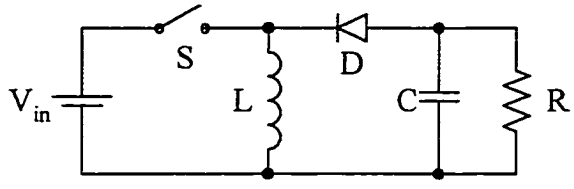
It should also be noted that energy balance from input to output for DC/DC converters is maintained in each switching cycle under steady-state operation conditions. However, this power balance for AC/DC converters is only valid over each half line cycle. This basic difference between AC/DC and DC/DC operations implies that a large energy storage tank must be present in the PFC circuit to accommodate large changes of the instantaneous input power and to sustain adequate power to the output converter in order to keep the load voltage constant. Generally speaking, this energy storage tank could be composed of inductors or capacitors or both. In many practical circuits, however, energy stored in electric rather than magnetic form is preferred and usually one or more capacitors are adopted. The need for storage capacitors is shown in Fig. 1-2 as C_s. For some simple circuits, this C_s could be the output capacitor of the converters in Fig. 1-3.



(a) Buck converter



(b) Boost converter



(c) Buck-boost converter

Fig. 1-3. Three basic DC/DC converters.

Since power transferred from line to the storage capacitors varies sinusoidally and the load draws constant power from the capacitors, it is expected that voltage across the capacitors contains large secondary harmonic ripple. Very often, this voltage is very high and is also not in the right voltage level required by the load. To obtain a smooth and tightly regulated load voltage, an output stage DC/DC regulator is required, as shown in Fig. 1-2. Noted that the front-end PFC converter and the load converter are independent and are separately controlled, this type of AC/DC conversion configuration is called two-stage scheme.

Input current shaping method can be roughly classified into CCM and DCM approaches depending on the inductor current of the PFC converter. If, within each switching period, the inductor current always greater than zero, the PFC converter is said to operate in continuous conduction mode, or CCM. Otherwise, it operates in discontinuous conduction mode.

Figure 1-4 shows the line current waveform when a CCM boost circuit is adopted as the front-end PFC converter. There are a number of control methods to enable the line current to track the line voltage. In Fig. 1-4, inductor current $i_L(t)$ is controlled to be within two sinusoidal current command limits, high limit $i_{H,limit}(t)$ and low limit $i_{L,limit}(t)$. If $i_L(t)$ decreases below $i_{L,limit}(t)$, PFC converter controller turns on the switch to allow line voltage to charge the inductor. When the current reaches $i_{H,limit}(t)$, the controller turns off the switch. This type of control strategy is called hysteresis control with $i_{H,limit}(t)$-$i_{L,limit}(t) = k_1$ or $i_{H,limit}(t) = k_2\, i_{L,limit}(t)$, where k_1 and k_2 are constants ($k_2 > 1$). Obviously the inductor current charging and discharging time are changing with the line voltage, resulting in variable switching frequency control.

Variable frequency current control can also be achieved without high limit $i_{H,limit}(t)$ command (constant on-time control with $t_m - t_k = k$, k is a constant) or without low limit $i_{L,limit}(t)$ command (constant off-time control with $t_{k+1} - t_m = k$, k is a constant).

Variable frequency control makes input filter and closed-loop design difficult. A typical constant frequency control method is the peak current control. In Fig. 1-4, if $t_{k+1} - t_k = T_s$, T_s is the switching period and is constant, and also only the high current limit $i_{H,limit}(t)$ is used. Constant frequency peak current control suffers from a subharmonic

instability when the resulting charging time is greater than 50% of the switching period T_s. To avoid this problem, a stabilizing ramp with proper negative slope is required.

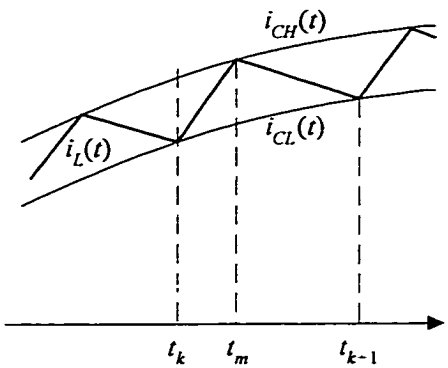


Fig. 1-4. Inductor or line current waveform in CCM for boost PFC converter.

Analysis and design of PFC converters employing these CCM methods to obtain unity power factor can be found in [24-36]. In [37-45] application of average current control and other CCM input current shaping techniques were also discussed.

Differences among these methods depend largely on how line current information is obtained. In addition to line current sensing, most of these methods also ask for sensing the line voltage to provide reference to the current command as shown in Fig. 1-2. It inevitably results in a complex control design.

The same PFC circuit can also achieve high power factor without resorting to the above complicated control loop design. This can be done by changing the operation mode of the PFC converter to DCM. In DCM operation, input energy transferred to the inductor when the switch is on is completely moved to the storage capacitors within each switching period. The peak inductor current is proportional to the line voltage when

charging time (or switch duty cycle) is fixed. The input current is now a train of high frequency triangular pulses whose average value over a switching cycle follows automatically and closely the line voltage as shown in Fig. 1-5 for the buck-boost example. Because of this "automatic" input current shaping property and simple feedback controller requirement, PFC converters employing DCM operation have been explored extensively and successfully and various topologies are available [22, 46-53].

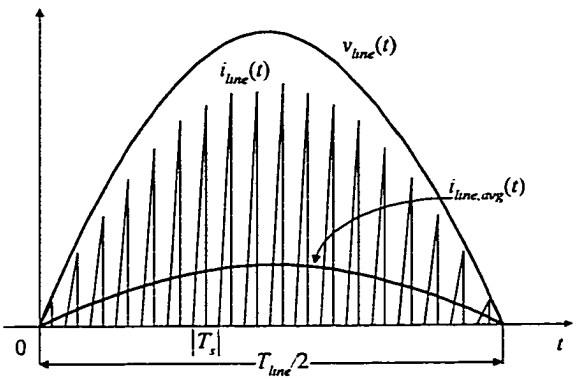


Fig. 1-5. Line current waveform of the DCM Buck-boost PFC circuit in a half line cycle.

It is seen from Fig. 1-2 that the two-stage scheme has separate controllers for the front-end PFC stage and the output DC/DC stage. The active switch in each power stage is controlled independently. In recent years research efforts have been made to combine these two stages and to allow a single active switch to be shared by both stages to reduce manufacturing cost. The underlined strategy of this consideration is to use one controller and one switch to perform both power factor correction and output voltage regulation. It is found that by proper arrangement of the storage capacitors the two active switches can

operate in unison and therefore their functions can be realized by one switch. Figure 1-6 shows the block diagram of this configuration which is usually referred to as the single-switch single-stage (S^4) scheme. Numerous S^4-PFC topologies have been reported and can be found in [20-22, 24-27, 29-32, 34-53]. Some typical S^4-topologies are shown in Figure 1-7 [22, 49].

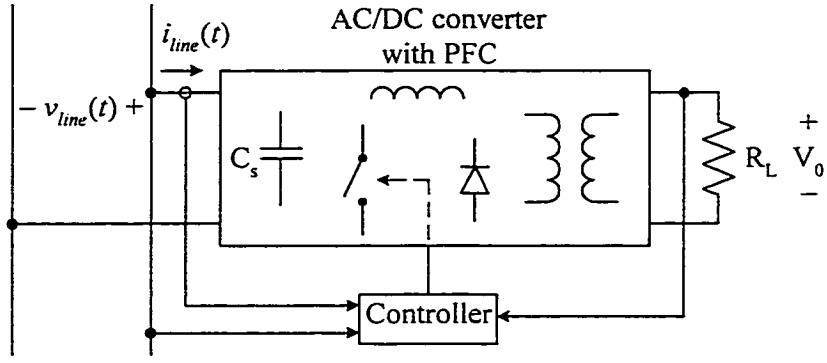


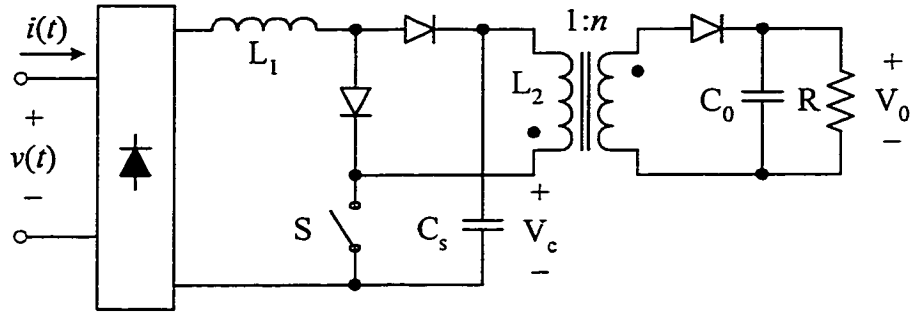
Fig. 1-6. Block diagram of the single-switch single-stage AC/DC converter with PFC.

It should be noted that since the active switch in S^4-PFC converters carries the total current previously handled by two separate switches in the two-stage scheme, requirement on the power handling capability of the switch is high. A common phenomenon associated with S^4-PFC converters is that the active switch suffers from a high voltage stress under high line and a high current stress under low line. High voltage stress is a result of high storage capacitor voltage and is also dependent on circuit operation modes. Since the PFC converter draws constant power from the line in each line cycle, switch current increases as line voltage decreases. The situation becomes even

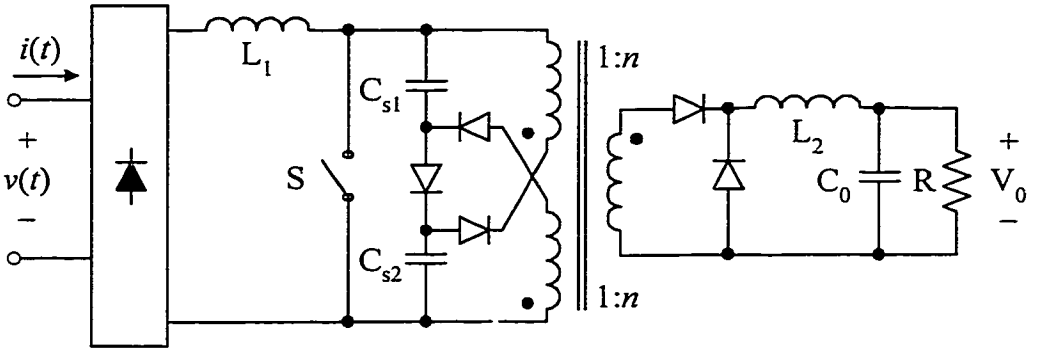
worse when PFC converters operate in DCM. Refer to Fig. 1-5, it is noticed that since inductor current is pulsating, the peak current flowing through the switch is at least twice the average inductor or line current. For this reason, S^4-PFC converters with DCM operation are only suitable for applications with power levels below a few hundred watts. At power levels greater than 1kW, CCM operation relying on more complicated control scheme becomes the dominant solution [24, 53].

1.3 Dissertation Outline

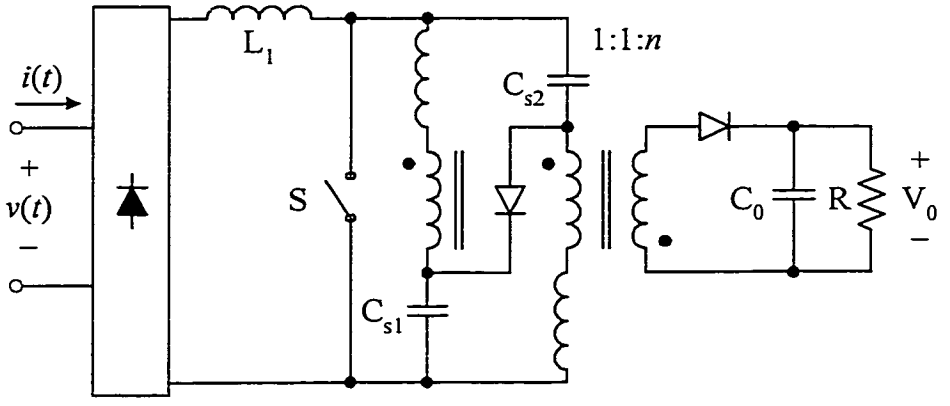
Power factor correction technique is an important research topic in power electronics. Chapter 2 will give an overview of the modeling techniques based on the average concept for switched-mode DC/DC converters. The harmonic and power factor properties of PFC converters will be studied in Chapter 3. Small signal behaviors of an S^4-PFC converter are first derived in Chapter 4 using the well-known state-space averaging method. The result is used as a reference to the PWM switch model to be derived in Chapter 5. An implementation error in the professional version of Pspice software for the conventional PWM model is first identified here and corrected as reported in Chapter 5. Improvement of this model under non-ideal conditions will also be described. The emphasis of this chapter is to introduce a new modeling approach based on the functionality of the inductors in deriving large-signal models for S^4-PFC converters. Application of the large-signal model for a specific PFC converter will be shown in Chapter 6. Summary and conclusions will be given in Chapter 7.



(a) Boost/flyback combination circuit



(b) Boost/forward combination circuit



(c) Boost/forward combination circuit

Fig. 1-7. Three typical S^4-PFC AC/DC converter topologies.

CHAPTER 2

AVERAGE MODELING TECHNIQUE OF DC/DC CONVERTERS

2.1 Introduction

Theoretically, switched-mode DC/DC regulators can be considered as a closed loop control system that consists of two functional blocks as shown in Fig. 2-1: power stage and feedback control circuit. The power stage, such as the three basic converters shown in Fig. 1-3, performs the energy transfer from the input source to the load. It can be operated either in DCM or CCM. The feedback control circuit can normally be characterized by an analog error compensator and a digital modulator. The error compensator is composed of an amplifier and a compensation network. It generates a voltage command signal according to the output voltage and/or inductor current that are to follow a preset reference value. The digital modulator is composed of a ramp signal generator, a comparator as well as a timing network to control the turn-on and -off of the active switch to achieve the controlled energy transfer in the power stage. For constant frequency pulse-width-modulation (PWM) control, this digital modulator is usually modeled as a constant gain.

It has been mentioned that the purpose of developing proper models for switched-mode converters is to study their dynamic behaviors with respect to external disturbances

and to allow sophisticated control theory to be applied to optimize converter responses. The difficulty in modeling switching converters arises from the inherently non-linear characteristics of the power converter. To most power supply design engineers, calculating and determining steady-state operation condition is not a problem and a unique operation point can always be found. However, predicting how circuit variables react with line/load changes and other disturbances is not easy. The answer is usually not unique either. Different techniques often predict different results and there are usually tradeoffs among accuracy, model complexity and the required computation time.

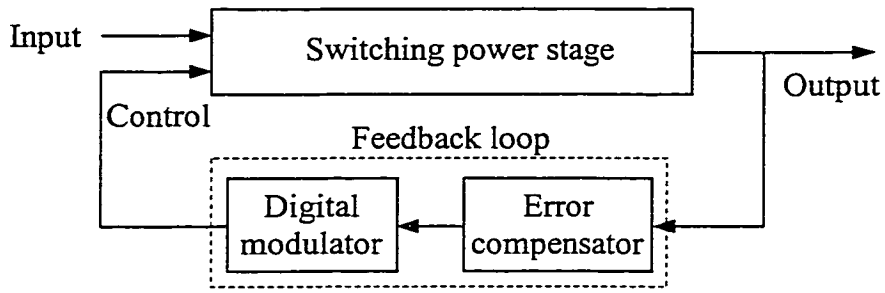


Fig. 2-1. General block diagram of a switched-mode DC/DC regulator.

In the past two decades, various modeling techniques have been reported. Most of them fall into two categories: discrete time-domain approach [54, 55] and averaging approach [56-58]. The operation of PWM converters is characterized by periodically changing topologies of a number of linear and time-invariant circuits. The discrete time-domain approach determines converter response by utilizing state-space equations and calculating transition matrix for each topology. It is an accurate method and is applicable

for any switching network. However, physical insight of the converter operation is unavailable and derivation of the expressions is complex and cumbersome.

On the other hand, averaging approach assumes that the time constant of the converter is much greater than the switching period and the converter's equivalent natural frequency is much smaller than the switching frequency. Fortunately, this condition is normally met in PWM converters. Although its accuracy degrades as the frequency of disturbing signals increases, derivation of the averaging model is much simpler than that of the time-domain model. In [59-61], it was shown that the increased error of the averaging approach at high frequency range is largely because of improper sampling of the output voltage with non-ideal output capacitors. By combining discrete time-domain and averaging techniques, it is possible to develop a model that is simple and accurate.

Of all the earlier approaches, the state-space averaging method [57, 58] developed by S. Cuk and R. Middlebrook in the 1970's was the most well known approach. It provided a generalized approach for a large class of PWM converters and has produced profound impact on the modeling and analysis of the DC/DC converters in the power electronics community. Since then, the concept of averaging has been explored extensively and lots of papers have been reported dealing with various improvements and theoretical foundations in average modeling [62-66, 71-77]. For example, more general models and extensions of the averaging technique that are not bounded to the small ripple condition were discussed in [71, 75, 76]. Among them, the three-terminal PWM switch model developed by V. Vorperian [62, 63] was an important contribution.

The state-space averaging and the PWM switch modeling are the most popular approaches currently being widely used by researchers and engineers in their study of stability and transient response of switching regulators. Although the PWM switch model greatly improved the modeling accuracy at high frequency range for DCM operating converters when compared with the state-space averaging, both approaches were based on the averaging concept. By averaging, detailed information about voltage and current waveforms, such as component voltage/current stresses, capacitor ESR effects, etc., are lost. In addition, both approaches give different models for converters operating in CCM and DCM. Basically it is unable to determine the operation modes simply by examining the average inductor current predicted from the model. To know whether the converter is in CCM or DCM or when the converter is going to change operation modes, power converter designers should go back to the actual switching circuit to check with the inductor current waveform. References [58] and [67] provide mathematical analysis governing converter operation modes under steady-state conditions based on circuit and operation parameters.

2.2 State-Space Average Modeling

The major idea of the state-space averaging method is to derive the dynamic behavior of the converter by averaging a set of linear state equations over a switching period. These state equations correspond to each topological structure the converter goes through in a switching period.

2.2.1 Continuous Conduction Mode

A classic PWM converter has two operation modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM, the instantaneous inductor current does not fall to zero at any time during the switching cycle, as shown in Fig. 2-2, where d is defined as the control duty cycle; whereas in DCM, the inductor current always start at zero at the beginning of each switching cycle and return to zero before the cycle ends. In CCM, the converter undergoes two topological changes. The state-space equations for each of these two structures can be described as ($\mathbf{x}$, $\mathbf{y}$ are state vector and output vector, respectively):

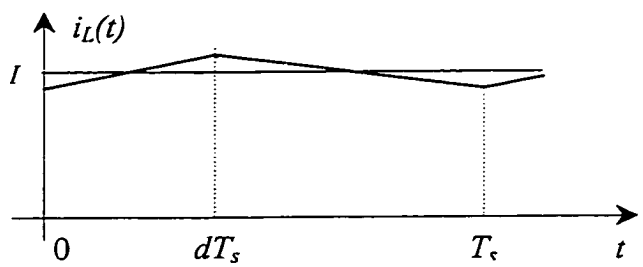


Fig. 2-2. Inductor current waveform in CCM operation.

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1 v_s, \quad \mathbf{y} = \mathbf{C}_1\mathbf{x} \qquad 0 \le t \le dT_s \tag{2.1}$$

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2 v_s, \quad \mathbf{y} = \mathbf{C}_2\mathbf{x} \qquad dT_s \le t \le T_s \tag{2.2}$$

The averaging technique suggests that these two state equations can be combined into one state equation by a set of state matrices **A**, **B** and **C** as follows,

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}v_s, \quad \mathbf{y} = \mathbf{C}\mathbf{x} \tag{2.3}$$

where v_s is the input voltage and,

$$\mathbf{A} = d\mathbf{A}_1 + (1\text{-}d)\mathbf{A}_2 \tag{2.4}$$

$$\mathbf{B} = d\mathbf{B}_1 + (1\text{-}d)\mathbf{B}_2 \tag{2.5}$$

$$\mathbf{C} = d\mathbf{C}_1 + (1\text{-}d)\mathbf{C}_2 \tag{2.6}$$

To obtain the system responses of the model described by Equations 2.3 to 2.6, we assume that the input voltage v_s and the duty cycle d are perturbed around their steady-state values such that $v_s = V_s + \hat{v}_s$, $d = D + \hat{d}$, which also cause the state vector and system output to deviate from their corresponding steady-state positions, namely $\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}$, and $\mathbf{y} = \mathbf{Y} + \hat{\mathbf{y}}$. Equation 2.3 can be written as:

$$\frac{d\hat{\mathbf{x}}}{dt} = \mathbf{A}\mathbf{X} + \mathbf{B}V_s + \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{v}_s + \left((\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_s\right)\hat{d} \tag{2.7}$$

$$\mathbf{Y} + \hat{\mathbf{y}} = \mathbf{C}\mathbf{X} + \mathbf{C}\hat{\mathbf{x}} + (\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}\hat{d} \tag{2.8}$$

Note that in obtaining the above expressions, it is assumed that the perturbations are significantly smaller than their respective steady-state values so that all the non-linear terms (multiples of perturbations) are neglected. Separating the steady state and the dynamic terms of the above linearized system results in the final state-space averaging model as given below:

- Steady-state model:

$$\mathbf{X} = -\mathbf{A}^{-1}\mathbf{B}V_s \tag{2.9}$$

$$\mathbf{Y} = \mathbf{C}\mathbf{X} = -\mathbf{C}\mathbf{A}^{-1}\mathbf{B}V_s \tag{2.10}$$

- Small-signal model:

$$\frac{d\hat{\mathbf{x}}}{dt} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{v}_s + \left((\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_s\right)\hat{d} \tag{2.11}$$

$$\hat{\mathbf{y}} = \mathbf{C}\hat{\mathbf{x}} + (\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}\hat{d} \tag{2.12}$$

In Equations 2.9 to 2.12, matrices **A**, **B** and **C** are calculated from Equations 2.4 to 2.6 by replacing d with its steady-state value D.

The significance of the small signal model as described by Equations 2.11 and 2.12 is that the frequency domain characteristic can be easily obtained using Laplace transformation. From the model, one can also derive an equivalent circuit model that provides a physical perception of the converter for design engineers.

Although the DC and the small signal model given by Equations 2.9 to 2.12 are derived from a converter with only two switching structures, this averaging approach also holds true for PWM converters with multi-topological structure changes, provided that the converter is working in CCM.

2.2.2 Discontinuous Conduction Mode

For converters working in DCM, the procedure of obtaining the DC and small signal model is basically the same as that shown above except that some modifications should be made. The major modification is the way the state variables are treated. In DCM operation, as can be seen in Fig. 2-3, the inductor current is fixed at zero at the beginning and end of each switching cycle even with small perturbations in the input and the control signal. It therefore no longer behaves as a valid state variable. This immediately reduces the order of the state-space representation and thus leads to an order-reduction dynamic model. The derivation of the model for this mode of operation is briefly summarized below.

When DCM operation is concerned, a classical PWM converter goes through three topological changes in stead of two as it does in CCM operation. Each topological stage corresponds to a different state equation. Namely,

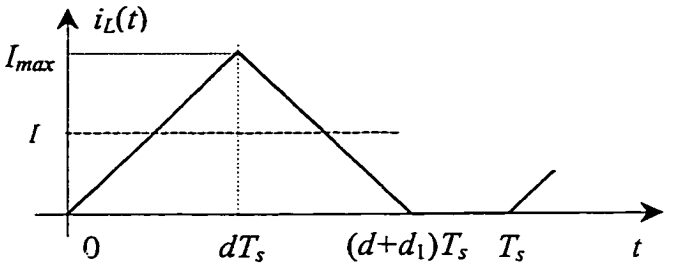


Fig. 2-3. Inductor current waveform in DCM operation.

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1 v_s \qquad 0 \le t \le dT_s \tag{2.13}$$

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2 v_s \qquad dT_s \le t \le (d + d_1)T_s \tag{2.14}$$

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_3\mathbf{x} + \mathbf{B}_3 v_s \qquad (d + d_1)T_s \le t \le T_s \tag{2.15}$$

Averaging the above state equations, we have,

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}v_s \tag{2.16}$$

where,

$$\mathbf{A} = d\mathbf{A}_1 + d_1\mathbf{A}_2 + (1 - d - d_1)\mathbf{A}_3 \tag{2.17}$$

$$\mathbf{B} = d\mathbf{B_1} + d_1\mathbf{B_2} + (1 - d - d_1)\mathbf{B_3} \tag{2.18}$$

Recall that in continuous conduction mode, Equation 2.16 was sufficient to describe the converter characteristic. Here for discontinuous conduction mode, it could not describe the switching converter completely since it does not take into account that the inductor current falls to zero before the next switching cycle begins. It seems that as a state variable, the inductor current $i_L(t)$ should respond to any perturbation in the input source or in the control duty cycle. On the other hand, the average current (defined as the integration of the inductor current over the time period when $i_L(t)$ is not zero) will fluctuate to accommodate any possible perturbations. Therefore, instead of using the inductor current as a state variable, we introduce the average of the inductor current as a new variable. It is obvious that,

$$i = \frac{I_{\max}}{2} = i(v_s, v_0, L, d, T_s) \tag{2.19}$$

where v_0 is the output voltage and L is the inductance.

From Equation 2.16, it is also obvious that the system behavior depends heavily on the controlled duty cycle d and the corresponding value d_1, which is unknown and needs to be determined. With the addition of Equation 2.19, all the circuit parameters and the DCM operating condition have been included. Thus the complete state-space averaging model for DCM operation is given by:

$$\frac{d\mathbf{x}}{dt} = \left(d\mathbf{A}_1 + d\mathbf{A}_2 + (1-d-d_1)\mathbf{A}_3\right)\mathbf{x} + \left(d\mathbf{B}_1 + d_1\mathbf{B}_2 + (1-d-d_1)\mathbf{B}_3\right)\mathrm{v}_s \qquad (2.20)$$

with two additional constraints:

$$\frac{di_L}{dt} = 0 \qquad (2.21)$$

$$i = \frac{I_{\max}}{2} = i(v_s, v_0, L, d, T_s) \qquad (2.22)$$

Follow the same procedure as that in CCM operation, the steady state and dynamic models for converters with DCM operation can also be obtained as:

- Steady-state model:

$$\mathbf{X} = -\mathbf{A}^{-1}\mathbf{B}V_s \qquad (1.23)$$

and

$$I = i(V_s,\ V_0,\ L,\ D,\ T_s) \qquad (1.24)$$

where **A** and **B** are obtained from Equations 2.17 and 2.18 by using steady state values D and D_1.

- Dynamic Model:

$$\frac{d\hat{\mathbf{x}}}{dt} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{v}_s + \left((\mathbf{A}_1 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_3)V_s\right)\hat{d} + \left((\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)V_s\right)\hat{d}_1 \tag{2.25}$$

and

$$\hat{i} = \frac{\partial i}{\partial v_s}\hat{v}_s + \frac{\partial i}{\partial v_0}\hat{v}_0 + \frac{\partial i}{\partial d}\hat{d} \tag{2.26}$$

2.3 Three-Terminal PWM Switch Modeling

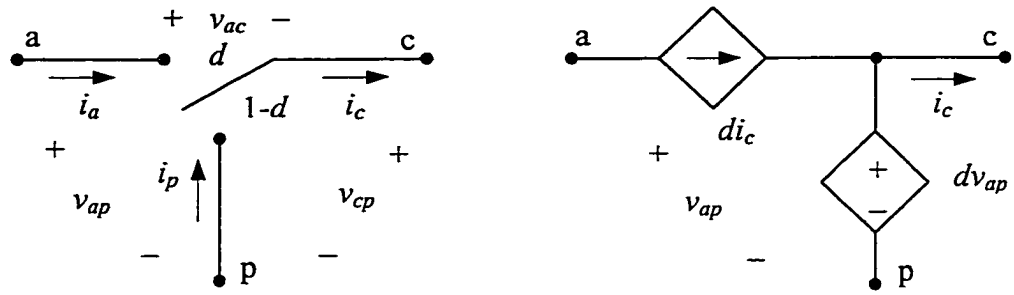
Unlike the systematic approach in the state-space averaging method where the derivation of the complete canonical circuit model and various transfer characteristics of a PWM converter relies on a considerable amount of matrix manipulations, the derivation of the PWM switch model solely follows a circuit oriented approach. The basic idea of this approach is to pick out the switches in the converter and to replace them with a proper equivalent circuit model. The whole process is analogous to the analysis of an amplifier circuit in electronics, where the nonlinear transistor is replaced by an h-parameter equivalent circuit. Once this is done, the amplifier can be analyzed using the well-established linear circuit analysis technique.

2.3.1 Continuous Conduction Mode

Investigation shows that the generation of classical PWM converters can be considered as a result of cyclic rotations of a three-terminal single-pole double-throw switch between the input and the output port [68]. This switch, as shown in Fig. 2-4(a), is normally implemented with an active switch and a passive switch, as is with the basic converters shown in Fig. 1-3. The active switch is usually implemented with a bipolar or a field-effect transistor whose turn on and off is directly controlled by the feedback circuit. The passive switch is usually a diode and its turn on and off is indirectly controlled by the state of the active switch and the converter topology. Since the three-terminal switch (called PWM switch with terminals a, p and c, which stands for active, passive and common, respectively) is the only nonlinear element in the converter, it is therefore responsible for the nonlinearity of PWM converters.

The averaging model of the PWM switch is shown in Fig. 2-4(b) for converters operating in CCM condition. It is obvious from Fig. 2-4(a) that current $i_c(t)$ is an independent variable and is controlled to flow either through terminal a or p. Similarly, voltage $v_{ap}(t)$ is independent since terminal a or p is connected to terminal c asynchronously. Therefore, it follows that,

$$i_a(t) = \begin{cases} i_c(t) & 0 \le t \le dT_s \\ 0 & dT_s \le t \le T \end{cases} \tag{2.27}$$



(a) a PWM switch (b) equivalent circuit model

Fig. 2-4. A PWM switch and its equivalent circuit model.

$$i_p(t) = \begin{cases} 0 & 0 \le t \le dT_s \\ i_c(t) & dT_s \le t \le T_s \end{cases} \tag{2.28}$$

and,

$$v_{cp}(t) = \begin{cases} v_{ap}(t) & 0 \le t \le dT_s \\ 0 & dT_s \le t \le T_s \end{cases} \tag{2.29}$$

$$v_{ac}(t) = \begin{cases} 0 & 0 \le t \le dT \\ v_{ap}(t) & dT_s \le t \le T_s \end{cases} \tag{2.30}$$

Average concept implies that the relationship among the average values of these variables must satisfy,

$$i_a = d\, i_c \tag{2.31}$$

$$i_p = (1\text{-}d)\, i_c \tag{2.32}$$

and

$$v_{cp} = d\, v_{ap} \tag{2.33}$$

$$v_{ac} = (1\text{-}d)\, v_{ap} \tag{2.34}$$

Using Equations 2.31 and 2.33 directly leads to the average circuit model of the PWM switch shown in Fig. 2-4(b). An equivalent form can also be obtained from Equations 2.32 and 2.34. It should be pointed out that the equivalent series resistance (ESR) of the output capacitor presents some impact on the terminal voltages. This impact can also be included into the model but a slight modification is required [62].

Figure 2-4(b) is actually the steady state circuit model of the PWM switch when all the variables are replaced by their corresponding DC values. Introducing perturbations into the terminal variables leads to the small signal model of the PWM switch.

Substitute in Equations 2.31 and 2.33 with $d = D + \hat{d}$, $i_a = I_a + \hat{i}_a$, $i_c = I_c + \hat{i}_c$, $v_{ap} = V_{ap} + \hat{v}_{ap}$, $v_{cp} = V_{cp} + \hat{v}_{cp}$, the perturbed terms then become as follows:

$$\hat{i}_a = D\hat{i}_c + I_c\hat{d}$$

$$\hat{v}_{cp} = D\hat{v}_{ap} + V_{ap}\hat{d} \tag{2.35}$$

This equation leads to a small signal model shown in Fig. 2-5.

As can be seen, with the PWM switch model, only the non-linear component represented by the three-terminal switch in a converter is considered. All the other elements are left untouched. This is in sharp contrast with the state-space averaging method where the whole circuit must be analyzed.

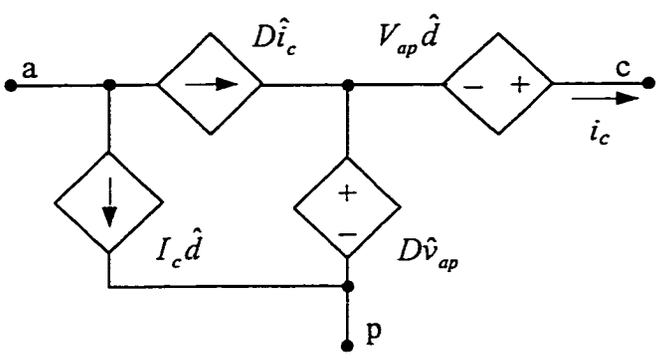


Fig. 2-5. Small signal model of the PWM switch.

2.3.2 Discontinuous Conduction Mode

For the three-terminal switch shown in Fig. 2-4(a), the model can also be developed similarly using the average concept when the converter is operating in DCM. Fig. 2-3 now represents the current in terminal c, i.e., $i_c(t)$. Current $i_a(t)$ is the portion of

$i_c(t)$ when $0 \le t \le dT_s$ and current $i_p(t)$ is the portion of $i_c(t)$ when $dT_s \le t \le (d+d_1)T_s$. Therefore, the average values can be written as:

$$i_a = \frac{dI_{\max}}{2} \tag{2.36}$$

$$i_p = \frac{d_1 I_{\max}}{2} \tag{2.37}$$

$$v_{ac} = \frac{LI_{\max}}{dT_s} \tag{2.38}$$

$$v_{cp} = \frac{LI_{\max}}{d_1 T_s} \tag{2.39}$$

These equations suggest that

$$v_{cp} = \mu v_{ac} \tag{2.40}$$

$$i_a = \mu i_p \tag{2.41}$$

$$\mu = \frac{d^2 T_s}{2L}\frac{v_{cp}}{i_a} = \frac{d^2 T_s}{2L}\frac{v_{ac}}{i_p} \tag{2.42}$$

The average model for the PWM switch described by Equations 2.40 to 2.42 is shown in Fig. 2-6.

Again, the steady-state model of the PWM switch in DCM can be obtained from Equations 2.40 to 2.42 or from Fig. 2-6 where all the variables are replaced by their DC values.

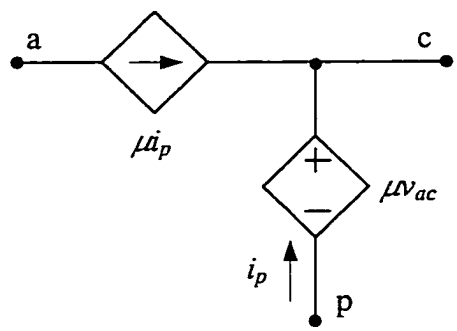


Fig. 2-6. The PWM switch model in DCM.

The small signal model is also obtainable through perturbation of Equations 2.40 to 2.42 and is given as:

$$\hat{i}_a = g_1 \hat{v}_{ac} + k_1 \hat{d} \tag{2.43}$$

$$\hat{i}_p = g_2 \hat{v}_{ac} + k_2 \hat{d} - g_3 \hat{v}_{cp} \tag{2.44}$$

where $g_1 = I_a/V_{ac}$, $g_2 = 2I_p/V_{ac}$, $g_3 = I_p/V_{cp}$, $k_1 = 2I_a/D$ and $k_2 = 2I_p/D$. The circuit representation of these two equations is given in Fig. 2-7.

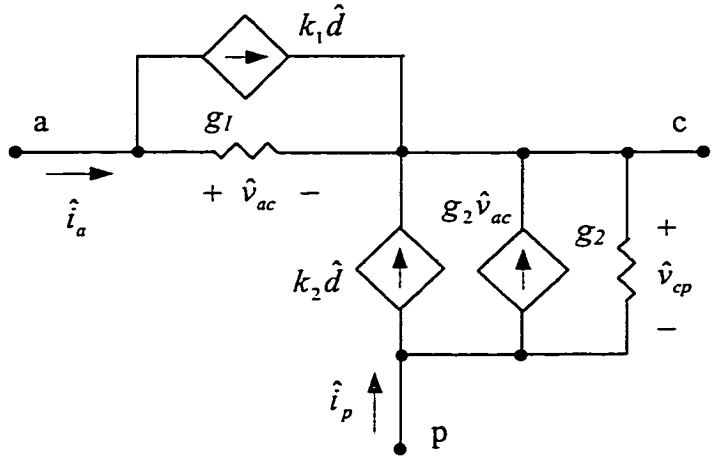


Fig. 2-7. Small signal model of the PWM switch in DCM.

As a final point, it should be mentioned that while use of CCM PWM switch model and the state-space averaging method yields the same results, for DCM operation, the conclusion is different. This is because the state-space average technique does not treat the discontinuous inductor current to be a state variable and hence results in a reduced order dynamic model. Whereas in PWM switch model, only the three-terminal switch is considered and linearized while all the other linear elements including the inductor with a discontinuous current are kept unchanged. The resulting linear circuit

model will certainly characterize the system with the same order as that when the converter is in CCM. The justification of this result can be found in [63].

2.4 The PWM Switch Model of the Flyback Converter and Weinberg Converter

2.4.1 The Flyback Converter

The flyback converter shown in Fig. 2-8 is chosen in this section as an example to show that the PWM switch modeling technique can also be applied to some converters that contain isolation transformers. Another reason is that a flyback structure can often be found in PFC converters either as the front-end PFC stage or the output stage. A PWM switch model developed here could be adopted directly in the modeling of PFC converters.

One of the obvious advantages of the PWM switch modeling approach is that the model automatically preserves the input-output property of the circuit such that there is no need for the users to concern about the output polarity. However, to keep this nice feature this approach may need some modifications when it comes with one or more isolation transformers in the converter circuit because of the polarity of the transformer. To add to the library of the well-documented models of the classical PWM converters, the models of the flyback converter is given in Fig. 2-9.

In Fig. 2-8, the "*" and "#" signs show the two possible dot notations (polarities) of a transformer connection and the diode with the sign indicates which direction the diode should be with the corresponding transformer polarity. The justification for the

dynamic model in Fig. 2-9(a) can be clarified by comparing its state-space equations with the averaged ones of the original converter shown in Fig. 2-8. The control coefficient μ for the DCM condition in Fig. 2-9(b) is given by,

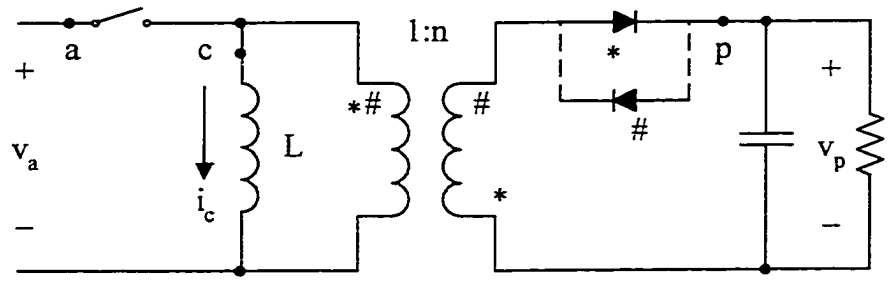


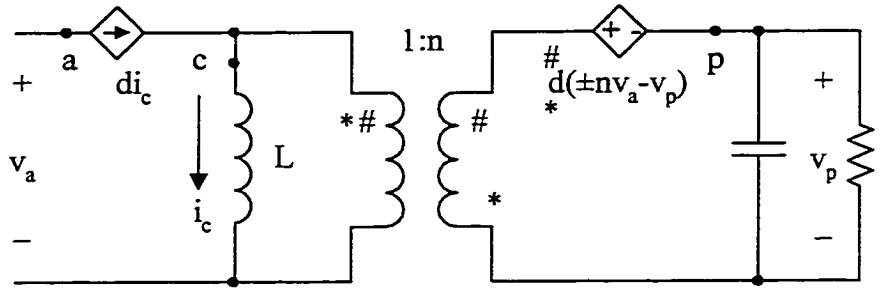
Fig. 2-8. Topology of the flyback converter.

$$\mu = \frac{d^2}{2Lf_s}\frac{v_{ac}}{i_p} \tag{2.45}$$

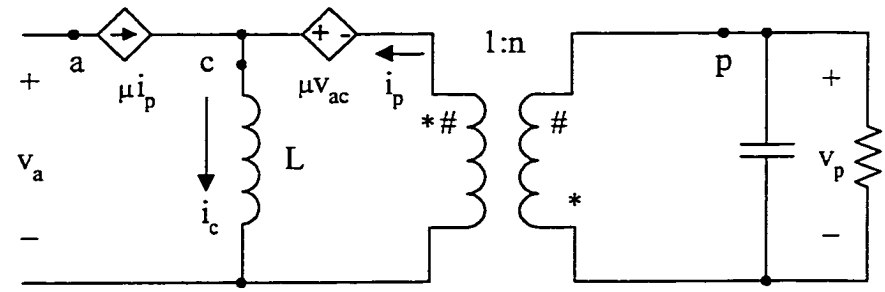
and,

$$d_1 = \frac{2Lf_s}{d}\frac{i_p}{v_{ac}} \tag{2.46}$$

In the above expressions, f_s is the switching frequency, d is the duty-cycle and d_1 is the relative time in a switching period the inductor current discharges to zero, respectively.



(a) CCM model



(b) DCM model

Fig. 2-9. PWM switch model of the flyback converter.

Next, Fig. 2-9(a) was taken to demonstrate that the transformer polarity does not affect the input output relation and the polarity information of the output voltage is contained in the model. Under steady-state condition, L is considered short and C is open, the following relation can be obtained from the circuit:

$$-d(\pm nv_a - v_p) = v_p \tag{2-47}$$

In the above expression, the "+" sign before nv_a corresponds to the transformer polarity indicated by "#". A transformer with this polarity should result in a negative output voltage v_p as is also predicted by the Equation 2-47 and the result is given as,

$$\frac{v_p}{v_a} = -\frac{+nd}{1-d} \tag{2-48}$$

2.4.2 The Weinberg Converter

The Weinberg converter is a cascade-input, parallel-output connection of the flyback converter and a transformer [69, 70]. This converter was adopted in the space station power supply systems. Figure 2-10 shows its simplified one-switch version. However, the model given in Fig. 2-11 can also be applied to the two-switch topology with minor modifications.

Justification of the average model in Fig. 2-11(a) can be understood by comparing the state-space equations of this model and the converter circuit (Fig. 2-10) following the steps outlined in Equations 2.1 to 2.6. Both give the same results as given below:

$$\begin{aligned} L\frac{di_L}{dt} &= -\left(\frac{1-d}{n} + \frac{d}{m}\right)v_0 + dv_s \\ C\frac{dv_0}{dt} &= \left(\frac{1-d}{n} + \frac{d}{m}\right)i_L - \frac{v_0}{R} \end{aligned} \tag{2.49}$$

Steady-state relations can be easily derived from Fig. 2-11(a). Consider,

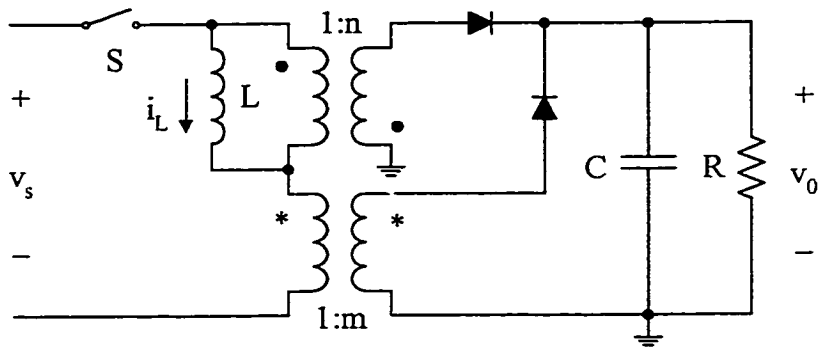
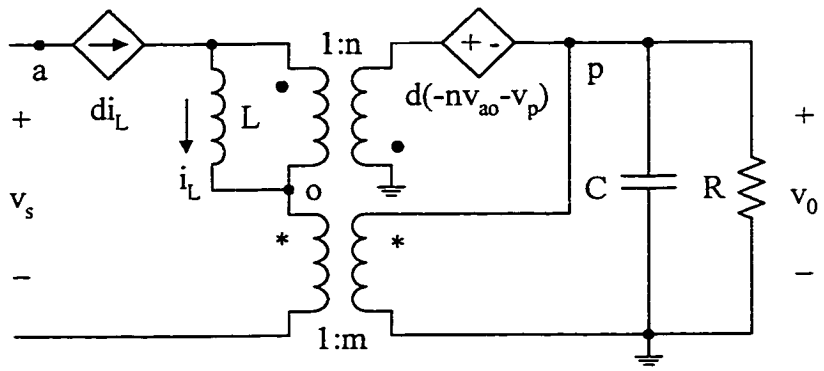
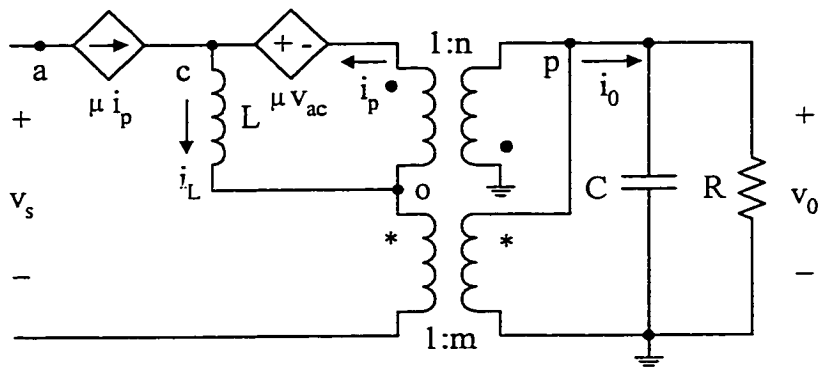


Fig. 2-10. Topology of the Weinberg converter.



(a) CCM model



(b) DCM model

Fig. 2-11. PWM switch model of the Weinberg converter.

$$V_{ao} = V_s - \frac{V_0}{m}$$

and,

$$V_0 + d(-nV_{ao} - V_0) = 0$$

The well-known voltage conversion ratio M for the Weinberg converter is obtained as:

$$M \triangleq \frac{V_0}{V_s} = \frac{d}{\frac{1-d}{n} + \frac{d}{m}} \tag{2.50}$$

For the DCM operation, Fig. 2-11(b) is also a very convenient model to derive steady-state voltage conversion ratio and critical condition governing the operation modes. The derivation process is given below:

$$I_0 = \frac{I_p}{n} + \frac{\mu I_p}{m}$$

or,

$$I_p = \frac{mn}{m + n\mu} I_0 \tag{2.51}$$

From Equation 2.45, we have,

$$\mu = \frac{D^2}{2Lf_s} \frac{V_s - \frac{V_0}{m}}{\frac{mn}{m+n\mu} I_0} = \frac{D^2}{k} \frac{m+n\mu}{mn} \left(\frac{1}{M} - \frac{1}{m} \right) \tag{2.52}$$

In Equation 2.52, M is the conversion ratio and k is defined as,

$$k \triangleq \frac{2Lf_s}{R} \tag{2.53}$$

Consider also,

$$V_0 = n\mu V_{ac} = n\mu \left(V_s - \frac{V_0}{m} \right)$$

or,

$$\mu = \frac{mM}{n(m-M)} \tag{2.54}$$

From Equations 2.52 and 2.54, we obtain,

$$M = \frac{D\left(\sqrt{D^2 + 4km^2} - D\right)}{2km} \tag{2.55}$$

Notice that in the above equation, M is independent of n.

The relative time D_1 for the inductor current to drop to zero can be determined from Equations 2.46 and 2.54:

$$D_1 = \frac{2Lf_s}{D}\frac{I_p}{V_s - \frac{V_0}{m}} = \frac{n\left(\sqrt{D^2 + 4km^2} - D\right)}{2m} \tag{2.56}$$

By letting D_1=1-D, the converter enters a critical operation mode where it operates at the edge of CCM and DCM. A critical circuit parameter defined in Equation 2.53 should satisfy the following expression for this operation mode:

$$k_{crit} = \frac{1-d}{n}\left(\frac{1-d}{n} + \frac{d}{m}\right) \tag{2.57}$$

2.5 Challenges in Modeling PFC Converters

While state-space averaging technique has been proven in the past to be a powerful tool for a large family of PWM converters, it breaks down when applied to resonant and multi-resonant converters. As has been shown in Section 2.2, the averaging process requires considerable amount of algebraic manipulations even for non-resonant power converters.

On the other hand, the three-terminal device method provides another alternative to model PWM converters following a circuit oriented approach. It is much simpler to use than the state space averaging approach for classical PWM converters in that only the nonlinear parts, i.e., the switches, are considered. Efforts were also devoted to apply this method in the modeling of resonant converters [73, 74]. However, the generalized application of this approach is restricted by its topological requirement; namely, an active switch and a passive switch be electrically connected together to form a three-terminal PWM switch. Even with a simple isolation transformer the PWM switch model would present a very different form as has been demonstrated in Figs. 2-8 and 2-9 with the flyback converter. In many of today's power electronic circuits, more complex structures and switch arrangements are readily observed and more complicated switching relations are present, as for the Weinberg converter circuit and particularly for PFC circuits. Because of the unpredictable number of switches (active and/or passive) that do not necessarily form PWM switches in the power stage and the complicated topological structure changes in a switching cycle, modeling of PWM power converter using the three-terminal device technique becomes very difficult. Specifically, for S^4-PFC converters, there is only one active switch and normally more than one passive switch, as can be noticed in Fig. 1-7. This situation, plus the presence of transformers, often makes it difficult to conceptualize a PWM switch. Unfortunately, very few papers have been reported on this challenging subject and therefore it remains an area to be developed. In [65], the authors successfully applied the PWM switch concept to converters with multiple separated active and passive switch pairs. However, method used there was only valid when the converter operated in continuous conduction mode. A loss-

free resistor (LFR) averaged model, which is similar to the PWM switch model, was also applied to simple DC/DC and PFC circuits with separated switches for CCM and DCM operation [79]. Again, the model also asks for an active switch to be with a passive switch. Another effort devoted to the modeling of a ZVS phase-controlled PWM converter using the averaged PWM switch model was carried out in [74] where the effective switching action of the active and passive switches is equivalent to a single PWM switch.

Another challenging issue in the dynamic modeling of PFC converters arises from the fact that the conversion ratio widely changes within each half-line period and the steady state operation point fluctuates at double the line frequency. Although the averaged modeling technique was not established vigorously on a theoretical basis, for switched-mode DC/DC converters, at least a fixed steady-state operation point can be found with this technique. Under a small ripple assumption, this steady-state point is actually very close to that of the actual converter. Perturbation around this point gives meaningful results in terms of small-signal transfer functions, input and output impedances.

However, in PFC converters the line voltage changes sinusoidally and a "steady-state" operation point exists only in the sense of a line cycle but not in the sense of a switching cycle. The meaningfulness of small-signal characteristics of PFC converters is questionable as the converter operation is actually under a large signal environment. For example, the output voltage of a PFC converter inevitably contains noticeable second order line harmonic AC component because of the rectified line voltage applied at the front-end PFC stage. It is impossible to distinguish what percentage of this output voltage ripple is the result of a small perturbation signal overriding on the top of the line voltage with the same

frequency. On the other hand, systematic design of PFC converter systems requires complete knowledge about dynamic characteristics of the power stage in order to make full use of the sophisticated feedback control theory. To solve this dilemma, some research results [47, 78] showed that the steady-state of PFC converters may be approximated by replacing the rectified AC input by a DC source with its magnitude equals the *rms* value of the AC line. Small signal analysis can then be performed similar to that in a DC/DC converter. Obviously, more theoretical investigation is needed to justify the approach.

CHAPTER 3

POWER FACTOR AND HARMONICS IN PWM CONVERTERS

3.1 Introduction

As has been described in Chapter 1, switched-mode DC/DC converters have widely been used as the front-end circuits to perform power factor correction and to reduce line frequency harmonics. By employing high frequency switching technique, the input current becomes a sinusoidal waveform that is in phase with the line voltage but is superimposed by many high frequency components.

In the past few years, various aspects regarding design and optimization of PFC converters have been discussed and hundreds of new topologies can be found in the open literature. For low-power, low-cost applications the DCM operation mode is often preferred in order to simplify the control. In DCM, the line voltage is only allowed to charge the input inductor of the PFC circuit for a fixed portion of a switching cycle and the energy absorbed by the PFC circuit is completely transferred to the output before the next switching cycle begins. The input current is pulsating triangular waveforms as shown in Fig. 1-5.

It is interesting to note that almost all PFC converters utilize only a few common front-end input structures and they can be classified into three categories: buck, boost and

buck-boost. The input properties of these basic types of PFC circuits with respect to power factor and harmonic characteristics maybe understandable qualitatively to many power supply designers. However, they have not been fully explored quantitatively. These characteristics are valuable information to PFC converter designers in choosing the right topology and designing reasonable operation conditions to meet their design specifications. In this chapter, the power factor and harmonic levels of the above mentioned basic PFC circuits operating in DCM are analyzed and evaluated. Simulation and experimental results to verify the theoretical analysis will be provided.

3.2 Definition of Power Factor and Total Harmonic Distortion

Power factor is a basic but important concept in power engineering. To an electric or electronic consumer, the power factor represents the percentage of equipment's electric capacity has been utilized to converter electric energy into other forms. To a power system, the power factor represents the percentage of how much energy the system can provide has actually been absorbed by consumers. A high power factor means high utilization of the system capacity, less energy bouncing in the system and more loads be allowed to connect to the system. Definition of power factor (*pf*) can be find in any engineering textbook as:

$$pf = \frac{P}{S} \tag{3.1}$$

P-real or active power, S-apparent power.

For a linear load that draws sinusoidal current from the power system, it is well known that $pf=\cos\theta$, where θ is the phase difference between the voltage and current.

For a nonlinear load, however, things will be different. In this situation, voltage and current waveforms deviate from a sinusoidal wave and contain harmonics. They can be expressed as:

$$v(t)=\sum_{n=1}^{\infty}\sqrt{2}V_n\sin(n\omega t+\phi_n)$$
$$i(t)=\sum_{n=1}^{\infty}\sqrt{2}I_n\sin(n\omega t+\varphi_n) \tag{3.2}$$

With this voltage and current, the power factor defined in Equation 3.1 becomes,

$$pf=\frac{\sum_{n=1}^{\infty}V_nI_n\cos(\phi_n-\varphi_n)}{\sqrt{\sum_{n=1}^{\infty}V_n^2}\sqrt{\sum_{n=1}^{\infty}I_n^2}} \tag{3.3}$$

For switched-mode PFC converters, current waveform is actually in phase with the line voltage when high switching frequency components have been filtered out, as is shown in Fig. 1-5. If we consider that with proper harmonic control, voltage distortion becomes negligible, Equation 3.3 can be simplified as:

$$pf = \frac{I_1}{\sqrt{I_1^2 + I_2^2 + \ldots + I_n^2 + \ldots}} = \frac{1}{\sqrt{1 + \frac{1}{I_1^2}\sum_{n=2}^{\infty} I_n^2}} \tag{3.4}$$

The above expression shows that by assuming sinusoidal voltage, the power factor of switched-mode PFC converters are solely determined by fundamental and harmonic currents. Notice that the "Σ" over I_1 term in the expression is defined as the square of *Total Harmonic* (current) *Distortion* factor (THD_i), or,

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} = \sqrt{\sum_{n=2}^{\infty} DFI_n^2} \tag{3.5}$$

$$pf = \frac{1}{\sqrt{1 + THD_i^2}} \tag{3.6}$$

where DFI_n is the *nth* harmonic current distortion factor.

3.3 Power Factor and Harmonic Current Distortion of Basic PFC Circuits

As mentioned before, large storage elements are required to compensate for the inequality between the instantaneous input and output power. In many applications, the output capacitor of the buck, boost and buck-boost converters can be used for this purpose when these converters are utilized as the front-end PFC circuits. In the following

analysis, it should be understood that voltage V_c is the equivalent voltage across the storage capacitors (if more than one capacitor is present in some schemes) that is responsible for discharging the inductor current. Also, resistor R_L represents the loading effects of the output DC/DC stage and inductor L the main energy transfer element in the front-end stage.

To achieve high quality input characteristics for PFC circuits operating in DCM condition, the average line current within each switching cycle should follow closely the line voltage. Design guidelines suggest that the main power switch be turned on for a fixed time in each switching period. This time is determined by the control circuit such that the desired amount of power can be transferred to the output. This simple control scheme often results in satisfactory power factor in many designs. For buck-boost PFC circuit and its variations, an exact sinusoidal input current can even be obtained after high frequency components are filtered out, as is shown in Fig. 1-5. However, for buck and boost PFC circuits, harmonic currents are present in the input current and they are dependent on circuit operation conditions. These relations are to be revealed analytically. In the following discussion, we also assume that the duty cycle D as defined in Fig. 3-1(b) is constant. In addition, since the switching frequency is much higher than the line frequency, line voltage applied to the front-end PFC stage is considered constant in a switching period.

3.3.1 Buck PFC Circuit

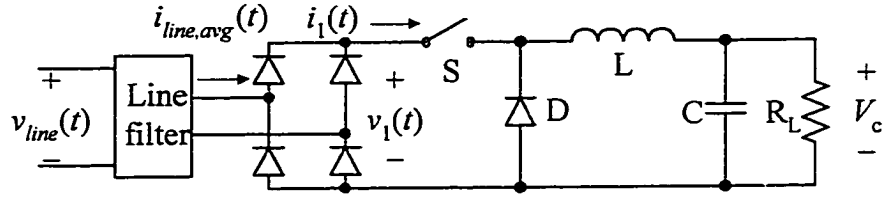
The circuit topology and its input current (or rectified line current) waveform in a switching period is shown in Fig. 3-1. Assume $v_{line}(t) = \sqrt{2}V_{in}\sin\omega_l t$, where V_{in} and ω_l are the *rms* value of the line voltage and line fundamental angular frequency, respectively. From Fig. 3-1, the periodical averaged line current is,

$$i_{line,avg}(t) = \begin{cases} i_l(t), & \sin^{-1}\dfrac{V_c}{\sqrt{2}V_{in}} < \omega_l t < \pi - \sin^{-1}\dfrac{V_c}{\sqrt{2}V_{in}} \\ -i_l(t-\dfrac{T_l}{2}), & \pi + \sin^{-1}\dfrac{V_c}{\sqrt{2}V_{in}} < \omega_l t < 2\pi - \sin^{-1}\dfrac{V_c}{\sqrt{2}V_{in}} \\ 0, & otherwise \end{cases} \tag{3.7}$$

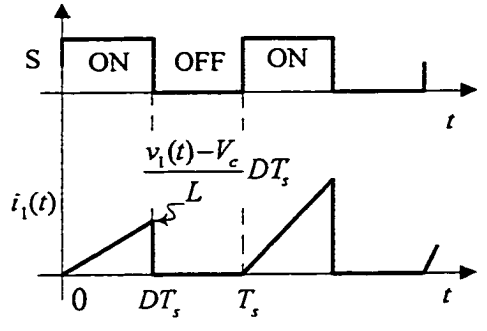
In the above expression, T_l is the period of the line voltage and $i_l(t)$ is the averaged switch current over a switching period T_s. It is given by,

$$\begin{aligned} i_l(t) &= \frac{D^2 T_s}{2L}(\sqrt{2}V_{in}\sin\omega_l t - V_c) \\ &= \frac{D^2 T_s}{2L}V_{in}(\sqrt{2}\sin\omega_l t - M) \end{aligned} \tag{3.8}$$

for $\sin^{-1}\dfrac{M}{\sqrt{2}} < \omega_l t < \pi - \sin^{-1}\dfrac{M}{\sqrt{2}}$, where M is the voltage conversion ratio and is defined as:



(a) Buck converter



(b) input current in a switching period

Fig. 3-1. Buck converter operating in DCM.

$$M = \frac{V_c}{V_{in}} \tag{3.9}$$

Note that proper operation of the buck converter requires that $M < \sqrt{2}$. Also, rectifier bridge does not allow nonzero input current when $|v_{line}(t)| < V_c$. Because of the periodical and symmetrical property of the averaged line current waveform, Fourier expansion gives,

$$i_{line,avg}(t) = \frac{D^2 T_s}{2L} V_{in} \sum_{n=1}^{\infty} (a_n \cos n\omega_1 t + b_n \sin n\omega_1 t) \tag{3.10}$$

with

$$a_n = b_{2n} = 0, \quad n = 1, 2, 3, \ldots$$

$$b_1 = \frac{\sqrt{2}}{\pi}(\pi - 2\theta - M\sqrt{2 - M^2}) \tag{3.11}$$

$$b_n = \frac{2\sqrt{2}}{\pi}\left(\frac{\sin(n+1)\theta}{n+1} - \frac{\sin(n-1)\theta}{n-1} - \frac{\sqrt{2}M\cos n\theta}{n}\right) \tag{3.12}$$

for $n = 3, 5, 7, \ldots$, where $\theta = \sin^{-1}\frac{M}{\sqrt{2}}$.

Total harmonic distortion factor of the input current THD_i and power factor of the PFC circuit pf can be calculated from Equations 3.11 and 3.12 according to the definition given in Equations 3.5 and 3.6. It is clear that pf and THD_i are only dependent on conversion ratio M. Figures 3-2 and 3-3 illustrate such relations. As can be seen, the main harmonic component of the buck PFC circuit is the third harmonic current, and as M increases, other harmonic components increase rapidly. Drastic distortion of the input current and poor power factor can be expected with large M, indicating that the buck converter is not a good circuit for DCM-PFC applications where large storage capacitor voltage is present.

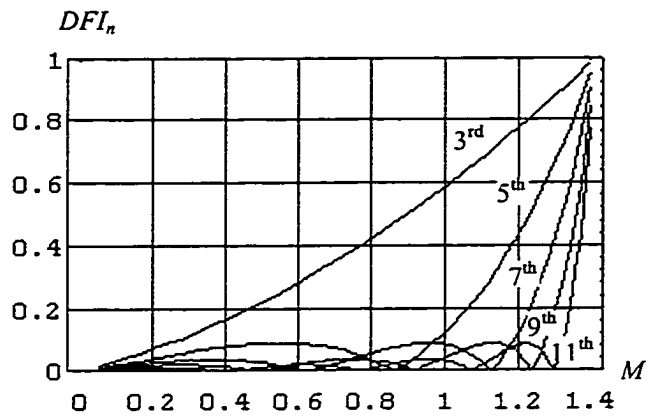


Fig. 3-2. Harmonic current distortion factor of the buck converter vs. conversion ratio.

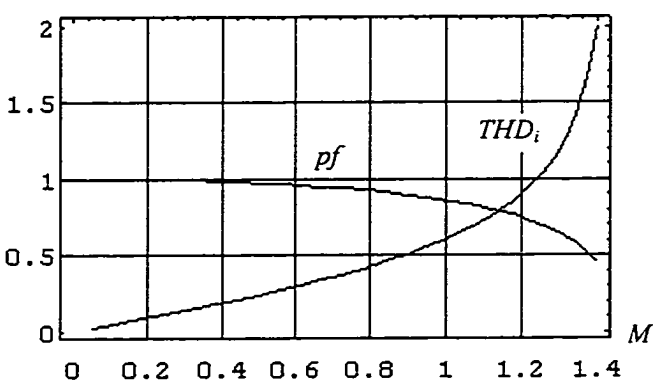
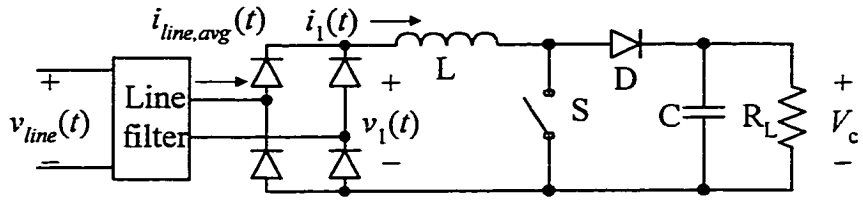


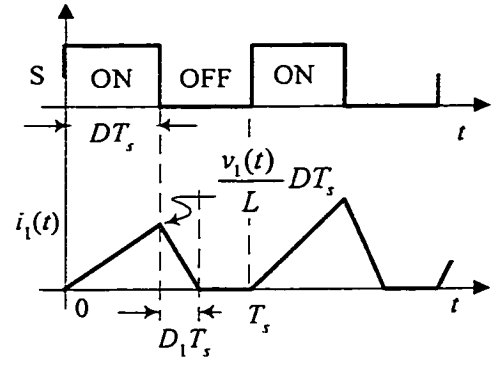
Fig. 3-3. Power factor and total harmonic distortion of the buck converter vs. conversion ratio.

3.3.2 Bocst PFC Circuit

Figure 3-4 shows the circuit topology of a boost converter and its input current waveform in a switching period. Similarly, the periodical averaged line current is:



(a) Boost converter



(b) input current in a switching period

Fig. 3-4. Boost converter operating in DCM.

$$i_{line,avg}(t) = \begin{cases} i_1(t), & 0 < \omega_1 t < \pi \\ -i_1(t - \frac{T_1}{2}), & \pi < \omega_1 t < 2\pi \end{cases} \tag{3.13}$$

Here $i_1(t)$ is the averaged inductor current over a switching period T_s and is given by,

$$i_1(t) = \frac{1}{T_s}\left[\frac{1}{2}(D + D_1)T_s \frac{v_{line}(t)}{L} DT_s\right]$$

$$= \frac{D^2 T_s V_c}{2L} \frac{\sqrt{2}\sin\omega_1 t}{M - \sqrt{2}\sin\omega_1 t} \tag{3.14}$$

For $0 < \omega_1 t < \pi$.

In Equation 3.14, M is also the voltage conversion ratio as defined in Equation 3.9. Once again, it is required that $M > \sqrt{2}$ for proper operation of the PFC circuit. From this equation it is clear that if M is much larger than 1.5, the averaged inductor current, or the rectified input current will be much closer to a rectified sinusoidal waveform, hence a near unity power factor can be obtained.

Fourier expansion of the periodical averaged line current waveform gives,

$$i_{line,avg}(t) = \frac{D^2 T_s}{2L} V_c \sum_{n=1}^{\infty} (a_n \cos n\omega_1 t + b_n \sin n\omega_1 t) \tag{3.15}$$

Again symmetrical property of the waveform ensures that $a_n = 0$, $b_{2n} = 0$ ($n = 1, 2, \ldots$). Other Fourier coefficients can be obtained as:

$$b_1 = \frac{2\sqrt{2}}{\pi}\left[-\sqrt{2} - \frac{\pi}{2}M + f(M)\right] \tag{3.16}$$

$$b_3 = \frac{2\sqrt{2}}{\pi}\left[\frac{2\sqrt{2}(6M^2-1)+3\pi M(2M^2-1)}{6} - (2M^2-3)f(M)\right] \tag{3.17}$$

$$b_5 = \frac{2\sqrt{2}}{\pi}\left[\frac{\sqrt{2}(-3+70M^2-60M^4)}{15} + \frac{\pi M(-1+6M^2-4M^4)}{2} - (-5+10M^2-4M^4)f(M)\right] \tag{3.18}$$

$\vdots$

where $f(M) = \dfrac{M^2(\pi + 2\tan^{-1}\sqrt{2}/\sqrt{M^2-2})}{2\sqrt{M^2-2}}$.

The effects of how conversion ratio affects the input power factor and harmonic contents in the line frequency range are demonstrated in Figs. 3-5 and 3-6. As can be seen, harmonic distortion in the averaged line current for the boost circuit is much smaller than that for the buck circuit in PFC applications. A near unity power factor ($pf >$ 0.99) can easily be obtained with the boost circuit when $M > 3$. The small distortion in the input current is caused by the existence of $D_1 T_s$ required to discharge the inductor current (Fig. 3-4). The higher the output voltage, the faster the inductor current reduces to zero and therefore the averaged input current over a switching period is more closely proportional to the line voltage. On the other hand, achieving small input current distortion is at the expense of increasing voltage stress on the storage capacitor, thus

requiring larger voltage rating capacitors. Fortunately there exists effective solutions to this problem as for the one to be discussed in the next chapter. Boost converter topology and many other converters adopting boost as their input stage such as Cuk, Sepic, are the most popular ones being utilized for PFC applications.

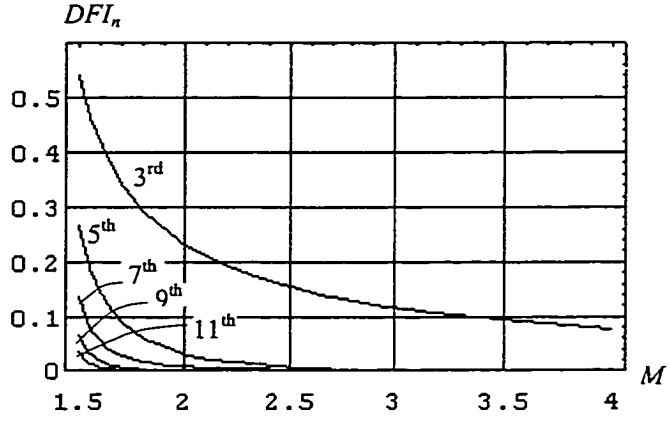


Fig. 3-5. Harmonic current distortion factor of the boost converter vs. conversion ratio.

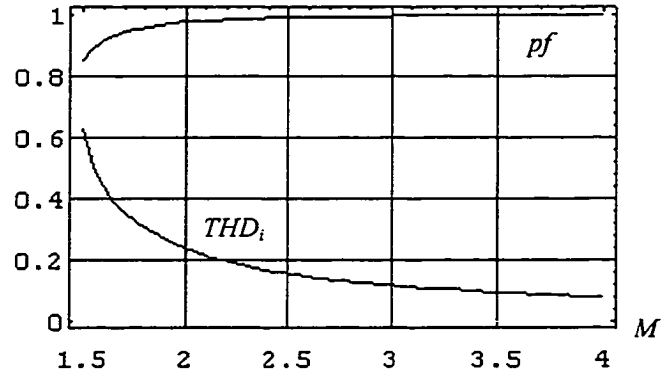
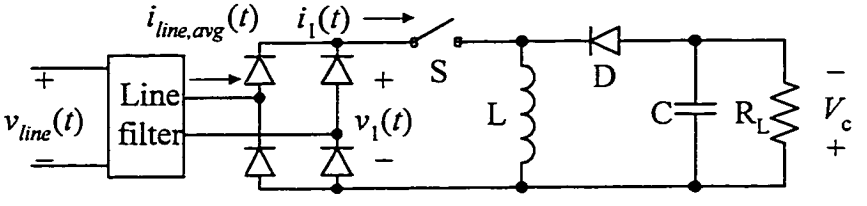


Fig. 3-6. Power factor and total harmonic distortion of the boost converter vs. conversion ratio.

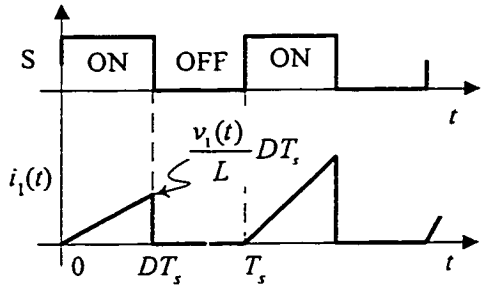
3.3.3 Buck-boost PFC Circuit

The circuit topology and input current waveform of the buck-boost circuit operating in DCM is shown in Fig. 3-7. In this case the input current in each switching period is equal to the inductor current when the switch S is ON. Therefore the periodical averaged input current can be calculated below:

$$i_{line,avg} = \frac{1}{T_s}\frac{1}{2}DT_s\frac{v_{line}(t)}{L}DT_s = \frac{D^2T_sV_{in}}{\sqrt{2}L}\sin\omega_l t, \quad 0 \le \omega_l t < 2\pi \tag{3.19}$$



(a) buck-boost converter



(b) input current in a switching period

Fig. 3-7. Buck-boost converter operating in DCM.

Equation 3.19 shows that the buck-boost circuit does not introduce harmonic distortions to the line current and hence is perfect for PFC applications. It also does not impose any limitation on the magnitude of the storage capacitor voltage for proper operation of the circuit. It forms a resistive emulator to the AC source. This excellent input property enables designers to concentrate on other issues such as voltage regulation and transient performance without worrying about power factor and harmonics on the input side.

3.4 Output Voltage of the PFC Stage

From the above discussion, it is clear that power factor and harmonic contents of a PFC converter is solely determined by the voltage conversion ratio of the front-end PFC stage when it operates in DCM. Obtaining a proper storage capacitor voltage needs to consider the PFC stage and the output stage. In DC/DC applications, voltage conversion ratio of basic DC/DC converters are functions of control duty ratio D (CCM), or functions of $d(t)$, circuit parameters as well as load conditions (DCM). For S^4-PFC converters, however, the storage capacitor needs to store sufficient energy to accommodate varying input power and to sustain constant power to the load. It will be heavily dependent on circuit parameters and operation modes of both stages. In many cases, the control duty ratio D is no longer a determining factor for this voltage but is only an operation parameter governing the operation modes for both stages. The storage capacitor voltage is predictable but it takes a quite different form from the DC/DC situations.

Take the Boost/flyback combination PFC circuit of Fig. 1-7(a) as an example. When both stage operate in DCM, applying power balance between input and output within a half line cycle results in the following expression [22]:

$$\frac{4}{T_1}\frac{V_{in}^2}{V_c}\frac{L_2}{L_1}\int_0^{T_1/2}\frac{\sin^2\omega_1 t}{V_c-\sqrt{2}V_{in}\sin\omega_1 t}dt=1 \tag{3.20}$$

This expression establishes a relation between the storage capacitor voltage and circuit parameters. It shows that the voltage conversion ratio is proportional to the inductance ratio between L_2 (magnetizing inductance of the transformer) and L_1 (choke inductance). A graphical presentation of this relation was also given in [22].

Unlike in the DC/DC boost converter where duty ratio is always present in the input-output relation, it does not appear in Equation 3.20. However, it should be noted that once inductors L_1, L_2 are determined, and hence V_c determined, the output voltage of the PFC converter V_0 is dependent on the duty ratio and load resistance as in a DC/DC flyback converter. Under steady-state operation,

$$V_0 = DV_c\sqrt{\frac{RT_s}{2L_2}} \tag{3.21}$$

To ensure that both stages operate in DCM, duty ratio and circuit parameters should satisfy the following conditions:

$$\frac{2n^2 L_2}{RT_s} < (1-D)^2 \tag{3.22}$$

$$\sqrt{2}V_{in} < (1-D)V_c \tag{3.23}$$

Figure 3-8 shows another single-switch PFC converter that consists of two flyback circuits. The flyback converter is the isolated version of the buck-boost converter and therefore it presents a unity power factor in PFC applications. When both stages operate in DCM, power balancing between input and output with a half line cycle gives [80]:

$$V_c = V_{in}\sqrt{\frac{L_2}{L_1}} \tag{3.24}$$

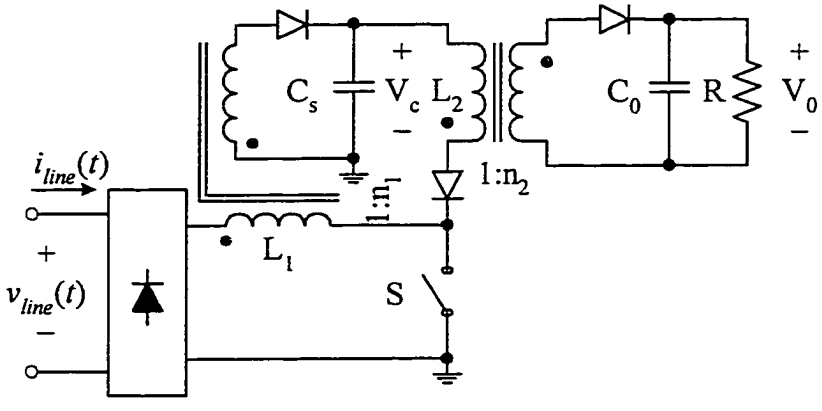


Fig. 3-8. A flyback/flyback combination PFC circuit.

Although this expression is quite different from Equation 3.20 and is much simpler, they both reveal that voltage across storage capacitors is only dependent on the input voltage and inductance of the front-end and output stages and is independent of duty ratio. It is also noted that the capacitor voltage is also independent of the load conditions. As a matter of fact, it is a common property for S^4-PFC converters that the capacitor voltage does not change with varying load current provided that both stages are in DCM [22, 81].

Even though the control duty ratio does not affect the voltage across storage capacitors, it does affect the output voltage and determine whether expressions 3.20 and 3.24 are valid or not. Therefore circuit and operation parameters should be properly designed to ensure both stages operate in DCM.

For the PFC converter shown in Fig. 3-8, output voltage is also given by Equation 3.21 since the output stage of both converters uses the flyback topology.

To ensure that both stages operate in DCM, duty ratio and circuit parameters should satisfy:

$$\frac{2n_2^2 L_2}{RT_s} < (1-D)^2 \tag{3.25}$$

$$2n_1^2 D^2 L_1 < (1-D)^2 L_2 \tag{3.26}$$

The output stage of the PFC converters can also operate in CCM. For the boost/flyback combination circuit, voltage across storage capacitors in this operation mode is given by,

$$2RT_s V_c V_{in}^2 \int_0^{T_1/2} \frac{\sin^2 \omega_1 t}{V_c - \sqrt{2} V_{in} \sin \omega_1 t} dt = T_1 L_1 (nV_c + V_0)^2 \tag{3.27}$$

Unlike in Equation 3.20 where the voltage conversion ratio depends only on inductance of the choke inductor and the transformer, output voltage and load information appear in Equation 3.27, which means that the storage capacitor voltage changes with load variations when the output stage operates in CCM.

For the flyback/flyback combination circuit with CCM operation on the output stage, the storage capacitor voltage is given by [80],

$$V_c = \frac{1}{n_2}\left(V_{in} \sqrt{\frac{RT_s}{2L_1}} - V_0 \right) \tag{3.28}$$

For the converter to operate in this mode, it is required that circuit parameters satisfy,

$$\sqrt{2} n_1 D V_{in} < (1 - D) V_c \tag{3.29}$$

$$2n_2^2 L_2 > RT_s(1-D)^2 \tag{3.30}$$

Once again it is noticed that when the output stage operates in CCM, voltage across the storage capacitor is a function of the output voltage and the load resistance. It is further noticed that this voltage increases with decreasing load current when the load voltage is kept constant. This conclusion, though not so obvious from Equation 3.27, is also generally applicable to all S^4-PFC converters with their front-end stage in DCM and output stage in CCM.

The above discussion suggests that although power factor and harmonic contents of PFC converters depends on capacitor voltage conversion ratio, selecting proper capacitor voltage is subjected to converter operation constraints and is also topological dependent.

3.5 Verification of the Power Factor and Harmonic Current Distortion in Basic PFC Circuits

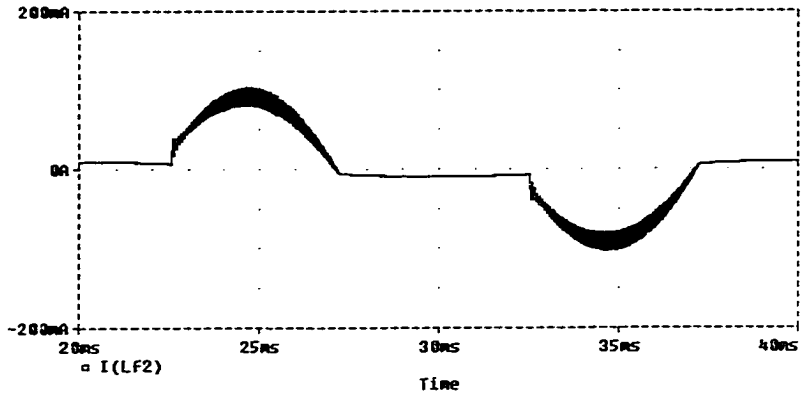
The three basic converter topologies as discussed in Section 3.3 were simulated when they are utilized as the PFC input circuits. The simulation was conducted when these circuits were operated in DCM conditions with a 110V (*rms*) AC input and a switching frequency of 50kHz. Figures 3-9(a), 3-9(b) and 3-9(c) show the simulated input current waveforms when most of the high frequency switching components have been filtered out by an EMI filter. Voltage conversion ratio is also given in the figure.

Harmonic analysis for these waveforms shows that current harmonic contents agree very well with theoretical predictions given by Fig. 3-2, Fig. 3-5 and Equation 3.19. Table 3-1 lists these results for comparison.

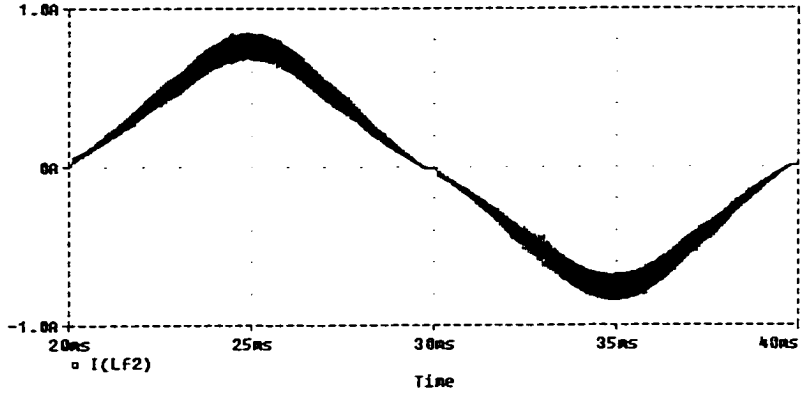
A power factor correction converter with a 50V, 50W output as shown in Fig. 1-7(c) was also implemented to verify the theoretical analysis. As can be noticed, the input stage is a boost circuit with two series storage capacitors as its output. The inductor currents in the PFC stage and the output stage both operate in DCM. Detailed analysis of this converter will be discussed in the next chapter. At 110V (*rms*) AC input, $V_{cs1}=V_{cs2}=191.5V$. Therefore, M can be calculated as $2\times191.5/110=3.48$.

The experimental input current waveform is shown in Fig. 3-10. Its harmonic content is measured and the result is also given in Table 3-1.

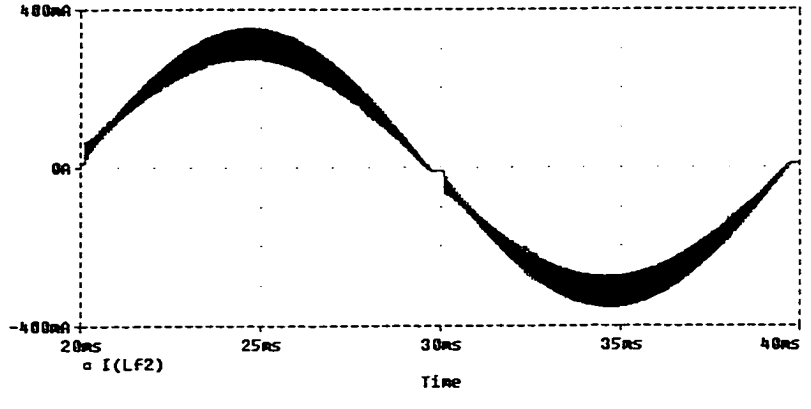
Table 3-1 shows excellent agreement between the measured harmonic contents for a boost input circuit and those obtained from theoretical analysis and simulated results, except for the 5^{th} and 9^{th} harmonic currents that are much larger. However their amount is much smaller than the dominant 3^{rd} harmonic content and is thus hard to be noticed in the THD value. The input current waveform still contains some high frequency components as can be observed in Fig. 3-10.



(a) Buck (M=1)



(b) Boost (M=3.48)



(c) buck-boost (M=1.82)

Fig. 3-9. Simulated waveforms of input currents drawn from the line source.

Table 3-1. Input harmonic current contents and power factors of the three basic PFC circuits

		DFI_3	DFI_5	DFI_7	DFI_9	THD_i	pf
Buck (M=1)	Theoretical	58.4%	11.7%	8.34%	3.89%	60.3%	0.856
	Simulation	58.2%	12.9%	8.24%	4.84%	60.4%	0.856
Boost (M=3.48)	Theoretical	9.37%	0.27%	0.22%	0.09%	9.37%	0.996
	Simulation	11.4%	0.51%	0.88%	0.44%	11.5%	0.993
	Experimental	10.5%	1.91%	0.87%	1.78 %	10.9%	0.994
Buck-boost (M=1.82)	Theoretical	0	0	0	0	0	1
	Simulation	0.57%	0.44%	0.40%	0.38%	0.91%	1

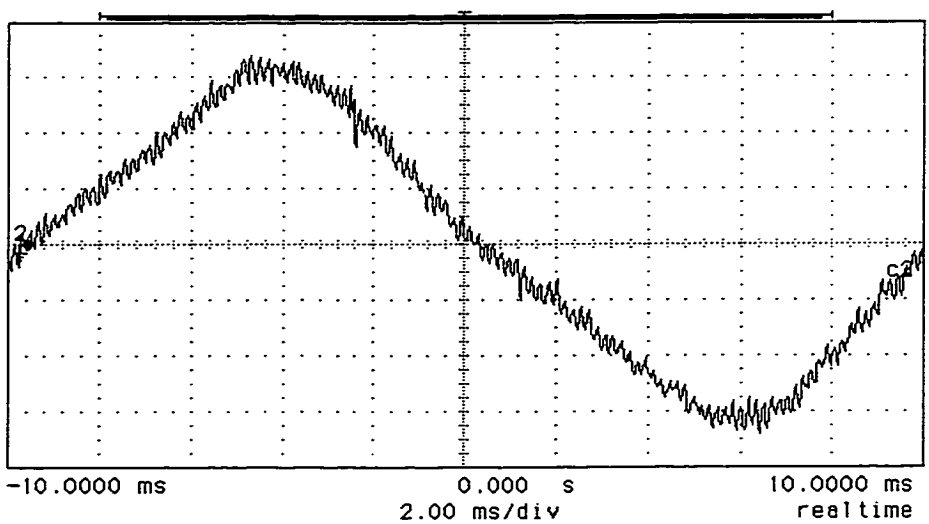


Fig. 3-10. Experimental input current waveform of an AC/DC converter (vertical scale: 0.25A/div).

3.6 Summary

Power factor and harmonic characteristics of three basic high frequency switched-mode PFC circuits operating in DCM conditions are discussed in this chapter. It is found that these characteristics are solely determined by the voltage conversion ratio of the PFC input stage in an AC/DC power supply system. This voltage conversion ratio is, however, dependent on both converter topology and operation mode of the output stage. S^4-PFC converters utilizing boost structures generate an intrinsic high voltage across the storage capacitor and the active switch. Some good PFC converter topologies produce lower voltage stress on capacitors and/or switches, but at the expense of degraded power factor and higher harmonics (except for using the buck-boost structure). On the other hand, the voltage conversion ratio is independent of load current and control duty cycle when the output stage also operates in DCM. This nice property enables selecting capacitors and switches with proper voltage ratings to be an easy task. When the output stage operates in CCM, voltage across storage capacitors becomes load dependent and increases drastically at light load, which may become the limiting factor in component selection. This capacitor voltage issue with respect to the operation mode of the output stage has been clarified analytically through two examples. Finally, the analytical result of this chapter enables power supply designers to select appropriate circuit topology and operation conditions to accomplish their design task. Theoretical predictions are verified by simulation and experimental results.

CHAPTER 4

SMALL-SIGNAL MODELING OF A SINGLE-SWITCH AC/DC PFC CIRCUIT BASED ON STATE-SPACE AVERAGING METHOD

4.1 Introduction

In this chapter, the steady state and dynamic characteristics of a one-switch PFC converter developed at the Applied Power Electronics Center at University of Central Florida will be studied. The circuit topology of this converter was shown in Fig. 1-7(c) to be a boost/forward combination circuit. Before going any further, a short glance at the topology of this PFC circuit reveals some interesting features. Some PFC circuits utilized a two-core configuration to provide input-output isolation and load voltage regulation, such as the flyback/flyback combination PFC circuit shown in Fig. 3-8. For the circuit to be discussed in this chapter, these two functions are accomplished by using only one forward type transformer. This greatly reduces the amount of energy circulating between the magnetic windings and thus more efficient energy conversion is expected. DCM operation of the boost input circuit further simplifies the circuit layout and control loop design.

As has been explained in Chapter 3, use of buck-boost and/or its derived forms as the PFC pre-regulator will theoretically generate a pure sinusoidal input current

waveform. For boost-type converters operating in DCM, the input current waveform deviates from a pure sinusoidal waveform depending on capacitor voltage conversion ratios. A storage capacitor voltage of at least three times the *rms* value of the line voltage is often required for a power factor greater than 0.99. This high voltage stress poses a serious problem in selecting proper capacitors, especially when the PFC circuit is to be used for a universal line input (88V to 264V, *rms*). However, this problem is solved elegantly in this converter by using two capacitors and a diode to form a series-charging, parallel-discharging switched-capacitor subcircuit. When this subcircuit is connected to the input section, these two capacitors are connected in series to discharge the input inductor. As a result, a much higher voltage is applied across the input choke inductor as compared with the case when only one capacitor is used. Thus the inductor current can be reduced to zero quickly after being charged to its maximum value during each switching period. In this manner, a high power factor is achieved without causing high voltage stress on the storage capacitors.

On the other hand, when the subcircuit is connected to the output section, a lower output voltage level can be sustained as these two capacitors are now in parallel. In fact, low level output voltage, low voltage stress on storage capacitors and high input power factor are often contradictory requirements in the designing of boost-type PFC converters. Use of the switched-capacitor circuit may achieve much better converter performance. This idea was first introduced by R. D. Middlebrook [82] for a DC/DC Cuk converter to obtain a large step-down of the input voltage without limiting the control duty cycle in its lower extremes. To obtain very low output voltages (5V, 3.3V or even

lower) in PFC converters with input-output isolation, the switched-capacitor scheme provides extra step-down of the capacitor voltage and thus avoids designing the isolation transformer with a high turns ratio. However, the benefits of increasing the number of storage capacitors to form a series-charging, parallel-discharging structure is also limited because of the increased core loss and the added complexity of the transformer as well as the increased number of diodes needed. In this particular converter, for example, with n capacitors, the number of diodes required is to be $3(n\text{-}2)+3$ when n is greater than 2. This will certainly affect the converter efficiency.

Use of a forward-type transformer in the application of switched-mode power conversion usually requires a tertiary winding to prevent the transformer core from saturation. Again, the unique structure of the switched-capacitor circuit in this converter provides another salient feature: the saturation of the transformer core is automatically prevented. For this reason, the transformer magnetizing inductance can be neglected and the design and analysis of the power converter are greatly simplified. In addition, leakage inductance of the forward transformer often generates large voltage spikes and ringing on the switch during its turning off. Once again this problem does not exist in this converter as the leakage inductance is utilized as the energy transfer element. As a result, further improvement in conversion efficiency is also expected.

The exploring of other outstanding features about this converter is beyond the topic of this chapter. One of those features worthy of mentioning here is that this converter is suitable for universal input operation by properly selecting the component values. This issue was fully discussed in [83]. However, only the steady state analysis

and design procedure were discussed there. Nothing was mentioned about the circuit dynamic behavior. As has been mentioned in Chapter 2, dynamic modeling of power factor correction converters is a challenging issue due to the fact that the input-output voltage conversion ratio widely changes within each half-line period and the steady state operation point fluctuates at a frequency that doubles the line frequency. One of the approximate approaches suggests that the small signal analysis can be performed similar to that of a DC/DC converter with the input voltage replaced by the *rms* value of the rectified line voltage.

In this chapter, we will first review briefly the circuit operation by giving the state equations for each operation mode. Then the steady state and small-signal models will be provided using the averaging technique. From these models, equivalent circuit representations and small signal transfer functions can be obtained. Based on these transfer functions, a discussion on the feedback controller design is also given to reveal the impact caused by the peculiar operation of the proposed converter. Simulation and experiment results are finally provided to verify the derived model.

4.2 Review of the Circuit Operation

The basic circuit diagram is redrawn in Fig. 4-1. Its key waveforms in a switching cycle are shown in Fig. 4-2. To simplify the analysis, in the following discussion we assume $C_{s1} = C_{s2} = C_s$ and $L_1 = L_2 = L_f$ so that $v_{cs1} = v_{cs2} = v_{cs}$ and $i_{L1} = i_{L2} = i_f$. Also note that within one switching period, the rectified input line voltage can be considered to be

constant and is denoted as v_g. The converter has four operation modes within a switching cycle and Fig. 4-3 shows the equivalent circuit for each mode.

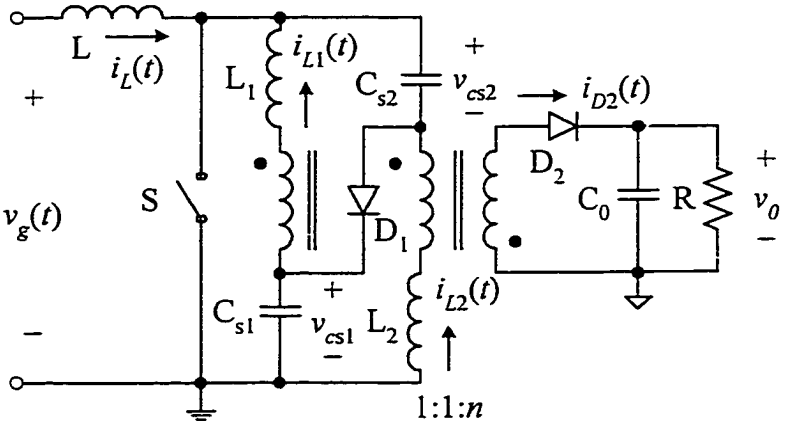


Fig. 4-1. Basic circuit diagram of the PFC converter.

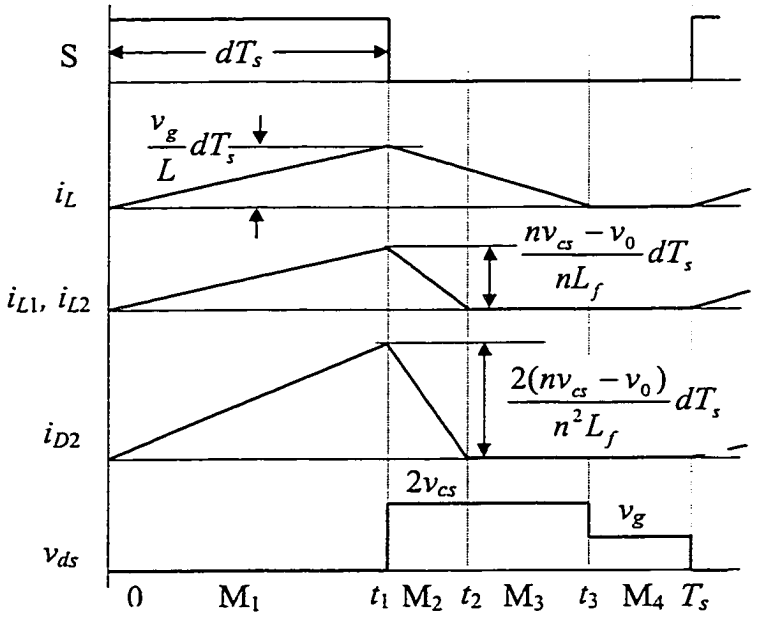


Fig. 4-2. Key waveforms of the converter.

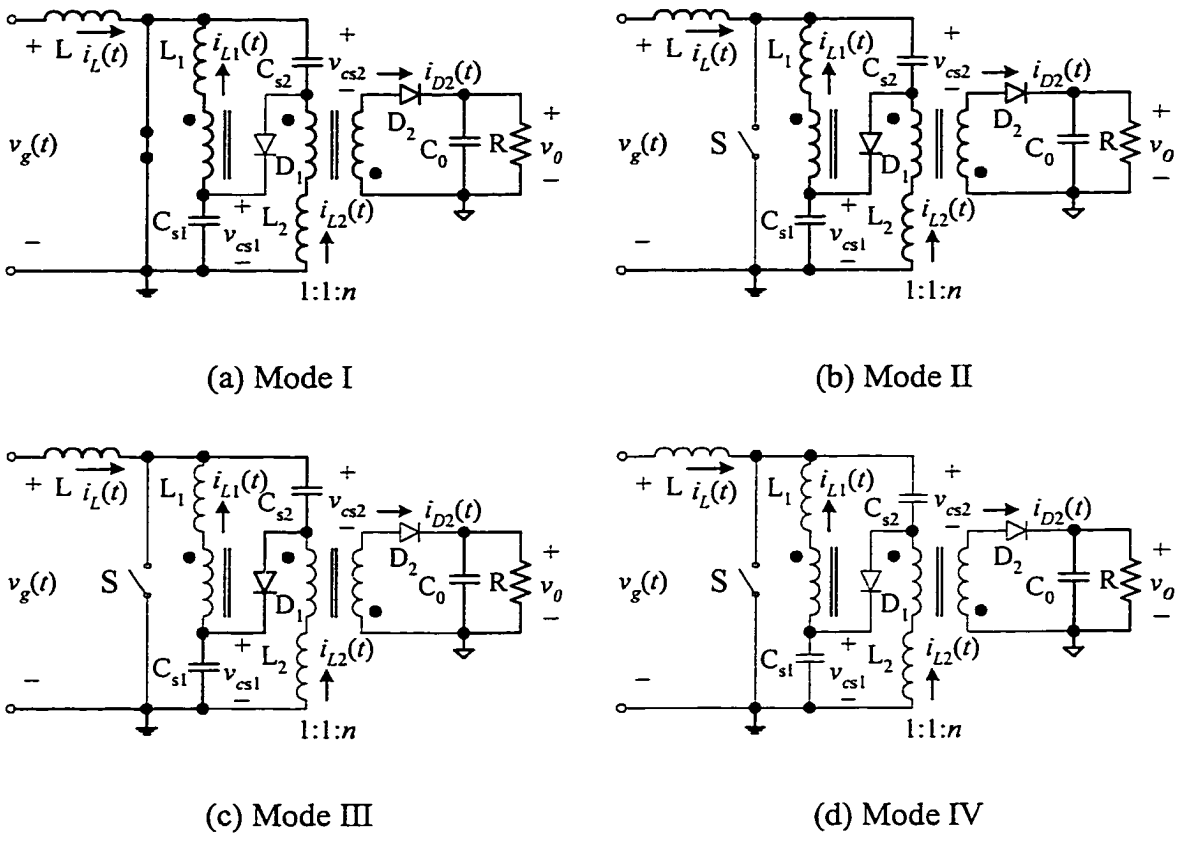


Fig. 4-3. Equivalent circuit of the PFC converter in each mode.

Mode I (t: 0~t_1):

Mode 1 begins when the power switch is turned on at t=0. During this period, energy is transferred from the power source to the choke inductor and the inductor current $i_L(t)$ increases linearly. At the same time, energy stored in the two storage capacitors C_{s1}, C_{s2} during the previous switching cycle is transferred to the load through two symmetrical branches on the primary side of the forward transformer. As a result, current in the two leakage inductors $i_{L1}(t)$, $i_{L2}(t)$ also increases until $t = t_1 = dT_s$ when the

power switch is turned off. Here d is the duty cycle which is determined by the feedback loop, and T_s is the switching period. During this period, we have the following current relations,

$$i_L(t) = \frac{v_g}{L}t, \quad i_f(t) = \frac{nv_{cs} - v_0}{nL_1}t, \quad i_{D2}(t) = \frac{2}{n}i_f(t).$$

Choosing $\mathbf{x} = \begin{bmatrix} v_{cs} & v_0 & i_L & i_f \end{bmatrix}^T$ as the state vector, the following state equation can be obtained:

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1 v_g \tag{4.1}$$

$$v_0 = \mathbf{C}_1\mathbf{x} \tag{4.2}$$

where,

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{C_s} \\ 0 & -\frac{1}{C_0 R} & 0 & \frac{2}{nC_0} \\ 0 & 0 & 0 & 0 \\ \frac{1}{L_f} & -\frac{1}{nL_f} & 0 & 0 \end{bmatrix}, \quad \mathbf{B}_1 = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L} \\ 0 \end{bmatrix}, \quad \mathbf{C}_1 = \begin{bmatrix} 0 & 1 & 0 & 0 \end{bmatrix} \tag{4.3}$$

Mode II (t: t_1~t_2):

In mode 2, diode D_1 conducts and C_{s1} (or C_{s2}) is charged by $i_L(t)$ and $i_{L2}(t)$ (or $i_{L1}(t)$). The primary currents of the transformer, $i_{L1}(t)$ and $i_{L2}(t)$, decrease quickly due to the fact that the voltage across each of the leakage inductor is now the sum of the reflected output voltage and the storage capacitor voltage. Mode 2 ends at $t=t_2$ when $i_{L1}(t)$ and $i_{L2}(t)$ reach zero (they will not become negative due to the presence of D_2 on the secondary side of the transformer). In mode 2, we have,

$$i_L(t) = \frac{v_g}{L} dT_s - \frac{2v_{cs} - v_g}{L}(t - dT_s) \tag{4.4}$$

$$i_f(t) = \frac{nv_{cs} - v_0}{nL_1} dT_s - \frac{nv_{cs} + v_0}{nL_1}(t - dT_s) \tag{4.5}$$

with

$$i_f(t)\Big|_{t=(d+d_1)T_s} = 0$$

and

$$d_1 = \frac{t_2 - t_1}{T_s} = \frac{nv_{cs} - v_0}{nv_{cs} + v_0} d \tag{4.6}$$

The state matrices are:

$$\mathbf{A}_2 = \begin{bmatrix} 0 & 0 & \frac{1}{C_s} & \frac{1}{C_s} \\ 0 & -\frac{1}{C_0 R} & 0 & \frac{2}{nC_0} \\ -\frac{2}{L} & 0 & 0 & 0 \\ -\frac{1}{L_f} & -\frac{1}{nL_f} & 0 & 0 \end{bmatrix}, \quad \mathbf{B}_2 = \mathbf{B}_1, \quad \mathbf{C}_2 = \mathbf{C}_1 \tag{4.7}$$

Mode III (t: t_2~t_3):

Mode 3 is an extended period of mode 2 in that the storage capacitors C_{s1} and C_{s2} are continuously being charged by current $i_L(t)$. During this period, the magnetic energy accumulated in the choke inductor L and energy from the input source are continuously transferred to C_{s1} and C_{s2} in the same manner as that in mode 2. Therefore, the rate of decrease in $i_L(t)$ is the same in these two modes and is given by,

$$\frac{di_L}{dt} = \frac{2v_{cs} - v_g}{L} \tag{4.8}$$

This mode ends when $i_L(t)$ decreases to zero at $t = t_3$ ($t_3 - t_2 = d_2 T_s$) and

$$d_2 = \frac{t_3 - t_2}{T_s} = \frac{V_g}{V_g - 2V_{cs}} d - d_1 \tag{4.9}$$

The state matrices for this mode are given by,

$$\mathbf{A}_3 = \begin{bmatrix} 0 & 0 & \frac{1}{C_s} & 0 \\ 0 & -\frac{1}{C_0 R} & 0 & 0 \\ -\frac{2}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{B}_3 = \mathbf{B}_1, \quad \mathbf{C}_3 = \mathbf{C}_1 \tag{4.10}$$

Mode IV (t: $t_3 \sim T_s$):

Mode 4 is known as the freewheeling stage and is used for regulation purposes only. Because of diode D_2, there is no energy transfer from the transformer to the load and the output voltage is maintained solely by the output capacitor C_0. The maximum regulation of this PFC converter is achieved when the time duration of this mode reduces to zero. At $t=T_s$, this mode ends and a new switching cycle begins.

The state matrices for this freewheeling stage are,

$$\mathbf{A}_4 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_0 R} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{B}_4 = [\mathbf{0}]_{4\times 1}, \quad \mathbf{C}_4 = \mathbf{C}_1 \tag{4.11}$$

4.3 State-Space Averaging Model

According to the averaging procedure described in Chapter 2, the following state space equations can be obtained by averaging the state matrices over a switching period,

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}v_g \\ v_0 = \mathbf{C}\mathbf{x} \end{cases} \tag{4.12}$$

Since the inductor currents operate in DCM, the complete averaging model of the converter can be obtained by the above state equations together with the following additional constraints:

$$\frac{di_L}{dt} = 0, \quad \frac{di_f}{dt} = 0 \tag{4.13}$$

$$i_L = \frac{v_g}{2L} dT_s, \quad i_f = \frac{nv_{cs} - v_0}{2nL_f} dT_s \tag{4.14}$$

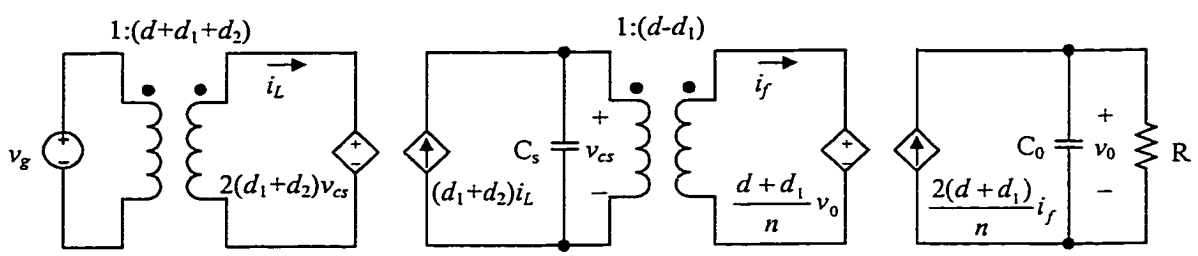
The state matrices in Equation 4.12 are given by,

$$\mathbf{A}=\begin{bmatrix} 0 & 0 & \frac{d_1+d_2}{C_s} & \frac{d_1-d}{C_s} \\ 0 & -\frac{1}{RC_0} & 0 & \frac{2(d+d_1)}{nC_0} \\ -\frac{2(d_1+d_2)}{L} & 0 & 0 & 0 \\ \frac{d-d_1}{L_f} & -\frac{d+d_1}{nL_f} & 0 & 0 \end{bmatrix} \tag{4.15}$$

$$\mathbf{B}=\begin{bmatrix} 0 \\ 0 \\ \frac{d+d_1+d_2}{L} \\ 0 \end{bmatrix} \tag{4.16}$$

$$\mathbf{C}=\begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{4.17}$$

Fig. 4-4 shows an equivalent circuit representation of the average model described from Equations 4.12 to 4.17.



$$i_L=\frac{v_g}{2L}dT_s,\ i_f=\frac{nv_{cs}-v_0}{2nL_f}dT_s$$

Fig. 4-4. Equivalent circuit of the averaged model.

4.3.1 Steady State Model

Steady state relations among the system quantities are given in Equations 4.18 and 4.19. These relations are the basis for the designing of nominal operation point. They are also obtained from Equations 4.12 to 4.17 by setting $\frac{d\mathbf{x}}{dt} = 0$ and replacing all the variables with their corresponding DC values.

$$\begin{cases} (D_1 + D_2)I_L = (D - D_1)I_f \\ nV_0 = 2R(D + D_1)I_f \\ 2(D_1 + D_2)V_{cs} = (D + D_1 + D_2)V_g \\ n(D - D_1)V_{cs} = (D + D_1)V_0 \end{cases} \tag{4.18}$$

with two additional constraints,

$$\begin{cases} I_L = \frac{V_g}{2L} DT_s \\ I_f = \frac{nV_{cs} - V_0}{2nL_f} DT_s \end{cases} \tag{4.19}$$

An equivalent circuit representation for the above DC model can also be obtained directly from Fig. 4-4 with the capacitors treated as open circuits. All the variables should be substituted by their DC values.

Equation 4.18 can be used to derive the dependence of DC quantities D_1, D_2, V_0, V_{cs} on circuit and control parameters. These relations are given in Equations 4.20 to (4.23).

$$D_1 = \frac{3k_2 + 4D^2 - a}{a + k_2 - 4D^2} D, \quad D_2 = bm_1 D - D_1 \tag{4.20}$$

$$m_1 = \frac{1}{4}\left(1 + \sqrt{1 + \frac{8}{b}}\right), \quad m_2 = \frac{a - (k_2 + 4D^2)}{2k_2} nm_1 \tag{4.21}$$

in which,

$$m_1 = \frac{V_{cs}}{V_g}, \quad m_2 = \frac{V_0}{V_g}, \quad k_1 = \frac{2n^2 L}{RT_s}, \quad k_2 = \frac{2n^2 L_f}{RT_s} \tag{4.22}$$

and

$$\begin{cases} a = \sqrt{(k_2 + 4D^2)^2 + 16k_2 D^2} \\ b = \dfrac{2k_1[2a(k_2 + 2D^2) - a^2 + k_2(4D^2 - k_2)}{k_2^2(a + k_2 - 4D^2)} \end{cases} \tag{4.23}$$

4.3.2 Small Signal Dynamic Model

Small signal relationship among state variables is derived by applying small signal perturbations $\hat{v}_g$ to the nominal input voltage V_g, and $\hat{d}$ to the nominal duty cycle D as shown by,

$$v_g = V_g + \hat{v}_g, \quad d = D + \hat{d}$$

These perturbations results in variations in the state variables and the output voltage, i.e.,

$$\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}, \quad v_0 = V_0 + \hat{v}_0$$

After linearizing the state equations and retaining only the first-order small signal terms, the following dynamic equations are obtained:

$$\begin{cases} C_s \dfrac{d\hat{v}_{cs}}{dt} = (\hat{d}_1 + \hat{d}_2) I_L + (D_1 + D_2)\hat{i}_L + (\hat{d}_1 - \hat{d}) I_f + (D_1 - D)\hat{i}_f \\ C_0 \dfrac{d\hat{v}_0}{dt} = -\dfrac{1}{R}\hat{v}_0 + \dfrac{2}{n}(D + D_1)\hat{i}_f + \dfrac{2}{n}(\hat{d} + \hat{d}_1) I_f \\ 2(\hat{d}_1 + \hat{d}_2) V_{cs} = (D + D_1 + D_2)\hat{v}_g + (\hat{d} + \hat{d}_1 + \hat{d}_2) V_g - 2(D_1 + D_2)\hat{v}_{cs} \\ (\hat{d} - \hat{d}_1) V_{cs} = \dfrac{1}{n}[(D + D_1)\hat{v}_0 + (\hat{d} + \hat{d}_1) V_0] - (D - D_1)\hat{v}_{cs} \end{cases} \tag{4.24}$$

with additional constraints,

$$\begin{cases} \hat{i}_L = \dfrac{T_s}{2L}(V_g\hat{d} + D\hat{v}_g) = \dfrac{I_L}{D}\hat{d} + \dfrac{I_L}{V_g}\hat{v}_g \\ \hat{i}_f = \dfrac{I_f}{D}\hat{d} + \dfrac{n\hat{v}_{cs} - \hat{v}_0}{nV_{cs} - V_0}I_f \end{cases} \tag{4.25}$$

The last two expressions in Equation 4.24 are the result of additional constraints in Equation 4.13. It is clear that the small signal model of the converter has been reduced to a second order system. In order to derive the system transfer functions, unknown modulation quantities such as $\hat{d}_1, \hat{d}_2$ must first be determined.

From the last two expressions in Equation 4.24, we have,

$$\hat{d}_1 = \frac{n(D - D_1)\hat{v}_{cs} + (nV_{cs} - V_0)\hat{d} - (D + D_1)\hat{v}_0}{nV_{cs} + V_0}$$

$$\hat{d}_2 = \frac{2(D_1 + D_2)\hat{v}_{cs} - V_g\hat{d} - (D + D_1 + D_2)\hat{v}_g}{V_g - 2V_{cs}} - \hat{d}_1$$

Substitution of the above expressions and Equation 4.25 into Equation 4.24, the general form of the small signal transfer functions for the input-to-output, $H_s(s)$, and control-to-output, $H_d(s)$, can be obtained as:

$$H_s(s)=\frac{\hat{v}_0(s)}{\hat{v}_g(s)}=\frac{a_{21}b_{11}}{s^2-(a_{11}+a_{22})s+a_{11}a_{22}-a_{12}a_{21}} \tag{4.26}$$

$$H_s(s)=\frac{\hat{v}_0(s)}{\hat{d}(s)}=\frac{b_{22}(s-a_{11})}{s^2-(a_{11}+a_{22})s+a_{11}a_{22}-a_{12}a_{21}} \tag{4.27}$$

where

$$a_{11}=\frac{1}{C_s}\left[\frac{2(D_1+D_2)I_L}{V_g-2V_{cs}}+\frac{n(D-D_1)I_f}{nV_{cs}+V_0}-\frac{n(D-D_1)I_f}{nV_{cs}-V_0}\right]$$

$$a_{12}=-\frac{I_f}{C_s}\left[\frac{D+D_1}{nV_{cs}+V_0}+\frac{D_1-D}{nV_{cs}-V_0}\right]$$

$$a_{21}=-\frac{2I_f}{C_0}\left[\frac{D-D_1}{nV_{cs}+V_0}+\frac{D_1+D}{nV_{cs}-V_0}\right]$$

$$a_{22}=-\left[\frac{1}{C_0R}+\frac{2(D+D_1)I_f}{nC_0}\left(\frac{1}{nV_{cs}+V_0}+\frac{1}{nV_{cs}-V_0}\right)\right]$$

$$b_{11}=\frac{I_L}{C_s}\left[\frac{D_1+D_2}{V_g}-\frac{D+D_1+D_2}{V_g-2V_{cs}}\right]$$

$$b_{22}=\frac{2I_f}{nC_0}\left[1+\frac{D_1}{D}+\frac{2nV_{cs}}{nV_{cs}+V_0}\right]$$

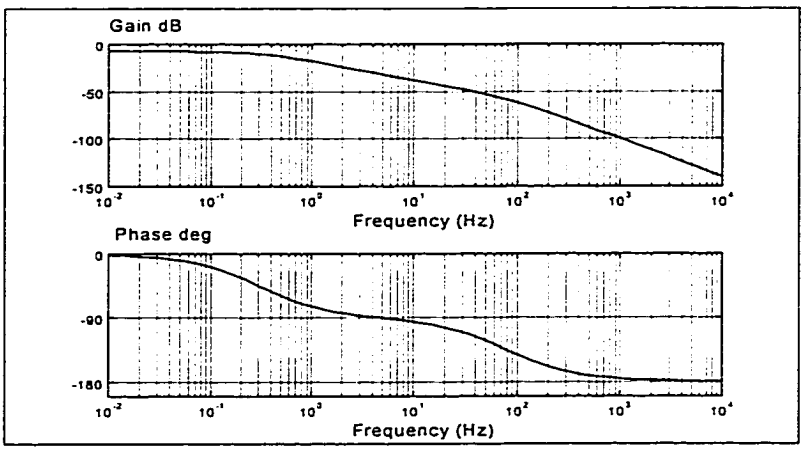
For the converter with a DC output 50W@50V, input voltage of 120V and the following set of circuit parameters: n=0.27, L=482.3μH, L_f=80.9μH, C_s=820μF, C_0=900μF, f_s=50kHz, the above expressions result in two transfer functions given as:

$$H_s(s) = \frac{394.7}{s^2 + 497.7s + 947.2} \tag{4.28}$$

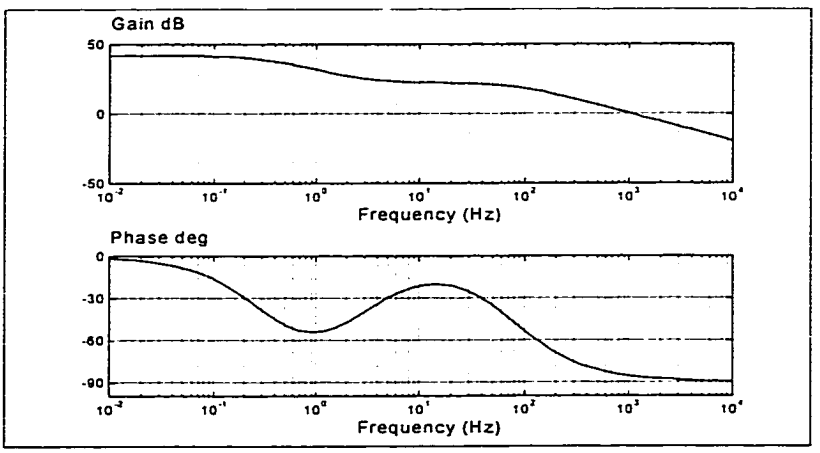
$$H_d(s) = \frac{6531(s + 17.78)}{s^2 + 497.7s + 947.2} \tag{4.29}$$

Frequency responses of these two transfer functions are shown in Figs. 4-5(a) and 4-5(b), respectively. It can be noticed that the system is highly damped, which is expected as the converter is operating in DCM condition. The two poles are well separated and are located around 0.5Hz and 80Hz, respectively. These values can also be estimated by considering that the boost and forward converters are operating separately in DCM conditions using the above parameters. In this case, the steady state storage capacitor voltage V_{cs} should be considered as the input of the forward converter and the sum of the two storage capacitor voltages ($2V_{cs}$) be the output voltage of the boost converter. From Equations 4.18 and 4.19 it turns out that V_{cs} is 194.4V and the locations of the poles are about 0.31Hz for the boost and about 78.3Hz for the forward converter. They are very close to the values in Fig. 4-5. However, the converter system discussed in this paper is not just a mere cascaded connection of a boost converter with a forward one. It is rather a result of more tightly interconnected subsystems owing to the unusual

operation of the switched-capacitor network as was mentioned in Section 4.1. This impact is manifested by the presence of an additional left-half-plane (LHP) zero in the control-to-output transfer function which does not belong to either of the subsystem and should be considered in the design of the feedback controller.



(a) input-to-output



(b) control-to-output

Fig. 4-5. Frequency responses for (a) input-to-output, and (b) control-to-output.

In the closed-loop design of the PFC converter system, the controller should be designed properly such that the bandwidth of the voltage loop is significantly lower than the 100/120Hz ripple frequency in the output to prevent degradation of the converter power factor. The crossover frequency of the loop gain is usually chosen between one-third or one-fourth of the line frequency. For a DCM operating boost converter used as a PFC pre-regulator, a single type-II compensator in most cases can provide reasonable phase margins (45°-60°) and suitable gain attenuations (30-40dB).

The introduction of an extra LHP zero normally increases the system stability. However, for the discussed converter, this zero is located at 2.83Hz which provides significant phase leading at the desired crossover frequency (refer to Fig. 4-5), making it harder for a type-II compensator to achieve a suitable phase margin. Therefore, an extra phase-lagging network without phase inversion has to be added into the feedback loop to null the low frequency zero. When implemented with an OpAmp, this network generates extra noise into the voltage loop and increases the number of components.

The equivalent small signal circuit model is also available from Equations 4.24 and 4.25 directly or from perturbing the circuit of Fig. 4-4 and through linearization and subtraction of the DC components. In the following process, we introduce three small signal currents, source current $\hat{i}_g$, storage capacitor current $\hat{i}_{cs}$ and output current $\hat{i}_0$ and express them as functions of input modulation $\hat{v}_g$, control modulation $\hat{d}$, circuit parameters as well as steady-state parameters. We have,

$$\hat{i}_g = (D + D_1 + D_2)\hat{i}_L + I_L(\hat{d} + \hat{d}_1 + \hat{d}_2)$$

$$= I_L\left(\frac{4V_{cs}}{2V_{cs} - V_g}\hat{d} - \frac{2(D_1 + D_2)}{2V_{cs} - V_g}\hat{v}_{cs} + \frac{2(D + D_1 + D_2)}{2V_{cs} - V_g}\frac{V_{cs}}{V_g}\hat{v}_g\right) \tag{4.30}$$

$$= j_{11}\hat{d} - j_{12}\hat{v}_{cs} + g_1\hat{v}_g$$

$$\hat{i}_{cs} = -\left(\frac{2(D_1 + D_2)I_L}{2V_{cs} - V_g} + \frac{2n(D - D_1)V_0 I_f}{n^2V_{cs}^2 - V_0^2}\right)\hat{v}_{cs}$$

$$+ \frac{2I_f(DV_0 - D_1 nV_{cs})}{n^2V_{cs}^2 - V_0^2}\hat{v}_0 + \left(\frac{D_1 + D_2}{V_{cs}} + \frac{D + D_1 + D_2}{2V_{cs} - V_g}\right)I_L\hat{v}_g \tag{4.31}$$

$$= j_{21}\hat{v}_g + j_{23}\hat{v}_0 - g_2\hat{v}_{cs}$$

$$\hat{i}_0 = \frac{2}{n}(D + D_1)\hat{i}_f + \frac{2}{n}(\hat{d} + \hat{d}_1)I_f$$

$$= \frac{8V_{cs}I_f}{nV_{cs} + V_0}\hat{d} + \frac{4I_f(DnV_{cs} + D_1V_0)}{n^2V_{cs}^2 - V_0^2}\hat{v}_{cs} - \frac{4(D + D_1)V_{cs}I_f}{n^2V_{cs}^2 - V_0^2}\hat{v}_0 \tag{4.32}$$

$$= j_{33}\hat{d} + j_{32}\hat{v}_{cs} - g_3\hat{v}_0$$

From Equations 4.30 to 4.32, the final form of the small signal circuit model is obtained and is shown in Fig. 4-6, in which g_1, g_2, g_3, j_{11}, j_{12}, j_{21}, j_{23}, j_{32}, j_{33} are given as follows:

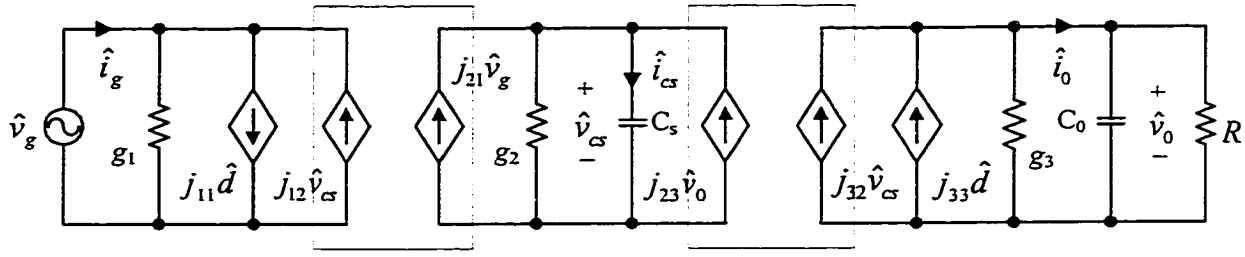
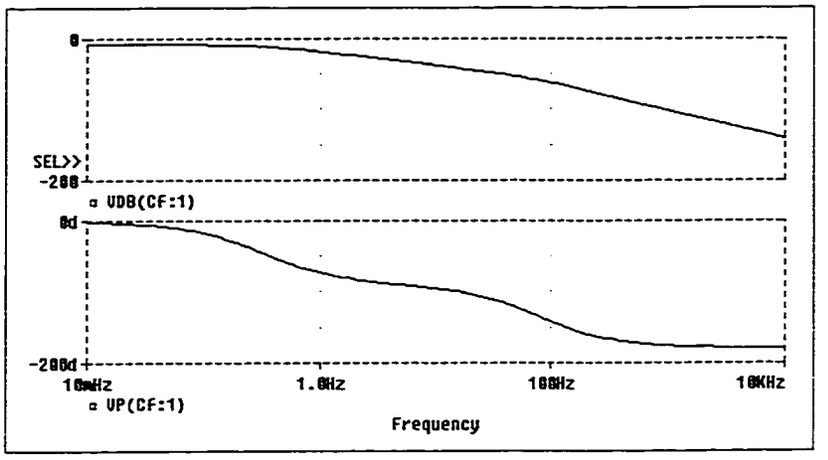


Fig. 4-6. Small signal equivalent circuit model.

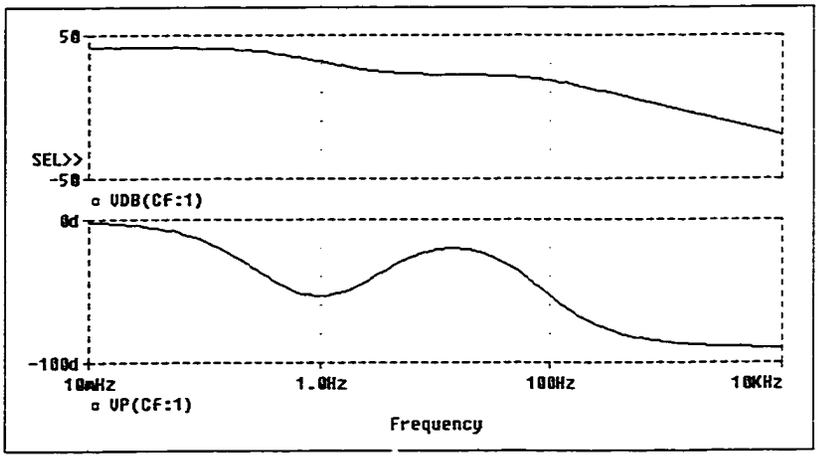
According to the derived small signal model of the converter circuit, Pspice simulation was also carried out with the same circuit parameter and operation condition as that used for Equations 4.28 and 4.29. Simulated frequency responses of the input-to-output and control-to-output are depicted in Figs. 4-7(a) and 4-7(b) respectively. It is found from Fig. 4-5 and Fig. 4-7 that the theoretical transfer characteristics agree very well with the simulation results.

4.4 Experimental Verification

A prototype unit was constructed with the parameters given in Section 4.3 in order to verify the small-signal model. Two types of measurements were performed: (1) input voltage is a rectified 60Hz line voltage and, (2) input voltage is a DC voltage with its value equals the *rms* value of the rectified line voltage. The measured control-to-output frequency characteristics are shown in Figs. 4-8(a) and 4-8(b).



(a) input-to-output

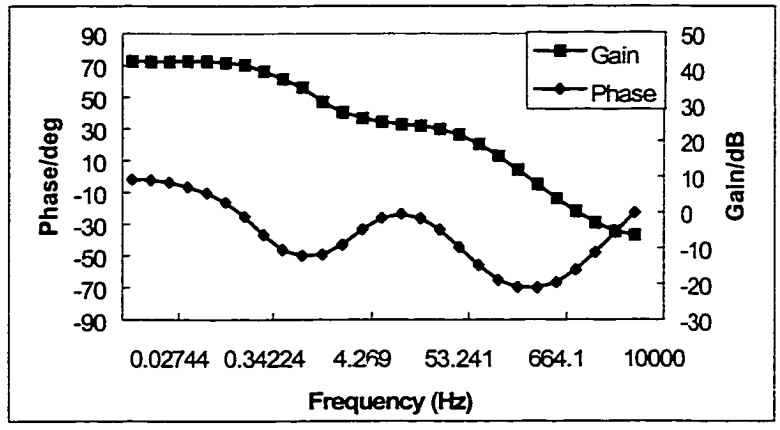


(b) control-to-output

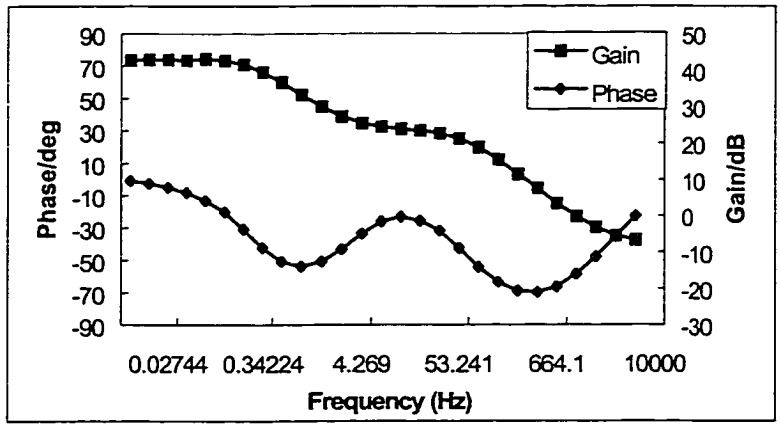
Fig. 4-7. Simulated small signal frequency responses for (a) input-to-output, and (b) control-to-output.

It is shown from Figs. 4-8(a) and (b) that the measurement results agree very well with the two types of input voltages. The differences are within 1dB between the gains and within 6° between the phases; thus verify the assertion that a PFC converter can be

treated as a DC/DC converter with its input voltage equals the *rms* value of the rectified AC line voltage. This treatment greatly simplifies the analytical process and allows most of the well-developed DC/DC converter techniques to be applied directly to the PFC applications.



(a) 120V (*rms*) AC input



(b) 120V DC input

Fig. 4-8. Measured control-to-output frequency characteristics with the input of (a) 120V (*rms*), and (b) 120V DC.

Compared the above measurement with the theoretical result given in Equation 4.29 and shown in Fig. 4-5(b), however, it is found that they match each other only in the low frequency range. There are significant differences when the frequency is higher than 300Hz where the measured phase begins to increase and the slope of the measured gain begins to slow down. This phenomenon clearly indicates that there is still a zero in the high frequency range that was not taken into account in our small-signal model. In practice, this zero is introduced by the non-ideality of the output capacitor. To explain this point, its equivalent-series-resistance (ESR) of 0.05Ω is considered in the model and the simulation result is given in Fig. 4-9. It is noticed that with this small ESR included, results from the measurement and the simulation are in good agreement.

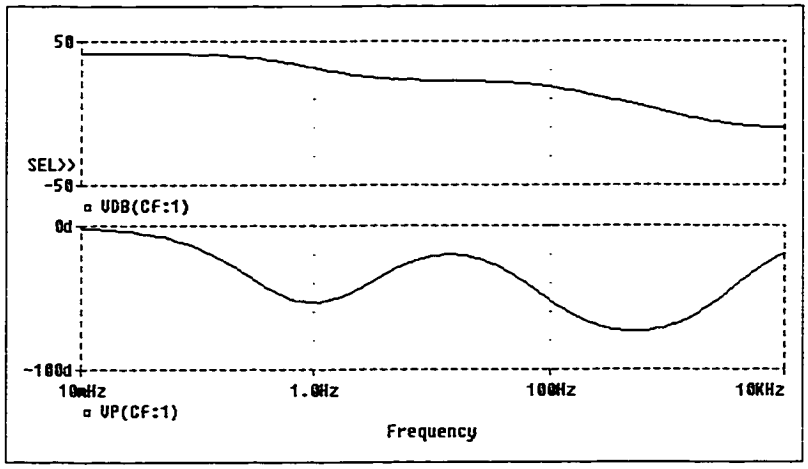
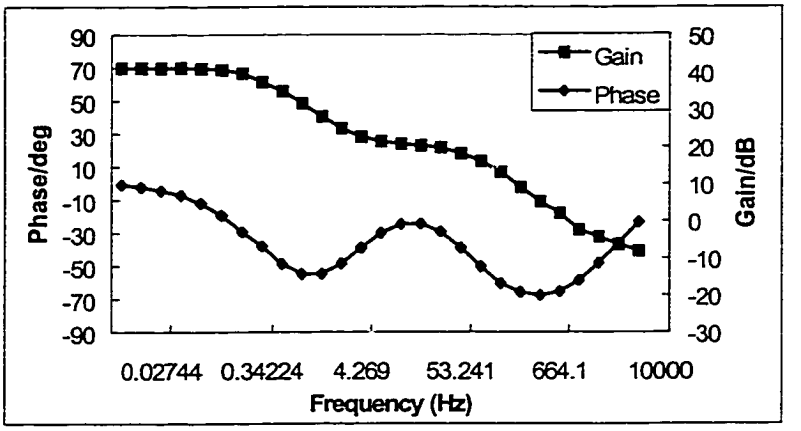
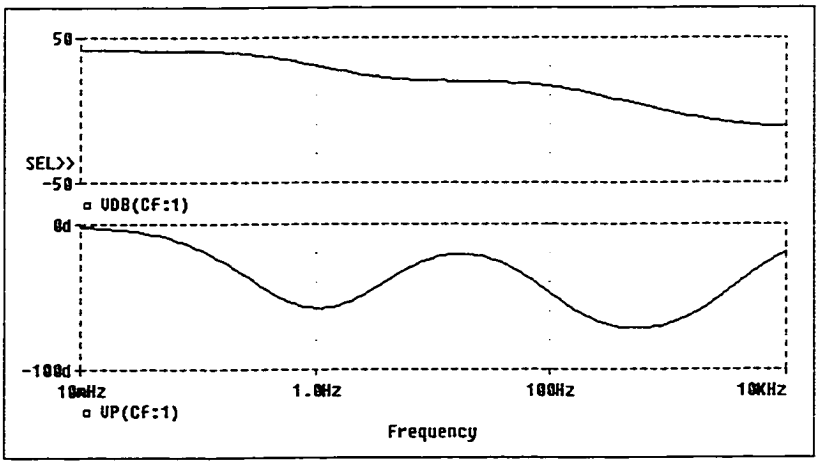


Fig. 4-9. Simulated control-to-output frequency characteristic with output capacitor ESR included.

Measurement of the frequency responses were also performed for different line conditions, and were compared to the simulation results according to the derived small-signal model. The experimental and simulated results are shown in Figs. 4-10(a) and 4-10(b) for V_g=110V DC input, respectively. Figures 4-11(a) and 4-11(b) show the measured and simulated results for V_g=150V DC input, respectively.

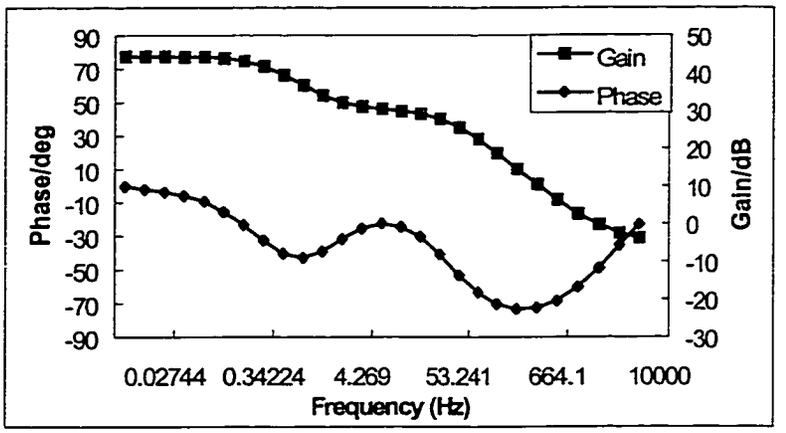


(a) mcasurement result

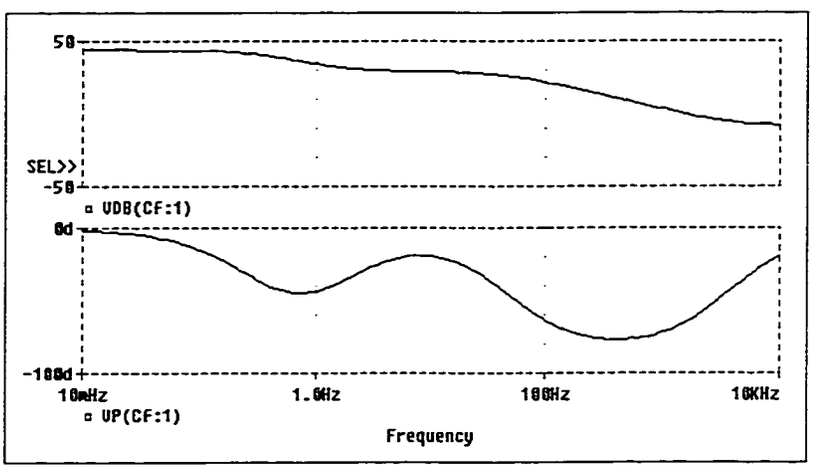


(b) simulation result

Fig. 4-10. Frequency response for a 110V DC input: (a) measured, (b) simulated.



(a) measurement result



(b) simulation result

Fig. 4-11. Frequency response for a 150V DC input: (a) measured, (b) simulated.

It is found from Figs. 4-10 and 4-11 that for each input voltage, the difference between the measured and simulated results is within 2dB in the magnitude. Discrepancy in the phase is within 5° for most of the measured frequency points except in the high frequency range where this value is larger but is still limited within 10°. These results

indicate that the proposed model is a good representation of the small-signal behavior of the converter, especially in the low frequency range.

4.5 Summary

In this paper, a small-signal model for a single-switch PFC converter was developed using the state-space averaging technique. The underlined assumption in the derivation was that the steady state condition could be determined by a DC input whose voltage equals the *rms* value of the rectified line input voltage. The assumption was verified experimentally, thus allowing the analytical method developed for DC/DC converters to be applicable directly to the PFC circuit design.

A special property in the output-to-control transfer function was observed. This property is characterized by the presence of a low frequency LHP zero which does not occur in either of the boost or forward converter when operating in DCM conditions. It is a result of the unique manner of the energy being transferred from the boost converter to the forward converter. The impact of this zero on the controller design was also discussed.

Finally, the effect of the ESR of the output capacitor on the dynamic behavior of the power factor correction circuit was illustrated. The developed mathematical and circuit models were verified by simulation and by the measurement data under different input voltages. All the results verify the validity of the developed models, especially in the low frequency range.

CHAPTER 5

PWM SWITCH MODELING OF SINGLE-SWITCH POWER FACTOR CORRECTION CONVERTERS

5.1 Introduction

It has been mentioned in Chapter 2 that there are a number of techniques available to modeling power electronics circuits. The averaging technique is the most popular approach adopted by many researchers to the analysis of DC/DC converters. The versatile state-space averaging approach can be applied to any PWM converters but its accuracy decreases at high frequency range for converters operating in DCM and thus introduces noticeable errors in predicting fast line or load transient responses. On the other hand, the PWM switch modeling approach improves the accuracy of DCM dynamic characteristics at high frequency range. However it may sometimes not apply directly to topologies where the active and passive switches are physically separated and their numbers are usually not equal. A "conceptual" PWM switch or a separated PWM switch may not easily be extracted.

Todate, the modeling of PFC converters has not been studied thoroughly as has been done with DC/DC converters. The phrase "small-signal characteristics" of PFC converters could be misleading as the converter operation is actually under large signal

environment. While experimental results as presented in Chapter 4 showed that the small signal behavior of PFC converters may be approximated by replacing the rectified AC input by a constant voltage that equals the *rms* value of the AC line, more theoretical investigation is still needed to justify the approach.

From Chapter 4 it is noted that deriving dynamic characteristics of PFC converters using the stage-space averaging method is very tedious and cumbersome. The resulting large and small signal models as shown in Fig. 4-4 and Fig. 4-6, however, are still not easy to use in predicting line and/or load transient performances and not quite satisfactory in obtaining frequency responses when information at high frequency range is required. This is due to the fact that the dynamic behavior of the inductors has been neglected. A PWM switch model can easily perform the required transient and small-signal performance study with a satisfactory accuracy for DCM converters, provided such a model can be found. For single-switch PFC converters, however, the number of passive switches is usually more than one. This plus the presence of transformers often makes it difficult to conceptualize a PWM switch. In this situation, the conventional approach of finding such a switch or a separated PWM switch needs to be modified. A more generalized PWM switch modeling approach suggests that the voltages responsible for charging and discharging of inductor current be identified and the functionality of switches be carefully investigated. Under some circumstances, fictitious switches and/or transformers maybe added in order to realize the functionality of the switches. Circuit transformation can then be applied and the available PWM switch modeling technique can be utilized.

In this chapter, the single-switch AC/DC converter discussed in Chapter 4 is again adopted to show the above modeling technique. The reason to use this converter as an example in this chapter is that it has two diodes, a three-winding isolation transformer and all the switches are separated. These are the main sources known to make it difficult to derive PWM switch models. It will be shown that the derived model for this converter can be easily implemented into the Pspice library to facilitate steady state and transient analysis. The modeling technique introduced is general and can be easily extended to other single-switch PFC converters operating in DCM condition.

Before discussing the model of the PFC circuit, an error of the classical DCM PWM switch model implemented in the Pspice library is first identified and solution to the problem is provided. This corrected Pspice library model is very useful since a lot of PFC circuits utilize a DCM operating boost topology as the front-end converter, as is the one discussed in Chapter 4 and is to be discussed in this chapter. Second, conduction losses will be modeled and included into the classical PWM switch model. This issue was considered in the past only with the assumption that inductor current ripple is negligible compared with its average value. However, when this current has large ripples, especially when it becomes discontinuous, the issue of properly modeling the conduction losses has not been addressed in the open literature. Such a non-ideal PWM switch model is presented in Section 5.3.

5.2 Correcting the Pspice Large-Signal Model for DCM PWM Converters

In this section, it will be shown that an incorrect parameter limit in the existing Pspice PWM switch model is responsible for consistent convergence problems or erroneous results encountered in simulating the boost converter operating in DCM. Such phenomena could not be observed when the model is utilized in the buck, buck-boost and Cuk converters. Correction of the model is provided and its validity is verified using a specific converter example. The results illustrate how the existing and corrected models produce different results when the boost converter is subjected to sudden load variations.

Unlike the state-space averaging approach which relies on algebraic manipulation of a set of state-space equations to derive the circuit model, the PWM switch model comes directly with the convenient circuit form. Thus makes it particularly suitable for designers to use circuit simulation tools to analyze PWM DC/DC converters. This evolved modeling technique has been adopted by MicroSim Corp. and incorporated into its professional versions of Pspice simulator [84]. The simulator's model library "swit_rav.lib" contains a number of PWM switch models for CCM, DCM and for voltage mode and current mode control. With these models, derivation of transient response and small-signal frequency characteristics of PWM DC/DC converters is greatly simplified. For example, the sub-circuit model VMLSDCM (its netlist is given in Table 5-1) presents the large-signal model for converters operating in DCM.

5.2.1 Analysis and Modification of the Model

Referring to Fig. 2-4(a) for the PWM switch and Fig. 2-6 for its equivalent circuit model in DCM operation, Pspice circuit diagrams describing this model are shown in Fig. 5-1. From Table 5-1, it is noted that the controlled voltage source *etbl* is a linear function of the control variable *i(vmp)* (i_p in Fig. 2-6) and is forced to be positive. This relation is shown in Fig. 5-2(a). Under steady state and transient conditions, current i_p is always positive in buck, buck-boost and Cuk converters. In these converters, the controlled voltage source *etbl* is assigned to a proper value (limited between 0 and 400) corresponding to the amount of current i_p. *However, this current will be negative in the boost converter under normal operation conditions*. In this case, *etbl* is always forced to be very small and it does not reflect the change in current i_p. As a result, *etbl* is always assigned to a minimum value (10^{-8}) which produces a very large *emew* (μ in Fig. 2-6) regardless of the amount of current i_p. This obviously results in erroneous simulation results.

Solution to this problem is to enable the controlled source *etbl* to accommodate bi-directional current flow for i_p. This can be done by modifying the *etbl* statement in the netlist with either the arithmetic expression (*value*) or the look-up table function (*table*) as given below:

*etbl anum 0 value={2*lfil*fs*i(vmp)}*

or

*etbl anum 0 table {2*lfil*fs*i(vmp)} (-400,-400) (400,400)*

Figure 5-2(b) shows the *corrected* relation between *etbl* and bi_p. Now *etbl* can take positive or negative values according to the direction of the control current.

Table 5-1. Netlist of the Pspice VMLSDCM Model

```
* Large signal discontinuous conduction voltage mode model
* Params: Rmphite→External ramp height, Valleyv→Valley voltage of external ramp
* LFIL→Filter inductance, FS→Operating frequency
* Pins: active (A), passive (P), common (C), control voltage (Vc)
.subckt VMLSDCM  A  P  C  Vc Params: Rmphite=2 Valleyv=1 LFIL=500u FS=50k
 vconv    conv    0    1
 emod     d       0    table {v(conv)*(v(vc)-valleyv)/rmphite} = (.01, .01) (.99, .99)
 etbl     anum    0    table {2*lfil*fs*i(vmp)} (1e-8, 1e-8) (400, 400)
 emew     mew     0    value={v(conv)*v(d)*v(d)*v(a,c)/v(anum)}
 gac      a       c    value={v(conv)*v(mew)*i(vmp)}
 ecp      c       x    value={v(conv)*v(mew)*v(a,c)}
 vmp      p       x    0
 rconv    d       0    1g
 rc       conv    0    1g
 ranum    anum    0    1g
 r5       mew     0    1g
.ends
```

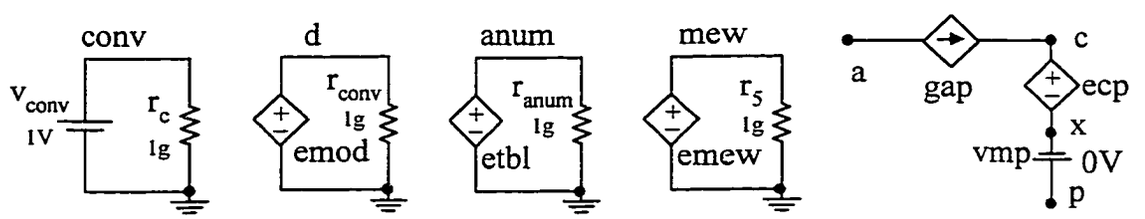
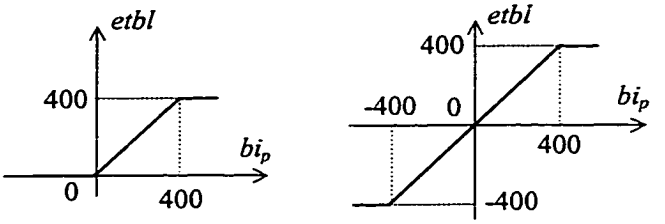


Fig. 5-1. Pspice circuit diagram for DCM PWM switch model.



(a) Pspice model (b) corrected model

Fig. 5-2. Controlled voltage source *etbl* vs. current i_p ($b = 2L_{fi}f_s$).

5.2.2 Verification of the Modified Model

With the above slight change, the VMLSDCM model can be used to simulate classical PWM converters including the boost converter without introducing any convergence problems or giving wrong solutions. An example is given in Fig. 5-3 showing the simulation schematic diagram of a DCM boost converter with switching frequency $f_s = 50$kHz, $VALLEYV = 1$ and $RMPHITE = 2$. In this figure, block U represents the corrected average switch model VMLSDCM. Since $V_c = 2$V, it is obvious from the Pspice model that the duty cycle $D = 0.5$. With all the available parameters, the output voltage of the boost converter can be easily predicted theoretically from the expression: $V_0 = \frac{V_{in}}{2}\left(1+\sqrt{1+\frac{2RD^2}{Lf_s}}\right)$, which gives about 25.9V output voltage for a 100Ω load and about 33.5V for a 200Ω load. Figure 5-4 shows the transient waveform of the output voltage ($V(C_0)$) from one steady-state to another when the load is subjected to a sudden change at $t = 2$ms. It can be seen that the simulation gives almost the same result with the corrected VMLSDCM model, with *etbl* equals -2.59 and -1.675 for 100Ω and 200Ω

loads, respectively. Under the existing incorrect model, *etbl* will be forced to equal 10^{-8} under both loads.

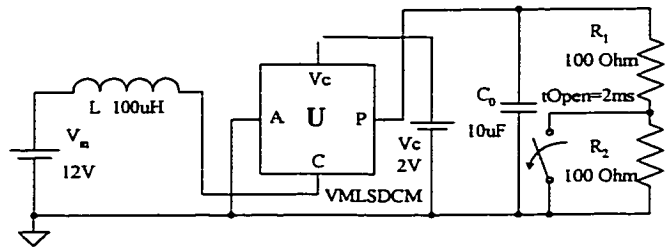


Fig. 5-3. Schematic diagram of the boost converter using the Pspice VMLSDCM model.

The existing Pspice model was also applied to this schematic diagram for comparison purposes. Two types of phenomena were observed. With the same initial inductor and capacitor conditions as the above example, a *convergence problem in transient bias point calculation* message was reported. However, when no initial condition was assigned to the inductor and capacitor, a false simulation result was obtained as shown in Fig. 5-5, which shows that the output voltage converges to about -21.45V!

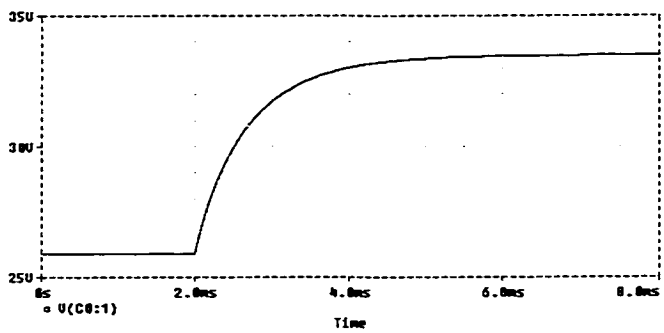


Fig. 5-4. Output voltage of the boost converter with the corrected VMLSDCM model.

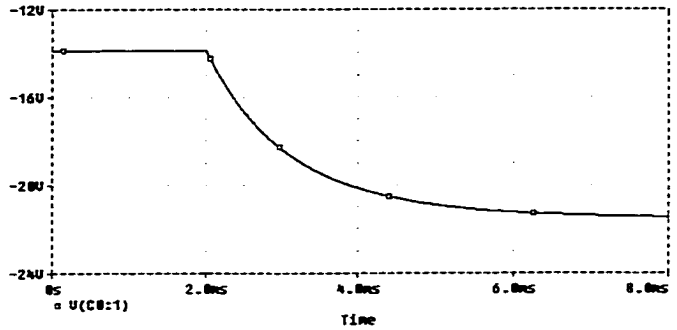


Fig. 5-5. Output voltage of the boost converter with the existing Pspice VMLSDCM model.

5.3 Modeling of Conduction Losses in PWM Converters

The three-terminal PWM switch model is a powerful and convenient tool in the study of PWM DC/DC converters. Non-ideal components such as inductor equivalent series resistance (ESR) and on-resistance of switches have measurable effect on the steady state and small signal performances of the converter. This effect was considered in some literature when the converter operated in CCM and under a small ripple assumption on the inductor current waveform [62, 79, 84]. However, accuracy of the model in these works decreases with the increasing of inductor current ripple with respect to its average value. To an extreme, when the converter operates in DCM, a proper method considering the effect of non-ideal components in the PWM switch model has not been found in the open literature. Such a PWM switch model is developed and implemented into the Pspice library in this section based on the energy loss invariant principle. It is found that duty cycle dependent parasitic resistors need to be used in the model. Accuracy of the

proposed model has been verified through Pspice simulation using a buck and a boost converter operating in DCM.

5.3.1 Conduction Losses in DCM Converters

In the following discussion, the diode is considered to be a constant voltage V_d in series with a linear on-resistor r_d when conducting. The active switch has an on-resistance of r_s and the inductor has an ESR of r_L. A basic problem in analyzing DC/DC converters with non-ideal components is that the inductor current will not be a triangular waveform superimposed on a DC current as was considered in lossless converters. Inductor current rises and falls exponentially with an average value of I' instead of I when ideal components are assumed, as is shown in Fig. 5-6. Whether it is easy or not to calculate the difference between them, it is quite clear that this difference is determined by the time constants in charging and discharging of the inductor. In our initial step, we assume that these time constants are much greater than the charging and discharging time of the inductor, i.e.:

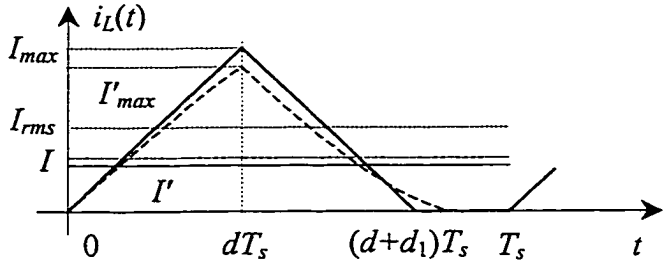


Fig. 5-6. Inductor current with ideal (solid line) and non-ideal (dashed line) components.

$$\frac{L}{r_s + r_L} >> dT_s, \quad \frac{L}{r_d + r_L} >> (1-d)T_s \tag{5.1}$$

and

$$\frac{v_{dis}}{r_d + r_L} >> I'_{\max} \tag{5.2}$$

where v_{dis} denotes the voltage applied to the first order L-R circuit to discharge the inductor. For the buck converter, this voltage is the load voltage subtracted by V_d.

Under these conditions, the difference between actual and ideal inductor current waveforms is negligible. In terms of energy losses in ESR and on-resistances, however, they are not negligible even though Equations 5.1 and 5.2 are satisfied.

In an average model, inductor current is measured by its average value over each switching cycle. This current also generates energy losses on the parasitic resistors, which are characterized by the *rms* value of the current instead of the average value. As qualitatively shown in Fig. 5-6, the *rms* value is clearly larger than the average value. To correctly model energy losses on the parasitic resistors in PWM converters, the energy loss in the average model must remain unchanged as in the actual switching converter. As a result, the *rms* and *average* values of the inductor current as shown in Fig. 5-6 are first determined and they are given below:

$$I_{rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_L^2(t)dt} = \sqrt{\frac{d+d_1}{3}} I_{\max} \tag{5.3}$$

$$I = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt = \frac{1}{2}(d+d_1)I_{\max} \tag{5.4}$$

where I_{max} is shown in Fig. 5-6.

The energy dissipated in the inductor ESR, r_L, over one switching period is given by:

$$W_{rL} = I_{rms}^2 r_L T_s = \frac{1}{3}(d+d_1)I_{\max}^2 r_L T_s \tag{5.5}$$

The same amount of energy dissipation should also be accounted for in the averaged model based on the *average* current. This implies that the ESR of the inductor should be replaced by an equivalent resistor to accommodate the difference between the *rms* and *average* values of the inductor current, i.e.,

$$W_{rL} = I^2 r_{L,eq} T_s = \frac{1}{4}(d+d_1)^2 I_{\max}^2 r_{L,eq} T_s \tag{5.6}$$

where $r_{L,eq}$ is the equivalent ESR of the inductor in the averaged model.

From Equations 5.5 and 5.6 it is easy to obtain:

$$r_{L,eq} = \frac{4}{3}\frac{r_L}{d + d_1} \tag{5.7}$$

Equation 5.7 suggests that the ESR of the inductor be replaced by a larger resistor in the averaged model. It is also noted that in the denominator, $(d+d_1)$ is the relative duration of the inductor current in each switch cycle within which this current is greater than zero. Obviously this equivalent resistance depends on control duty cycle and circuit parameters.

To calculate the equivalent on-resistance for the active switch and the passive switch, same procedure described from Equation 5.3 to Equation 5.7 can be followed. However, the result can also be obtained simply by observing that the relative duration of the current flowing through the active switch is d and that flowing through the passive switch is d_1. Therefore,

$$r_{s,eq} = \frac{4}{3}\frac{r_s}{d}, \quad r_{d,eq} = \frac{4}{3}\frac{r_d}{d_1} \tag{5.8}$$

where $r_{s,eq}$, $r_{d,eq}$ is the equivalent on-resistances of the active switch and the diode in the averaged model, respectively.

Figure 5-7 shows the DCM PWM switch circuit model with conduction losses included. From Chapter 2, we know that,

$$\mu = \frac{d^2 T_s}{2L}\frac{v_{ac}}{i_p}, \quad d_1 = \frac{d}{\mu} \tag{5.9}$$

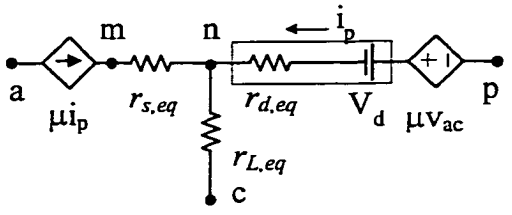


Fig. 5-7. DCM PWM switch circuit model with conduction losses.

5.3.2 Conduction Losses in CCM Converters

The above discussion about equating energy dissipation between the actual switching converter and its averaged DCM model can also be applied to deriving the CCM PWM switch model with conduction losses. Inductor current waveform of the ideal converter for this case was shown in Fig. 2-2 under steady-state operation conditions. It is redrawn in Fig. 5-8 but is shown with larger current ripple with I denotes the average value and ΔI the inductor current ripple. To include conduction losses in the CCM model, the relation between *average* and *rms* values of this current needs to be determined first.

The portion of the inductor current during [0, dT_s] time period flows through the active switch and the other portion in each switching period flows through and passive switch. Simple mathematical derivation reveals that the *rms* values of the inductor current ($I_{L,rms}$) as well as the switch current ($I_{sw,rms}$, $I_{D,rms}$) have the following forms:

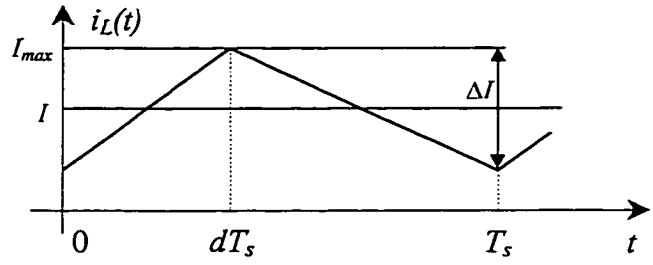


Fig. 5-8. Ideal inductor current waveform for CCM condition.

$$I_{L,rms} = \sqrt{1 + \frac{1}{12}\left(\frac{\Delta I}{I}\right)^2}\, I = \beta I \tag{5.10}$$

$$I_{sw,rms} = \sqrt{d}\, I_{L,rms}, \quad I_{D,rms} = \sqrt{1-d}\, I_{L,rms} \tag{5.11}$$

With the same assumption on the time constant as given in Equations 5.1 and 5.2, the energy loss invariant principle outlined from Equation 5.3 to Equation 5.7 results in:

$$r_{L,eq} = \beta^2 r_L, \quad r_{s,eq} = \frac{\beta^2}{d} r_s, \quad r_{d,eq} = \frac{\beta^2}{1-d} r_d \tag{5.12}$$

Equation 5.12 shows that the equivalent resistance in the averaged CCM model depends on both the duty ratio d (excludes the ESR of the inductor) and the relative inductor current ripple. If we consider that a lumped resistor in the inductor branch is responsible for all the conduction losses, then the equivalent resistance of this resistor can be expressed as:

$$r_{eq} = \beta^2 \left[r_{L,eq} + d r_{s,eq} + (1-d) r_{d,eq} \right] \tag{5.13}$$

Under a small ripple assumption, i.e., $I >> \Delta I$, coefficient β^2 becomes very close to unity. In this case,

$$r_{eq} \approx r_{L,eq} + d r_{s,eq} + (1-d) r_{d,eq}$$

It is interesting to note that this result is exactly the same as that presented in [62, 79, 84]. Another interesting observation of the equivalent resistance given in Equation 5.12 shows that when the converter operates in critical conduction mode, Equation 5.12 takes the simple form as that of Equations 5.7 and 5.8 for the DCM model with d_1=1-d. This result demonstrates that both CCM and DCM averaged models agree with each at critical conduction mode.

5.3.3 Verification of the Non-Ideal PWM Switch Model

The non-ideal PWM switch model can be easily implemented into the Pspice library. Table 5-2 shows the Pspice netlist of the DCM PWM switch circuit model given in Fig. 5-7 (LOSSY_LSDCM). Noted that in the netlist, the controlled voltage source *evdrd* denotes the voltage across the conducting diode. The direction of the diode forward voltage drop V_d depends on the direction of current *i*(*vxy*) (i_p in Fig. 5-7). For the Boost converter, this current is negative and therefore the controlled voltage source *evdrd* should take this into account. This issue has already discussed in Section 5.2.1.

Table 5-2. Netlist of the Pspice LOSSY_LSDCM Model

```
* Large signal discontinuous conduction voltage mode model
* (including ESR of the inductor, on-resistance of switches and diode voltage drop)
* Params: Rmphite→External ramp height, Valleyv→Valley voltage of external ramp
* LFIL→Filter inductance, FS→Operating frequency
* rs→on-resistance of the active switch, rd→on-resistance of the diode
* Vd→diode forward voltage drop, RL→ESR of the inductor
* Pins: active (A), passive (P), common (C), control voltage (Vc)
.subckt LOSSY_LSDCM A P C Vc Params: RMPHITE=2 VALLEYV=1 FS=50k
+                                    LFIL=500u RL=0 RS=0 RD=0 VD=0
emod    d     0   table { (v(vc)-VALLEYV)/RMPHITE} = (.01, .01) (.99, .99)
remod   d     0   1g
etbl    anum  0   value={2*LFIL*FS*i(vxy)}
ranum   anum  0   1g
emew    mew   0   value={v(d)*v(d)*v(a,n)/v(anum)}
gac     a     m   value={v(mew)*i(vxy)}
ecp     x     p   value={v(mew)* (v(a,m)+v(n,c))}
rmew    mew   0   1g
vxy     x     y   0
ers     m     n   value={v(mew)*i(vxy)*4*RS/3/v(d)}
evdrd   y     n   value={i(vxy)*4*RD*v(mew)/3/v(d)+VD*SGN(i(vxy))}
erl     n     c   value={v(mew)*i(vxy)*4*RL/3/v(d)}
.ends
```

Another phenomenon about the equivalent resistors (Equations 5.7 and 5.8) is that although their dependency on control duty ratio is somewhat different, the voltages across them turn out to have the same expressions as given below:

$$v_r = \frac{4}{3}\frac{\mu i_p}{d} r$$

where r is the ESR of the inductor or on-resistances of the switches. This relation has been used in the netlist to describe the controlled voltage sources *evdrd*, *esr* and *esl*.

To show that Fig. 5-7 is a more accurate model when conduction losses are considered, the LOSSY_LSDCM and the available Pspice VMLSDCM models are applied to the Buck converter and the Boost converter to study the steady state and load transient performances. The results are then compared with those obtained from cycle-by-cycle simulation of the actual converter circuits. It should be pointed out that for ideal converters, the LOSSY_LSDCM model is identical with the Pspice VMLSDCM model, as can be seen from Fig. 5-7.

Therefore, simulation results will be characterized by the following three approaches: (a) cycle-by-cycle simulation of the actual converter, (b) simulation using the derived LOSSY_LSDCM model, and (c) simulation using the Pspice VMLSDCM model but with the resistors connected outside the model terminals.

The following circuit and operation parameters are used in the simulation:

1. Buck converter: V_{in}=24V, d=0.25, f_s=50kHz, L=20μH, C=47μF and sudden load changes (from 6Ω to 3Ω) occur at t=1ms.
2. Boost converter: V_{in}=24V, d=0.25, f_s=50kHz, L=10μH, C=47μF and sudden load changes (from 12Ω to 9Ω) occur at t=1ms.

Comparison is first made to show the steady state and transient output voltages for both converters with small conductive resistances (r_L=0.1Ω, r_s=0.2Ω, r_d=0.11Ω, V_d=0.8V). Simulation results are given in Fig. 5-9 for the Buck converter and Fig. 5-10 for the Boost converter. With these circuit parameters, it is easy to test that Equations 5.1 and 5.2 are satisfied, which means that circuit time constants are much larger than the charging and discharging time of the inductor in each switching period.

Figures 5-9 and 5-10 show clearly that the derived model is much more accurate than the existing lossless model. Since the conductive resistances are small, energy losses on these resistors are also small. It is therefore expected that both models should give approximate output voltages. As can be measured from Fig. 5-9 for the Buck converter, the load voltage predicted by the existing model is only 1.54% greater than that predicted by the derived model when the load resistance is 6Ω. This figure changes to 1.82% when the load resistance reduces to 3Ω. For the Boost converter, as can be seen from Fig. 5-10, difference between the voltages predicted by both models is more pronounced but this difference is still only 2.97% and 2.60% of the voltage of the derived model at 12Ω and 9Ω load resistance, respectively.

Next the resistors are intentionally increased in order to test the accuracy of the derived model under conditions that requirements given by Equations 5.1 and 5.2 are not satisfied. Output voltages for the Buck converter and the Boost converter with large conductive resistances (r_L=0.5Ω, r_s=0.5Ω, r_d=0.61Ω, V_d=0.8V) are shown in Fig. 5-11 and Fig. 5-12, respectively.

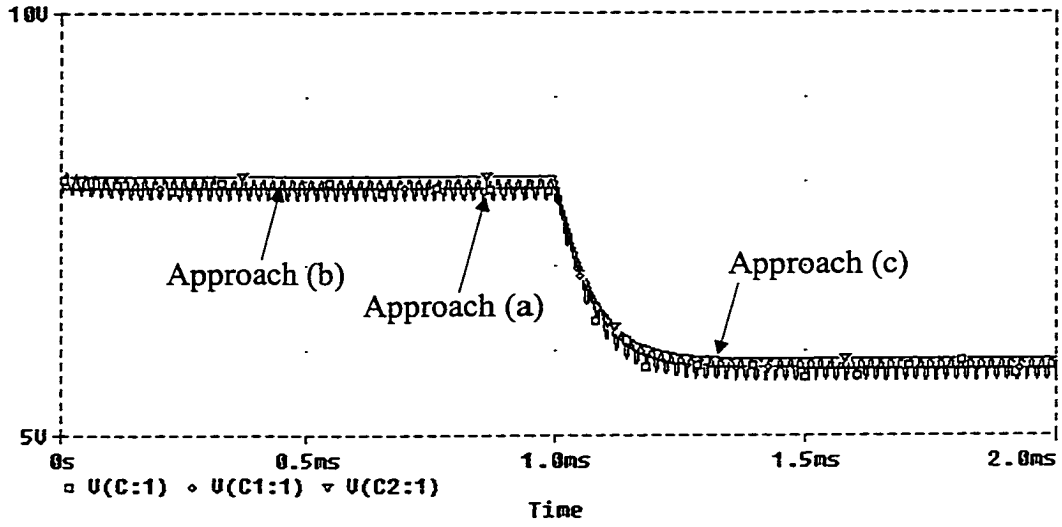


Fig. 5-9. Simulation results for the Buck converter with small conduction losses.

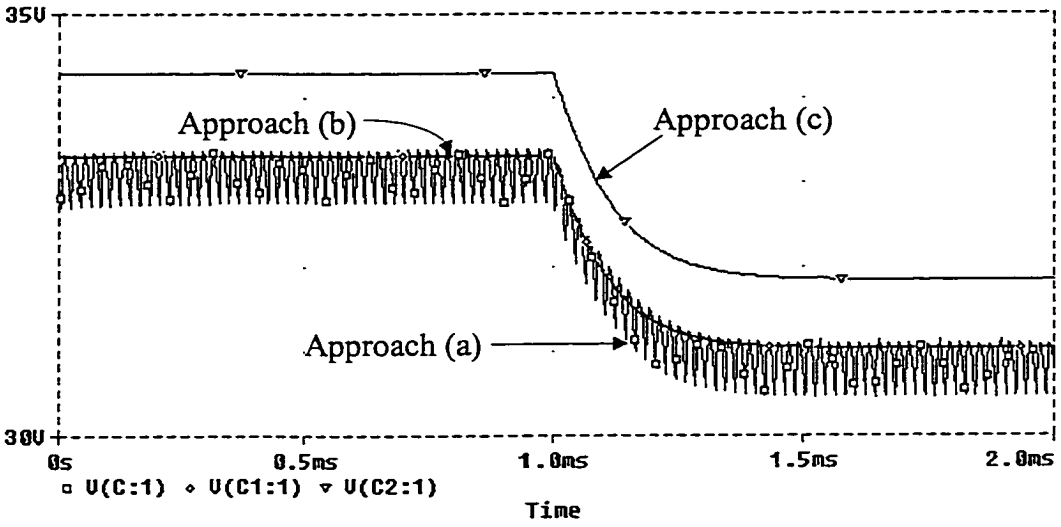


Fig. 5-10. Simulation results for the Boost converter with small conduction losses.

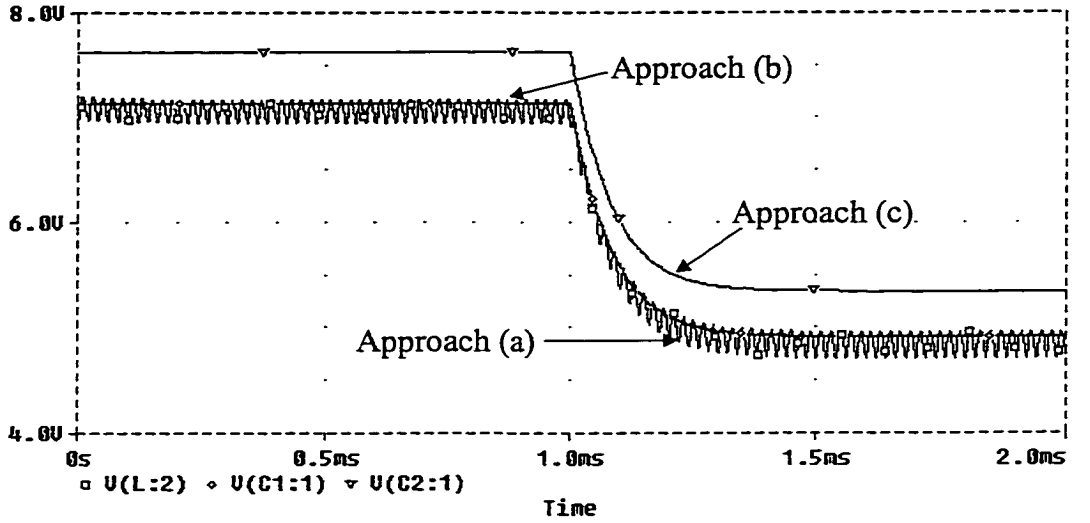


Fig. 5-11. Simulation results for the Buck converter with large conduction losses.

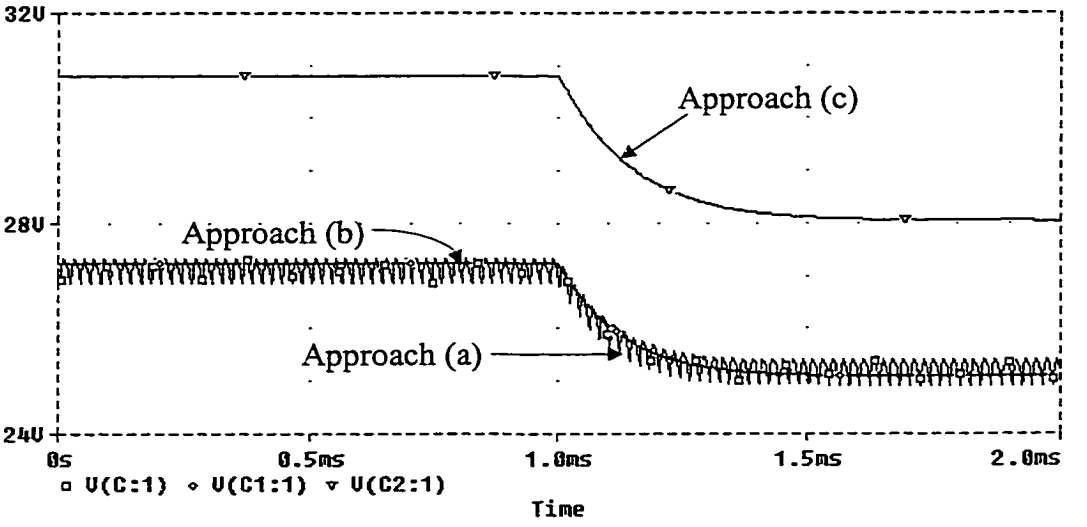


Fig. 5-12. Simulation results for the Boost converter with large conduction losses.

It is found from Figs. 5-11 and 5-12 that even with large conduction losses, the load voltage predicted by the derived model still tracks the actual converter output voltage precisely. On the other hand, the existing model generates noticeable errors that are 6.98% greater at 6Ω and 8.80% greater at 3Ω load resistor for the Buck converter, and are 13.1% greater at 12Ω and 11.8% greater at 9Ω load resistor for the Boost converter. The improved accuracy of the derived model can be explained by the fact that even though the average switch and inductor currents deviate from that in the ideal converter, there is a significant difference between the *rms* value and the average value of these currents. More losses have therefore been accounted for in the derived model as are with the actual converter.

With the derived large-signal model available, we can now proceed to study how non-ideal components affect the dynamic behavior of PWM converters. This can be done by either linearizing the model around a steady-state operation point or simply use the circuit simulator to generate the bode plots. Figures 5-13 and 5-14 compare the simulated control-to-output and input-to-output transfer functions for the ideal Buck converter and the non-ideal Buck converter with large conduction losses.

From these two figures, it can be noted that the converter is a second order system as acclaimed in [62]. As is expected, the two poles for both cases are well separated. The non-ideal converter presents slightly smaller gain and is also slightly more damped. It is estimated from these figures that both transfer characteristics have almost the same resonant frequency of about 5.17kHz, a dominant pole of slightly greater than 1kHz and a second pole of greater than 25kHz. These results agree very well with theoretical

expectation [62] for the ideal Buck converter with a resonant frequency of 5.19kHz, a pole at 1.43kHz and another one at 31.2kHz.

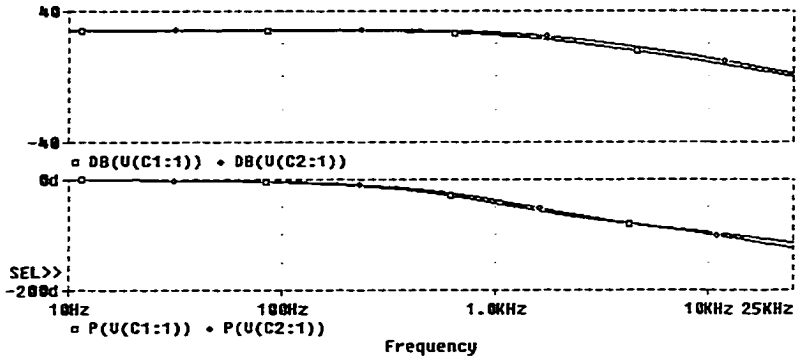


Fig. 5-13. Control-to-output transfer functions of the ideal (◊) and non-ideal (□) Buck converters with a load resistance of 6Ω.

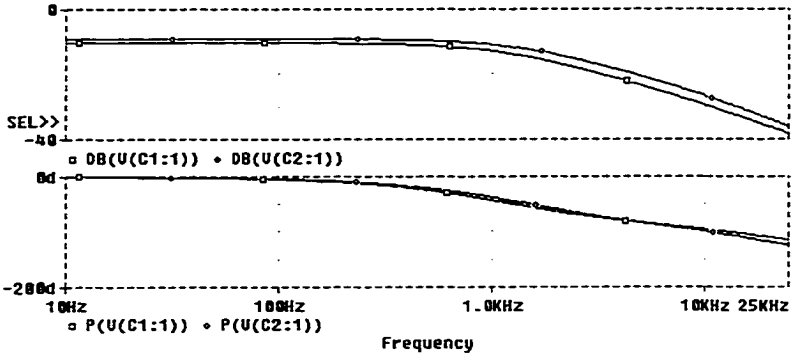


Fig. 5-14. Input-to-output transfer functions of the ideal (◊) and non-ideal (□) Buck converters with a load resistance of 6Ω.

Frequency characteristics of the ideal and non-ideal Boost converter can also be obtained. They are shown in Fig. 5-15 for the control-to-output and in Fig. 5-16 for the

input-to-output relations. Similar conclusions with respect to pole position and damping can also be drawn as with the Buck converter. A common property of the bode plots shown from Fig. 5-13 to Fig. 5-16 is that conduction losses do not have significant effect on the dynamic behaviors of the Buck and the Boost converter except for the reduction of the gain in the transfer functions. It is also noted that the open loop gain of the Boost converter is more sensitive to the ESR of the inductor and on-resistance of the switch.

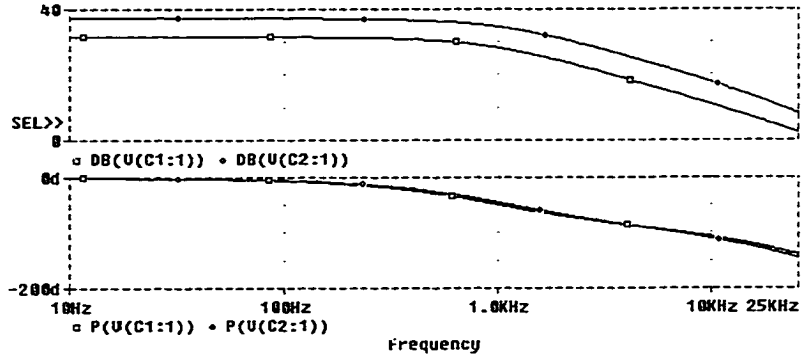


Fig. 5-15. Control-to-output transfer functions of the ideal (◊) and non-ideal (□) Boost converters with a load resistance of 12Ω.

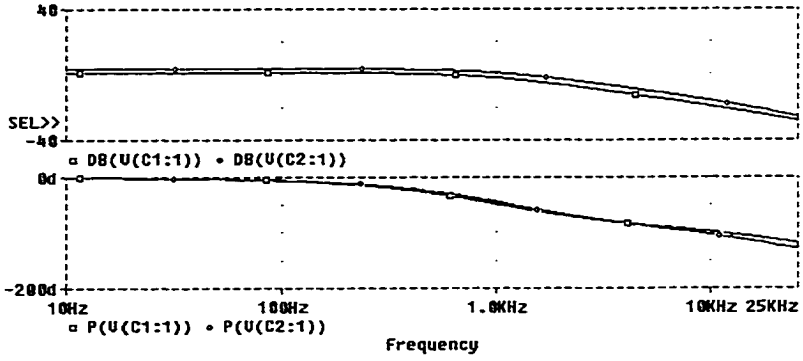


Fig. 5-16. Input-to-output transfer functions of the ideal (◊) and non-ideal (□) Boost converters with a load resistance of 12Ω.

5.4 Dynamic Modeling of Single-Switch PWM PFC Converters

As has been described in Chapter 2 and Chapter 4, a large group of PFC converters use only one active switch to control line current and to regulate output voltage. Modeling of such converters using the well-known state-space averaging method is cumbersome and the resulting model is not easy to use either. On the other hand, the three-terminal PWM switch modeling approach preserves the physical perception of the converter and is also easy to apply to perform small-signal and transient analyses. This approach, however, could not be applied directly to many popular PFC converters.

In this section, an extended PWM switch modeling approach which does not rely on identifying a physical three-terminal switch in a converter is proposed. The approach will be illustrated by the PFC circuit discussed in Chapter 4 (Fig. 4-1). It will be shown that the derived model can be easily implemented into the Pspice library to facilitate steady state and transient analyses. The modeling technique introduced can be easily applied to other single-switch PFC converters operating in DCM condition. Verification of the derived model is also given.

5.4.1 Derivation of the PWM Switch Model

First, the PWM switch of the front-end boost stage can be easily identified. It should be noted that even though the output diode (passive switch) is not present in this stage, the operation of the choke inductor L is exactly the same as that in the Boost converter with its charging voltage to be $v_g(t)$ (rectified line voltage) and discharging

voltage to be ($2v_{cs}$-$v_g(t)$). The function of the passive switch is realized by the rectifying bridge and other circuit components.

Next, the energy transfer pattern of the forward stage will be investigated. In order to clearly understand the operation of the two leakage inductors L_1, L_2, the waveform of the leakage current ($i_{L2}(t)$ for example) in a switching cycle was redrawn in Fig. 5-17. It is found that the charging slope is proportional to the difference between the input (v_{cs}, storage capacitor voltage) and the reflected output voltage, the same manner as that in the traditional forward converter. However, the discharging slope is now proportional to the sum of the input and the reflected output voltage. This is in sharp contrast to the traditional forward converter where the energy transfer inductor is discharged by the output voltage only. It is this interesting energy transfer pattern that prohibits the direct application of the well-known PWM modeling technique.

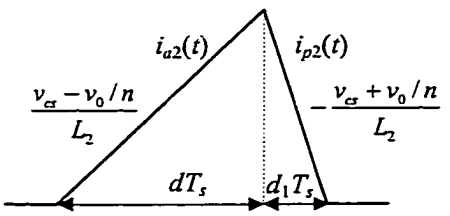


Fig. 5-17. Leakage inductor current waveform ($i_{L2}(t)$).

To correctly model the energy transfer from storage capacitors to the load through leakage inductors, a fictitious switching circuit consisting of an active switch, S_a, a passive switch, D_a and an ideal 1:1:1 three winding transformer as shown in Fig. 5-18 is

constructed to accomplish the desired functionality. With S_a operates synchronously with the main switch S in Fig. 4-1, one can easily verify that the inductor is charged by (v_{cs}-v_0/n) and discharged by (v_{cs}+v_0/n) similar to that in the actual circuit. In the following derivation steps, the same assumption with respect to storage capacitors and leakage inductors is also made as that in Chapter 4, i.e., $C_{s1} = C_{s2} = C_s$, $v_{cs1} = v_{cs2} = v_{cs}$ and $L_1 = L_2 = L_f$, $i_{L1}(t) = i_{L2}(t) = i_f(t)$. Therefore, analysis can be concentrated on one inductor current. In addition, we use the notation $i(t)$ to denote the instantaneous current and i to denote its average value over a switching cycle.

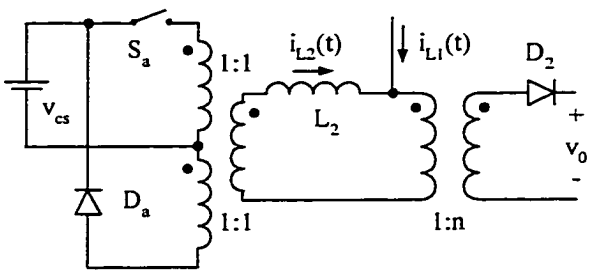


Fig. 5-18. A fictitious circuit which generates the current waveform in Fig. 5-17.

The switching circuit of Fig. 5-18 can be further simplified as shown in Fig. 5-19. Since the transformer is assumed to be ideal, diode D_2 can be removed as its function is accomplished by the fictitious diode D_a. From Fig. 5-19, it is obvious that,

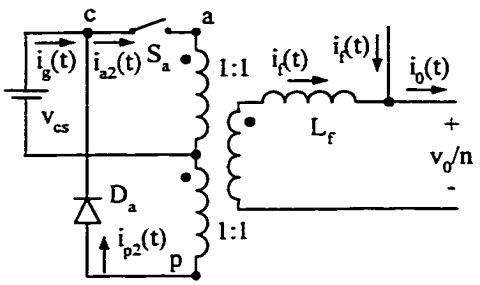


Fig. 5-19. Simplified fictitious switching circuit of Fig. 5-18.

$$i_{a2} = \frac{1}{2} i_{pk} d, \quad i_{p2} = \frac{1}{2} i_{pk} d_1 \tag{5.14}$$

or

$$i_{a2} = \frac{d}{d_1} i_{p2} \tag{5.15}$$

where i_{pk} is the peak value of current $i_f(t)$

However, i_{pk} can also be expressed as,

$$i_{pk} = \frac{v_{ca}}{L_f} d T_s = \frac{v_{cp}}{L_f} d_1 T_s \tag{5.16}$$

or

$$v_{ca} = \frac{d_1}{d} v_{cp} \tag{5.17}$$

In the above expressions, T_s is the switching period (T_s=1/f_s) and $d_1 T_s$ is the discharging time of current $i_f(t)$

From Equations 5.14 to 5.17, the following relationship between the average voltage and current can be obtained:

$$i_{a2} = \mu_2 i_{p2}, \quad v_{cp} = \mu_2 v_{ca} \tag{5.18}$$

$$\mu_2 = \frac{d}{d_1} = \frac{d^2}{2L_f f_s} \frac{v_{cp}}{i_{a2}} = \frac{d^2}{2L_f f_s} \frac{v_{ca}}{i_{p2}} \tag{5.19}$$

The large-signal average model following these equations is given in Fig. 5-20. This model can now be inserted into the PFC converter circuit to derive the complete model. However, the model given in Fig. 5-20 contains a three-winding transformer and it is not in a form that can be used conveniently. It will be more desirable if a relationship between the input and output can be directly established. This will be accomplished through the following algebraic calculations (suppose the center tap of the transformer is also grounded):

$$i_g = \mu_2 i_{p2} - i_{p2} = (\mu_2 - 1) i_{p2}$$

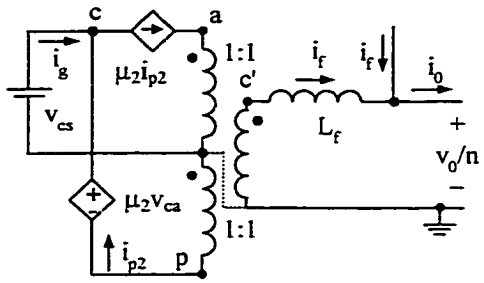


Fig. 5-20. PWM switch model of the fictitious switching circuit.

$$i_f = \mu_2 i_{p2} + i_{p2} = (\mu_2 + 1)\, i_{p2}$$

$$i_g = \frac{\mu_2 - 1}{\mu_2 + 1} i_f = \frac{\mu_2 - 1}{2(\mu_2 + 1)} i_0 \tag{5.20}$$

and

$$v_{cs} + v_{c'} = v_{cp} = \mu_2 v_{ca} = \mu_2 (v_{cs} - v_{c'}) \tag{5.21}$$

$$v_{c'} = \frac{\mu_2 - 1}{\mu_2 + 1} v_{cs} \tag{5.22}$$

also,

$$i_{a2} = \mu_2 i_{p2} = \frac{\mu_2}{\mu_2 + 1} i_f = \frac{\mu_2}{2(\mu_2 + 1)} i_0$$

From Equations 5.21 and 5.22,

$$v_{cp} = \left(\frac{\mu_2 + 1}{\mu_2 - 1} + 1\right) v_{c'} = \frac{2\mu_2}{\mu_2 - 1} v_{c'}$$

According to Equation 5.19,

$$\mu_2 = \frac{d^2}{2L_f f_s} \frac{v_{cp}}{i_{a2}} = \frac{d^2}{2L_f f_s} \frac{4(\mu_2 + 1)}{\mu_2 - 1} \frac{v_{c'}}{i_0} \tag{5.23}$$

The final PWM switch model for the circuit shown in Fig. 5-19 can be easily deduced from Equations 5.20 to 5.23 and it is given in Fig. 5-21.

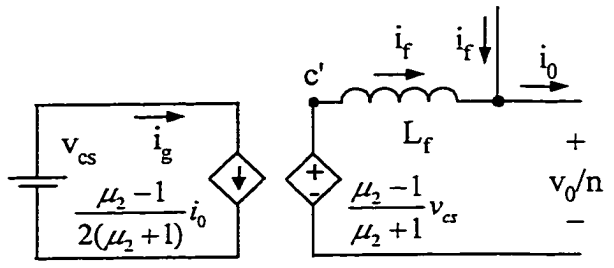


Fig. 5-21. Simplified PWM switch model of the fictitious switching circuit.

From Fig. 5-21, we may derive the steady-state relation between the load voltage V_0 and the storage capacitor voltage V_{cs}. Consider inductor L_f to be short circuited in steady state, we have,

$$\frac{V_{c'}}{I_0} = \frac{R}{n^2}$$

where R is the load resistance. Also, if we define,

$$k_2 = \frac{2n^2 L_f f_s}{R}$$

Equation 5.23 becomes,

$$\mu_2 = \frac{D^2}{k}\frac{4(\mu_2 + 1)}{\mu_2 - 1}$$

or

$$\mu_2 = \frac{k_2 + 4D^2 + \sqrt{(k_2 + 4D^2)^2 + 16k_2D^2}}{2k_2} \tag{5.24}$$

Therefore, the output voltage is given by,

$$\begin{aligned} V_0 &= \frac{\mu_2 - 1}{\mu_2 + 1} n V_{cs} = \frac{4D^2}{k_2 \mu_2} n V_{cs} \\ &= \frac{\sqrt{(k_2 + 4D^2)^2 + 16k_2D^2} - (k_2 + 4D^2)}{2k_2} n V_{cs} \end{aligned} \tag{5.25}$$

This expression is exactly the same as Equation 4.21 obtained from the state-space averaging method.

With the circuit model in Fig. 5-21 available, we are now ready to derive the complete large-signal model for the PFC converter. Recall that at the front-end boost stage, the output voltage is the sum of the two capacitor voltages, while each capacitor is charged by the same current flowing through the passive switch (not physically present in this converter). At the output forward stage, each capacitor provides a current i_f to the output through the leakage inductor L_f (Fig. 5-21). Therefore a complete circuit model can be obtained by placing the boost stage with its PWM switch model and the forward stage with the model shown in Fig. 5-21. The PWM switch model for the boost stage is available directly from the Pspice library as described in Section 5.2. Figure 5-22 shows the resulting circuit model, where

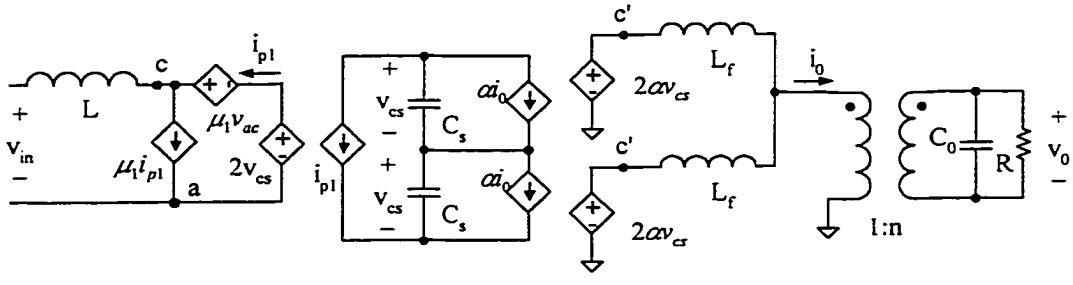


Fig. 5-22. The complete large-signal circuit model of the PFC converter.

$$\mu_1 = \frac{d^2}{2Lf_s}\frac{v_{ac}}{i_{p1}} \tag{5.26}$$

and α is defined as,

$$\alpha \triangleq \frac{1}{2}\frac{\mu_2 - 1}{\mu_2 + 1} \tag{5.27}$$

Circuit equivalent transformation can be applied to Fig. 5-22, resulting in a simplified model shown in Fig. 5-23 which further leads to a final complete large-signal model given in Fig. 5-24. In Figs. 5-23 and 5-24, v_1 is defined as,

$$v_1 \triangleq 2v_{cs} \tag{5.28}$$

With this definition and considering Equation 5.22, parameter μ_2 defined by Equation 5.23 will be reduced to a much simpler form as,

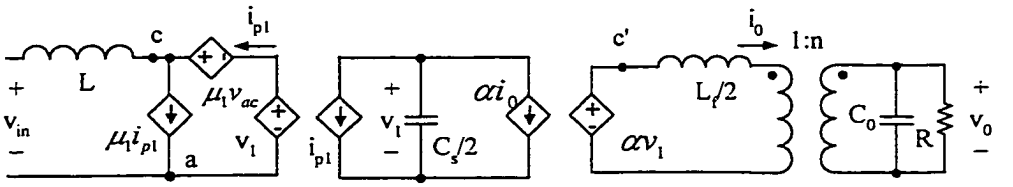


Fig. 5-23. Simplified circuit model of the PFC converter (v_1=$2v_{cs}$).

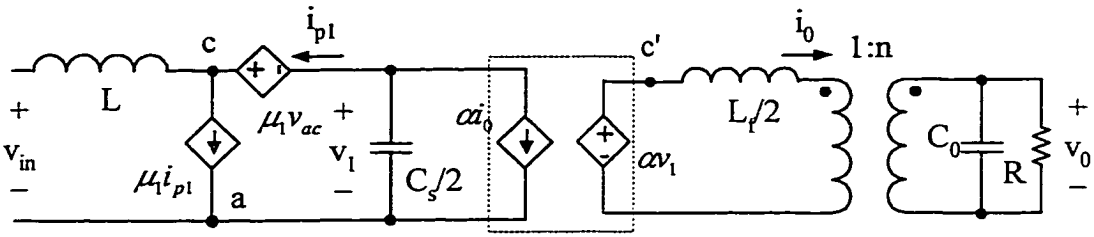


Fig. 5-24. The final large-signal circuit model of the PFC converter ($v_1=2v_{cs}$).

$$\mu_2 = \frac{d^2}{2L_f f_s}\frac{4(\mu_2+1)}{\mu_2-1}\frac{v_{c'}}{i_0} = \frac{d^2}{L_f f_s}\frac{v_1}{i_0} \tag{5.29}$$

Now let's take another approach to apply the PWM switch modeling technique in treating such a complicated switching network. The output forward stage of the discussed converter can be conceptually represented by a switching network block U1 as shown in Fig. 5-25. From previous discussion, average switch voltages and currents (over a switching period) with respect to the three-terminal PWM switch formed by S_a, D_a satisfy:

$$v_{qn} = \mu_2 v_{mq}, \quad i_{a2} = \mu_2 i_{p2} \tag{5.30}$$

where,

$$\mu_2 = \frac{d^2}{2L_f f_s}\frac{v_{mq}}{i_{p2}} \tag{5.31}$$

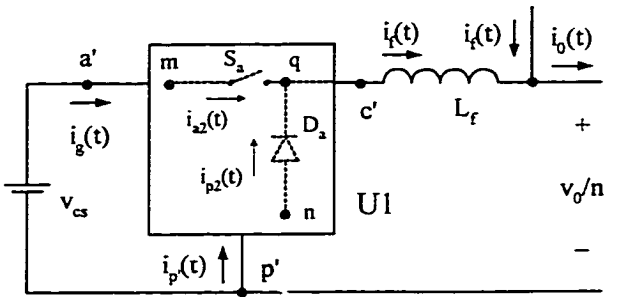


Fig. 5-25. Switching circuit block diagram of the output stage.

In Equation 5.30, v_{mq} is the voltage charging the leakage inductor and v_{qn} is the voltage discharging the inductor. According to the operation principle of the converter or Fig. 5-17, switching block U1 enables,

$$v_{qn} = v_{a'p'} + v_{c'p'}, \qquad v_{mq} = v_{a'c'} \tag{5.32}$$

Substitute into Equation 5.30, we have,

$$v_{a'p'} + v_{c'p'} = v_{a'c'} + 2\,v_{c'p'} = \mu_2\, v_{a'c'}$$

or,

$$v_{c'p'} = \frac{\mu_2 - 1}{2} v_{a'c'} \tag{5.33}$$

Also,

$$v_{a'p'} = v_{a'c'} + v_{c'p'} = \frac{\mu_2 + 1}{2} v_{a'c'}$$

Therefore,

$$v_{a'c'} = \frac{2}{\mu_2 + 1} v_{a'p'} \tag{5.34}$$

$$v_{c'p'} = \frac{\mu_2 - 1}{\mu_2 + 1} v_{a'p'} \tag{5.35}$$

Considering node p' is grounded and $v_{a'p'} = v_{cs}$, Equation 3.35 is exactly the same as Equation 5.22.

Regarding average capacitor current i_g and leakage inductor current i_f, Fig. 5-17 clearly shows that i_f is the sum of currents i_{a2} and i_{p2}. However, i_g is equal to i_{a2} subtracted by i_{p2}. This is because the discharging leakage inductor current is flowing into the capacitor according to the operation principle of the converter. Therefore,

$$i_f = i_{a2} + i_{p2} = (\mu_2 + 1)\, i_{p2} \tag{5.36}$$

$$i_g = i_{a2} - i_{p2} = (\mu_2 - 1)\, i_{p2} \tag{5.37}$$

$$i_g = \frac{\mu_2 - 1}{\mu_2 + 1} i_f \tag{5.38}$$

This expression is also exactly the same as Equation 5.20.

Substitute Equations 5.32, 5.34 and 5.36 into Equation 5.31, same expression as Equation 5.29 about the coefficient μ_2 will be obtained, indicating that the large-signal model shown in Fig. 5-24 can also be obtained.

Relationship between the nonlinear controlled sources in the forward stage can be easily implemented into the Pspice library (Pspice netlist is provided in Table 5-3). With this library file, steady state and dynamic properties of the PFC converter will be studied.

Before moving to the next section to the DC and small-signal characteristics of the derived model, a brief discussion of the model will help to justify the resulting parameter values of the energy transfer components. It is noted from Fig. 5-24 that an equivalent capacitor with a capacitance of $C_s/2$ and a voltage of v_1 ($=2v_{cs}$) is present. This agrees with the fact that the output current of the boost stage charges the two storage capacitors in series. It is also argued, however, that the two capacitors are discharged in parallel at the output forward stage and the model should also reflect this fact. The argument can be explained from the point of view of the total amount of stored energy in the capacitors. It is easy to verify that this energy is $C_s v_{cs}^2$ in the two capacitors in the actual converter, which is exactly equal to that stored in the equivalent capacitor in the model. This amount of energy is required to hold the output voltage constant.

In addition, this PFC converter utilizes two leakage inductors to transfer energy from two storage capacitors to the load in parallel. This fact is also manifested in the model (Fig. 5-24) where the output buck-type converter stage has an inductor with its inductance equals $L_f/2$.

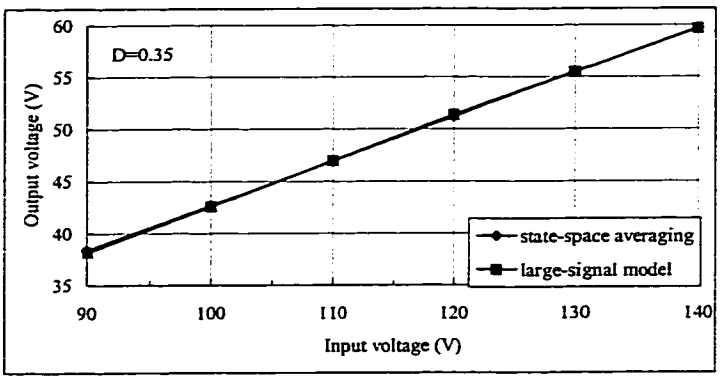
Table 5-3. Netlist of the Pspice FORWARD_LSDCM Model

```
* Large signal discontinuous conduction voltage mode model
* Params: Rmphite→External ramp height, Valleyv→Valley voltage of external ramp
* LFIL→Filter inductance, FS→Operating frequency
* Pins: active (A), passive (P), common (C), control voltage (Vc)
.subckt FORWARD_LSDCM  A  P  C  Vc  Params: RMPHITE=2 VALLEYV=1
+                                                FS=50k LFIL=500u
emode    d      0    table { (v(vc)-VALLEYV)/RMPHITE} = (.01, .01) (.99, .99)
rd       d      0    1g
etbl     anum   0    table {LFIL*FS*i(vxc)} = (-400,-400) (400,400)
ranum    anum   0    1g
emew     mew    0    value={v(d)*v(d)*v(a,p)/v(anum)}
gap      a      p    value={0.5*(v(mew)-1)*i(vxc)/(v(mew)+1)}
ecp      x      p    value={0.5*(v(mew)-1)*v(a,p)/(v(mew)+1)}
rmew     mew    0    1g
vxc      x      c    0
.ends
```

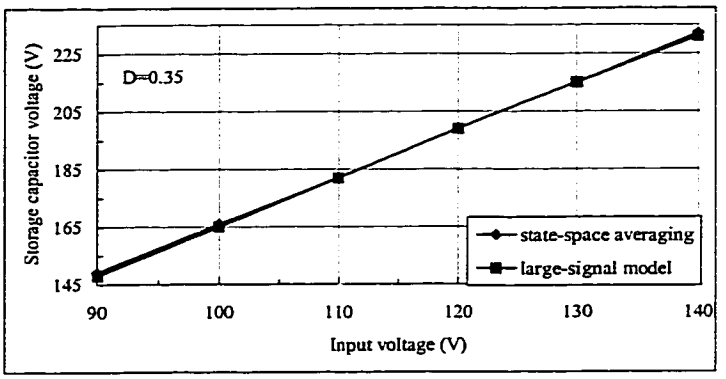
5.4.2 Verification of the Derived Model

To study the steady state property of the PFC converter, a DC voltage source is placed at the input of Fig. 5-24. The resulting storage capacitor voltage as well as output voltage are calculated through Pspice simulation and are to be compared with those obtained from state-space averaging method. The result is given in Fig. 5-26. To obtain these results, the following parameters are used and the duty ratio is fixed at D=0.35: n=0.27, L=482.3μH, L_f=80.9μH, C_s=820μF, C_0=900μF, f_s=50kHz and R=50Ω. It can be

seen that when input voltage changes from 90V to 140V, both the model and the state-space averaging methods predict almost the same DC results, as shown by the perfect overlay of the two curves.



(a) Output voltage vs. input voltage

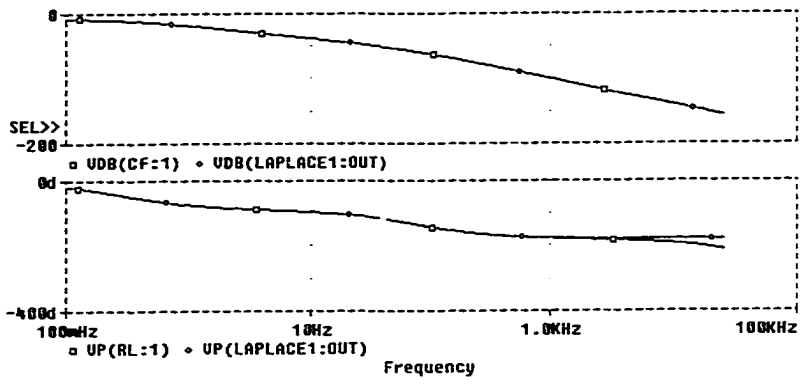


(b) Storage capacitor voltage vs. input voltage

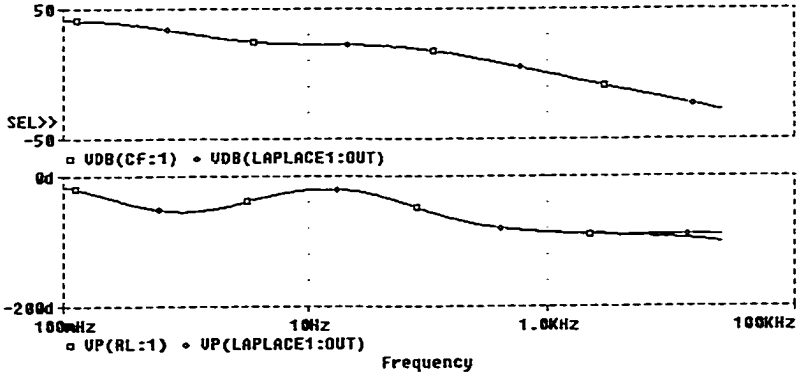
Fig. 5-26. Steady-state output and capacitor voltages from two approaches.

The Pspice AC sweep function is used to generate the bode plots of the model. Fig. 5-27 shows the input-to-output and control-to-output frequency response of the derived model when DC input voltage is 120V and duty ratio is 0.34. These results are

also compared with the bode plots obtained from the state-space averaging method presented in Chapter 4. It is noticed that they agree perfectly with each other at low frequency range. When frequency increases, the derived model predicts more phase delays which clearly indicate that the PFC converter discussed is not a second order system as is predicted by the state-space averaging method. In fact, the model presents a fourth order converter since there are four storage elements in the circuit.



(a) line-to-output



(b) control-to-output

Fig. 5-27. Bode plots of the small-signal frequency responses of the derived model (◊-state space averaging model, □-derived model).

Figure 5-28 shows the closed loop load voltage transient waveform obtained from simulating the actual switching circuit and the derived model with a 120V DC input and a 50Ω to 100Ω load changes. It is seen that both responses are very close to each other. However, the cycle-by-cycle simulation result (thick line) resonates somewhat slower and also attenuates faster, which could be the effect of non-ideal diodes that are not considered in the derived model. In addition, the feedback controller is not optimized since the purpose is to evaluate how the derived model approximates the actual circuit performance.

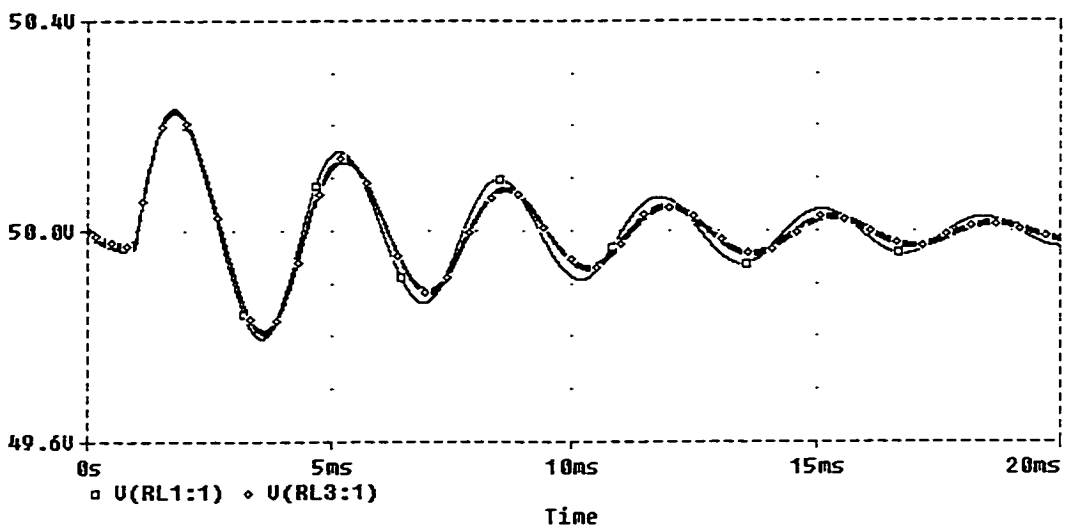
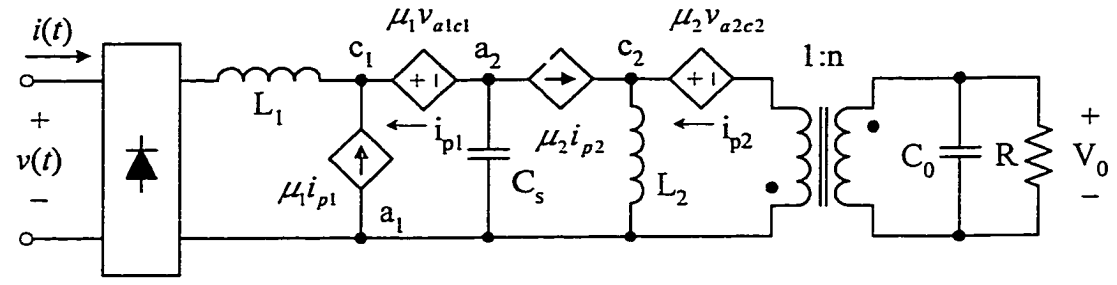


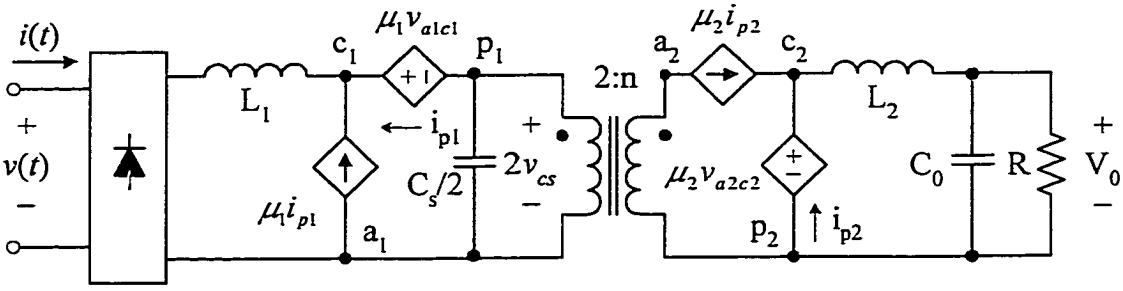
Fig. 5-28. Load voltage transient waveforms predicted by simulating the actual circuit (thick line) and the model under 50Ω to 100Ω load change.

5.4.3 Application of the Modeling Technique to Other PFC Converters

The extended PWM switch modeling technique that discussed in this section can be easily applied to derive many popular PFC converters. This method does not rely on identifying the three-terminal PWM switch structures. Instead, it concentrates on the charging and discharging of the inductor and the overall functionality of the switches. Figure 5-29 shows the large signal PWM switch models derived from the extended modeling technique for the two PFC converter circuits given in Figs. 1-7 (a) and 1-7(b) when they operate in DCM, in which,



(a) Boost/flyback combination circuit



(b) Boost/forward combination circuit

Fig. 5-29. Large signal models for the PFC converters given in Figs. 1-7(a) and 1-7(b).

$$\mu_1 = \frac{d^2}{2L_1 f_s}\frac{v_{a1c1}}{i_{p1}}, \quad \mu_2 = \frac{d^2}{2L_2 f_s}\frac{v_{a2c2}}{i_{p2}} \tag{5.39}$$

5.5 Summary

In this chapter, an implementation error of the DCM PWM switch model in the Pspice library is first identified and correction is provided. This modification enables power supply designers to correctly simulate the Boost converter. Then conduction losses in PWM converters are modeled and included in the PWM switch model based on equating the energy loss in the actual and average circuits. The resulting effect is that larger equivalent parasitic resistance is to be used in the model and this resistance is also duty ratio dependent. It is found that, in DCM PWM converters, conduction losses do not have significant effect on their dynamic responses except that open loop gain of the power stage is slightly reduced. It is also found that the steady state and dynamic behaviors of the Boost converter seem to be more sensitive to the conduction losses than that of the Buck converter.

Finally a more generalized PWM modeling method is described. This method does not rely on finding the three-terminal switch structure that is usually not directly available in present S^4-PFC converters. It can easily be applied to PFC converters in CCM or DCM operation as long as the charging and discharging voltage of the inductor is determined.

CHAPTER 6

CLOSED LOOP DESIGN OF A DISTRIBUTED POWER SUPPLY SYSTEM WITH POWER FACTOR CORRECTION

6.1 Introduction

Over more than thirty years, many alternative approaches for the design of switched-mode power supplies have been reported in the open literature. In many applications, the conventional centralized approach of using only a single bulky power processing unit was often a good choice. This bulky power unit or converter processes all the needed power and provides different voltage levels required by different loads or load converters. So far, extensive work has been done regarding the topological selection, analysis and design of this single converter scheme. System interaction between the single power converter and the downstream load converters were also studied [85, 86], where design guidelines ensuring stable operation of this scheme were developed in terms of output impedance of the former one and input impedance of the downstream converters. Although an optimized design could be achieved in some applications for this arrangement, it may lead to high manufacturing cost because of time and effort it takes for different power rating requirements.

An alternative approach to the single converter scheme is the distributed power system (DPS) scheme. The DPS structure distributes the needed power among several smaller power converters and then connects them in parallel to provide a common DC voltage bus to power one or several loads. This structure not only relieves the excessive electrical stresses on power switches and other components in the centralized bulky converter, but also allows the smaller power supply converters to be designed and manufactured into standard "plug-in" modules to enable the ease of system expansion and maintenance. Aside from these attractive features, the performance of a DPS structure heavily relies on a careful design of the control strategy to minimize the interactions among building modules. These interactions may develop a noticeable imbalance in the output current from module to module and degrade system performance and reliability.

Figure 6-1 shows the block diagram for the centralized and distributed power supply systems.

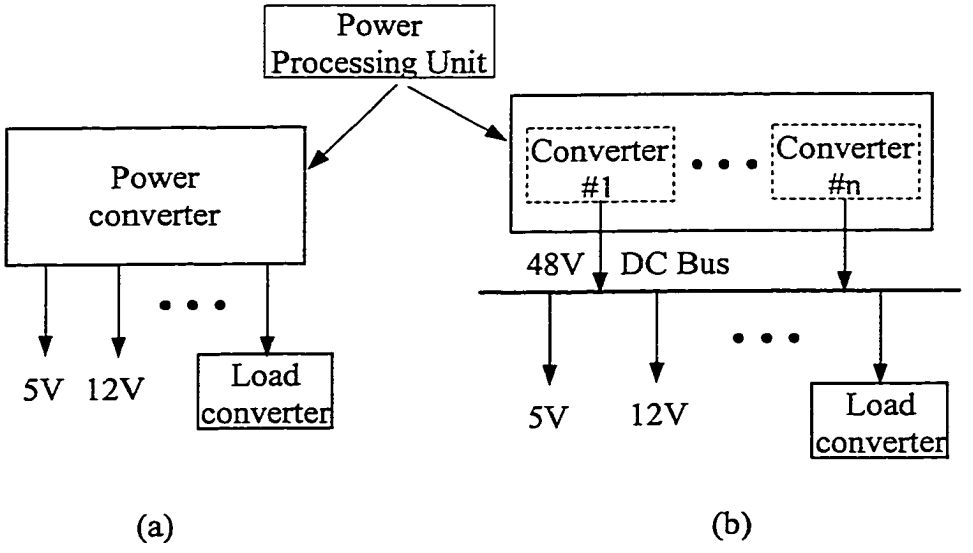


Fig. 6-1. Block diagram of two power supply systems: (a) centralized, (b) distributed.

Stability and dynamic characteristics regarding parallel operation of DC/DC converters have been studied extensively with the loop gain concept and classical control theory [87, 88]. In these studies, the parallel-connected converters were assumed identical so that a reduced-order power stage model can be used to avoid tedious calculations. In many off-line applications, it is desired that the distributed system must also provide high power factor and low THD when connected to the mains. However topics of DPS and PFC are usually discussed separately in the open literature. Paralleling of PFC converters has not been thoroughly studied and only a few papers were devoted to this subject [89]. Figure 6-2 shows a typical DPS in communication systems in which a number of AC/DC PFC converters provide the necessary DC power. In a DPS with PFC converters, line harmonic current suppression is also a critical issue in addition to other considerations in paralleling DC/DC converters. In this chapter, large signal transient behaviors for two parallel PFC converters discussed in the previous two chapters will be studies. The study will focus on closed-loop controller design of one DPS structure in achieving both high power factor in the input and equal load sharing between the two converter outputs.

6.2 Closed-Loop Design of Two Parallel PFC Converters

6.2.1 Description of Central Limit Control Scheme

A uniform current distribution among paralleling modules is of primary concern in a DPS. One of the factors affecting uneven load sharing is the unbalanced cable resistance from the load to each module's output. It has been demonstrated [90] that even

a small difference among cable resistances could drastically affect the output current of each module. Among various approaches the central limit control (CLC) scheme [90] shown in Fig. 6-3 is an effective one to control the current delivered by each module. In the CLC scheme, only a common reference voltage and one compensator are used. In order to achieve the desired current sharing, the current control signal of each converter is added to the output of the error compensator and the result is used as the control voltage of each PWM modulator. CLC scheme effectively minimizes the influence of circuit parameter discrepancies of each module on its output current and features precise output voltage regulation in DC/DC applications.

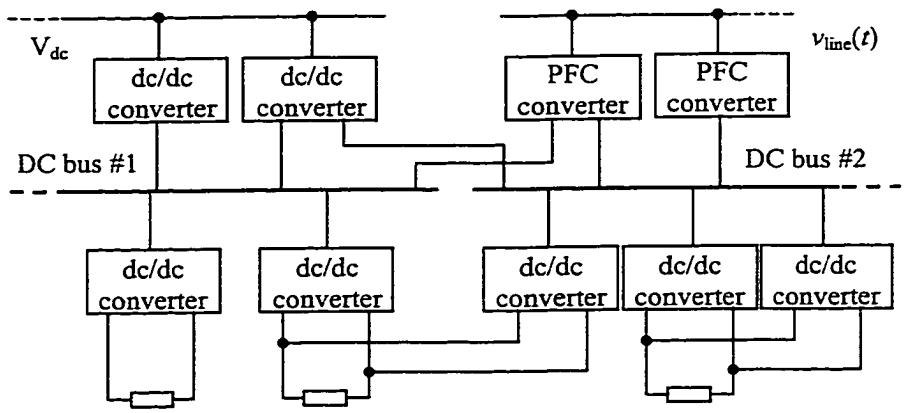


Fig. 6-2. Block diagram of a typical distributed power system.

In many high power applications, PFC converters operating in continuous conduction mode (CCM) are usually implemented with the current mode control and a current loop is included. In these converters, the compensator and CLC outputs v_{c1} and v_{c2} are used to determine the magnitude of the sinusoidal reference current. Thus the

scheme shown in Fig. 6-3 is suitable for PFC converters in both CCM and DCM modes. In this scheme, we included the cable resistance for converter #1 (R_{cb1}) and converter #2 (R_{cb2}). Current sharing is controlled by properly distributing current control signals i_{c1}, i_{c2} to each converter.

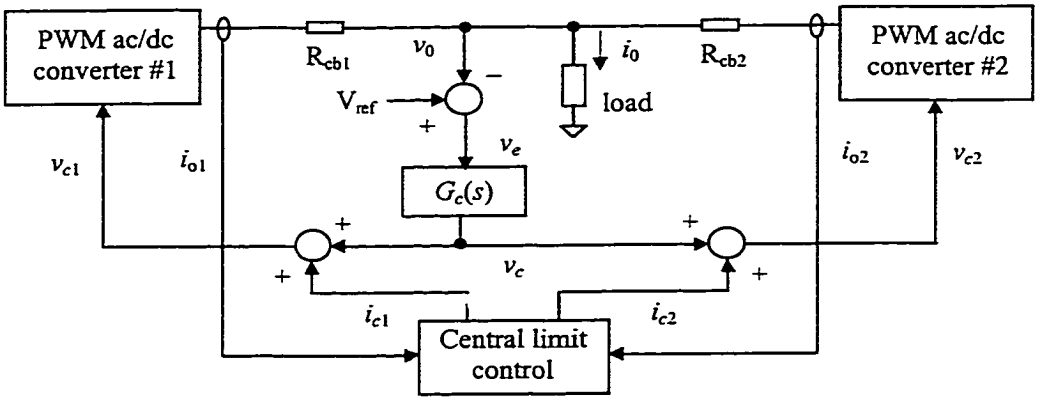


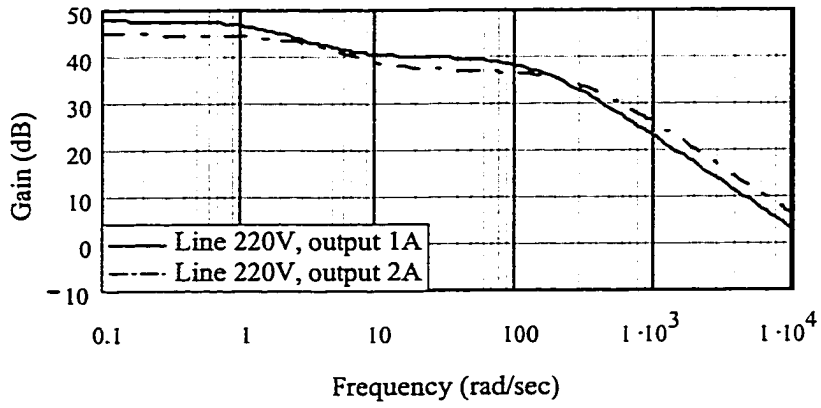
Fig. 6-3. Block diagram of a CLC scheme.

6.2.2 Voltage Loop Controller Design

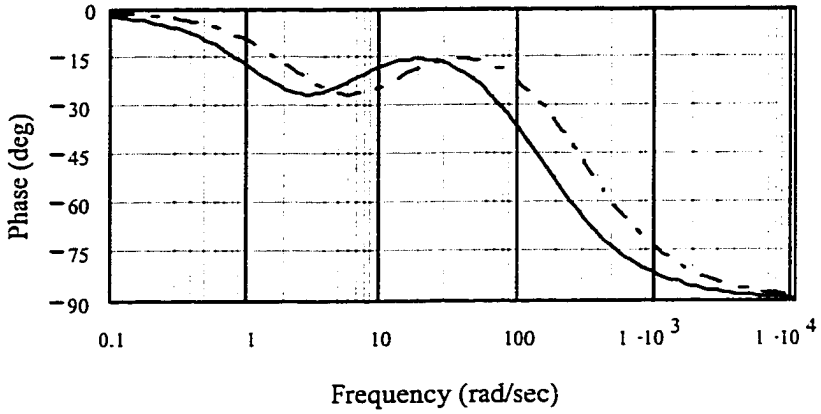
The major concern in simulating a closed-loop system is in the design of the compensator transfer function $G_c(s)$ to avoid unstable operation when the source voltage and/or load are subjected to large variations. These variations change the operation conditions of the converter circuits and therefore affect their dynamic characteristics. This effect becomes more pronounced in the low frequency range when these converters are operating in DCM conditions. Fig. 6-4 shows the bode plots of the control to output voltage transfer functions for each individual PFC converter discussed in Chapter 4 under 220V line and two different load conditions. They are given by,

$$H_{d1} = \frac{13942.7(s+4.32)}{s^2+141.5s+245.9}, \quad V_g = 220\text{V}, \quad I_{L1} = 1\text{A}$$

$$H_{d2} = \frac{19718(s+8.64)}{s^2+283s+983.5}, \quad V_g = 220\text{V}, \quad I_{L2} = 2\text{A}$$



(a)



(b)

Fig. 6-4. Control-to-output voltage frequency response of the AC/DC converter:

(a) magnitude, (b) phase.

More accurate transfer functions can be obtained directly from simulating the large circuit model derived in Chapter 5 (Fig. 5-24).

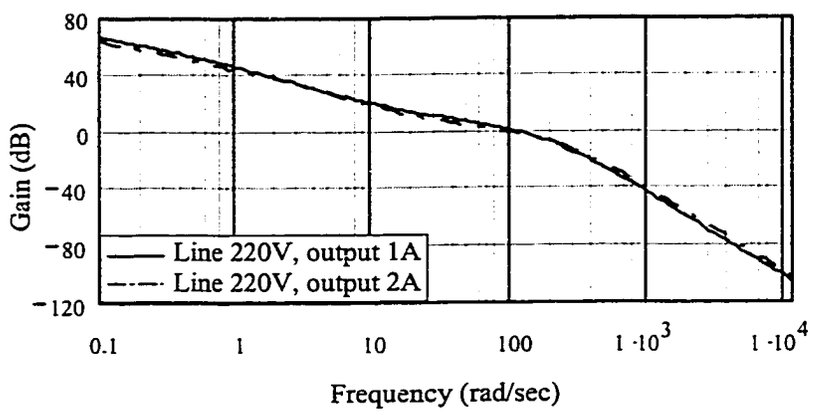
Unlike in DC/DC power supplies, design of AC/DC converters requires that the crossover frequency of the voltage loop gain should be no greater than one-fourth or one-third of the line frequency to avoid degradation of the input power factor. Unfortunately the PFC power stage exhibits a relatively small phase delay in this frequency range (approximately 20°-40°), which makes it impossible to compensate with a common 2nd order compensator. A systematic approach led to a 3rd order compensator design with its transfer function given as:

$$G_c(s) = \frac{39270(s+52.5)}{s(s+210)(s+105)}$$

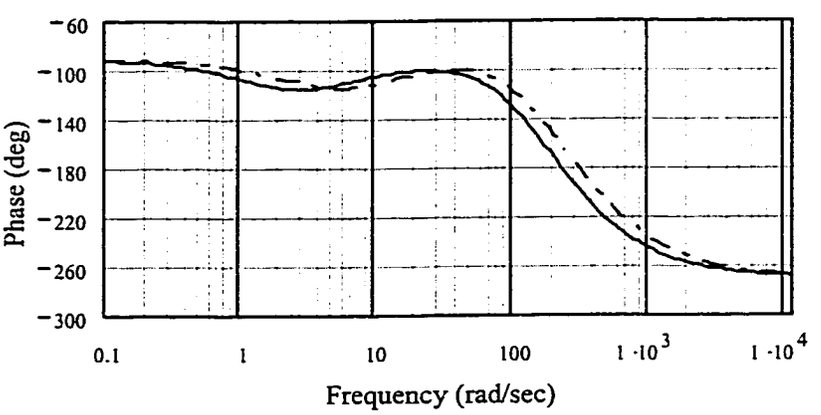
With the above transfer function, voltage loop gain for each converter can be depicted when voltage sampling gain and modulator gain are considered and it is shown in Fig. 6-5. It is seen that this compensator results in a 45° phase margin at crossover frequency f_{co}=16.7Hz when output current is 1A. It also gives a 65° phase margin at the other load condition.

The presence of non-zero R_{cb1} and R_{cb2} in Fig. 6-3 integrates the two converters into a mutually dependent system. Since current sharing and transient responses are concerned, a reduced-order power stage model as was used in [87, 88] can not be used. Studying the dynamic behavior of this system could be performed by cycle-by-cycle simulation of the actual PFC converter circuit. However, this approach is not encouraged

as it may take many hours for a circuit simulator to run just several line cycles because of the wide separation between the switching and line frequencies. In addition, detailed information about component voltages and currents within a switching period is not necessary, as we are more interested in the response of "average" input current and output voltage and current in the time scale of line periods. Because of this reason, large signal averaged model is particularly suited for transient study of PFC converter systems. Its application will be illustrated in the next two sections.



(a)



(b)

Fig. 6-5. Voltage loop gain for each AC/DC converter: (a) magnitude, (b) phase.

6.2.3 Current Loop Controller Design

Figure 6-6 is the block diagram for the current sharing control. It shows how the voltage command signal v_c (refer to Fig. 6-3) is modified and added to the signals i_{c1} and i_{c2} to influence the output voltage of each module.

Use of a single voltage compensator poses some requirements on the design of current controller $G_{ci}(s)$. First, let's consider the case when $G_{ci}(s)$ is a constant. Exact current distribution between the modules requires that current command i_{c1}, i_{c2} be superpositioned on v_c to generate an appropriate output voltage and not be zero even if the current error signal i_e is zero. However, this requirement could not be satisfied with a constant gain. Figure 6-7 shows the two output current with $G_{ci}(s) = 0.2$. It can be noticed that current error exists between the modules.

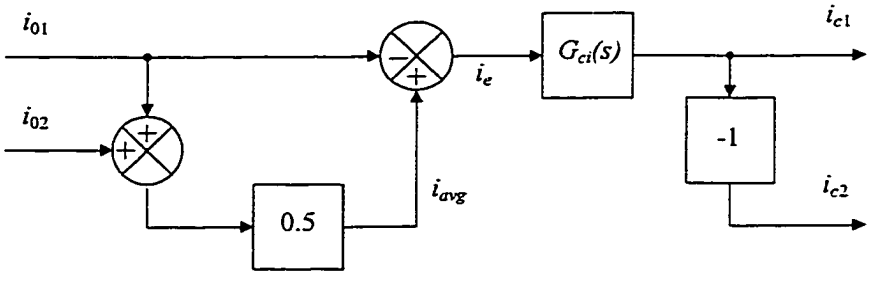


Fig. 6-6. Central limit current control scheme.

The above discussion suggests that the type of current loop gain be increased in order to achieve exact current sharing. The simplest approach is to include an integration

stage in the loop. Inclusion of an integrator in the loop also contributes to the elimination of the influences on current distribution because of non-identical modules. As was discussed in [91], crossover frequency of the current loop gain should be much higher than that of the voltage loop gain to ensure stability and to improve current control. Since the crossover of the voltage loop is relatively low in PFC converters, a current loop crossover of two decades above the voltage loop crossover would guarantee a prompt action in the current control. Limiting current loop bandwidth also helps to avoid high frequency switching noises. Figure 6-8 shows the bode plot of current loop gain with $G_{ci}(s) = \frac{10^4}{s}$. Figure 6-9 shows the corresponding output current of each module. It can be seen that with an integration stage included in the current loop, exact current sharing is obtained.

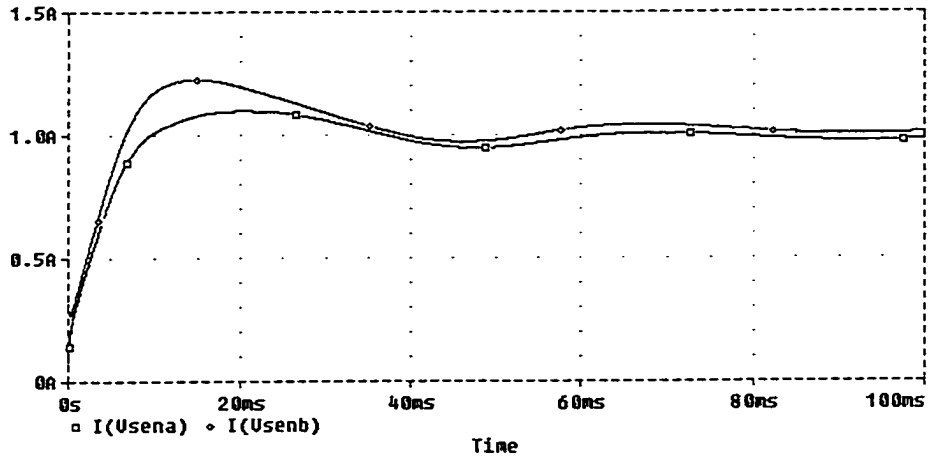


Fig. 6-7. Output current waveforms with $G_{ci}(s) = 0.2$.

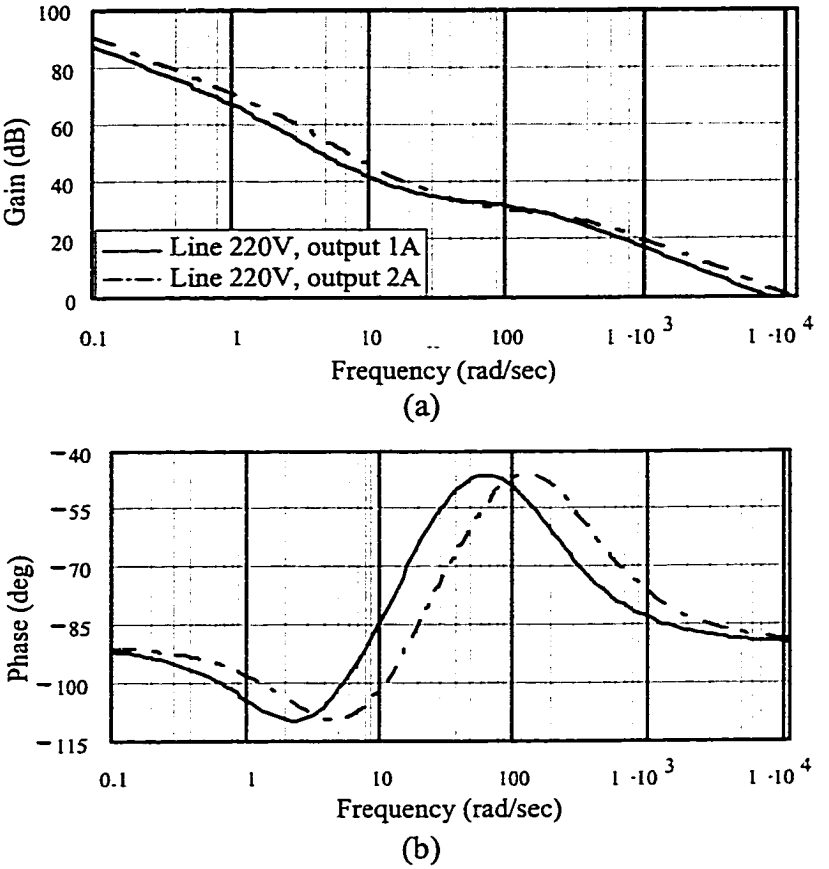


Fig. 6-8. Current loop gain for each AC/DC converter with $G_{ci}(s) = \frac{10^4}{s}$:

(a) magnitude, (b) phase.

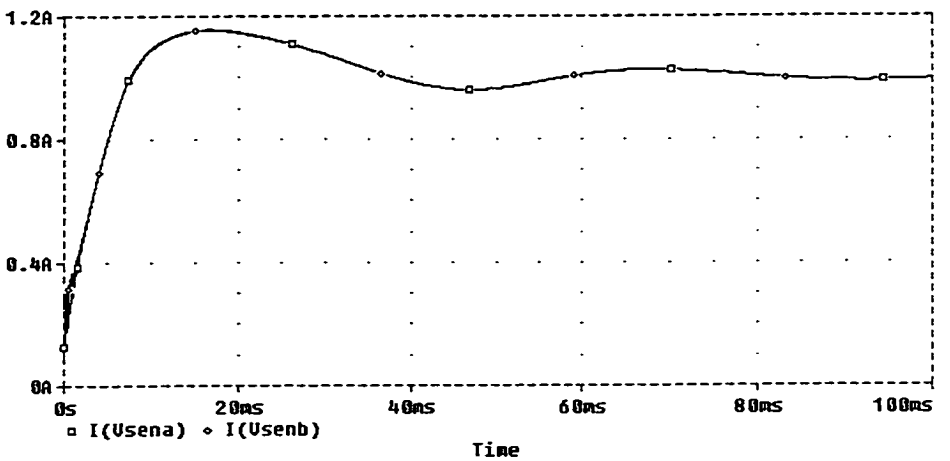
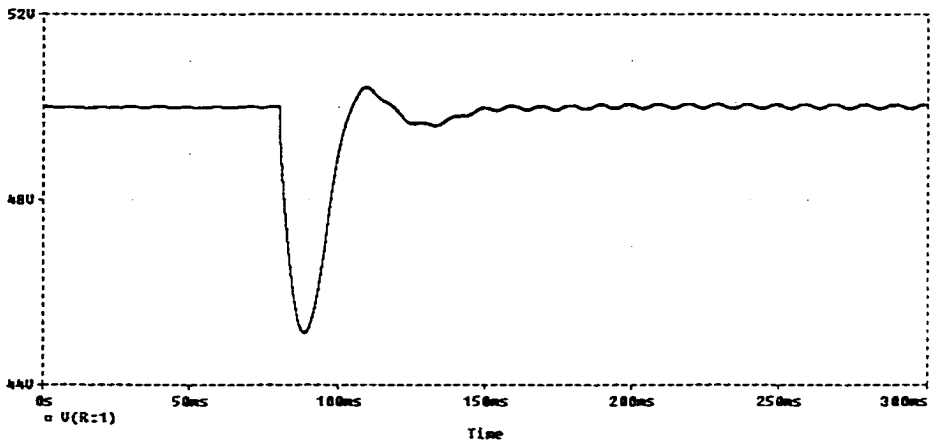


Fig. 6-9. Output current waveforms with $G_{ci}(s) = \frac{10^4}{s}$.

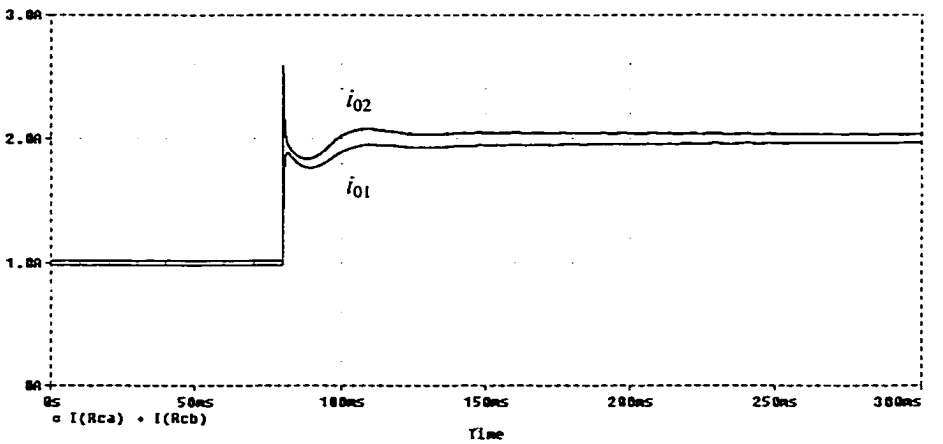
6.3 Simulation Results of the DPS with Power Factor Correction

The DPS utilizing CLC as shown in Fig. 6-3 was simulated using two 50VDC output voltage modules operating at 50kHz switching frequency. Stability and current sharing ability were examined under different load conditions with different cable resistance (R_{cb1}=0.8Ω and R_{cb2}=0.2Ω). First, actual converter module given in Fig. 4-1 with circuit parameters specified in Section 4.3 was utilized to examine the CLC performance with a constant current controller ($G_{ci}(s)$ = 0.2) when the common load current i_0 experiences a sudden increase (2A→4A) at t=80ms. The results are shown in Fig. 6-10. Converter modules were then substituted by the large signal model given in Fig. 5-24 and almost identical waveforms were generated (Fig. 6-11). It should be pointed out that simulation with the large signal model took less than 1% of the time needed with the actual converter circuit and no convergence problems encountered.

From Figs. 6-10 and 6-11, it can be seen that although the load voltage returns to the desired 50V, exact current sharing was not obtained. This could only be realized with an integration current controller as discussed in Section 6.2.3 and the waveforms are illustrated in Fig. 6-12. Notice that the transient waveform of the load voltage is not affected in these two cases. Fig. 6-13 shows that the averaged input current waveform is in phase with the line voltage. Its low frequency harmonic content, *THD* and the resulting power factor are listed in Tables 6-1 for the case when i_0 is 4A. Clearly a high power factor (*pf*) is obtained in the line input (97.9%).

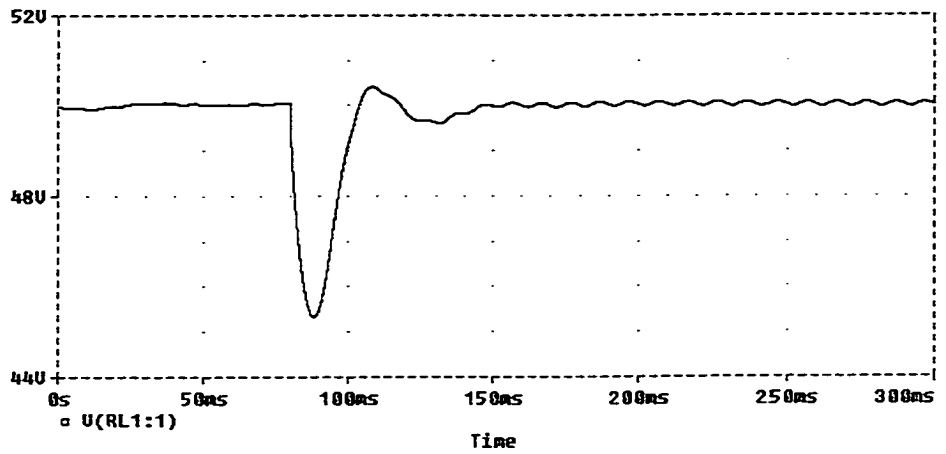


(a)

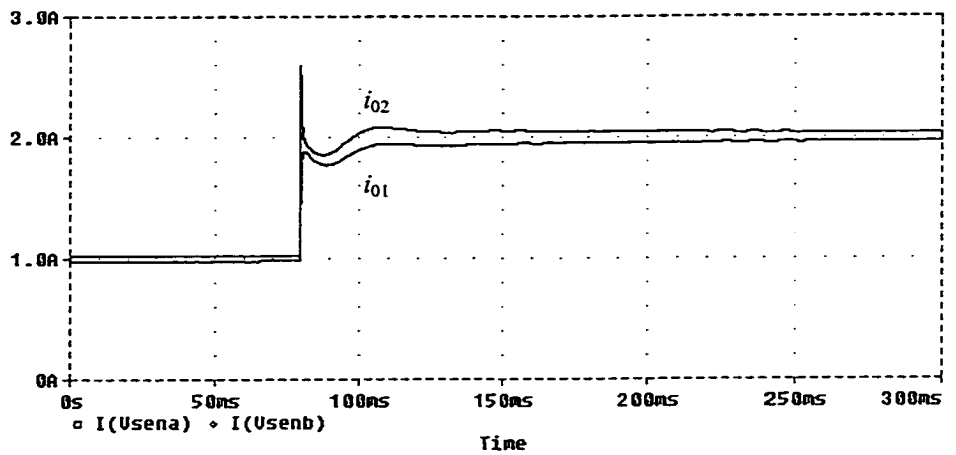


(b)

Fig. 6-10. Simulation waveforms using the actual switching circuit and a constant current controller: (a) load voltage (v_0), (b) output current of each converter.

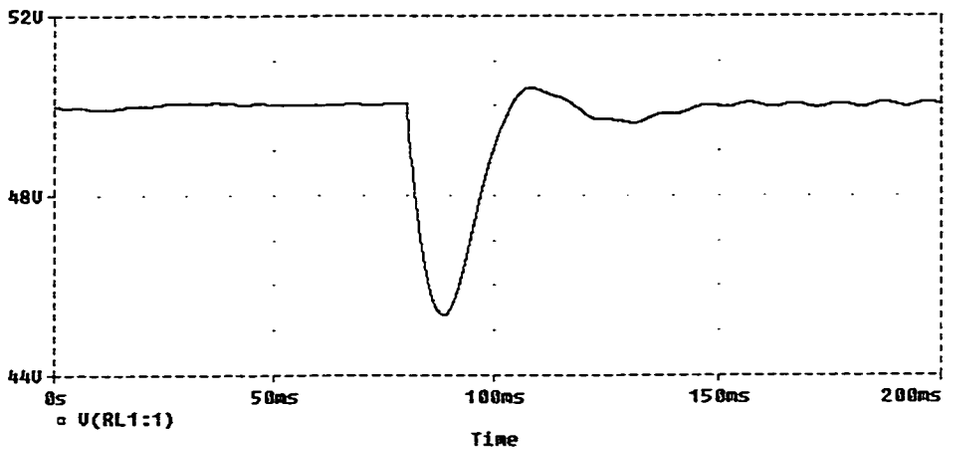


(a)

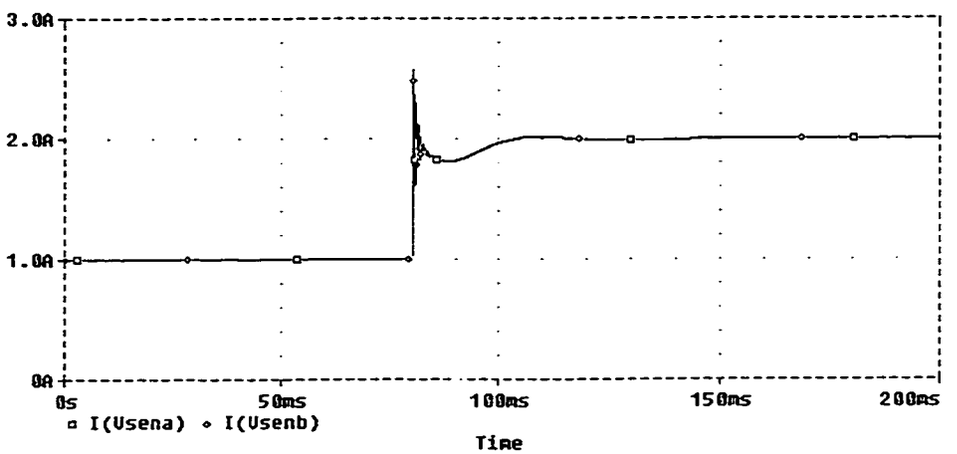


(b)

Fig. 6-11. Simulation waveforms using the large-signal model and a constant current controller: (a) load voltage (v_0), (b) output current of each converter.



(a)



(b)

Fig. 6-12. Simulation waveforms using the large-signal model and a constant current controller: (a) load voltage (v_0), (b) output current of each converter.

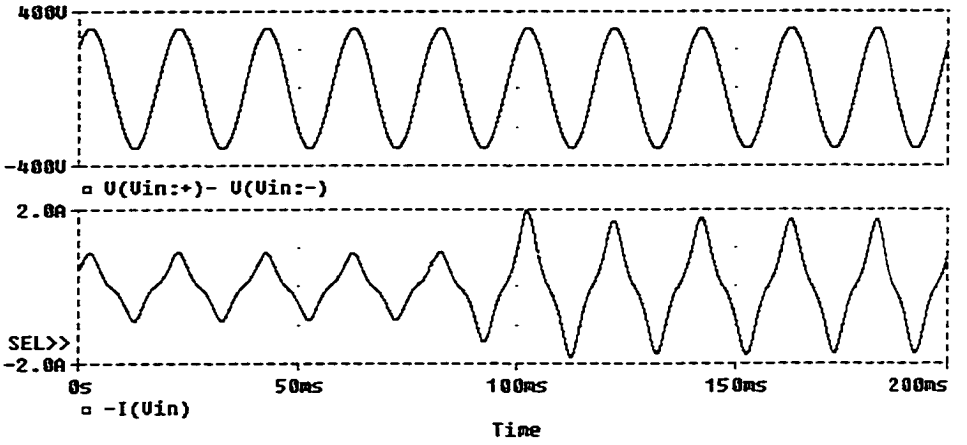


Fig. 6-13. Input voltage and current waveforms with sudden load change (2A→ 4A) at t=80ms.

Table 6-1. Harmonic contents in the line current (220V line and 4A load current)

Current (mA, *rms*)				*THD*	*pf*
I_1	I_3	I_5	I		
992.8	204.8	20.6	1013.9	20.7%	0.979

6.4 Summary

A parallel Distributed Power System (DPS) structure using two identical AC/DC PFC converters is presented in this chapter. Both voltage and current loop design of such a system is described based on the average model. It is suggested that a pole be placed in the current controller transfer function in order to achieve exact current sharing for a DPS utilizing central limit control scheme. The designed system achieved both high power factor at the input and stable load voltage regulation at the output. It also maintained a precise load current distribution even with unequal cable resistances from each converter

output to the load. Use of the large signal average model can save a great deal of time and effort in analyzing such complex systems.

CHAPTER 7

CONCLUSIONS

This dissertation is devoted to the dynamic modeling of switched-mode PWM converters with emphasis on single-switch single-stage power factor correction (S^4-PFC) converters. Harmonic contents and power factors of PFC converters utilizing the classical PWM converter as the front-end stage are also calculated.

It has been known that power factor and harmonic contents of PFC converters depend on the voltage conversion ratio of the front-end stage when it operates in DCM. These relationships are derived analytically in this dissertation. For S^4-PFC converters, however, this voltage conversion ratio is not directly controllable but is dependent on converter topology and operation conditions. The analytical result obtained provides power supply designers a quantitative reference in evaluating input characteristics of their design.

It is found that the small signal behavior of the PFC converter can be approximately determined using a DC input with its value equals the *rms* value of the AC line voltage. Although only one active switch is present in the S^4-PFC converter to control the power transfer from the AC line to the load, the power flow actually passes through two cascaded processing stages. Interaction between these two stages introduces

an extra LHP zero in the control-to-output transfer function if the front-end stage operates in DCM. This zero may bring some undesirable effects to the voltage controller design. This issue is discussed in Chapter 4.

A new averaged modeling approach has been developed utilizing the PWM switch concept. Deriving a large signal model based on this approach relies on identifying the charging and discharging voltages applied to the inductors instead of relying on identifying the three-terminal PWM switch which, in most cases, does not exist in S^4-PFC converters. Once these voltages are obtained, a fictitious switching network can be conceptualized to realize the functionality of the switch operation. This method is more accurate than the state-space averaging method since it remains the full system order. It is also much easier to use and can be easily implemented into the Pspice library. The large signal model obtained is especially useful in feedback control loop design and transient response study for complex converter systems as has been shown in a distributed power supply system with power factor correction.

Another important result obtained in this dissertation is that modeling of non-ideal PWM converters with conduction losses is studied. This issue has not been reported in the open literature except for converters operating in CCM and under small ripple conditions. The modeling approach proposed is based on the fact that the *average* and *rms* current values are different in every circuit branch of the PWM converter circuit. Maintaining equal conduction losses in the actual switching converter and its averaging model results in larger equivalent resistance to be used in the model. This resistance is also duty ratio dependent. Verification of the proposed method is provided with two

examples using a Buck converter and a Boost converter operating in DCM. The result shows that the Boost converter is more sensitive to conduction losses with respect to steady state and small signal frequency responses. In addition, the proposed method gives the same model as that reported previously when the converter operates in CCM and under small ripple conditions.

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