OPTIMIZATION AND DESIGN OF PHOTOVOLTAIC MICRO-INVERTER

by

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ABSTRACT

To relieve energy shortage and environmental pollution issues, renewable energy, especially PV energy has developed rapidly in the last decade. The micro-inverter systems, with advantages in dedicated PV power harvest, flexible system size, simple installation, and enhanced safety characteristics are the future development trend of the PV power generation systems. The double-stage structure which can realize high efficiency with nice regulated sinusoidal waveforms is the mainstream for the micro-inverter.

This thesis studied a double stage micro-inverter system. Considering the intermittent nature of PV power, a PFC was analyzed to provide additional electrical power to the system. When the solar power is less than the load required, PFC can drag power from the utility grid.

In the double stage micro-inverter, the DC/DC stage was realized by a LLC converter, which could realize soft switching automatically under frequency modulation. However it has a complicated relationship between voltage gain and load. Thus conventional variable step P&O MPPT techniques for PWM converter were no longer suitable for the LLC converter. To solve this problem, a novel MPPT was proposed to track MPP efficiently. Simulation and experimental results verified the effectiveness of the proposed MPPT.

The DC/AC stage of the micro-inverter was realized by a BCM inverter. With duty cycle and frequency modulation, ZVS was achieved through controlling the inductor current bi-directional in every switching cycle. This technique required no additional resonant components and could be employed for low power applications on conventional full-bridge and half-bridge inverter topologies. Three different current mode control schemes were derived from the basic theory of the proposed technique. They were referred to as Boundary Current Mode (BCM), Variable Hysteresis Current Mode (VHCM), and Constant Hysteresis Current Mode (CHCM) individually in this paper with their advantages and disadvantages analyzed in detail. Simulation and experimental

results demonstrated the feasibilities of the proposed soft-switching technique with the digital control schemes.

The PFC converter was applied by a single stage Biflyback topology, which combined the advantages of single stage PFC and flyback topology together, with further advantages in low intermediate bus voltage and current stresses. A digital controller without current sampling requirement was proposed based on the specific topology. To reduce the voltage spike caused by the leakage inductor, a novel snubber cell combining soft switching technique with snubber technique together was proposed. Simulation and experimental waveforms illustrated the same as characteristics as the theoretical analysis.

In summary, the dissertation analyzed each power stage of photovoltaic micro-inverter system from efficiency and effectiveness optimization perspectives. Moreover their advantages were compared carefully with existed topologies and control techniques. Simulation and experiment results were provided to support the theoretical analysis.

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CHAPTER ONE: INTRODUCTION

1.1 World Energy Status

Since the Industrial Revolution, fossil fuels have been extensively used. To release the energy stored in fossil fuels, combustion is required. During this process, a release of emissions and particulates is unavoidable into the atmosphere. Moreover, transportation, and extraction of fossil fuels cause environmental pollution along with serious consequences such as air pollution, water deterioration, soil degradation, and global warming.

Presently fossil fuels dominate the energy consumption in the world. Based on the statistics, 86.4% of the primary energy consumption in the world comes from fossil fuels[1], and 67.6%[2] of the electric energy consumption comes from fossil fuels. As energy demand in the world keeps increasing (which is expected to rise from 13934 TWh in 2001 to 24673 TWh in 2025 at an annual rate of 2.4%[3, 4]), with the reserves fossil fuels being very limited (Years of production left in the ground with the current proved reserves and flows: Coal: 148 years, Oil: 43 years, Natural gas: 61 years[5]), the energy structure requires adjustment.

Renewable energies, including wind power, solar power, biomass, geothermal power, tidal and wave power, and nuclear power have been developed and utilized to adjust the energy structure.

Nuclear energy is suitable for large scale application nowadays[6]. However, the well-known tragic consequences to the Fukushima nuclear plant from the earthquake and tsunami in Japan on 11 March 2011, has led to a much stronger political focus on renewable energy as the solution to the energy problems. Both Japan and Germany have recently announced the abandonment of expanding nuclear power usage.[7]

The PV power generation could be implemented for large scale with significant advantages [8] below has developed quickly in recent decades.:

- no water needs;
- no moving parts that allows cheaper maintenance;
- effective use of both direct and scattered (diffuse)radiation;
- no need in high qualified personnel;
- noiseless performance;
- no hazardous substance emissions, made of green materials
- can be used for systems of any capacity;
- flat construction allows to integrate the systems in both new and existent buildings;
- can be used as building materials, no additional buildings and infrastructure are necessary;
- It is possible to create a distributed system;

Since the first Photovoltaic cell was made in 1954, in Bell Laboratories [9] by Daryl Chapin, Calvin Souther Fuller and Gerald Pearson, PV power generation has been proposed and studied. The first profitable market of PV power generation is the aerospace application. In the recent decades, significant efforts on new materials, device concepts and processes, and manufacturing technologies have been made to bring down the cost and expand the PV power applications.

To support the development of the PV power, many countries have policies (eg: feed-in tariffs and tax breaks), plans and targets to stimulate the PV growth [10-13].

Driven by these incentives, the cost of typical solar PV modules has fallen from nearly US\$19 per Wp(watts at peak output) in 1982 to around US\$1.59 per Wp today[14]. The global PV module price curves for different PV materials are illustrated as Figure 1.1.

The global installed PV capacity has multiplied by a factor of 37 in ten years from 1.8GW in 2000 to 67.4GW at the end of 2011, a growth rate of 44% per year[14]. Figure 1.2 illustrates the global solar PV capacity bars based on different local regions.

The future developments of PV generation mainly rely on the technical and strategic developments to decrease the cost and increase the reliability in advance.



Figure 1. 1PV module price experience [14]



Figure 1. 2 Global solar PV capacity [14]

APEC refers to Asia-Pacific Economic Cooperation in Figure. 1.2.

1.2 Solar Power System

Solar power systems can be divided into two parts: PV cells which are grouped together to form a PV panel to convert solar power into voltage variance DC electrical power; and power components system (which is generally referred to as power generation system), including DC/DC converters, DC/AC inverters, controllers, etc., which convert the voltage variance DC power into DC or AC power differed by load requirements. The developments of PV power system mainly rely on the technical developments on the two parts individually.

1.2.1 PV Cell Technology

There are a wide range of PV cell technologies on the market today, using different types of materials. Much research has been focused on PV cells and materials as they constitute almost 50% of the system cost. Based on the differences of manufacturing process and commercial maturity, PV cell production technologies can be classified into three generations:

1.2.1.1 First Generation

The first generation uses wafer-based crystalline silicon (c-Si) technology, either single crystalline (sc-Si) or multi-crystalline (mc-Si). Single-crystalline cells are more efficient than multi-crystalline cells but are more expensive to manufacture. This generation is dominated by Silicon (Si) and some extent Gallium-Arsenide (GaAs) and is one of the mainstream PV technologies used today.

1.2.1.2 Second Generation

The second generation are based on thin-film PV technologies and can be classified into three types: 1) amorphous (a-Si) and micromorph silicon (a-Si/uc-Si); 2) Cadmium-Telluride (CdTe); and 3) Copper-Indium-Selenide (CIS) and Copper-Indium- Gallium-Diselenide (CIGS). Other PV cell technologies include the multi-junction PV cells which absorb and convert more solar spectrum into electricity compared with single-junction cells. The thin-film PV cells are also widely used in today's market.

1.2.1.3 Third Generation

The Third generation PV cells include technologies, such as concentrating PV (CPV), dye-sensitized, organic PV cells and quantum dots, which are still under development and could become viable commercial options in the future to reduce the cost.



Figure 1. 3 Three generations of PV cells [15, 16]

Figure.1.3 illustrates the comparison of these three PV cell generations in efficiency and cost.

1.2.2 PV Power Generation System

The PV generation can be generally divided into two types: off-grid systems and grid-connected systems. The off-grid systems produce power independently of the utility grid. Examples are telecommunications units, remote stations, rural electricity supply, and auxiliary power units for emergency services or military applications. Up until the mid-1990s, most PV systems were standalone off-grid applications. The grid-connected systems are connected with the utility grid. Some of these systems feed the local load requirement first and provide surplus power into grid, while others feed all the power into the grid without considering local load. Because the utility grid provides unlimited storage power, the system could take care of large load variations.

Since 2005, the grid connected systems have steadily gained market because of the governments' promotions. Today they represents about 75% of the global PV market today.[1, 2]

Figure 1.4 illustrates the disparity in different countries' market distribution between grid-connected and off-grid installations.



Figure 1. 4 Market share of cumulative installed PV capacity, by application (IEA 2011)

1.2.2.1Conventional Grid-Connected PV Power System

In the grid-connected PV systems, DC/AC inverters are the essential part to invert dc power out of PV cell to grid-compatible ac power. The current injected to the grid should be high quality sinusoidal waveforms synchronized with the utility grid voltage. Besides, the power injected into the grid is dependent upon the maximum power available from the PV panel side which varies with temperature and irradiance.

Thus based on the inverter configuration differences, the grid-connected PV system can be classified into four groups: centralized type[4], string type[17], multi-string type[18, 19], and module integrated type[20-23].

A. Centralized type

The centralized inverters, as illustrated in Figure 1.5 (a), are usually implemented in large scale PV farrms and connect to interface a large number of PV panels to the grid. The PV panels

are connected in series firstly (or called strings) to generate a sufficiently high voltage and avoid further amplification, and then these series are connected in parallel through string diodes to obtain the desired high power level. This arrangement is the earliest configuration type as it offers economies of scale. Later on because of severe disadvantages, the usage of the centralized inverters decreases.[18, 24, 25]

• Disadvantages in power losses:

As illustrated in Figure 1.5 (a), series diodes are required for every parallel branch to ensure the power flow directions. However, these diodes increase the power losses and decrease the system efficiency. Moreover, the unequal power distribution and mismatching of maximum power points for PV panels increase power losses further. Because it is a centralized control, when it fails, all power from the solar installation is lost.

• Disadvantages in cost:

Due to the high DC voltage and high power, the installation and maintenance of the centralized type inverters is complex and expensive, requiring specialist skill and safety procedures. The high voltage DC cables between PV modules and the inverter also increases the cost. Moreover, the inflexible design of centralized inverter eliminates the possibility of mass production benefit in cost. The inverter is required to be located in a protected environment indoors because of the large power, which increases cost in initial system construction.

• Disadvantages in other aspects:

There are other disadvantages such as the inflexible design(which does not permit power level expandability); short life time (most manufacturers of these type inverters only warrant their products for 5 or 10 years); poor power quality (The grid-connected stage was usually line commutated by means of thyristors, involving many current harmonics) and so on.

7



Figure 1. 5 PV inverter structures: (a) central type, (b) string type, (c) multi-string type, (d) module integrated type

To avoid the problems caused by centralized type inverters, string and multi-string inverters are proposed. Compared with centralized inverters, the string and multi-string type inverters do not require series diodes, which would save power losses. Moreover, the possibility of mass production of inverters enables a cost reduction. In string or multi-string inverters, since each string operates independently of each other, if one string fails, all power from the other strings can still feed into the grid.

B. String type

The string type as illustrated in Figure 1.5 (b), has several PV panels which are connected in series as a string. Each string is connected with a DC/AC converter, which allows the MPP of each PV string to be optimized, and the expanding of a PV system could be simply realized by inserting additional strings and inverters to the existing platform [18, 24, 25]. This type of inverter can be considered a reduced version of the centralized inverter. The voltage level can be high to avoid voltage amplification, or the voltage level can be low by involving a transformer or DC/DC converter to the inverters. Therefore the number of PV panels is more flexible to construct each string.

C. Multi-string type

For multi-string type as illustrated in Figure 1.5 (c), several PV panels are connected in series and then connected with a low power DC/DC converter as a string, while several DC/DC converters as multiple strings are connected together with one DC/AC converter.

The multi-string type can be referred to as a variation of two-stage inverter string type, which can also realize optimal MPP of each string and flexibility with string design. The multi-string inverter combines the advantages of string inverter with the lower costs of centralized inverter. Although string type and multi-string type offer an improvement compared with centralized type, they still suffer from some disadvantages as high initial cost associated with acquisition and installation.

D. Module-integrated type

The module integrated type inverters illustrated as in Figure 1.5 (d) are also referred to as micro-inverters, and the power range is commonly between 150W and 300W. Each PV panel has a single inverter attached at the back. The output of micro-inverters are connected together to convert raw DC power from PV panel to AC power and provide power into the grid, thus no high voltage DC cable is required as centralized type inverters.

Since micro-inverters can perform a dedicate PV power harvest for every single PV panel, the misleading problems caused by shading, dust, dirt, or other possible non-uniform changes in temperatures and irradiations are minimized compared with other types inverters. Moreover, micro-inverters have low voltage DC link, thus when failure cases take place, it is easy to replace or repair the broken part, and during this process, little affection will happen on the whole power generation system. These plug-N-play inverters are easily installed, simple in maintenance, and possible in mass production. [18, 24-26] Whereas they allow greater flexibility by allowing the use of panels with different specifications, different ratings, or produced by different manufacturer. This type of inverters would be the development trend of PV system design.

1.2.2.2 Micro-Inverters

For the micro-inverter applications, the inverter is put behind the PV panel with connection at the input side, and the output side is connected with the grid. Thus three functions should be realized simultaneously by the micro-inverter:

- High gain voltage rising
- DC/AC voltage inverting
- MPPT

There are various inverter topologies suitable for micro-inverter applications. Based on different consideration reference, the inverter topologies could be classified into different groups. For electrical ground consideration, the micro-inverter could be classified into galvanic isolation

and non-galvanic isolation. [27] Whereas based on the number of power processing stages, the micro-inverter could be classified into single-stage inverter, double-stage inverter, and three-stage inverter.

A. Micro-inverters classified with isolation

The galvanic isolation inverters implements transformer to achieve high voltage gain and provides doubly grounded for the source and the grid. Normally, low voltage rated switches are allowed for usage in the primary side. Several countries including U.S. have compulsory requirement of galvanic isolation. Due to the location of the transformers, the galvanic isolation inverters can be classified as grid line connection, transformer in DC/DC stage, and transformer in DC/AC stage. Due to the operation frequency, the galvanic isolation inverters can be classified as high frequency (HF) transformer inverters and low frequency (LF) transformer inverters. The individual types are illustrated in Figure 1.6.



Figure 1. 6 Different isolation micro inverter structures (a) grid line connection (b) transformer in DC/DC stage (c) transformer in DC/AC inverter for single stage micro inverter (d) transformer in DC/AC stage for double stage micro inverter

The grid line connection type as illustrated as Figure 1.6 (a) has a transformer operating at line frequency, which is regarded as a poor component due to large size, weight and price. The conventional types under implementation are high frequency transformers as illustrated in Fig.

1.6 (b)(c)(d). Various topologies with high frequency transformers have been proposed in the recent decades. With active semiconductors, high frequency voltage waveforms are generated at the input side of the transformer, and Rectifier Bridge is connected with the output side of the transformer to convert the high frequency waveforms into the DC waveform or line frequency waveform. Thus switching losses for the switches in the primary side and conduction losses in the secondary side are the main concern in the efficiency improvement consideration.

As classical boost topology cannot provide high voltage gain considering the low efficiency, the non-galvanic isolation inverters implement magnetic methods or capacitive methods to increase voltage gain. In magnetic methods, coupled inductors are involved into the inverter topologies [23, 28]. As isolated inverters, the magnetic methods rely on turns ratio to raise voltage. Although they may achieve better efficiency due to single stage topologies, they use transformers but do not provide ground isolation. The capacitive methods can be realized by voltage multiplier stages [22, 28], or rely on a group of capacitors which could be charged as parallel connection with the source, and discharged as series connection with the load [28-30]. This kind of topologies do not require a transformer, thus less cost, and smaller size and weight could be achieved [22, 23, 28, 30]. However transient high charging or discharging current restrict the usage for safety consideration.

B. Micro-inverter classified with power processing stages

Based on the power conversion stages, the grid connected PV inverters can be classified into three groups: single-stage inverter, double-stage inverter, and three-stage inverter.

For the single-stage inverters, MPPT, DC/AC power conversion, and voltage amplification should be realized in one power conversion stage, thus overall efficiency might be improved, especially when solar insolation is low. Moreover, size and components would be saved. The structure of single stage inverters is illustrated in Figure 1.7 (a). As three functions have to be realized on a single stage, the controller should be much more complicated [31, 32]. Several

single stage inverter topologies with suitable control schemes have been proposed in literatures [33]. Their applications as micro-inverters are still very limited, especially in the three-phase area.



Figure 1. 7 Different power stage micro inverter structures: (a) single-stage (b) double-stage (c) three-stage

For the double-stage inverters illustrated in Figure 1.7 (b), the first stage is a DC/DC converter, and the second stage is a DC/AC inverter. There are multiple functions to be realized by micro-inverters. Benefit from the two stages, based on the voltage conversion classification, is that the DC voltage rising function and DC/AC voltage inverting function could be decoupled. Whereas based on the power-transfer consideration, the MPPT function and bus voltage balance function would be separated so that the circuit design and controller design would be much simpler. The double-stage inverters are the main stream of the PV micro-inverters nowadays. Considering the isolation mandatory, commonly the isolation transformer is placed at the DC/DC stage. [34-36]

The three-stage inverters are illustrated as in Figure 1.7(c), with the two DC/DC converters, and a DC/AC inverter. As illustrated in [18, 37], the first DC/DC converter stage is used to generate a constant low DC voltage; the second DC/DC converter stage is used to provide the isolation and high voltage gain with a transformer, while the third DC/AC inverter stage converts the DC power into AC power and feeds it into the grid. The three-stage inverter has the best

reliability compared with single-stage and double-stage inverters. However, it also has the worst efficiency because of these energy processing stages.

1.2.2.3 The AC PV Module

AC PV module refers to a PV panel integrated with a micro-inverter as illustrated in Figure 1.8. The output of an AC PV module is AC power which could be directly connected with a utility grid. The concept was first proposed by Caltech's Jet Propulsion Laboratory [20, 21] in the1970s. From the 1990s with support from government, the technologies of AC module developed rapidly. With many advantages over central inverter systems and string inverter systems, the AC PV module is believed to be the future development trend of PV solar power systems.

The advantages of AC PV modules are:

• Low minimum system size to unlimited maximum system size

The rated AC PV module could be as small as 100W or even less. Thus the minimum system could be as small as 100W or even less. With required power size increasing, more and more AC modules could be added into the existing system. As illustrated in Figure 1.9, the system size could be extended to any desired power range. So the AC PV module is suitable for both residential PV system and PV farm system. With the flexible system size, the AC PV module has great market potential.

• Simple and flexible installation options

Since the output of the AC module is AC power and no DC cable is accessible to users, the installation could be greatly simplified and easily performed by electricians. Moreover, the various parts of the PV panel do not need to match exactly with each other, so various manufacturers' products could be selected. These characteristics could decrease installation cost greatly.

• Enhanced safety

Without high DC voltage accessible to the users, the AC modules are inherently safer than conventional centralized or string type PV systems. AC module wiring can be done with zero voltage on all wires, terminals and switches until a connection is made to a circuit breaker in the service panel.



Figure 1. 8 The AC PV module[38]



Figure 1. 9 Grid-tie PV AC modules[38]

1.2.2.4 AC Module Inverter Design Consideration

Based on the previous analysis and discussion of the PV power generation systems, the AC module inverters with obvious advantages are selected to construct the PV system in this thesis. Since the performance of an AC module inverter is determined by factors including efficiency, reliability, isolation, and power density, these factors should be employed to direct the detail design of an AC module inverter.

A. Isolation

In the United States the grounding of the PV source is required in PV installation, which is equivalent to the galvanic isolation requirement. As illustrated in Figure 1.6, the galvanic isolation is realized through a transformer.

B. Efficiency

The AC module efficiency is constructed by PV panel efficiency, MPPT efficiency and inverter conversion efficiency. The PV panel efficiency is determined by PV cell technology as discussed in section 1.2.1., where MPPT is the fundamental component for tracking the maximum power of PV panel continuously under changing environment (i.e. solar irradiance and temperature). The MPPT efficiency is evaluated with static and dynamic efficiency. The commercial inverter MPPT efficiency is larger than 98%. The inverter conversion efficiency is a weighed conversion efficiency that considers several operating conditions. [39, 40] The inverter conversion efficiency is the decisive factor from the investor point of view.

C. Power density

The power density is an important factor to decrease the inverter volume and cost. Since the AC module inverter is attached behind the PV panel as illustrated in Figure 1.8, the inverter volume is preferred to be small.

D. Reliability

Most commercial PV modules are guaranteed to perform at specified levels of output for 20 to 25 years.[41] Integrating the inverter to the PV module necessitates that they both must have matched expected lifetimes so that the inverter should also have a lifetime for 20 to 25 years.

Based on these above factors, a few restrictions could be given on the design of AC module inverters:

• Compared with single-stage and three-stage inverters, the double-stage inverter structure should be selected because of better efficiency with high quality AC output.

- Soft switching is a technical method to improve the inverter conversion efficiency. The realization of soft switching is preferred not only because of efficiency improvement, but also because the possibility of improving switching frequency and power density.
- Considering isolation requirement, as low frequency transformer is not only large but also power consuming, the high frequency transformer should be selected in the inverter design.
- To improve the reliability, the capacitance of system is preferred to be the smaller, the better.

1.3 Objectives and Outlines

The main objectives of this thesis are to provide a specific analysis about a high efficiency module solar system architecture.

The dissertation is divided into five chapters, which are organized as follows:

Chapter one provides a background introduction of the PV system. The worldwide energy shortage status makes renewable energy applications extremely attractive. Among various renewable energy types, solar energy with the advantages of clean, inexhaustible, safe, and globally applicable is extremely suitable for large scale application. The PV system as the major implementation of solar energy can be divided into two parts: PV cells and power components. Both of them have been analyzed carefully, especially the power components part, which is the objective of this thesis. Based on the considerations from efficiency, power density, galvanic isolation and reliability, several restrictions are generated to guide the specific design of the AC module inverter.

Chapter two provides the study of DC/DC stage. DC/DC stage performs an important role in converting DC power from PV panel side voltage to DC bus voltage required in the micro-inverter. Various topologies of DC/DC converter have been reviewed. Resonant topologies with soft switching are studied in detail when operating as DC/DC stage. LLC converter with advantages over other resonant converters is selected as DC/DC stage eventually.

A novel MPPT with fast tracking speed and little oscillation power loss is proposed to track the maximum power on LLC converter with frequency modulation. The feasibility of the proposed MPPT method is proved mathematically. Simulation and experiment results verify the theory analysis.

Chapter three provides the study of DC/AC stage. A brief introduction is given on DC/AC inverter topologies. To improve the inverter efficiency, based on chapter one, the soft switching technique should be employed. Thus a review of the soft switching technologies on inverters is given. A proposed BCM inverter technique is analyzed in detail. A 150W inverter prototype was built and experiments were carried out on both full-bridge and half-bridge inverter topologies. Experimental waveforms verify the operation principle.

To give a comparison with the proposed soft switching, ARCP on the same prototype as existing soft switching technique is performed. Experiment results demonstrate that the proposed control-realized soft switching has better efficiency with fewer components.

Chapter four provides the complementary part of the module solar system architecture---the energy storage integrated with the micro-inverter/Utility interactive systems. To balance the intermittent and unpredictable nature of PV energy with fluctuating load, energy storage is required to be integrated with the existed PV system. The grid connection type energy storage, which requires least energy storage capacity, is preferred. The PFC converter is an important component to realize it. A biflyback PFC topology is studies in this chapter with a DSP controller. A new snubber cell is proposed to restrict the voltage stress and realize the soft switching. Simulation and experiment verify the analysis.

Chapter five summarizes the whole thesis and describes the future work based on the existed experiments and analysis.

CHAPTER TWO: DC/DC CONVERTER STAGE

In the double stage micro-inverter PV systems, the DC/DC converter performs an important role in converting DC power from PV panel side voltage to required DC bus voltage. There are several technical challenges that exist for the DC/DC converter:

- PV panel is connected as the input source of the DC/DC converter, which has a wide input voltage range depending on the operating conditions of PV cell. Also the converter is required to regulate the constant output voltage. Generally the PV panel voltage is about 20~50V, while the DC bus voltage is around 400V. Thus a large voltage rising function is required.
- As a renewable energy, the PV source is continually affected by environmental factors such as irradiance and temperature. Thus the output power of the PV panel can vary significantly in a day, which requires the DC/DC converter to operate in a large power range.
- Increasing power density is another requirement for the DC/DC converter, which would decrease the micro-inverter volume and be convenient for the module-integrated structure design. Thus cost of installation and transportation would be reduced.
- In addition, a high efficiency is required to increase the micro-inverter efficiency under operational conditions.

To deal with all these technical requirements, much literature focusing on DC/DC converters has been published.[42-45]

2.1 Analysis to Resonant Topologies

Classified by the operation differences, the DC/DC converter can be divided into two parts: pulse width modulation (PWM) converters and resonant converters. PWM DC/DC converters refer to conventional converters with pulse width modulation regulating current or voltage, whereas resonant DC/DC converters refer to the converters with controlling energy cycling in L-C resonant tanks to process the power conversion. Considering the galvanic isolation, a transformer is usually adopted in the DC/DC converters. Both pulse width modulation (PWM) converters and resonant converters are practicable to adopt the isolation transformer.

For the PWM converters, the leakage inductance of the transformer would add voltage stress and increase switching power losses to the main switches. Moreover, the hard switching increases electromagnetic interference (EMI) and restriction on high switching frequency. However, the resonant converters, with the advantages below are suitable for the application as the intermediate stage between the PV generator and the inverter in PV systems.

- Reduced switching losses due to soft-switching operation in all the switches.
- Reduced size due to high switching frequency capability of the resonant nature of the circuit.
- No adverse effect of voltage stresses on devices due to leakage inductance since it forms part of resonant circuit.

However the performance of resonant converter depends upon not only circuit parameters, but also control techniques, which is difficult to determine with output power and input voltage variance. That is one of the reasons why PWM converters are broadly utilized with duty cycle control in the realization of PV micro-inverters.

There are various control methods for the resonant converters. For example, frequency modulation, phase shift modulation, skipping pulses modulation, hybrid bridge control, etc. Among all these control methods, the variable frequency control is the most conventional for application.[46-49]

In the variable frequency control, the duty cycle is usually maintained at 50%. With frequency modulation, circulating energy in the LC tank is manageable; therefore output power is controllable with the desired output voltage.

2.1.1 Introduction of Resonant Topologies



Figure 2. 1 General scheme of a resonant converter

There are various resonant converters whose topologies can generally be illustrated in Figure 2.1, where a half or full bridge is connected with DC source to generate a square voltage excitation to the resonant network. Then a resonant network is provided for circulation and delivery of power, where a transformer is provided for galvanic isolation. Sometimes the primary inductor of the transformer operates as part of the resonant tank. At the other end, a rectifier constructed with diodes is cascaded to convert the squire voltage into DC output voltage.

Based on the resonant network complexity, the most commonly known resonant converter topologies could be classified into three groups:

• Second order resonant converter

For example: Series resonant converter (SRC) and parallel resonant converter (PRC)

• Third order resonant converter

For example: series-parallel resonant converter LCC (or SPRC), LLC resonant converter

• Fourth order resonant converter

For example: LCLC resonant converter

All of the topologies are analyzed individually as follows with frequency as the control parameter.

2.1.2 Frequency Modulation of Resonant Topologies

2.1.2.1 Second Order Resonant Converter

A. SRC

The topology of a series resonant converter (SRC) is illustrated as in Figure 2.2 (a). The resonant tank is constructed with a capacitor C_s and an inductor L_s connected in series as illustrated in Figure 2.2 (b), where the R_{eq} refers to the equivalent impedance of the output load resistance observing from the primary side of the transformer.



(a)

(b)

Figure 2. 2 SRC topology: (a) input full bridge output half bridge circuit (b) resonant tank

For the resonant tank, resonant radiance frequency and resonant impedance are

$$\omega_{\rm os} = \frac{1}{\sqrt{L_{\rm s}C_{\rm s}}},$$

 $Z_{cs} = \sqrt{\frac{L_s}{C_s}}$ respectively. To simplify the analysis, the switching frequency could be normalized as: $f_n = \omega_n = \frac{\omega}{\omega_{os}}.$

Because of the 0.5 constant duty cycle, the input of a resonant tank is a square-wave voltage generated by the full bridge:

$$E = \begin{cases} V_{in} & S_{2,4} \text{ on, } S_{1,3} \text{ off} \\ -V_{in} & S_{1,3} \text{ on, } S_{2,4} \text{ off} \end{cases}$$
(2.2)

The input impedance at the resonant input side:

$$Z_{in} = jZ_{cs}(f_n - \frac{1}{f_n}) + R_{eq}$$
 (2.3)

To make sure that the resonant link does not enter the capacitive zone, $f_n>1$ should be satisfied.

Although state functions can be provided to solve the accurate voltage gain of $\frac{V_o}{V_{in}}$, it is usually cumbersome due to the complex interaction between the resonant components. Thus Fourier transform is applied here to transfer the square-wave signal into a combination of odd harmonic components, the expression is as follow

$$E = V_{in} \frac{4}{\pi} \sum_{k=1,3...}^{\infty} [\sin(k\omega_s t)/k]$$
(2.4)

Thus classical ac-circuit analysis can be applied for each harmonic component.

$$\left|\frac{R_{eq}}{Z_{in}}\right| = \frac{R_{eq}}{\sqrt{Z_{cs}^{2}(f_{n}-1/f_{n})^{2}+R_{eq}^{2}}}$$
(2.5)

$$M_{k} = \frac{V_{o}(k)}{V_{in}} = \frac{2n}{k} \left| \frac{R_{eq}}{\sqrt{Z_{cs}^{2} (kf_{n} - 1/(kf_{n}))^{2} + R_{eq}^{2}}} \right|$$
(2.6)

And the voltage gain M can be met with equation (2.7).
$$M = \frac{V_{o}}{V_{in}} = \sqrt{\sum_{k=1,3...}^{\infty} M_{k}^{2}}$$
(2.7)

Based on expression (2.5), the frequency-gain curves for different load could be drawn as in Figure 2.3, where P_n refers to rated power for the SRC converter.



Figure 2. 3 normalized Gain vs frequency waveforms under various loads for SRC

It is obvious to observe from Figure 2.3 that when switching frequency is moving away from the resonant frequency in the inductive zone, the normalized voltage gain ($M_n=M/2n$) drops quickly, especially when load increases. For example, for the full load curve illustrated in Figure 2.3, the gain drops five times (from 1 to 0.2) when switching frequency drops only 15% (from 1 to 1.15). Thus the frequency modulation for this frequency section is much more sensitive than for the other sections.

B. PRC

The topology of parallel resonant converter (PRC) is illustrated as in Figure 2.4 (a). The

resonant tank is constructed with a capacitor C_s and an inductor L_s connected in parallel as illustrated in Figure 2.4 (b), where the R_{eq} refers to the equivalent impedance of the output load resistance observing from the primary side of the transformer. And the expression for R_{eq} is the same as (2.1).



(b)

Figure 2. 4 PRC topology: (a) input full bridge output half bridge circuit (b) resonant tank

For the resonant tank, resonant radiance frequency and resonant impedance are $\omega_{os} = \frac{1}{\sqrt{L_s C_p}}$

$$Z_{cs} = \sqrt{\frac{L_s}{C_p}}$$
 respectively. To simplify the analysis, the switching frequency could be normalized as:

$$f_n = \omega_n = \frac{\omega}{\omega_{os}}$$

The parallel impedance observed from the primary transformer side is:

$$Z_{\rm P} = \frac{R_{\rm eq}}{1 + j\,\omega C_{\rm P} R_{\rm eq}} \tag{2.8}$$

The input impedance observed from the full bridge side is:

$$Z_{in} = \frac{R_{eq} + j \frac{f_n}{Z_{cs}} [Z_{cs}^2 - R_{eq}^2 (1 - f_n^2)]}{1 + \frac{f_n^2 R_{eq}}{L_s}}$$
(2.9)

To make sure that the resonant link is not capacitive, the imaginary part of (2.9) should be positive. Thus (2.10) could be solved as requirement for inductive load.

$$f_n > \sqrt{1 - \frac{Z_{cs}^2}{R_{eq}^2}}$$
 (2.10)



Figure 2. 5 Normalized Gain vs frequency waveforms under various loads for PRC

To implement the frequency analysis as in SRC part, the voltage gain for each harmonic sinusoid voltage can be calculated by (2.11), while the overall voltage gain could be calculated by (2.2).

$$M_{k} = \frac{2n}{k} \cdot \frac{R_{eq}}{\sqrt{Z_{cs}^{2} (kf_{n})^{2} + [R_{eq}(1 - k^{2}f_{n}^{2})]^{2}}}$$
(2.11)

The frequency-gain waveforms under various load conditions are drawn out as in Figure 2.5 with boundary line provided to separate inductive zone with capacitive.

Observing from Figure 2.5, the normalized gain value in inductive zone can be larger or smaller than 1, which allows the converter to operate in a wider gain range compared with SRC converter. For lighter load conditions, the slope is much steeper than the heavier load condition when normalized switching frequency is in range [1, 1.25], which is also the range for $M_n>1$.

2.1.2.2 Third Order Resonant Converter

A. LCC

The topology of LCC resonant converter is illustrated as in Figure 2.6 (a). The resonant tank is illustrated in Figure 2.6(b), a capacitor is connected with an inductor and another capacitor is in series. The R_{eq} refers to the equivalent impedance of the output load.



(b)

Figure 2. 6 LCC topology: (a) input full bridge output half bridge circuit (b) resonant tank

The resonant tank is constructed by a series load (Z_s) and a parallel load (Z_p) . They can be expressed individually as follows:

$$Z_{s} = j(\omega L_{s} - \frac{1}{\omega C_{s}})$$
(2.12)

$$Z_{\rm P} = \frac{R_{\rm eq}}{1 + j\omega C_{\rm P} R_{\rm eq}} \tag{2.13}$$

The resonant frequency of the LCC converter is $\omega_{os} = \sqrt{\frac{C_s + C_p}{L_s C_s C_p}}$, which is also the open

circuit resonant frequency. The switching frequency can be normalized as $f_n = \omega_n = \frac{\omega}{\omega_{or}}$, and

 $F_n = f_n \sqrt{1 + 1/k_C}$ is the short circuit resonant frequency, where $k_C = \frac{C_p}{C_s}$.

The voltage gain for kth order harmonic component of the LCC converter is

$$M_{k} = \frac{2n}{k} \cdot \frac{R_{eq}}{\sqrt{\frac{L_{s}}{C_{s}}(kF_{n} - 1/(kF_{n}))^{2} + R_{eq}^{2}(kc+1)^{2}(1 - k^{2}f_{n}^{2})^{2}}}$$
(2.14)

The input impedance observed from the full bridge side is:

$$Z_{in} = \frac{R_{eq} + j[L_s - \frac{L_s C_p}{f_n^2 (C_s + C_p)} + C_p R_{eq}^2 (k_c + 1)(f_n^2 - 1)]}{a}$$
(2.15)

Where $a = 1 + \frac{f_n^2 (C_s + C_p) C_p R_{eq}^2}{L_s C_s}$, and (2.16) is a sufficient condition to make sure that Z_{in} is

inductive.

$$f_n \in (\sqrt{\frac{c - a + \sqrt{(a - c)^2 - 4bc}}{2c}}, \infty)$$
 (2.16)

Where $a = L_s(C_s + C_p)$, $b = L_sC_p$, $c = C_p(C_s + C_p)(k_c + 1)R_{eq}^2$

The solution (2.16) is varied with the output load. Figure 2.7 illustrates the frequency-gain

waveforms under various load conditions. The green section in Figure 2.7 is the inductive zone while the red region is the capacitive zone calculated from (2.16).



Figure 2. 7 Normalized Gain vs frequency waveforms under various loads for LCC

Observing from Figure 2.7, inside the inductive zone, the smaller the frequency, the larger the normalized gainis. For a lighter load condition, the voltage gain VS frequency slope is much steeper than the heavier load condition when the normalized switching frequency is less than 1.25. When the normalized switching frequency is larger than 1.25, with frequency increasing, the voltage gain decreases slowly and approach together under various load.

B.LLC

The topology of LLC resonant converter is illustrated as in Figure 2.8 (a). The resonant tank is constructed with a capacitor C_s , an inductor L_s and a transformer with primary inductor L_p connected in series as illustrated in Figure 2.8 (b), where the R_{eq} refers to the equivalent impedance of the output load.





The resonant tank is constructed by a series load (Z_s) and a parallel load (Z_p) , and they can be expressed individually as follows:

$$Z_{s} = j(\omega L_{s} - \frac{1}{\omega C_{s}})$$
(2.17)

$$Z_{p} = \frac{j\omega L_{p}R_{eq}}{R_{eq} + j\omega L_{p}}$$
(2.18)

The voltage gain for every harmonic component of the LLC converter can be calculated with equation (2.19)

$$M_{k} = \frac{V_{o}(k)}{V_{in}} = \frac{2n}{k} \left| \frac{(kf_{n})^{2}(m-1)}{(m(kf_{n})^{2}-1) + jQ(m-1)((kf_{n})^{2}-1)kf_{n}} \right|$$
(2.19)

Where
$$m = \frac{L_s + L_p}{L_s}$$
, $f_r = \frac{1}{2\pi\sqrt{L_sC_s}}$, $f_n = \frac{f_s}{f_r}$, $Q = \frac{\sqrt{L_s/C_s}}{R_{eq}}$, $R_{eq} = \frac{2V_o}{n^2\pi^2 I_o}$, and $V_o(k)$ refers to

the kth order harmonic of the output voltage. fs refers to switching frequency of the full bridge; R_{eq}

refers to the equivalent load resistance at the primary side of the transformer, and n refers to the turns ratio of the transformer.

The input impedance observed from the full bridge side is:

$$Z_{in} = \frac{\frac{L_p^2}{L_s C_s} f_n^2 R_{eq}}{R_{eq}^2 + \frac{L_p^2}{L_s C_s} f_n^2} + j(L_s + \frac{R_{eq}^2 L_p}{R_{eq}^2 + \frac{L_p^2}{L_s C_s} f_n^2} - \frac{L_s}{f_n^2})$$
(2.20)

To make sure that the resonant link is inductive, the imaginary part of (2.20) should be positive. Thus the frequency requirement of soft switching could be calculated as (2.21).

$$f_n \in (\sqrt{\frac{a-b+\sqrt{(a-b)^2+4a}}{2a}},\infty)$$
 (2.21)

Where $a = \frac{L_p^2}{R_{eq}^2 L_s C_s}$, $b = \frac{L_p + L_s}{L_s}$.

The boundary line of inductive and conductive zones is illustrated as in Figure 2.9, where normalized gain vs frequency waveforms under various loads for LLC converter are drawn out.

Observing from Figure 2.9, inside the inductive zone, when the normalized switching frequency is lower than 1, the smaller the frequency, the larger the normalized gainis. When the normalized switching frequency is larger than 1, with frequency increasing, the voltage gain decreases very slowly. For lighter load conditions, the voltage gain VS frequency slope is much steeper than the heavier load condition.



Figure 2. 9 Normalized Gain vs frequency waveforms under various load for LLC converter

2.1.2.3 Fourth Order Resonant Converter

A. SPRC (LCLC)

The SPRC, also known as the LCLC resonant converter, is a combination of SRC and PRC. The topology of the LCLC converter is illustrated in Figure 2.10 (a). The Figure 2.10 (b) shows the simplified resonant tank of the LCLC converter, where the R_{eq} refers to the equivalent impedance of the output load.

The resonant tank is constructed by a series load (Z_s) and a parallel load (Z_p), and they can be expressed as follows (2.22) and (2.23)

$$Z_{s} = j(\omega L_{s} - \frac{1}{\omega C_{s}})$$
(2.22)

$$Z_{p} = \frac{j\omega L_{p}R_{eq}}{j\omega L_{p} + R_{eq} - \omega^{2}L_{p}C_{p}R_{eq}}$$
(2.23)



(b)

Figure 2. 10 LCLC topology: (a) full bridge circuit (b) resonant tank

The voltage gain for individual harmonic components could be expressed as

$$M_{k} = \frac{2n}{k} \cdot \frac{b}{\sqrt{(ad+b)^{2} + a^{2}c^{2}}}$$
(2.24)

Where $f_n = \omega_n = \frac{\omega}{\omega_{os}}$, $\omega_{os} = \frac{1}{\sqrt{L_sC_s}}$, $Z_{cs} = \sqrt{\frac{L_s}{C_s}}$, $k_L = \frac{L_p}{L_s}$, $k_C = \frac{C_p}{C_s}$, $k_R = \frac{R_{eq}}{Z_{cs}}$, $a = kf_n - \frac{1}{kf_n}$,

 $b = k_L k f_n \, , \ c = \frac{k_L}{k_R} k f_n \, , \ d = 1 - k_L k_C k^2 {f_n}^2 \, .$

The input impedance observed from the full bridge side is:

$$Z_{in} = Z_{cs}(ja + \frac{jb}{jc+d}) = Z_{cs} \cdot \frac{bc + j[a(c^2 + d^2) + bd]}{d^2 + c^2}$$
(2.25)

To make sure that the resonant link is not capacitive, (2.26) should be satisfied.

$$a(c^2 + d^2) + bd > 0$$
 (2.26)

To simplify the derivation, assume kk = 1, (2.27) could be induced from (2.26)

$$f_n \in (\sqrt{\frac{A - \sqrt{A^2 - 4}}{2}}, 1) \cup (\sqrt{\frac{A + \sqrt{A^2 - 4}}{2}}, \infty)$$
 (2.27)

Where $A = 2 - k \ln(\frac{Z_{cs}^2}{R_{eq}^2} - 1)$.



Figure 2. 11 Normalized Gain vs frequency waveforms under various load for LCLC

The solution (2.27) is varied with the output load. Figure 2.11 illustrates the frequency-gain waveforms under various load conditions. The green sections in Figure 2.11 are the inductive zone while the red regions are the capacitive zone calculated from (2.27).

It is obvious to observe from Figure 2.11 that both the upper and lower resonant frequencies are changing with load. Fortunately they do not change as much as LLC. Based on Figure 2.11, an appropriate operation frequency range is selected as [2, 2.5], which is inductive zone.

2.1.3 Operation of Resonant Topologies Connected with PV Panel

In the two-stage micro-inverter, the output of DC/DC stage is connected as the input of DC/AC stage. Conventionally, to promise the stable operation of the DC/AC inverter, the bus voltage is required to be a constant value V_{ref} , which is expressed as

$$V_{o} = V_{ref} \tag{2.28}$$

Considering the power balance,

$$V_{in}I_{in} = V_0I_0 = V_{ref}I_0 \tag{2.29}$$

In the two-stage micro-inverter system, the input side of resonant converter is connected with a PV panel.



Figure 2. 12 Equivalent circuit of a PV panel

The equivalent circuit of a PV panel is illustrated in Figure 2.12, and the input current and input voltage follows the equation (2.24).

$$I_{in} = I_L - I_D[e^{\frac{V_{in} + I_{in}R_s}{a}} - 1] - \frac{V_{in} + I_{in}R_s}{R_{sh}}$$
(2.30)

In (2.30), five parameters I_L , I_D , a, R_s , and R_{sh} could be calculated by the short circuit current I_{sc} , open circuit voltage V_{oc} , MPP current I_{mp} , and MPP voltage V_{mp} . As I_{sc} , V_{oc} , I_{mp} and V_{mp} are various with different irradiances and temperatures, the curves of V_{in} VS I_{in} could be drawn out based on equation (2.30).

Combined equations (2.28), (2.29) with characteristic equations of resonant converters together, input current VS input voltage waveforms could be generated and drawn out individually.

To observe the operation points of PV panel connected resonant converter, characteristic waveforms of PV panel under different irradiances could be drawn out based on equation (2.30). The joint points of these curves with the former relationship curves illustrate the expected operation points of these resonant converters connected with PV panel.

All of the commonly used resonant converter topologies are analyzed individually as PV panel connected DC/DC stage of micro-inverters. Waveforms are drawn and illustrated as follow.

2.1.3.1 Second Order Resonant Converter

A. SRC

Based on equations (2.1), (2.6), (2.7), (2.28), (2.29), 3D relationship of input voltage, input current and normalized switching frequency could be calculated and drawn in Figure 2.13.

The characteristic waveforms of PV panel are drawn with waveforms of SRC as illustrated in Figure 2.14. The operation joint points illustrate the expected operation points of this converter connected with PV panel.

To simulate the operation of SRC converter as the first stage of a micro-inverter, the system parameters are assumed as: V_{ref} =400V, n=25;C_s=1.17uF; L_s=6uH; thus resonant frequency f_o=60.1kHz.

It is obviously to observe from Figure 2.14 that,

- For one V-I curve, one switching frequency relates to only one set of V_{in} and I_{in}. With frequency increasing, V_{in} increases and I_{in} decreases.
- The operation point of PV panel changes much more with frequency in range [1.1 1.2] than in other frequency ranges.
- When the normalized switching frequency is over 1.2, the PV current is approximated fixed with fixed frequency under various irradiances.
- When the normalized switching frequency is less than 1.1, the PV voltage is approximated fixed with fixed frequency under various irradiances.



Figure 2. 13 SRC converter 3D relationship of input voltage, input current and normalized switching frequency based on $V_0=V_{ref}$



Figure 2. 14 V-I curves under various irradiances for SRC converter

Thus if a frequency modulation MPPT is required for the SRC converter here, it requires three different tracking algorithms for three different frequency zones [1, 1.1], [1.1, 1.2] and [1.2, 2] because these three zones illustrate totally different VI characteristics.

Moreover, the required transformer turns ratio is too large: for this case, n=25 (if full bridge is

applied as the output side, n=50) for voltage gain $M = \frac{V_{ref}}{V_{mpp}} < 14$, which would add power losses and transformer volume for the converter. Thus the SRC converter is not suitable to be applied as the DC/DC stage between PV panel and DC/AC stage.

B. PRC

With the same progress, the 3D relationship of input voltage, input current and normalized switching frequency could be calculated and drawn in Figure 2.15.

To illustrate the operation of PRC converter as the first stage of a micro-inverter, the system parameters are assumed as: Vref=400V, n=5.5;Cp=1uF; Ls=5uH; resonant frequency fo=71.2kHz.

In Figure 2.16, the voltage-current curve of PV panel is the same as in SRC analyses. The joint points of PRC curves with the PV curves illustrate the expected operation points of this PRC converter connected with PV panel.



Figure 2. 15 PRC converter 3D relationship of input voltage, input current and normalized switching frequency based on $V_0=V_{ref}$



Figure 2. 16 V-I curves under various irradiances for PRC converter

Based on the observation of Figure 2.16, characteristics can be obtained as follow:

• The appropriate operation frequency range for MPP searching is narrow.

fne(1.1,5

Thus PRC parameters should be carefully designed to determine the frequency searching range.

- For one V-I curve, one switching frequency relates to only one set of V_{in} and I_{in}. With frequency increasing, V_{in} increases and I_{in} decreases.
- With the frequency increasing, the moving speeds on all PV panel's VI curve are approximately stable.
- Because the SRC VI curves bend more with the power increasing, and the voltage of MPPs change little with irradiance variance, the higher irradiance condition has a smaller frequency for MPP.

Due to the complex interaction between the PRC resonant components, the relationship between V_{in} and f_n is nonlinear and non-explicit. Moreover, the nonlinearity in PV module characteristics exacerbates the complexity of power control with the frequency parameter. Thus simulation instead of direct calculation of the PRC micro-inverter was built to demonstrate the

power curves as in Figure 2.17.



Figure 2. 17 Simulation P-F curves of PRC micro-inverter connected with PV panel

The simulation is built with MATLAB simulink. Figure 2.17 shows that with the irradiance decreasing, the switching frequency for MPP is increasing, which is the same as former the analysis with equations' calculation.

2.1.3.2 Third Order Resonant Converter

A. LCC

Based on equations (2.1), (2.14), (2.7), (2.22), (2.23), 3D relationship of input voltage, input current and normalized switching frequency could be calculated and drawn in Figure 2.18.



Figure 2. 18 LCC converter 3D relationship of input voltage, input current and normalized switching frequency based on $V_0=V_{ref}$

Figure 2.18 illustrates the 3D relationship of input voltage and input current under various switching frequency based on the condition required for two stage inverter $V_o=V_{ref}$. It is obvious to observe from Figure 2.18 that with switching frequency increasing, voltage increases while current decreases. And when switching frequency is resonant frequency, the current is almost constant.

Figure 2.19 illustrates the characteristics of PV array and LCC converter, thus the joint points are the operation points of the LCC converter applied as the first stage of the micro-inverter.

Based on the observation of Figure 2.19, LCC characteristics can be obtained as follow:

• The appropriate initial operation frequency range for MPP searching is narrow.

fn∈(11.25

Thus LCC parameters should be carefully designed to determine the frequency searching range.

 For one V-I curve, one switching frequency relates to only one set of V_{in} and I_{in}. With frequency increasing, V_{in} increases and I_{in} decreases.



Figure 2. 19 V-I curves under various irradiances for LCC converter

• For the same switching frequency, with the power increasing, the slope of VI curve is decreasing, which means that with the irradiance changing, the frequency for MPPs changes a lot.

Simulation based on the same set of parameters as previous calculations of the LCC micro-inverter is built with MATLAB simulink. Figure 2.19 shows that with the irradiance decreasing, the switching frequency for MPP is increasing, which is the same as former the analysis with equations' calculation.



Figure 2. 20 Simulation P-F curves of LCC micro-inverter connected with PV panel

B. LLC

Based on power balance and two stage inverter requirement $V_o=V_{ref}$, the relationship of input voltage, input current and normalized switching frequency could be calculated and waveforms could be drawn in Figure 2.21.



Figure 2. 21 LLC converter 3D relationship of input voltage, input current and normalized switching frequency based on $V_o=V_{ref}$



(a)



(c)

Figure 2. 22 V-I curves of a PV panel and LLC converter under various switching frequency: (a) $f_n \in [0.5, 1.9 \text{ (b) } f_n \in [0.5, 3.5 \text{ (c) Inductive zone}$

Figure 2.21 illustrates that when $f_n=1$, V_{in} is kept constant regardless of the input current value, otherwise the slope of VI curve is keep changing.

As illustrated in Figure 2.21, with the load increasing, the boundary frequency for inductive zone increasing and changing range is very large. As the MPPT progress, the load is always changing. To keep the LLC operating under inductive load, there are two ways:

- Use the worst boundary which takes place at full load.
- Calculate the boundaries for various loads and adjust the boundaries simultaneously with load.

To solve the boundary selection problem, VI curves of PV panel and LLC converter are drawn out as in Figure 2.22. To promise the successful MPPT of this micro-inverter, the LLC parameters should be carefully designed to make sure that the joint points of LLC curves and PV curves include the MPPs.

In Figure 2.22 (a), with the f_n increasing, the frequency curves become closer to each other, which means that the higher the frequency, the less difference in power, especially when input current is small (less than 2A). If the worst boundary is applied, the PV panel curve section that could be covered is very narrow, which is not good for MPPT under various condition.



Figure 2. 23P-F curves of LLC micro-inverter connected with PV panel under various irradiances

Figure 2.22 (b) illustrates when frequency is increased much more than resonant frequency, the frequency lines bend and cover more section again. Thus in limited conditions, well designed LLC can also adopt the worst boundary as boundary for the whole MPPT progress.

Figure 2.22 (c), the different loads with their boundary frequencies are provided, thus the inductive zone can be drawn out. It is obvious to observe from Figure 2.22 (c) that with the frequency decreasing less than 1, the VI curves of LLC bend more and more thus it cannot enter larger power section provided by the PV curves. Thus another constant boundary which is much smaller than the worst boundary can be selected here.

Simulation based on the same set of parameters as previous calculations of the LLC micro-inverter is built with MATLAB simulink. And P-F curves of LLC micro-inverter connected with PV panel under various irradiances are illustrated in Figure 2.23.

The initial operation of the LLC micro-inverter begins from the high frequency side for a soft start. If a conventional P&O or INC method is applied here, the MPPT would fail immediately as little power difference observed at 280kHz as illustrated in Figure 2.23.

2.1.3.3 Fourth Order Resonant Converter

A. SPRC (LCLC)

It can be observed from Figure 2.24 that, with the switching frequency increasing, the V_I curves intend to "bend" with increasing power, which means faster increasing in voltage while slower increasing in current.

Figure 2.25 illustrates the characteristics of PV array and LCLC converter, thus the joint points are the operation points of the LCLC converter applied as the first stage of the micro-inverter.

Based on the observation of Figure 2.25, characteristics can be obtained as follow:



Figure 2. 24 LCLC converter 3D relationship of input voltage, input current and normalized switching frequency based on $V_o = V_{ref}$



Figure 2. 25 V-I curves under various irradiances for LCLC converter

- The appropriate initial operation frequency range for MPP searching is narrow. fn ∈(22.35 Thus LCLC parameters should be carefully designed to determine the frequency searching range.
- With the frequency increasing, the moving speed on PV panel's VI curve is approximately stable

• VI curves bend with the power increasing. The curvature of the bend is not as much as illustrated in Figure 2.16. Thus the MPP voltage does not change as much as PRC converter when irradiance changes, which means that the bus capacitor would have a less impulse in voltage when irradiance suddenly changes. Thus LCLC converter is more suitable than PRC converter in frequency modulated MPPT application.



Figure 2. 26 Simulation P-F curves of LCLC micro-inverter connected with PV panel

Due to the complex interaction between the LCLC resonant components, the relationship between V_{in} and f_n is nonlinear and non-explicit. Moreover, the nonlinearity in PV module characteristics exacerbates the complexity of power control with the frequency parameter. Thus simulation instead of direct calculation of the LCLC micro-inverter was built to demonstrate the power curves as in Figure 2.26.

The simulation is built with MATLAB simulink. These power curves satisfy the requirement in section II. Thus the proposed MPPT would be suitable to apply here.

2.1.4 The Reason for Selecting LLC as DC/DC Converter Stage

Among all the commonly known resonant converters with advantages in high efficiency and low noise, they have some disadvantages compared with LLC converters which limit their applications.

For the second order resonant converters as SRC and PRC, although they have the simplest resonant converters with minimum components, the SRC converter cannot regulate output voltage under unloaded condition. Moreover, ZVS would be lost under a light load condition, whereas the PRC converter has an efficiency changing obviously with load. LCC converter is the third order resonant converter as same complexity as LLC converter, however it suffers from an efficiency changing as input voltage varies.

Fourth order resonant converters have two major drawbacks: 1) complicated analysis 2) the additional reactive elements affect its size, weight and efficiency.

Thus LLC resonant converter becomes increasing important with additional benefits compared with other resonant converters. The advantages of the LLC resonant topology are: [50-52]

- The leakage inductor and magnetic inductor of transformer can serve as components to build the resonant tank, which would help with reducing the overall volume of the LLC resonant converter.
- Soft-switching condition could be realized for the entire load range (from no-load to full-load), thus switching loss is very low.
- The LLC converter is easy to design with a wide range of input voltage levels and the

efficiency is kept high.

• There are low voltage stress and zero current switching (ZCS) on the secondary rectifier output voltage. No secondary filter inductor means low voltage stress on the rectifier diode. In addition, ZCS of the secondary diode removes its reverse recovery problem.

Thus LLC topology is selected here to perform as the first stage converter in the micro-inverter design.

2.2 MPPT Control for Resonant Topologies

The PV cell is a time variant power generator. The variance can be caused by irradiance and temperature difference. Thus the maximum power point (MPP) of the PV panel is always changing as illustrated in Figure 2.27. Therefore, an efficient maximum power point tracking (MPPT) technique is very important to track the maximum solar power continuously under various environmental conditions.



Figure 2. 27 PV panel power with changing environment

2.2.1 Introduction of MPPT Technologies

Since 1960s, when the MPPT was first proposed; the study of MPPT has become an important technical area for PV generator systems. Especially with the application of digital signal processor (DSP), many MPPT algorithms have been proposed and practiced in the recent decades. Generally speaking, the MPPT algorithms can be classified into four groups: direct calculation methods, intelligent methods, incremental conductance (INC) methods, and perturb and observe (P&O) methods.

Direct calculation methods adopt approximation methods to simplify the MPP determination process [53-56]. For example, [54]assumes a linear relationship between V_{MPP} and V_{OC} of the PV panel; [55]assumes a linear relationship between I_{MPP} and I_{SC} ; while [53] assume a polynomial relationship between PV power and voltage. This type of MPPTs deals with the PV panel parameters directly and requires no tracking iteration process. However, linear approximations [54, 55] have a low accuracy at MPP, while polynomial approximations [53, 56] require a complex calculation periodically.

Intelligent methods depend on expert knowledge obtained from a large database [57, 58]. Although they can perform effective MPPT, the panel dependent and time consuming data training processes are unavoidable. This type of MPPTs is not suitable for the frequency modulated LLC converter because the complicated relationship of voltage gain versus frequency would make the fuzzy logic and neural network much more complicated than for PWM converters.

Incremental conductance (INC) algorithms are based on the fact that the slope of the P-V (or P-I) curve is zero at the MPP [27, 59, 60]. Similar to P&O algorithms, an iteration step size is maintained while adjusting the control parameter until the MPP is achieved. The only difference is that P&O methods directly compare P to determine whether MPP has been achieved or not, while INC methods indirectly compare dP/dV (or dP/dI). INC methods are as efficient as P&O methods

but also suffer the same drawbacks.

P&O methods are the most widely used MPPT because of their simplicity and effectiveness. When a perturbation is applied to the control parameter, PV power is measured and compared with the previous measured PV power. If the power increases, the same perturbation is applied to get the next PV power, otherwise an opposite perturbation is made. By this process, the operating point of the system gradually moves towards the MPP and oscillates around it in steady-state conditions. For a conventional P&O method, the perturbation is fixed. If the perturbation is large, the steady state oscillation around MPP would increase, which would increase power losses. If the perturbation is small, the MPPT speed would decrease, which would prolong tracking time. Thus an appropriate perturbation is required to balance the steady state accuracy and dynamic behavior with various irradiations and loads. To improve the performance, variable perturbs P&O methods are utilized [61-64]. They can operate the MPPT with a big step-size for a fast tracking speed at start and with a small step-size for an accurate MPP close to the steady state. However, in variable step MPPT [61-64], perturbs are adjusted directly to the duty cycle, which has a simple relationship with the input voltage (or current). When MPPT is used in a resonant topology with frequency modulation which has inexplicit relationship with input voltage (or current), existing variable step P&Os could not be employed directly. Only fixed step P&Os are applied on the frequency modulation resonant converters [49, 65], which would increase MPPT tracking time and power losses.

2.2.2 Proposed Center Points Iteration MPPT

A Center Points Iteration MPPT method is proposed in this chapter. It can be implemented in resonant converters with a variable step. The advantages of the proposed MPPT are as follows:

- Directly adjust frequency for resonant converter.
- Variable perturb value during tracking progress and no oscillation under steady-state.

- Simple calculation, easy application, and fast tracking speed.
- Independent of initial environment parameters.
- Inherently deal with a part of multi-peaks power curves.

The proposed method divides the full range of the control parameter into four non-overlapped intervals with three center points. PV powers of the three points are measured and compared. Two of the four intervals are selected as the possible MPP existing intervals, and the other two are not. These existing intervals are then divided into another four intervals for the next power comparisons. The iteration is continued until the MPP is achieved. An Advanced Center Points Iteration MPPT has been derived based on this theory. The advanced version has faster MPPT and smoother tracking progress, which will reduce the power losses. The proposed MPPT is implemented in a two stage micro-inverter with a LLC resonant converter as the first stage. Simulation and experimental results demonstrate the effectiveness of the proposed MPPT method.

2.2.2.1 Verification of Proposed MPPT

Consider the problem of searching the global maximum of a function P(f) in a closed interval $[f_1, f_2]$. Assume that the maximum is achieved by $P(f_m)$, $f_m \in [f_1, f_2]$, and the function P(f) satisfies the requirements:

$$\forall f_a, f_b \in [f_1, f_m], f_a \ge f_b \Longrightarrow P(f_a) \ge P(f_b)$$

 $\forall f_a, f_b \in [f_m, f_2], f_a \ge f_b \Longrightarrow P(f_a) \le P(f_b)$

Divide the interval into fourths by three center-points: $f_3 = \frac{f_1 + f_2}{2}$, $f_4 = \frac{f_1 + f_3}{2}$, and

$$f_{5} = \frac{f_{2} + f_{3}}{2}$$
. The f_{m} has four possible positions:
(1) $f_{m} \in [f_{1}, f_{4}] \Rightarrow \begin{cases} f_{4}, f_{3}, f_{5} \in [f_{m}, f_{2}] \\ f_{4} \leq f_{3} \leq f_{5} \end{cases} \Rightarrow P(f_{4}) \geq P(f_{3}) \geq P(f_{5})$

$$(2) f_m \in [f_5, f_2] \Rightarrow \begin{cases} f_4, f_3, f_5 \in [f_1, f_m] \\ f_4 \le f_3 \le f_5 \end{cases} \Rightarrow P(f_4) \le P(f_3) \le P(f_5)$$
$$(3) f_m \in [f_4, f_3] \Rightarrow \begin{cases} f_3, f_5 \in [f_m, f_2] \\ f_3 \le f_5 \end{cases} \Rightarrow P(f_3) \ge P(f_5)$$
$$(4) f_m \in [f_3, f_5] \Rightarrow \begin{cases} f_4, f_3 \in [f_1, f_m] \\ f_4 \le f_3 \end{cases} \Rightarrow P(f_4) \le P(f_3)$$

Once $P(f_3)$, $P(f_4)$ and $P(f_5)$ are measured, the results with the aforementioned possible positions are compared:

If $P(f_3) \ge P(f_4)$, $P(f_3) \ge P(f_5)$, (3) and (4) are the possible intervals for the maximum value, and $[f_4, f_5]$ is selected as the next iteration interval.

If $P(f_4) \ge P(f_3)$, $P(f_4) \ge P(f_5)$, (1) and (3) are the possible intervals for the maximum value, and $[f_1, f_3]$ is selected as the next iteration interval.

If $P(f_5) \ge P(f_3)$, $P(f_5) \ge P(f_4)$, (2) and (4) are the possible intervals for the maximum value, and $[f_3, f_2]$ is selected as the next iteration interval.

Once the maximum function value of the three center points is obtained, the next iteration would start the local search. If iterations are continued, the interval would converge at the global maximum point.

Based on the above derivation, a MPPT technique could be generated. Any PV power function that satisfies the pre-set requirements would be compatible with the proposed MPPT method. For example, all of the power curves illustrated in Figure 2.28 are suitable for application of the proposed MPPT.



Figure 2. 28 Power curves suitable for Center Points Iteration MPPT

2.2.2.2 Implementation of Proposed MPPT on LLC Converter

A. Central points iteration MPPT control

The flowchart of the proposed MPPT technique is illustrated as Figure 2.29(b)(c). The control parameter is the switching frequency. As shown in Figure 2.29 (a), the whole frequency region is first divided into 4 parts: part 1: F(1)~F(4), part 2: F(4)~F(3), part 3: F(3)~F(5), part 4: F(5)~F(2).Considering the inductive zone of LLC converter as illustrated in Figure 2.22(c), the initial boundary frequencies are set as: F(1)=0.5F_r, F(2)=2F_r, where F_r refers to the LLC resonant frequency and can be calculated by $F_r = \frac{1}{2\pi\sqrt{L_rC_r}}$

As illustrated in Figure 2.29 (b), (2.31) is used to determine whether the LLC converter has started operation yet.

$$I_{\rm n} > \xi \tag{2.31}$$

Threshold ξ is used to determine if the initial MPPT has been finished or not. The value of ξ is based on the PV panel current measured at start point $2F_r$, which is usually very small as illustrated in Figure 2.23. If (2.31) is 'false', LLC converter has not started yet, thus the initialization begins immediately.





(c)

Figure 2. 29 Application of the proposed MPPT on the LLC micro-inverter: (a)Proposed MPPT iterations (b)Overall flowchart of MPPT (c)Detail flowchart of the proposed MPPT

As illustrated by Figure 2.29 (c), powers P3, P4 and P5 are measured specifically at frequencies F(3), F(4) and F(5).

If the maximum power is P3, the searching range can be reduced by reassignment:

F(1) = F(4), F(2) = F(5), F(3) = F(3).

If the maximum power is P5, the searching range can be reduced by reassignment:

$$F(1) = F(3), F(2) = F(2), F(3) = F(5).$$

If the maximum power is P4, the searching range can be reduced by reassignment:

$$F(1) = F(1), F(2) = F(3), F(3) = F(4).$$

The next iteration dividing center points are calculated by:

$$F(4) = \frac{F(3) + F(1)}{2}, \ F(5) = \frac{F(2) + F(3)}{2}$$

The interval is divided into 4 parts again for the next power comparisons. Keep doing the iterations until the boundary frequencies are close enough to reach the MPP criterion:

$$P_{\max}(P3, P4, P5) - P_{\min}(P3, P4, P5) < \varepsilon$$
 (2.32)

The threshold ε determines whether the MPP has been reached or not. The value is based on the current and voltage sensing accuracy. In this paper it is selected to be 0.5% P_n.

After the MPP is achieved, the MPPT is stopped and the PV current I_{in} is monitored.

$$\Delta I_{\rm in} > \sigma \tag{2.33}$$

Threshold σ is used to determine if the irradiation has been changed. When the irradiation condition changed, the PV output voltage would change slowly due to the capacitor C_{in}, leading the current to increase (or decrease) significantly beyond the limit σ . The value is also based on the input current sensing accuracy.

If (2.33) is observed 'true', the MPP may move and the new tracking progress should start again. The small value σ decides the sensitivity of the system to the environment variance. Although environment temperature may change V_{mp} in a large scale, because of the relatively high thermal inertia of PV array, the progress cannot complete in a few seconds. Moreover irradiance cannot change V_{mp} in large scale, thus the new MPPT does not need to restart from the initial interval again. As illustrated in Figure 2.29(b), searching around $F_{max}\pm 0.2F_r$ is tested enough. (F_{max} refers to the last maximum power frequency) This would speed up the new MPPT progress.



(b)

Figure 2. 30 Advanced Center Points Iteration MPPT control: (a) MPPT iterations (b) Flowchart

During the MPPT progress, the transient changes of input power would generate impulses on

the DC-link voltage. Although the impulses are non-avoidable, their magnitudes could be reduced as much as possible. In this paper, three approaches are applied to reduce the impulse:

- As illustrated in Figure 2.29 (a), the frequency is searching back and forth to ensure the perturbations are as small as possible.
- At the beginning, the frequency perturbations are huge. A buffer zone can be provided to smooth impulses caused by the huge perturbations. In the buffer zone, the frequency is changing at an acceptable small step until it reaches the expected value.

B. Advanced Center Points Iteration MPPT control

To accelerate the MPPT speed in advance, additional criterions can be included to shrink the possible maximum power existing intervals. This is referred to as Advanced Center Points Iteration MPPT control in this paper. The Advanced Center Points Iteration is illustrated in Figure 2.30.

The logic of the Advanced Center Points Iteration MPPT can be expressed simply as:

If an increasing or decreasing power trend is observed (for example in Figure 2.30(a), $P_n(4)>P_n(3)>P_n(5)$), we guess that this trend would be kept for the next testing point ($F_{n+1}(5)$). If the measured power verified this guess (if $P_{n+1}(5)>P_n(3)$), keep guessing that the trend would be kept for next testing point ($F_{n+1}(4)$) as well. Otherwise, return to do the regular Center Points Iteration MPPT in local range (between $F_{n+1}(5)$ and $F_n(3)$). Because the range can shrink based on the test result, the advanced version would accelerate the tracking speed.

•
$$P_n(4) > P_n(3) > P_n(5)$$

When $P_n(4)>P_n(3)>P_n(5)$ is observed, the PV power shows an increasing trend with the frequency decreasing. To figure out where the power increasing trend would end, switching frequencies

$$F_{n+1}(5) = (3F_{n+1}(4) + F_{n+1}(1))/4, F_{n+1}(3) = (F_{n+1}(4) + F_{n+1}(1))/2,$$

 $F_{n+1}(4) = (F_{n+1}(4) + 3F_{n+1}(1))/4$
can be tested one by one to observe where the power begins to decrease.

If $P_{n+1}(5) < P_n(4)$, which means the power increasing trend ending before $F_{n+1}(5)$, the possible maximum power interval can be reduced to $[F_{n+1}(5), F_n(3)]$.

If
$$\begin{cases} P_{n+1}(3) < P_{n+1}(5) \\ P_{n+1}(5) > P_n(4) \end{cases}$$
, which means the trend ending before $F_{n+1}(3)$, the possible maximum

power interval can be reduced to $[F_{n+1}(3), F_n(4)]$.

If
$$\begin{cases} P_{n+1}(4) < P_{n+1}(3) \\ P_{n+1}(3) > P_{n+1}(5), \text{ which means the trend ending before } F_{n+1}(4), \text{ the possible maximum} \\ P_{n+1}(5) > P_n(4) \end{cases}$$

power interval can be reduced to $[F_{n+1}(4), F_{n+1}(5)]$.

If no ends are observed in F_{n+1} iteration, new test of F_{n+2} iteration would start to shrink the interval in advance.

•
$$P_n(4) < P_n(3) < P_n(5)$$

If $P_n(4) < P_n(3) < P_n(5)$, the progress is similar with the former one to determine where the power increasing trend ends with the frequency increasing.

```
• Otherwise
```

No acceleration could be provided.

The Advanced Center Points Iteration MPPT increases complexity, however it approaches the MPP faster and can return to the normal Center Points Iteration MPPT operation if not required. With the Advanced Center Points Iteration MPPT applied, the longest tracking time takes place when the MPP is at the center frequency of the initial boundaries. Since no trend was observed in the process, the Advanced Center Points Iteration MPPT would default to normal Center Points Iteration MPPT operation.

C. Partial shaded application

When the PV panel is operating in a partial shaded condition, the P-V characteristic is more

complicated than uniform isolations, which would generate multi-peaks on the power curve. Only one of the peaks is the global maximum power point which should be tracked, the others are local maximum points which should be avoided. When the power curve satisfies the requirement in section II, the proposed MPPT is effective to track the global peak.



(b)

Figure 2. 31 MPPT tracking with proposed MPPT under partial shading: (a)P-V curve with I-V curve (b) P-Fs curve

An example of a partial shading PV panel is provided by Figure 2.30 (a). There are three peaks P₁, P₂, and P₃ for the whole P-V curve. P₂ is the global peak while P₁ and P₃ are local peaks. Conventional INC or P&O algorithms could not identify the global peak. If they are applied here, wrong peaks would be tracked. However, the proposed MPPT with flowchart illustrated in Figure 2.28 (c) would track the global peak. The supposed tracking process is illustrated in Figure 2.30. Advanced Center Points Iteration MPPT control would increase tracking speed because of near boundary frequency at P_2 as illustrated in LLC simulation curve Figure 2.30 (b).

2.2.3 Simulation Results

2.2.3.1 Simulation Results on LLC Resonant Converter

A simulation prototype was built with Simulink to prove the proposed MPPT algorithm.

PV system parameters are set as: PV panel curve: I_{sc} =11.2A, V_{oc} =41.2V, I_{mp} =9.6A, V_{mp} =31.25V, P_{max} =300W; LLC converter parameters: C_r =680nF, L_r =1.9uH, L_m =10.3uH, n=5.55, F_r =140kHz; Initial frequency range: 70kHz~280kHz; the reference DC link voltage is set as V_{ref} =400V. The input capacitor connected to the PV panel: C_{in} =22uF (the calculation of C_{in} is provided in appendix)



Figure 2. 32 V-I simulation waveforms of LLC converter with variance frequencies

When a DC current source I_{in} is connected to the LLC converter with the restricted DC link voltage V_{ref} , the data of V_{in} can be recorded at different switching frequencies under various I_{in} values. The fitting V-I curves with the PV panel curve as a comparison are illustrated in Figure 2.31. They illustrate the same characteristics as analyzed in section III, which verify the

correctness of the calculations in Figure 2.2.



Figure 2. 33 Overall control diagram of the proposed MPPT for grid-tied two-stage LLC micro-inverter

The overall control diagram of the proposed MPPT for grid-tied two-stage LLC micro-inverter is illustrated in Figure 2.32. The PI voltage regulator is applied on the DC/AC inverter to regulate the bus voltage to V_{ref} , and the feed forward I_{ref} is calculated from I_{in} and V_{in} ($I_{ref}=V_{in}I_{in}/V_{ref}$) to accelerate the reaction time of the PI regulator. The proposed MPPT control method is realized on the DC/DC converter stage.

Simulation waveforms of the micro-inverter applied the proposed MPPT are illustrated in Figure 2.33.



Figure 2. 34 Proposed MPPT operation waveforms: (a) PV power vs Time (b) Switching frequency vs Time (c) DC-link voltage vs Time

As illustrated in Figure 2.28, the frequency of $P_{max}(P3,P4,P5)$ is used as the center point of the next iteration, so that the power at this frequency does not need measurement again. Thus excluding the first iteration, every iteration has only two frequencies. The waveforms are illustrated in Figure 2.33, the first iteration has three different frequencies; while other iterations

have two frequencies. This saves the simulation time.

From the observation of Figure 2.33, the proposed MPPT method uses 3 iterations to enter the maximum power range ($P_{max}\pm5\epsilon$), and 5 iterations to convergent at the MPP. Figure 2.33 (c) shows that the dc-link voltage has impulses when frequency perturbations taking place. With the perturbation decreasing, the impulse magnitude is decreasing.



(c)

Figure 2. 35 MPPT waveforms when irradiation changing from 100% to 50% at the time $t_x=0.2s$:(a) PV power vs Time (b) Switching frequency vs Time (c) DC-link voltage vs Time

Figure 2.33 shows that when a sudden change from 100% to 50% irradiation takes places at time t_x =0.2s, the proposed MPPT algorithm uses 1 iteration to enter the maximum power range ($P_{max}\pm5\epsilon$), and 4 iterations to convergent at the new MPP.

Advanced Center Points Iteration MPPT is implemented on the same prototype, and simulation waveforms are illustrated in Figure 2.35. The MPPT takes only 1 iteration to enter the maximum power range ($P_{max}\pm5\epsilon$), and 4 iterations to achieve the MPP. Compared with Figure 2.33, it saves the tracking time and power losses during the tracking process.



(c)

Figure 2. 36 Advanced Center Points Iteration MPPT control: (a) PV power vs Time (b) Switching frequency vs Time (c) DC-link voltage vs Time

To give a comparison with the proposed MPPT, conventional P&O controllers with fixed perturb are implemented on the simulation prototype.



Figure 2. 37 Conventional fixed perturb P&O MPPT: (a) $\Delta f_s=10$ kHz, (b) $\Delta V_{in}=1V$

Figure 2.37 (a) shows the MPPT curve with a fixed perturb step Δf_s =10kHz provided to the switching frequency. The initial frequency is 200kHz to avoid the "flat section" near 280kHz as shown in Figure 2.23. As illustrated in Figure 2.37 (a), to avoid the oscillation under steady state, if an oscillation is observed and confirmed, the P&O would be stopped at the higher power point. If the perturb step is reduced, the oscillation would decrease while the tracking time would increase. Moreover, it is obvious to observe from Figure 2.23 that with irradiance decreasing, lower start frequency is required to operate the MPPT successfully. For example, under 500W/m², it is better to start MPPT at 160kHz.

Figure 2.36 (b) shows the MPPT curve with a fixed perturb step ΔV_{in} =1V. The perturbation is provided to the input voltage by adding a PI regulator on the LLC stage. As illustrated in Figure 2.36 (b), the frequency adjustment caused by the PI regulator induces high frequency power oscillation, which is unavoidable. The oscillation magnitude generates low accuracy MPP. With the perturbation reduced, the oscillation would not be decreased.



(a)

(b)

Figure 2. 38 Proposed MPPT operation waveforms under partial shading condition: (a) PV power vs Time (b) Switching frequency vs Time

Figure 2.36 illustrated the operation waveforms of the proposed MPPT when partial shading of Figure 2.31 is provided. The operation process is exactly as same as expected in Figure 2.31.

2.2.3.2 Simulations on Other Resonant Converters

The proposed MPPT is also suitable to be applied on other resonant converters analyzed before. Simulation prototypes were built with Simulink to carry out the proposed MPPT to support the analysis.

A. PRC

PV system parameters are set as: PV panel curve: $I_{sc}=11.2A$, $V_{oc}=41.2V$, $I_{mp}=9.6A$, $V_{mp}=31.25V$, $P_{max}=300W$; PRC converter parameters: $C_p=1uF$; $L_s=5uH$; n=5.5, $F_r=71.2kHz$; Initial frequency range: 60kHz~106kHz; the reference DC link voltage is set as $V_{ref}=400V$. Simulation waveforms are illustrated in Figure 2.38.



(a)

(b)

Figure 2. 39 Proposed MPPT operation waveforms on PRC converter: (a) PV power vs Time (b) Switching frequency vs Time

B. LCC

PV system parameters are set as: PV panel curve: $I_{sc}=11.2A$, $V_{oc}=41.2V$, $I_{mp}=9.6A$, $V_{mp}=31.25V$, $P_{max}=300W$; PRC converter parameters: $C_s=1uF$, $C_p=1uF$, $L_p=10uH$, n=5.5, $F_r=71.2kHz$; Initial frequency range: 72kHz~90kHz; the reference DC link voltage is set as $V_{ref}=400V$. Simulation waveforms are illustrated in Figure 2.39.



(b)

Figure 2. 40 Proposed MPPT operation waveforms on PRC converter: (a) PV power vs Time (b) Switching frequency vs Time

C. LCLC

PV system parameters are set as: PV panel curve: $I_{sc}=11.2A$, $V_{oc}=41.2V$, $I_{mp}=9.6A$, $V_{mp}=31.25V$, $P_{max}=300W$; PRC converter parameters: n=4, $V_{ref}=400V$, $C_s=1.17uF$, $C_p=0.585uF$, $L_s=4.06uH$, $L_p=8.12uH$, $F_r=73.04kHz$; Initial frequency range: 150kHz~180kHz; the reference DC link voltage is set as $V_{ref}=400V$. Simulation waveforms are illustrated in Figure 2.40.



(b)

Figure 2. 41 Proposed MPPT operation waveforms on PRC converter: (a) PV power vs Time (b) Switching frequency vs Time

As illustrated in Figure 2.39~Figure 2.41, proposed MPPT operation can successfully track the maximum power point on various resonant converter topologies.

2.2.4 Experiment Results

2.2.4.1 Experiment Results on LLC Prototype

A LLC micro-inverter prototype was built to carry out the proposed MPPT algorithm. A solar array simulator (Agilent Modle E4360A) was used to simulate a PV source. For the LLC converter, the circuit parameters are set as: $C_{in}=22uF$, $C_r=680nF$, $L_r=1.9uH$, $L_m=10.3uH$, n=5.5, $F_r=140kHz$. The DC link voltage is controlled to be 400V. The initial searching interval is [70kHz, 280kHz].

The Cin refers to the input capacitance connected in parallel with PV panel, which is used to

stabilize the input voltage. For the LLC converter, considering the maximum input current condition, which would generate maximum ripple on input capacitor, the basic equation $\int i_{C_m} = \int C \frac{dV_{C_m}}{dt}$ is used to calculate the capacitance.



(c)

Figure 2. 42 Input capacitor current with various switching frequencies: (a) $F_s < F_r$ (b) $F_s > F_r$ (c) $F_s = F_r$

Based on simulation, input capacitor current is illustrated in Figure 2.41, where

$$t_x \le 2.3 us \tag{2.34}$$

The LLC resonant cycling period is

$$T_r = 1/140 \text{kHz} = 7.143 \text{us}$$
 (2.35)

Thus input capacitance could be calculated with

$$C_{in} = \frac{\int i_{C_{in}}}{\Delta V_{C_{in}}} \le \frac{\int^{t_x} I_{in, peak}(\sin\omega t - \sin\omega(\frac{T_s}{4} - \frac{t_x}{2}))dt}{\Delta V_{C_{in}}}$$
(2.36)

Assume that $\Delta V_{Cin} < 1V$, $I_{in,peak} < 20A$, the input capacitance should be larger than 14.15uF. In this prototype, the input capacitance is selected to be 22uF.



Figure 2. 43 Advanced Center Points Iteration MPPT waveforms with different PV curves: (a) $I_{sc}=5A$, $V_{oc}=34V$, $V_{mp}=29V$, $I_{mp}=4A(b)I_{sc}=11A$, $V_{oc}=34V$, $V_{mp}=30V$, $I_{mp}=10A$ (c)MPP changing from $I_{mp}=5A$, $V_{mp}=31V$ to $I_{mp}=4A$, $V_{mp}=29V$ (b)MPP changing from $I_{mp}=4A$, $V_{mp}=29V$ to $I_{mp}=5A$, $V_{mp}=31V$

Figure 2.43 demonstrates the Advanced Center Points Iteration MPPT applied on the prototype. Figure 2.42 (a) shows the MPPT waveforms with PV curve: $I_{sc}=5A$, $V_{oc}=34V$, $I_{mp}=4A$, $V_{mp}=29V$ set inside the solar array simulator. Figure 2.43 (b) shows the MPPT waveforms under PV curve: $I_{sc}=11A$, $V_{oc}=34V$, $I_{mp}=10A$, $V_{mp}=30V$. Figure 2.43 (c) and (d) shows the MPPT when MPP is changing from $I_{mp}=5A$, $V_{mp}=31V$ to $I_{mp}=4A$, $V_{mp}=29V$, and changing back individually. As illustrated in Figure 2.43, the Advanced Center Points Iteration MPPT shows a fast tracking speed with little oscillation in steady state. Figure 2.43 has a smooth MPPT progress because of the buffer zone provided for the large frequency perturbation.

To observe the Advanced Center Points Iterations MPPT more clearly, less buffer zone is provided and iterations are slowed down. Experiment waveforms are as shown in Figure 2.43.



(c)

Figure 2. 44 Advanced MPPT waveforms with less buffer and reduced iteration time with different PV curves: (a) $I_{sc}=5A$, $V_{oc}=34V$, $I_{mp}=4A$, $V_{mp}=29V(b)$ MPP changes from $I_{mp}=4A$, $V_{mp}=29V$ to $I_{mp}=5A$, $V_{mp}=31V$ (b) MPP changes from $I_{mp}=5A$, $V_{mp}=31V$ to $I_{mp}=4A$, $V_{mp}=29V$

Figure 2.44 illustrates the advanced MPPT applied on the prototype with fewer buffers. Figure 2.44 (a) shows the MPPT waveforms of the prototype under PV curve: $I_{sc}=5A$, $V_{oc}=34V$, $I_{mp}=4A$, $V_{mp}=29V$. The MPPT takes 2 iterations to enter the maximum power range ($P_{max}\pm5\epsilon$), and 3 iterations to achieve the MPP. Figure 2.44 (b) shows the MPPT waveforms when the PV curve is changing from $I_{sc}=5A$, $V_{oc}=34V$, $I_{mp}=4A$, $V_{mp}=29V$ to $I_{sc}=6A$, $V_{oc}=34V$, $I_{mp}=5A$, $V_{mp}=31V$. The MPPT takes 2 iterations to enter the maximum power range ($P_{max}\pm5\epsilon$), and 4 iterations to achieve the MPP. Figure 2.44 (c) shows the MPPT waveforms when the PV curve is changing back. The MPPT takes 1 iterations to enter the maximum power range ($P_{max}\pm5\epsilon$), and 2 iterations to achieve the MPP.

Figure 2.44 demonstrates the process detail of the advanced MPPT clearly as it is slowed down for observation purposes. Although the number of MPP required iterations is dependent on specific conditions, the proposed MPPT can always enter the maximum power region ($P_{max}\pm5\epsilon$) in one or two iterations, which is very fast compared with the conventional P&O MPPT.



Figure 2. 45 Center Points Iteration MPPT under PV curve: I_{sc} =5.6A, V_{oc} =38.5V, V_{mp} =28.5V, I_{mp} =4.9A (a)Normal Center Points Iteration MPPT (b)Advanced Center Points Iteration MPPT

To give a comparison with the Normal Center Points Iteration MPPT, an experiment was performed on the same prototype. The MPPT waveforms are as illustrated in Figure 2.45. PV curve is set as: I_{sc} =5.6A, V_{oc} =38.5V, V_{mp} =28.5V, I_{mp} =4.9A. Figure 2.45 (a) shows that the Normal

Center Points Iteration MPPT takes 4 iterations to enter the maximum power region, and more than 5 iterations to reach the MPP. While Figure 2.45 (b) shows that the Advanced Center Points Iteration MPPT takes 2 iterations to enter the maximum power region, and 3 iterations to reach the MPP.

Figure 2.45 shows that the Advanced Center Points Iteration MPPT really makes improvement as expected based on the Normal Center Points Iteration MPPT.

2.2.4.2 Experiment Results on LCLC Prototype

A LCLC converter prototype was built to carry out the proposed MPPT algorithm. A solar array simulator (Agilent Modle E4360A) was used to simulate a PV source. For the LCLC converter, the circuit parameters are set as: $C_{in}=22uF$, $C_s=590nF$, $C_p=276nF$, $L_s=6.23uH$, $L_p=12.6uH$, n=2.26, $F_r=84kHz$. Since only DC/DC converter is provided here, the output DC voltage of the LCLC converter is uncontrolled to regulate the output power.

Based on the analysis about the LCLC resonant converter in section 2.1.2.3, the initial searching interval is selected to be $[1.9F_r, 2.5F_r]$, which is [160kHz, 210kHz].



Figure 2. 46 Advanced Center Points Iteration MPPT waveforms with different PV curves: (a) I_{sc} =5.6A, V_{oc} =38V, V_{mp} =28V, I_{mp} =4.9A (b)MPP changing from I_{mp} =2A, V_{mp} =25V to I_{mp} =4A, V_{mp} =30V

Figure 2.46 illustrates the advanced MPPT applied on the LCLC prototype. Figure 2.46 (a) shows the MPPT waveforms of the prototype under PV curve: $I_{sc}=5A$, $V_{oc}=34V$, $I_{mp}=4A$, $V_{mp}=29V$.

Figure 2.46 (b) illustrates the advanced MPPT operation when the maximum power point suddenly changed from $I_{mp}=2A$, $V_{mp}=25V$ to $I_{mp}=4A$, $V_{mp}=30V$. As illustrated in Figure 2.46, the Advanced Center Points Iteration MPPT shows a fast tracking speed with little oscillation in steady state. For the LCLC topology, the initial frequency range is much narrower than the LLC topology.

2.3 Summary

In this chapter, the importance of DC/DC converter is analyzed carefully as a construction part of the two-stage micro-inverter with the technical requirements listed out. The resonant converters with advantages in soft switching and high switching frequency are good candidates for the two-stage micro-inverter. The operations of various conventional resonant converters are analyzed carefully in frequency domain. Because the LLC topology among these resonant converters has further advantages in soft switching under various loads, it is selected as the DC/DC stage.

To track the maximum power point of the PV panel, MPPT function is very important to harvest solar power continuously under various environments. Although a lot of MPPT techniques have been proposed since the 1960s, few of them deal with frequency modulation on resonant converters. A center points iteration MPPT is proposed in this chapter. The MPPT is verified to be suitable for various PV power curves as analyzed. The simulation PV power curves of the LLC micro-inverter under various irradiances have a flat section which would mislead the conventional MPPT. However, the proposed MPPT could solve the problem with Center Points Iteration. Moreover the proposed MPPT has a fast tracking speed and little oscillation power loss in steady state. An Advanced Center Points Iteration MPPT is induced based on the same theory to accelerate the tracking speed. Flowcharts of the MPPT are provided to apply the theory with a DSP.

Simulation and experiment results verify the effectiveness of the proposed MPPT. To expand

the MPPT application, the simulations of proposed MPPT on other resonant converters are carried out. The waveforms show the feasibilities.

The proposed MPPT is also applied on other resonant converters under simulations with MATLAB SIMULINK. Waveforms support its effectiveness in frequency modulation on various resonant converters. Moreover, a LCLC converter prototype is also built to carry out the experiments to confirm the analysis in advance. The experiment results match with the theory analysis as expected.

CHAPTER THREE: DC/AC INVERTER STAGE

3.1 DC/AC Inverter Topologies Introduction

In double-stage micro-inverter PV systems, the DC/AC inverter stage is employed to convert DC power into AC power and feed the power into the utility grid. Since the input side is high constant DC voltage generated by the DC/DC converter stage, and galvanic isolation is already realized in DC/DC converter stage, the DC/AC inverter stage has no requirements in voltage rising and isolation. Thus a lot of topologies are suitable to apply here.

Based on the topologies' differences, the DC/AC inverters can basically be divided into three groups: voltage source inverter (VSI), current source inverter (CSI), and impedance source inverter (ZSI), which are illustrated individually in Figure 3.1.



Figure 3. 1 Three classes of inverters topologies: (a) VSI (b) CSI (c)ZSI

Figure 3.1(a) shows the topology of a conventional VSI. According to the literatures[66, 67],

so far VSIs are the dominant topologies for PV inverter applications with advantages below.

- Mature in topologies and controller design techniques.
- Various existed soft switching methods for efficiency improvement.
- Broad applications in whole power levels.

There are also some disadvantages of the typical VSIs which have to be considered in design.

- The maximum ac voltage output of a VSI is limited by the dc input source voltage because of the buck intrinsic quality. Dead-time to block both upper and lower devices for safety considerations which would cause waveform distortion.
- An output LC filter is needed in providing a sinusoidal voltage compared with the CSI, which would cause additional power loss and increase control complexity.

The current source inverter (CSI) as illustrated in Figure 3.1(b) does offer some specific advantages below. CSIs are now another option for the PV inverter application with advantages below.[66]

- Intrinsic boost function which has less strict requirement on the DC bus voltage.
- Implicit output short circuit protection.
- Significantly reduced electromagnetic interference because of the capacitive voltage filters located directly on the inverter output.[68]

There are also some disadvantages of the CSIs mentioned as below which have limited the application of the CSIs.

- Usually a relatively large inductor connecting with dc bus voltage in series is required.
- At least one of the upper devices and one of the lower devices have to be gated on at any time. Overlap time is also required for safety consideration which would cause waveform distortion.
- The main switches have to block reverse voltage that requires series diodes in combination, which increases the conduction losses.

The CSIs are mainly known from high power level and lately are investigated in the

application of medium and low power PV inverter.[69, 70]

The Z-source inverter is a combination of VSI and CSI, as illustrated in Figure 3.1 (c). Since proposed in the last decade by paper [71], ZSIs are widely studied and analyzed for advantages below.

- They can operate as either the voltage source or the current source type.
- Theoretically, the voltage gain can be any value between $0 \sim \infty$.
- No safety problem caused by short circuit or open circuit.
 There are also some disadvantages of the ZSIs.
- Contains relatively high input current ripples, which may result in high stresses on the DC-link inductors and capacitors.[72]
- More complicated in controller design compared with VSIs and CSIs.
- No soft switching techniques available now for ZSIs.

Thus the ZSIs are rarely implemented for low power applications [73-76].

Considering the application of the DC/AC inverter stage, which is connected with a resonant DC/DC converter described in chapter two, the efficiency and volume requirements have the highest priority. Thus the VSI with the soft switching techniques available is the most competitive candidate compared with CSI and ZSI. Moreover, the micro-inverter usually has a low power level, which is rarely implemented by CSI and ZSI. In addition, as the first DC/DC stage has realized the voltage rising function, the advantages of CSI and ZSI in boost intrinsic are no longer competitive. Combining these considerations, VSI is selected for the application of the DC/AC inverter stage here.

3.2 Review of the Soft Switching Technologies on Inverters

In the application of VSI, increasing the switching frequency has become a design trend as it can decrease the size of both the reactive filter and energy-storage capacity, thus achieving higher power density and better dynamic performance. However, higher switching frequency results in not only higher switching losses but also more severe electromagnetic interference (EMI).

To increase the switching frequency, while maintaining the decent conversion efficiency and low EMI, soft switching is one of best options.

In the recent decades various soft switching methods have been proposed [77-80]. They can generally be classified into two categories: passive soft switching [78-80] and active soft switching [81-94]. Active soft switching techniques, which usually can realize soft-switching conditions at full load range with high switching frequency, are preferable in recent research.

A variety of active soft switching topologies have been proposed in last three decades [81-94]. Most of them can be divided into three groups: auxiliary resonant commutated pole (ARCP) group [81-84], resonant DC link inverter (RDCLI) group [85-90], and resonant AC-link converter (RACLC) [91-94].

3.2.1 ARCP

Since the basic ARCP topology was proposed in 1990, many soft switching topologies have been derived from the conventional ARCP topology [81-84]. Soft switching can be realized on both main switches and auxiliary switches. Although they can be applied broadly for the voltage source type single phase or three phase inverter, the number of auxiliary components is difficult to reduce.

3.2.2 RDCLI

The RDCLI was first proposed in 1986, and many topologies have been induced based on the fundamental RDCLI [85-90]. Comparing with the ARCP, they have the advantages of a lower number of auxiliary switches, lower voltage stress on the main switches and simpler control circuit for auxiliary switches [85-88]. For example, [89, 90] are proposed as minimum components soft switching topology. However, the driving signals of the auxiliary switches are always easily

influenced by various disturbances such as actions of the main switches.

3.2.3 RACLC

The RACLC was also proposed in 1990. The RACLC topologies are preferred as they can realize voltage boosting and electrical isolation at the same time [91-94], which is an advantage for the application of new energy power system generation. However the control circuit is complex and the bi-directional switches are required.

3.3 The Proposed BCM Technique Without Auxiliary Components

Auxiliary components are unavoidable for all of the soft switching topologies mentioned above. They construct a high-frequency resonant network centered around the main semiconductors [95, 96]. During their commutations the resonant network operates for a very short period to create ZVS or ZCS conditions for the main semiconductors.

The proposed soft switching technique simplifies the inverter topology and reduces the cost as it does not require any auxiliary components. The body capacitors of the main MOSFETs and the output linear inductor are applied together to form a resonant circuit. The inductor current is intentionally operated in bi-direction within a switching cycle to generate ZVS conditions during commutations. Meanwhile the average inductor current is controlled to generate an AC voltage on the output capacitor. The realization of ZVS decreases switching losses while the bi-directional current increases conduction losses (because the bi-directional current increases the rms value). A trade-off has to be made between them. The proposed soft switching technique is suitable for low power applications, where the switching losses usually are dominant.

Three different current mode control schemes are derived from the basic operation principle of the proposed soft switching technique. They are referred to as Boundary Current Mode (BCM) control scheme, Variable Hysteresis Current Mode (VHCM) control scheme, and Constant Hysteresis Current Mode (CHCM) control scheme respectively. All of which are easily implemented with a digital controller.



3.3.1 Operation Principle of the Proposed ZVS Technique

(c)



Figure 3.2 illustrates a set of inverter topologies suitable to operate the proposed soft switching technique. Figure 3.2(a) demonstrates a single-phase full bridge inverter; Figure 3.2(b) demonstrates a single-phase half bridge inverter; and Figure 3.2(c) demonstrates a three-phase half bridge inverter. For the three-phase half bridge inverter, because the three phases are decoupled, each phase operates independently as the same as single-phase half bridge inverter. Therefore, in this paper, the detailed operation principles and design considerations are analyzed only for single-phase inverter topologies (including both half and full bridge single-phase inverters).

In Figure 3.2 the diode and capacitor in parallel with the switch are the body diode and the

parasitic capacitance of MOSFET respectively. To achieve zero voltage switching conditions, each MOSFET should be turned on after its body diode is conducting. Therefore, a bi-directional inductor current is required for every switching cycle.



Figure 3. 3 Key waveforms of BCM inverter

3.3.1.1 Full bridge single-phase inverter

Figure 3.2 (a) illustrates a full-bridge single-phase inverter with one leg operating in switching frequency and the other leg operating in line frequency. To simplify the analysis, assume that the whole inverter system has achieved steady state, and the output voltage (V_o) is predominantly sinusoidal. Since the switching frequency (f_s) is much higher than the output voltage frequency, the load voltage (V_o) is assumed to be constant in one switching period (T_s) . The positive directions of the output voltage and the inductor current are illustrated as Figure 3.4 <stage 1>. Depending on the polarity of the output voltage, the operation of the inverter can be divided into two modes: 1. Mode 1 (V_o >0); 2. Mode 2 (V_o <0). Each mode has 6 stages as shown in



Figure 3.4. The detailed analysis is as follows.

Figure 3. 4 Operation stages for the full bridge single-phase inverter

• Mode 1 ($V_0 > 0$)

Stage 1 $[t_0-t_1]$: During this stage Q_1 and Q_4 are on, whereas Q_2 and Q_3 are off. The DC voltage transfers energy to the inductor and the inductor current increases linearly. The voltage across output capacitor C_1 is zero and the voltage across capacitor C_2 is equal to the input voltage.

$$\begin{cases} i_{Ls}(t) = \frac{(V_d - u_o)}{L_s} t + i_{Ls}(t_0) \\ V_{C_1}(t) = 0 \\ V_{C_2}(t) = V_d \end{cases}$$
(3.1)

Stage 2 $[t_1-t_2]$: Q_1 turns off when the inductor current reaches the expected peak current at time t_1 . The output capacitors of the MOSFETs C_1 and C_2 are charged and discharged respectively through the inductor current until C_2 is fully discharged. The status expressions are depicted as

$$\begin{cases} V_{C_1}(t) = k_1 \cos(\omega_0 t) + k_2 \sin(\omega_0 t) + V_d - V_o \\ i_{L_s}(t) = \frac{1}{Z_0} (-k_1 \sin(\omega_0 t) + k_2 \cos(\omega_0 t)) \end{cases}$$
(3.2)

Where

$$k_{1} = \frac{V_{o}cos(\omega_{0}t_{1}) - I_{p} + Z_{0}sin(\omega_{0}t_{2})}{cos\omega_{0}(t_{1} - t_{2})} , \quad k_{2} = \frac{V_{o}sin(\omega_{0}t_{1}) + I_{p} + Z_{0}cos(\omega_{0}t_{2})}{cos\omega_{0}(t_{1} - t_{2})} , \quad \omega_{0} = \frac{1}{\sqrt{2CL_{s}}} ,$$

$$Z_{0} = \sqrt{\frac{L_{s}}{2C}}, C_{1} = C_{2} = C$$

Stage 3 $[t_2-t_3]$: As C₁ is charged above DC bus voltage, the inductor current freewheels through the body diode D₂, creating zero voltage switching condition for Q₂. The inductor current flows through the body diode D₂ and decreases linearly as shown in Figure 3.3.

Stage 4 [t_3 - t_4]: At time t_3 , with the arriving of the driver signal for Q_2 , the conductivity of the MOSFET increases. Thus the inductor current can be regarded as shifting from D_2 "channel" to Q_2 conductive "channel". The inductor current first decreases to zero and then increases in the negative direction. The status equations in this stage are the same as those in stage 3.

Stage 5 [t_4 - t_5]: At time t_4 , Q_2 turns off, and the negative peak current charges the capacitor C_2 to DC bus voltage and discharges the capacitor C_1 to zero voltage respectively. The status equations in this stage are the same as those in stage 2.

Stage 6 [t_5 - t_6]: When the voltage across C_2 increases above DC bus voltage, the body diode D_1 freewheels the inductor current. The status equations are the same as stage 1.



Figure 3. 5 Operation stages for the half bridge single-phase inverter

• Mode 2 ($V_o < 0$)

The analysis for this mode is similar to the analysis for mode 1 except Q_2 and Q_3 are kept the on-state for all the six stages.

It is worth noting that a power MOSFET is commonly considered as a uni-directional switch since it blocks voltage only in one direction. However, a power MOSFET can conduct currents in both directions. The operation of low voltage power MOSFETs in their third quadrant (when $V_{ds} < 0$ and $I_{ds} < 0$) is widely used in synchronous rectifier buck converters. The use of higher voltage (i.e.

600V in our case) power MOSFET in the third quadrant is less common, but nevertheless follows a similar operation principle.

3.3.1.2 Half bridge single-phase inverter

Figure 3.2 (b) illustrates a half-bridge single-phase inverter circuit. It can also be regarded as one phase of the three-phase inverter as shown in Figure 3.2 (c). Take Figure 3.2 (b) as an example, when the switching commutation takes place the body capacitors C_1 , C_2 and the inductor L_s construct a resonant network to generate zero voltage condition for the next turning-on switch during the dead time. The analysis procedure is the same as the afore-presented full-bridge inverter. The operation equivalent circuits for each stage are illustrated as in Figure 3.5.

3.3.2 Current Modulation Design



(c)

Figure 3. 6 Inductor current waveforms for different current mode control schemes:(a)BCM, (b)CHCM, (c)VHCM

To ensure that the average output current during every switching cycle is equal to Io,peaksinot,

requirement $I_{p+}+I_{p-}=2I_{o,peak}\sin\omega t$ has to be satisfied in every switching cycle. (I_{p+} and I_{p-} refer to the positive and negative peak currents individually.)

The proposed current control schemes satisfy the requirements as illustrated in Figure 3.6. For these three schemes, I_{p+} and I_{p-} have different expressions. (To simplify the analysis all the expressions are under $V_0>0$ condition.)

3.3.2.1 Boundary Current Mode (BCM)

As illustrated in Figure 3.6(a), the BCM mode is featured with a fixed reverse current ΔI , where the peak current I_{p+} and I_{p-} can be expressed as:

$$\begin{cases} I_{p+} = 2I_{o, peak} \sin \omega t + \Delta I \\ I_{p-} = -\Delta I \end{cases}$$
(3.4)

$$I_{p+}-I_{p-}=2(I_{o, peak}\sin\omega t + \Delta I)$$
(3.5)

3.3.2.2 Constant Hysteresis Current Mode(CHCM)

The CHCM mode is shown as Figure 3.6(b). This mode is featured with a constant hysteresis. The peak current I_{p+} and I_{p-} can be expressed as:

$$\begin{cases} I_{p+} = I_{o, peak} \sin \omega t + \Delta I \\ I_{p-} = I_{o, peak} \sin \omega t - \Delta I \end{cases}$$
(3.6)

$$\mathbf{I}_{p+} - \mathbf{I}_{p-} = 2\Delta \mathbf{I} \tag{3.7}$$

3.3.2.3 Variable Hysteresis Current Mode (VHCM)

The VHCM mode is shown as Figure 3.6(c). This mode has a variable current band with a variable reverse current. The peak currents I_{p+} and I_{p-} can be expressed as:

$$\begin{cases} I_{p+} = (2I_{o, peak} - I^*) \sin \omega t + \Delta I \\ I_{p-} = I^* \sin \omega t - \Delta I \end{cases}$$
(3.8)

$$I_{p+}-I_{p-} = 2[(I_{o, peak} - I^*)sin\omega t + \Delta I]$$
(3.9)

For (3.9), $0 < I^* < I_{o,peak}$, when I^* decreases to zero (3.9) can be simplified to (3.5) and when I^* increases to $I_{o,peak}$ (3.9) can be simplified to (3.7).

As analyzed before, the key point of this soft switching technique is that the inductor current should be large enough to generate the zero voltage condition during the switching transition periods as shown in Figure 3.3. Thus the dead time and the peak inductor current should satisfy the equation below.

$$t_{\text{deadtime}} > t_{\text{D}} = 2CV_{\text{in}}/I_{\text{p}+/-}$$
(3.10)

Where $t_{deadtime}$ refers to deadtime, and t_D refers to time required to generate ZVS.

To simplify the analysis, $t_{deadtime}$ is assumed to be much smaller than the switching periods and duty cycles. According to the voltage-second balance across the inductor L_s the expression of turn-on/off time and switching frequency can be derived for the half bridge inverter as:

$$\begin{cases} t_{on} = \frac{L_{s}(I_{p} + -I_{p})}{V_{d} - u_{o}} \\ t_{off} = \frac{L_{s}(I_{p} + -I_{p})}{V_{d} + u_{o}} \\ F_{s} = \frac{V_{d}^{2} - u_{o}^{2}}{2L_{s}(I_{p} + -I_{p})V_{d}} \end{cases}$$
(3.11)

The maximum and minimum frequencies of the half bridge inverter are

$$\begin{cases} F_{smin} = F_s \mid (\omega t = \frac{\pi}{2}) \\ F_{smax} = F_s \mid (\omega t = 0) \end{cases}$$
(3.12)

For the full bridge inverter the equation for turn-on/off time and switching frequency can be expressed as:

$$\begin{cases} t_{on} = \frac{L_{s}(I_{p} + -I_{p})}{V_{d} - u_{o}} \\ t_{off} = \frac{L_{s}(I_{p} + -I_{p})}{u_{o}} & (u_{o} = V_{o,peak} |sin\omega t|) \\ F_{s} = \frac{u_{o}V_{d} - u_{o}^{2}}{L_{s}(I_{p} + -I_{p})V_{d}} \end{cases}$$
(3.13)

Based on equations (3.11) and (3.13) the frequency comparison waveforms for full bridge inverter and half bridge inverter can be illustrated as Figure 3.5 (a). (Figure 3.5 (a) shows the



(a)



Figure 3. 7 (a)Switching frequency comparison waveforms, (b)Inductor current rms value comparison

waveforms of the switching frequency VS ω t.) For the same topology under the same controller scheme, the shapes of frequency waveforms are similar with each other. Moreover, for the same set of V_d, V_o, P_o, and L_s, the full bridge inverter always has a lower switching frequency than the half bridge inverter. It is obvious to observe from Figure 3.7 (a) that for the full bridge topology the switching frequency increases/decreases rapidly near the area of k π (k is integer 0,1,2...) and

achieves zero at the points of $k\pi.(u_o=V_{o,peak}|sink\pi|=0 \rightarrow F_s = \frac{u_oV_d - {u_o}^2}{L_s(I_{p+}-I_{p-})V_d} = 0)$ For the filter

design consideration usually the switching frequency is not changing from zero to the maximum value shown as Figure 3.7 (a). So when the switching frequency drops close to zero all switches could be turned off at the same time until the switching frequency rises up away from zero again.

This period is referred as all-off period in this paper. When the all-off period is small enough the output voltage distortion caused by this period could be neglected (When the all-off period is less than $\pi/36$, THD caused by the all-off period is less than 1%). Based on equation (3.13) and the distortion consideration of the all-off period, the maximum and minimum frequency expression of full bridge inverter are derived:

$$\begin{cases} F_{smin} = F_{s} \mid \omega t = \frac{\pi}{72} \\ F_{smax} = \begin{cases} F_{s} \mid V_{o, peak} \sin \omega t = \frac{V_{d}}{2} & CHCM \\ F_{s} \mid \sin \omega t = \sqrt{\left(\frac{\Delta I}{I}\right)^{2} + \frac{\Delta I V_{d}}{I V_{o, peak}}} - \frac{\Delta I}{I} & BCM \\ VHCM \end{cases}$$
(3.14)

Where, for BCM: I=I_{o,peak}, and for VHCM: I=I_{o,peak}-I^{*}.

Based on equations (3.4-3.9) the frequency comparison waveforms for three different current mode control schemes are also illustrated in Figure 3.7 (a). It is obvious to observe from Figure 3.7 (a) that for both inverter topologies the BCM has the widest switching frequency range while the CHCM has the narrowest range. The frequency range of the VHCM is somewhere between them. Figure 3.7 (b) illustrates that for both inverter topologies the BCM has the lowest rms value of inductor current while the CHCM has the highest rms value of inductor current. The frequency range is reduced at the expense of the increased current near the zero crossing point, which also causes the rms value of I_{Ls} increase and the conduction losses increase.

3.3.3 Power Dissipation Analysis

Although the proposed current modulations realize zero voltage switching during the turn-on period, there are still various losses for the inverter system such as the MOSFETs and the inductor conduction losses, the anti-parallel diodes losses, the MOSFETs turn-off switching losses, and the inductor core losses etc.

3.3.3.1 Conduction Losses

The conduction loss

$$P_{\text{cond}} = I_{\text{rms}}^{2} (R_{\text{on}} + R_{\text{Ls}})$$
(3.16)

$$I_{ms}^{2} = \sum \int_{0}^{toni} (I_{p-} + \frac{I_{p+} - I_{p-}}{t_{oni}} t)^{2} dt + \int_{0}^{t_{offi}} (I_{p+} - \frac{I_{p+} - I_{p-}}{t_{offi}} t)^{2} dt$$
(3.17)

In (3.17), t_{oni} and t_{offi} are calculated by (3.11) and (3.13); R_{on} is the total conduction resistance of MOSFETs; and R_{LS} is the ac resistance of the inductor L_s .

3.3.3.2 Anti-Parallel Diodes Losses



Figure 3. 8 (a) equivalent circuit model for conducting diode (b) turn-off transient for MOSFET

The anti-parallel diode of a MOSFET when passing through a current can be equivalent as a voltage drop u_{D0} connected in series with a resistor R_D as shown in Figure 3.7(a). Turn-off losses in the anti-parallel diode are very small and are normally ignored. Turn-on losses can be calculated by

$$P_{D} = \sum (t_{deadtime} - t_{D})(u_{D} * I_{p + / -} + R_{D} * I_{p + / -}^{2})$$
(3.18)

In (3.18), $t_{deadtime}$ and t_D are shown as Figure 3.3 $t_{deadtime}$ is a given constant, while t_D can be

calculated by (3.10).

3.3.3.3 MOSFETs Turn-Off Loss

During the turn-off period, the MOSFET voltage V_{DS} is rising and current I_D is falling as illustrated in Figure 3.7(b). The MOSFET operates in magnifying region. Thus the capacitance C_{iss} is changing suddenly.

$$P_{Moff} = \sum \frac{1}{2} V_{in}(I_{p+} - I_{p-})(t_{rise} + t_{fall})$$
(3.19)

In (3.19),
$$t_{rise} = \frac{V_{DS}C_{rss}R_G}{V_{plateau}}$$
, $t_{fall} = \frac{V_{DS}C_{rss}R_G}{V_{GS} - V_{plateau}}$. Observing from the MOSFET data sheet.

 C_{rss} is decreasing a lot with the increasing of the voltage V_{DS} . Normally $C_{rss}(I_D*R_{dson}) >> C_{rss}(V_{in})$, to simplify the calculation, assume that $C_{rss} = C_{rss}(I_D*R_{dson})/2$.

3.3.3.4 Inductor Core Losses

As the voltage across the inductor is a frequency-varying, duty cycle-varying waveform, the core losses are very difficult for calculation. Paper [86] proposed a core loss estimation method dealing with these limitations.

$$P_{\text{core}} = \sum \alpha V[(\Delta B^{m}/(2t_{\text{oni}})^{n})t_{\text{oni}} + (\Delta B^{m}/(2t_{\text{offi}})^{n})t_{\text{offi}}]$$
(3.20)

In (3.20), V is the volume of the core. Although α , m and n are constants for each core material, multiple linear regression technique based on core loss data pool is required to obtain them. As the inductor core losses are difficult to calculate under the varying-frequency varying-duty cycle conditions, it is not included in the loss analysis here.


Figure 3. 9 Maximum switching frequency and power losses for different current modulations

Figure 3.9 shows the maximum switching frequency with the power losses for various current modulations. To give a comparison between these current mode controllers, not only are the circuit parameters for the inverter systems the same, but also $(I_{p+}-I_{p-})|_{max}=5A$ is selected as a restrictive condition for all these control schemes. For the half bridge inverter under VHCM control when ΔI decreases to 0.735A VHCM scheme can be simplified to BCM scheme, and when ΔI increases to 2.5A VHCM scheme turns into CHCM scheme. It is obvious to observe from Figure 3.8 that with the increase of ΔI ,the maximum switching frequency decreases, and the power losses increase. Additionally, the full bridge inverter has obviously narrower switching frequency range and fewer power losses than the half bridge inverter under the same current mode controller.

3.3.4 Modeling and Controller Design



Figure 3. 10 Close loop hybrid control diagram



Figure 3. 11 Equivalent circuit of power plant



Figure 3. 12 Simplified block diagram of loop gain

To ensure the ZVS for turn-on switching transitions a close loop controller to restrict the peak inductor current $I_{p+/-}$ is very important, especially when disturbances from the output side or the input side are injected into the inverter system. This requires accurate sensing of the peak inductor current. However, as the switching frequency is varying with time and the highest operation

frequency could go beyond 200kHz, at which frequency the ADC sampling of peak inductor current is too fast for the DSP.

Therefore, a hybrid current control strategy, which combines analog and logic units, is proposed. The diagram is shown in Figure 3.10. Since the inductor current includes both the switching frequency and the line frequency it is hard to measure with a single transformer. However, it can be sensed with a high frequency current transformer and a low frequency current sensor chip which are separately sensed and added from the capacitor and the output side inductor. The DSP takes the tasks of outside PI control (as shown in Figure 3.10) and produces the current reference according to the selected current control scheme.

The analog and logic units implement the current mode control. As the three-phases are decoupled with each other in the three-phase half bridge inverter, the single-phase half bridge controller can be simply extended for the three-phase application. For each phase only two comparators and a D flip-flop are needed to achieve peak current comparisons and produce the switching signals. Each of the discrete components has only several nanoseconds propagation delay. With the hybrid control the overall current control delay does not exceed 250ns.[88]

To analyze the controller design, the equivalent circuit of power plant could be simplified as illustrated in Figure 3.11, where the input voltage is a square signal generated with the bridge. The two voltage levels of the square signal are V_d and $-V_d$ individually, while the time lengths for different values are dependent on the controller.

The close loop gain could be simplified as illustrated in Figure 3.12, where the G_{iv} refers to the power plant illustrated in Figure 3.11; G_{EA} refers to the outside PI control; G_{id} refers to the current comparators; and k_s refers to the proportion value between instantaneous inductor current and line frequency inductor current.

$$\begin{cases} G_{iv} = \frac{R_L}{1 + sC_sR_L} \\ G_{EA} = k_p + \frac{k_i}{s} \\ G_{id} = \frac{V_d - V_o}{L_s} \\ k_s = \frac{1}{2} \end{cases}$$
(3.21)

Like the peak current controller, the current comparators simplify the voltage loop design to a first order system design, which is easy to compensate stable.

3.3.5 Simulation and Experiment Results of Proposed ZVS Technique

3.3.5.1 Simulation Results of Proposed ZVS Technique

Matlab Simulink has been used to simulate the proposed control algorithms. Parameters of the full bridge single-phase inverter simulation system are set as: Input: $250V_{dc}$, Output: $170V_{ac,pk}$, rated power: 150W, 60Hz; L_s=560uH, C_s=1uF. Parameters of the half bridge single-phase inverter simulation system are set as: Input: $420V_{dc}$, Output: $170V_{ac,pk}$, rated power: 150W, 60Hz, L_s=220uH, C_s=1uF.

For application consideration the inverter may provide power to various output loads. When the load is not resistive, DSP is used to get the degree differential between output voltage and output current as analyzed in [89] and a degree adjustment can be made in calculation. Figure 3.13(a-c) illustrates the full bridge inverter waveforms when connecting to a resistive load, inductive load, and capacitive load respectively.



(a)



(c)

(b)

Figure 3. 13 Simulation waveforms for various load for a full bridge inverter:(a)resistive load (b)inductive load (c)capacitive load



(a)

(c)

Figure 3. 14 Simulation waveforms for various load for a half bridge inverter:(a)resistive load (b)inductive load (c)capacitive load



(c)

Figure 3. 15 Simulation waveforms for three different current mode control schemes: (a)BCM (b)CHCM (c)VHCM



(c)

Figure 3. 16 FFT analysis of output voltage for three different current mode control schemes: (a)BCM (b)CHCM (c)VHCM

For the full bridge inverter, as analyzed before, all switches are turned off during zero crossing section of the output voltage to avoid zero switching frequency, and this causes the distortion in the output voltage as shown in Figure 3.13. Especially when connected with an inductive/capacitive load, the distortion is worse than when connected with a resistive load, because the current magnitude of voltage zero crossing point is larger than the minimum $I_{P+/-}$ value under resistive load. On the other side, the half bridge inverter with higher switching frequency does not have that zero crossing distortion as it does not have an all-off period as illustrated in Figure 3.7 (a). The simulation waveforms of the half bridge inverter for various load is shown in

Figure 3.14.

The proposed VHCM and CHCM current control schemes, which mainly aim at reducing the switching frequency, are not necessary for the full bridge inverter, especially when considering the voltage distortion caused by the zero crossing point. Thus a half bridge inverter is selected to apply these current control schemes. Simulation waveforms are illustrated as Figure 3.15. The switching frequency ranges for individual current control schemes are VHCM: 33kHz-160kHz, CHCM: 33kHz-95kHz, and BCM: 30kHz-238kHz. The FFT analysis histograms of the output voltages for the three schemes are illustrated as Figure 3.16. The CHCM has the best THD, while the BCM has the worst THD. The VHCM has a THD between them.

3.3.5.2 Experiment Results of Proposed ZVS Techniques

A 150W single-phase full-bridge inverter prototype has been built and the proposed control scheme has been applied to the prototype. The digital controller is implemented by microchip dspic30f2023. Parameters of the circuit system are set as below:

Input: $250V_{dc}$, Output:117 $V_{ac,rms}$, Rated power: 150W, 60Hz; Switching frequency: 15kHz~41kHz; L_s=561uH, R_s=0.2 Ω , C_s=1uF

Figure 3.17(a) demonstrates an output voltage waveform together with an inductor current waveform; which match the simulation results fairly well. Figure 3.17(b-d) illustrate the key waveforms of the proposed ZVS operation in one switching cycle, which are the same as those in Figure 3.3. It is obvious that before the arrival of the turn-on signal, the drain source voltage across the corresponding MOSFET has already decreased to zero. Therefore the proposed controller can realize ZVS during turn-on transitions.



Figure 3.18 illustrates output voltage and inductor current waveforms when connecting with

(b)

Figure 3. 18 Waveforms of BCM full bridge inverter: (a) capacitive load (b) inductive load

(a)

capacitive load and inductive load individually. Their shapes are similar with the simulation waveforms illustrated in Figure 3.17.

To give a comparison of the proposed soft switching technique, continuous conduction mode (CCM) hard switching control is implemented on the same prototype. The detailed parameters are as follows:



Figure 3. 19 Efficiency waveform of full bridge BCM inverter





(c)

Figure 3. 20 Waveforms of half bridge inverter with different current mode control schemes: (a)BCM (b)CHCM (c)VHCM

Input voltage: $250V_{dc}$, Output voltage: $170V_{ac,pk}$, Rated power:150W, 60Hz; Switching frequency: 20kHz; Ls=2.61mH, Rs= 0.6Ω , Cs=1uF

Figure 3.19 shows the efficiency comparison between the full bridge BCM and hard-switching technique for full resistive load. The peak efficiency of the BCM technique can reach up to 98.5%, which is over 1.5% higher than the peak efficiency of the hard switching technique. All the efficiency was measured by a PZ4000 power analyzer. The measured efficiency does not include driving power loss.

The VHCM and CHCM current control schemes are aimed at decreasing switching frequency in order to decrease switching loss and increase efficiency. As illustrated in Figure 3.7 (a), the half bridge inverter has a much wider switching frequency range than the full bridge inverter. Therefore a half bridge inverter prototype was built to implement the three different current control schemes. The detailed parameters of the inverter are as follows:

Input voltage: $420V_{dc}$, Output voltage: $170V_{ac,pk}$, Rated power: 150W, 60Hz; Ls=220uH, Rs= 0.3Ω , Cs=2.2uF

	Frequency	THD(%)	Efficiency(%)	$I_{Ls,rms}(A)$
BCM	33kHz~325kHz	2.4%	97.5%	1.56
VHCM	33kHz~190kHz	1.9%	97.4%	1.62
СНСМ	33kHz~95kHz	1.4%	97.2%	1.8

Table 3. 1 Comparison of three different comparison modes

As for the CHCM and VHCM, different current bands can be applied on the prototype, and they may all have various affections on the output efficiency. To give a comparison between these current mode controllers, $I_{p+}-I_{p-}|_{max}=5A$ is selected as a restrictive condition for all control modes. Additionally, to separate the VHCM scheme away from the CHCM scheme and the BCM scheme, $I_{o,peak}-I^*=\Delta I$ is set as an additional restriction for the VHCM scheme.(This makes the VHCM scheme directly in the middle of the CHCM scheme and the BCM scheme) The output voltage and inductor current waveforms for three current mode controls are illustrated as in Figure 3.20 and the efficiency and frequency ranges are listed in Table 3.1.

Figure 3.20 illustrates experimental waveforms of the three current mode control schemes. They are the same as the simulation waveforms illustrated by Figure 3.15.

3.4 Comparison Research of ARCP with Proposed ZVS Technique

A resonant tank of ARCP topologies consists of one resonant inductor, two bi-directional switches and two resonant capacitors, which could be added to a hard switching inverter without modifying the basic main circuit. During the commutation transitions, through the resonant tank zero voltage condition could be provided to the main devices and zero current condition could be provided to the auxiliary switches on both turn on and turn off period. Moreover, no extra voltage or current stresses could be added to the main switches. Thus high efficiency could be achieved under high switching frequency.

3.4.1 Operation Principle of ARCP

To give a comparison with the proposed ZVS, a conventional single phase ARCP is provided here. The topology of the ARCP is illustrated as in Figure 3.21, where S_1 and S_2 operate at high switching frequency, while S_3 , S_4 operate at line frequency.



Figure 3. 21 Simplified ARCP single phase inverter topology

The auxiliary switches operate during the commutation periods of the main switches. When S_2 is about to open and S_1 is about to close, the operation principle is illustrated as in Figure 3.22 and Figure 3.23.



<stage 3>

Figure 3. 22 Operation stages for the full bridge single-phase ARCP inverter

Stage 1 [t_0 - t_1]: During this stage, the auxiliary switch S_{a1} and main switch S_2 are closed. The energy stored on capacitor C_2 is charging inductor L_r through S_{a1} , D_{a2} , D_{s2} , and S_2 , and inductor

current is increasing linearly as illustrated in Figure 3.23.



$$i_{Lr}(t) = \frac{V_{in}}{2L_r} t$$
(3.22)

Figure 3. 23 Key waveforms of ARCP inverter

Stage 2 [t_1 - t_2]: During this stage, the main switch S_2 is opened. The resonant circuit is built up with components C_1 , C_2 , L_r , C_{r1} and C_{r2} . When the voltage across C_{r1} achieves zero, the diode D_1 is turned on automatically, which creates the ZVS condition for the turning on of main switch S_1 .

$$\begin{cases} V_{Cr2}(t) = k_1 \sin(\omega_0 t) - \frac{V_{in}}{2} \cos(\omega_0 t) + \frac{V_{in}}{2} \\ V_{Cr1}(t) = V_{in} - V_{Cr2}(t) \\ i_{Lr}(t) = 2C_r \omega_0 [k_1 \cos(\omega_0 t) + \frac{V_{in}}{2} \sin(\omega_0 t)] + I_0 \end{cases}$$
(3.23)

Where $\omega_{0} = \sqrt{2L_{r}C_{r}}$, $k_{1} = \frac{i_{Lr}(t_{1}) - I_{o}}{2C_{r}\omega_{o}}$

Stage 3 [t2-t3]: During this stage, the main switch S_1 is closed. The voltage on C_1 begins to discharge inductor current i_{Lr} through S_{a1} , D_{a2} , D_{s1} , and S_1 as illustrated in Figure 3.22<stage 3>. When the inductor current is decreased to zero, the diode Da2 would block the current on the

negative direction, thus ZCS would be generated for the turn off of auxiliary switch S_{a1} . Then S_{a1} would be closed.

$$i_{Lr}(t) = i_{Lr}(t_2) - \frac{V_{in}}{2L_r}t$$
(3.24)

For the commutation of S_1 open and S_2 open, the auxiliary circuit operates the same way as discussed before.

3.4.2 Experiment Results of ARCP Technique

The experiment waveforms of the ARCP are illustrated as in Figure 3.24. It operates under the ZVS the same way as described in Figure 3.23.



(c)

Figure 3. 24 Experiment waveforms of the ARCP: (a) Driver signals for main and auxiliary switches (b) Resonant inductor current with a main switch driver signal (c) The driver signal and voltage across the MOSFET



Figure 3. 25 Efficiency waveform of full bridge single phase ARCP inverter

The efficiency waveform of the single phase ARCP under different power is illustrated as in Figure 3.25. Compared with the proposed single phase BCM efficiency illustrated in Figure 3.19, the ARCP has much lower efficiency when the load is light. Moreover, the resonant circuit requires much more components compared with the BCM inverter, thus the cost is high.

3.5 Summary

In this chapter, the DC/AC inverters can be briefly classified into three groups: VSI, CSI, and ZSI. As in chapter two, the LLC converter is selected as the DC/DC stage of double stage micro-inverter, the high voltage gain and isolation requirements are already satisfied. Thus the advantages of CSI and ZSI in voltage rising is no longer attractive. Moreover, the VSI having various soft switching techniques available to improve the efficiency and power density is selected as the topology of DC/AC inverter stage.

A review of the soft switching technologies on inverters is provided. Although all of them can realize soft switching, they require additional components as well. Thus a novel kind of ZVS technique without auxiliary components is proposed in this chapter, which is called BCM inverter. According to the proposed technique, the body capacitors of the main MOSFETs and the output linear inductor are applied together to form a resonant circuit. The inductor current is intentionally operated in bi-direction within a switching cycle to generate ZVS conditions during commutations. The operation principle is analyzed carefully with three different current modulation designs provided. The power dissipation is calculated to compare these current modulations. Simulation and experiment results verify the feasibility of the proposed soft switching technique.

To give a comparison of the proposed ZVS technique with the conventional ZVS techniques, an ARCP prototype with advantages in turn-on and turn-off soft switching on all switches is provided. Experiment results show that the proposed BCM inverter has a better efficiency.

CHAPTER FOUR: ENERGY STORAGE INTEGRATED WITH THE MICRO-INVERTER/UTILITY INTERACTIVE SYSTEMS

4.1 The Significance of Energy Storage Integrated PV Power System

PV modules and arrays produce DC power, and the simplest PV system configuration is connecting load directly to the PV array. Due to various application requirements, electrical loads are varying widely in characteristics. Some of them require DC or AC power, while others may operate from either, such as resistive loads or universal motors. Considering the application requirements depending on load usage, load type, insolation, auxiliary power sources and many other factors, different components could be added in the simplest PV system to increase the complexity and configure different PV systems. For example, residential system, traffic light system, street lighting system, water pumping system, car charging system, solar farm system and so on. Some of them operate with the utility grid connection; some operate independently; while others operate appropriately in both situations.



Figure 4. 1 PV system configurations

There are currently some difficulties addressed to the PV systems, especially with the stand alone configuration.

Firstly, due the nonlinear characteristic VI curves of PV panel, which is varying with temperature and irradiance, the PV energy is by nature intermittent and unpredictable.

Secondly, any power-generating system, for example a PV system, faces the problem of matching energy supply with demand. Demand can fluctuate considerably and changes occur within minutes or seconds.

To balance the requirements from fluctuated load and intermittent source, energy storage is introduced into the PV system. The configuration could be illustrated in Figure 4.1.



Figure 4. 2 Configuration of PV system with energy storage

When the maximum power generated by PV panels is more than load demand, the excess energy would be flowed and stored in energy storage for later usage. When the load is over the maximum power supplied from the PV panels, energy storage releases power to the loads.

Energy Storage performs two functions to increase the consistency, stability and reliability of PV system.

- Short term power balancing
- Long term power management

Short term power balancing deals with the intermittent and unpredictable PV power, which requires the energy storage system has fast dynamic response, high accuracy, symmetrical (charge/discharge) power handling capability, long cycling life, and low cost. Literature [97-99] propose different topologies and controllers for the short term power balancing requirement.

Longer term energy management deals with the shifting load with relatively slow charging/discharging time over a long duration, which requires high energy storage capacity, high conversion efficiency, and low cost. For example, the street lighting system discussed in [99, 100] deals with the long term power management, which charges the battery during daytime, and releases energy at night.

As a vital part of integrating and stabilizing PV systems, energy storage techniques have many types. Considering the current primarily used and researched techniques, they could be classified into seven groups characterized by the stored energy forms.

- Compressed Air Energy Storage (CAES)
- Pumped Hydro Storage (PHS)
- Superconducting Magnetic Energy Storage (SMES)
- Super-capacitors and capacitors
- Flywheel
- Fuel cell
- Battery



Figure 4. 3 Storage classification considering the functions [101]

With consideration of functions [101], these storage techniques can be classified as illustrated in Figure 4.3. Among all these energy storage techniques, batteries, particularly lead-acid types, with the cheapest price and mature technology, are by far the most common means used for energy storage in PV systems.



(c)

Figure 4. 4 Architectures of battery integrated PV systems: (a) PV panel connection type (b) DC bus connection type (c) AC bus connection type

4.2 PV System Architecture with Batteries

Based on the differences of the batteries' locations, the architectures of battery integrated PV systems could be classified into three groups as illustrated in Figure 4.4.

4.2.1 PV Panel Connection Type

This type is illustrated in Figure 4.4 (a), where the batteries are directly or indirectly connected with the PV panel. The dashed DC/DC converter is designed to charge/discharge the batteries, which is avoidable in some PV systems. Literatures [102, 103]refer to this kind of architectures.

4.2.2 DC Bus Connection Type

This type is illustrated in Figure 4.4 (b), where the batteries are connected with DC bus lines. The dashed DC/DC converter refers to charger/discharger for the batteries, which is avoidable in some PV systems. Literatures [104-106] refer to this kind of architectures.

4.4.3 AC Bus Connection Type

This type is illustrated in Figure 4.4 (c), where the batteries are connected with the ac lines with a PFC converter. The ac lines could be connected with utility grid as shown in Figure 4.4 (c), and could also be diesel generator, wind turbines or any other electric source to improve load availability when PV energy is not available, as illustrated in Figure 4.5 PFC is unavoidable as AC power is required to convert to DC power for battery storage. Literature [107-110] refers to architecture with batteries connected with ac lines.

Comparing those three architectures together, the PV panel connection type connects batteries at the PV panel side. When charging the batteries from the PV panel, the charging circuit is the shortest, thus the efficiency is the best. However, when charging the batteries from the grid side, the charging circuit is much longer, and efficiency is reduced. Moreover, a bidirectional DC/DC converter and DC/AC inverter are required, which would increase the system complexity. Thus commonly for PV panel connection architecture the batteries are charged from the PV panel and discharged to the load or grid. The architecture is mostly suitable for low cost and low power systems.

The DC bus connection type PV system connects DC bus lines directly with batteries or indirectly with the bi-directional DC/DC converter. The indirect connection would reduce the system efficiency since two-level conversion is used for battery charging. While the direct connection would affect battery life-time and utilization sine the batteries involved in energy conversion.

The AC line connection type PV system could charge the batteries from both the PV panel side and the grid side. Under the application of hybrid systems, the batteries can be charged from various electric sources as illustrated in Figure 4.5. Thus AC line connection provides a convenient and reliable auxiliary energy for the load with small battery capacity. And it is suitable for the application of PV involved uninterruptible power supply (UPS), unified power quality controller (UPQC), and so on.

To improve the system efficiency and optimize the batteries' charging and discharging progress, sometimes different architecture types are combined. For example, literature [111] combines the PV panel connection type and DC bus connection type. Literature [108] combines the AC bus connection with DC bus connection type.



Figure 4. 5 Architecture of battery integrated hybrid system

4.3 PFC Introduction for Energy Storage Systems

For the application of AC bus connection type PV system architecture, PFC plays an important role as rectifier and charger for the energy storage batteries.

Because of the ac side connection, which could absorb power from the utility, conventional battery chargers are termed to be unidirectional. Compared with early designed battery chargers, which exhibit a poor power factor due to the high current distortion, and large ripple in battery charging current with a bulky inductor, the newly developed PFCs with carefully designed current shaping and phasing have achieved close to power factor 1, better current quality with higher efficiency and lower THD.



Figure 4. 6 Topology-based classification of PFC

In recent decades, many PFC topologies and control approaches have been proposed. For the classification of these PFC topologies, every basic DC-DC converter topologies (Buck, Boost, Buck~Boost, Flyback, Sepic, Cuk, push-pull), can be used to build up corresponding DC/AC PFC circuits. Moreover, the combinations between them such as Buck-Flyback and Boost-Flyback can also be applied as PFC circuit. Besides, multilevel AC/DC converters could be applied as PFC topologies to reduce the harmonics and THD of the input ac current [112-117]. Based on these fundamental circuits, considering the bridge type (full bridge, half bridge or diode bridge), isolation requirements (with or without transformer), and current flow directions (unidirectional or bidirectional), hundreds of PFC topologies have been derived in previous literatures. [112-117] The topology-based classification can be illustrated as in Figure 4.6.

The most common approach to power factor correction (PFC) is illustrated in Figure 4.7 (a), which typically consists of a pre-regulator for PFC stage, cascaded with a DC/DC converter stage.

Each of the switching converter stages requires a separate controller, which increases the complexity and cost.

Single stage PFC converters that integrate input current shaping, isolation and DC/DC functions in the same stage are attractive for low power area applications. The block diagram of a typical single-stage PFC is illustrated in Figure 4.7 (b). Because of shared controller and active switches, the single stage PFC converters have advantages in cost, size, efficiency, and reliability compared with double stage PFC converters.



(a)

(b)

Figure 4. 7 Conventional two-stage PFC (a) and single-stage PFC (b)

4.4 Digital Control of Biflyback PFC Topology

In recent years, many literatures about single stage PFC topologies have been published. Considering the electric isolation requirement, the flyback single stage PFC converters due to their simple circuit configuration and low component counts, have become attractive candidates for single stage PFC applications. The conventional topology of flyback PFC is illustrated in Figure 4.8. The circuit consists of an uncontrolled rectifier bridge cascaded with a flyback converter. The flyback PFC converter has two operation modes: one mode is when the primary inductor of transformer is shorted and the energy is stored in the transformer. The other mode is when the magnetic energy stored in the transformer flows through the diode into the load. The input current can be made to be fully discontinuous, bounded by a sinusoidal envelop to generate a good current shaping.



Figure 4. 9 Discontinuous input current waveforms of Flyback PFC

However, this topology this topology suffers from high voltage and current stresses which limit its application. As illustrated in Figure 4.8, the voltage stress across the switch can be expressed as equation (4.1).

$$\mathbf{V}_{s} = \mathbf{V}_{in, pk} + \mathbf{n} \cdot \mathbf{V}_{o} \tag{4.1}$$

Moreover, because of the discontinuous input current waveforms illustrated in Figure 4.9, the peak current stress on the switch is much larger than the analogous sinusoidal input current.

Single stage Biflyback PFC that combines the advantages of single stage PFC and flyback topology, with its advantages of low intermediate bus voltage and current stresses [118], is adopted in this chapter. The topology of Biflyback PFC is shown as Figure 4. 10.

The circuit consists of two flyback circuits connected together with shared switch S and output circuit. The first flyback is constructed with a rectifier bridge, diode D, transformer T_1 , switch S and diode D₁. And the second flyback circuit is constructed with bus capacitor C_s, transformer T₂, and diode D₂. The operations of these two flyback are intermingled with each other, and play different function roles in the PFC. Generally speaking, the first flyback transformer T₁ in the PFC cell operates in DCM to obtain high power factor, while the secondary flyback transformer T₂ in DC/DC conversion cell operates in CCM to reduce the current stress and achieve tight output voltage regulation.



Figure 4. 10 Biflyback PFC topology

4.4.1 Operation Principle

To simplify the analysis, the following assumptions are made first:

- No leakage inductance or resistance in two transformers
- V_{Cs} (voltage across storage capacitor) and output V_o are constant
- All switch components are ideal
- Input voltage is constant during each switching cycle



(c)

Figure 4. 11 Biflyback PFC equivalent circuit under different periods: (a) Equivalent circuit during S ON period (b) Equivalent circuit during S OFF period under flybcak mode (c) Equivalent circuit during S OFF period under boost mode



(b)

(a)

Figure 4. 12 Operation key waveforms: (a) under flyback mode (b) under boost mode

When switch S is ON, the equivalent circuit of Figure 4.11 is shown as Figure 4.12(a). The primary magnetic inductor L_1 of transformer T_1 is charged by the rectifier bridge, while the primary magnetic inductor L_2 of transformer T_2 is charged by capacitor C_s . The secondary side current of both transformers are blocked individually by diodes D_1 and D_2 . Thus the load power is supplied by capacitor C_o independently. The key waveforms of operation of this period are illustrated as Figure 4.12 (a) and (b) in interval $[t_0 \sim t_1]$.

The state equations of this period can be expressed as (4.2).

$$\begin{cases} L_1 \frac{di_{L_1}}{dt} = |V_{in}| \\ L_2 \frac{di_{L_2}}{dt} = |V_{C_s}| \\ C_s \frac{dV_{C_s}}{dt} = -I_o \end{cases}$$

$$(4.2)$$

When switch S is off, the operation has two working modes depending on the instantaneous value of input voltage. The operation modes over one line cycle are illustrated as in Figure 4.13.



Figure 4. 13 Operation modes during one line cycle

The boundary time for two modes can be calculated with equation (4.3).

$$t_{x} = \frac{1}{\omega} \sin^{-1} \left(\frac{V_{Cs} + n_{2}V_{o} - n_{1}V_{o}}{V_{in, pk}} \right)$$
(4.3)

Where ω refers to the angular frequency of input voltage, and V_{in,pk} refers to the amplitude of input voltage.

4.4.1.1 Flyback Mode

When the rectified voltage $|V_{in}|$ is smaller than voltage $V_{Cs}+n_2V_o-n_1V_o$, the input current could be blocked by diode D. The magnetic energy stored in transformers T_1 and T_2 during ON period would transfer to electric energy at the secondary sides and flow to the output load through diode D₁ and D₂ individually. Thus both T₁ and T₂ operate as flyback transformers. The equivalent circuit of this mode is illustrated as in Figure 4.11(b). The key waveforms of operation of this period are illustrated as interval $[t_1 \sim t_3]$ in Figure 4.12 (a).

In interval $[t_1 \sim t_2]$, the state equations of this period can be expressed as (4.4).

$$\begin{cases} \frac{L_{1}}{n_{1}^{2}} \frac{di_{D1}}{dt} = |V_{0}| \\ \frac{L_{2}}{n_{2}^{2}} \frac{di_{D2}}{dt} = |V_{0}| \\ C_{s} \frac{dV_{Cs}}{dt} = i_{D1} + i_{D2} - I_{0} \end{cases}$$
(4.4)

When the secondary current of transformer T_1 has decreased to zero, the diode D1 will block its increasing in the negative direction. And the secondary current of T2 will keep decreasing until the switching cycle ends. This period is illustrated as interval $[t_2 \sim t_3]$ in Figure 4.12(a).

4.4.1.2 Boost Mode

When the rectified voltage $|V_{in}|$ is larger than voltage $V_{Cs}+n_2V_o-n_1V_o$, the input current flows through diode D to charge capacitor C_s. Because of this current, the secondary side current of T₁ is blocked by diode D₁. Thus the primary winding of the first transformer T1 operates as a boost inductor. Energy stored in T₁ would divide into two parts. One part flows through L₂ to charge intermediate bus capacitor C_s and the other transfers through T₂ to the output side. Whereas T₂ operates as flyback transformer, and magnetic energy stored during ON period would transfer to electric energy and flow to the output load through diode D₂. As the voltage across L₁ is negative, current in this boost inductor would decrease to zero, and diode D would prevent the current from going negative. The equivalent circuit of this mode is illustrated in Figure 4.11(c). The key waveforms of operation of this period are illustrated as interval [t₁~t₃] in Figure 4.12 (b). The state equations of this period can be expressed as (4.5).

$$\begin{cases} L_{1} \frac{di_{L1}}{dt} = |V_{in}| - V_{Cs} - n_{2}V_{o} \\ \frac{L_{2}}{n_{2}^{2}} \frac{d(i_{D2} - i_{L1}/n_{1})}{dt} = |V_{o}| \\ C_{s} \frac{dV_{Cs}}{dt} = i_{D2} - I_{o} \end{cases}$$
(4.5)

4.4.2 DSP Control Design Analysis

In the controller design of Biflyback PFC converter, as discussed in [118], the conventional analog control strategy is illustrated in Figure 4.6.



Figure 4. 14 Conventional control strategy of Biflyback PFC

The output voltage V_o is sensed and compared with a reference value V_{ref} , then with PI regulation a reference current value is generated. With triangle carrier frequency determining the switching frequency, the duty cycle is determined by the comparator between the reference current generated with voltage loop and the peak current sensed in switch S₁. Compared with conventional flyback PFC, where the reference current is generated by multiplying voltage PI regulator output with the quasi-sinusoidal voltage after the diode bridge for current shaping function, the controller shown in Figure 4.14 depends completely on the automatic PFC effect of DCM operation of T₁. The controller focuses on achieving tight output voltage regulation and thusly could not realize good effect in input current shaping.

Analysis is carried out in this chapter to provide further research on current shaping. The input current is the same as the current in the primary side of transformer T_1 .

4.4.2.1 Flyback mode

Based on the analysis in the last section, as illustrated in Figure 4.12 (a), the average input current of a switch cycle is calculated with equation (4.6)

$$< i_{in}(t) > T_{s} = < i_{L1}(t) > T_{s} = \frac{1}{T_{s}} \left[\int_{0}^{DT_{s}} i_{L1}(t) dt + \int_{DT_{s}}^{T_{s}} 0 dt \right]$$

= $\frac{1}{2} \left(\frac{|V_{in}|}{L_{1}} DT_{s} \right) D = \frac{T_{s}}{2L_{1}} D^{2} |V_{in}|$
 $\propto |V_{in}|$ (4.6)

4.4.4.2 Boost mode

As illustrated in Figure 4.12(b), the current i_{L1} decreases to zero at time t_2 , which can be calculated with equation (4.7)

$$i_{L1}(t_{2}) = 0 \Longrightarrow i_{L1}(t_{2}) = \frac{|V_{in}| - (V_{cs} + n_{2}V_{o})}{L_{1}}(t_{2} - DT_{s}) + i_{L1}(DT_{s}) = 0$$

$$\implies t_{2} = \frac{V_{cs} + n_{2}V_{o}}{V_{cs} + n_{2}V_{o} - |V_{in}|} DT_{s}$$
(4.7)

Average input current of a switch cycle is calculated as equation (4.8)

$$<\dot{i}_{in}(t) > T_{s} = <\dot{i}_{L1}(t) > T_{s} = \frac{1}{T_{s}} \int_{0}^{t^{2}} \dot{i}_{L1}(t) dt$$

$$= \frac{1}{2} \left(\frac{|V_{in}|}{L_{1}} DT_{s} \right) \frac{t_{2}}{T_{s}} = \frac{T_{s}}{2L_{1}} D^{2} \frac{V_{cs} + n_{2}V_{o}}{V_{cs} + n_{2}V_{o} - |V_{in}|} |V_{in}|$$

$$\propto |V_{in}|$$
(4.8)

It can be seen from (4.8) that in order to keep a linear relationship between average input

current and input voltage, $D^2 \frac{V_{cs} + n_2 V_o}{V_{cs} + n_2 V_o - |V_{in}|}$ should be kept as constant, which means D

should have a linear relationship with $\sqrt{\frac{V_{cs} + n_2 V_o - |V_{in}|}{V_{cs} + n_2 V_o}}$ as shown in (4.9).

$$D = k \sqrt{\frac{V_{cs} + n_2 V_o - |V_{in}|}{V_{cs} + n_2 V_o}}$$
(4.9)

If k is the constant value of the duty cycle in the flyback mode, then the duty cycle of

 $k \sqrt{\frac{V_{cs} + n_2 V_o - \mid V_{in} \mid}{V_{cs} + n_2 V_o}} \ \, \text{in boost mode can keep the same linear relationship between input current}$

and input voltage as in flyback mode.

Power factor correction shapes the input current, which ideally emulate a pure resistor load to the power network.

$$< i_{in}(t) > T_s = \frac{1}{R_{eq}} |V_{in}|$$
 (4.10)

 R_{eq} can be gotten from energy balance

$$P_{in} = P_o = \frac{V_{in.ms}^2}{R_{eq}}$$
(4.11)

Combining (4.10) and (4.11) with (4.6) and (4.9), the duty cycle that can guarantee input current shaping is shown in (4.12)

$$D = \begin{cases} \sqrt{\frac{2P_{o}L_{1}}{T_{s}V_{in.ms}^{2}}} & |V_{in}| < V_{cs} + n_{2}V_{o} - n_{1}V_{o} \\ \\ \sqrt{\frac{2P_{o}L_{1}(V_{cs} + n_{2}V_{o} - |V_{in}|)}{T_{s}V_{in.ms}^{2}(V_{cs} + n_{2}V_{o})}} & |V_{in}| > V_{cs} + n_{2}V_{o} - n_{1}V_{o} \end{cases}$$

$$(4.12)$$

The derived expression of D in equation (4.9) is implemented in the digital controller in order to calculate a required D value that assures power factor correction in both flyback and boost modes. The output of D calculator block is multiplied with the output of the voltage loop PI controller, to give out a finial PWM signal controlling the switch S_1 shown as Figure 4.15.

In Figure 4.15, the final duty cycle signal given into the PWM module is generated by multiplying D calculator together with PI controller of voltage loop. It could be comprehended as follows: During practical usage, output power P_0 is always changing. PI controller gives the duty cycle that is required by output power P_0 and reference voltage V_{ref} , while D calculator gives the weights of two different working modes in one line cycle to adjust the duty cycle produced by the PI controller and obtain a better power factor. As equation (4.12) is only used for producing the
adjusting weights of different working modes, P_o can be carried out from (4.12) and given into the PI controller to produce the duty cycle. As the PI controller is flexible and stable for various output power, the control strategy should also work during different output power.

In the conventional control strategy of biflyback PFC illustrated in Figure 4.6, the current sensing of switch S_1 is required, which increases the circuit complexity.



Figure 4. 15 DSP control strategy of biflyback PFC

The digital controller illustrated in Figure 4.15 achieves output voltage and line current regulations by means of adaptive digital algorithm to optimize the current and voltage loops within the line cycle and without input current sampling.

4.4.3 Steady State Analysis

When the whole biflyback system reaches a steady state, output voltage V_0 is supposed to reach a constant value. The average current in L_2 of a line cycle must keep a constant value, thus the average duty cycle of a line cycle can be given as:

$$< D > T = \frac{n_2 V_o}{< V_{cs} > T + n_2 V_o}$$
 (4.13)

From equation (4.12) and Figure 4.7, it is obvious to see that the real duty cycle can not be always kept as constant as the average duty cycle shown in equation (4.13). It is changing around

the average duty cycle. If $D < \frac{n_2 V_o}{V_{cs} + n_2 V_o}$, it is possible that T_2 operate under DCM. During boost mode, if current in L_2 reaches zero before current in L_1 reaches zero, secondary inductance of T_2 and capacitance of D_2 would compose an oscillating circuit, which would prevent current in L_1 from decreasing. And T_1 may enter CCM mode, which will break the deduction presumption of equation (4.12). However if current in L_2 reaches zero after current in L_1 reached zero, there will be no affection on T_1 and deduction of equation (4.12). Thus to ensure T_1 works under DCM during boost mode, it is very important to keep

$$\frac{DT_{s} |V_{in}|}{n_{2}V_{o} + V_{cs} - |V_{in}|} < \frac{DT_{s}V_{cs}}{n_{2}V_{o}} \Longrightarrow (V_{cs} - |V_{in}|)(n_{2}V_{o} + V_{cs}) > 0 \Longrightarrow V_{cs} > |V_{in}|$$
(4.14)

$$\frac{DT_{s} |V_{in}|}{n_{2}V_{o} + V_{cs} - |V_{in}|} < (1 - D)T_{s} \Longrightarrow D < \frac{n_{2}V_{o} + V_{cs} - |V_{in}|}{n_{2}V_{o} + V_{cs}}$$
(4.15)

To keep T₁ works under DCM during flyback mode:

$$\frac{DT_{s} |V_{in}|}{n_{1}V_{o}} < (1-D)T_{s} \Longrightarrow D < \frac{n_{1}V_{o}}{n_{1}V_{o} + |V_{in}|}$$

$$(4.16)$$

Suppose t_x is the mode boundary which divides the flyback mode and boost mode, for power balance

$$\frac{T}{4}P_{o} = \int_{0}^{t_{x}} < i_{in}(t) >_{T_{s}} |V_{in}| dt + \int_{t_{x}}^{T} < i_{in}(t) >_{T_{s}} |V_{in}| dt$$
(4.17)

Take equation (4.6) and (4.8) into (4.17)

$$\frac{T}{4}P_{o} = \int_{0}^{t_{x}} \frac{D^{2}T_{s}V_{in}^{2}}{2L_{1}} dt + \int_{t_{x}}^{\frac{T}{4}} \frac{D^{2}T_{s}V_{in}^{2}}{2L_{1}} \frac{V_{cs} + n_{2}V_{o}}{V_{cs} + n_{2}V_{o} - |V_{in}|} dt$$
(4.18)

$$\frac{\partial P_{o}}{\partial t_{x}} = -\frac{2D \left| t_{x}^{2} T_{s} \right|}{TL_{1}} \frac{V_{in, peak}^{3} \sin^{3}(\omega \omega)}{V_{cs} + n_{2} V_{o} - V_{in, peak} \sin \omega i_{x}} < 0$$

$$(4.19)$$

$$\frac{\partial P_{o}}{\partial V_{cs}} = \frac{\partial P_{o}}{\partial t_{x}} \frac{\partial t_{x}}{\partial V_{cs}} < 0$$
(4.20)

It is obvious to see from equation (4.20) that with the increasing of output power P_0 , the

intermediate capacitor voltage V_{Cs} will tend to decrease. With equation (4.14), we know that output power has a maximum limit with any fixed system and fixed input voltage to keep T_1 operates under DCM. As duty cycle is keep changing every duty cycle, and expression of D given by equation (4.12) is deduced from power balance, it cannot be combined with equation (4.18) which is also deduced from power balance to calculate and set up system parameters. But if the duty cycle is assumed to be constant expressed as equation (4.13), when input voltage V_{in} is given, output power P_o , output voltage V_o and intermediate capacitor voltage V_{Cs} could be calculated based on (4.18) to give a direction in the whole parameter design.

4.4.4 Simulation and Experiment Results

A simulation prototype is built up using Matlab Simulink to test the proposed control algorithm. Parameters of simulation system are set as below:

Input: 110Vac, Output: 20Vdc @100W, Switching frequency: 100kHz

The main components: Intermediate capacitor $C_s = 150 \mu F$

 T_1 primary inductance $L_1 = 90 \text{uH}$, turn ratio $n_1 = 6$

 T_2 primary inductance $L_2 = 600 \text{uH}$, turn ratio $n_2 = 3.5$



Figure 4. 16 Waveforms of input voltage and input current under Vin,rms=110V, and Po=30W



(a)



Figure 4. 17 Waveforms under Vin,rms=110V, and Po=100W : (a) Input voltage and input current (b) Duty cycle (c)I_{L1}



Figure 4. 18 Waveforms I_{L1} under Vin,rms=85V, and Po=100W

The simulation waveforms are illustrated as Figure 4.16~Figure 4.18.

One prototype with topology shown as Figure 4.10 is built up and tested in practice. The design parameters, tested voltage range and power range are

Input: 85~135Vac, Output: 20Vdc @20~100W, Switching frequency: 100kHz

The main components: Intermediate capacitor $C_s = 150 \mu F$

 T_1 primary inductance $L_1 = 90 \text{uH}$, turn ratio $n_1 = 5$

 T_2 primary inductance $L_2 = 600 \text{uH}$, turn ratio $n_2 = 3$



Figure 4. 19 Primary side current of T_1 and duty cycle waveforms @100W with 110V input Top:duty cycle(0.2/div) Bottom: current (2A/div) Timebase: 2.00ms/div

As output voltage is fixed to be 20V, with output current increasing from 1A to 5A, output

power is increasing from 20W to 100W. Input current and duty cycle waveforms at 100W output power with 110V input voltage are shown as Figure 4.19. The waveforms have similar shape as in simulation (shown as Figure 4.17(a) and (b)).



Figure 4. 20 Primary side current of T₁ @100W with 85V input voltage

Power factor values at different input voltage and output power are read directly from source machine, which is illustrated as in Table 4.1.

$I_{in}(A)$ $V_{in}(V)$	1	2	3	4	5
85	98.3	98.5	98.7	98.1	94.5
110	99.4	98.1	99.2	98.2	97.3
135	98.7	99.1	99.3	98.7	97.4

Table 4. 1 Power factor values under various input voltage and output power

Power factor drops suddenly at 100W with 85V input voltage is because the current in L_1 enters CCM zone at peak input voltage, as illustrated in Figure 4.20.

4.5 Snubber Cell Design for Low Power PFC

In the single stage PFC converters, for the requirement of isolation, a transformer is usually cascaded with a DC/DC converter. The leakage inductor of the transformer would cause a high voltage spike on the switch during the turning off periods. This voltage spike increases voltage stress on the switching device extensively, which would increase switching losses. With higher

voltage duration switch selection conduction losses would increase as well. To reduce the voltage spike, a snubber circuit design is necessary.

In recent years, many soft switching techniques and snubber techniques have been proposed for PFC converter [119-121]. However, few of them include both functions in one cell. In this section, a new snubber cell combining soft switching technique with snubber technique is proposed, moreover this snubber cell can be implemented generally to all isolated single-stage PFC with a boost type input shaper. Besides these topology advantages, the auxiliary switch and the main switch share the same PWM signal which also simplify the control scheme. Operation principle of the soft switching technique is analyzed in detail, and parameters design is discussed theoretically.





Figure 4. 21 (a)proposed snubber cell, (b)proposed snubber circuit for Biflyback PFC converter, (c)proposed snubber circuit for BIFRED PFC converter

Figure 4.21 presents the new active snubber cell and its applications in both Biflyback and BIFRED topologies as examples. The main switch S_1 and the auxiliary switch S_r share the same PWM signal. To simplify the operation analysis, assume that the capacitor C_s is large enough; therefore the voltage across this capacitor can be represented as a constant value V_{Cs} . Take the Biflyback topology as an example to analyze the operation principles of the snubber cell. Assume that the whole PFC converter system has achieved a steady status. Operation of the snubber cell can be divided into three stages as illustrated in Figure 4.21. The detailed analysis follows.



(c)

Figure 4. 22 various operation stages during one switching cycle: (a) <stage 1>, (b) <stage 2>, (c) <stage 3>

Stage 1[t_0 - t_1]: As illustrated in Figure 4.21 (a), during this stage both switches S₁ and S_r are off. Since the Biflyback PFC converter has two operation modes: boost mode and flyback mode; if the converter operates under boost mode, leakage current of the transformer T₁ flows through the diode D_{r1} to charge the capacitor C_r, otherwise the converter operates under flyback mode, leakage currents of both transformers flow through D_{r1} to charge C_{r1}. The diode D_{r1} and D_{r3} are both off since no currents flow through them. The key waveforms of this stage are illustrated as Figure 4.14.



Figure 4. 23 Key waveforms of snubber cell

Stage 2[t₁-t₂]: Both switches S_1 and S_r are turned on during this period whereas the diodes D_{r1} and D_{r3} are blocked by the reverse voltage across them individually. Energy stored in the capacitor C_r during stage 1 are discharged through the inductor L_r and the diode D_{r2} to charge C_s . When the voltage V_{Cr} is larger than V_{Cs} , current i_{Lr} increases, and when the voltage V_{Cr} drops below V_{Cs} , i_{Lr} decreases. During this period, diode D_{r1} would prevent V_{Cr} from going negative, and D_{r2} would prevent i_{Lr} from going negative.

Stage $3[t_2-t_3]$: If i_{Lr} reaches zero before the turning off of switches, stage 3 would be illustrated as in Figure 23 (a), i_{Lr} and V_{Cr} would keep zero until the next turning on signal arrives. Otherwise, stage 3 would be illustrated as in Figure 23 (b) and Figure 22 (c). S_1 and S_r are turned

off; i_{Lr} flows through D_{r2} and D_{r3} to keep charging C_s until i_{Lr} decreases to zero. D_{r2} and D_{r3} would block i_{Lr} from going negative. On the other side the leakage currents are charging C_r as analyzed in stage 1.

4.5.2 Parameters Design

To ensure the soft switching conditions, observing from Figure 4.22 and Figure 4.23, two requirements have to be pre-satisfied: V_{Cr} has to achieve zero during the turn-on period, and i_{Lr} has to achieve zero before the end of the turn-off period. The second requirement is easy to meet because of the freewheeling diode D_{r3} . To satisfy the first requirement, parameters' design for the snubber circuit should be systematically analyzed.

For stage 2,

$$\begin{cases} V_{Cr} - L_r \frac{di_{Lr}}{dt} = V_{Cs} \\ C_r \frac{dV_{Cr}}{dt} = -i_{Lr} \end{cases}$$
(4.21)

Assume that at the beginning of the turn-on period,

$$\begin{cases} V_{Cr}(0) = V_{Cs} + V_{con} \\ i_{Lr} = 0 \end{cases}$$
 (4.22)

and before the end of the turning-on period, the voltage $V_{\mbox{Cr}}$ should decrease to zero

$$V_{Cr}(t_x) = 0 (t_x < t_{on})$$
 (4.23)

Take (4.22-4.23) as boundary restriction for equation (4.21), it is directly to derive equation (4.24)

$$\begin{cases} \mathbf{V}_{\mathrm{Cr}} = \mathbf{V}_{\mathrm{con}} \mathbf{C} \mathbf{S} \mathbf{\omega}_{\mathrm{o}} t + \mathbf{V}_{\mathrm{Cs}} \\ \mathbf{i}_{\mathrm{Lr}} = \mathbf{V}_{\mathrm{con}} \sqrt{\frac{\mathbf{C}_{\mathrm{r}}}{\mathbf{L}_{\mathrm{r}}}} \mathbf{S} \mathbf{i} \mathbf{n} \mathbf{\omega}_{\mathrm{o}} t & (\mathbf{\omega}_{\mathrm{o}} = \frac{1}{\sqrt{\mathbf{L}_{\mathrm{r}}} \mathbf{C}_{\mathrm{r}}}) \end{cases}$$
(4.24)

Since the voltage V_{Cr} has to achieve zero during the turn-on period, among (4.24), the amplitude V_{con} should be greater than V_{Cs} , and V_{con} is larger, the voltage V_{Cr} is decreasing faster to

zero. And for the current i_{Lr} , in order to reduce the current stress on auxiliary diodes D_{r1} and D_{r2} , L_r is preferred to be larger and C_r is preferred to be smaller.

To get further restriction for parameters selection, consider the charge balance. The electric charge stored on the capacitor C_r is charged by the leakage current

$$C_{r}(V_{con} + V_{Cs}) = \int i_{leak} dt \qquad (4.25)$$

Every time the main switch turns off, the leakage current charges the capacitor C_r until it decreases to zero. Assume the initial leakage current is I_0 , and the leakage inductor is L_{leak} ,

$$C_{\rm r}(V_{\rm con} + V_{\rm Cs}) = \frac{I_0}{2\pi\sqrt{L_{\rm leak}C_{\rm r}}}$$
(4.26)

For the Biflyback PFC converter system, when the system works under boost mode, the leakage current is mainly supplied by the second transformer T_2 ,

$$I_0 = \frac{V_{Cs}DT}{L_2}$$
(4.27)

where L_2 stands for the primary side inductance of T_2 ; D stands for the duty cycle, and T stands for the switching cycle. When the system works under the flyback mode, the leakage currents are supplied by both transformers

$$\begin{cases} I_{01} = \frac{V_{in}DT}{L_1} \\ I_{02} = \frac{V_{Cs}DT}{L_2} \end{cases}$$
(4.28)

where L_1 stands for the primary side inductance of T_1 . For the flyback mode, the charge should be calculated separately for each transformer and added together. Consider practical operation conditions, the leakage inductance is usually less than 5% of the transformer inductance. Combining all these restrictions above, values of L_r and C_r could be appropriately selected.

4.5.3 Simulation and Experiment Results

A simulation Biflyback prototype is built up using Matlab Simulink to test the proposed snubber cell. Parameters of the simulation system are set as below:

Input: 110Vac, Output: 20Vdc @100W, Switching frequency: 100kHz

The main components: Intermediate capacitor $C_s = 150 \mu F$

 T_1 primary inductance $L_1 = 90 \text{uH}$, turn ratio $n_1 = 6$

 T_2 primary inductance $L_2 = 600 \text{uH}$, turn ratio $n_2 = 3.5$

The simulation waveforms are illustrated as below. leakage inductors are 5% of primary inductors for individual transformers; Switching frequency: 100kHz. The auxiliary components:

 $C_r = 4.4 nF$, $L_r = 35 uH$.



Figure 4. 24 Simulation waveforms of the snubber cell with application in Biflyback PFC

Waveforms of Figure 4.23 illustrate the same characteristics as analyzed in Figure 4.24. The prototype of BIFRED PFC converter is also built up with simulink, simulation waveforms are the same as Figure 4.24.

The biflyback PFC prototype built in the former sections is used to carry out the experiments.

The experiment results are measured when the input voltage is 80Vac, and the output power is 20Vdc @50W.

The key waveforms are illustrated as in Figure 4.25 (a), which is similar with the simulation waveforms provided in Figure 4.24. Thus the main switch operates under ZVS during turn-off transitions, whereas the auxiliary switch operates under ZCS on both turn-on and turn-off transitions as expected in parameter design section.



(b)

(a)

Figure 4. 25fExperiment waveforms of snubber cell under different PFC topologies: (a) Biflyback PFC (b) BIFRED PFC

By disconnecting the secondary side of the transformer, a BIFRED PFC converter is constructed from the Biflyback PFC converter, and experiments are also carried out on the converter. Key waveforms illustrated in Figure 24 (a) are measured when the input voltage is 80Vac, and the output power is 25Vdc @50W, which also confirms the practicability of the proposed snubber cell.

4.6 Summary

The simplest PV power system is to connect the PV panel directly with the load. To satisfy various practical application requirements, different equipments are added into the system to increase the complexity and construct various system architectures. Because of the nature of the PV source characteristics in generating intermittent and unpredictable power, which has to deal with fluctuated load demands, energy storage is provided to the system to optimize the dispatching of power and increase the power quality and stability of the PV system. Among all these energy storage techniques, batteries are by far the most common means used for energy storage in PV systems. Classified by the different connection locations, energy storage integrated PV systems can be divided into three groups: PV panel connection type, DC bus connection type and AC bus connection type. In the AC bus connection type, PFC is required to convert AC source into DC source and charge the batteries.

In this chapter, a single stage single switch biflyback PFC converter is proposed with a digital controller. Compared with the analog controller in [118], the digital controller can achieve a better PFC without a current sensing circuit required. The operation principle and digital control design are analyzed in detail. Simulation and experiment results are provided to prove the analysis. To deal with the voltage peak during turn off period caused by the leakage inductor, a snubber circuit is proposed. The snubber cell cannot only clamp the scale, but also provide a soft switching to the main switch. Moreover, no additional PWM is required since the auxiliary switch could share the same PWM with the main switch. The operation principle and digital control design are analyzed in detail. Simulation and experiment results are provided to prove the analysis.

CHAPTER FIVE: CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

Photovoltaic (PV) panels convert solar energy into electric power. Voltage and current at PV terminals have a complicated nonlinear relationship depending on the environment temperature and irradiance. To best regulate the available power from the PV panels, several power electronic technologies have been developed in recent decades.

In this dissertation, AC PV module which can directly provide ac power to the grid is selected to carry out the PV power conversion system. Micro-inverter as a main component of AC PV module is carefully studied to achieve high power density, high power efficiency and optimum electrical quality.

In numerous micro-inverter topologies, the dual stage inverter structure is selected in this thesis. In dual-stage inverters, the DC voltage rising circuit and DC/AC voltage inverting circuit would be decoupled, while the MPPT function and bus voltage balance function would be separated as well. Thus the circuit design and controller design would be much simpler compared with single stage inverter. Compared with three stage inverters, the dual stage inverters have a better power efficiency and fewer components for less energy processing stages.

For the first DC/DC stage of the dual-stage inverters, the resonant converter topologies are suitable candidates. As the resonant nature can generate soft switching conditions for all switches, switching frequency could be increased, while power density and efficiency could be increased as well.

The MPPT function is realized in the DC/DC stage. However the performance of the resonant

converter depends upon not only circuit parameters, but also operation conditions, which are difficult to determine with load and input voltage variance. In chapter two, analysis is made based on the frequency modulation for various resonant converters (including the series resonant converter (SRC), the parallel resonant converter (PRC), the series-parallel resonant converter LCC (or SPRC), LLC resonant converter and LCLC resonant converter). Conclusions about whether or not they are suitable to carry out MPPT with frequency modulation are discussed respectively for each topology. Since the power frequency (P-F) waveforms of various resonant converters are different from each other, conventional MPPT might fail for some P-F waveform. To solve this problem, a novel center points MPPT is proposed. A LLC converter prototype is built for the verification of the proposed MPPT, the proposed MPPT have advantages in fast tracking speed and little oscillation power loss. To expand the applications of the proposed MPPT, simulations on other resonant converters are also carried out, and experiments on LCLC prototype are practiced. The waveforms and results show the same characteristics as theory analysis.

For the second DC/AC stage of the dual-stage inverters, the soft switching techniques are required to improve power efficiency and power density. The active soft switching techniques are reviewed in chapter three. All of them require additional components to construct a high-frequency resonant network around the main switches. During their commutations the resonant network operates for a very short period to create ZVS or ZCS conditions for the main semiconductors. Chapter three proposes a novel ZVS technique without auxiliary components. The operation principle and modulation schemes are analyzed in detail. Controller applied with DSP is provided

with analysis. Simulation and experiment results verify the feasibility of the proposed ZVS technique.

As the available power generated by PV panels are time varying and circumstance dependent, power load can fluctuate considerably and changes occur within minutes or seconds. To balance the requirements from fluctuated load and intermittent source, energy storage is introduced into the PV system. Thus in some PV system applications, electric power from grid or other source (for example: batteries) is provided to the load when PV power is insufficient. In these cases, the usages of PFC converters are required.

Chapter four provides a review on the PFC topologies. A single stage biflyback PFC is selected for small power application because of its advantages in voltage and current stresses and simplicity in topology. In former analog controllers of the biflyback PFC, the voltage loop for voltage regulation is realized with a PI controller, while the current loop for input current shaping is dependent fully on the DCM automatic power factor correction function, with peak current restriction provided to the main switch. In chapter four, a DSP controller is provided for regulation input current shaping based on mathematical analysis. The new controller is simple in control and does not need current sensing, which saves cost in advance. Simulation and experiment results illustrate the effectiveness of the proposed controller.

To deal with the peak voltage caused by leakage inductor of transformers in the single stage PFC, a snubber cell is provided. As analyzed in chapter four, it has a wide application range in all boost type input current shaper PFC. The auxiliary switch in snubber cell shares the same PWM signal with the main switch, which does not need any additional controller circuit. The operation principle is discussed carefully. The prototypes of the snubber cell are built on the Biflyback PFC converter and the BIFRED PFC converter individually. Experiment waveforms prove its practicability.

5.2 Future Works

Based on the V-I relationships of various resonant converters calculated in chapter twothere are some voltage and current which could not be arrived at by these resonant converters. Thus to ensure the MPPT could successfully find the real maximum power point (MPP) of the PV panel, the parameters of resonant converters should be designed carefully based on the possible MPPs regions. Thus further calculations and analysis are required to optimize the design for every resonant converter.

For the ZVS technique proposed in chapter three, the switching frequency varies in a huge range, which would increase the complexity of EMI design. Moreover, the large switching frequency range also is an obstacle in decreasing inductor volume and increasing power density. Further study is required to solve this problem in deriving new topology or novel control schemes. Further research can focus on narrow down the frequency range without sacrificing the power efficiency.

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