ADVANCED TECHNIQUES OF SINGLE-STAGE POWER FACTOR CORRECTION AC-DC CONVERTERS

by

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ABSTRACT

Power supplies connected to AC mains introduce harmonic currents in the utility. It is very well known that these harmonic currents cause several problems such as voltage distortion, heating, noises, and reduce the capability of the line to provide energy. This fact and the presence of Standards or Recommendations have forced the industry to use power factor correction (PFC) in power supplies.

This dissertation aims to improve the performance of the single-stage power factor correction (S^2 PFC) AC-DC converters with reduced cost. In the dissertation's first two chapters, an overview of current techniques for single-stage PFC AC-DC power systems is given. Further, issues and challenges of the existing systems are addressed in detail.

In the dissertation's third chapter, the existing S^2 PFC AC-DC approaches are topologically generalized to pursue a methodology for potential topology variation, thereafter to overcome the issues that block the applications of single stage PFC AC-DC conversion approaches.

In the dissertation's following chapters, applications of the proposed translation rule are discussed, and the subject of design of high quality S^2 PFC AC-DC power systems is investigated from the perspective of cost-effectivity, simplifying the conversion process while simultaneously keeping acceptable performance. The focus is put on alleviating voltage stress and current stresses, and better energy management in power conversion

that features reduced complexity and higher efficiency.

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1 INTRODUCTION

1.1 Research Background and Motivation

Power conversion system design issues are becoming increasingly important in state-of-the-art electronic systems. However, the basic power architecture in current electronic systems remains the same as it was decades ago [1]. Many current power architectures are no longer effective in terms of performance and/or cost.

Power supplies connected to AC mains introduce harmonic currents in the utility. It is very well known that these harmonic currents cause several problems such as voltage distortion, heating, noises, and reduce the capability of the line to provide energy. This fact and the presence of Standards or Recommendations have forced the industry to employ power factor correction in power supplies. Active power factor corrective techniques are becoming an important feature that is compulsorily required of switching power supplies.

Unity power factor and tight output voltage regulation are achieved with the very well known two-stage approach, shown in Figure 1-1. This is probably the best option for high power AC-DC converters due to the following reasons:

- Sinusoidal line current guarantees the compliance of any Regulations.
- It is valid to operate with universal line voltage.

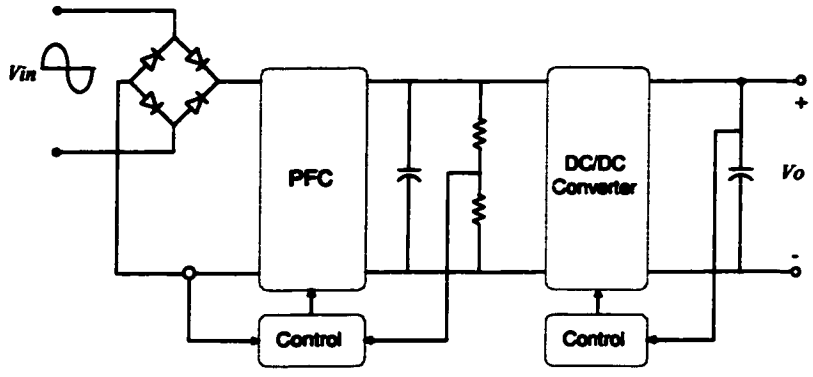


Fig. 1-1 Two-stage PFC AC-DC scheme

- Voltage on the storage capacitor is controlled and it allows a good design of the second stage.

However, since two cascading converters compose the power stage, size, cost and efficiency are penalized, mainly in low to medium power applications.

Although unity power factor is the ideal objective, it is not necessary to meet the Regulations with unity power factor. For example, both IEEE 519 and IEC 1000-3-2, despite being very different in nature, allow the presence of harmonics in the line current [2]. This fact has lead to the publication of a great number of papers in the last years, with solutions that obtain some advantages over the two-stage approach. Some of these circuits are practical but others are too complex to be worth the change.

The motivation drives us to incorporate advanced power conversion techniques into the system of Fig.1-1 in order to obtain further simplification of the overall AC-DC structure. An alternative solution to realize the goal is to integrate the active PFC stage

with the isolated high quality output DC-DC stage into one stage, which is known as single-stage converter with the least components and simplest controller.

Theoretically, changing the two-stage scheme to one-stage scheme can substantially mitigate the cost and complexity of PFC AC-DC converter. Then the question arises, why has such a concept not been extensively adopted in today's power systems? The answer is because there are still some of the existing technical challenges with respect to the development of viable single-stage PFC AC-DC converters, such as high voltage stress, high current stress and low efficiency, etc.

It's noted that the 2001 global market forecast indicated that the hottest trend in the external AC-DC power supply markets is the rapid growth in the higher wattage segments, typically wattage range of 50W to 150W (or higher). Compared with the lower-wattage segments, this segment is growing at a faster rate of about 16.7% per year [3]. Therefore, pursuing a cost-effective single-stage conversion scheme with improved performance, especially reduced voltage and current stresses, is still an attractive research topic.

With the effectivity of newly issued national and international Regulations, and increasing dollar market, the cost-effective S^2 PFC AC-DC conversion is one of the hottest research areas in power electronics. This dissertation is intended to systematically address the major technical issues in existing S^2 PFC AC-DC conversion and to give proper cost-effective solutions.

1.2 Dissertation Outline

The dissertation is organized into eight chapters, including the conclusion chapter, as follows:

Chapter 1 presents background and motivations of this work.

Chapter 2 offers a review for current techniques proposed for the PFC AC-DC conversion and discusses in details various issues, solution trends, and.

Chapter 3 first generalized the current S^2 PFC AC-DC conversion approaches into two categories, and addresses the key issues of S^2 PFC AC-DC converters from the view of topology. Then, several potential topology variations, applying generalized rules, are proposed to overcome the barriers summarized in Chapter 2.

Chapter 4 first introduces the mechanism of high voltage stress in single-stage PFC approaches, and briefs the documented solutions. Then, a new PFC cell with inherent voltage clamping feature, called "fly-boost", is presented based on topological methodology.

Chapter 5 presents three current stress suppression techniques. Current stress leads to lower efficiency and deteriorates EMI performance, generally, DCM operation inevitably brings about higher current stress, and CCM is preferred from the view of lower current stress. Lower current stress DCM operation scheme and high power factor CCM operation scheme are proposed for specific applications.

Chapter 6 investigates better energy management techniques in terms of processing less energy or processing it with higher efficiency. Unlike the two-stage schemes, in which the power being processed twice by two serially connected stages, single-stage scheme has potential to process less energy during power conversion. In this part, straight energy transfer and high efficiency processing with soft switching scheme are introduced, and the characteristics such as increased efficiency, near unity power factor and lower voltage stress are experimentally verified.

Chapter 7 proposed two novel critical conduction mode control schemes, which are tailored for proposed topology to further improve its performance.

Chapter 8 summarizes the conclusions of this work and presents suggestions for future work in related research directions.

2 REVIEW OF SINGLE-STAGE PFC CONVERTERS

2.1 Introduction

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produces radiated and conducted electromagnetic interference, and leads to poor utilization of the capacity of the power sources. In compliance with IEC 1000-3-2 harmonic regulation, many power factor corrected AC-DC rectifiers have been proposed in recent years. For single-phase electronics applications, passive power filters, active one- and two-stage power factor correction (PFC) rectifiers are typical approaches used to achieve high power factor and low total-harmonic-distortion (THD). Passive power filters exhibit high efficiency and low cost, but they are bulky and heavy due to the size of the line frequency inductors and capacitors.

The two-stage PFC approach uses an input current shaping converter in front of a DC-DC converter. The two converters are controlled independently to achieve high quality input current shaping and fast output voltage regulation. This method is known for its superior performance, such as high power factor, low input current harmonics, good hold-up time, and optimized design of the DC-DC converter, but at the cost of additional semiconductor switches and control circuitry that may not be justified for lower power applications. In a single-stage PFC rectifier, input-current shaping, isolation,

and fast output regulation are performed in a single-stage. A single-stage PFC rectifier typically integrates an input current shaper and an isolated DC-DC converter with a shared switch and controller. The energy storage device in between serves as a buffer for frequency isolation between the PFC and the DC-DC converter as well as provides necessary hold up time. This method provides a compromise between the performance and cost.

Comprehensive comparisons of the two approaches at manufacturing cost and performance [3] have shown that the single-stage PFC is a cost-effective solution for low power applications (typical below 200 watts).

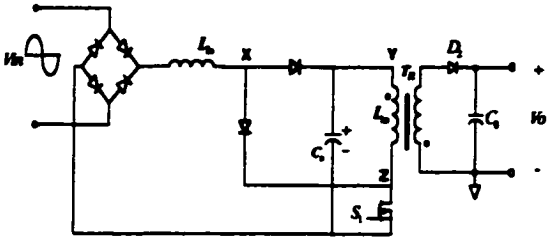
2.2 Review of Single-Stage PFC Converters

The concept for single-stage PFC can be traced back to some early work presented in [4,5]. In article [4], a single power stage with dual outputs produces both the desired DC output and a boosting supply in series with the input. Without active control of the boost supply, a reasonably good input current shape results due to the natural gain characteristics of the boost resonant circuit. This circuit is original but the component count is high. Another way to realize single-stage PFC is by cascading a boost PFC with a DC-DC converter using one switch as shown in [5]. Both pulse width modulation (PWM) and frequency modulation (FM) were applied in the control circuitry. The rectifier has very high power factor. However, the circuit suffers wide frequency

variation and high voltage stress. Nevertheless, this circuit presents an early form of the single-stage PFC method that integrates a boost PFC with a DC-DC converter in a cascade fashion. A very systematic synthesis of single-stage PFC using a cascade method was initiated in [6] in 1992, in which some new PFC rectifiers, BIFRED and BIBRED, were resulted from integrating a boost input current shaper with a flyback or buck converter. The characteristic marker of these rectifiers is that the energy storage capacitor is in the series path of the energy flow. Synthesis of single-stage PFC by inserting a diode in front of the Cuk and Sepic converters have resulted in the same topologies [7,8]. In BIFRED and BIBRED, the boost PFC operates in discontinuous conduction mode (DCM) to achieve automatic input current shaping, while the DC-DC converter operates in continuous conduction mode (CCM). The DC-bus capacitor voltage has a strong dependency on the load. For universal input applications, such circuits will suffer high voltage stress at light load. Articles [7,9] use frequency modulation method to keep the DC-bus voltage under control during light load. Article [8] shows a new operation mode that operates both the boost and the flyback in DCM, which has effectively reduced the DC-bus voltage and significantly improved the input current waveform.

In 1994, a new family of single-stage PFC converter was synthesized in [10] that integrates a boost PFC with a DC-DC converter in such a way that the energy storage capacitor is in the parallel path of the energy flow as shown in Fig. 2-1(a). In all the PFC converters shown in [10], the boost PFC operates in DCM to achieve automatic input current shaping, while the DC-DC converter may operate in either CCM or DCM.

However, if the DC-DC converter is in CCM, the DC-bus capacitor voltage varies with



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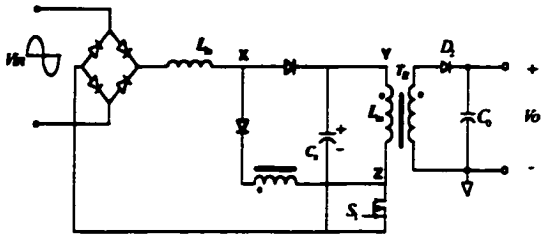

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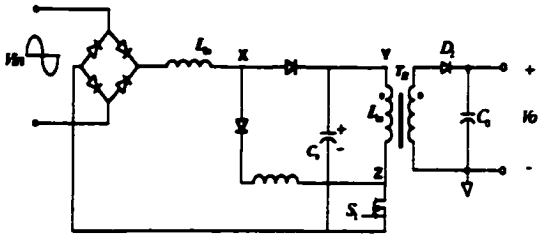

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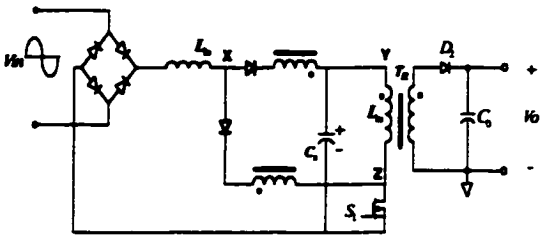

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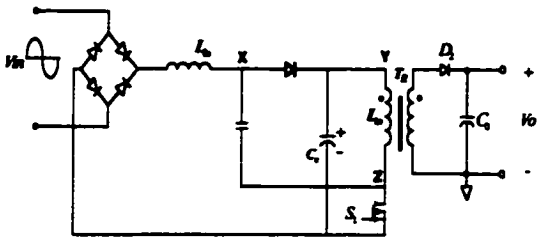

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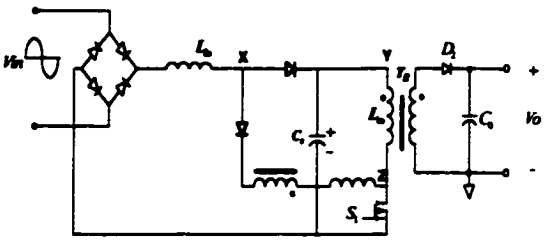

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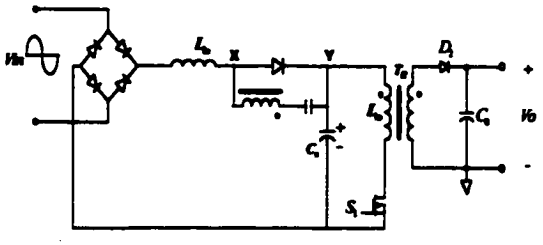

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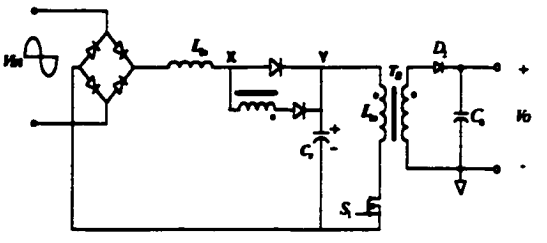

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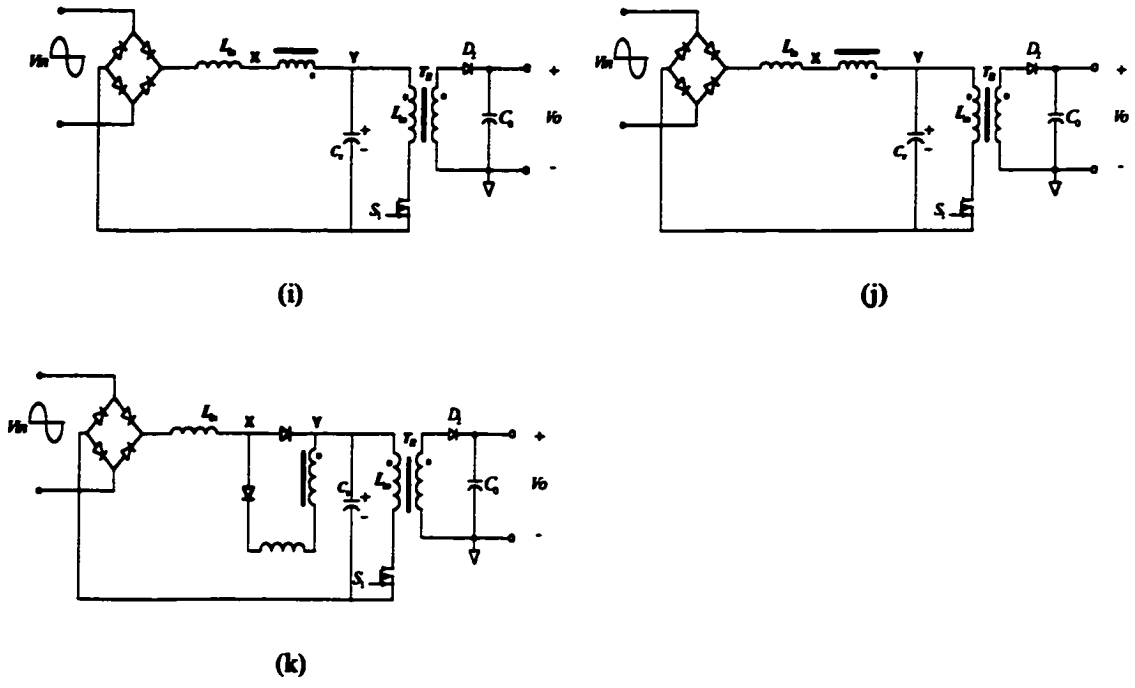


Fig. 2-1 Existing S^2 PFC Topologies

the load. For universal input applications, it will suffer high voltage stress at high input voltage and light load, which requires expensive capacitors and increases the switch voltage stress. This phenomenon appears inherent to the rectifiers that cascade a boost PFC with DC-DC converter as shown in [5,6,10]. Switching frequency modulation methods were reported to alleviate the DC-bus voltage [11,12,13]. However, the switching frequency could span ten times over the whole load range in order to maintain the DC-bus voltage be low 450V, which is undesirable for the magnetic component design. Another way to suppress the DC-bus voltage is to keep the DC-DC converter in DCM for the entire load range [14,15,16], because the DC-bus voltage becomes independent of the load in DCM. However, for low-voltage applications, e.g. computer

power supplies, continuous conduction mode DC-DC converter is preferred, since it leads to lower conduction loss and smaller ripple. As a result, a compromise between the THD and the voltage stress was proposed in [17] by negative magnetic feedback using an additional transformer winding during the switch-ON interval, as shown in Fig. 2-1(b). Similar approaches were seen in [18]. Article [19] presents a comprehensive study of the magnetic feedback phenomenon and design guidelines. With this negative feedback, the conduction angle of the input current is reduced. The gained benefit is that the DC-bus capacitor voltage Vcb may be maintained below 450V, while the DC-DC converter is in CCM for heavy load, which warrants the use of low cost 450V electrolytic capacitors. A single-stage PFC method with double-negative magnetic feedbacks (feedback during both switch ON and OFF intervals) was proposed [20,21] as shown in Fig. 2-1(c). This method can also keep the voltage Vcb below 450V. In addition it enables CCM operation of both the PFC and the DC-DC converter while the input harmonics are still within the range of Class D standard. In order to reduce the conduction loss and ripple in the input, several single-stage PFC rectifiers with CCM operated PFC were proposed recently as shown in Fig. 2-1(d), (e) (f), (g). The converter in Fig. 2-1(d) was derived from the charge bump concept [23] and the converters in Fig. 2-1(e-g) are based on series insertion of a voltage source and a loss free resistor in between the diode bridge and the DC-DC converter [24-28]. A magnetic switch concept was introduced in [29-33], where the PFC usually contains one additional winding coupled to the transformer of a DC-DC converter.

Several examples are shown in Fig. 2(h), (i), (j), where the input PFC cell in Fig. 2-1(i) operates in CCM. Note that although the flyback DC-DC converter is shown in all approaches in Fig. 2-1, the discussion here are applicable to forward and other topologies as well.

Topologies variations are also found in many other forms. A parallel PFC concept was reported in [34], while three switch-states were used to provide two-dimensional control for the PFC function and fast output regulation. The performance is commendable but the implementation is very complicated. In [35,36], a flyback converter is used as PFC, which results in better input current waveform but higher current stress. An interesting method of combining a boost PFC with a forward converter with two energy storage capacitors was shown in [37]. With two capacitors, the spike due to the leakage inductance during switch turn off is subdued. Very good performance was demonstrated. Article [38] shows a new single-stage PFC rectifier that uses an AC side inductor and two additional diodes to directly connect the AC voltage to the switch. This circuit has similar operational principle as the one proposed in [10], but with less conduction loss. The rectifier proposed in [16] uses a boost bridge rectifier that shares its switches with the following flyback DC-DC converter with the intention to increase the power level. Since both the boost bridge rectifier and the flyback converter operate in DCM, the conduction loss is high. In addition, this circuit may suffer high common mode noise. Article [39] presented a rectifier that integrates a boost PFC and a half bridge DC-DC converter. Synchronized rectifiers are used to achieve high efficiency for low voltage applications. Article [40] proposed a regenerative clamping circuit for single-stage PFC to reduce the

turn-off losses and stress of the switch. In addition, the power factor is also improved. Article [41] reported a single-stage high power factor converter using the Sheppard-Taylor topology. Two possible operation regimes are described. Compared to the usual boost-buck cascade operating in the first regime, the proposed converter has a wider operating range. When operating in the second regime, the modified boost stage has the ability of producing a harmonic free input current, unlike the standard boost PFC whose current always suffers a cusp distortion. A new parallel approach for single-stage PFC was reported in [42~45] that employs an auxiliary DC-DC converter to supplement energy to the load when the direct power from the line is low. This method improves overall efficiency because only partial energy is processed twice. An additional switch is required. Extensive syntheses were performed in [46,47] that yielded many families of single-stage PFC rectifiers based on dither effect [46] and partial energy processing [47]. These two papers present interesting teaching from the principle of synthesis as well as analysis to the implementation of the new circuits, and thus are valuable to researchers in the power factor correction area.

2.3 Issues, Trend and Challenges

The underlining strategy of the single-stage PFC scheme is to design the circuit in a certain way that allows its PFC circuit and power conversion circuit to share the same power switch with the same controller. From the above existing research efforts, we

found this kind of arrangement brought about several main issues, which we will discuss below.

The first issue is the high voltage stress, accompanying a wide capacitor voltage range. The high bus capacitor voltage-stress generally makes most of the existing S^2 converters impractical [1]. The inherent reason of high DC-bus voltage is in power unbalance between the input and the output. Although the output power is kept relatively constant over one line cycle, instantaneous AC input power always varies. As a result, a bulky capacitor is needed to handle the instantaneous power difference between the input and output, such that the output voltage is regulated tightly and free of line ripple. It is because single-stage converters have only limited capability to process unbalanced power with a single active switch and limited capacitance capacitor. The high bus capacitor voltage stress normally exists for most of single-stage PFC converters, which makes most of existing single-stage converters impractical for universal input usage. This issue is more severe under high line and light load conditions [2,4]. A high bus voltage means high component rating, high cost and low efficiency. The accompanying issue with the first one is that the wide capacitor voltage range of the single-stage PFC converters will require larger component ratings compared to the two-stage PFC converters. To make situation worse, the intermediate bus voltage is determined by many factors such as boost inductance, transformer turns ratio, and input voltage, etc. Therefore, how to characterize bus voltage and optimize designing of the power stage will be further challenges.

The second issue is the high current stress due to the DCM operation. The PFC stage in an S^2 PFC AC-DC converter normally operates in DCM mode to utilize its inherent current shaping capability, therefore, compared with cascading two-stage schemes, S^2 PFC AC-DC conversion has higher current stress. Current stress not only accompanies with increased switching losses and lower efficiency, but also brings about annoying EMI issues.

The third issue is as the result of high voltage and current stresses, the lower efficiency. The fourth issue is that one power stage and DCM operation makes S^2 PFC AC-DC converters only attractive for low power applications, limiting its application. Therefore, how to push the power rating higher with a low-cost single-stage approach becomes a natural objective.

Although unity power factor is the ideal objective, it is not necessary to meet today's Regulations with unity power factor. For example, both IEEE 519 and IEC 1000-3-2, even being very different in nature, allow the presence of harmonics in the line current [1,2]. This fact opens the door for the trade-off quality-cost techniques, which are capable of overcoming the above issues. Actually in the last years, a great number of papers pursue such solutions that obtain some advantages over the two-stage approach. Some of these circuits are practical, but most of them are too complex to be worth the change.

Seeking the simplest low cost S^2 PFC solution with better performance, including high efficiency, low voltage and current stresses, low harmonics and high power factor will be further efforts, and are the objective of this dissertation.

2.4 Summary

A review of existing single-stage PFC AC-DC converters is given in this Chapter. Main issues such as high voltage stress, high current stress, low efficiency and low power rating in current S^2 PFC AC-DC approaches are summarized and presented as the topic needs further efforts.

3 TOPOLOGICAL METHODOLOGY FOR SINGLE-STAGE PFC CONVERTERS

3.1 Introduction

For single-stage PFC rectifiers, the performance measures, such as efficiency, hold up time, component count and circuit complexity, component voltage and current stresses, input current quality, etc., are largely dependent on the circuit topology. In recent years, the heat wave of searching for single-stage PFC rectifiers has resulted in hundreds of published papers in the open literatures and countless topologies. This chapter presents a topological study of the representative S^2 PFC converters. The intention of this study is to find a topological relationship among various converters, topologically explain the main drawbacks of current S^2 PFC converters, and to pursue potential variations to overcome the barriers that limit the application of S^2 PFC converters.

3.2 2-Terminal PFC Cell and 3-Terminal PFC Cell

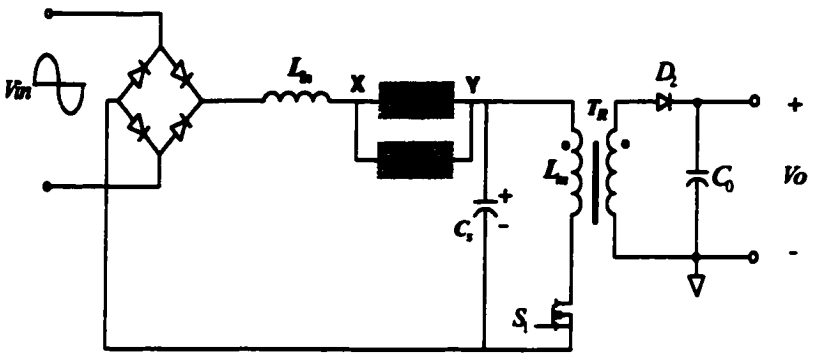
From the review of S^2 PFC AC-DC converters, it is noticed that the group of circuits shown in Fig. 2, characterized by the energy storage capacitor in the parallel path

of the energy flow, represents the main stream. The focus of this Chapter is thereby on the topological rules of this group of converters. The 2-or 3-terminal concept presented in [48] is extended to study the PFC cells. In spite of different PFC realization mechanism, from a topology point of view, the input current shaping circuits in Fig. 2-1 can be symbolized as 2- or 3-terminal cells, as shown in Fig. 3-1. Each PFC cell contains an input inductor and two branches. The "charge branch" is used to charge the input inductor when the switch is ON. The "discharge branch" is used to discharge the inductor and transfer the energy from the input inductor to bulk capacitor or output when the switch is OFF. The branches are usually composed of diodes, capacitor, inductors, and extra windings of the transformer or their combinations. Terminal X is connected to the input diode bridge; terminal Y is connected to the DC-bus bulk capacitor Cs; and terminal Z is connected to the switch in the DC-DC converter.

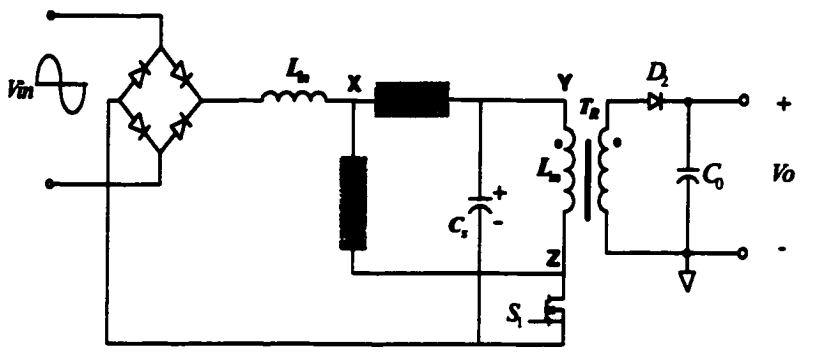
The 2-terminal PFC cell is inserted between the input diode bridge and DC-bus capacitor. It contains one winding coupled to the transformer of a DC-DC converter in the charge branch. When the switch is ON, the voltage across the winding cancels the capacitor voltage, so that the inductor sees only the input voltage that charges the inductor. The input inductor is discharged through the discharge branch when the switch is OFF. The topologies in Fig. 2-1(g-j) are several examples of single-stage PFC with 2-terminal PFC cells.

In a 3-terminal PFC cell, the switch is connected in a series with the charge branch. When the switch is ON, the input inductor is charged through a switch. Similar to the 2-

terminal PFC cell, the inductor current is discharged through the discharge branch. The PFC cells in topologies of Fig. 2-1 (a-f) belong to this group.



(a) 2-Terminal PFC cell scheme



(b) 3-Terminal PFC cell scheme

Fig. 3-1 Generalized PFC schemes

3.3 Topological Analysis for Key Issues

From above generalized S^2 PFC AC-DC approaches, it is found that many reported single-stage PFC converters are electrically equivalent despite that they are topologically

different, because they employ equivalent PFC cells, although their configurations are different.

Besides, the existing issues, to a certain extent, can be topologically explained:

First, in all of the existing schemes, a Boost PFC cell is serially connected with a power charge and/or discharge path. Under this arrangement, the PFC inductor is charged in ON interval, and discharged in a boost mode in OFF interval. In the other words, all the power processed in power stage should be stored in the PFC inductor first. Thereby its boost operation mode theoretically gives the explanation why the voltage across the bulk capacitor, under any case, is higher than the peak value of input voltage. Besides, the combined PFC cell and DC-DC cell need to be well matched from the view of energy transferring, since duty ratio is only determined by the DC-DC stage. Without introducing power transferring information in a DC-DC cell will certainly result in the build up of unbalanced energy, in terms of high intermediate DC-bus voltage. That is to say, in most cases, DC-bus voltage stayed in an uncontrolled condition.

Second, since all the power should be stored in the PFC inductor first, and the PFC inductor had to operate in DCM mode to utilize its inherent current shaping feature, so input current peak should be high enough to get the desired output power, with no choice to reduce its current stress.

Third, from the view of energy transfer stream, it can be found that all the energy stored in the boost inductor should be discharged to the buffer capacitor first, and then be delivered to the output. That is to say, all the energy has been processed twice, although

its structure is a so-called single-stage. This fact is another cause resulting in lower conversion efficiency.

3.4 Variations of PFC Cell and Their Potential Features

From the above topological analysis, we found it is possible to break the confinement of current PFC cells to overcome the issues existing in current S^2 PFC AC-DC approaches:

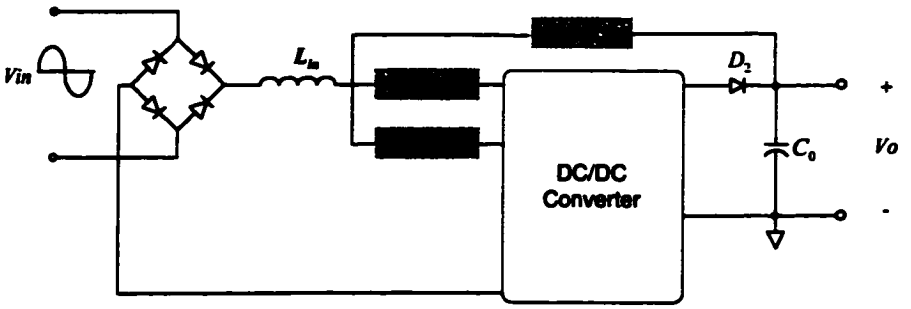
First, it is not necessary that the energy stored in the PFC inductor must be discharged to the buffer capacitor; therefore, a concept to build an alternative energy transfer path arises here naturally. For example, building another discharging path straight to the output side, as shown in Fig. 3-2(a), probably gains the following benefits:

(1) Controllable bus voltage, intuitively, less energy charged to the buffer capacitor, certainly will reduce the voltage across it. Therefore, the bus voltage may be controlled through selecting the proper energy portion being charged to the buffer capacitor.

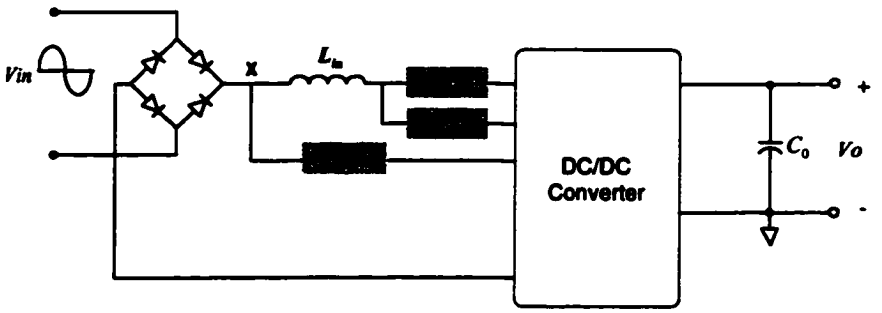
(2) Reduced current stress, since the discharging mode of the boost PFC inductor has already been changed. To obtain the same RMS input current, it could be carried out in a lower peak value mode.

Second, it's not necessary that all the power transferred to the output have to be stored in the Boost PFC inductor first. In fact, unlike cascading two-stage schemes, the energy had to be processed twice by two serially connected power stages. A S^2 PFC AC-

DC converter, from the view of its structure, it is not necessary to process the energy twice. Here an attempt arises why not push the joint "X" ahead in front of the inductor, as shown in Fig. 3-2 (b). Reducing power being charged into the PFC boost inductor can further alleviate voltage stress and provide a possibility to increase the inductance of the boost inductor to reduce the peak current; thus obtaining less current stress with higher efficiency.



(a) An alternative-discharging path for Boost inductor



(b) An bypass path for Boost inductor

Fig. 3-2 Topology variations for the generalized schemes

3.5 Summary

Many single-stage PFC can be viewed as a combination of the DC-DC converter with a 2-terminal or 3-terminal PFC cell. The main drawbacks of current S^2 PFC AC-DC converter can be explained, to a certain extent, from its topological features. In S^2 PFC AC-DC converters, as state-of-the-art electronic systems, it is possible to overcome the main drawbacks by breaking the confinement of current PFC cells, and employing proper topologies capable of changing current energy transferring modes.

4. VOLTAGE STRESS SUPPRESSION TECHNIQUES

4.1 Introduction

For S^2 PFC converters, the DC-bus voltage stress is one of the most important issues. The inherent reason for high DC-bus voltage is the power unbalance between the input and the output. In single-stage PFC AC-DC conversion, although the output power is kept relatively constant in a certain time range, instantaneous AC input power always varies. As a result, a bulky capacitor is needed to buffer the instantaneous power difference between the input and output, such that the output voltage is regulated tightly and free of line frequency ripple. Since single-stage converters have limited capability to process unbalanced power with a single active switch, and the buffer capacitor has limited capacitance, the high voltage-stress will be built up across the buffer capacitor for most of single-stage PFC converters. Resulting high voltage normally goes beyond the tolerance of commercially available capacitors, and limits the power switches to components with higher voltage ratings, which means either high $R_{ds,ON}$ (ON Resistance) or V_F (Forward Voltage Drop).

High bus voltage means high component rating, high cost, and low efficiency. High variable bus voltage, in fact, makes most of existing single-stage converters impractical for universal input applications. This issue is more severe in case of high line and light

load. Therefore, further efforts need to be invested to alleviate DC-bus voltage and optimize designing power stage. In this section, after briefing the existing approaches, an inherent voltage-clamping scheme is proposed, analyzed and experimentally validated.

4.2 Mechanism for High Intermediate Bus Voltage Stress

Figure 4-1 shows a general block diagram of S^2 PFC converters, which use only one active switch and one controller. In order to generalize the concept of bus voltage stress, it is desirable to use two functional blocks, a PFC block and a DC-DC block, to represent the S^2 PFC AC-DC converter, as shown in Fig. 4-2. The first block is a PFC stage to achieve high power factor function, which is usually a boost-like converter; the

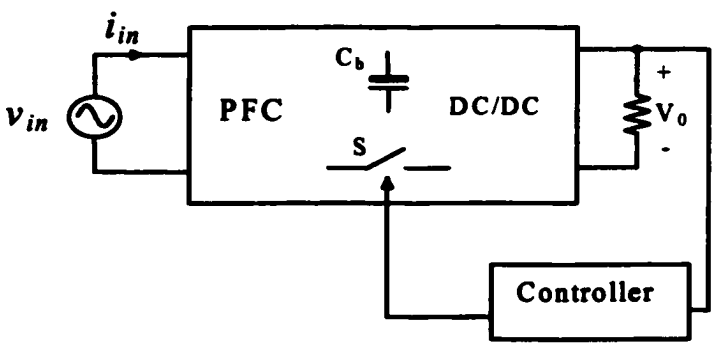


Fig. 4-1 General block diagram of S^2 PFC converters

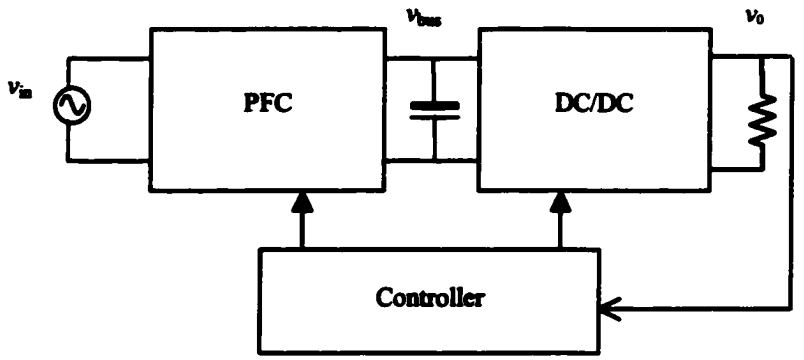


Fig. 4-2 Functional block diagram of S2 PFC converters

second functional block is a DC-DC converter to obtain tight regulation with output isolation. There is a bulky capacitor between the two functional blocks to withstand the fluctuating input power and rectified line ripple. Both PFC block and DC-DC block can operate either in DCM or in CCM. Therefore, there are four possible combinations to implement in S^2 PFC converters, i.e., DCM PFC + CCM DC-DC, DCM PFC + DCM DC-DC, CCM PFC + CCM DC-DC and CCM PFC +DCM DC-DC. However, these combinations present different forms of the power balance relationship. For example, the DCM PFC + CCM DC-DC combination generates a DC-bus voltage that could be as high as over 1000 V at high line and light load conditions for universal line applications [18]. Selection of switches and capacitors in this case would be limited and very costly.

Usually, it is required that the PFC block has an inherent PFC property, while using the controller regulates the output voltage of DC-DC block. On the other hand, the CCM operation for DC-DC block is preferred to reduce power losses. Therefore, for the

operating mode, the DCM PFC + CCM DC-DC is deemed to be ideal in the low to medium power level. However, critical bus voltage stress occurs in this combination. Figure 4-3 shows the relationship between the input power and the duty cycle in the PFC block, and between the output power and the duty cycle in the DC-DC block [18]. The figure explains well the reason why the unbalanced power exists.

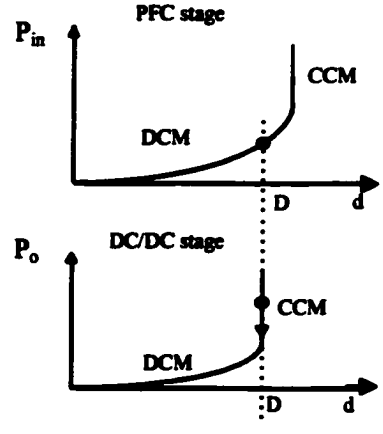


Fig. 4-3 Relationship between the input power, output power, and duty-cycle

Since the DC-DC stage operates in CCM, the duty cycle does not change with the load variation according to Fig. 4-3. The duty cycle doesn't change immediately when the output power decreases, because of the CCM operation in the DC-DC block. Thus, the input power remains the same as that of the heavy load. There exists an unbalanced power between the input and the output. This unbalanced power has to be stored in the bulk capacitor C_B, causing the DC bus voltage to increase. As a result, the output voltage will increase too. To compensate for the output voltage increase due to the increase of the bus voltage, the voltage feedback loop is operated to regulate the output voltage as a

constant. So the duty ratio has to decrease, and the input power also decreases correspondingly. This dynamic process will not stop until the input power equals the output power, and new power equilibrium is reached. In summary, power unbalance in different operating mode combination is the inherent reason for causing high bus voltage. The detailed analysis and explanation of the power balance relationship for the other combination modes have been presented in [18].

4.3 Several Schemes to Alleviate Bus Voltage

From the above analysis, perceptively, the bus voltage could be controlled within proper range so as to make a S^2 PFC converter be practical. The analysis also provides some possible approaches to resolve the bus voltage stress problem of the S^2 AC-DC converter at high line light load. If the power delivered by both blocks of the converter is either duty cycle dependent or independent simultaneously, the converter should have less bus voltage stress under the proper design. Some S^2 PFC implementation circuits with proper bus voltage have been presented in [19, 20, 21, 23]. This section classifies these circuits into the following three categories of schemes to suppress high bus voltage stress:

4.3.1 Series-Charging, Parallel Discharging Capacitors Scheme (SCPDC)

A S^2 PFC converter with low capacitor bus voltage is proposed in [36, 37] Actually, it is a combination of a boost circuit and a forward circuit, as shown in Fig. 4-4.

There are two primary windings connected with separate bulk capacitors in series in the isolated transformer of the DC-DC stage. It is because of this unique structure, which makes the converter capacitors implement series-charging, parallel discharging capacitors scheme (SCPDC). The SCPDC means that the two energy-storage capacitors are charged in series when the switch is OFF, and discharged in parallel when the switch is ON. Thus, effectively, a two-to-one voltage division is introduced into the original single bulk capacitor, as most S^2 PFC converters hold, such as BIFRED and BIBRED converters.

However, although the two serially connected capacitors can handle higher voltage, the real DC-bus voltage is still high, and high voltage rating components had to be used in this conversion scheme.

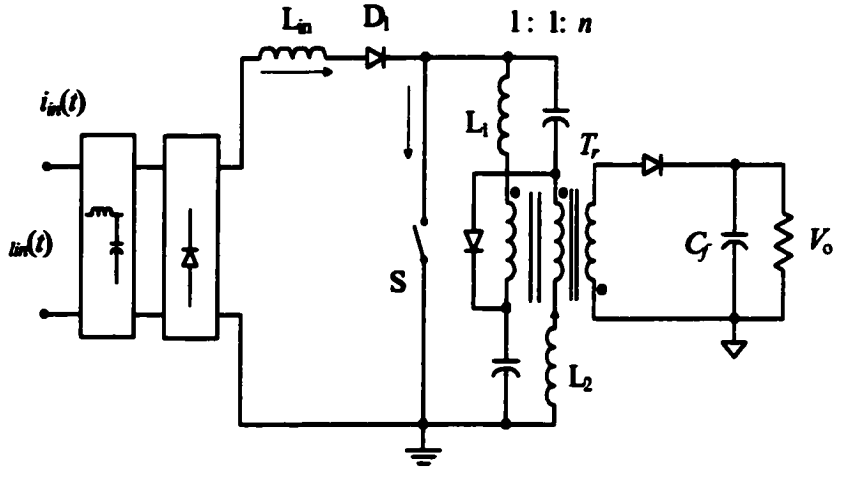


Fig. 4-4 A S^2 PFC converter with low Capacitor voltage

4.3.2 Bus Voltage Feedback

Figure 4-5 shows the modified BIFRED converter with the bus voltage feedback. The basic BIFRED converter is actually a combination of a DCM boost converter and a DC-DC flyback converter. This converter is not practical due to high DC bus voltage caused by unbalance power between two functional blocks of PFC and DC-DC. [18]

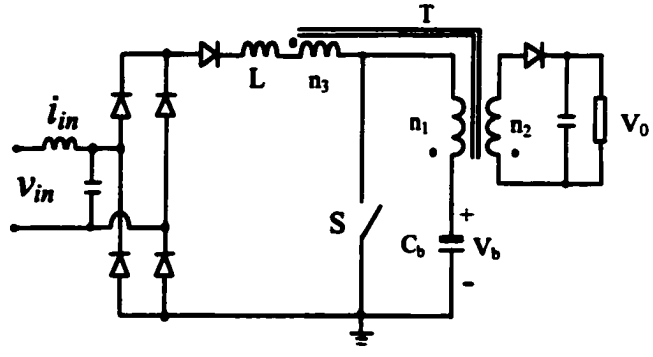


Fig. 4-5 BIFRED converter with DC voltage feedback

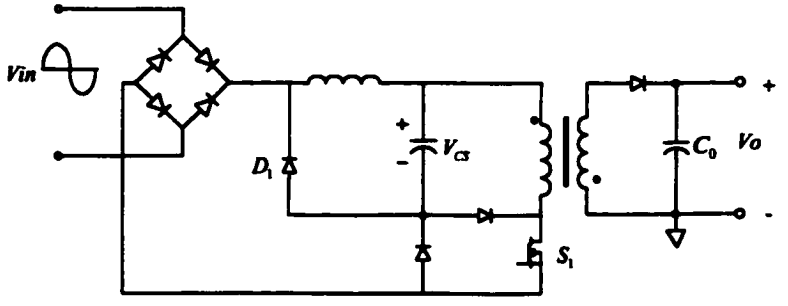
In the modified scheme, an additional transformer winding n3 is added on the boost inductor branch in the series. The winding then can feedback the bus capacitor voltage when the boost inductor is charged, and the feedback depth depends on the DC-bus voltage level. The feedback depth will increase when the bus voltage has an increasing trend. Thus, the input power can be automatically reduced to guarantee the balance between input and output power. As a result, the DC-bus voltage is limited within a proper range.

Based on the concept of using bus voltage feedback, some of the new topologies can be derived. In fact, this concept can be extended to most S^2 PFC converters, which adopted a DCM boost converter as the PFC function cell. Several derived example circuits are demonstrated in [24,25].

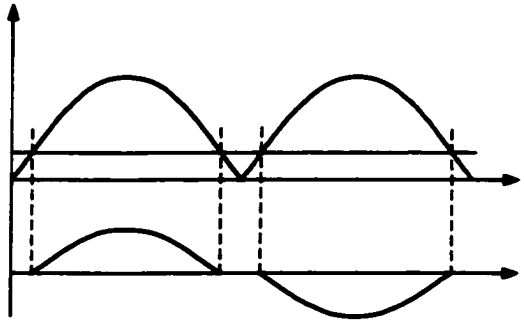
However, the penalty is, while obtaining low bus voltage, that input current waveform is deteriorated because of the reduced conduction angle resulted from the feedback winding, and this drawback limits its application in practical S^2 PFC AC-DC conversion.

4.3.3 Utilizing Buck Topology

Shown in Fig. 4-6 is a buck-based S^2 PFC converter. In this scheme, the DC-bus voltage can be greatly reduced at light load since the output voltage of the buck converter is always lower than the input voltage. However, the reduced conduction angle is introduced when the line voltage is lower than the voltage across the bulk capacitor, which inherently leads to current harmonics and a reduced power factor.



(a) Topology



(b) Operation modes of C_s in one line cycle

Fig. 4-6 Buck based S^2 PFC converter

4.4 Control Schemes to Alleviate Bus Voltage

4.4.1 DCM + CCM combination with variable frequency control

This scheme was proposed in [18]. Since the gain of the CCM DC-DC stage depends only on the duty-cycle, and the gain of the DCM boost input block depends on the frequency rather than duty-cycle, it is possible, for the DCM boost input block to regulate the capacitor voltage (without affecting the output) by a variable-frequency control. That is to say, the input power of PFC block is inversely proportional to the switching frequency at DCM with a constant duty ratio, and the unbalanced power between the input and output decreases with the increasing of switching frequency. This scheme is proven effective to resolve the bus voltage stress problem. The drawback of this approach is that large load variation range results in large range of variation in switching frequency. For a load change from full to 10% of the rated load, the switching

frequency has to be as 10 time as that of the full load to remain the same bus voltage. Such wide switching frequency variation makes it difficult to optimize the inductive components of the converter. In practical circuits, the frequency range is smaller than the theoretically calculated one because 100% efficiency is assumed in theoretical analysis.

4.4.2 Both Functional Blocks Operate under Same Mode

As discussed in the last section, power unbalance in the combination DCM + CCM will cause high voltage stress on the intermediate DC-bus. However, there is no DC-bus voltage stress problem in combinations of same operating mode, either in DCM or in CCM for the two functional blocks, i.e., DCM + DCM and CCM + CCM. Taking DCM + DCM for example, the duty-cycles of the two blocks in Fig. 4-2 will simultaneously decrease with the load becoming light. As a result, the input power also decreases with output power because of decreased duty-cycle. There is no unbalanced power between the input and the output. Power balance relationship is similar in CCM + CCM combination. Thus it is concluded that there is no DC-bus voltage issue, for both functional blocks operate under the same mode with proper circuit design.

Both functional blocks operate under the same mode, i.e., (DCM PFC+ DCM DC-DC) and (CCM PFC + CCM DC-DC) combinations are practical solutions. However, the former takes a low efficiency because of higher conduction loss and turn off switching losses; the latter, generally speaking, has relatively lower power factor and higher distortion in input current.

4.4.3 Proposed critical DCM + CCM Operation Mode

If the DC-DC stage operates in DCM at light load, the CCM at heavy load can also limit the DC-bus voltage stress. This statement will be verified through the next theoretical analysis of an example circuit.

Figure 4-7 shows the operation waveform of a boost inductor in Fig. 4-4, and, as it can seen, the input peak current in each switching can be expressed as:

$$I_{pk} = \frac{V_{in} Sin\omega t}{L_1} dT_s$$

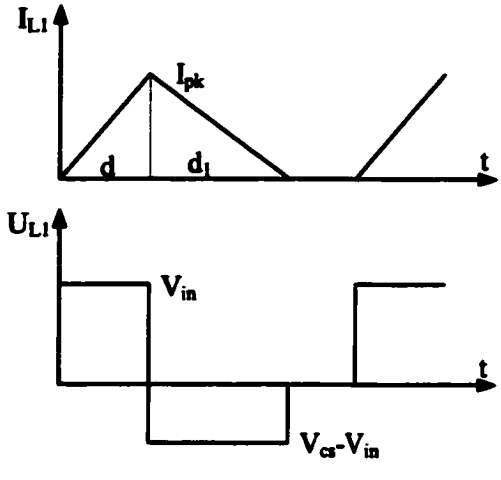


Fig. 4-7 Operation waveform of boost inductor in Fig. 4-4

The demagnetizing duration is:

$$d_1 = \frac{V_{in} \sin \alpha t}{V_{cs} - V_{in} \sin \alpha t} d$$

So, the average input current in one switching cycle can be expressed:

$$I_{avg} = \frac{1}{2}(d + d_1) I_{pk} = \frac{V_{ca} \cdot V_{in} \sin \omega t \cdot d^2 T_s}{2L_1 (V_{ca} - V_{in} \sin \omega t)} \tag{4-1}$$

Let $m_1 = \frac{V_{ca}}{V_{in}}$, then,

$$P_{in} = I_{avg} I_{in} = \int_0^{\frac{T}{2}} \frac{V_{ca} \cdot V^2_{in} \sin^2 \omega t \cdot d^2 T_s}{2L_1 (V_{ca} - V_{in} \sin \omega t)} dt = \frac{d^2 T_s V^2_{in}}{2\omega L_1} \int_0^{\pi} \frac{\sin^2 x}{1 - \frac{1}{m_1} \sin x} dx$$

$$= P_{out} = \frac{1}{\eta} \frac{T}{2} \frac{V_0^2}{R_L} = \frac{1}{\eta} \frac{\pi}{\omega} \frac{V_0^2}{R_L}$$

After integration,

$$\frac{2m_1}{\sqrt{m^2_1 - 1}} \left(\frac{\pi}{2} + arctg \frac{1}{\sqrt{m_1^2 - 1}}\right) - \pi - \frac{2}{m_1} = f(m_1) = \frac{1}{m^2_1} \frac{\pi n^2 V_0^2}{\eta D^2 V^2_{in}} \frac{2L_1}{n^2 R_L T_s} \tag{4-2}$$

Let $m_2 = \frac{V_0}{V_{ca}}$, then:

Choose L_2 to operate in CCM, so: $m_2 = D$

$$V_0^2 = \frac{m_1^2 m_2^2 V_{in}^2}{n^2} = \frac{m_1^2 D^2 V_{in}^2}{n^2}$$

And,

$$f(m_1) = \frac{2\pi}{\eta} \frac{L_1}{n^2 R_L T_s} \tag{4-3}$$

Choose L_2 to operate in DCM, $m_2 = \frac{2}{1 + \sqrt{1 + \frac{4k}{D^2}}}$, where $k = \frac{2L_2}{R_L T_s}$

Then,

$$f(m_1) = \frac{m_2^2}{D^2} \frac{2\pi}{\eta} \frac{L_1}{n^2 R_L T_s} = \frac{4}{\left(D + \sqrt{D^2 + \frac{8L_2}{R_L T_s}}\right)^2} \cdot \frac{2\pi}{\eta} \frac{L_1}{n^2 R_L T_s} \tag{4-4}$$

Thereafter the DC-bus voltage in different operation modes can be derived from the above analysis. Fig. 4-8 shows a design example, in which Vcs are given under different R_L in two operation modes.

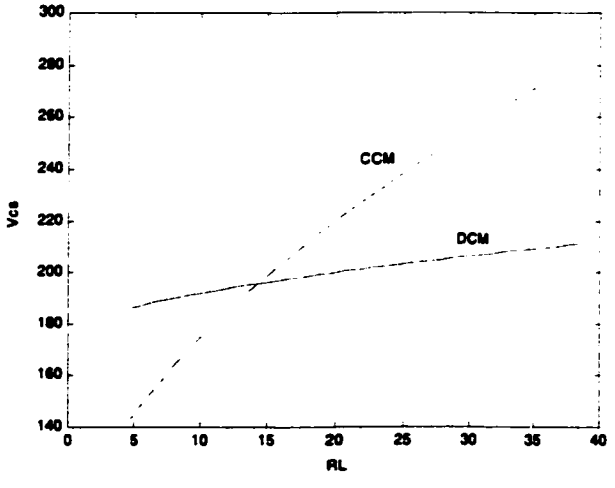
Critical value for L_1 and L_2 are also given as following:

For L_1, because at critical point, $m_1 = \frac{1}{1-D}$

And due to $\frac{V_0}{V_{in}} = \frac{V_0}{V_{cs}} \cdot \frac{V_{cs}}{V_{in}} = \frac{m_2}{1-D}$

So from expression (1), we can get:

$$k = \left(\frac{2}{\sqrt{D(2-D)}}\left(\frac{\pi}{2} + actg\frac{1-D}{\sqrt{D(2-D)}}\right) - \pi - 2(1-D)\right) \cdot \frac{\eta D^2}{\pi m_2^2} \qquad (4\text{-}5)$$



$(\eta = 0.75, f_s = 500KHz, L_1 = 30uH, L_2 = 10uH, D = 0.3, n = 3)$

Fig 4-8 Calculated curve of Vcs versus R_L

For L_2,

From $I_{L2,avg} = \frac{nV_{cs} - V_0}{2L_2} DT_s = \frac{V_0}{R_L}$

And critical operation condition, $V_0 = D \cdot nT_s$

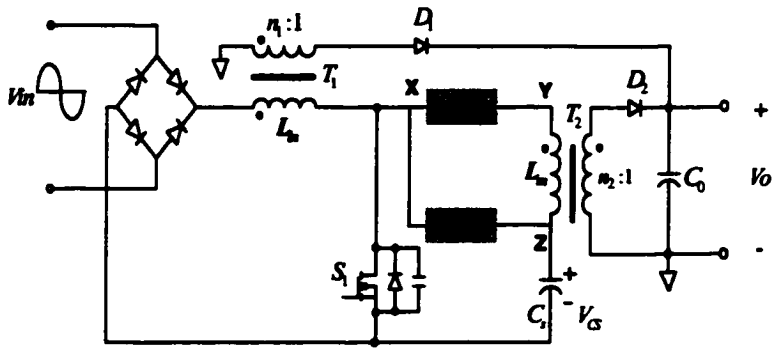
$$k = \frac{2L}{R_L T_s} = \frac{(1-D)nV_{cs}}{nV_{cs}} = 1 - D \qquad (4\text{-}6)$$

From the analysis above, it's not difficult to conclude such operation conditions need fine tuned parameters, and therefore, also impractical in quantity manufacturing.

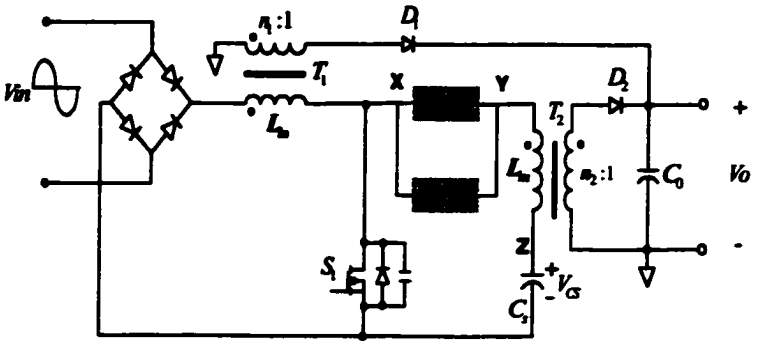
4.5 Voltage Clamping Scheme

4.5.1 Conceptual Overview

Shown in Fig. 4-9 is the configuration of a Fly-boost PFC AC-DC converter, using a Flyback transformer replace the traditional boost inductor in a generalized S^2 PFC AC-DC scheme with a three-terminal cell or two-terminal cell.



(a) Three-terminal scheme



(b) Two-terminal scheme

Fig. 4-9 Voltage claming PFC scheme with flyboost transformer

During the ON interval, the proposed scheme works in the same mode as previous approaches: Flyback transformer acts as a traditional boost inductor, and energy in storage capacitor C_s is discharged through the DC-DC conversion cell.

During the OFF interval, due to the huge capacitance of the output capacitor, the primary voltage of the Flyback transformer T_1 is clamped to n_1V_0. Therefore,

For a single-stage PFC scheme with a three-terminal cell, as shown in Fig. 4-9(a),

$$V_X \le V_{in} + n_1V_0 \qquad (4\text{-}7)$$

$$V_Z \le V_X \qquad (4\text{-}8)$$

For a single-stage PFC scheme with a two-terminal cell, as shown in Fig. 4-9(b),

$$V_X \le V_{in} + n_1V_0 \qquad (4\text{-}9)$$

$$V_Z \le V_X - n_2V_0 = V_X + (n_1 - n_2)V_0 \qquad (4\text{-}10)$$

Therefore, theoretically, for both three-terminal schemes and two-terminal schemes, the introduction of a flyback transformer brings about inherent voltage clamping capability for the bulk capacitor.

Comparing the voltage expression in (4-8) and (4-10), an exciting case came up here. In schemes with a two-terminal cell, V_z can be designed to any desired value by properly choosing n_1 and n_2, which are turn ratios of transformers T_1 and T_2, respectively.

In Fig. 4-9(b), after merging the charging and discharging path, a bi-directional DC-DC cell with an input Flyback transformer constitutes the simplest configuration, as shown in Fig. 4-10. In practical applications, the voltage across the bulk capacitor should be higher than the input voltage from the view of demagnetizing of the input Flyback transformer. Therefore, a forward diode from the bridge rectifier is connected straight to the positive terminal of the bulk capacitor, keeping its voltage always above the input voltage to obtain the minimum input current distortion, as shown in Fig. 4-10.

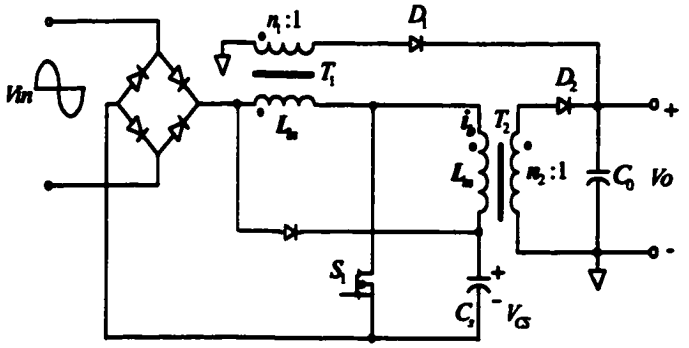


Fig. 4-10 Proposed PFC AC-DC Configuration

4.5.2 Proposed Practical Cost-effective Topology

The practical S^2 PFC AC-DC converter, as shown in Figure 4-11(a), basically is derived from the topology as shown in Fig. 4-10. The input PFC inductor is replaced with a Flyback transformer T_1 and a small boost inductor L_1, in practical applications. L_1 can be designed as the leakage inductance of transformer T_1. An additional winding N_a of DC-DC transformer T_2 and a small capacitor C_1 are introduced to constitute a lossless snubber, to reduce the main switch turn-off spike resulted from the leakage inductances.

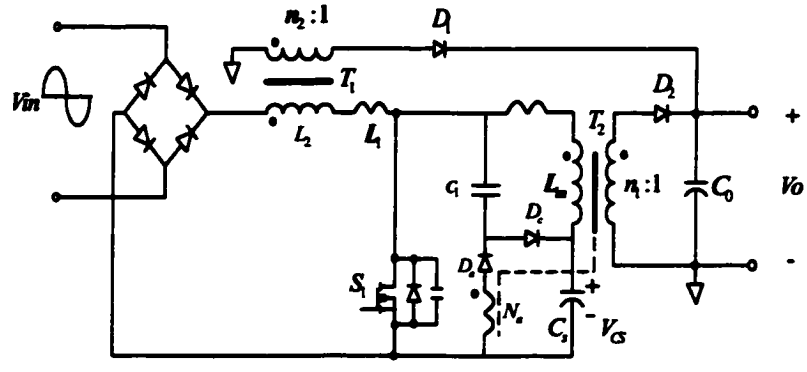


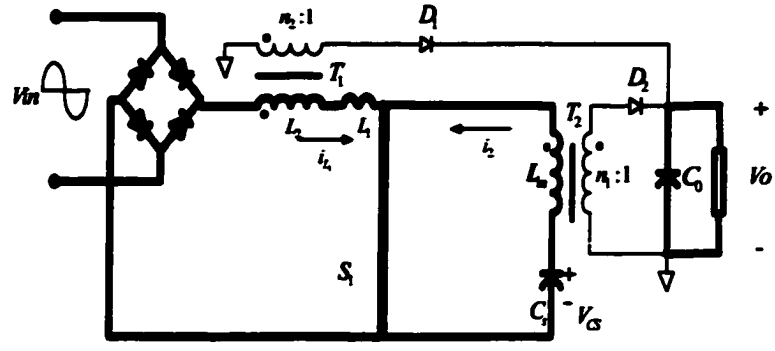
Fig. 4-11 Proposed Topology

4.5.3 Operation Principle and Basic Relationship

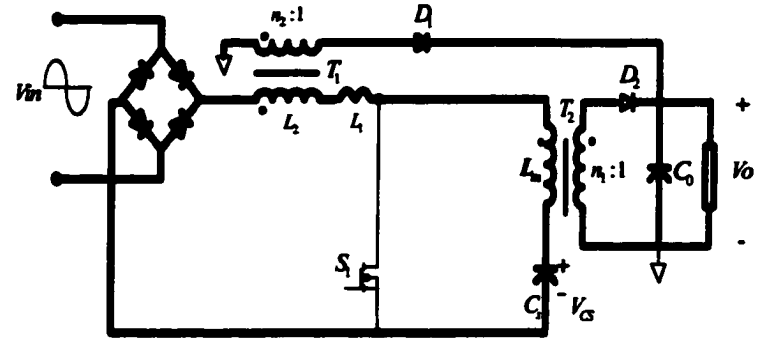
4.5.3.1 Operation Principle

The circuit operation will be discussed for one arbitrarily chosen switching cycle Ts, and under assumption that all components are ideal. And to simplify the analysis, lossless snubber branch constituted by C_1, N_a, D_c and D_a, is also neglected here.

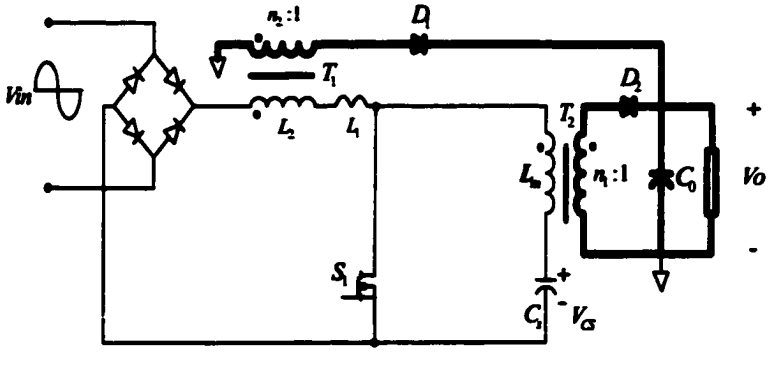
The switching cycle Ts is divided into four intervals corresponding to different circuits shown in Fig. 4-12 (a)-(d). The key waveforms are shown in Fig. 4-13.



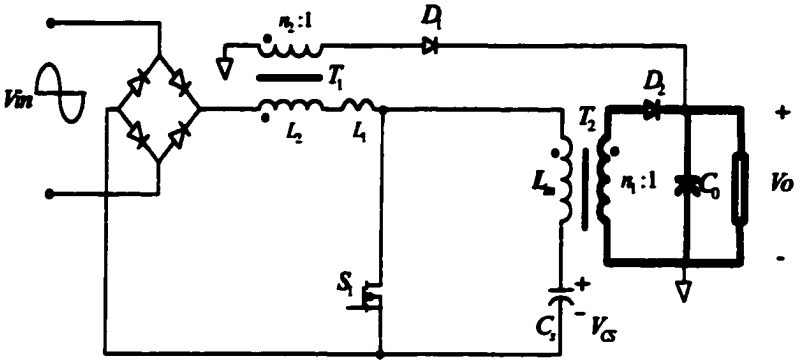
(a) Interval [t0 –t1]



(b) Interval [t1 –t2]



(c) Interval [t2 –t3]



(d) Interval [t3 –t0 +Ts]

Fig. 4-12 Operation Modes of four intervals in one switching cycle

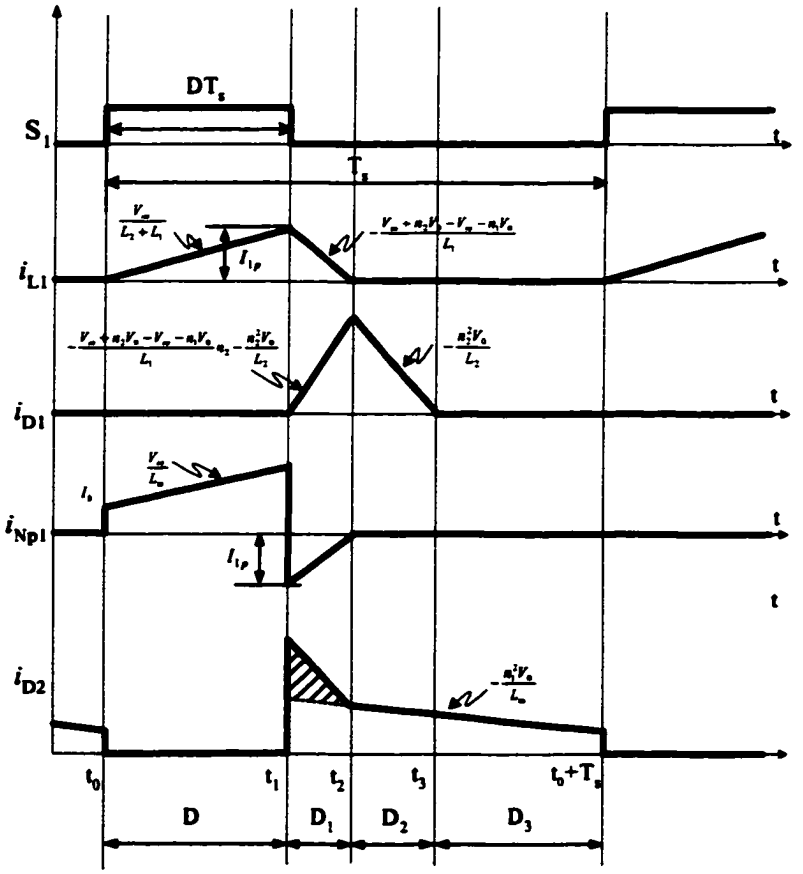


Fig. 4-13 Idealized Key waveforms in one switching cycle

Interval 1 [t0~t1]: At t0, the active switch is turned ON, the input voltage Vin is applied to the Flyback transformer T_1 and inductor L_1, and the current i_{L_1} starts to build up linearly from zero. At the same time, the intermediate capacitor voltage V_{cr} is applied to the primary winding of transformer T_2, which also resulted in its current increase linearly.

Interval 2 [t1~t2]: When the switch is turned OFF at t1, the current i_{L_1} begins to flow through the primary winding of transformer T_2. The energy stored in the Flyback transformers T_1 and T_2 start to be discharged to the output. This interval ends at t2 when i_{L_1} reaches zero.

Interval 3 [t2~t3]: From moment t2, the current flowing through D_2 decreases linearly with a slope $\frac{n_1^2 V_0}{L_m}$; and also the current flowing through D_1 decays with the slope $\frac{n_2^2 V_0}{L_2}$ until it reaches zero at t3.

Interval 4 [t3~t0+Ts]: The current flowing through D_2 keeps gradually decreasing with a slope $\frac{n_1^2 V_0}{L_m}$ until the switch is turned ON, starting another switching cycle at t0+Ts.

Based on the above basic operation, we can formulate some basic equations. It can be shown that the average value of the input current i_{L_1}, denoted as $\bar{i}_{L_1}$, over the switching cycle Ts is given by:

$$\bar{i}_{L1} = \frac{D+D_1}{2} I_p = \frac{D+D_1}{2} \frac{|V_{in}|}{L_1+L_2} DT_s \tag{4-11}$$

where the duty ratio D_1 can be found from the voltage balance on L_1 as:

$$D_1 = \frac{L_1|V_{in}|D}{(V_{cr}+n_1V_0-n_2V_0-|V_{in}|)(L_1+L_2)} \tag{4-12}$$

Combining Eqs. (4-11) and (4-12) and by letting:

$A = V_{cr}+n_1V_0-n_2V_0-|V_{in}|$, $m = \frac{L_2}{L_1}$ and,

$|V_{in}| = \sqrt{2}V_{rms}|\sin\theta|$, $\bar{i}_{L_1}$ can be rearranged as:

$$\bar{i}_{L1} = \frac{D^2|V_{in}|T_s}{2L_1(1+m)}\left(1+\frac{|V_{in}|}{A(1+m)}\right) \tag{4-13}$$

Similarly the average value of the output current i_{D_1} over Ts can be found from:

$$\bar{i}_{D_1} = \frac{D_1+D_2}{2} I_{p2} = \frac{D_1+D_2}{2} n_2 \frac{(mA-n_2V_0)DT_sV_{in}}{Am(1+m)L_1} \tag{4-14}$$

where D_2 can be found from:

$$D_2 = \frac{mA-n_2V_0}{n_2V_0} D_1 \tag{4-15}$$

Combining Eqs. (4-12), (4-14) and (4-15), $\bar{i}_{D_1}$ can be rearranged as:

$$\bar{i}_{D_1} = \frac{|V_{in}|^2 D^2 T_s}{2A(1+m)^2 L_1} \frac{(mA-n_2V_0)}{V_0} \tag{4-16}$$

To implement a commercially available capacitor and its related voltage rating components, now take the voltage across the bulk capacitor as a design parameter. The averaged bulk capacitor charging current over Ts can be expressed as:

$$\bar{i}_{charge} = \frac{1}{2} D_1 I_p = \frac{|V_{in}|^2 D^2 T_s}{2AL_1(1+m)^2} \tag{4-17}$$

And discharging current can be found by subtracting the current flowing in D_1 and the shadowed current of D_2 in Fig. 4-12 from the load current to yield,

$$\bar{i}_{discharge} = \frac{D}{n_1}\left(\frac{P_0}{V_0} - \bar{i}_{D_1} - \bar{i}_{D_2}\right) = \frac{D}{n_1}\left(\frac{P_0}{V_0} - \frac{|V_{in}|^2 D^2 T_s (mA - n_2 V_0)}{2A(1+m)^2 L_1 V_0} - \frac{n_1 |V_{in}|^2 D^2 T_s}{2A(1+m)^2 L_1}\right) \tag{4-18}$$

In steady state, over half a line cycle, the net charging current for the bulk capacitor should be zero, thus:

$$\int_0^{\pi} \bar{i}_{charge} d\theta = \int_0^{\pi} \bar{i}_{discharge} d\theta \tag{4-19}$$

From Eqs. (4-17), (4-18) and (4-19), we obtain the following equation:

$$\int_0^{\pi} \left(\frac{D^2 T_s}{2AL_1(1+m)^2}\left(1 + \frac{D}{n_1}\frac{(Am - n_2 V_0)}{V_0} + D\right)|V_{in}|^2 - \frac{DP_0}{n_1 V_0}\right) d\theta = 0 \tag{4-20}$$

where P_0 is the output power, since input power is equal to the output power, so:

$$P_0 = P_{in} = \frac{1}{\pi}\int_0^{\pi} \bar{i}_{L1} |V_{in}| d\theta$$

$$= \frac{1}{\pi}\int_0^{\pi} \frac{D^2 T_s}{2L_1(1+m)}\left(1 + \frac{|V_{in}|}{A(1+m)}\right)|V_{in}|^2 d\theta \tag{4-21}$$

Combining Eqs. (4-20) and (4-21) to yield the following transcendental equation set:

$$\int_0^{\pi}\left(1+\frac{n_1V_0-DV_{cr}}{D(V_{cr}+(n_1-n_2)V_0)(1+m)-\sqrt{2}mV_{rms}\sin\theta}\right)d\theta=1$$

$$\int_0^{\pi}\frac{V_{rms}^2D^2T_s\sin^2\theta}{L_1(1+m)}\left(1+\frac{\sqrt{2}V_{rms}\sin\theta}{(1+m)(V_{cr}+(n_1-n_2)V_0-\sqrt{2}V_{rms}\sin\theta}\right)d\theta=\pi P_0 \qquad (4\text{-}22)$$

That allows us to find numerically the voltage across the bulk capacitor as a function of the *rms* value of input voltage and the output voltage V_0 as well as turn ratios n_1, n_2 and $m=\frac{L_2}{L_1}$.

4.5.3.2 DCM operation of PFC cell

As explained in the modes analysis, if Flyback transformer T_1 is not completely reset during the OFF state of the main switch, the distortion of the line current will dramatically increase. In other words, to obtain a line current close to a sinusoidal waveform under entire line and load conditions, the diode current i_{D_1} should be decreased to zero before the main switch conducts. Since the worst case happens at a full load and minimum line voltage, the DCM condition of i_{D_1} can be found from Fig. 4-13:

$$D_1+D_2\le 1-D_{max} \qquad (4\text{-}23)$$

From (4-12) and (4-15), (4-23) can be derived as:

$$D_{max}\left(\frac{m|V_{min}|}{n_2V_0(1+m)}+1\right)\le 1 \qquad (4\text{-}24)$$

Therefore, the maximum duty ratio must be designed to meet (4-24) to guarantee no serious input current distortion happens under any case.

Topology Features

From the above analysis, we can summarize the features of the proposed topology:

1. Reduced voltage stress: Inserting a Flyback transformer to the traditional input inductor brings about inherent voltage clamping capability across its primary when the switch is OFF. Besides, the storage capacitor is always charged through the transformer T_2, therefore, if L_1 is much smaller than L_2, the storage capacitor is charged in an apparent controlled mode, $V_{cs} \le V_{in} + (n_2 - n_1)V_0$. Properly selected n_1, n_2 and m can guarantee the DC-bus voltage well above the peak value of the input voltage. As a consequence, the commercially available capacitor can be used, and moreover, 600V components can be used in the power stage for universal input applications.

2. Higher efficiency: In Fig. 4-12, the current flowing through D_1 and the shadowed portion of D_2 is directly delivered to the output through T_1 and T_2 without storing in C_s first. Therefore, a lion share power was transferred to the load without being processed twice. The overall conversion efficiency can be improved consequently. For the currently existing cascade two-stage or single-stage approaches, basically, the power is processed serially by PFC cell and DC-DC cell, and the overall efficiency is given by the product of two stage efficiencies,

i.e., $\eta = \eta_1 \eta_2$, where η_1 and η_2 are the efficiencies of two stages respectively. In the proposed topology, supposing k is the ratio at which power is transferred to the output just through the PFC stage, then, the efficiency of the proposed structure can be expressed as $\eta = k\eta_1 + (1-k)\eta_1\eta_2 > \eta_1\eta_2$. Obviously the overall efficiency can be improved by minimizing the power process times. In addition, reduced current stress also brings about higher efficiency due to reduced turn off losses.

3. Reduced current stress: It can be shown from i_{D_2} in Fig. 4-12, that the existence of interval D_2 will decrease the duty cycle when line voltage nears its peak value, and thus can effectively reduce the peak value of input current when transferring the same average input current. Therefore, the main switch can be turned OFF under reduced current stress.

4. Low turn off spikes: The snubber capacitor C_1 can effectively suppress the turn off spikes of the main switch, and in each switching cycle, its stored energy can also be released to the output through the coupling winding at the moment of the main switch being turn ON.

5. High power application potential: Two Flyback transformer configuration has the potential to increase the power conversion rating and also release the thermal design difficulties due to distributed heat dissipation.

6. In addition, reduced cost and improved reliability due to least components are also preferred in practical applications.

4.5.4 Simulation and Experimental Results

In order to verify the above analysis, a 20V@4.5A PSPICE closed loop simulation circuit is built up as shown as Fig. 4-14.

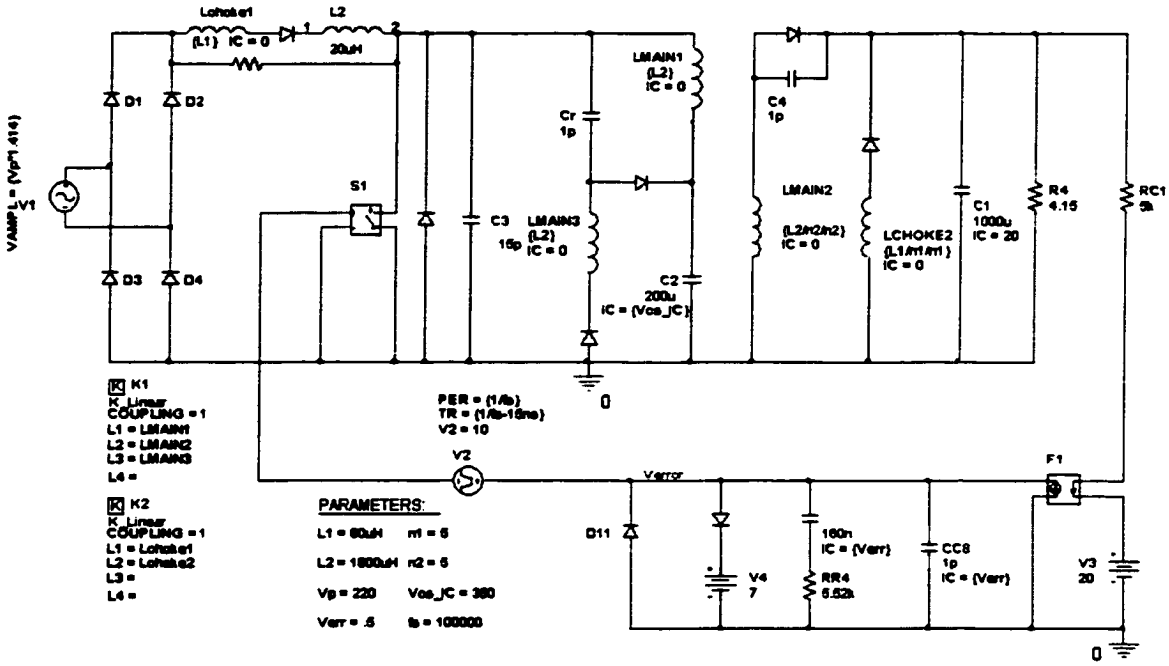


Fig. 4-14 Simulation Schematics

Figure 4-15 presents the simulation results for the proposed topology. Figure 4-15(a) gives the simulated key waveforms in one line cycle:

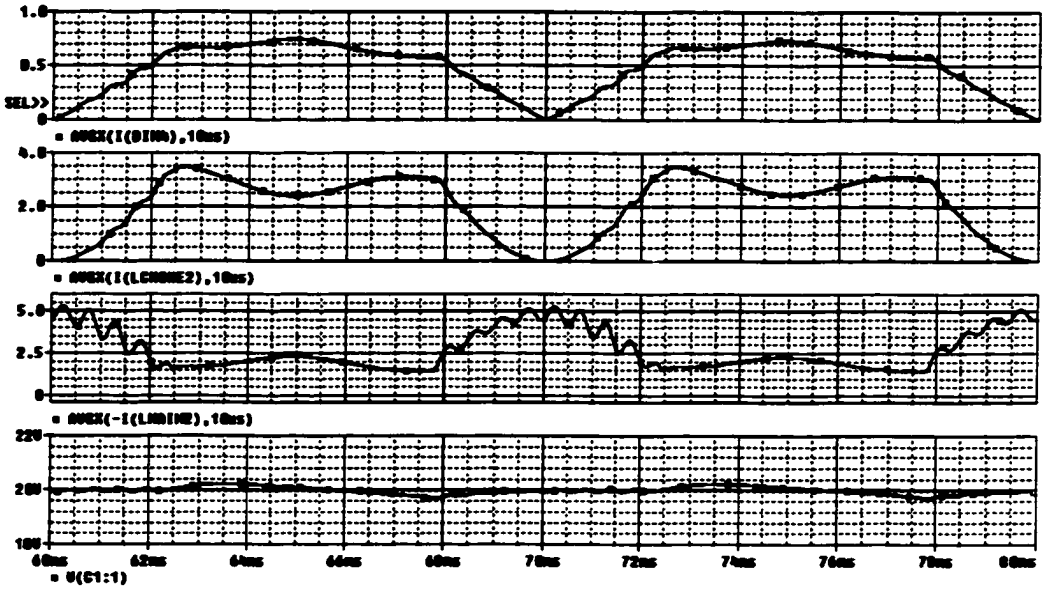
The first trace shows the rectified input current, which is nearly sinusoidal waveform with lower crest value. It should be noted here that the practical waveform would be better since the input filter has not been implemented in front of the presented simulation scheme.

The second trace indicates the current transferred to the output through T1, resulting in more than 50% energy delivered to the output directly without being processed twice, as previous approaches did.

The third trace indicates current transferred to the output through T2, which just fills the valley of the second current trace to pursue the trade-off between the high power factor and low output ripple; It also can be seen only a small output portion powered by the buffer capacitors.

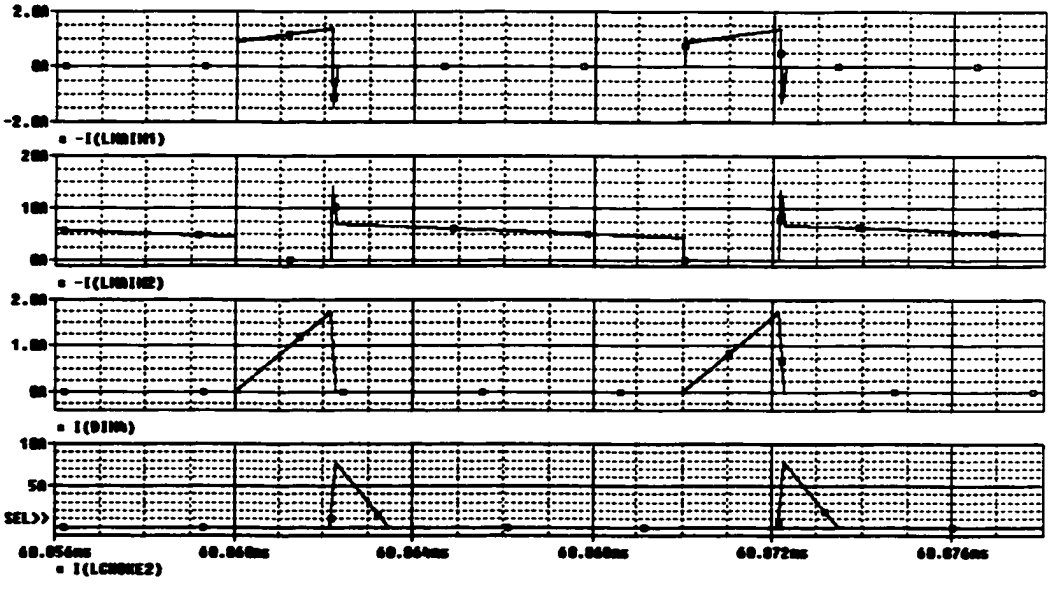
The last trace gives the output voltage to indicate the proposed power conversion scheme can obtain pretty small output ripple with near unity power factor.

Figures 4-15(b) and (c) show the current flowing through the primary and secondary windings of two transformers in one switching cycle for the input line across zero and near peak value, respectively. It can be found that the waveforms agree well with the above analysis. For the bulk capacitor, in half a line cycle, it exhibits net discharge performance in one switching cycle around line voltage across zero, and net charge performance near line voltage near the peak.

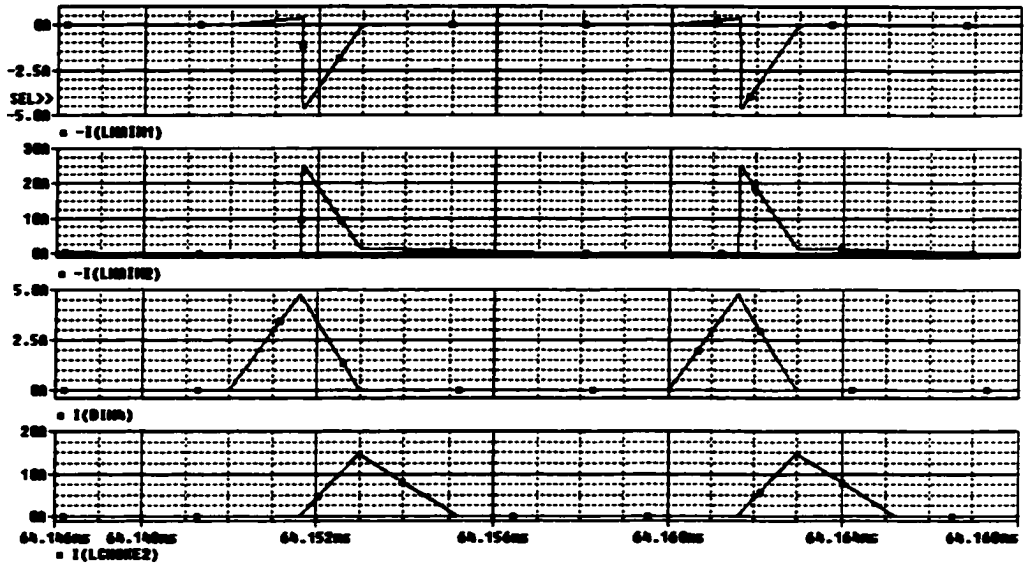


- *First trace: Rectified input current;*
- *Second trace: Current transferred to the output through T1;*
- *Third trace: Current transferred to the output through T2;*
- *Fourth trace: Output Voltage*

(a) Simulated waveforms over one line cycle



(b) Windings current around line voltage across zero



(c) Windings current around line voltage near the input peak value

Fig. 4-15 Simulation results

A 90~265V/60Hz input, 20V@4.5A output prototype was built to experimentally verify the proposed scheme, as shown in Fig. 4-16. The following key components were implemented in the experimental circuit: Flyback transformer T1: n2=4.1/L2=80uH/L1=23uH; DC-DC transformer T2: Np:Ns:Na = 4.1:1:4.1; Switches— S1: IRF9N65; Storage Capacitor — 100uF/450V; Clamp capacitor — 4.7n; Boost Diode — DSEI 806A; Secondary rectifier diode D1, D2 — 10CT150; Switching frequency — 100kHz.

Figure 4-17 presents the waveforms under full load and nominal input (110V/60Hz) condition. The upper trace indicates the prototype achieved near sinusoidal input current waveform.

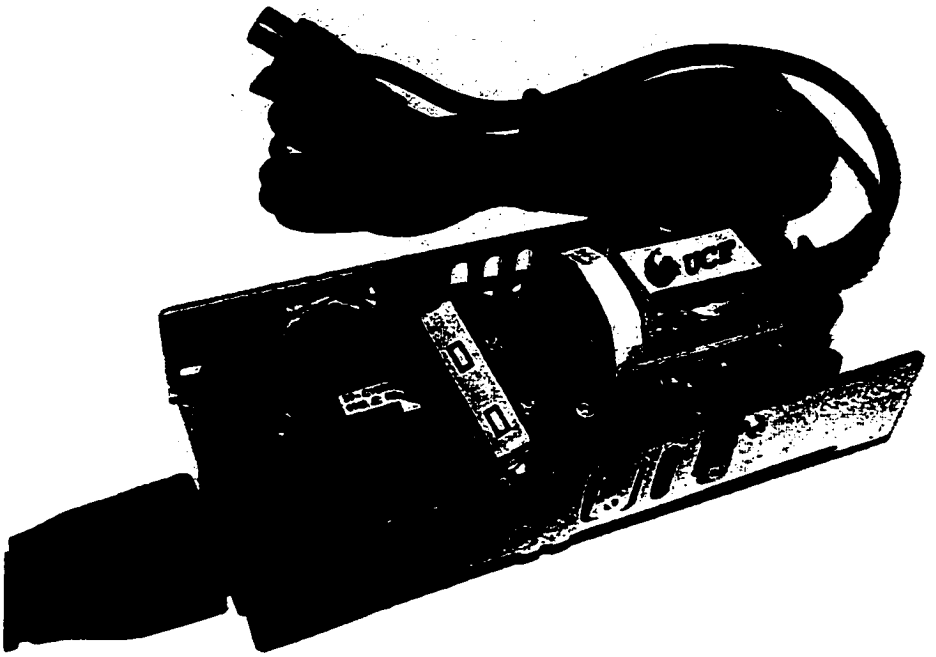


Fig. 4-16 Universal input 20V@4.5A Adapter prototype

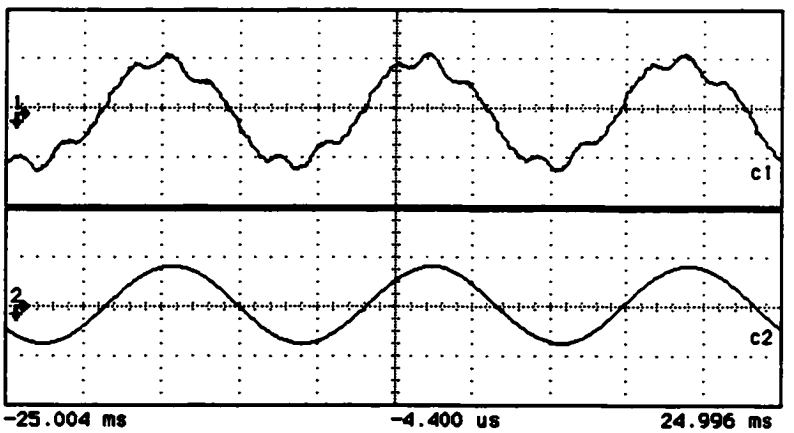


Fig. 4-17 Measured line current and voltage

Figures 4-18 and 4-19 present the full load efficiency and power factor under different input voltage, respectively. The results indicate the efficiency stays above 81% and the Power Factor of the developed prototype stays above 0.95 through the entire

input range. Figure 4-20 indicates the DC bus voltage is well below 400V through the universal input range, which makes the commercial available capacitor practical in this adapter.

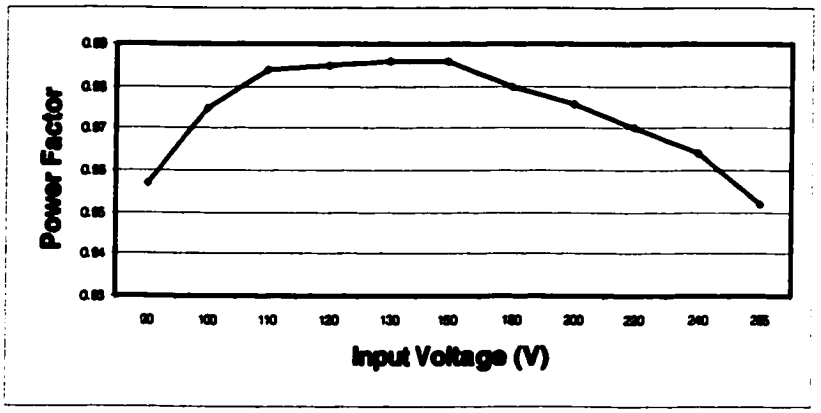


Fig. 4-18 Measured power factor vs. line voltage under full load

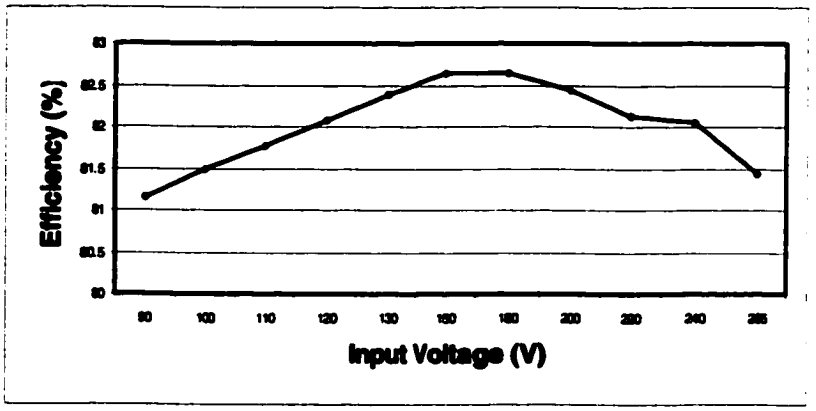


Fig. 4-19 Measured efficiency vs. line voltage under full load

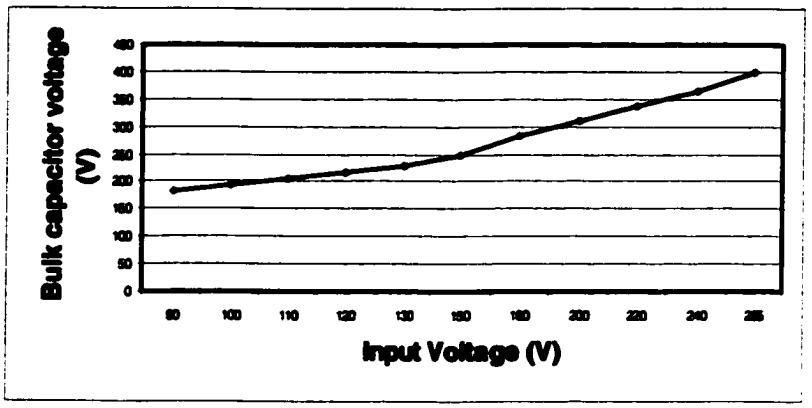


Fig. 4-20 Maximum voltage vs. line voltage under full load

4.5.5 Topology Derivation

The DC-DC transformer in the proposed topology can also be designed to have another forward winding, as shown in Fig. 4-21. The modified topology can reduce the secondary current stress and further improve the conversion efficiency, in addition to still keeping the inherent DC-bus voltage claming capability.

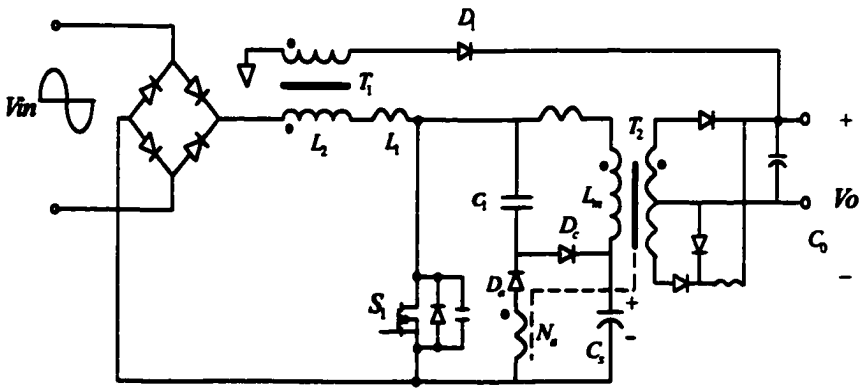


Fig. 4-21 Topology derivation

4.6 Summary

This chapter first analyzes the mechanism of high intermediate DC-bus voltage, and after briefing existing stress-alleviating approaches, a simple inherent voltage clamping scheme for S^2 PFC AC-DC conversion is introduced. A practical application topology was proposed, analyzed and used to experimentally validate the concept.

5. CURRENT STRESS ALLEVIATING APPROACHES

5.1 Introduction

The PFC stage in an S^2 PFC AC-DC converter normally operates in DCM mode to utilize its inherent current-shaping capability. Therefore, compared with cascading two-stage schemes, S^2 PFC AC-DC conversion has higher current stress. Current stress not only accompanies with increased switching losses and lower efficiency, but also brings about annoying EMI issues. Pursuing a current alleviating scheme will "kill two birds with one stone" to increase the power conversion efficiency, and help to release the pressure of the S^2 PFC AC-DC converter EMI filter design.

As stated in the first chapter, it is not necessary to achieve sinusoidal input current waveform to meet the regulations. Non-sinusoidal approach sometimes is a better choice in terms of performance and cost. In this chapter, three near sinusoidal input current approaches are introduced to alleviate current stress, thereafter to pursue the better trade-off quality-cost performance.

5.2 Peak Value Clamping Technique

Figure 5-1 shows three different types of line current waveforms with various distortions. It is known that waveform A exists in traditional converters composed of a diode bridge and a filter capacitor. This waveform fails to meet the regulations due to its high harmonic current. Whereas, the sinusoidal waveform B represents the ideal case that

guarantees the converter's compliance with any national and international regulation. Such converters usually involve a high cost and complex circuitry. Finally, the flat top current waveform C, from mathematic calculation, as shown in Fig. 5-2, is a near sinusoidal waveform; for the flat top current waveform the power factor can reach up to 0.98 with 0.7 height ratio. So if the power stage could realize flat top input current waveform, the power factor would still stay fairly high. Moreover, during the flat top interval, if the energy can be delivered directly to the output, then higher efficiency can also simultaneously be achieved since partial power being delivered to the output has only been processed once.

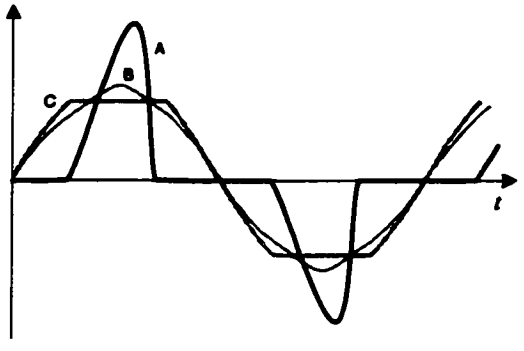
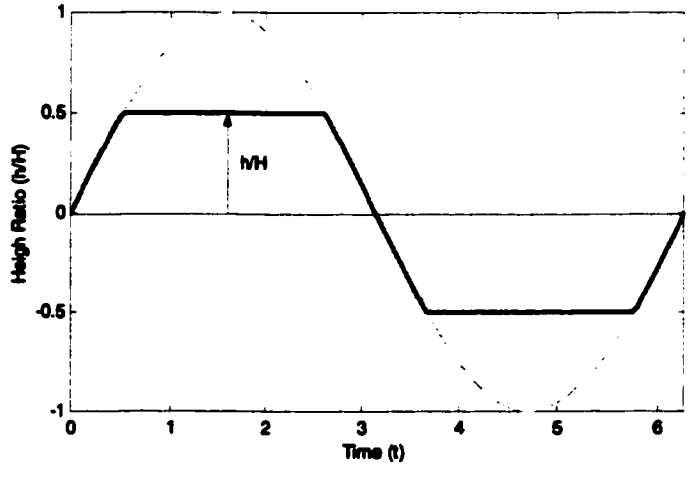
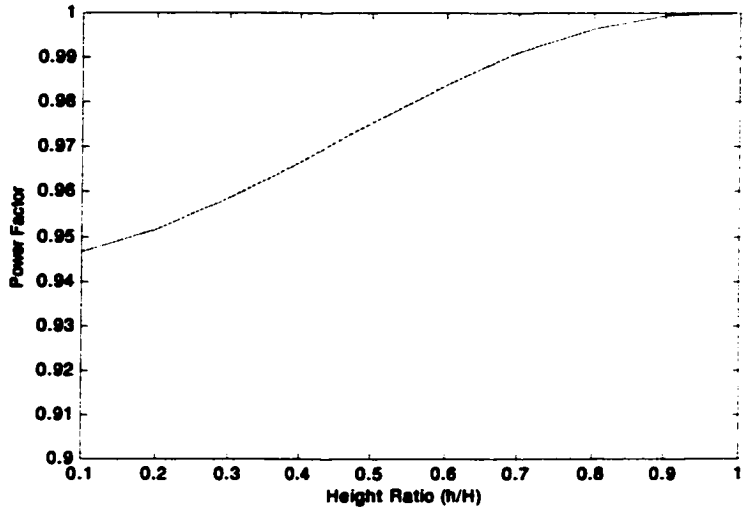


Fig. 5-1 Assorted input current waveform



(a) Flat-top current waveform, height ratio: h/H



(b) Power factor with different height ratio

Fig. 5-2 Current waveform with flat-top (a) and the power factor with different height ratio (b)

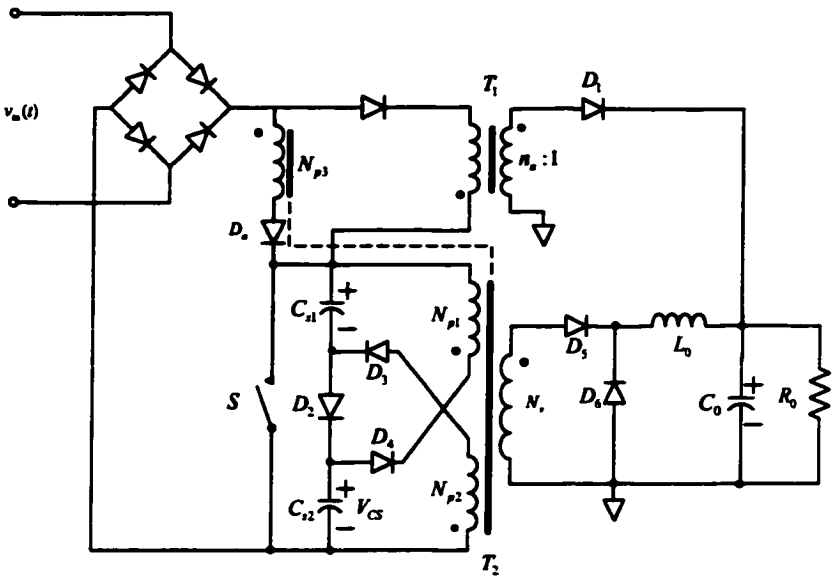
5.2.1 Proposed Topology and Operation Principle

Figure 5-3(a) embodies the proposed flat top input current and direct energy transfer concept with modified topology in [6]. An additional winding coupled with the main transformer connects the input line to the switch through a diode, and a Flyback transformer is implemented to replace the traditional boost PFC inductor, and thereafter suppress the voltage stress of the power stage.

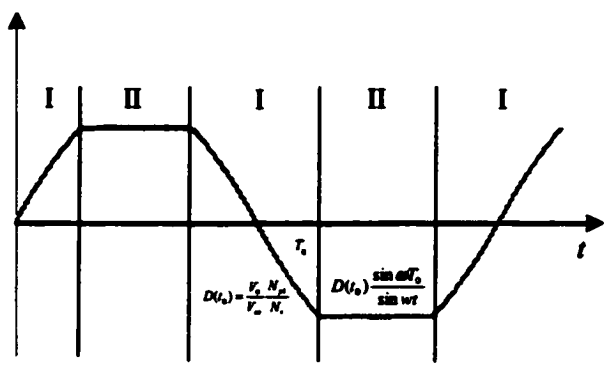
Figure 5-3(b) shows the operation cases of the proposed diagram. As it can be seen, the energy is transferred to the output in a hybrid case:

Case I: This case is subject to the following relationship:

$$V_{in} < \frac{N_{p3}}{N_{p2}} V_{cs}$$

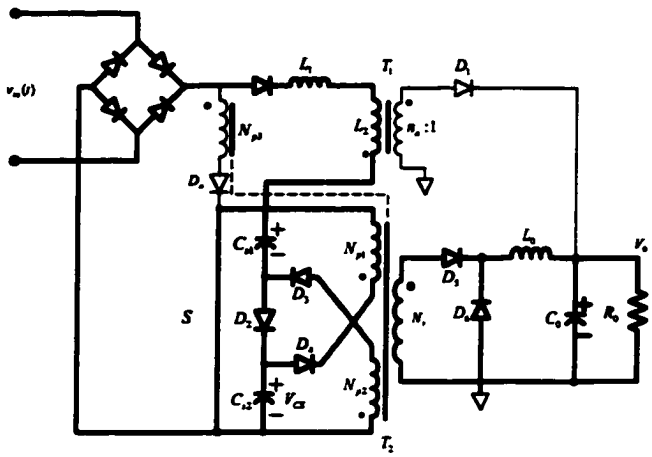


(a) Proposed Topology

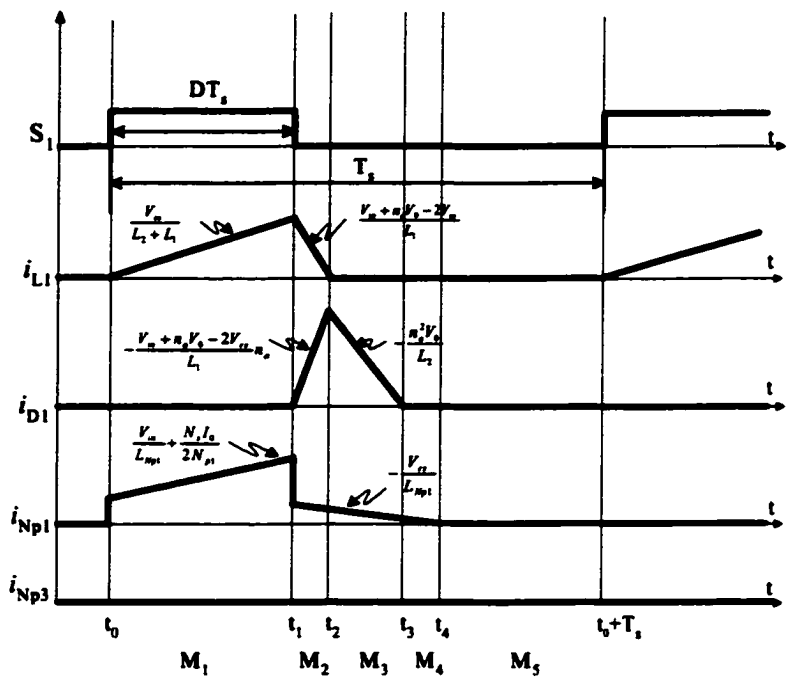


(b) Operation Cases

Fig. 5-3 Proposed topology and its operation case



(a) Switch ON in Case I



(b) Key waveforms in Case I

Fig. 5-4 Case I

Given this condition, when the switch is ON, winding Np3 will see no current since Da is reverse biased. The energy storage capacitors Cs1 and Cs2 power the output side through the winding Np1 and Np2, as shown in Fig. 5-4(a).

Due to the constant voltage across the energy storage capacitor, the duty cycle is also kept nearly constant. When the Flyback transformer operates in Discontinuous Current Mode (DCM), input current follows the input voltage, as shown in Fig. 5-3(b), achieving sinusoidal shape. The key waveforms are shown in Fig. 5-4(b), and the modes of operation are detailed as follows:

Mode 1 [t_0~t_1]: At t_0, the main switch is turned on and the current flowing through the Flyback transformer T1 and its leakage inductance increases as follows:

$$i_{L1} = \frac{V_{in}}{L_1 + L_2} t \tag{5-1}$$

where L_2 is the primary magnetizing inductance of T_2. Since the Flyback and forward stage share the same switch, the current in winding Np1, Np2 also increase linearly.

$$i_{Np1} = \frac{V_{cs}}{L_{Np1}} t + \frac{N_s I_0}{2N_{p1}} \tag{5-2}$$

where L_{Np1} and I_0 mean the primary magnetizing inductance of Np1 and output current, respectively.

Mode 2 [t_1~t_2]: Mode 2 begins when the switch is turned off at t_1. Current in Flyback transformer primary decrease linearly as follows:

$$i_{L1} = i_{L1}(t_1) + \frac{V_{in} + n_s V_0 - 2V_{cs}}{L_1} (t - t_1) \tag{5-3}$$

D1 carries the reflected current of L1 as given by:

$$i_{D1} = \frac{2V_{cr} - V_{in} + n_a V_0}{L_1} t \qquad (5\text{-}4)$$

and the forward transformer T2 enters into demagnetizing mode with the decaying slope:

$$i_{Np1} = i_m(t_2) - \frac{V_{cr}}{L_{Np1}}(t - t_2) \qquad (5\text{-}5)$$

Mode 3 [t_2~t_3]: Mode 3 begins when the current in L1 is reduced to zero. In this mode, the energy charged in the auxiliary transformer during Mode 1 continues to be transferred to the load.

The D1 see the current decays with the slope of $-n_a^2 V_0 / L_2$ from the initial current reflected to the Flyback transformer. It can be written as:

$$i_{D1} = n_a I_{L1}(t_2) - \frac{n_a^2 V_0}{L_2}(t - t_2) \qquad (5\text{-}6)$$

Mode 4 [t_3~t_4]: Only a small magnetizing current continues to flow in the primary windings Np1 and Np2, which finally vanish at t_4.

Mode 5 [t_4~t_5]: Between t_4 and t_5, the current in the circuit only existed in the output side, the free wheeling current in L0 and load current discharging the output capacitor.

Case II: This case is subject to the following relationship:

$$V_{in} \geq \frac{N_{p3}}{N_{p2}} V_{cr}$$

Given this condition, the key waveforms are shown in Fig. 5-5(b). All the modes, except for Mode I, are nearly the same as in Case I.

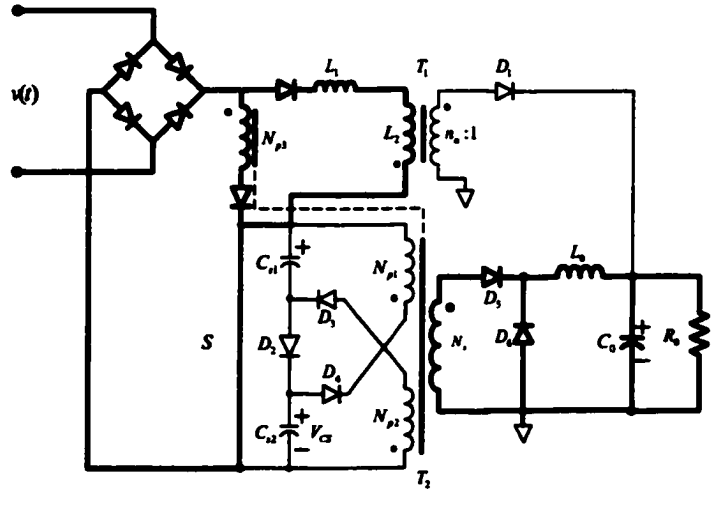
Mode 1 [t_0~t_1]: At t0, the main switch is turned on and the current flowing through Flyback transformer T1 and its leakage inductance increases in the same way as Eq. (1).

However, for the DC-DC transformer, only winding Np3 carries the current during this interval. Moreover, the input power is delivered directly to the secondary side. No current flows through primary windings Np1 and Np2 since D3 and D4 are reverse biased. The current in primary winding Np3 is given by:

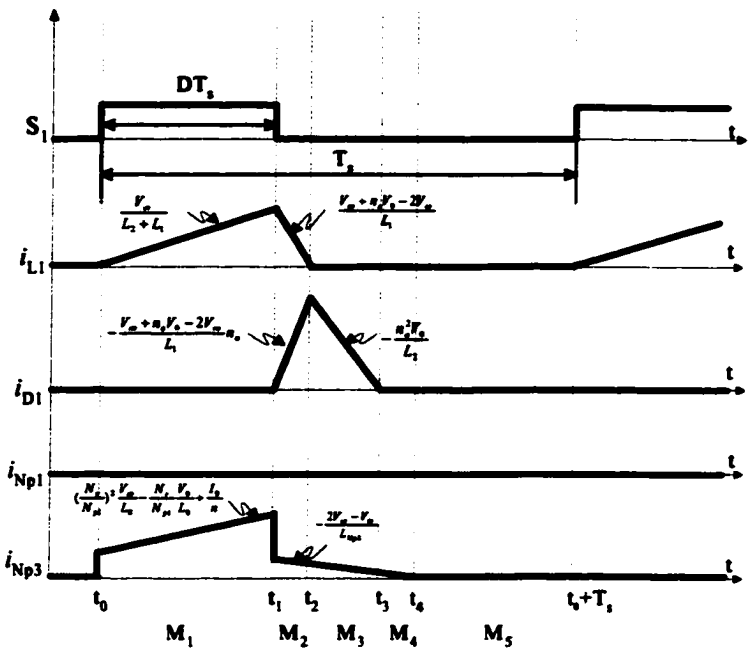
$$i_{Np3} = \frac{V_{in}}{L_{Np3}} t + \frac{N_s I_0}{N_{p3}} \qquad (5\text{-}7)$$

where LNp3 and I0 mean the primary magnetizing inductance of winding Np3 and output current, respectively.

The demagnetizing mechanism is also quite different in Case 1. For $t > t_2$, i_{Np3} is given by,



(a) Switch ON in Case II



(b) Key waveforms in Case II

Fig. 5-5 Case II

$$i_{Np3} = i_m(t_2) - (2V_{cr} - V_{in})/L_{Np3}\,(t - t_2) \tag{5-8}$$

In Case II, assume T2 operates in Continuous Current Mode (CCM), and then the following equation applies,

$$\frac{N_s}{N_{p3}} D(t) V_{in} \sin \omega t = V_0 \tag{5-9}$$

Assuming Eq. (5-9) at $t = T_0$, the following qualities are applied:

$$\frac{N_s}{N_{p3}} D(T_0) V_{in} \sin \omega T_0 = V_0 = \frac{N_s}{N_{p1}} V_{cr} D(T_0) \tag{5-10}$$

Hence, from Eq. (5-10) the duty cycle in Region II is given by,

$$D(t) = D(T_0) \frac{\sin \omega T_0}{\sin \omega t} \tag{5-11}$$

Eq. (5-11) indicates the duty ratio will decrease in cosecant mode from T_0 to next line peak moment, and the input peak current in Region II:

$$i_{pk}(t) = D(t)T_s \frac{V_{in} \sin \omega t}{L_{in}} = D(T_0)T_s \frac{V_{in} \sin \omega T_0}{L_{in}} \qquad (5\text{-}12)$$

From the Eq. (5-12), we conclude that the input peak current stays almost constant throughout Region II.

Equation (5-10) indicates T_0 depends on the turn ratio of $\frac{N_s}{N_{p3}}$ and $\frac{N_s}{N_{p1}}$, so changing the turn ratios can adjust the duration of Case I and II, and substantially adjust the portion of direct energy transfer.

Obviously the constructed hybrid energy transfer topology has the following advantages:

1. The overall efficiency will be improved since considerable energy is being delivered to the output directly from the line during Case II (Region II), without passing the buffering storage capacitor. Simply, the efficiency will be improved due to less power being processed.
2. In Case II, with the constant peak current, the turn off losses of the switch will also be reduced, which will further help to improve the efficiency. Besides, since partial power is transferred directly through the DC-DC transformer. The Flyback transformer can choose higher inductance to reduce the switch turn-off peak value, say less current stress.

3. The proposed topology achieves a high power factor with a simple single switch, single control loop, and low cost scheme. The new power flow path can be achieved just with an additional winding and one rectified diode. As described earlier, the flat top current waveform can obtain a fairly high power factor and low harmonics. And due to the effect of low frequency filter in front of the input side, the converter can actually obtain an even higher power factor than expected.

5.2.2 Simulation and Experimental Results

In order to verify the above analysis, a 48V@4.17A PSPICE closed-loop simulation circuit is built up as shown in Fig. 5-6.

Figure 5-7 gives the simulated results for the proposed topology.

Fig. 5-7(a) presents key waveforms in one line cycle: The first trace shows the input line voltage. The second trace indicates the reference voltage for the Pulse Width Modulation (PWM). As it can be seen, the pulse width did exhibit the performance given by Equation (5-2), after the input voltage exceeds the preset value, the pulse width will decrease in a cosecant mode until the instant voltage reaches its peak value. This feature helps to alleviate the current stress, thereafter to improve the overall conversion efficiency. The third trace indicates the averaged input current. As expected, when the input voltage is lower than the preset value, the input current will follow the input voltage; after input exceeds the preset value, the input current exhibits near constant. It should be noted here that the practical waveform would be better since the input filter has not been implemented in front of the presented simulation scheme. The fourth trace shows the averaged current flowing through the additional winding Np3. It can be found

in this interval that a large portion of the input power has been delivered to the output directly. The fifth trace gives the averaged current flowing through winding Np1 (Np2 the same). It also can be seen that only a small output portion is powered by the buffer capacitors.

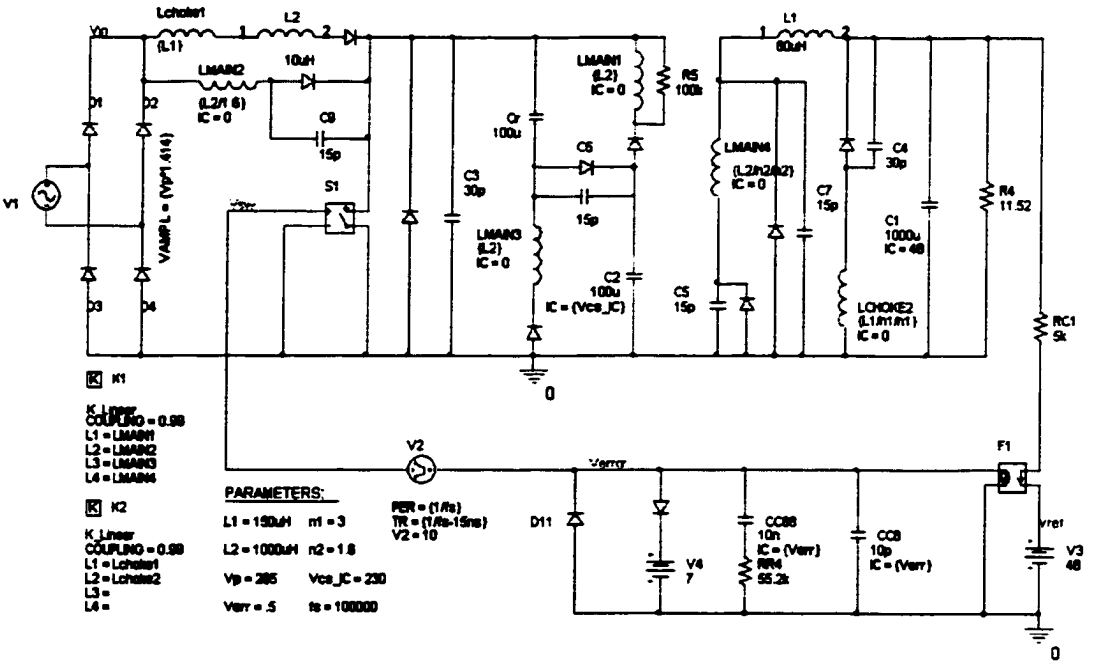
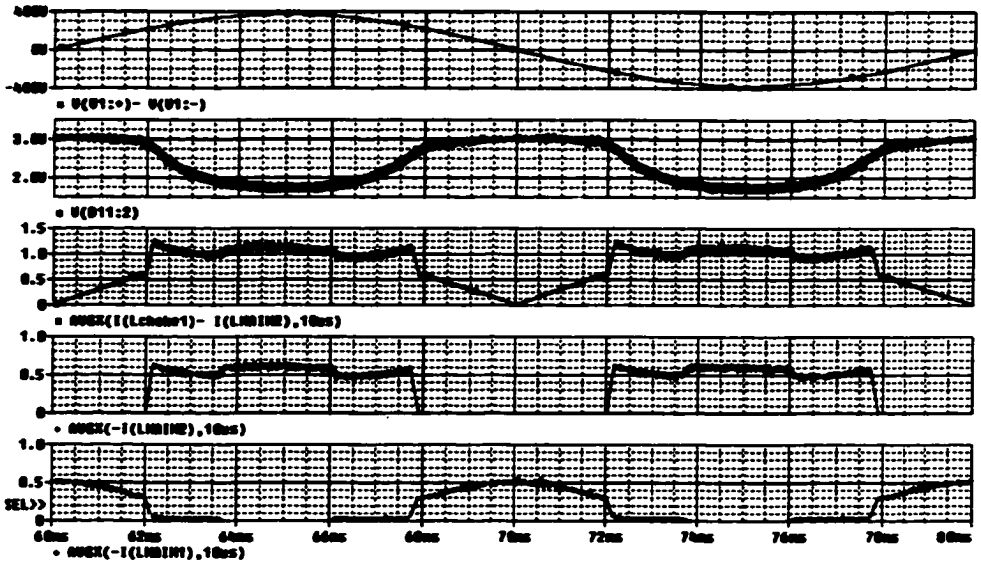


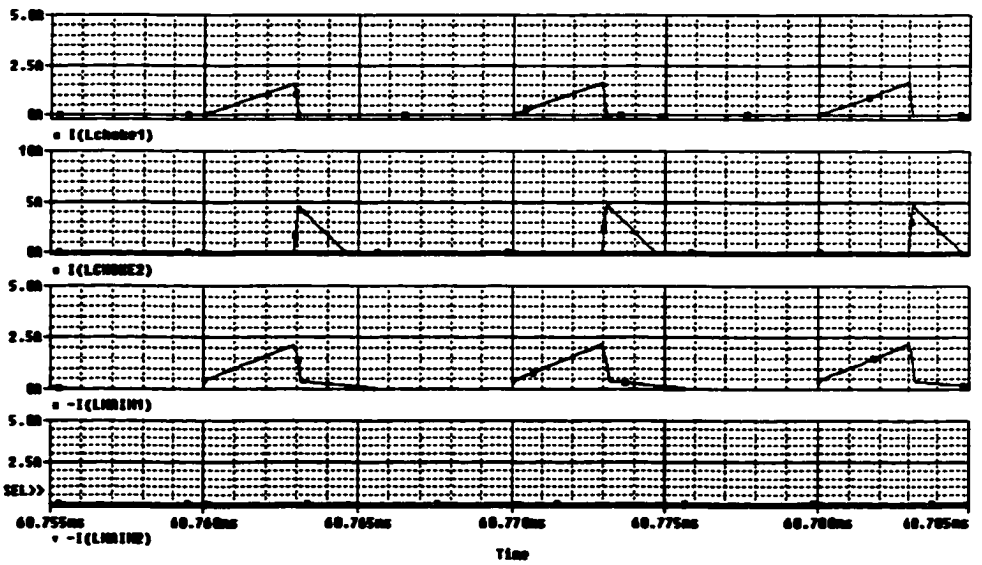
Fig. 5-6 Simulation Schematics

Figures 5-7(b) and (c) show the current flowing through the different windings in one switching cycle during Case I and Case II, respectively, which agreed well with the discussion in Section II. It also can be found that windings Np1 and Np3 carry current in different intervals.

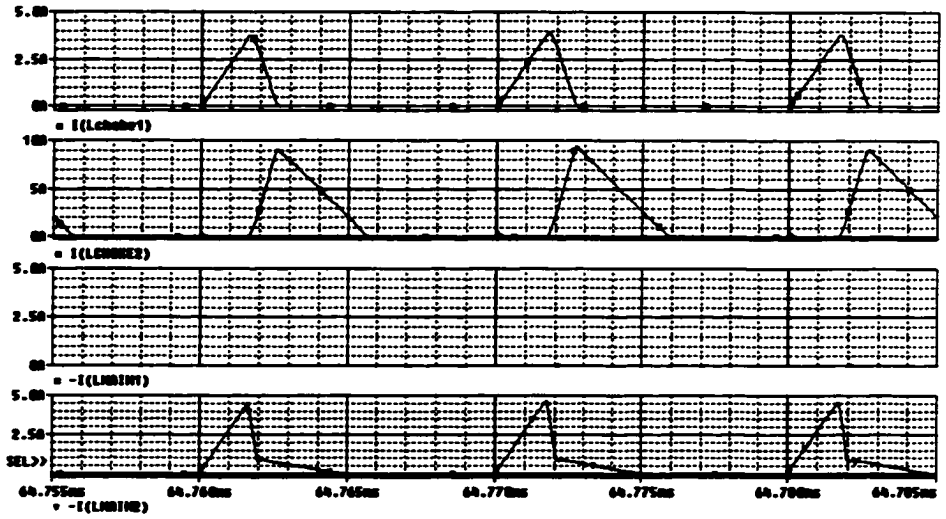


- *First trace: line voltage;*
- *Second trace: Reference voltage for PWM generation;*
- *Third trace: Averaged input Current;*
- *Fourth trace: Averaged current flowing through N_{p3};*
- *Fifth trace: Averaged current flowing through N_{p1}*

(a) Simulation waveforms in one line cycle



(b) Current flowing through different windings in Case I



(c) Current flowing through different windings in Case II

Fig. 5 -7 Simulation results

To verify the steady-state operation and the performance of the proposed topology shown in Fig. 5-3, a 48V@4.17A experimental prototype was built for universal input application. Figure 8 gives the measured reference voltage for PWM generation and line voltage waveforms. As it can be shown, pulse width is decreased according to $D(t) = D(T_0)\frac{\sin \omega T_0}{\sin \omega t}$ when the instant line voltage exceeds the preset value; in the other period, pulse width will keep constant to let the input current shape follow input voltage, therefore, obtain the desired flat-top current shape.

The input current waveform and the current flowing through the additional winding Np3 and primary winding Np1 under nominal input voltage and the maximum output power are shown in Fig. 5-9(a). Note that the energy is transferred to the output side directly through the additional winding Np3 when the line voltage exceeds the preset value, whereas the energy storage capacitor powering the output through winding Np1

when the line voltage dropped below the preset value. The corresponding power factor and the efficiency obtained with the prototype built were 0.986 and 85.6%, respectively. Figure 9(b) shows the related waveforms for 220V input and full load output, the corresponding power factor and the efficiency was 0.962 and 86%, respectively.

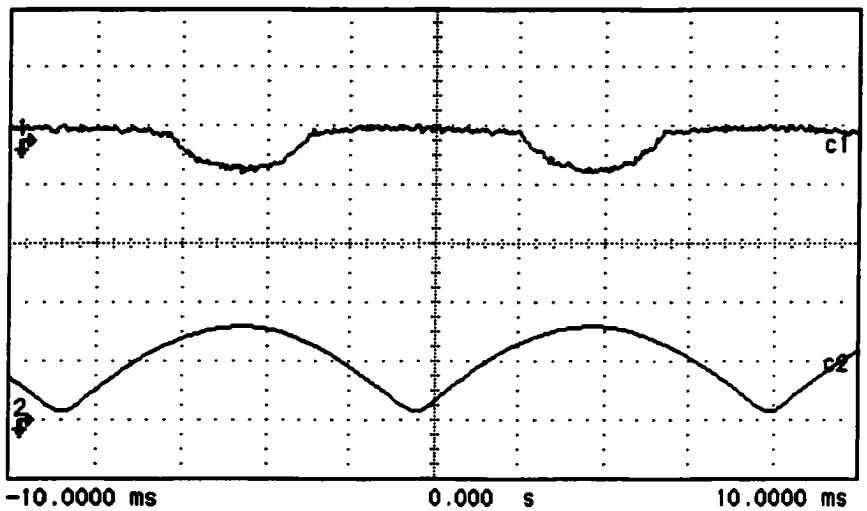
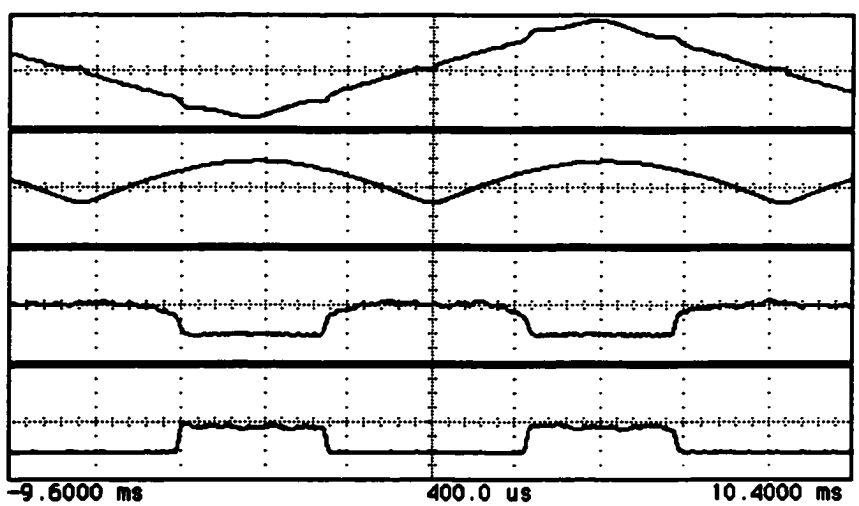
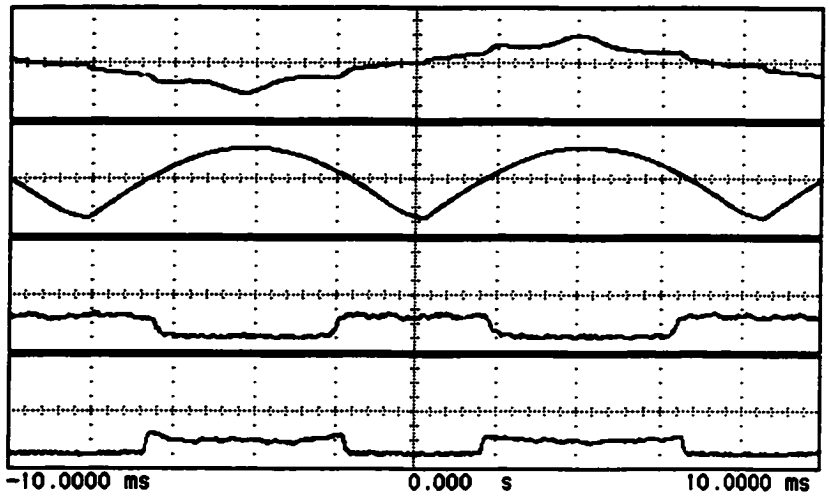


Fig. 5 -8 Reference voltage for PWM generation (upper trace 1V/div) and input voltage (lower trace 100V/div, P_{out} = 48V @ 4.17A)



(a) V_{in} = 110V, P_{out} = 48V @ 4.17A



Trace 1: input line current (5A/div);

Trace 2: input voltage (200V/div);

Trace 3: averaged current flowing through winding Np1 (5A/div);

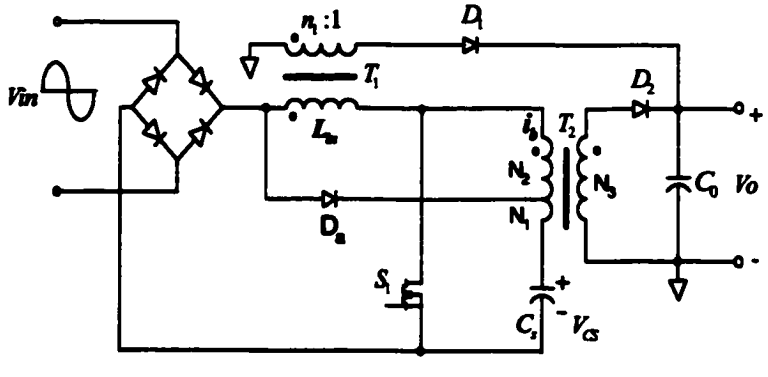
Trace 4: averaged current flowing through winding Np3 (5A/div)

(b) $V_{in} = 220V$, $P_{out} = 48V@4.17A$

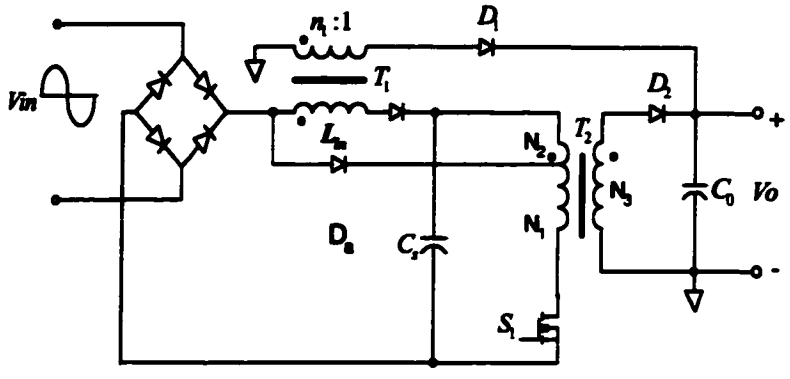
Fig. 5-9 Experimental results

5.2.3 Topology Derivations

The proposed concept can be applied to most of the single-stage converters. Typical applications are shown in Fig. 5-10. As it can be seen, for simplicity, only one additional diode is needed to carry out the proposed concept.



(a) Modified BIFRED topology



(b) Modified Redl's topology

Fig. 5-10 Topology derivations

The proposed flat-top current waveform with direct energy transfer concept in AC-DC converter is a simple solution to improve the conversion efficiency, and yet still achieves a high power factor. Using the proposed technique, energy transfers in hybrid modes: during the interval that instant line voltage exceeds the preset value, energy is transferred directly to the output side from the input line, rather than from the energy storage capacitor in the power factor correction (PFC) cell. The energy transfer mode therefore resulted in higher efficiency due to the reduced power processing times, as well as reduced switching losses. In the region in which the instant line voltage is below the preset value, the energy storage capacitor in the PFC cell then powers the output load to obtain smaller output ripple and a higher power factor due to the constant duty cycle and buffered DC bus voltage. The direct energy transfer duration can be adjusted to meet the specified requirements via selecting a proper preset value. The proposed concept achieved high efficiency and a high power factor with a simple, low cost scheme, and can be extended to other well-known topologies.

5.3 Peak Value Reduction Approach

The scheme proposed in Fig. 4-11 not only has the inherent voltage clamping capability, it also brings about another bonus, in that to a certain degree, it is capable of reducing the current stress. This feature can be illustrated through the operation modes as shown in Fig. 5-11.

It can be seen from i_{D_2} in Figure 5-11, that the existence of interval D_1 will decrease the duty cycle when line voltage is near its peak value, and thus can effectively reduce the peak value of input current when transferring the same average input current. Therefore, the main switch can be turned off under reduced current stress.

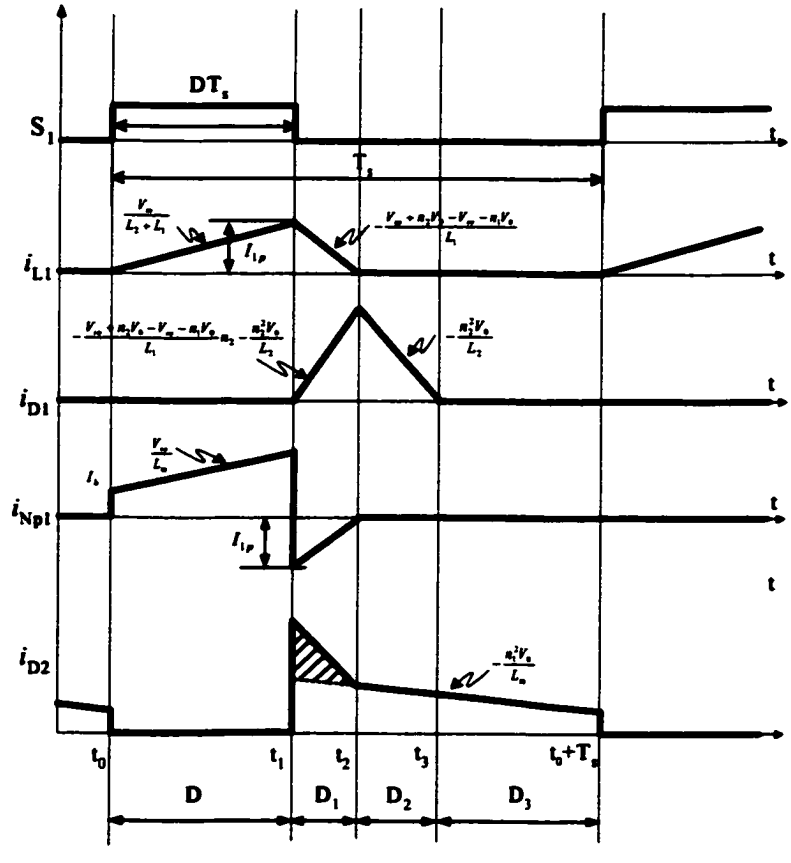


Fig. 5-11 Idealized Key waveforms in one switching cycle

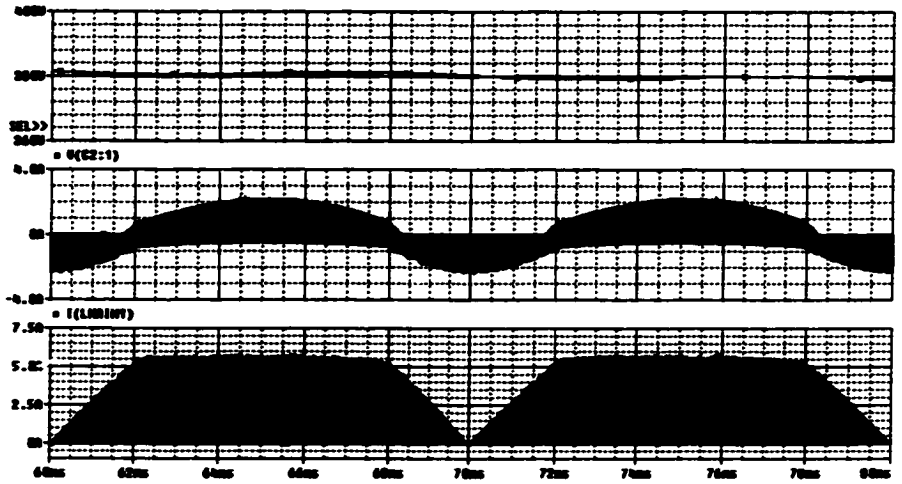


Fig. 5-12 Simulated results for circuit shown in Fig. 4-12

Fig. 5-12 gives the simulated waveform for the circuit shown in Fig. 4-11. The top trace indicates the voltage across the bulk capacitor being well controlled under 400V; the middle trace shows the current flowing through the primary winding of the DC-DC transformer; and the bottom trace clearly indicates that the peak current has already been reduced remarkably.

5.4 CCM approaching Schemes

CCM or Critical CCM operation certainly has lower current stress. Therefore, some literatures tried adopting CCM or Critical CCM operation in S^2 PFC AC-DC converters to alleviate current stress. The literature [23] carried out the PFC via charge-pump concept, and the PFC stage operates in CCM modes. However, such CCM approaches are parameter sensitive and just marginally meet the requirements.

Using a Flyback transformer replace the traditional boost inductor, a CCM PFC scheme, adopting a resonant tank, is given as shown as Fig. 5-13. Closed loop simulation

and experimental results are also presented in Fig. 5-14(a) and (b) respectively. CCM operation did can effectively improve the conversion efficiency and has a much better EMI performance. However, generally speaking, it will also lead to increased harmonic contents, and therefore deteriorate the input current quality. Besides, sound input current shaping capability normally just limits to a narrow load range, in the other words, poor input current shaping occurs in the application with wide load range.

Therefore, up to now, the proposed CCM topology could merely be considered an alternative approach for high power density applications that have stringent high efficiency and loosely power factor requirement.

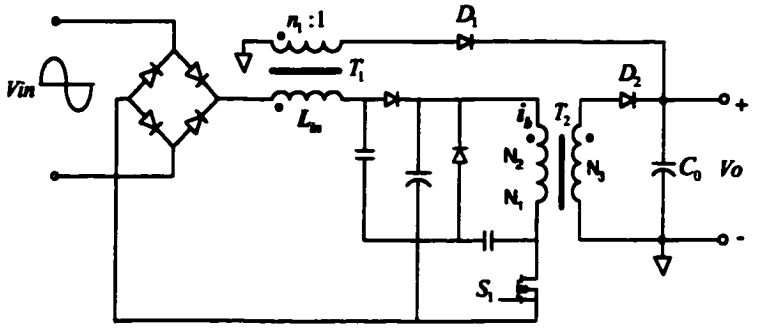
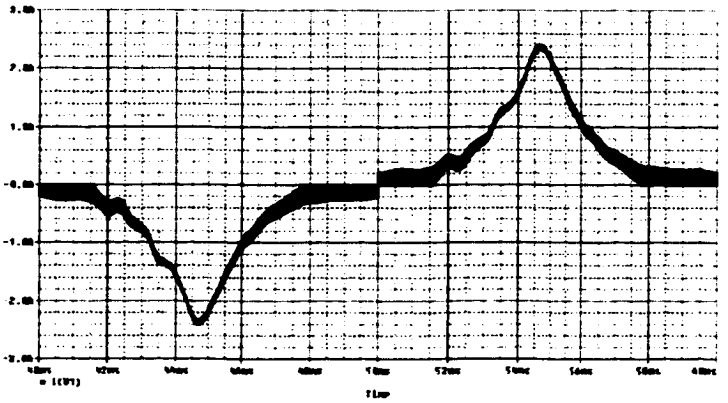
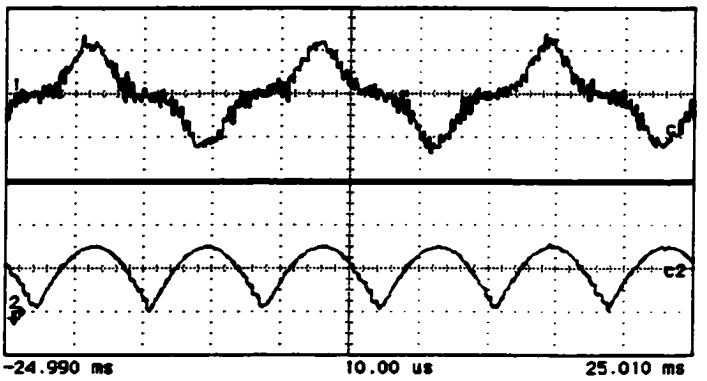


Fig. 5-13 Single-stage CCM PFC with Resonant Tank



(a) Simulation Waveform



(b) Experimental Results

Fig. 5-14 Single-stage CCM PFC Operation

5.5 Summary

This chapter introduces three current stress suppression techniques, i.e. flat top peak current clamping, peak current reducing, and resonant tank CCM current shaping techniques. Simulation results and experiment are carried out to verify the concept.

A near flat-top input current waveform and direct energy transferring AC-DC converter which features high efficiency and high power factor is described. In the proposed converter, energy transfers in hybrid mode which means that when the instant line voltage exceeds the preset value, energy is transferred directly to the output side from the input line; otherwise the energy storage capacitor powers the output load. The performance of the proposed concept was evaluated on a 200W (48V@4.17A) experimental prototype. It is shown that the efficiency is increased significantly over the case without the direct energy concept. Proof of the concept was verified theoretically and experimentally. Here, we propose a novel method that allows a parallel path of

energy transfer in order to minimize power-processing times and simultaneously let the converter maintain a high power factor.

6. CONTROL SCHEME ENHANCEMENT

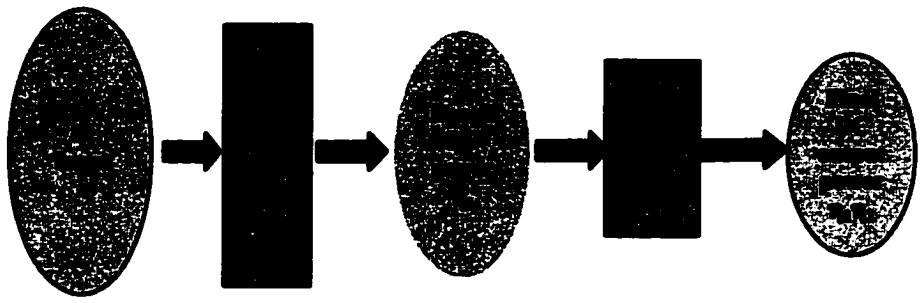
6.1 Conceptual Overview

Control scheme enhancement means improving single -stage AC-DC converter performance through proper control approaches.

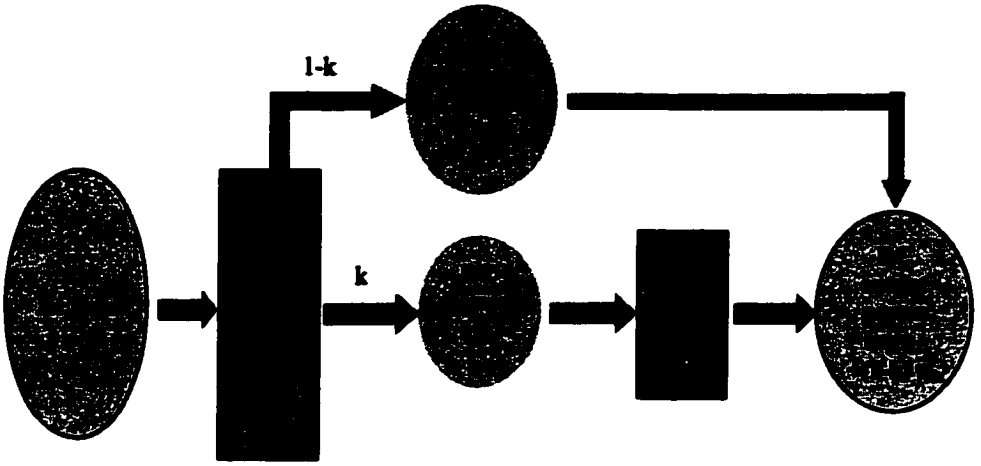
Unlike cascading two-stage topology, the energy had to be processed twice by two serially connected power stages, as shown in Fig. 6-1. For the S^2 PFC AC-DC converter, from the view of its structure, it's not necessary to process all the energy twice.

In fact, several circuits have been presented with this philosophy, seeking to increase its conversion efficiency.

Two parallel paths were introduced in [34] for energy processing. Partial power is delivered through one of them straight to the load. The rest is stored after the first processing and then delivered to the load. The output power is managed only 1.32 times in such an effort. The problem is that the power stage is quite complex, it requires at least three switches plus a specific control scheme.



(a) Energy serially processing schemes



(b) Energy parallel processing schemes

Fig. 6-1 Energy processing schemes

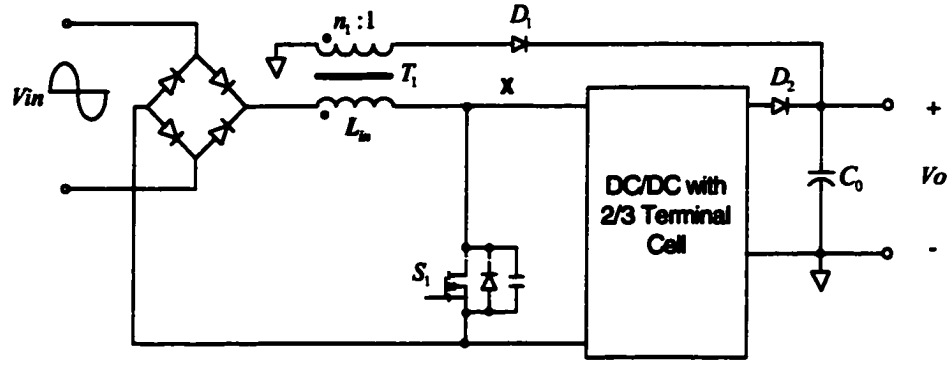
Circuits described in [42] split the power waveform in two equal parts giving one of them to the load. This is achieved by changing the position of the converters of the two-stage approach. Therefore, 50% of the output power is processed once. The rest half is managed twice. So, output power is managed 1.50 times without increasing the complexity of the circuit. The problem is that the field of application is limited due to the restrictions in the connection of the converters.

6.2 Processing Less Energy

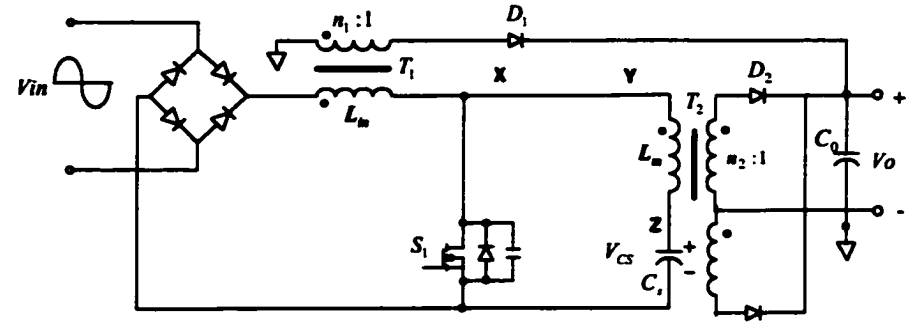
6.2.1 System Configuration and Operation Principle

In Fig. 6-2 (a), another energy discharge path for the boost inductor is constructed in the output side, therefore; in the main switch OFF interval, partial power is delivered straight to the output without being stored in the buffer capacitor first, thus reducing the energy portion that was processed twice.

In Fig. 6-2(b), implementation of a bi-directional DC-DC cell also has inherently less energy processing capability, since in the interval that Cs is charged, the DC-DC transformer operates in forward mode, and delivers partial power to the output side directly. Such an elaborate scheme insures that more than 50% energy is being transferred to the output directly.



(a) Fly boost scheme



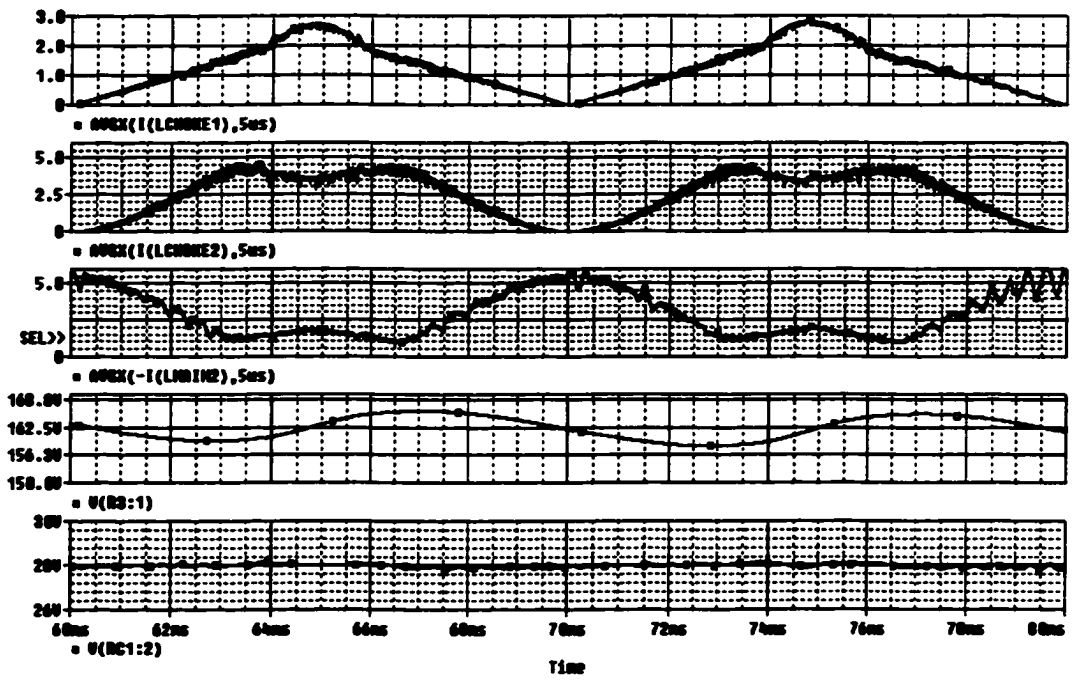
(b) Bi-direction DC-DC cell scheme

Fig. 6-2 Less energy processing schemes

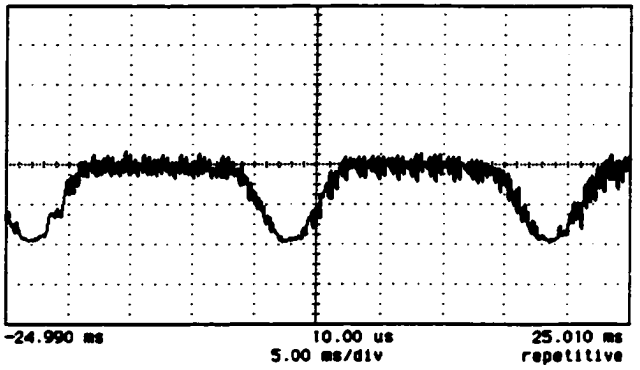
6.2.2 Simulated and Experimental Verifications

Simulation and experiment are also carried out to verify the above analysis. Figure 6-3(a) gives the simulated key waveforms in one line cycle for an 85~265V/60Hz input, 28V@5.35A output design example, using the scheme shown in Fig.6-2(b). The first

trace shows the rectified input current, which is nearly a sinusoidal waveform with unity power factor; the second trace indicates the current transferred to the output through a flyback transformer T_1, resulting in more than 50% energy transferred to the output side without processed twice, which helps to increase the overall efficiency of the converter. The third trace indicates current transferred to the output through a bi-directional transformer T_2, which just fills the valley of the second current trace to pursue the trade-off between the high power factor and low output ripple. The fourth trace shows the charge and discharge variations of the bulk capacitor, which also clearly indicates the transition of transferring power through T_1 or T_2. The last trace gives the output voltage to indicate the proposed less energy processing scheme can obtain a pretty small output ripple with near unity power factor.



(a)



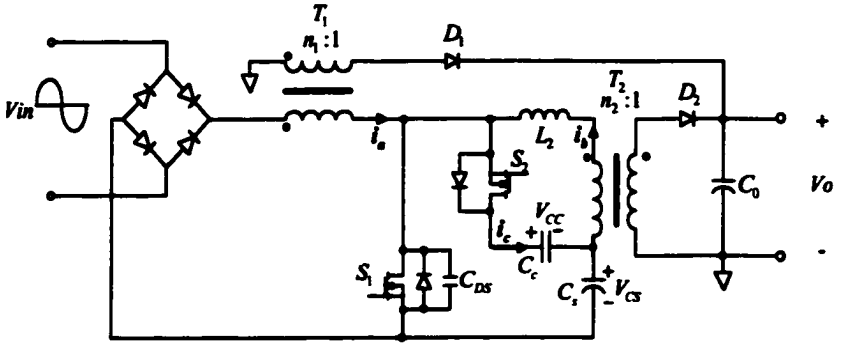
(b)

Fig. 6-3 Simulation (a) and experimental (b) results for the topology shown in Fig. 4-11(a)

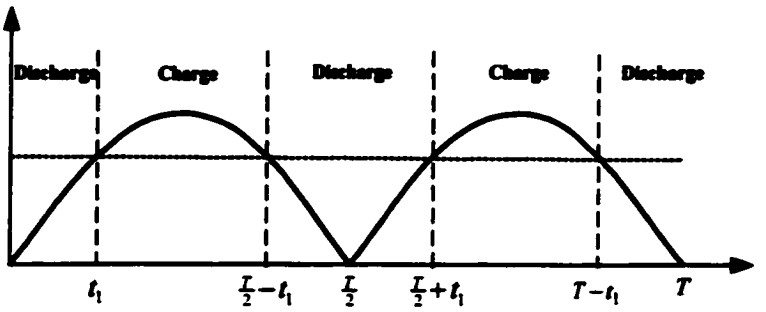
6.3 Higher Efficiency Processing Approaches

6.3.1 System Configuration and Operation Principle

In the S^2 PFC AC-DC converter, higher efficiency processing certainly can further improve the conversion efficiency, and boost its competence with cascading two-stage approaches. In Fig. 6-4, an active clamp cell is implemented in the less energy processing scheme shown in Fig. 6-2. An active clamp cell basically does not change the scheme's operation mechanism shown in Fig. 6-4(b), however, it can effectively remove the turn-off spikes and reduce the turn on switching losses, which will be detailed in the following sections.



(a) Topology



(b) Operation modes of C_s in one line cycle

Fig. 6-4 Active clamp Bi-flyback converter

6.3.2 Control Design

For active clamp Flyback topology introduced in [50], the auxiliary switch is usually turned on and off alternatively with the main switch, achieving a soft switching condition simultaneously for both switches. However, in such control mode, the DC bus voltage still stays beyond the tolerance of the commercially available capacitor. In this paper, a modified control scheme aiming at further alleviating the DC bus voltage to below 400V through the universal input range, without sacrificing the efficiency and the power factor, is proposed and experimentally verified.

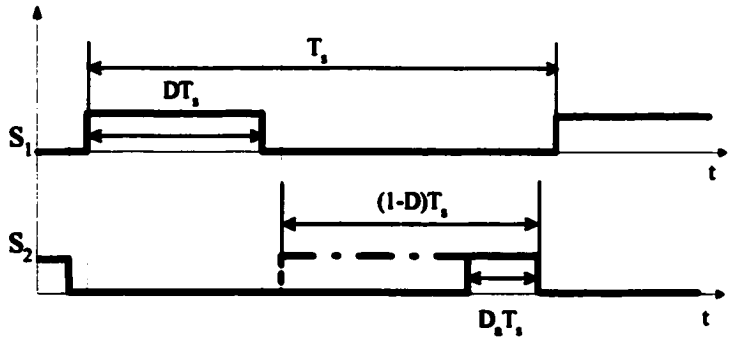


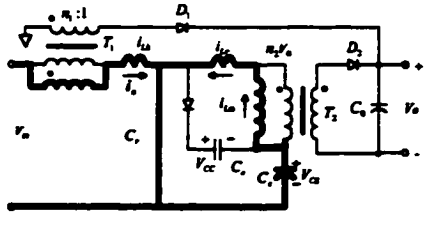
Fig. 6-5 Modified control scheme

The control scheme for the proposed converter is shown as Fig. 6-5. The auxiliary switch is turned on with a fixed narrow pulse width $D_r T_s$, rather than the conventional complimentary signal of the main switch ($(1-D)T_s$) in the active clamp application [50].

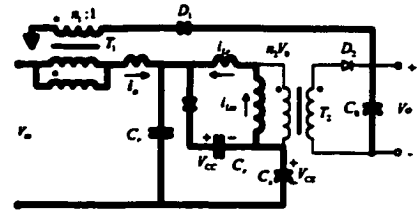
As discussed in the afore-description, the operation mode of transformer T_1 and T_2 varies in one line cycle, depending on the charge or discharge condition of the bulk capacitor, which is governed by the equation: $V_{in}(t)+n_1V_0 = V_{cr}+n_2V_0$. Therefore, here we can also divide a one line cycle into charge and discharge intervals to analyze the operation principle of the active clamp Bi-flyback converter, and afterwards to illustrate how the modified control scheme and active clamp cell works.

The following discussion takes into account the leakage inductance of both transformers, and assumes that:

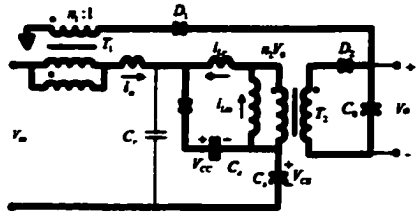
- All components are ideal;
- Leakage inductance is much less than the magnetizing inductance for both flyback transformers: $L_k << L_p$ for T1 and $L_r << L_m$ for T_2.



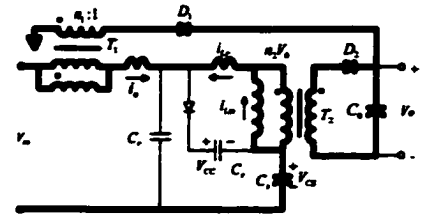
Mode 1: $[t_0 - t_1]$



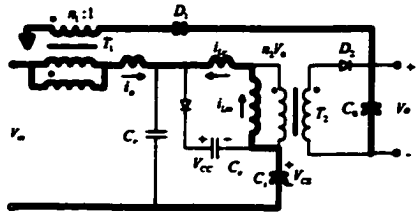
Mode 2 $[t_1 - t_2]$



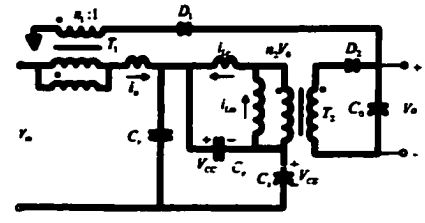
Mode 3: [$t_2 - t_3$]



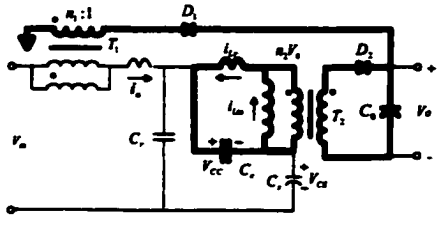
Mode 4: [$t_3 - t_4$]



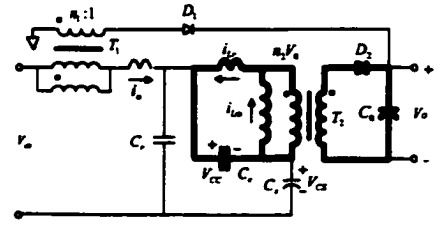
Mode 5: [$t_4 - t_5$]



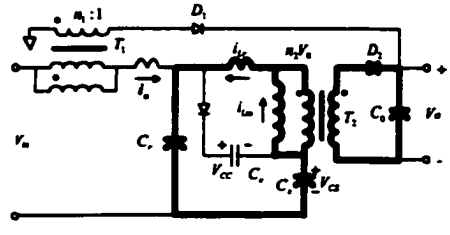
Mode 6: [$t_5 - t_6$]



Mode 7: [$t_6 - t_7$]

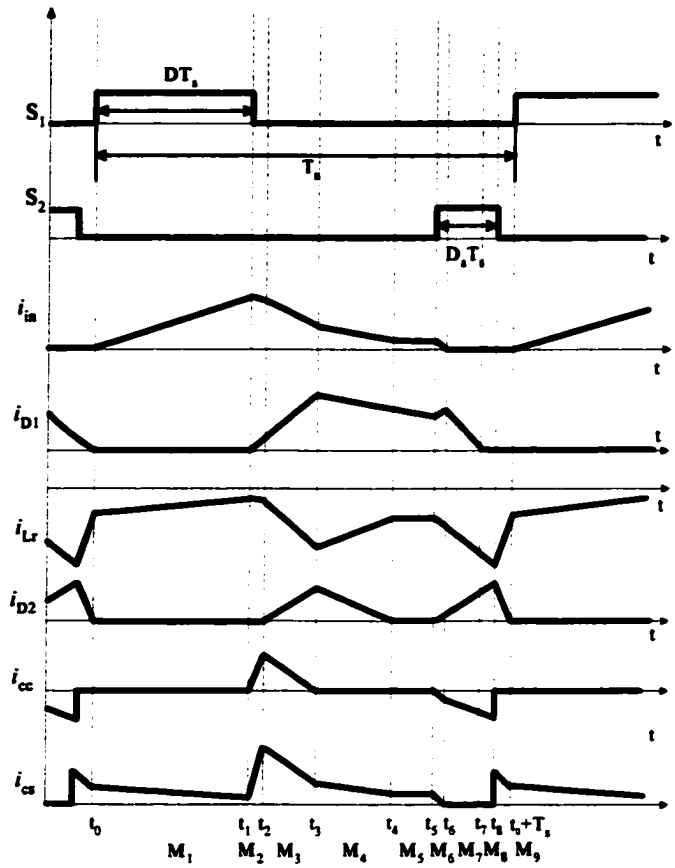


Mode 8: [$t_7 - t_8$]



Mode 9: [t8 – t0+ Ts]

(a) Operation modes



(b) Key waveforms

Fig. 6-6 Operation modes (a), and key waveforms in charge interval (b)

6.3.2.1 Charge Interval

The operation modes and key waveforms in the charge interval are illustrated in Figs. 6-6(a) and (b) respectively. The detailed operation of the circuit can be explained as follows with focusing on the current variation flowing through the bulk capacitor.

Mode 1: [t0 – t1]

At t0, S_1 is turned on while S_2 is off, as shown in Fig. 6-6(a). The output rectifiers D_1 and D_2 are reverse biased. For T_1, the magnetizing inductance Lb, together with the leakage inductance Lk, is charged linearly up according to the Equations:

$$(L_B + L_k)\frac{di_{in}}{dt} = V_{in}$$

For T_2, the magnetizing inductance Lm, together with the resonant inductance Lr, is also charged up linearly. And the current flowing through bulk capacitor i_{cs} decreases linearly according to the Equation:

$$(L_r + L_m)\frac{di_{cs}}{dt} = V_{cs}$$

Mode 2: [t1 – t2]

At t_1, S_1 is soft turned off due to the existence of switch parasite capacitance C_r. Since the charging duration is relatively short, this soft turning off duration could be neglected here to simplify the analysis.

When V_{Cr} increases to the value of V_{Cs}, i_{in} will be diverted to charge C_c and C_s. Since $C_c >> C_r$, current can be considered totally flowing through C_c.

Since the secondary voltage of transformer T_1 is sufficient to forward bias D1, the primary voltage of T_1 is then clamped to approximately $n_1 V_0$. Therefore, in this period we have the following governing equations:

$$L_k\frac{di_{cs}}{dt} = V_{in} + n_1 V_0 - (V_{cs} + v_{cc})$$

$$i_{cs} = -i_{Lr} + C_c\frac{dv_{cc}}{dt}$$

$$(L_r + L_m)\frac{di_{Lr}}{dt} = v_{cc}$$

Due to $L_m >> L_r$, i_{Lr} can be considered to be constant $i_{Lr} \approx I_{Lr}$ to simplify the analysis, so:

$$i_{cs} = \sqrt{\frac{\Delta^2}{\frac{L_k}{C_c}} + I^2_{Lr}}\sin\left(\frac{t}{\sqrt{L_k C_c}} + \tan^{-1}\frac{I_{Lr}}{\Delta}\sqrt{\frac{L_k}{C_c}}\right) \qquad (6\text{-}1)$$

where, $\Delta = V_{in} - n_1 V_0 - V_{cs}$.

Mode 3: [t2 – t3]

At t_2, when voltage across the clamp capacitor V_{Cc} increases until $V_{cc} \cdot \frac{L_m}{L_r + L_m} \geq n_2 V_0$, D_2 becomes also forward biased and T_2 operates in forward mode. The transformer primary voltage is clamped, by the large output capacitance, to approximately $n_2 V_0$. Equations of this mode are:

$$(L_r + L_k)\frac{di_{Lr}}{dt} = -(V_{in} + n_1 V_0) + (V_{cs} + n_2 V_0)$$

$$L_r \frac{di_{Lr}}{dt} = -v_{cc} + n_2 V_0$$

$$i_{cs} = -i_{Lr} + C_c \frac{dv_{cc}}{dt}$$

Since V_{Cs} can be considered constant, so current flowing through bulk capacitor i_{cs} decrease near linearly.

Mode 4: [t3 – t4]

At $t = t_3$, current flowing through C_c reaches zero with $i_{cs} = i_{Lr} = i_{in}$, V_{Cc} then reaches its maximum value, blocking the body diode of auxiliary switch S_1. The current i_{cs} decreased according to the following Equation:

$$(L_r + L_k)\frac{di_{cs}}{dt} = -(V_{in} + n_1 V_0) + V_{cs} + n_2 V_0$$

Mode 5: [t4 – t5]

At $t = t_4$, D_2 is reverse biased and i_{cs} decreased linearly by the following relationship:

$$(L_r + L_m + L_k)\frac{di_{cs}}{dt} = -(V_{in} + n_1 V_0) + V_{cs}$$

Since $L_m >> L_r$, i_{cs} almost kept constant.

Mode 6: [t5 – t6]

At $t = t_5$, turn on S_2, V_{Cc} applied upon transformer T_2 with its primary voltage again clamped to $n_2 V_0$. By neglecting the effect of C_r, we have:

$$L_r\frac{di_{Lr}}{dt} = V_{cc} - n_2 V_0$$

$$L_k\frac{di_{cs}}{dt} = (v_{cc} + V_{cs}) - (V_{in} + n_1 V_0)$$

$$i_{cs} = -i_{Lr} + C_c\frac{dv_{cc}}{dt}$$

Mode 7: [t6 – t7]

At $t = t_6$, $i_{in} = i_{cs} = 0$, and we have

$$v_{cc} - n_2 V_0 = L_r\frac{di_{Lr}}{dt}$$

$$i_{Lr} = -C_c \frac{dv_{cc}}{dt}$$

Since we assume $C_c >> L_r$, i_{Lr} increases linearly as shown in Fig.6-6 (b).

Mode 8: [t7 – t8]

The operation mode is almost the same as Mode 7, except there is no current flowing through the secondary of transformer T_1.

Mode 9: [t8 – t0+ Ts]

The auxiliary switch is turned off at t_8, effectively removing C_c from the circuit. At this moment, the magnetizing current diverted to the bulk capacitor is given by:

$$i_{cc}(t)\Big|_{t=t_8} = i_{Lr}(t)\Big|_{t=t_8} = \frac{V_{cc} - n_2 V_0}{L_r} D_a T_s \qquad (6\text{-}2)$$

In this mode, a resonant network is formed between L_r and the main switch drain to source capacitance C_r. The primary voltage of the transformer T_2 remains clamped at $n_2 V_0$ as C_r is discharged to provide a soft switching condition for the main switch. The first order differential equation in terms of C_r and L_r are given by:

$$L_r \frac{di_{Lr}}{dt} = V_{cc} + n_2 V_0 - v_{cr}$$

$$C_r \frac{dv_{cr}}{dt} = i_{Lr}$$

At $t = t_0 + T_s$, D_2 is reverse biased by V_0. The magnetizing and leakage inductances of both transformers begin to linearly charge again, starting another switching cycle.

6.3.2.2 Discharge Interval

The operation modes and key waveforms in the discharge interval are illustrated in Figs. 6-7(a) and (b) respectively. The brief description of operation can be explained as follows:

Mode 1: [t0 – t1]

Same as Mode 1 in the charging interval in Fig. 6-6(b).

Mode 2: [t1 – t2]

Same as Mode 2 in the charging interval in Fig. 6-6(b).

Mode 3: [t2 – t3]

At t2, when voltage across the clamp capacitor V_{Cc} becomes $V_{cc}\frac{L_m}{L_r+L_m} \geq n_2 V_0$, D_2 is forward biased and T_2 operates in flyback mode. The transformer primary voltage is clamped by the large output capacitance to approximately $n_2 V_0$. The equation in this mode are given by:

$$C_c \frac{dv_{cc}}{dt} = i_{cc},\ C_r \frac{dv_{cr}}{dt} = i_{cc} + i_{Lr}$$

$$v_{cr} = v_{cc} + V_{cs},\ L_r \frac{di_{Lr}}{dt} = v_{cc} - n_2 V_0$$

$$i_{cs} = i_{cc} - i_{Lr}$$

Since it is assumed that $C_c >> C_r$, current can be considered to flow fully through C_c.

Mode 4: [t3 – t4]

In this mode, current i_{cs} reaches zero, and we have:

$$L_r \frac{di_{Lr}}{dt} = v_{cc} - n_2 V_0$$

$$C_c \frac{dv_{cc}}{dt} = i_{Lr},\ i_{Lr} = i_{cc}$$

Mode 5: [t4 – t5]

Same as Mode 4 except there is no current flowing through the secondary of transformer T_1

Mode 6: [t5 – t6]

At $t = t_5$, i_{Lr} reaches zero and clamp capacitor C_c is blocked by the reverse biased body diode of S_2, and L_r will resonant with C_r according to the following equation:

$$L_r \frac{di_{Lr}}{dt} = V_{cs} + n_2 V_0 - V_{cr}$$

$$C_r \frac{dV_{cr}}{dt} = i_{Lr}$$

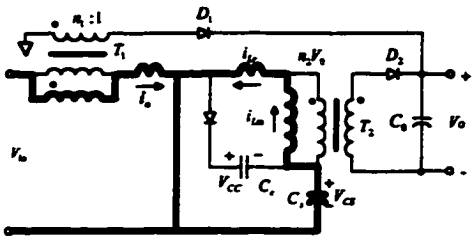
Mode 7: [t6 – t7]

Same as Mode 8 in the charging interval in Fig. 6-6(b).

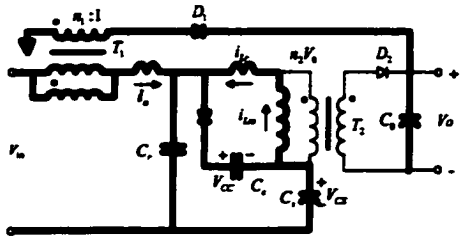
Mode 8: [t7 – t0+ Ts]

Same as Mode 9 in the charging interval in Fig. 6-6(b).

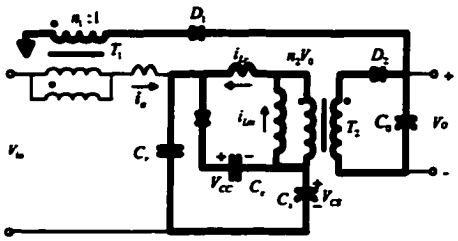
At $t = t_0 + T_s$, D_2 becomes reverse biased by V_0. The magnetizing and leakage inductances of both transformers begin to linearly charge again, starting another switching cycle.



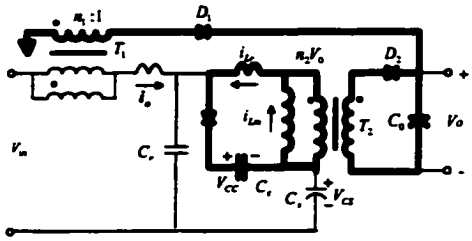
Mode 1: [$t_0 - t_1$]



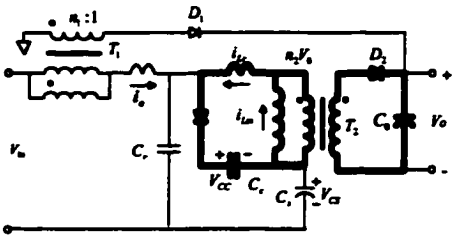
Mode 2 [$t_1 - t_2$]



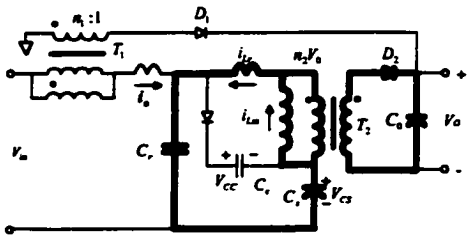
Mode 3: [$t_2 - t_3$]



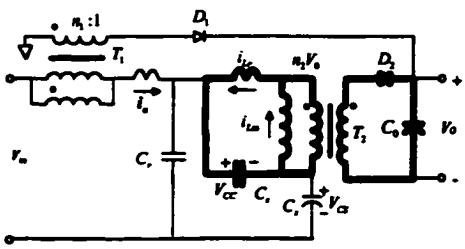
Mode 4: [$t_3 - t_4$]



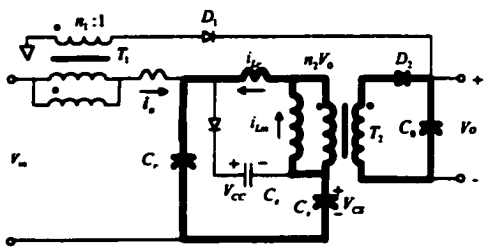
Mode 5: [$t_4 - t_5$]



Mode 6: [$t_5 - t_6$]

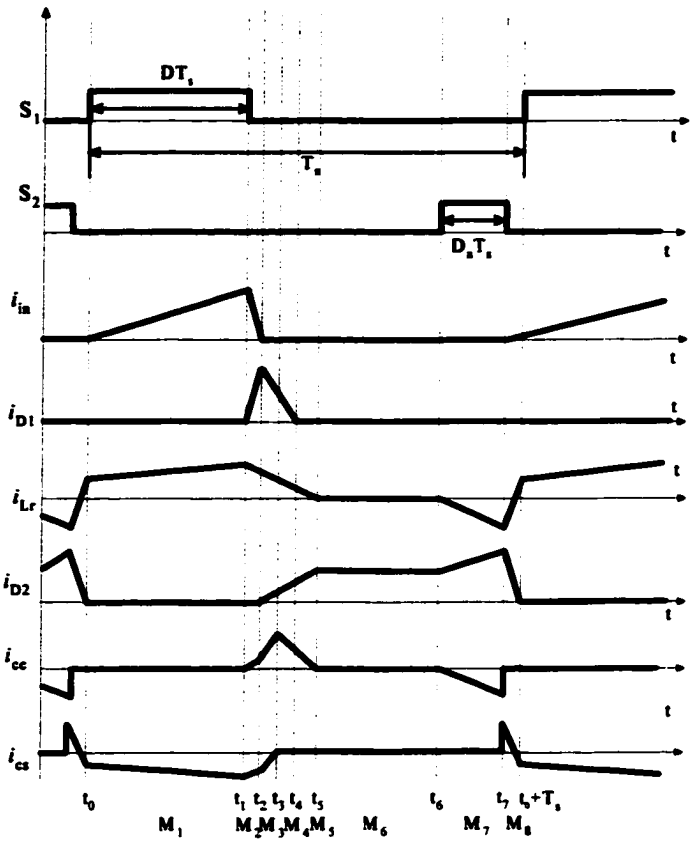


Mode 7: [t6 – t7]



Mode 8: [t7 – t0+ Ts]

(a)Operation mode



(b) Key waveforms

Fig. 6-7 Operation modes (a), and key waveforms in discharge interval (b)

From the afore-description, the operation condition of the bulk capacitor in each switching cycle could be determined through the current variation flowing through it.

From bulk capacitor current waveform i_{cs} shown in Fig. 6-6 and Fig. 6-7, it can be easily concluded that at the moment of main switching being turned on, its body diode is already forward biased and carries current, which means the energy stored in the parasite capacitor of the main switch has been transferred to the inductance components, therefore a soft switching turned on process can be achieved. And since the capacitance of Cc is much bigger, the energy stored in the leakage inductance can also be effectively absorbed by Cc to avoid over-voltage turn off spikes. Soft switching condition makes high

frequency operation and increasing the power density possible in the S^2 PFC AC-DC conversion.

Besides, the ON time of the auxiliary switch did affect the bulk capacitor voltage stress. We note:

1) For both charge and discharge intervals, at the instant of turning off the auxiliary switch, the discharging current of the clamp capacitor diverted to the bulk capacitor, since this current is proportional to the ON time of the auxiliary switch, as shown by Equation (6-2). Therefore, reducing the length of ON time can effectively alleviate the voltage stress across the bulk capacitor.

2) Due to cost and size considerations, the clamp capacitor is pretty small compared to the bulk capacitor, therefore, larger ON time will lead to lower final voltage across the clamp capacitor at the moment of the auxiliary switch being turned off. Since D2 is forward biased until V_{Cc} increases to the value $V_{cc}\frac{L_m}{L_r+L_m} \geq n_2 V_0$, it's easy to conclude from Equation (6-1), that just after turning on the main switch, the lower V_{Cc} will result in more current charged to the bulk capacitor in the next switching cycle. If V_{cc} was kept at a higher value, partial current could have been transferred to the output through the secondary winding of the PFC Flyback transformer.

6.3.3 Experimental Results

Fig. 6-8 Developed prototype for NASA

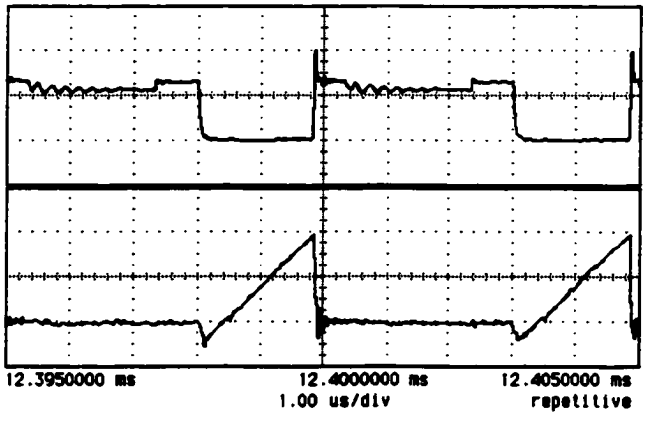


Fig. 6-9 Soft switching waveforms (Upper: Drain source voltage; Lower: Drain current)

Fig. 6-8 presents the practical prototype, and the operation waveform of the main switch is given as shown in Fig. 6-9. The bottom trace indicates that at the moment of main switching being turned on, its body diode already carries reverse current, which means the energy stored in the parasite capacitor have been transferred to the inductance components, therefore a soft switching turned on process is achieved. And since the

capacitance of Cc is much bigger, the energy stored in the leakage inductance can be effectively absorbed by Cc to obtain low turn off spikes. Since the main switch operates in a soft switching condition, even under 200KHz, the overall efficiency can still be improved above 81% over the entire input voltage range, as shown in Fig. 6-10.

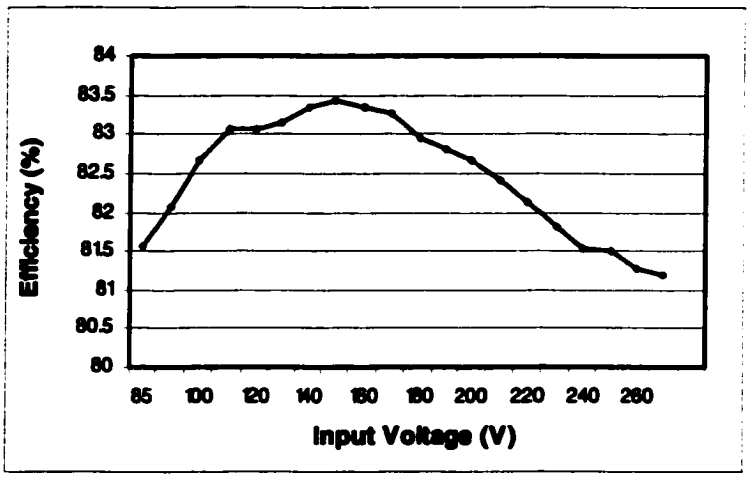


Fig. 6-10 Full load efficiency over the entire line

6.4 Summary

Better energy management techniques, including processing less energy or processing it with higher efficiency are introduced in this Chapter. Providing another discharging path in the output side for the Boost PFC inductor and adopting a bi-directional DC-DC converter is a simple and effective solution for processing less energy. Implementing an active clamp cell to achieve soft switching can further improve the efficiency and boost switching frequency and power density.

7. CONTROL SCHEME ENHANCEMENT

7.1 Conceptual Overview

Control scheme enhancement means improving performance of single-stage PFC AC-DC converters through proper control approaches.

For a small to medium power single-stage PFC AC-DC converter, the DC-DC section prefers a flyback circuit due to the minimum number of semiconductor and magnetic components.

In the flyback converter, the primary inductance of the transformer is generally much lower than the inductance of its counterpart in the forward converter. Hence, the rate of change of current during the primary conducting phase, ON period, is large, giving a large triangular shape to the primary current pulse. This triangular waveform is ideal for the application of current mode control, providing good noise immunity and well defined switching levels to the current comparator. With current mode control, there are two control loops in operation. The first, fast acting inside loop controls the peak primary current, while the second, much slower outside loop adjusts the current control loop to define the output voltage. The overall effect of these two control loops is that the power supply responds as a voltage controlled current source.

There are a number of advantages to be gained from current mode control. First of all, the system responds as if the primary is a high impedance current source and the

effective inductance of the converter transformer is removed from the output filter equivalent circuit. This results in a simple first order transfer function. Hence the control circuit may have a good high frequency response, improving the input transient performance. Line ripple rejection and loop stability are improved. A second major advantage is that primary current limiting is automatically provided without additional components.

For a current mode single-stage PFC AC-DC converter with flyback DC-DC conversion, the flyback DC-DC converter can be tailored operating in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Delivering the same power, CCM operation normally accompanied with less RMS current, lower turn-off losses and therefore, higher efficiency. However, since flyback circuit is basically boost derived family circuit, it has inherent Right Half Plane Zero (RHPZ) when it operates in continuous conduction mode, and therefore the system stability might be an important concern.

In CCM, in time domain, a large step load increase requires a corresponding percentage rise of the inductor current. This necessitates a temporary duty-cycle augmentation which causes the diode conduction time to diminish. Therefore, it implies a decrease in the average diode current at first, rather than an increase as desired. When heavily into the continuous mode, and if the inductor current rate is small compared to the current level, it can take many cycles for the inductor current to reach the new value. During this time, the output current is actually reduced because the diode conduction time has been decreased, even if the peak diode current is rising. The extra delay is mathematically described by a Right Half Plane Zero (RHPZ) in the transfer function

($Av=\frac{(1-S_z)\cdot\cdots}{\cdots}$), and forces the designer to roll off the loop gain at a point where the phase margin is still secure. Actually, a classical zero in the left half plane ($Av=\frac{(1+S_z)\cdot\cdots}{\cdots}$) provides a boost in gain and phase at the point it is inserted. Unfortunately, the RHPZ gives a boost in gain, but lags the phase. More viciously, its position moves as a function of the load which makes its compensation an almost impossible exercise. Rolling off the gain well under the worse RHPZ position is the usual solution.

In DCM, by definition, a third state is present whether either the diode or the switch conduct, and the inductor current is null. This idle time allows the switch duty cycle to lengthen in the presence of a step load increase without lowering the diode conduction time. In fact, it is possible for the DCM circuit to adapt perfectly to a step load change of any magnitude in the very first switching period, with the switch conduction time, the peak current, and the diode conduction time all increasing at once to the values that will be maintained at the new load current.

As we saw, keeping DC-DC flyback stage in DCM will allow us to design the compensation network in an easier way. It will also ensure stable and reliable behavior as long as you stay in the discontinuous area.

DCM operation offers improved dynamic performance of the flyback converter and easier compensation network design, but suffers from higher current stress and switch turn-off losses. Critical conduction mode, as the name suggested, is actually operating at the boundary of continuous and discontinuous conduction modes. Critical conduction mode, also called transition mode or boundary mode, gained more interest and

application in recent years. It easies converter compensation network design and also features high frequency response and lower current stress.

Besides, the soft turn-on of the switch might also be accomplished in the flyback converter operating in the critical conduction mode. Since the voltage on the primary switch at the turn-on instant is high and the associated capacitive turn-on loss is substantial, the soft turn-on switch is highly desirable.

In this chapter, critical conduction mode and its derivations are introduced for single-stage PFC AC-DC converter. Improved performance and features are validated through detailed analysis and system simulation.

7.2 Critical Conduction Mode Single-stage PFC AC-DC Conversion

Since the topology in previous chapters introduced another flyback transformer to replace the traditional boost inductor to achieve voltage clamping for the bulk capacitor, and the secondary of flyback PFC transformer connected directly to the output side, galvanic isolation for this secondary truly increases the system cost apart from the extra ultra fast recovery rectifier. Now let us take away the secondary winding and its associated rectifiers, the circuit becomes the standard BIFRED converter, as shown in Fig. 7-1. As the name suggests, the BIFRED converter consists of a boost circuit integrated with a flyback circuit, such that only one switch is required.

In this chapter, BIFRED converter will be tailored with critical conduction mode operation.

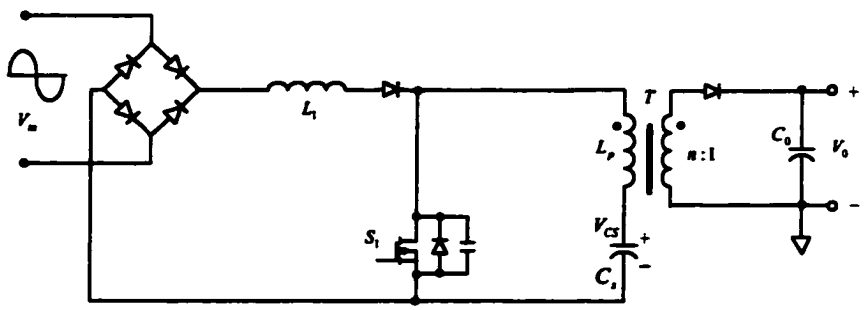


Fig. 7-1 The BIFRED converter

For a conventional BIFRED converter, as Madigan et al. outlined in [42], the boost inductor is designed so that the input current remains discontinuous over the entire range of operating conditions while the flyback converter operates in a continuous conduction mode over the specified load range. For open loop operation, the output voltage ripple is much less than that of the more conventional power factor correction topologies because of the presence of the large intermediate bulk capacitor. Therefore, the output voltage can be regulated with a high bandwidth loop without causing significant distortion of the line current. However, it will be shown that the BIFRED has a serious drawback as a single-stage converter. As proved in section 4.4, the input power in a discontinuous mode boost converter is given by,

$$P_{in} = I_{avg} I_{in} = \int_0^{\frac{T}{2}} \frac{V_{cs} \cdot V^2_{in} \sin^2 wt \cdot d^2 T_s}{2L_1 (V_{cs} - V_{in} \sin wt)} dt = \frac{d^2 T_s V^2_{in}}{2\alpha L_1} \int_0^{\pi} \frac{\sin^2 x}{1 - \frac{V_{cs}}{V_{in}} \sin x} dx \qquad (7\text{-}1)$$

Since this power is proportional to the square of the duty cycle, a small duty cycle is required for light loads. However, the voltage gain of a continuous conduction mode DC-DC flyback circuit is given by,

$$\frac{nV_o}{V_{cs}} = \frac{D}{1-D} \qquad (7\text{-}2)$$

This voltage gain is independent of the load conditions. Therefore, the only way that the input power can be reduced and the output voltage maintained constant for decreasing loads, is for the bulk capacitor voltage to increase.

7.2.1 Operation Principle

The origin of the high bulk capacitor voltage problem can be perceived as the conflict between the characteristics of the boost converter and the flyback converter. The boost converter requires a variable duty cycle in order to modulate the input power, while the flyback converter requires an almost constant duty cycle to maintain a constant output voltage. However, this problem can be resolved if the flyback is designed to operate in the critical conduction mode, since the input power under this condition is given by,

$$P_{out} = \frac{D^2 T_s}{2L_p} V_{ca}^2 \qquad (7\text{-}3)$$

where Lp is the magnetizing inductance of the flyback transformer referred to the primary. This power is also proportional to the square of the duty cycle, thus eliminating the source of conflict between the two stages.

Figure 7-2 shows the ideal waveforms of a BIFRED converter in which the boost section operates discontinuously while the flyback section operates in critical conduction mode.

7.2.1.1 Large Signal Model

If the inductor and capacitor currents are averaged over a switching period, a large signal instantaneous average representation of the operation of the converter provides an analytic perspective of the overall action of the BIFRED in critical conduction mode.

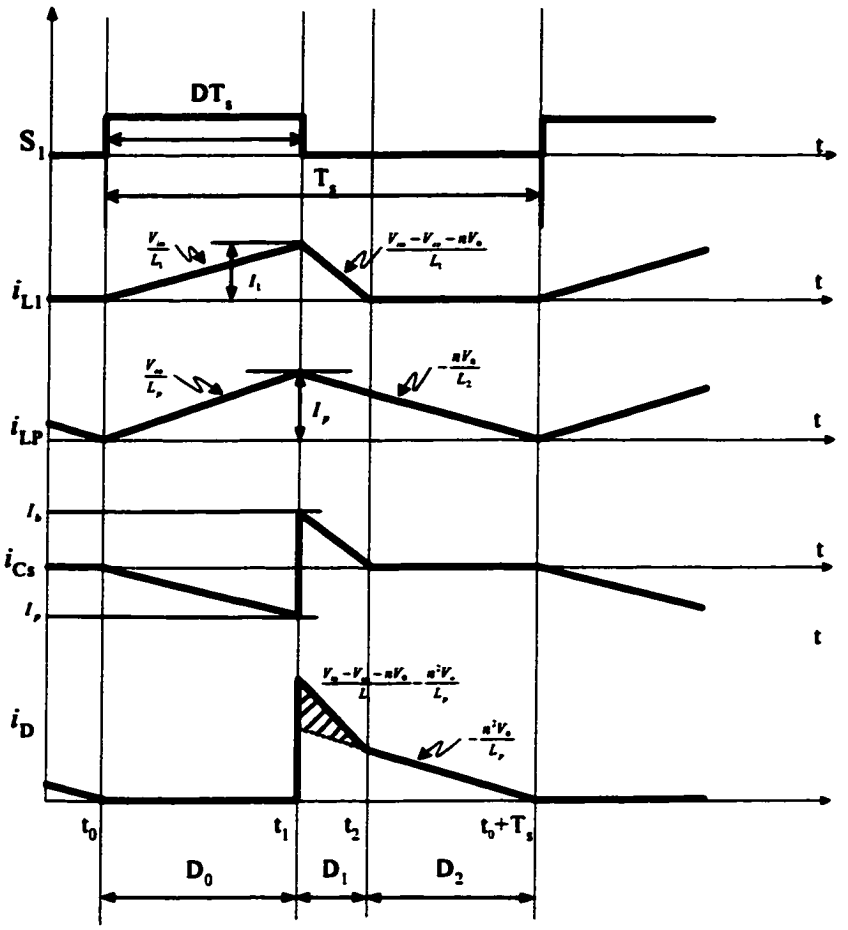


Fig. 7-2 Idealized Key waveforms for BIFRED with critical conduction mode

$$i_{L1} = \frac{D^2 T_s}{2L_1}\left(\frac{V_{in}(V_{cs} + nV_o)}{V_{cs} + nV_o - V_{in}}\right) \tag{7-4}$$

$$(C_s \frac{dV_{cs}}{dt})_{av} = \frac{D^2 T_s}{2}\left(\left(\frac{1}{L_1}\frac{V^2_{in}}{V_{cs} + nV_o - V_{in}}\right) - \frac{V_{cs}}{L_p}\right) \tag{7-5}$$

$$0 = \frac{DV_{cs}}{n} - (1-D)V_o \tag{7-6}$$

$$(C_o \frac{dV_o}{dt})_{av} = \frac{D^2 T_s n}{2}\left(\frac{1}{L_1}\frac{V^2_{in}}{V_{cs} + nV_o - V_{in}} + \frac{1}{L_p}\frac{V^2_{cs}}{nV_o}\right) - \frac{V_o}{R} \tag{7-7}$$

7.2.1.2 Steady-State Solution

Averaging the bulk capacitor current and the output capacitor current over a half line period, which must be zero, can provide steady-state analysis.

If it is assumed that the switching period T_s and duty ratio D are constant over the line period, and the ripple content of the output voltage and bulk capacitor voltage can be neglected, then averaging over a half line period results in the following equation for V_{cs} in the steady state:

$$V_{cs} = \frac{V_{in,peak} L_p}{L_1}\left(-\frac{2}{\pi} - M + \frac{2}{\pi}\frac{M^2}{\sqrt{M^2-1}}\left(\frac{\pi}{2} + \tan^{-1}\frac{1}{\sqrt{M^2-1}}\right)\right) \qquad (7\text{-}8)$$

where M is defined as $M = \frac{V_{cs} + nV_o}{V_{in,peak}}$. Note that the bulk capacitor voltage is independent of the load resistance. Therefore, as the load changes, the change in duty cycle is necessary to maintain a constant output voltage so that the input and output power remain equal, with no net change in the energy stored in the converter over the half line cycle. Since the input inductor operates discontinuously and the flyback transformer operates in critical conduction mode, this zero change in energy implies that the bulk capacitor voltage stays constant for changing loads.

However, the voltage does depend on converter parameters and on the input voltage. While the output power through the flyback converter is more dependant on the bulk capacitor voltage than the input voltage, the input power can be maintained constant by increasing the effective boost gain-- The bulk capacitor voltage increases by a greater amount than the input voltage such that the down slope of the input inductor current is higher, thereby reducing the averaging input current and hence the input power. With the higher bulk capacitor voltage, the duty cycle must also decrease marginally to ensure the

power through the flyback section also remains constant. Therefore, a balance is reached whereby the bulk capacitor voltage increases slightly and the duty cycle decreases marginally for an increase in the input voltage.

7.2.1.3 Maintaining Discontinuous Conduction Mode

As well as ensuring that the boost converter operates in discontinuous mode to achieve better current shaping and the flyback operates in critical conduction mode, the BIFRED converter must be designed such that the input inductor current becomes discontinuous before the current in the magnetizing inductance of the flyback transformer reaches zero. Otherwise, there is a risk that the bulk capacitor voltage would be insufficient to cause the input inductor current to decay to zero before the next switching cycle.

The condition for ensuring correct operation is given by,

$$\frac{V_{cs}}{V_{in,peak}} \geq 1 \qquad (7\text{-}9)$$

If $V_{in,peak} \geq V_{cs}$, then for operation near the peak of the input voltage, a current would begin to build up in the input inductor and the magnetizing inductance as soon as the flyback output diode had ceased conducting. After a few switching cycles, the input inductor current would be continuous. To ensure that this current remains discontinuous, the input inductance and magnetizing inductance must be selected so that the bulk capacitor voltage is always greater than the input voltage, i.e. similar to the condition for a normal boost converter.

To ensure that the flyback section of the converter remains discontinuous, the magnetizing inductance of the transformer must be limited to a value that will allow

discontinuous operation for the maximum output power and for the minimum bulk capacitor voltage. When operating at the cusp of the input voltage, the energy contribution from the boost input is zero and hence all the energy is supplied by the bulk capacitor. Therefore, the switch on-time is maximum at this point and hence the maximum magnetizing inductance referred to the primary is

$$L_{p,max} = \frac{(\frac{V_{cr,min} nV_o}{V_{cr,min} + nV_o})^2 T_s}{2P_{out,max}} \qquad (7\text{-}10)$$

To ensure that the converter operates in the correct mode, the magnetizing inductance must be calculated from above equation and then the input inductance can be selected by setting the bulk capacitor voltage equal to the peak of the minimum input voltage.

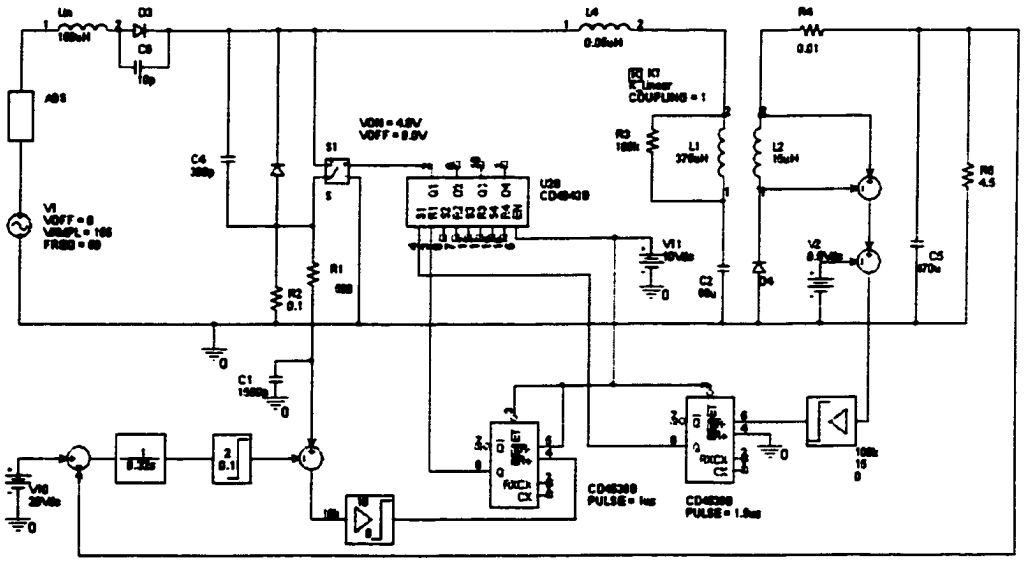
7.2.2 Simulated Verifications

Simulations have been carried out to verify the analysis above. Figure 7-3 (a) gives the simulation scheme with the critical conduction DC-DC conversion for an 85~265V/50Hz input, 20V@4.5A output design example.

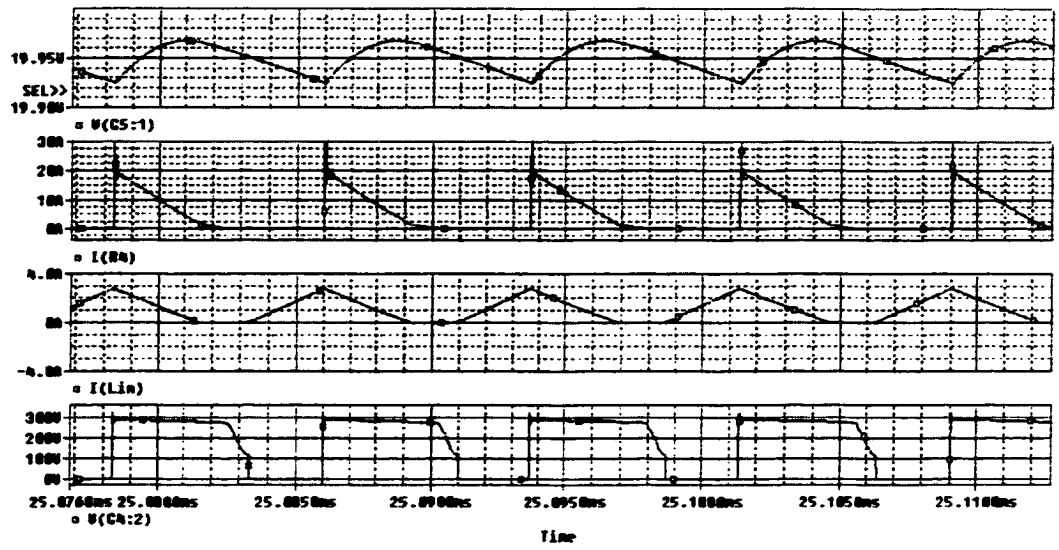
Figure 7-3(b) and (c) give the simulated operation waveforms when the input voltage nears its peak and zero in one line cycle, respectively.

The first trace shows that the output voltage to indicate the proposed critical conduction control scheme can obtain pretty small high frequency output ripple. The second trace indicates the flyback transformer did operate in critical conduction mode, and the switch is turned on when the current flowing through the secondary reaches zero. Besides, in each switching cycle, direct energy transfer occurs as shown in shadowed

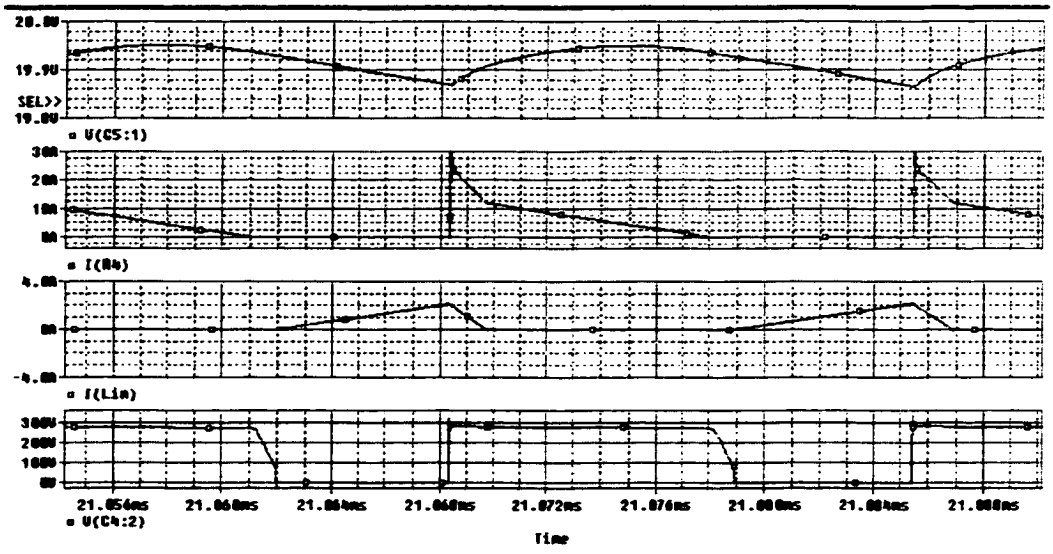
area in Fig. 7.2. The third trace indicates discontinuous conduction current in the PFC boost inductor. It is obvious that the switching frequency is higher when input voltage is near its peak value. The fourth trace shows the voltage across the switch, it can be seen that before the switch is turn on, the voltage has been reduced to a pretty low value. Assuming that the parasite capacitance across the switch is C_{ds}, previous turn on losses $\frac{1}{2}C_{ds}V_{ds}^2$ will be reduced to $\frac{1}{2}C_{ds}V_{ds}'^2$. Since V_{ds}' is much small compared to V_{ds}, a significant amount of energy will be saved.



(a) Simulation circuit



(b) Simulation waveforms when input voltage around peak value in one line cycle



(c) Simulation waveforms when input voltage around zero in one line cycle

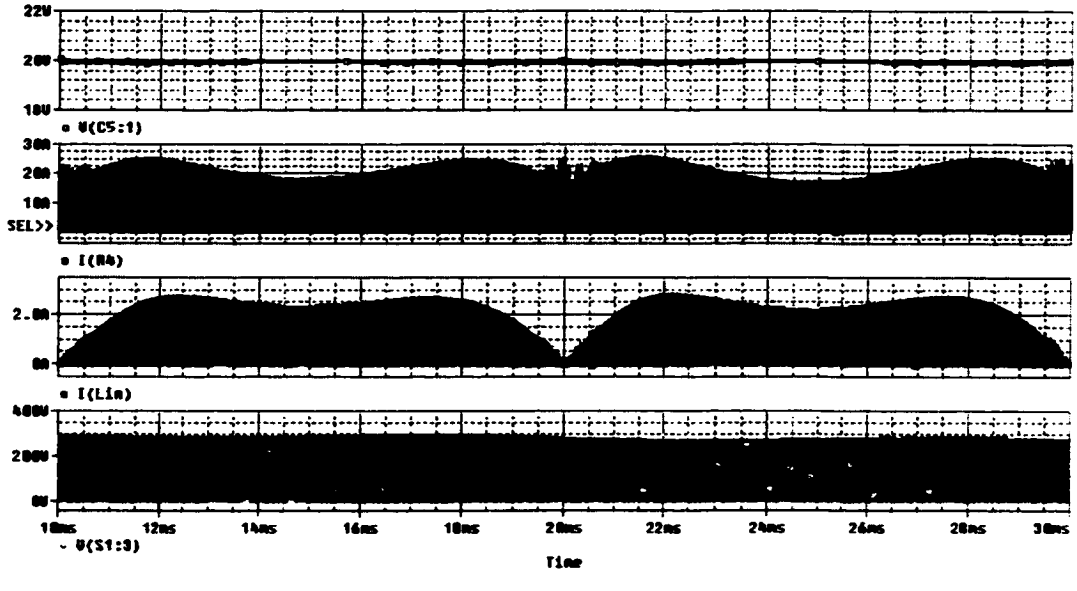
Fig. 7-3 Critical conduction mode control simulation circuit and detailed waveforms

Figure 7-4 gives the simulated operation waveforms in one line cycle.

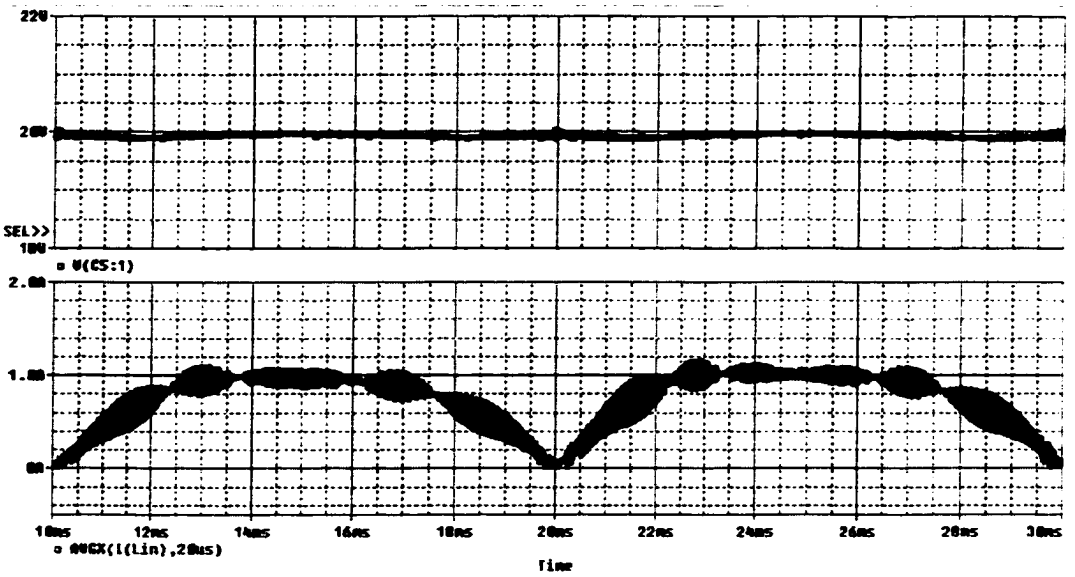
Figure 7-4(a) presents the operation envelop for key parameters in one line cycle. The first trace shows the output voltage to indicate that the line frequency output ripple is also less than 200mv, 1% of the output voltage; The second trace indicates the current

flowing through the secondary or flyback transformer. It can be seen that due to current mode control, secondary of flyback transformer carries higher current when input voltage near zero since ON time increases to reach the threshold of current limit. The third trace indicates the current envelope in the PFC boost inductor, it is obvious that higher switching frequency when input voltage near its peak value reduces the current stress and helps to achieve higher efficiency and a better power factor. The fourth trace shows the voltage across the switch.

Figure 7-4(b) shows the output voltage and averaged input current in one line cycle. It can be seen that the critical conduction mode can also achieve desired flat top current shaping capability.



(a) Simulation waveforms in one line cycle



(b) Output voltage and averaged input Line current

Fig. 7-4 Simulation waveforms in one line cycle

Figure 7-5 presents the low cost critical conduction mode PFC AC-DC adapter scheme with least components.

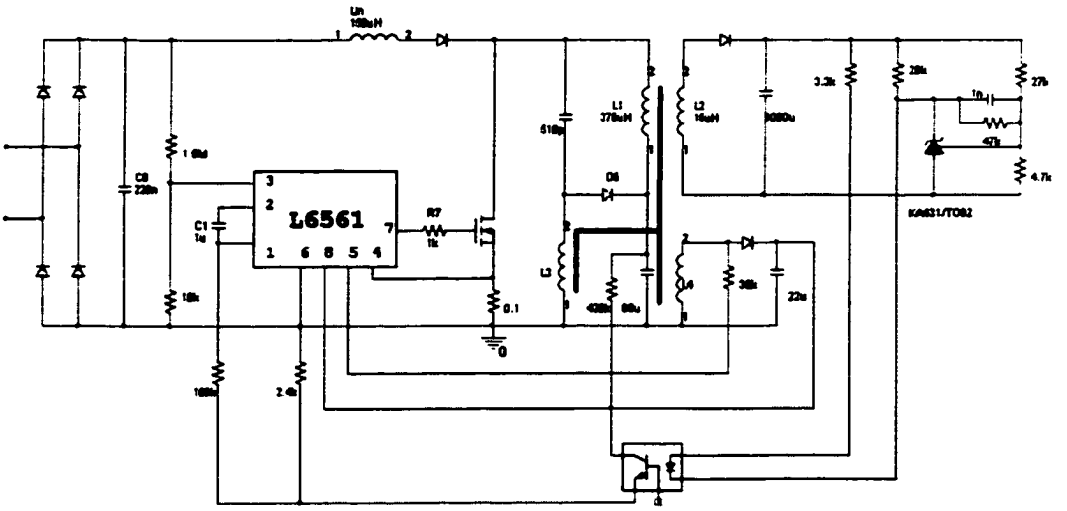


Fig. 7-5 Experimental setup based on the proposed topology shown in Fig. 4-11(a)

7.3 Derived Critical Conduction Scheme for Single-stage PFC AC-DC Conversion

In the previous section, we found out that the parameters must be well designed to assure that the current in the boost inductor decreases to zero before the current through the secondary winding of the flyback transformer reduces to zero. For universal input applications, selection of the boost inductor must be compromised for both high and low line conditions, high line input prefer higher inductance to have reduced current stress and lower RMS current, low line input have to select lower inductance to avoid input current distortion results from the CCM operation of the boost inductor. In addition, for practical products, parameter tolerance should also be taken into account. Therefore, boost inductance selection has to greatly sacrifice high line input performance, and particularly the efficiency.

Now let us examine again the critical control scheme for the flyback DC-DC cell, as shown in Fig. 7-6. The switch is turned on the moment the current is flowing through the secondary or flyback transformer reaches zero, regardless of the status of the current flowing through the boost inductor. If we take the boost inductor current state as another dominator to turn on the switch, the operation modes of the converter might be switched from DCM PFC plus critical conduction mode DC-DC to critical conduction mode PFC plus DCM DC-DC. Either case could avoid excessive DC bus voltage stress. Also, input current distortion resulted from CCM operation in the PFC stage will be eliminated, so higher inductance could be implemented for universal application to reduce current stress and RMS current to have higher efficiency.

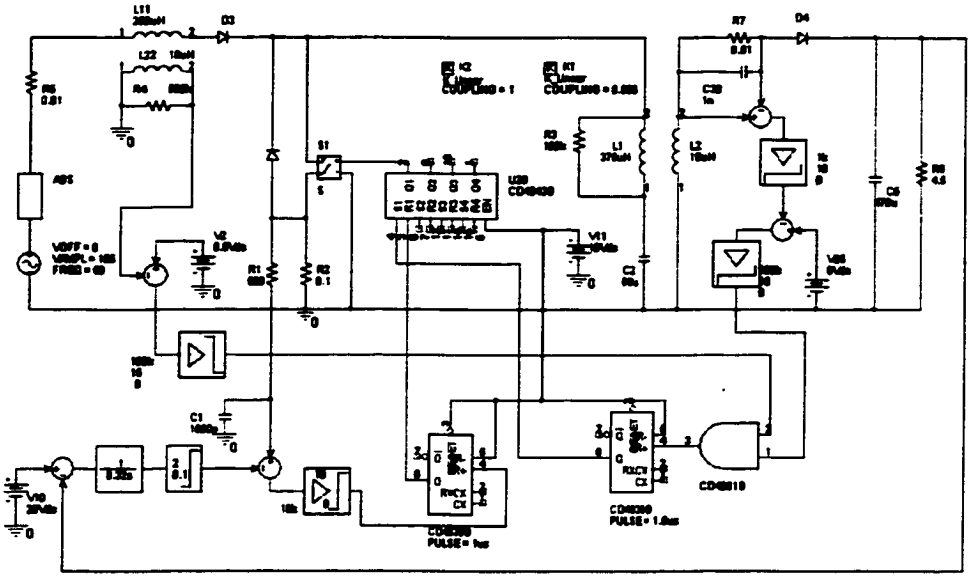


Fig. 7-6 Derived critical conduction control scheme

Figure 7-7 presents simulation results with a derived critical conduction control scheme. It can be seen that sound power factor correction and low output ripple have been obtained when input inductance has been increased from 150uH in Fig.7-3 (a) to 250uH. Such a control scheme could also be transplanted into other single-stage PFC AC-DC converters.

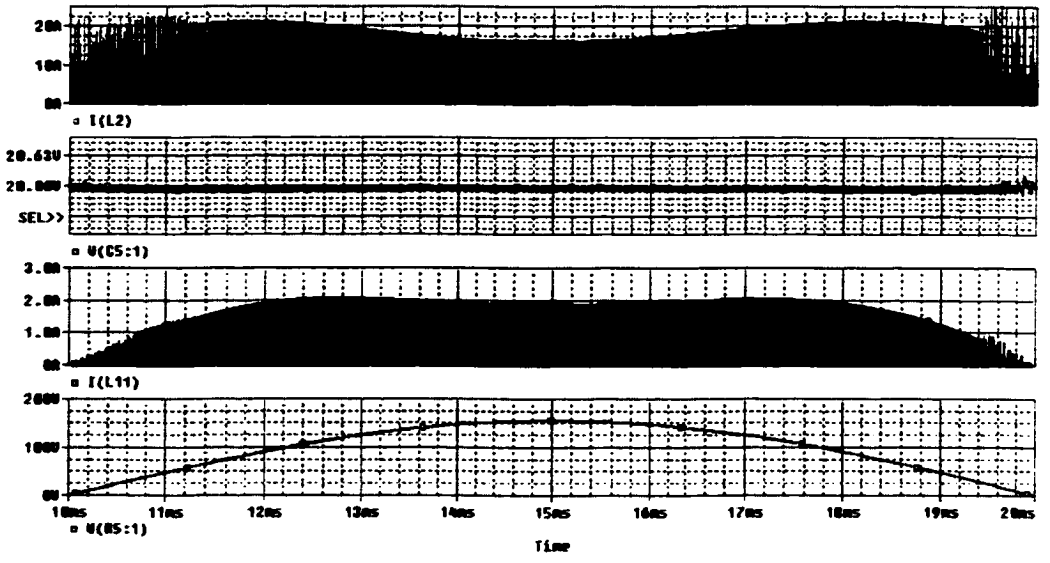


Fig. 7-7 Simulation results with derived critical conduction control scheme

In single-stage PFC AC-DC converters, flyback might be the best choice for DC-DC conversion cell from the standpoint of cost. Current mode control brings in several advantages such as improved transient performance, line ripple ripple rejection and automatic current limit.

For the current mode flyback converter, CCM operation normally accompanied with less RMS current, lowers turn-off losses and therefore, increases efficiency. However, to stabilize the system might be difficult, since the flyback topology has an inherent Right Half Plane Zero (RHPZ). DCM operation offers improved dynamic performance and easier compensation network design, but suffers from higher current stress and switch turn-off losses. Critical conduction mode, which operates at the boundary of continuous and discontinuous conduction modes, features high frequency response, lower current stress and soft switching potential.

Critical conduction mode could be transplanted into single-stage PFC AC-DC converter. BIFRED converters, which do not need galvanic isolation compare with previous topologies, are taken as an example for introducing such a control scheme. Detailed analysis and system simulation indicated that lower current stress, soft switching and low DC bus voltage stress can be achieved with critical conduction mode control. For a single-stage PFC AC-DC conversion, derived critical conduction mode can be implemented to assure no CCM operation appeared in PFC cell and DC-DC cell under any case. Thereafter a higher boost inductor could be used to have lower current stress and still keep the capability to eliminate current distortion results from PFC cell CCM operation and high DC bus voltage stress results from DC-DC cell CCM operation.

8. SUMMARY

This dissertation explores advanced techniques in single-stage power factor correction AC-DC conversion, with the objective of achieving improvements in converter topology, system performance and cost-effectiveness over conventional approaches. Major conclusions achieved are summarized as follows:

Many single-stage PFC can be viewed as a combination of the DC-DC converter with a 2-terminal or 3-terminal PFC cell. From generalized S^2 PFC AC-DC approaches, we found that many reported single-stage PFC converters are electrically equivalent despite that they are topologically different, because they employ equivalent PFC cells although their configurations are different. The key issues of the current S^2 PFC AC-DC converter can be explained, to a certain extent, from its topological features. It is possible for S^2 PFC AC-DC converters, as state-of-the-art electronics systems, to overcome the main drawbacks by breaking the confinement of current PFC cells, and employing proper topologies capable of changing current energy transferring modes. Two solutions are proposed in this dissertation: First, it is not necessary that the energy stored in the PFC inductor must be discharged to the buffer capacitor; Second, it's not necessary that all of the power transferred to the output have to be stored in the Boost PFC inductor first.

CCM operation of the DC-DC cell in the S^2 PFC AC-DC converter is preferred due to its higher efficiency. However, it is proved in this dissertation that it will bring about

high bus voltage stress generally beyond the tolerance of commercially available capacitors. Light load DCM and heavy load CCM hybrid operation mode can suppress the voltage stress, but it is still not the ideal solution. Employing an additional energy discharge path for the boost inductor can reduce the energy charged to the buffer capacitor, thereafter to reduce its voltage, while introducing a bi-directional DC-DC transformer has the ability to further reduce the voltage stress across the bulk capacitor, since the energy stored in PFC inductor charges the capacitor through an equivalent voltage source.

The PFC stage in the S^2 PFC AC-DC converter normally operates in DCM mode to utilize its inherent current shaping capability, therefore, compared with cascading two-stage schemes, the S^2 PFC AC-DC conversion has higher current stress. Current stress not only accompanies with increased switching losses and lower efficiency, but also brings about annoying EMI issues. Providing another parallel path for the boost inductor can obtain flat top input current and thereof reduce the current stress. Setting up another discharging path for the boost inductor can change its discharging mode, thus achieving reduced current stress. The PFC stage CCM operation utilizing a resonant tank has the least current stress, however, it is at the penalty of lower power factor.

Better energy management techniques, including processing less energy or processing it with higher efficiency are introduced in this dissertation. Providing another discharging path in the output side for the Boost PFC inductor and adopting a bi-directional DC-DC converter is a simple and effective solution for processing less

energy. Implementing an active clamp cell to achieve soft switching can further improve the efficiency and boost switching frequency and power density.

Current mode control brings in several advantages such as improved transient performance, line ripple rejection, and automatic current limit. For a current mode flyback converter, CCM operation is normally accompanied with less RMS current, lower turn-off losses and thereafter, higher efficiency. However, stabilizing the system might be difficult since flyback topology has inherent Right Half Plane Zero (RHPZ). DCM operation offers improved dynamic performance and easier compensation network design, but suffers from higher current stress and switch turn-off losses. Critical conduction mode, which is operating at the boundary of continuous and discontinuous conduction modes, features high frequency response, lower current stress and soft switching potential.

Critical conduction mode could be transplanted into a single-stage PFC AC-DC converter to achieve reduced current stress, low DC bus voltage stress and reduced turn on switching losses. In addition, a derived critical conduction control scheme, which take into account both current status in the PFC cell and DC-DC cell can be implemented to assure that no CCM operation appeared in PFC cell and DC-DC cell under any case. Such a control scheme allows implementing a higher boost inductor to have lower current stress and still keeps the capability to eliminate current distortion result from PFC cell CCM operation and high DC bus voltage stress resulting from DC-DC cell CCM operation.

The proposed concepts have been verified by simulation and experiment results, and the prototype employing these techniques present the following features:

1. *Reduced cost and improved reliability:* This is due to the least components being incorporated.

2. *Reduced current stress:* The operation mode of a traditional boost inductor has been modified to reduce the peak value of input current when transferring the same average input current. Therefore, the main switch can be turned off under reduced current stress.

3. *Reduced voltage stress:* The storage capacitor is charged under the governing mode: $V_{cs} < V_{in}(t) + n_1 V_0 - n_2 V_0$, therefore, the DC bus voltage can be well controlled above the peak value of the input voltage. As a consequence, the commercially available capacitor can be used. Moreover, 600V components can be used in the power stage for universal input applications.

4. *Less energy processing:* Both the additional discharge path for the Boost PFC inductor and Bi-directional DC-DC cell will transfer the input power directly to the output .

5. *Higher efficiency:* More than half of the energy transferred straight to the load certainly can increase the overall efficiency. For the currently existing cascade two-stage or single-stage approaches, basically, the power is processed serially by the PFC cell and DC-DC cell, the overall efficiency is given by the product of the two stage efficiencies, i.e., $\eta = \eta_1 \eta_2$, where η_1 and η_2 are the efficiencies of the two stages respectively. In the proposed topology, if we suppose k is the ratio at which power is

transferred to the output just through PFC stage, then the efficiency of the proposed structure can be expressed as $\eta = k\eta_1 + (1-k)\eta_1\eta_2 > \eta_1\eta_2$. Obviously, the overall efficiency can be improved by minimizing the power process times. In addition, reduced current stress and application of 600V components also brings about higher efficiency due to reduced switching and conduction losses.

6. ***Higher efficiency processing:*** An active clamp cell can reduce the switching losses and further improve the system conversion efficiency.

7. ***High frequency response and system stability:*** Since the PFC cell normally uses boost topology and the DC-DC cell prefers a boost derived topology, called flyback, both of them have inherent right half plane zero when operating in CCM mode. The proposed critical conduction mode control scheme and its derivations can assure complete energy transfer in each switching cycle, therefore it has excellent system stability and high frequency response.

8. ***High power application:*** Multiple energy transferring paths have the potential to increase the power conversion rating and also release the thermal design difficulties due to distributed heat dissipation.

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