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SINGLE-STAGE SINGLE-SWITCH POWER FACTOR CORRECTION CIRCUITS: ANALYSIS, DESIGN AND IMPLEMENTATION

by

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ABSTRACT

As a branch of active power factor correction (PFC) techniques, the single-stage single-switch (S^4) technique receives particular attention because of its low cost implementation. Using DCM converter in front of the line to achieve high power factor operation can further reduce the power supply cost. The performance of such kind of AC/DC converter strongly depends on the complexity of its circuit topology. However analysis and design of the DCM-S^4 converter is yet to be formulated. In this dissertation, new methods to analyze and design the S^4-PFC converters have been developed. These methods are generally suitable for all kinds of DCM-S^4 converters. This dissertation also gives an overview of recent active PFC techniques. Based on the general study and review of the S^4-PFC technique, four converter topologies have been proposed with emphasis on different applications. Analysis and design of these converter topologies are presented with simulation and experimental verifications. For all these converters, high input power factor and acceptable efficiency have been achieved. The low voltage stresses on the storage capacitors for these converters result in low cost implementation of the proposed topologies.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

1.1.1 The Needs for Harmonics Reduction and Power Factor Correction in Utility Power System

For hundreds of years past, people have been aware of the necessity of the natural environment protection of the earth they live in. Nowadays, programmed utilization of natural resource has been recognized as important natural agenda item. Like our earth, the utility power supply that we are now using in every aspect of life was clean when it was invented in 19th century. Meanwhile, due to the intensive use of this utility fueled by unprecedented technological progress in the last fifty years, the power supply condition becomes "polluted". However, public concern about the "dirty" environment in the power system has not been drawn until early of 1980's [1-6].

Since ac electrical energy is the most convenient form of energy to be generated, transmitted and distributed, ac power systems had been swiftly introduced into industries and residences. With the proliferation of utilization of electrical energy, more and more heavy loads have been connected into the power system. During 1960's, large electricity consumers such as electrochemical and electro-metallurgical industries applied capacitors as VAR compensator to their systems to minimize the demanded charges from utility companies and to stabilize the supply voltages. As these capacitors present low

impedance in the system, harmonic currents are drawn from the line. Owing to the non-zero system impedance, line voltage distortion will be incurred and propagated. The contaminative harmonics can degrade power quality and affect the system performance in the following ways:

(a) As the current harmonics increase the *rms* value of the total current, they do not deliver any real energy in Watts to the load, resulting in inefficient use of equipment capacity and unnecessary over rating (i.e. low power factor).

(b) Harmonics will increase conductor loss and iron loss in transformers, decreasing transmission efficiency and causing thermal problems.

(c) The odd-order harmonics are extremely harmful to a three-phase system, causing overload of the unprotected neutral conductor.

(d) Oscillation in power system should be absolutely prevented in order to avoid endangering the stability of system operation.

(e) High peak harmonic currents may cause automatic relay protection devices to mis-trigger.

(f) Harmonics could cause other problems such as electromagnetic interference to interrupt communication, degrading reliability of electrical equipment, increasing product defective ratio, insulation failure, audible noise, etc.

Perhaps the greatest impact of harmonic pollution appeared in early 1970's when static VAR compensators (SVCs) were extensively used for electric arc furnaces, metal rolling mills and other high power appliances. The harmonic currents produced by partial conduction of SVC are odd-order, which are especially harmful to three-phase power

system. Harmonics can affect operations of other devices that are connected to the same system and, in some situation, their own operations of those who generate the harmonics.

The ever deteriorated supply environment did not become of major concern until the early 1980's when the first technical standard IEEE519-1981with respect to harmonic control at point of common coupling (PCC) was issued [8-9]. The significance of issuing this standard was not only that it provided the technical reference for design engineers and manufactures, but also that it opened the door for further research in harmonic reduction and power factor correction (PFC). Stimulated by the harmonic control regulation, researchers and industry users started to develop low-cost devices and power electronic systems to **reduce** harmonics since it is neither economical nor necessary to eliminate the harmonics.

Research on harmonic reduction and power factor correction has become intensified during the last ten years. With the rapid development in power semiconductor devices, power electronic systems have matured and expanded to new and wide application rage from residential, commercial, aerospace to military and other applications. Power electronic interfaces, such as switch mode power supplies (SMPS), are now clearly superior over the traditional linear power supplies, resulting in more and more interfaces switched into power systems. While the SMPSs are highly efficient, but because of their non-linear behavior, they draw distorted current from the line, resulting in high total harmonic distortion (THD) and low power factor (PF). To achieve a smaller output voltage ripple, practical switch-mode power supplies use a large electrolytic capacitor at the output side of the single-phase rectifier. Since the rectifier diodes conduct only when the line voltage is higher than the capacitor voltage, the power supply draws

high *rms* pulsating line current. As a result, high THD and poor power factor (usually less than 0.67) are present in such power systems [6-10]. Even though each device, individually, dose not present much serious problem with the harmonic current, utility power supply condition could be deteriorated by the massive use of such systems. In recent years, declining power quality has become an important issue and continues to be recognized by government regulatory agencies. With the introduction of compulsory and more stringent technical standard such as IEC1000-3-2, more and more researchers from both in industries and universities are focusing in the area of harmonic reduction and power factor correction, resulting in numerous circuit topologies and control strategies.

Generally, the solution for harmonic reduction and PFC are classified into passive approach and active approach. The passive approach offers the advantages of high reliability, high power handling capability and easy to design and maintain. However, the operation of passive compensation system is strongly dependent on the power system and does not achieve high power factor. While the passive approach can be still the best choice in many high power applications, the active approach dominates the low to medium power applications due to their extraordinary performance (unity power factor and efficiency approach to 100%), regulation capabilities and high density. With the power handling capability of power semiconductor devices being extended to megawatts, the active power electronic systems tend to replace most of the passive power processing devices [2-4].

Today's harmonic reduction and PFC techniques to improve distortion are still under development. Power supply industries are undergoing the change of adopting more and more PFC techniques in all off-line power supplies.

1.1.2 Definition of Power Factor and Total Harmonic Distortion

Power factor is a very important parameter in power electronics because it gives a measure of how effective the real power utilization in the system is. It also represents a measure of distortion of the line voltage and the line current and phase shift between them. Referring to Fig. 1-1(a), we define the input power factor at terminal a-a' as the ratio of the average power and the apparent power measured at terminals a-a' as described in Eq. (1.1) [8-10]:

$$PowerFactor\,(PF) = \frac{Real\ Power(Average)}{Apparent\ Power}. \tag{1.1}$$

Here, the apparent power is defined as the product of *rms* values of $v_s(t)$ and $i_s(t)$.

In a linear system, because load draws purely sinusoidal current and voltage, the power factor is only determined by the phase difference between $v_s(t)$ and $i_s(t)$. Equation (1.1) becomes,

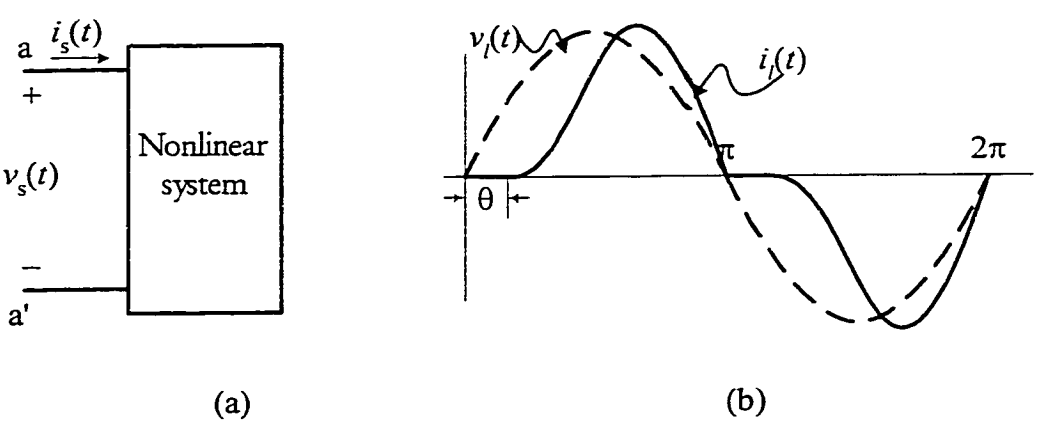


Figure 1-1 Nonlinear load draws distorted line current: (a) nonlinear system connected to the line; (b) line voltage and current waveforms

$$PF = \frac{I_{s,rms} V_{s,rms} \cos\theta}{I_{s,rms} V_{s,rms}} = \cos\theta \tag{1.2}$$

where, $I_{s,rms}$ and $V_{s,rms}$ are *rms* values of line current and line voltage, respectively, and θ is the phase shift between line current and line voltage. Hence, in linear power systems, the power factor is simply equal to the cosine of the phase-angle between the current and voltage. However, in power electronic system, due to the nonlinear behavior of active switching power devices, the phase-angle representation alone is not valid. Figure 1-1(b) shows that the nonlinear load draws typical distorted line current form the line. Calculating power factor for distorted waveforms is more complex when compared with the sinusoidal case. If both line voltage and line current are distorted, then Eqs. (1.3) and (1.4) give the Fourier expansion representations for the line current and line voltage, respectively:

$$i_s(t) = I_{DC} + \sum_{n=1}^{\infty} I_{sn} \sin(n\omega t + \theta_{in}) = I_{DC} + I_{s1} \sin(\omega t + \theta_{i1}) + \sum_{n=2}^{\infty} I_{sn} \sin(n\omega t + \theta_{in}) \tag{1.3}$$

$$v_s(t) = V_{DC} + \sum_{n=1}^{\infty} V_{sn} \sin(n\omega t + \theta_{vn}) = V_{DC} + V_{s1} \sin(\omega t + \theta_{v1}) + \sum_{n=2}^{\infty} V_{sn} \sin(n\omega t + \theta_{vn}) \tag{1.4}$$

Applying the definition of power factor given in Eq. (1.1) to the distorted current and voltage waveforms of Eqs. (1.3) and (1.4), power factor PF may be expressed as

$$PF = \frac{\sum_{n=1}^{\infty} I_{sn,rms} V_{sn,rms} \cos\theta_n}{I_{s,rms} V_{s,rms}} = \frac{\sum_{n=1}^{\infty} I_{sn,rms} V_{sn,rms} \cos\theta_n}{\sqrt{\sum_{n=1}^{\infty} I_{sn,rms}^2 \sum_{n=1}^{\infty} V_{sn,rms}^2}} \tag{1.5}$$

where, $V_{sn.rms}$ and $I_{sn.rms}$ are the *rms* values of the n^{th} harmonic voltage and current, respectively, and θ_n is the phase shift between the n^{th} harmonic voltage and the n^{th} harmonic current.

Since most of power electronic systems draw their input voltage from a stable line voltage source $v_s(t)$, the above expression can be significantly simplified by assuming the line voltage is pure sinusoidal and distortion only limited to $i_s(t)$, i.e.,

$$v_s(t) = V_s \sin \omega t \tag{1.6}$$

$$i_s(t) = \text{distorted (non-sinusoidal).} \tag{1.7}$$

Then it can be shown the power factor can be expressed as

$$PF = \frac{I_{s1.rms}}{I_{s.rms}} \cos\theta_1 = k_{dist} \cdot k_{disp} \tag{1.8}$$

where,

θ_1: the phase angle between the voltage $v_s(t)$ and the fundamental component of $i_s(t)$;

$I_{s1,rms}$: *rms* value of the fundamental component in line current;

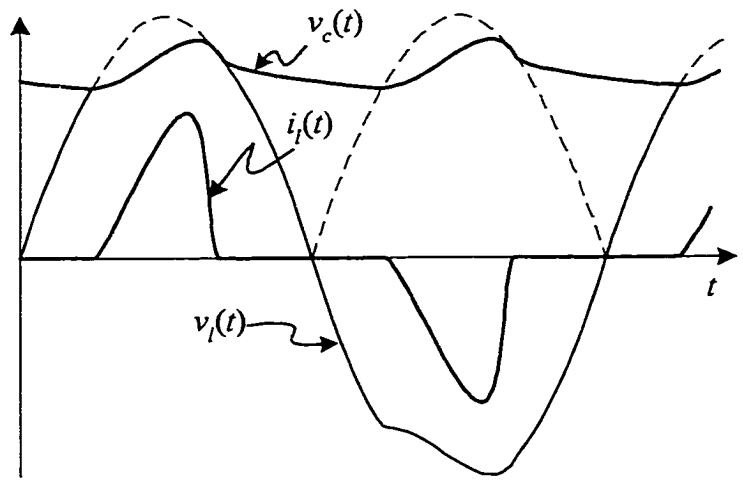
$I_{s,rms}$: total *rms* value of line current;

$k_{dist} = I_{s1.rms}/I_{s.rms}$: distortion factor;

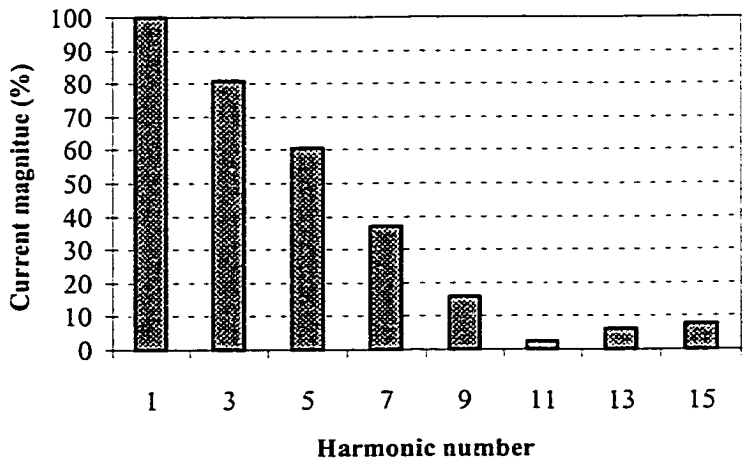
$k_{disp} = \cos\theta_1$: displacement factor.

Another important parameter that measure the percentage of distortion is known as the current Total Harmonic Distortion (THD_i) which is defined as follows,

$$THD_i = \sqrt{\frac{\sum_{n=2}^{\infty} I_{sn.rms}^2}{I_{s1.rms}^2}} = \sqrt{\frac{1}{k_{dist}^2} - 1} \ . \tag{1.9}$$



(a)



(b)

Figure 1-2 Conventional switch-mode power supplies suffer from harmonic distortion and poor power factor: (a) typical waveforms of a conventional switch-mode power supply; (b) spectrum of typical switch-mode power supply

1.1.3 Conventional AC/DC Power Supply

Conventionally switch-mode power supplies use capacitive rectifiers in front of the ac line which resulting in the capacitor voltage v_c and high *rms* pulsating line current $i_l(t)$ as shown in Fig. 1-2(a), when $v_l(t)$ is the line voltage. Such line current is full of odd numbers harmonics as it can be shown in Fig. 1-2 (b). As a result, THD_i is as high as 0.7 and poor power factor is usually less than 0.67.

As we can see from Eqs. (1.8) and (1.9), power factor and total harmonic distortion are related to distortion and displacement factors. Therefore, improvement in power factor also implies harmonic reduction.

1.1.4 Harmonic Standards

The publication of specific national and international standards becomes one aspect of the most important momentum to thrust the contemporary power electronic industry. It encourages the researchers to develop more efficient power electronic system to comply with these standards. With regard to harmonic control, **IEC 1000-3-2** and **IEC 1000-3-4** (recommended by International Electrotechnical Commission (IEC)), and **IEEE 519-1992** (recommended by the Institute of Electrical and Electronics Engineers (IEEE), Inc.) are commonly recognized. The applications of these standards refer to different equipment size and supply point.

The IEC 1000-3-2 sets limits for the harmonic currents generated by electrical and electronic equipment drawing input current up to 16A/phase. The standard categorizes the equipment into four classes. Class A includes all the balanced three-phase equipment and all other equipment that do not belong to Classes B, C and D; Class B is for portable tools; Class C is for lighting equipment; Class D is for the equipment draws pulsating

current with single hump in half line cycle and has input power between 50W to 600W. Since most of the power electronic systems can be categorized into Class D, it receives particular attention in the power electronic industry. Table 1-1 lists the harmonic current limits for Class D equipment. The maximum permissible harmonic currents are given in both mA/Watt and absolute Amper.

Table 1-1 IEC 1000-3-2 harmonic limits for Class D equipment

Harmonic order n	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \le n \le 39$ (odd harmonics only)	38.5/n	Refer to Class A

Table 1-2 IEC 1000-3-4 harmonic limits for equipment with $R_{SCC} \ge 33$

Harmonic number n	Admissible harmonic current I_n/I_1(%)	Harmonic number n	Admissible harmonic current I_n/I_1(%)
3	21.6	21	≤0.6
5	10.7	23	0.9
7	7.2	25	0.8
9	3.8	27	≤0.6
11	3.1	29	0.7
13	2.0	31	0.7
15	0.7	≥33	≤0.6
17	1.2		
19	1.1	even	≤8/n or 0.6

The IEC 1000-3-4 deals with the equipment that draws line current higher than 16A. This standard gives certain consideration of the equipment size and the system size by defining a ratio R_{SCC} of short-circuit current to nominal current at the connection point. Table 1-2 shows the limits for equipment with R_{SCC} larger than 33.

The standard IEEE 519-1992 does not mention requirements for any equipment because the main concern in this standard is on system measurements. Instead, the harmonic current limits have been imposed on the so-called point of common coupling (PCC), where the consumer is connected to the utility. The harmonic current limits depend on the size of the load compared with the size of the supply system at the PCC. Table 1-3 gives current distortion limits for systems from 120V to 69kV, where I_{SC}/I_L is the ratio of the short-circuit current available at the PCC to the fundamental component of the maximum demand load current (average value of maximum demand over the previous 12 months). TDD is total demand distortion, which is defined as the total root-sum-square harmonic current distortion in percent of the maximum demand load current.

Table 1-3 IEEE 519-1992 maximum odd harmonic current distortion in % of I_L

I_{SC}/I_L	<11	11≤ h <17	17 ≤ h< 23	23 ≤ h <35	35≤ h	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100< 1000	12.0	5.5	5.0	2.0	1.0	15.0
1000 >	15.0	7.0	6.0	2.5	1.4	20.0

h: harmonic number.

1.2 RESEARCH OBJECTIVES

The objectives of this research are:

- To investigate various recent techniques in single-phase harmonic reduction and power factor correction.
- To formulate the theory of single-phase AC/DC converter with harmonic reduction and power factor correction.
- To develop new AC/DC converter topologies with low cost.

- To develop new AC/DC converter topologies with improved performance.
- To develop new AC/DC converter topologies for different applications.

1.3 OUTLINE OF THIS DISSERTATION

The needs for power factor correction and harmonic reduction in utility power supply and research background are introduced in Chapter 1. In Chapter 2, the principle of operation of active power factor correction circuit is generally discussed. A new method of analyzing and designing S^4 converter has been proposed. Chapter 3 gives an overview of recent techniques in active power factor correction. Two new converter topologies have been proposed in Chapter 4 with emphasis on high power factor and low storage capacitor voltage stress operation. In Chapter 5, a soft-switching single-stage AC/DC converter and a low-voltage S^4 converter have been presented. Finally, in Chapter 6, we summarized the dissertation and draw some conclusions.

CHAPTER 2

GENERAL PRINCIPLE OF OPERATION OF PFC CIRCUITS

2.1 INTRODUCTION

At the line side, unity power factor operation requires the power consumer draw instantaneous power flow in alternative way. However, the power consumer usually needs a constant DC power flow. Therefore the basic task of a power factor corrector is to buffer the power flow. A lot of circuits can be served as power factor corrector, but their performances are not the same. High-frequency switching technique has been successfully used in PFC AC/DC power conversion. However analysis and design of the converter are yet to be formulated. In this chapter, the principle of operation of power factor corrector will be generally discussed. Some new methods to analyze and design the S^4 converter will be developed. These methods are generally suitable for all kinds of DCM single-stage single-switch converters.

2.2 ENERGY BALANCE IN POWER FACTOR CORRECTION CIRCUITS

Figure 2-1 shows a diagram of an AC/DC PFC unit. Let $v_l(t)$ and $i_l(t)$ be the line voltage and line current, respectively. For an ideal PFC unit (PF = 1), we assume:

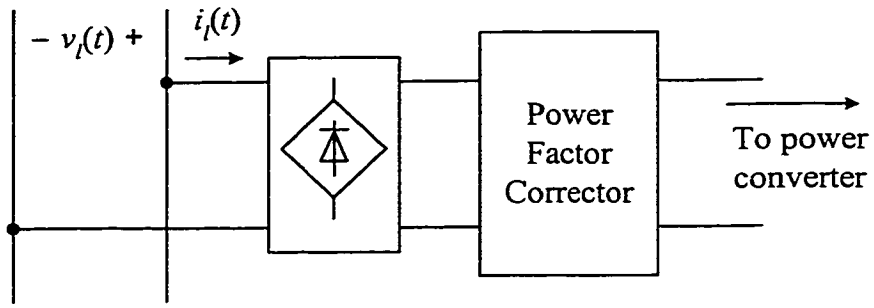


Figure 2-1 Block diagram of AC/DC PFC unit

$$v_l(t)=V_{lm}\sin\omega_l t\,; \tag{2.1a}$$

$$i_l(t)=I_{lm}\sin\omega_l t\ . \tag{2.1b}$$

where, V_{lm} and I_{lm} are amplitudes of line voltage and line current, respectively, and ω_l is the angular line frequency. The instantaneous input power is given by,

$$p_{in}(t)=V_{lm}\,I_{lm}\sin^2\omega_l t=P_{in}\left(1-\cos 2\omega_l t\right) \tag{2.2}$$

where, $P_{\text{in}}=\frac{1}{2}V_{lm}\,I_{lm}$ is the average input power.

As we can see from Eq. (2.2), the instantaneous input power contains not only the real power (average power) P_{in} component but also an alternative component with frequency $2\omega_l$ (i.e. 100Hz or 120Hz), shown in Fig. 2-2. Therefore, the operation principle of a PFC circuit is to process the input power in a certain way that it stores the excessive input energy (area I in Fig. 2-2) when $p_{in}(t)$ is larger than $P_{in}(=P_o)$, and releases the stored energy when $p_{in}(t)$ is less than $P_{in}(=P_o)$ to compensate for area II.

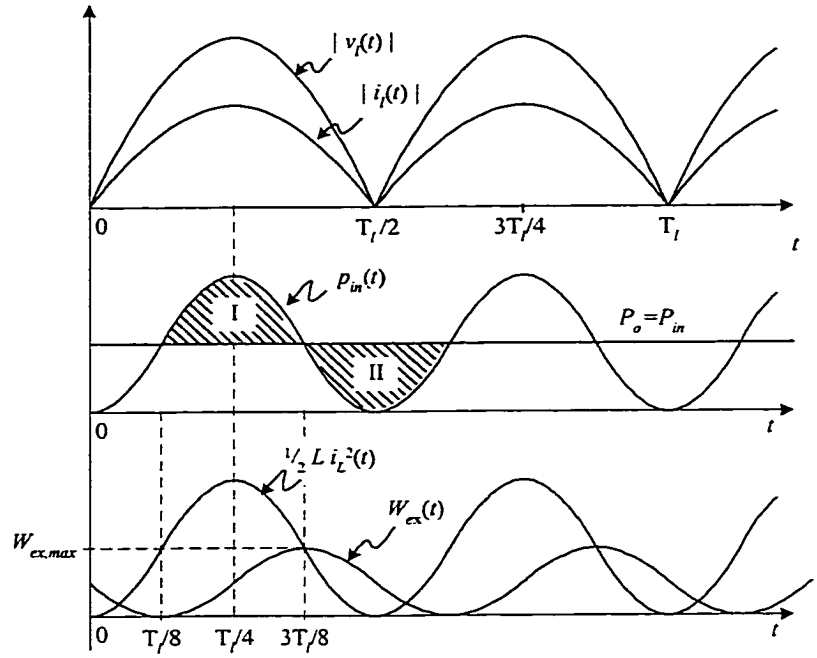


Figure 2-2 Energy balance in power factor corrector

The excessive input energy, $W_{ex}(t)$, is given by,

$$W_{ex}(t) = \frac{P_o}{2\omega_l}(1-\sin 2\omega_l t) \tag{2.3}$$

At $t = 3T_l/8$, the excessive input energy reaches the peak value:

$$W_{ex,max} = \frac{P_o}{\omega_l} \tag{2.4}$$

The excessive input energy has to be stored in the dynamic components (inductor and capacitor) in the PFC circuit. In most of the power factor correction circuits, an input inductor is used to carry the line current. For unity power factor, the inductor current (or averaged inductor current in switch mode PFC circuit) must be a pure sinusoidal and in

phase with the line voltage. The energy stored in the inductor ($\frac{1}{2}Li_L^2(t)$) cannot completely match (instantaneously) the change of the excessive energy as shown in Fig. 2-2. Therefore, to maintain the output power constant, another energy storage component (usually the output capacitor) is needed.

Generally speaking, compromise must be made between the input power factor and the output voltage ripple. In most cases, the output voltage of the power factor corrector cannot be used to supply the load since it is full of second harmonic. Therefore, a DC/DC converter, called post-regulator, is normally cascaded to the power factor corrector to tightly regulate the output voltage of the power supply. To address the feature in layout, the power factor corrector is also called front-end converter.

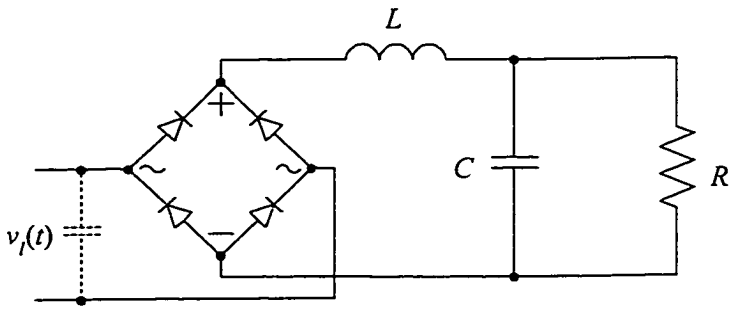


Figure 2-3 Inductive-input power factor corrector

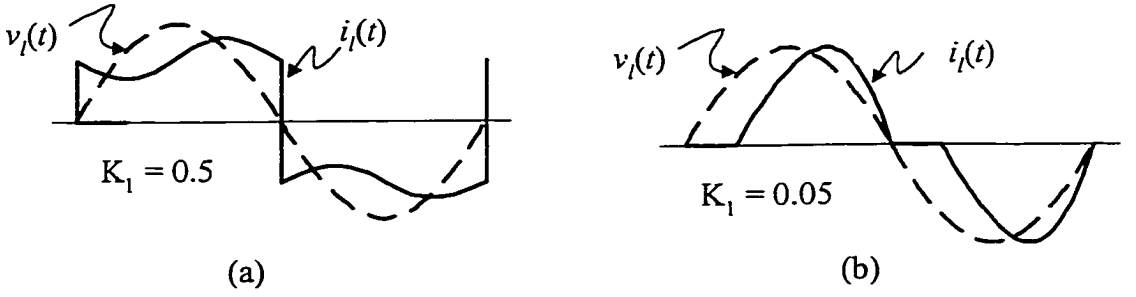


Figure 2-4 Input current waveform of an inductive-input filter:
(a) in CCM; (b) in DCM

The most common off-line passive PF corrector is the inductive-input filter, shown in Fig. 2-3. For operation in continuous conduction mode (CCM), the input current tends to be a square waveform in phase with the line voltage, shown in Fig. 2-4(a). Smaller output voltage ripple can be obtained at the output of the corrector due to nearly constant inductor current. However, the input current can trace the line voltage in shape. In another word, the input/output instantaneous power balance is only favorable to the constant DC output. Depending on the filter inductance, this circuit can give a maximum of 90% power factor [11]. When the input inductor operating in CCM, the power factor is given by,

$$PF = 0.9\sqrt{1 + (0.075/K_1)^2} \tag{2.5}$$

where,

$$K_1 = \frac{\omega L}{\pi R} \tag{2.6}$$

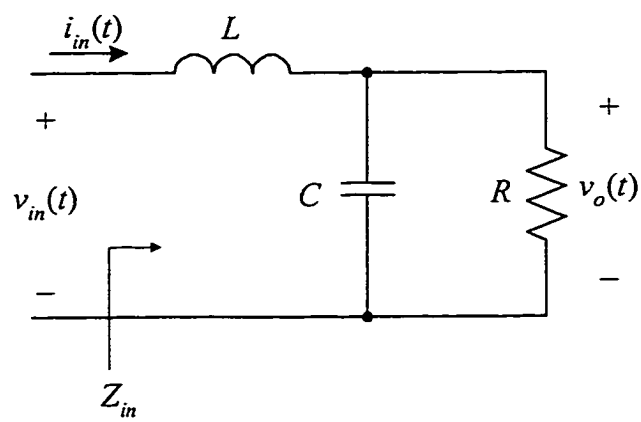


Figure 2-5 Low-pass filter

In DCM, the PF corrector is simply a low pass inductive filter as shown in Fig. 2-5, whose transfer function and input impedance are given by,

$$H(s)=\frac{V_o(s)}{V_{in}(s)}=\frac{1}{s^2LC+sL/R+1} \tag{2.7a}$$

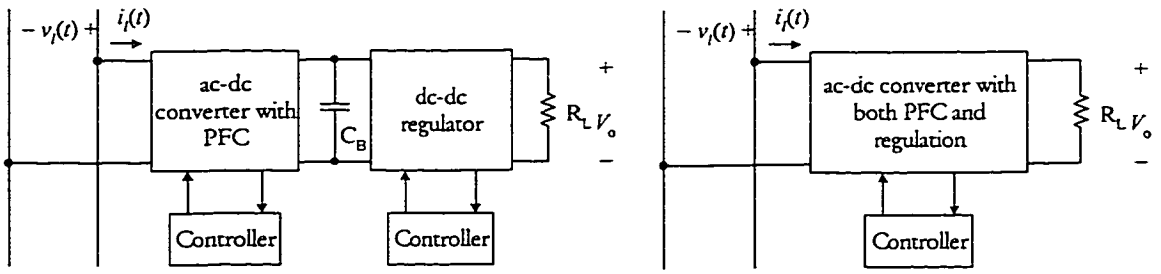
$$Z_{in}(s)=\frac{V_{in}(s)}{I_{in}(s)}=R\frac{s^2LC+sL/R+1}{sRC+1} \tag{2.7b}$$

Equation (2.7b) shows that in DCM operation, unavoidable phase displacement between $v_{in}(t)$ and $i_{in}(t)$ is incurred in the inductive-filter corrector. Nevertheless, since the inductor is charged only when the rectified line voltage is higher than the output voltage, dead region in the line current appears, shown in Fig. 2-4(b). Consequently, the inductive-filter in DCM is not able to balance the input and output power in an efficient way to give either good power factor or smaller output ripple.

In contrast to the passive PFC technique, the active PFC technique is more effective in improving input power factor. High-frequency switched semiconductor devices are introduced in this technique that aimed at forcing the input current to trace the line voltage in shape and phase. The input inductor can also operate in CCM or DCM. However, the concept should be understood in the sense of switching cycle. In next section, some inherent properties of the basic converter topologies will be discussed based on high-frequency power factor correction applications.

2.3 SYSTEM CONFIGURATIONS OF PFC POWER SUPPLY

Broadly speaking, a single output high-frequency PFC electronic system can be realized in two configurations, i.e. two-stage configuration (shown in Fig. 2-6(a)) and single-stage configuration (shown in Fig. 2-6(b)). In the two-stage configuration, an AC/DC converter is connected to the line to provide good input power factor and generate a roughly regulated dc voltage. Usually this voltage cannot directly supply the load since it contains intolerable second harmonic content. Therefore, followed by the AC/DC converter, a DC/DC converter is cascaded to tightly regulate the output voltage. These two power stages are controlled separately, and thus it makes optimization of both converters possible. Another advantage of two-stage configuration is that it is easy to expand the system for multi-output. The main drawbacks of this scheme are its higher cost and larger size resulting from its increased component number and complicated control circuits.



(a) (b)

Figure 2-6 System configurations of PFC power supply: (a) Two-stage scheme; (b) One-stage scheme

Although the two-stage scheme approach is commonly adopted in industry, it received limited attention by the academic research community, where emphasis has been made in minimizing efficiency loss and achieving fast regulation [72-74]. The one-stage PFC scheme combines the power factor correction circuit and the voltage regulation circuit in one stage. Due to the simplified power stage and control circuit of the single-stage scheme, it is attracted to many applications with cost and size restriction [46-71]. The one-stage scheme, therefore becomes the main stream of contemporary research due to the ever-increasing demands for inexpensive power supply in residential and office appliances.

The underlying strategy of this scheme is to design the circuit in such a way that it allows its PFC circuit and voltage regulation circuit to share the same control circuit. Typically, the input circuit in one-stage PFC power supplies is an AC/DC converter operating in discontinuous conduction mode (DCM). The peak of the inductor current is proportional to the instantaneous line voltage automatically. The average inductor current per switching cycle (i.e. line current) is therefore tracing the line voltage in shape and phase. As a result, no control loop is required at the input side. This is the main advantage over a continuous conduction mode (CCM) power factor correction circuit in which multi-loop control strategy is necessary. However, the peak input current of DCM converter is at least twice as high as its corresponding average input current [24], which causes high current stresses on switches, resulting in intolerable conduction losses, switching losses and copper losses in high power applications. In practice, DCM

technique is only suitable for low to medium level power processes. When high power process is needed, the core converter operating in CCM is preferred.

2.4 POWER FACTOR CORRECTION CAPABILITIES OF THE BASIC CONVERTER TOPOLOGIES

The core of a high-frequency power factor corrector is its DC/DC counterpart. This converter can employ one of the basic DC/DC converter topologies or their variation versions. However, when they are applied to the rectified line voltage, they may behave differently. A converter operating in CCM will not draw a sinusoidal current from the line unless certain control circuit regulates its input current. CCM PWM switch model [90] can be easily applied to these converters to obtain their large signal equivalent circuits. Generally, a converter operating in CCM can be modeled by a low-pass filter with controlled parameters; A converter operating in DCM will draw a current with its peak automatically follow the line voltage, resulting in a sinusoidal-like average line current. However, different type of converter draws different shape of average line current. In order to examine the PFC properties of the basic converters, we will investigate their input characteristics. Because the input currents of these converters are discrete when operating in DCM, only averaged input currents are considered. Since switching frequency is much higher than the line frequency, we will assume that the line voltage is constant in a switching cycle. In steady-state operation, the output voltage is nearly constant and the variation in duty ratio is slight. Therefore, constant duty ratio is considered in deriving the input characteristics.

Next, we will briefly present the basic PWM converters when used as PFC circuits.

A. The buck converter

Figure 2-7 shows the buck PF corrector. When the buck converter operates in CCM, by using PWM switch modeling technique [90], the circuit topology can be modeled by the equivalent circuit shown in Fig. 2-8. Since the circuit model is a large signal model, analysis of power factor performance based on this model is valid. It can be shown that the transfer function and input impedance are given by

$$H(s)=\frac{V_o(s)}{V_{in}(s)}=\frac{d}{s^2LC+sL/R+1} \tag{2.8a}$$

$$Z_{in}(s)=\frac{V_{in}(s)}{I_{in}(s)}=\frac{R}{d^2}\frac{s^2LC+sL/R+1}{sRC+1} \tag{2.8b}$$

where d is the duty ratio of the switching signal applied to the switch S.

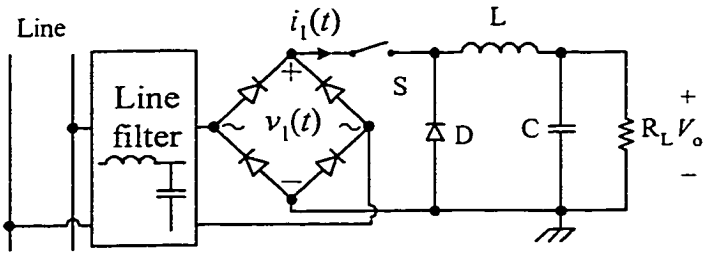


Figure 2-7 The buck converter

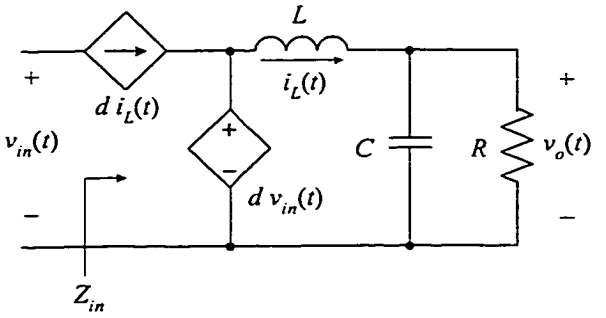


Figure 2-8 PWM switch model of the buck converter

Notice that Eqs. (2.8a) and (2.8b) are different from Eq. (2.7a) and (2.7b) in that they have introduced the control variable *d*. By properly controlling the switching duty ratio to modulate the input impedance and the transfer function, a pure resistive input impedance and constant output voltage can be obtained. Thereby, power factor correction and output regulation can both be achieved. However, despite that the buck converter operates in CCM, it draws discontinuous current, which has a peak value significantly higher than its average current, resulting in lower efficiency (higher switch conduction loss) and higher differential-mode EMI. An effective line filter must be designed to reduce the THD of the input current.

For the buck converter operating in DCM, its input current waveform is shown in Fig. 2-9(a). Assuming the line voltage remains constant within a switching cycle, hence the average input current in this switching cycle, when the line voltage is higher than the output voltage, is calculated by

$$i_{1,avg}(t)=\frac{1}{T_s}\left[\frac{1}{2}\cdot DT_s\cdot\frac{v_1(t)-V_o}{L}DT_s\right]$$

where T_s is the switching period.

Therefore, the average input current over half line cycle can be expressed as,

$$i_{1,avg}(t)=\begin{cases}\dfrac{D^2T_s}{2L}v_1(t)-\dfrac{D^2T_s}{2L}V_o & (v_1(t)>V_o)\\ 0 & (v_1(t)\le V_o)\end{cases} \qquad (2.9)$$

Figure 2-9(b) shows that the input voltage-input current I-V characteristic consists of two straight lines in quadrants I and III. It should be noted that these straight lines do

not go through the origin. When the rectified line voltage $v_1(t)$ is less than the output voltage V_o, negative input current would occur. This is not allowed because the bridge rectifier will block the negative current. As a result, the input current is zero near the zero cross point of the line voltage, as shown in Fig. 2-9(b). Actually, the input current is distorted simply because the buck converter can work only under the condition that the input voltage is larger than the output voltage. Therefore the basic buck converter is not a good candidate for DCM input power factor correction.

Comparing with the other type of high-frequency PFC circuits, the buck corrector offers inrush-current limiting, overload or short-circuit protection and over-voltage protection for the converter due to the existence of the power switch in front of the line. Another advantage is that the output voltage is lower than the peak of the line voltage, which is usually the case normally desired. The drawbacks of using buck corrector may be summarized as follows:

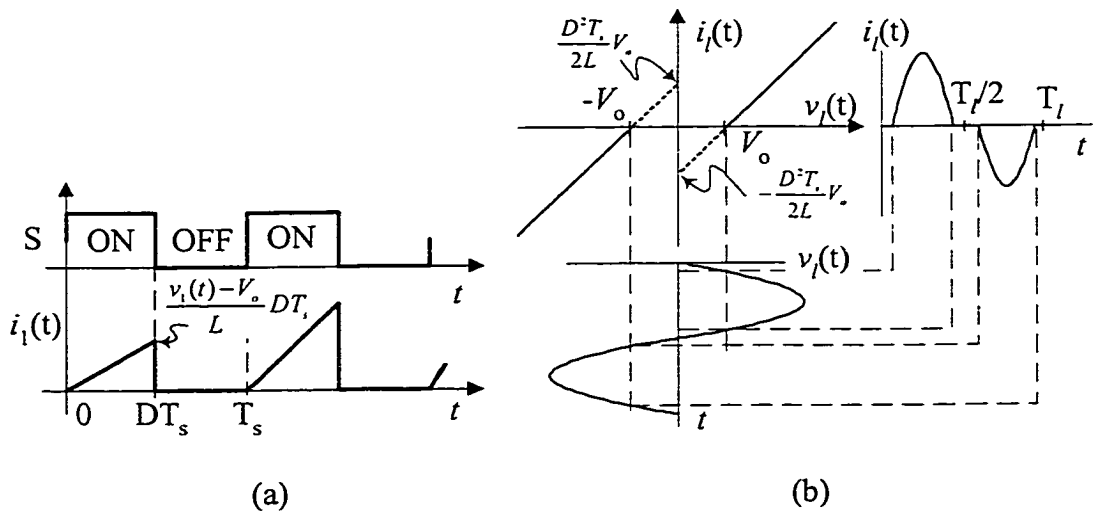


Figure 2-9 The buck converter operating in DCM: (a) input current waveform; (b) input V-I characteristic

- When the output voltage is higher than the line voltage, the converter draws no current from the line, resulting in significant line current distortion near the zero-across of the line voltage;
- The input current is discontinuous, leading to high differential-mode EMI;
- The current stress on the power switch is high;
- The power switch needs a floating drive.

B. The boost converter

The boost corrector and its equivalent PWM switch modeling circuit for CCM operation are shown in Figs. 2-10 and 2-11, respectively. Its transfer function and input impedance are given by,

$$H(s)=\frac{V_o(s)}{V_{in}(s)}=\frac{1/d'}{s^2\left(L/d'^2\right)C+s\left(L/d'^2\right)/R+1}; \tag{2.10a}$$

$$Z_{in}(s)=\frac{V_{in}(s)}{I_{in}(s)}=d'^2R\frac{s^2\left(L/d'^2\right)C+s\left(L/d'^2\right)/R+1}{sRC+1}, \tag{2.10b}$$

where $d'=1-d$.

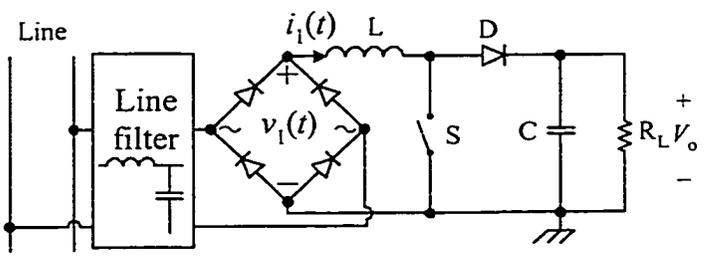


Figure 2-10 The boost converter

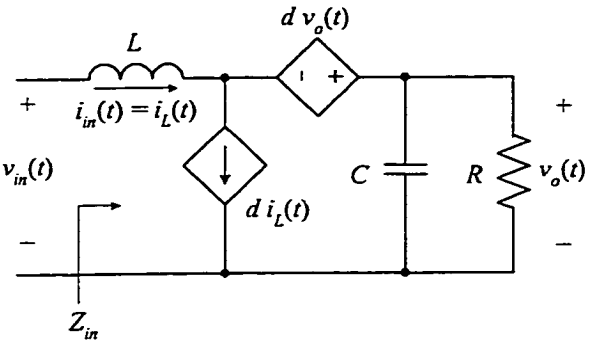


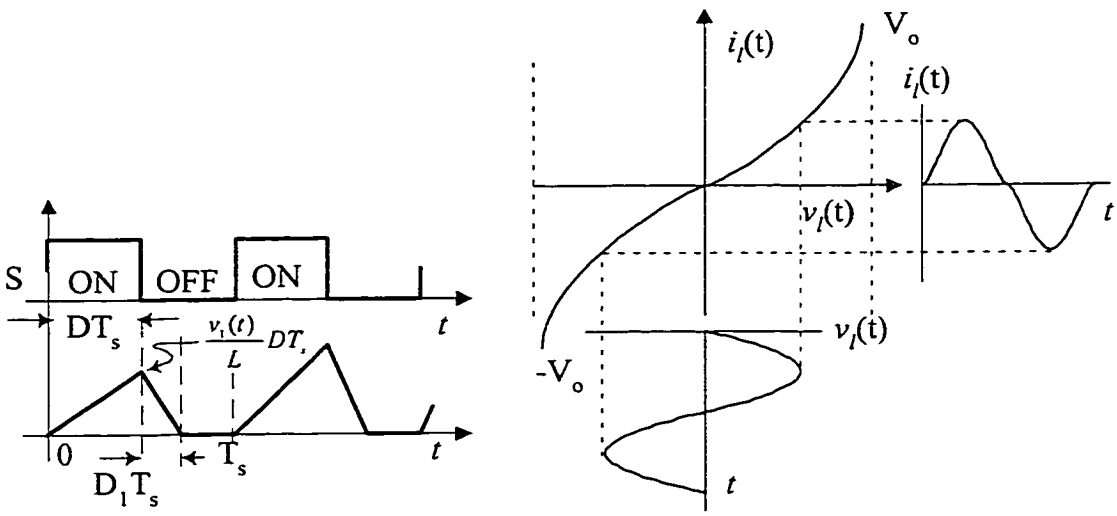
Figure 2-11 PWM switch model of the boost corrector

Unlike in the buck case, it is interesting to note that in the boost case, the equivalent inductance is controlled by the switching duty ratio. Consequently, both the magnitude and the phase of the impedance, and both the dc gain and the poles of the transfer function are modulated by the duty ratio, which implies a tight control of the input current and the output voltage. The boost converter operating in CCM has a continuous input current. The current stress on the switch is much less than that of the buck converter. So, the boost converter has less difficulty in dealing with EMI and efficiency loss than the buck converter has.

The input current waveform for the boost converter operating in DCM is shown in Figs. 2-12(a). The input I-V characteristic can be found as follows:

$$i_{1,avg}(t) = \frac{1}{T_s}\left[\frac{1}{2}\cdot(D+D_1)T_s\,\frac{v_1(t)}{L}DT_s\right] \tag{2.11}$$

$$= \frac{D^2 T_s}{2L}\,\frac{v_1(t)V_o}{V_o - v_1(t)}$$



(a) (b)

Figure 2-12 The boost converter operating in DCM: (a) input current waveform; (b) input V-I Characteristic

By plotting Eq. (2-11), we obtain the input I-V characteristic curve as given in Fig. 2-12(b). As we can see that as long as the output voltage is larger than the peak value of the line voltage in certain range, the relationship between $v_1(t)$ and $i_{1,avg}(t)$ is nearly linear. When the boost converter connected to the line, it will draw almost sinusoidal average input current from the line.

As one might notice from Eq. (2.11) that the main reason for the non-linearity is the existence of D_1. Ideally, if $D_1 = 0$, the input I-V characteristic will be a linear one.

Because of the above reasons, boost converter is comparably superior to most of the other converters when applied to do PFC. However, it should be noted that boost converter can operate properly only when the output voltage is higher than its input

voltage. When low voltage output is needed, a step-down DC/DC converter must be cascaded. Other advantages of boost corrector include less EMI and lower switch current and grounded drive. The shortcomings with the boost corrector are summarized as:

- The output voltage must be higher than the peak of line voltage;
- Small line current distortion still exists;
- Inrush-current limiting, overload and over-voltage protections are not available.

C. The buck-boost converter

For the buck-boost converter of Fig. 2-13 operating in CCM, we have the PWM model shown in Figs. 2-14. The expressions for transfer function and input impedance are,

$$H(s)=\frac{V_o(s)}{V_{in}(s)}=\frac{d/d'}{s^2\left(L/d'^2\right)C+s\left(L/d'^2\right)/R+1} \tag{2.12a}$$

$$Z_{in}(s)=\frac{V_{in}(s)}{I_{in}(s)}=\left(\frac{d'}{d}\right)^2 R\frac{s^2\left(L/d'^2\right)C+s\left(L/d'^2\right)/R+1}{sRC+1} \tag{2.12b}$$

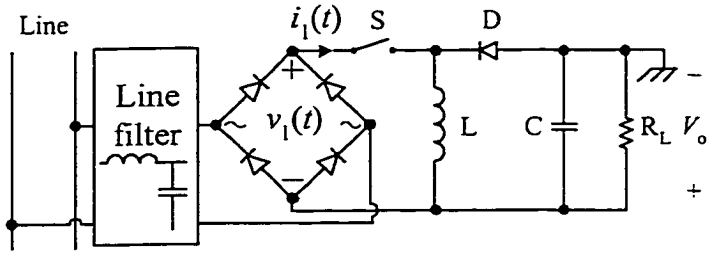


Figure 2-13 The buck-boost converter

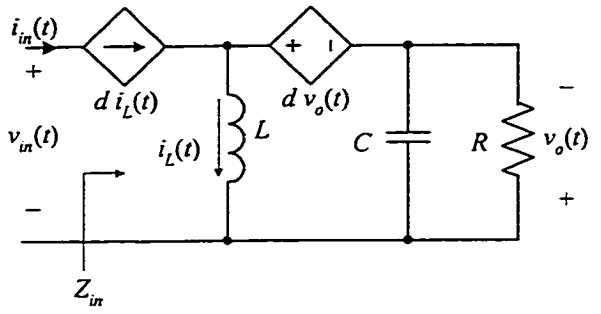


Figure 2-14 PWM switch model of the buck-boost converter

The buck-boost corrector combines some advantages of the buck corrector and the boost corrector. Like a buck corrector, it can provide circuit protection, and like a boost corrector its input current waveform and output voltage can be tightly controlled. Besides, the output voltage can be either higher or lower than the peak of the line voltage. However, the power switch locating at the input discontinues the input current, resulting in the same drawbacks as the buck converter suffers, i.e., high differential-mode EMI and high switch conduction loss.

For the buck-boost converter operating in DCM converter, the averaged input current of this converter can be found according to its input current waveform, depicted in Fig. 2-15(a).

$$i_{1,avg}(t)=\frac{D^2T_s}{2L}v_1(t) \tag{2.13}$$

Equation (2.13) gives a perfect linear relationship between $i_{1,avg}(t)$ and $v_1(t)$, which proves that a buck-boost has excellent automatic PFC property. This is because the input

current of buck-boost converter does not related to the discharging period D_1. Its input I-V characteristics and input voltage and current waveforms are shown in Fig. 2-15(b). Furthermore, because the output voltage of buck-boost converter can be either larger or smaller than the input voltage, it demonstrates strong availability for DCM input technique to achieve power factor correction. So, theoretically buck-boost converter is a perfect candidate. However, the buck-boost corrector has the following disadvantages:

- The input current is discontinued by the power switch, resulting in high differential-mode EMI;
- The current stress on the power switch is high;
- The power switch needs a floating drive;
- The polarity of output voltage is reversed.

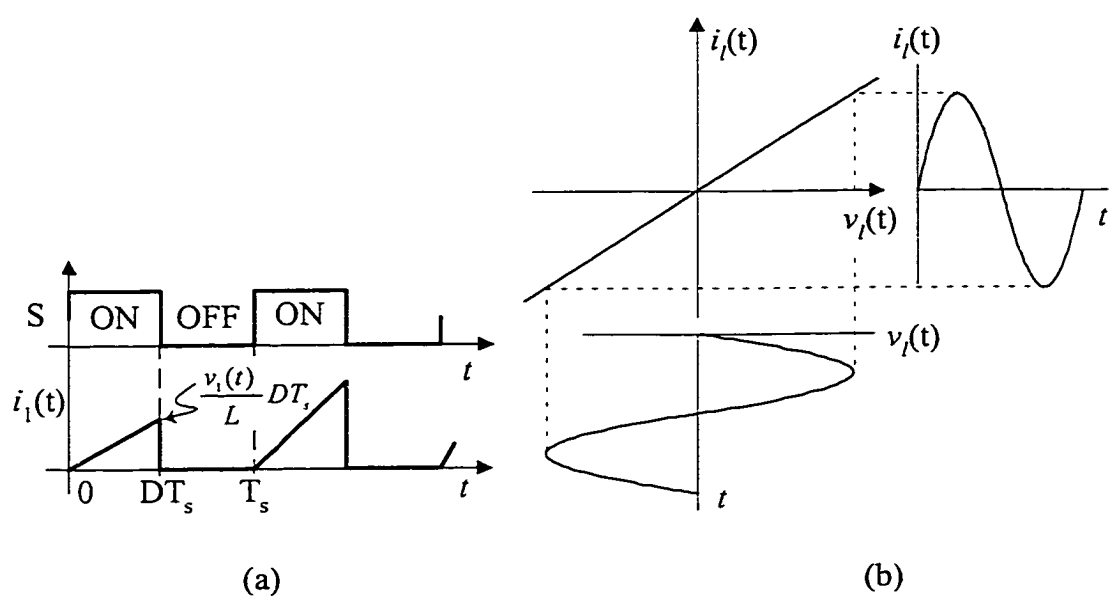


Figure 2-15 The buck-boost converter operating in DCM: (a) input current waveform; (b) input V-I Characteristic

D. The flyback converter

The flyback converter is an isolated converter whose topology is shown in Fig. 2-16. Primarily, this converter is derived from the buck-boost converter. However, the flyback converter is normally used in DCM (i.e., the magnetic is completely reset in each switching cycle) in order to make better use of the transformer core characteristics. Figure 2-17 shows its input current waveform. The input voltage-input current relationship is similar to that of the buck-boost converter:

$$i_{1.avg}(t)=\frac{D^2T_s}{2L_m}v_1(t)\,. \tag{2.14}$$

Where, L_m is the magnetizing inductance of the output transformer.

Therefore, it has the same input I-V characteristic, and hence the same input voltage and input current waveforms as those the buck-boost converter has, shown in Fig. 2-15(b).

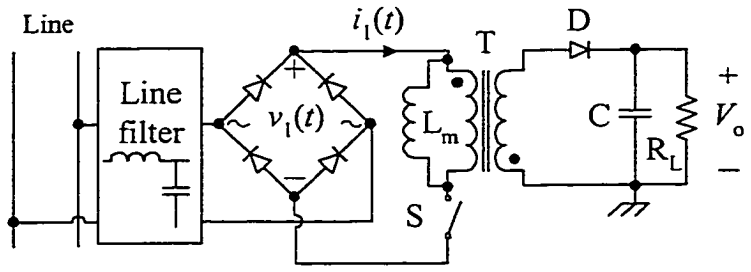


Figure 2-16 The flyback converter

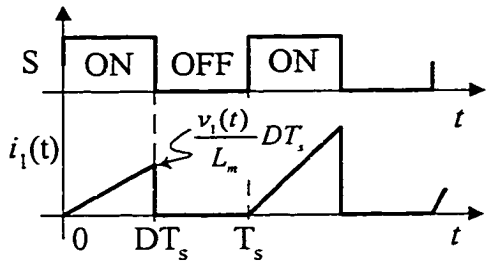


Figure 2-17 Input waveform of the flyback converter operating in DCM

Comparing with the buck-boost converter, the flyback converter has all the advantages of the buck-boost converter. What's more, input-output isolation can be provide by flyback converter. These advantages make flyback converter well suitable for power factor correction with DCM input technique. Comparing with boost converter, the flyback converter has better power factor correction and the output voltage can be either higher or lower than the input voltage. However, because of the use of power transformer, the flyback converter has high *di/dt* noise due to the existence of leakage inductance, lower efficiency and lower density (larger size and heavier weight). Also, in its principle of operation, the flyback converter needs to store the energy to be transferred to the output in the duty cycle interval. Limited by the saturation characteristic of the magnetic core, the flyback converter is only good for low to medium power level applications.

E. The forward converter

The circuit shown in Fig. 2-18 is a forward converter. The forward converter is a buck derived converter. In order to avoid transformer saturation, it is well known that the forward converter needs the 3rd winding to demagnetize (reset) the transformer.

Unfortunately, when the forward converter is connected to the rectified line voltage, the demagnetizing current through the 3rd winding will be blocked by the rectifier diodes. Therefore, normally the forward converter is not a choice for PFC purpose unless a certain circuit variation is made.

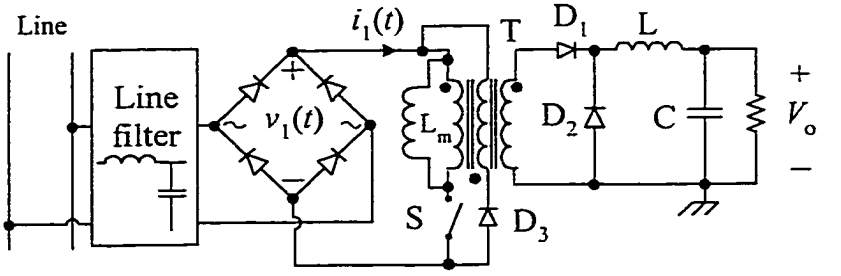


Figure 2-18 The forward converter

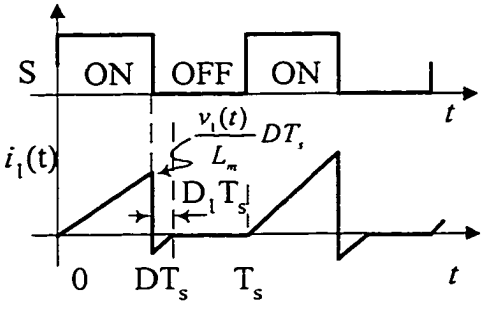


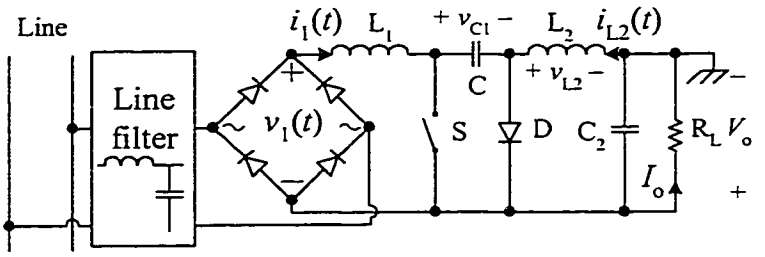
Figure 2-19 Input current waveform of the forward converter operating in DCM

F. The Cuk and the Sepic converters

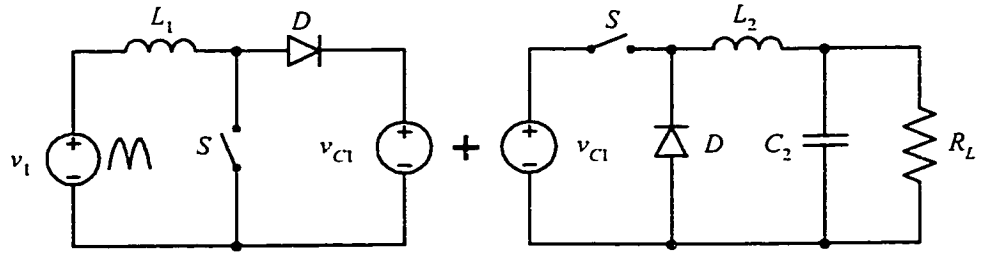
By combining a boost converter with a buck converter or a buck-boost converter, the Cuk converter or the Sepic converter is derived, shown in Figs. 2-20 and 2-21, respectively. Each of these converter topologies has two inductors, with one located at its input and the other at its output. Since the input power factor mainly comes from the

front-end stage, these converters behave similar to the boost converter at their input sides when they are employed as active power factor correctors. Like the boost converter, when the input inductor operates in CCM, the input current (= input inductor current) can be well controlled to follow the line voltage in shape and phase. The input inductor smoothes the input current, which brings us with relieved EMI problem and switch conduction loss.

It can be shown that Cuk converter and Sepic converter given in Figs. 2-20(a) and 2-21(a), respectively, have the same input I-V characteristic for DCM operation. Let's consider the case when the input inductor current operates in DCM while the output inductor operates in CCM. To investigate the input characteristic of these converters, let's take the Cuk converter as an example.



(a)



(b)

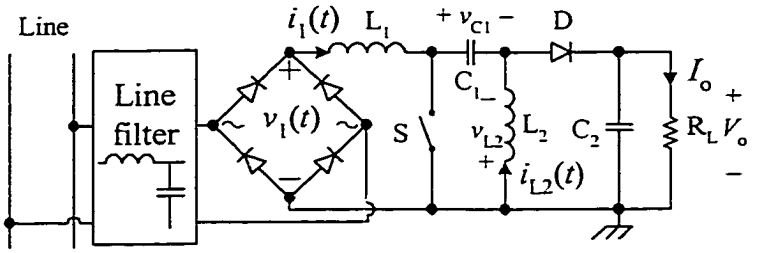
Figure 2-20 The Cuk converter (a) and its equivalent circuit (b)

For the Cuk converter shown in Fig. 2-20(a), the waveforms for input inductor current (=input current), output inductor current and the voltage across the output inductor are depicted in Fig. 2-22. Assume that the capacitor C_1 is large enough to be considered as a voltage source V_c, in steady-state, employing volt-second equilibrium principle on L_2, we obtain

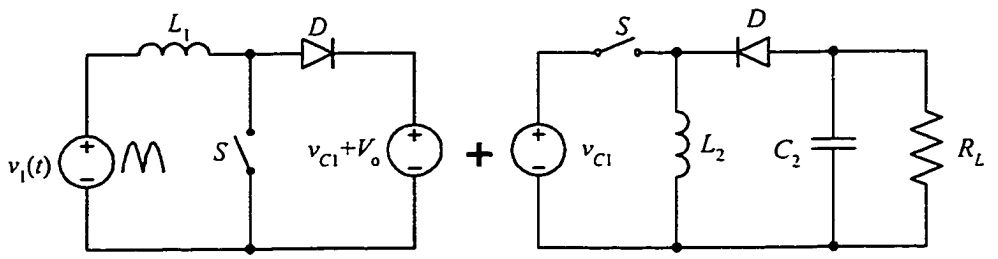
$$V_C = \frac{1}{D} V_o \tag{2.15}$$

The input inductor current reset time ratio D_1 is given by,

$$D_1 = \frac{D^2 v_1(t)}{V_o - D v_1(t)} \tag{2.16}$$



(a)



(b)

Figure 2-21 The Sepic converter (a) and its equivalent circuit (b)

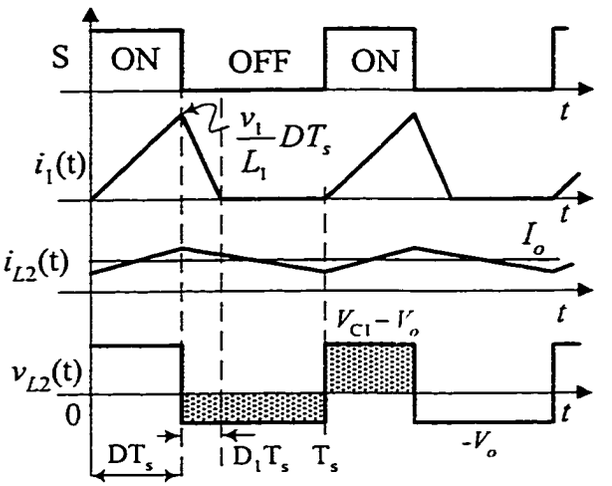


Figure 2-22 Typical waveforms of the Cuk converter with input inductor current operating in DCM

Therefore the averaged input current can be found as

$$i_{1,avg}(t)=\frac{1}{T_s}\left[\frac{1}{2}\cdot(D+D_1)T_s\frac{v_1(t)}{L}DT_s\right] \tag{2.17}$$

$$=\frac{D^2T_s}{2L}\frac{v_1(t)V_o}{V_o-Dv_1(t)}$$

It can be seen that Eq. (2.17) is very similar to Eq. (2.11) except that the denominator in the former equation is $V_o - Dv_1(t)$ instead of $V_o - v_1(t)$. This will lead to some improvement in that I-V characteristic in Cuk corrector. Referring to the I-V characteristic shown in Fig. 2-12(b), Cuk converter has a curve more close to a straight line. It can be shown that the same equation and I-V characteristic can be also obtained for the Sepic converter. Furthermore, both the Cuk and the Sepic converter have inherent inrush and overload protection abilities. Their output ripple is lower than the 2nd order

converters are. Such improvements, however, are achieved at the expense of using more circuit components. In fact, these converters can be recognized as the so-called single-stage single-switch PFC converters since each of them consists of two converters handling with only one switch. The Sepic converter has additional advantages over the Cuk converter since it automatically introduces a step-down function between the input and output circuits (or, the Sepic converter has lower capacitor voltage than the Cuk converter which makes it more cost-effective) and it has non-inverted output.

g) The Zeta converter

Figure 2-23(a) gives the Zeta converter connected to the line. This converter is a combination of a buck-boost converter and a buck converter. In DCM operation, the key

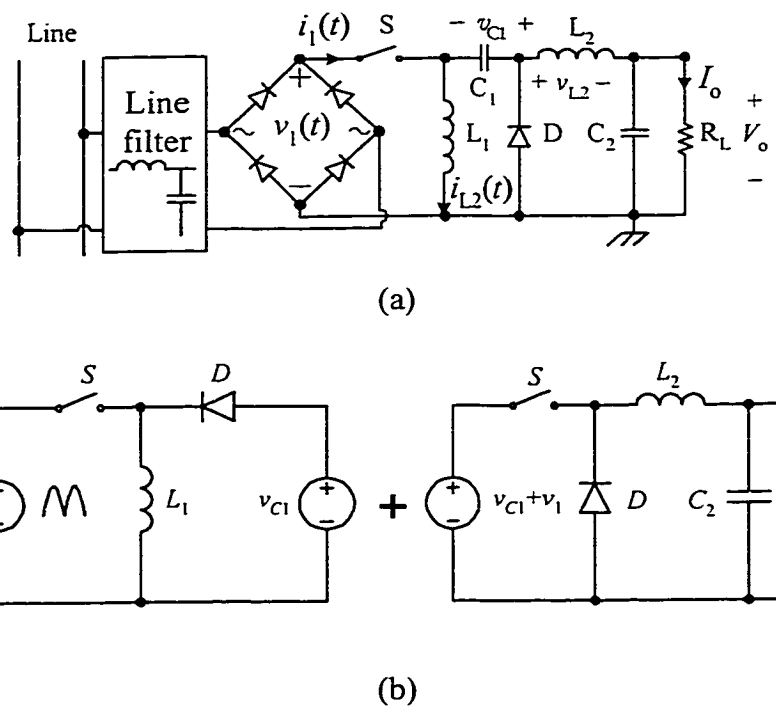


Figure 2-23 The Zeta converter (a) and its equivalent circuit (b)

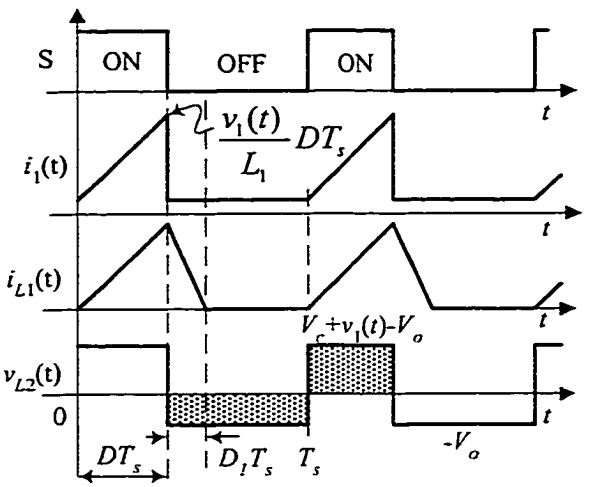


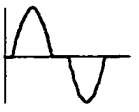
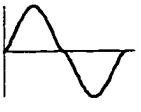
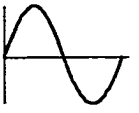
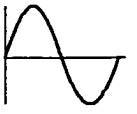
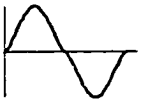
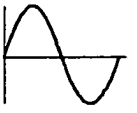
Figure 24 Typical waveforms of Zeta converter with input inductor operating in DCM

waveforms are illustrated in Fig. 2-24, where we presume the capacitor being equivalent to a voltage source V_c. As we can see that the converter input current waveform is exactly the same as that drawn by a buck-boost converter. Thus, the average input current for the Zeta converter is identical to that for the buck-boost, which is given by Eq. (2.12). As a result, the Zeta converter has good automatic PFC capability like the buck-boost converter. The improvement achieved here is that the output is non-inverted. However, floating drive required by the power switch still remains.

Based on the above discussion, we may conclude that all the non-isolated converters operating in CCM can be used to achieve power factor correction. The boost converter and the Sepic converter are superiors ones since they provide lower EMI and higher efficiency. All the eight basic converters except forward converter have good inherent PFC capability and are available for DCM PFC usage. Among them, boost converter and flyback converter are especially suitable for single-stage PFC scheme because they have minimum component count and grounded switch drive, and their

power switches are easy to be shared with the output DC/DC converter. The characteristics of the eight basic converter topologies are summarized as in Table 2-1.

Table 2-1 Comparison of basic converter topologies operating for PFC

	Buck	Boost	Buck-Boost	Flyback	Forward	Cuk and Sepic	Zeta
Line current waveform (DCM)					-		
Switch drive	Floating	Grounded	Floating	Grounded	Grounded	Grounded	Floating
Peak input current	High	Lower	High	High	-	Lower	High
Inrush and overload protection	✓	×	✓	✓	-	✓	✓
Components count in power stage	4	4	4	4	7	6	6
Output voltage	$V_o<V_{l.m}$	$V_o>V_{l.m}$	Inverted	$V_o<V_{l.m}$ or $V_o>V_{l.m}$	-	$V_o<V_{l.m}$ or $V_o>V_{l.m}$; Inverted for Cuk	$V_o<V_{l.m}$ or $V_o>V_{l.m}$

2.5 STEADY-STATE ANALYSIS OF DCM-S^4 PFC CONVERTER

The steady-state analysis of an AC/DC converter involves two operation frequencies, i.e. the line frequency, f_l, (50Hz or 60Hz) and high switching frequency, f_s (10's kHz). The input of the power stage is a rectified sinusoidal voltage, which implies that the conversion ratio M is varying periodically. However, such a time varying conversion ratio is neither convenient to used nor necessary since the line voltage is commonly given by its *rms* value. In DCM-S^4 converter scheme, only one feedback control loop is needed to regulate the energy from the storage capacitor to the output.

Because of the large value of the storage capacitor, its dc voltage remains almost constant over the entire line cycle. Therefore, the duty ratio is not sensitive to the change in instantaneous line voltage. However, the average duty ratio should maintain the input circuit feeding energy to the storage capacitor to keep the average input power equal to the output power.

2.5.1 Conversion Ratio

In order to describe the input/output characteristic, we define the AC/DC conversion ratio as the ratio of the average output voltage and the *rms* value of the input as given in Eq. (2.18).

$$M \triangleq \frac{V_o}{V_{l.rms}} \tag{2.18}$$

In common, to find the conversion ratio of a given AC/DC converter, we need to establish the input/output power conservation equation. The average output power can be always expressed as V_o^2/R_L but the input power is hardly described accurately since the line current is generally distorted from a sinusoidal waveform. Therefore, development of certain approximated methods to simplify the analysis will be helpful.

2.5.1.1 Simplified approaches to analyze AC/DC conversion ratio

Seen by the line voltage, the AC/DC converter can be emulated by a pure resistor when $v_l(t)$ and $i_l(t)$ are in phase (assuming PF = 1). Conceptually, the effective (i.e. *rms*) voltage or current can be understood as an equivalent dc voltage or current that provides the same average power as that of the voltage or current does when both of them are

applied to the same resistor. As a result, AC/DC steady-state analysis can be approximated by DC/DC steady-state analysis in which the ac input voltage is replaced by a DC input voltage equal to the *rms* value of the line voltage [16]. Let's call this analysis method "DC substitution method".

There is another alternative to determine the input power for a given front-end converter topology. Based on the average input current expressions given in Section 2.4, the peak values of the line currents can be found. Under the assumption of PF=1, the steady-state power conservation equation can be set as $V_{l,rms}\frac{I_{l,\max}}{\sqrt{2}}=\frac{V_o^2}{R_L}$. Thereby, the steady-state analysis can be performed. Let's call this method "approximate rms method".

In comparing the two methods, let us take the buck converter shown in Fig. 2-25 as an example. The expression, Eq. (2.9), of the average line current in half line cycle is rewritten as follows,

$$i_{l,avg}=\frac{D^2T_s}{2L}\left[v_1(t)-V_o\right] \qquad (\phi<\omega_l t<\pi-\phi) \qquad (2.19)$$

Where, ω_l is the line angular frequency, and

$$\phi=\sin^{-1}\left(\frac{V_o}{\sqrt{2}V_{l,rms}}\right)=\sin^{-1}\left(\frac{M}{\sqrt{2}}\right). \qquad (2.20)$$

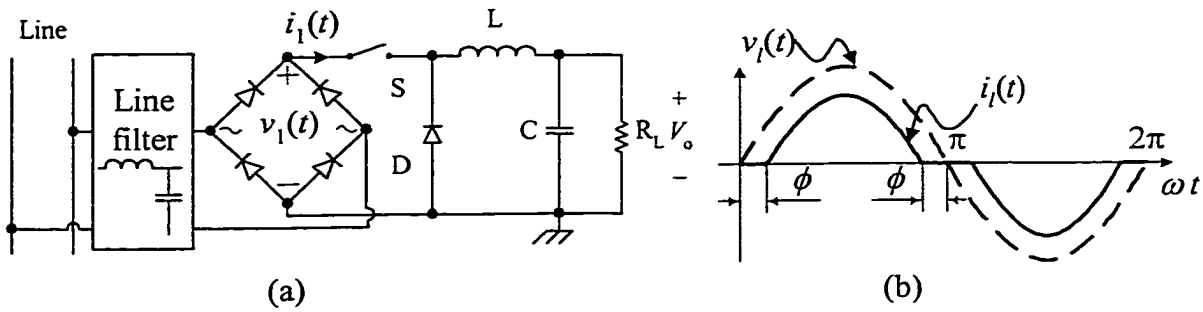


Figure 2-25 The buck converter operating in DCM for PFC: (a) the buck converter; (b) the current waveform draw from the line

First, let's use the definition of average power to calculate the average input power, i.e.,

$$P_{in} = \frac{1}{\pi}\int_{\phi}^{\pi-\phi} v_l(t)\cdot i_{l,avg}(t)\, d\omega_l t$$

$$= \frac{1}{\pi}\int_{\phi}^{\pi-\phi}\left[\sqrt{2}\,V_{l,rms}\sin\omega_l t\cdot\frac{D^2T_s}{2L}\left(\sqrt{2}\,V_{l,rms}\sin\omega_l t - V_o\right)\right] d\omega_l t$$

$$= \frac{D^2T_s}{2\,\pi L}\int_{\phi}^{\pi-\phi}\left[2V_{l,rms}^2\sin^2\omega_l t - \sqrt{2}\,V_{l,rms}V_o\sin\omega_l t\right] d\omega_l t$$

$$= \frac{D^2T_sV_{l,rms}^2}{2\,\pi L}\left(\pi - 2\phi + \sin 2\phi - 2\sqrt{2}\,M\cos\phi\right)$$

Setting $P_{in} = P_{out}$, we have,

$$\frac{D^2T_sV_{l,rms}^2}{2\,\pi L}\left(\pi - 2\phi + \sin 2\phi - 2\sqrt{2}\,M\cos\phi\right) = \frac{V_o^2}{R_L}$$

Solving the above equation for D, we obtain,

$$D=\sqrt{\frac{2\pi\tau_n}{\pi-2\phi+\sin 2\phi-2\sqrt{2}M\cos\phi}}\,M \tag{2.21}$$

Where, $\tau_n=\frac{\tau}{T_s}$ is normalized load time constant, and $\tau=\frac{L}{R_L}$ is load time constant. Both of them are proportional to the load current.

Equation (2.21) describes the accurate relationship between D and M since it is derived directly from the definition of average power. In the following, we will derive the same relationship by using the "DC substitution method" and the "approximate *rms* method". Comparison will be made among these methods to show their accuracy.

DC substitution method

Using a DC voltage source with value $V_{l,\text{rms}}$ to supply the buck converter, in DCM operation we have the average input current,

$$I_{in}=\frac{D^2T_s}{2L}\left(V_{l,rms}-V_o\right)$$

According to $V_{l,\text{rms}}\,I_{in}=V_o^2/R_L$, it yields,

$$\frac{D^2T_s}{2L}\left(V_{l,rms}-V_o\right)\cdot V_{l,rms}=\frac{V_o^2}{R_L}$$

Solving for D leads to,

$$D=\sqrt{\frac{2\tau_n}{1-M}}\,M \tag{2.22}$$

Approximate rms method

From Eq. (2.19), it is clear that the peak line current appears at $v_l = V_{l,max}$, that is,

$$I_{l,\max} = \frac{D^2 T_s}{2L}\left(V_{l,\max} - V_o\right)$$

Assuming PF = 1, then the rms value of the line current can be approximated by,

$$I_{l,rms} = \frac{I_{l,\max}}{\sqrt{2}} = \frac{D^2 T_s}{2L}\left(V_{l,rms} - \frac{V_o}{\sqrt{2}}\right)$$

Then, set $V_{l,rms}\, I_{l,rms} = V_o^2/R_L$, i.e.,

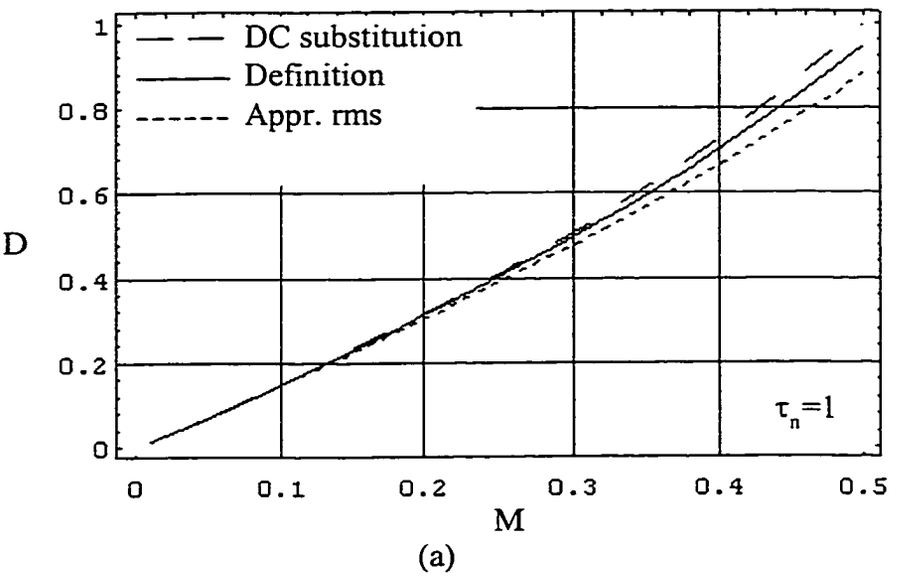
$$\frac{D^2 T_s}{2L}\left(V_{l,rms} - \frac{V_o}{\sqrt{2}}\right)\cdot V_{l,rms} = \frac{V_o^2}{R_L}$$

Therefore,

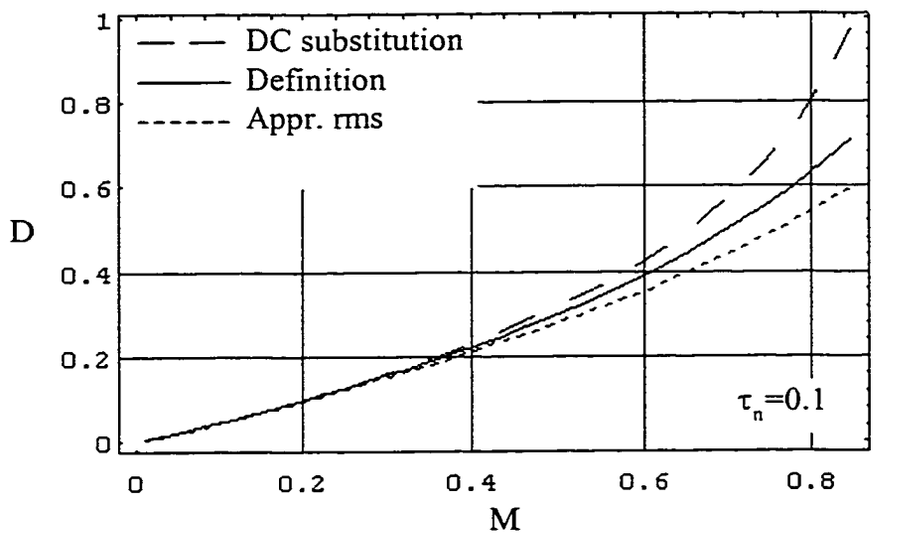
$$D = \sqrt{\frac{2\tau_n}{1-\left(M/\sqrt{2}\right)}}\, M \qquad (2.23)$$

Comparing Eq. (2.23) with Eq. (2.22), we notice that both the equations present the same type of function except a minor difference in their coefficients. The affect of such difference can be illustrated by plotting all the three expression in one graph shown in Fig. 2-26. At heavy load and smaller conversion ratio, the "DC substitution method" presents slightly higher accuracy than the "approximated rms method" does, shown in Fig. 2-26(a) ($\tau_n = 1$). However, at light load, with the conversion ratio going to high the curve given by "DC substitution method" exhibits strong tendency to deviate the curve

calculated from the average power definition method, shown in Fig. 2-26(b). In contrast, the "approximated rms method" gives more accurate result since both Eq. (2.21) and Eq. (2.23) show infinite duty ratio mathematically when M approaching $\sqrt{2}$, while Eq. (2.22)



(a)



(b)

Figure 2-26 Comparison of duty ratio versus conversion ratio curves obtained from three methods: (a) at $\tau_n = 1$; (b) at $\tau_n = 0.1$

trends to a infinite duty ratio at M =1. In the viewpoint of circuit operation, the "approximated rms method" sets forth an inequality $M < \sqrt{2}$, which can be explicitly deciphered as that the effective operation period for the buck converter is defined by $V_o < v_l(t) < V_{l,max}$, while the range has been incorrectly reflected by $V_o < v_l(t) < V_{l,rms}$ in the "DC substitution method". Based on the above comparison, we will use the "approximated rms method" to perform steady-state analysis in this dissertation.

2.5.1.2 AC/DC conversion ratio of S^4 converters

Figure 2-27 depicts a block diagram of a single-stage, single-switch AC/DC converter. Typically, the input circuit is one of those second order basic converter topologies with DCM operation. Commonly at least one bulk capacitor is needed between the input and the output circuit to balance the instantaneous power. Since the bulk capacitor voltage has important significance in the S^4 converter, let's define the following ratios:

$$M_0 \triangleq \frac{V_o}{V_{Cs}} \tag{2.24}$$

$$M_1 \triangleq \frac{V_1}{V_{l,rms}} \tag{2.25}$$

$$M_2 \triangleq \frac{V_{Cs}}{V_1} \tag{2.26}$$

Hence, the input/output conversion ratio $M = \frac{V_o}{V_{l,rms}}$ is given by,

$$M = M_0 M_1 M_2 \tag{2.27}$$

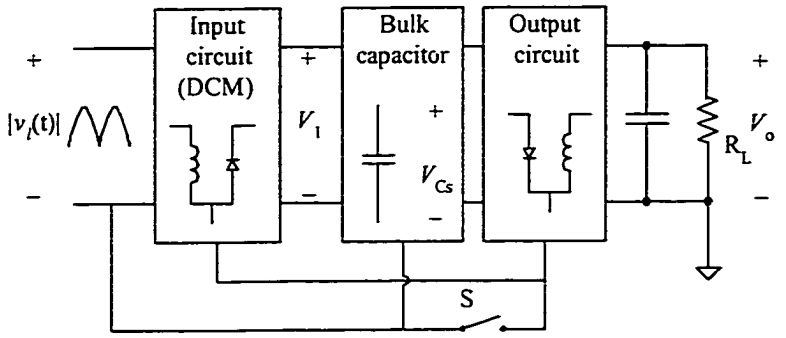


Figure 2-27 Block diagram of a single-stage single-switch AC/DC converter

Depending on the input circuit, the AC/DC conversion ratio can be determined as follows:

A. S^4 converter with buck type input circuit

Figure 2-28 shows the block diagram representation for an S^4 converter with a buck type input circuit. The line current in half line cycle is given by,

$$i_l(t)=\begin{cases}\dfrac{D^2T_s}{2L}v_l(t)-\dfrac{D^2T_s}{2L}V_1 & (v_1(t)>V_1)\\ 0 & (v_1(t)\le V_1)\end{cases} \tag{2.28}$$

The peak and *rms* line currents can be easily obtained from the above equation,

$$I_{l,\max}=\frac{D^2T_s}{2L}\left(V_{l,\max}-V_1\right)$$

$$I_{l,rms}=\frac{D^2T_s}{2L}\left(V_{l,rms}-\frac{V_1}{\sqrt{2}}\right) \tag{2.29}$$

Thus the steady-state power conservation is set by,

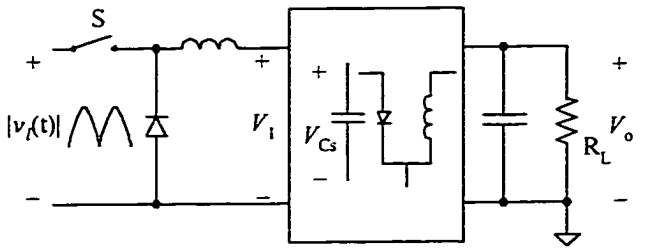


Figure 2-28 S^4 converter with buck type input circuit

$$\frac{D^2 T_s}{2L}\left(V_{l.rms} - \frac{V_1}{\sqrt{2}}\right)\cdot V_{l.rms} = \frac{V_o^2}{R_L}$$

Noticing the definitions of M and M_1, the duty ratio can be expressed as,

$$D = \sqrt{\frac{2\tau_n}{1-\left(M_1/\sqrt{2}\right)}}\,M \tag{2.30}$$

To express the ratio M_1 in Eq. (2.30) in terms of D and M, we need further information about the connection structure of the bulk capacitor(s) and the output circuit. Practically, for a given AC/DC converter, it is easier to find the ratios M_2 and M_0 in terms of D and M. According to Eq. (2.27), M_1 can be determined:

$$M_1 = \frac{M}{M_2(D,M)\cdot M_0(D,M)} \tag{2.31}$$

B. S^4 converter with boost type input circuit

Figure 2-29 shows the block diagram of S^4 converter with boost type input circuit. For this kind of converter, we have line current expression for the first half line cycle,

$$i_l(t) = \frac{D^2 T_s}{2L} \frac{v_l(t) V_1}{V_1 - v_l(t)} \qquad (v_l(t) > 0) \tag{2.32}$$

It can be seen that the line voltage and the line current reach their peak values at the same time. Using "approximated *rms* method" we have

$$I_{l.rms} = \frac{D^2 T_s}{2L} \frac{V_{l.rms} V_1}{V_1 - \sqrt{2} V_{l.rms}} \tag{2.33}$$

Considering $P_{in} = P_{out}$, we hold,

$$\frac{D^2 T_s}{2L} \frac{V_{l.rms}^2 V_1}{V_1 - \sqrt{2} V_{l.rms}} = \frac{V_o^2}{R_L}$$

Therefore,

$$D = \sqrt{2\tau_n \left[1 - \left(\sqrt{2}/M_1\right)\right]}\, M \tag{2.34}$$

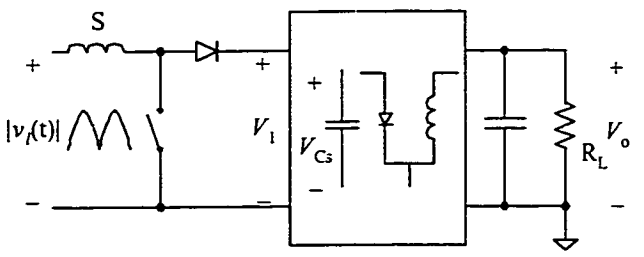


Figure 2-29 S^4 converter with boost type input circuit

C. S^4 converter with buck-boost or flyback type input circuit

The block diagram of S^4 converter with buck-boost type input circuit is illustrated in Fig. 2-30. It is shown in Section 2.4 that the buck-boost converter and the flyback converter have the same expression for the line current, that is,

$$i_l(t)=\frac{D^2T_s}{2L}v_l(t) \tag{2.35}$$

Obviously, we have,

Finally,

$$D=\sqrt{2\tau_n}\,M \tag{2.37}$$

$$I_{l,rms}=\frac{D^2T_s}{2L}V_{l,rms} \tag{2.36}$$

Hence,

$$\frac{D^2T_s}{2L}V_{l,rms}^2=\frac{V_o^2}{R_L}$$

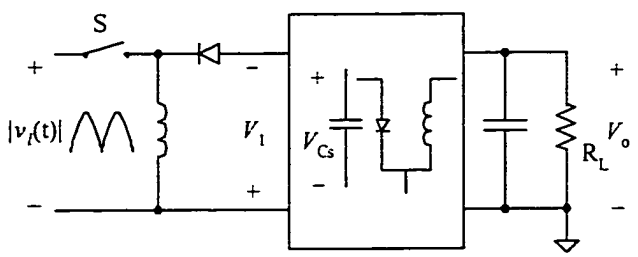


Figure 2-30 S^4 converter with buck-boost type input circuit

It is interesting to see that the duty ratio to conversion ratio relationships for the buck-boost and flyback type input AC/DC S^4 converter are linear and only dependent upon their input circuit. Whatever the output circuit is employed, it will never affect the power flow from the input to output.

Examples:

The Cuk, Sepic and Zata converter are most common fourth order converters. They can be also considered as single-stage single-switch converters when they are used for power factor correction. Let's take these three converters as examples to determine their AC/DC conversion ratio.

Example 1: The Cuk converter

Referring to Fig. 2-20, the Cuk converter can be decomposed into a boost converter cascaded with a buck converter. It is easy to find that,

$$M_2 = \frac{V_{Cs}}{V_1} = 1$$

and

$$M_0 = \frac{V_o}{V_{Cs}} = D$$

Therefore,

$$M_1 = \frac{M}{M_2(D,M) \cdot M_0(D,M)} = \frac{M}{D}$$

Applying the conversion ratio formula for the boost type input converter, we have,

$$D=\sqrt{2\tau_n\left[1-\left(\sqrt{2}/M_1\right)\right]}\ M$$

$$=\sqrt{2\tau_n\left[1-\left(\sqrt{2}\,D/M\right)\right]}\ M$$

Further solve the above equation for D, leading to,

$$D=\left(\sqrt{\tau_n^2+2\tau_n}-\tau_n\right)M \tag{2.38}$$

Example 2: The Sepic converter

The Sepic converter is a combination of boost converter and a buck-boost converter, shown in Fig. 2-21. It is found that,

$$M_0=\frac{D}{1-D}$$

$$M_2=1-D$$

So,

$$M_1=\frac{M}{M_2(D,M)\cdot M_0(D,M)}=\frac{M}{D}$$

As a result the same result as that for the Cuk converter can be obtained for the Sepic converter, i.e.,

$$D=\left(\sqrt{\tau_n^2+2\tau_n}-\tau_n\right)M \tag{2.39}$$

Example 3: The Zeta converter

Because the Zata converter is derived from the buck-boost converter cascaded with the buck converter, it is a buck-boost type input AC/DC converter. Therefore, the AC/DC conversion ratio can be directly written as,

$$D=\sqrt{2\tau_n}\,M \tag{2.40}$$

2.5.2 Regulation Capabilities

In Section 2.5.1, we discussed the relationships between duty ratio and AC/DC conversion ratio for the S^4 PFC converters. These relationships build up control curves for the control circuit to regulate the converter output. However, the duty ratio to conversion ratio relationship alone cannot completely describe the converter regulation characteristics. For example, mathematically the duty ratio represented in these equations can go to one, but practically the duty ratio has to be confined within certain value to ensure the input inductor operate in DCM. Therefore, certain constraints must be imposed onto these D-M relationships to truncate the control curves. As a result, the regulation capabilities are also limited by the constraints. In this section, we will discuss the duty ratio limit so that the line regulation capability and load regulation capability can be evaluated. The discussion is very useful for design optimization.

Apparently, if we confine the duty ratio within certain range so that even if the line voltage reaches its peak value the input inductor still operates in DCM, the DCM operation over the whole line cycle can be ensured. The upper limit for the duty ratio is in such that it makes the input inductor operate in critical conduction mode (CrCM) when

the line voltage peak appears. Let's name the converter operation mode a "peak critical mode (PCrM)" in which the input inductor operates in CrCM at the peak line voltage.

For an AC/DC converter operating in PCrM, the duty ratio is a function of conversion ratio M and normalized load time constant τ_n, denoted by,

$$D = f_{PCrM}(M, \tau_n) \tag{2.41}$$

For the same converter, when the input inductor operates in DCM, we represent the control function as,

$$D = f_{DCM}(M, \tau_n). \tag{2.42}$$

Essentially, if the converter operation satisfies both the above two equations, the limit duty ratio for DCM operation of the input inductor is reached. Therefore the maximum duty ratio can be determined by,

$$\begin{cases} D_{\max} = f_{PCrM}(M, \tau_n) \\ D_{\max} = f_{DCM}(M, \tau_n) \end{cases} \tag{2.43}$$

In constructing the above equations, Eq. (2.42) can be determined based on the method introduced in Section 2.5.1. As for Eq. (2.41), the following discussion will help illustrate the concept.

A. S^4 converter with buck type input circuit

For the buck type input circuit operating in PCrM, volt-second balance on the input inductor holds at peak line voltage. Referring to Fig. 2-28, we have,

$$(V_{l.\max} - V_1)D = V_1(1-D)$$

That is,

$$V_1 = D\,V_{l.\max} \tag{2.44}$$

Substituting V_1 in Eq. (2.29) for the above expression, it yields,

$$I_{l.rms} = \frac{D^2 T_s}{2L}(1-D)V_{l.rms} \tag{2.45}$$

Considering $P_{in} = P_{out}$, we get,

$$\frac{D^2 T_s}{2L}(1-D)V_{l.rms}^2 = \frac{V_o^2}{R_L}$$

Through properly arrangement, we obtain the following third order nonlinear equation:

$$D^3 - D^2 + 2\tau_n M^2 = 0$$

The real root of the above equation is,

$$D = \sqrt[3]{-\tau_n M^2 + \sqrt{\tau_n^2 M^4 - \frac{1}{27}}} + \sqrt[3]{-\tau_n M^2 - \sqrt{\tau_n^2 M^4 - \frac{1}{27}}} \tag{2.46}$$

$$= f_{PCrM}(M, \tau_n)$$

B. S^4 converter with boost type input circuit

Similarly, let's consider PCrM operation for the boost type input circuit. Referring Fig. 2-29, the volt-second balance equation at peak line voltage is written as,

$$D V_{l,\max} = (V_1 - V_{l,\max})(1-D)$$

Expressing V_1 in term of D, it gives,

$$V_1 = \frac{\sqrt{2} V_{l,rms}}{1-D}. \tag{2.47}$$

Introducing Eq. (2.47) into Eq. (2.33), through simplification we obtain,

$$I_{l,rms} = \frac{D T_s}{2L} V_{l,rms} \tag{2.48}$$

Applying the power conservation principle, to yield,

$$\frac{D T_s}{2L} V_{l,rms}^2 = \frac{V_o^2}{R_L}$$

Finally, the maximum duty ratio is found as,

$$D = 2\tau_n M^2 \tag{2.49}$$

$$= f_{PCrM}(M, \tau_n)$$

C. S^4 converter with buck-boost or flyback type input circuit

According to Fig. 2-30, for the buck-boost converter in PCrM operation, the volt-second balance equation at peak line voltage is,

$$D V_{l.\max} = (1-D) V_1 \tag{2.50}$$

Or,

$$V_1 = \frac{\sqrt{2}\, D}{(1-D)} V_{l.rms} \tag{2.51}$$

However, the input current *rms* given by Eq. (2.36) dose not relate to the demagnetizing voltage, V_1, of the input inductor. In another word, the PCrM operation relies on the connection of the bulk capacitor(s) and the output circuit of the AC/DC converter. Therefore, directly solving Eq. (2.51) and noticing $M_1 = V_1/V_{l.rms}$, we have,

$$\begin{aligned} D &= \frac{M_1}{\sqrt{2}+M_1} \\ &= f_{PCrM}(M, \tau_n) \end{aligned} \tag{2.52}$$

Where, M_1 can be determined by Eq. (2.31), i.e.,

$$M_1 = \frac{M}{M_2(D,M)\cdot M_0(D,M)}$$

For the flyback type input converter with transformer ratio n, the similar equation can be obtained except that all the M1 in Eq. (2.52) should be attached with ratio n, that is,

$$D = f_{PCrM}(M, \tau_n) = \frac{n M_1}{\sqrt{2} + n M_1} \tag{2.53}$$

Example:

Consider the Cuk converter, let's analyze its line regulation capability and load regulation capability.

The Cuk converter is a boost type input converter. Therefore,

$$D = f_{PCrM}(M, \tau_n) = 2\tau_n M^2 \tag{2.54}$$

In Section 2.5.1.2, we obtained,

$$D = f_{DCM}(M, \tau_n) = \left(\sqrt{\tau_n^2 + 2\tau_n} - \tau_n\right) M \tag{2.55}$$

Solving Eqs. (2.54) and (2.55), it yields,

$$D_{max} = \tau_n + 1 - \sqrt{\tau_n^2 + 2\tau_n} \tag{2.56}$$

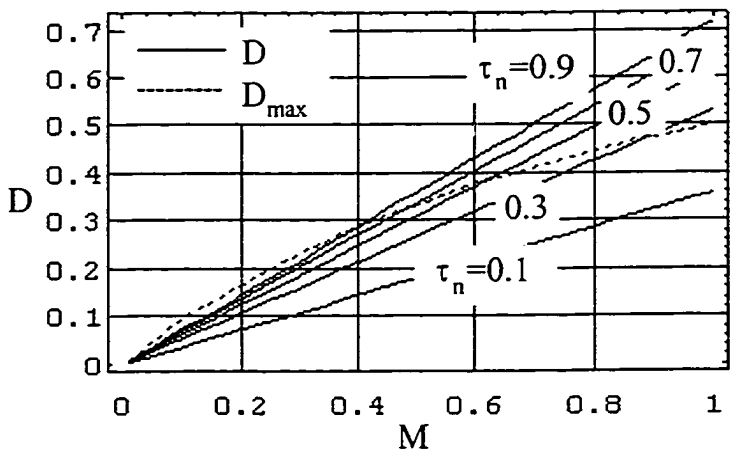
Or,

$$D_{max} = \frac{M}{M+1} \tag{2.57}$$

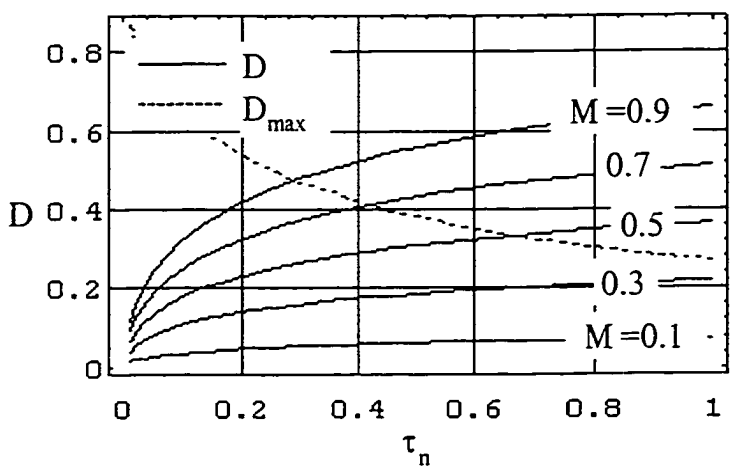
By plotting Eqs. (2.55) and (2.57) with different normalized load time constants, we get Fig. 2-31(a) to investigate the line regulation capability. For example, for load τ_n = 0.5, the AC/DC conversion ratio M cannot exceed 0.6, which implies that as long as the

input voltage rms value is higher than $V_o/0.6$, the Cuk converter can maintain the output voltage at V_o by adjusting the duty ratio, theoretically.

The load regulation capability can be examined referring to the plot created according to Eqs. (2.55) and (2.56) with different conversion ratios, shown in Fig. 2-31(b). For a fixed AC/DC conversion ratio, by controlling the duty ratio, the load can vary from open circuit to 0.63 with the output voltage keeping constant.



(a)



(b)

Figure 2-31 Regulation capabilities of the Cuk converter:
(a) line regulation capability; (b) load regulation capability

2.5.3 *Storage Capacitor Voltage*

The primary concern in S^4-AC/DC converter is its cost effectiveness. The cost of the bulk capacitor is heavily dependent on the capacitor voltage stress. Therefore, analysis of the bulk capacitor voltage behavior has very important practical meaning.

Commonly, the S^4 converter has an input inductor and an output inductor (or an equivalent inductor at the output). The operation modes (CCM or DCM) of these two inductors will strongly affect the behavior of the bulk capacitor voltage. Let's consider the block diagram shown in Fig. 2-32 in the following analysis.

Basically, there are four cases when different conduction modes of the input and output inductors are taken into consideration, i.e., CCM-CCM, CCM-DCM, DCM-CCM and DCM-DCM. In all the cases, the charge and discharge currents of the input and the output inductors are functions of voltages V_{in}, V_o, V_1 and V_2. In most S^4 converters, the voltages V_1 and V_2 are directly proportional to the bulk capacitor voltage V_{Cs}. Therefore, variations in V_1 and V_2 imply the change in V_{Cs}. Before we analyze each combination, let us clarify the following rules with regard to duty ratio and the voltages applied to an inductor under different conduction modes:

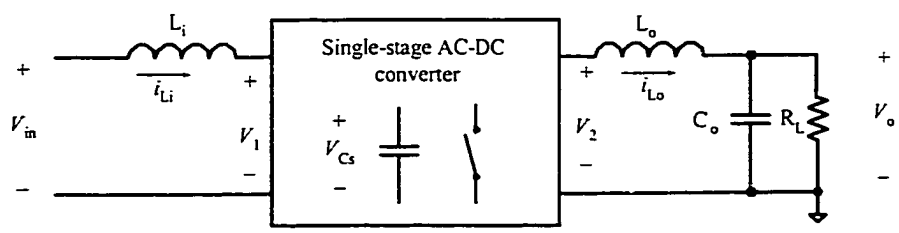


Figure 2-32 A block diagram of S^4 converter for bulk capacitor voltage analysis

Rule 1: In steady-state, for an inductor operating in CCM, the volt-second balance should be kept in the whole switching cycle, i.e.,

$$V_{ON}\, D = V_{OFF}\,(1-D) \tag{2.58}$$

If one of the voltages, V_{ON} or V_{OFF}, is fixed, changing in the other voltage must accompany with variation in the duty ratio, or vice versa.

Rule 2: In steady-state, for an inductor operating in DCM, the volt-second balance is kept only in part of the whole switching cycle. Hence the inductor voltage and the duty ratio have more freedom to change.

Next we will discuss the four possible combinations of CCM and DCM operations.

A. CCM-CCM type S^4 converter:

In this case, both the input and the output inductor operations are governed by rule 1. Generally, when the switch is off, the fixed output voltage will apply to

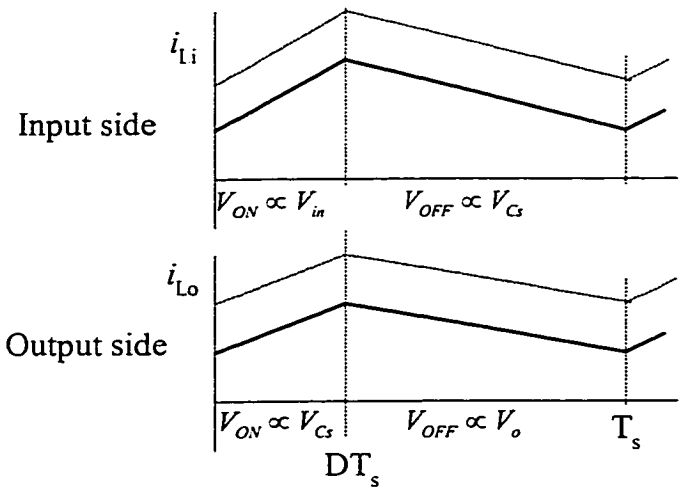


Figure 2-33 Input and output inductor waveforms of CCM-CCM type S^4 converter

demagnetize the output inductor. Adjusting duty ratio to regulate the load current implies changing V_1 (also the bulk capacitor voltage V_{Cs}). Since the capacitor voltage apply to the input inductor in OFF time, while to the output inductor in ON time, volt-second balance for both sides could not hold at the same time. As a result, remaining duty ratio and bulk capacitor voltage unchanged becomes the only solution under load variation.

B. CCM-DCM type S^4 converter:

Since the output side is in DCM, with the load current changing, the duty ratio must be adjusted in order to keep the average inductor current equal to the load current. To maintain volt-second balance at the input inductor, the bulk capacitor voltage has to follow the duty ratio's change. Therefore in CCM-DCM combination S^4 converter, both the duty ratio and the bulk capacitor voltage are functions of the load. It also can be seen form Fig. 2-34 that the capacitor voltage increases at heavy loads.

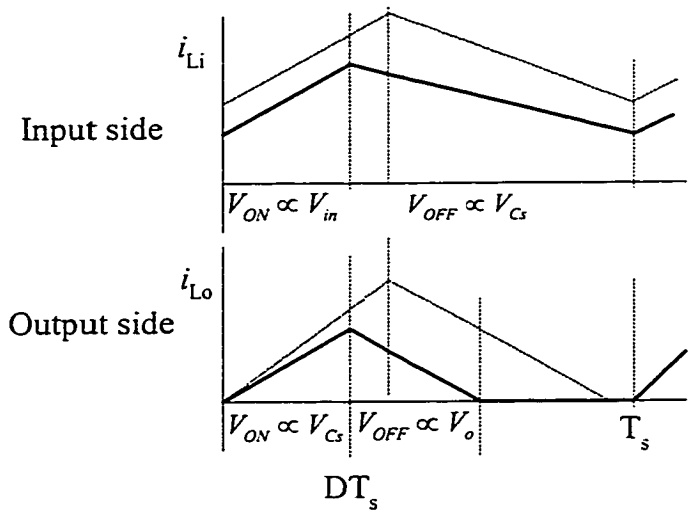


Figure 2-34 Input and output inductor waveforms of CCM-DCM type S^4 converter

C. DCM-CCM type S^4 converter:

Referring to Fig. 2-35, the DCM-CCM case is similar to the CCM-DCM combination. For the same reason, both the duty ratio and the bulk capacitor voltage are load dependent. However, the capacitor voltage decreases with the load becoming heavy.

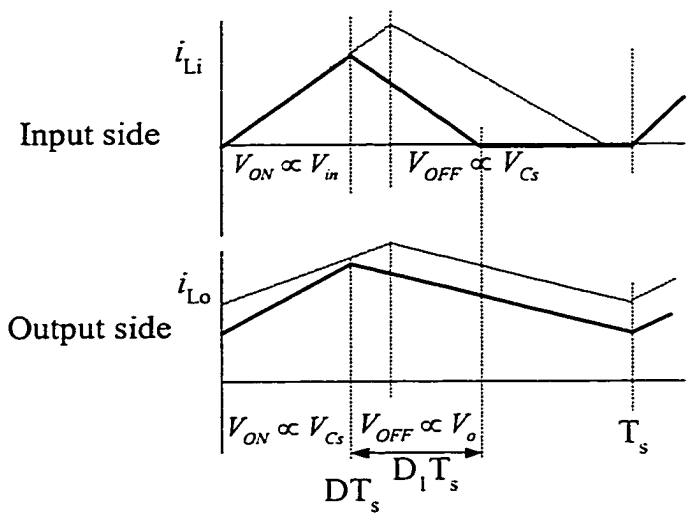


Figure 2-35 Input and output inductor waveforms of DCM-CCM type S^4 converter

D. DCM-DCM type S^4 converter:

For an S^4 converter with both sides operating in DCM, duty ratio must be adjusted with the load change in order to maintain the output voltage constant. It seems that the bulk capacitor voltage is also possible to change with the load. However, it can be shown that with a constant capacitor voltage, through geometry calculation on Fig. 2-36, we have the following area ratio equation:

$$\frac{S_{\Delta A_o B_o O_o}}{S_{\Delta A_i B_i O_i}} = \frac{S_{\Delta A_o' B_o' O_o}}{S_{\Delta A_i' B_i' O_i}} = \frac{1}{M} \tag{2.59}$$

Because the average areas of triangles $\Delta A_iB_iO_i$ and $\Delta A_i'B_i'O_i$ represent the input currents before and after load change, and the average areas of triangles $\Delta A_oB_oO_o$ and $\Delta A_o'B_o'O_o$ represent the output currents before and after load change, Eq. (2.59) implies constant conversion ratio has been already achieved. Therefore, in DCM-DCM type S^4 converter, bulk capacitor voltage is independent of load change.

Commonly, when both input and output sides operate in the same conduction mode, the capacitor voltage is independent from the load. Figure 2-37 summarizes the above discussion for the four types of combinations.

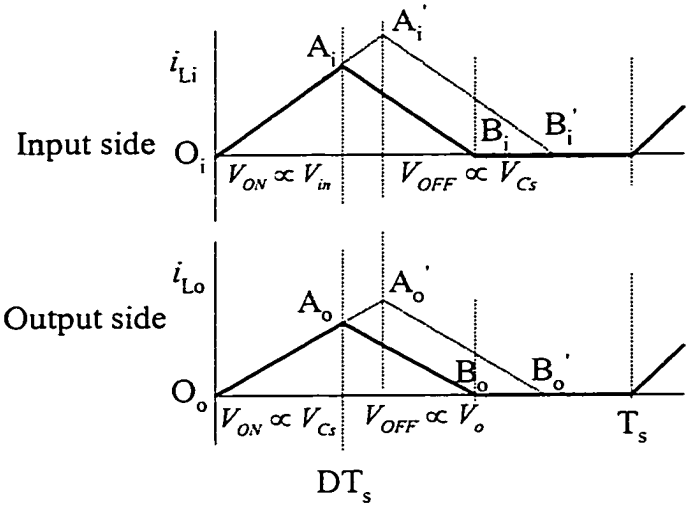


Figure 2-36 Input and output inductor waveforms of DCM-DCM type S^4 converter

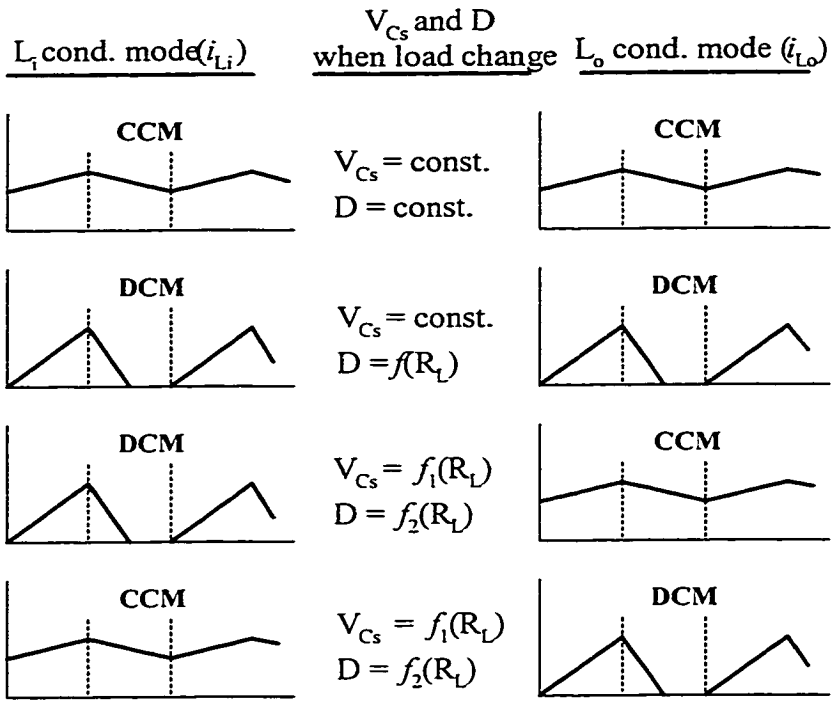


Figure 2-37 Duty ratio and bulk capacitor voltage behavior of four types of S^4 converters

2.5.4 Important Issues in S^4 PFC Converter

The difficulties in constructing an effective S^4 AC/DC converter topology are:

a) The unavoidable leakage inductance of the power transformer produces high voltage spike at switching instances, resulting in decreased efficiency.

b) Because the power switch performs both PFC and load and line regulations, the converter regulation capabilities are limited, resulting in difficulty in using them in universal input application.

c) Under high current and low duty ratio conditions, the bulk capacitor voltage is high, as a result, high rating capacitor and switching devices must be used which in turn results in increased cost.

d) The input stage still draws considerably distorted line current.

2.6 SUMMARY

In this chapter, we discussed the instantaneous power balance in PFC circuits. The passive corrector cannot do this job in high power factor way since the storage elements are not be able to compensate the energy difference between the input and the output in a desired manner. The PFC properties of high-frequency correctors in DCM depends on the converter topologies, while in CCM they are dominated by control circuit. For DCM-S^4 AC/DC converters, generalized analysis and design methods are given in this chapter. They provide designers and researchers with strong tools to optimize power supply and develop new topologies.

CHAPTER 3

OVERVIEW OF SINGLE-PHASE HIGH-FREQUENCY PFC TECHNIQUES

3.1 INTRODUCTION

This chapter presents an overview of various active harmonic reduction and power factor correction techniques in the open literature. The primary objective of this work is to give a brief introduction of these techniques and provide references for future researchers in this area. The discussion in this chapter includes commonly used control strategies and various types of converter topologies. Some comparison among these control strategies and converter topologies will be given.

3.2 CLASSIFICATION OF HIGH-FREQUNCY POWER FACTOR CORRECTORS

The continuous research in improving system power factor has resulted in countless circuit topologies and control strategies. Classified by their principles of operations to realize PFC, they can be mainly categorized into discontinuous conduction mode (DCM) input technique and continuous conduction mode (CCM) shaping technique. The recent research interest in DCM input technique is focused on developing PFC circuit topologies with a single power switch, result in single-stage single-switch converter (so-called S^4-converter). The CCM shaping technique emphasizes on the control strategy to achieve unity input power factor. The important topics in this line of

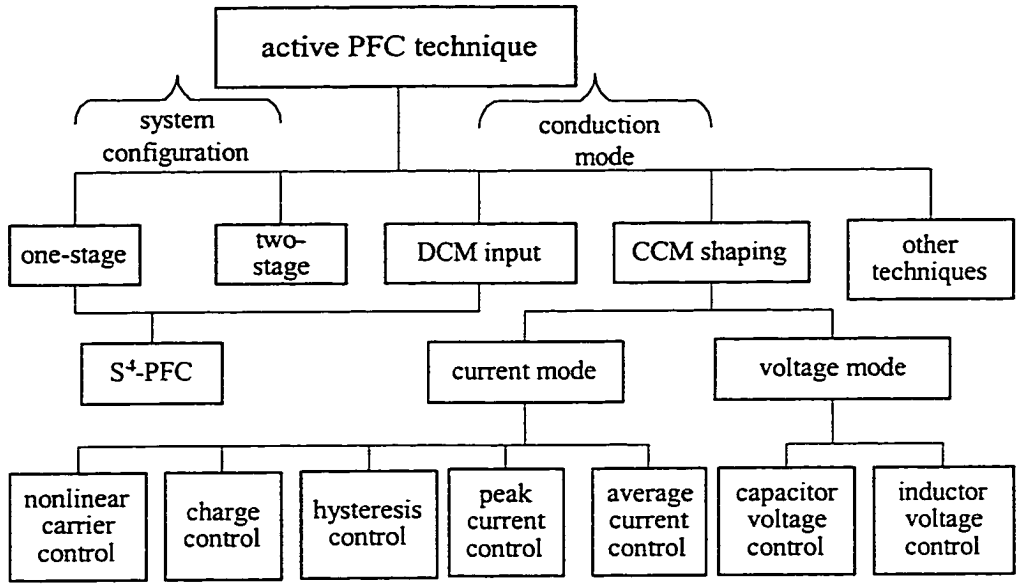


Figure 3-1 Overview of power factor correction techniques

research are concentrated on degrading complexity of the control circuit and enhancing dynamic response of the system, resulting in some new control methods. Figure 3-1 shows an overview of these techniques based on conduction-mode and system configuration types.

3.3 CCM SHAPING TECHNIQUE

Like other power electronic apparatus, the core of a PFC unit is its converter, which can operate either in DCM or in CCM. The benefit from DCM technique is that low cost power supply can be achieved because of its simplified control circuit. However, in higher power applications the high peak input current of DCM converter causes intolerable losses as well as severe EMI problem. In practice, DCM technique is only

suitable for low to medium level power application, whereas, CCM is used in high power cases. However, a converter operating in CCM does not have PFC ability inherently, i.e., unless a certain control strategy is applied, the input current will not follow the waveform of line voltage. This is why most of the research activities in improving power factor under CCM condition have been focused on developing new current shaping control strategies. Depending on the system variable being controlled (either current or voltage), PFC control techniques may be classified as current control or voltage control. Current control is the most common control strategy since the primary objective of PFC is to force the input current to trace the shape of line voltage.

To achieve both PFC and output voltage regulation by using a converter operating in CCM, multi-loop controls are generally used. Figure 3-2 shows the block diagram of AC/DC PFC converter with CCM shaping technique. Where, H_l is a line voltage compensator, H_x is a controlled variable compensator, and $x(t)$ is the control variable that can be either current or voltage.

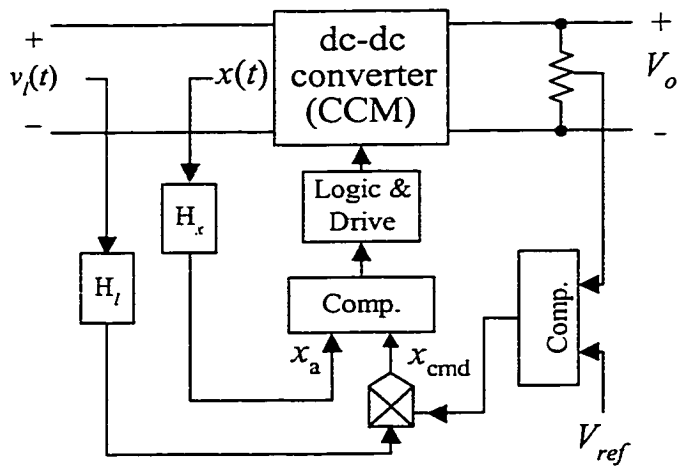


Figure 3-2 Block diagram of PFC converter with CCM shaping technique

Normally, in order to obtain a sinusoidal line current and a constant dc output voltage, line voltage $v_l(t)$, output voltage V_o and a controlled variable $x(t)$ need to be sensed. Depending on whether the controlled variable $x(t)$ is a current (usually the line current or the switch current) or a voltage (related to the line current), the control technique is called "current mode control" or voltage mode control," respectively. In Fig. 3-2, two control loops have been applied: the feedforward loop and the feedback loop. The feedforward loop is also called "inner loop" which keeps the line current to follow the line voltage in shape and phase, while the feedback loop (also called "outer loop") keeps the output voltage to be tightly controlled. These two loops share the same control command generated by the product of output voltage error signal and the line voltage (or rectified line voltage) signal.

3.3.1 Current Mode Control

Over many years, different current mode control techniques were developed. In this section, we will review several known methods.

A. Average current control

In average current control strategy, the average line current of the converter is controlled. It is more desired than the other control strategies because the line current in a switch-mode power supply can be approximated by the average current (per switching cycle) through an input EMI filter. The average current control is widely used in industries since it offers improved noise immunity, lower input ripple and stable operation [19-23].

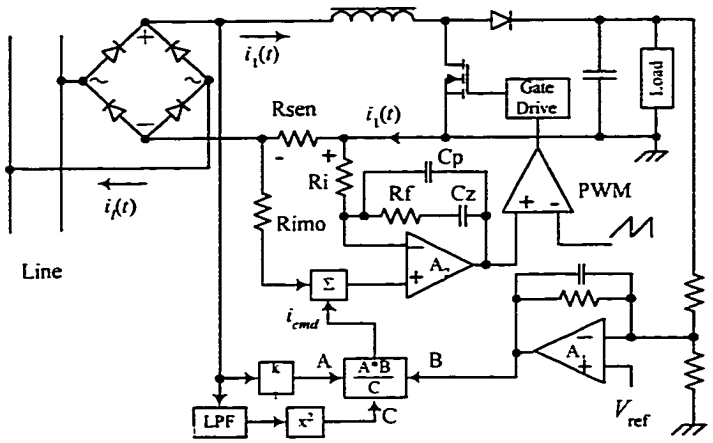


Figure 3-3 Boost corrector using average current control

Figure 3-3 shows a boost PFC circuit using average current control strategy. In the feedforward loop, a low value resistor R_{sen} is used to sense the line current. Through the op-amp network formed by R_i, R_{imo}, R_f, C_p, C_z and A_2, average line current is detected and compared with the command current signal, i_{cmd}, which is generated by the product of line voltage signal and the output voltage error signal.

There is a common issue in CCM shaping technique, i.e., when the line voltage increases, the line voltage sensor provides an increased sinusoidal reference for the feedforward loop. Since the response of feedback loop is much slower than the feedforward loop, both the line voltage and the line current increase, i.e., the line current is heading to wrong changing direction (with the line voltage increasing, the line current should decreases). This results in excessive input power, causing overshoot in the output voltage. The square block, x^2, in the line voltage-sensing loop shown in Fig. 3-3, provides a typical solution for this problem. It squares the output of the low-pass filter (LPF), which is in proportion to the amplitude of the line voltage, and provides the divider

(A*B)/C with a squared line voltage signal for its denominator. As a result, the amplitude of the sinusoidal reference i_{cmd} is negatively proportional to the line voltage, i.e., when the line voltage changes, the control circuit leads the line current to change in the opposite direction, which is the desired situation. The detailed analysis and design issues can be found some open literatures [19-21].

As it can be seen, the average current control is a very complicated control strategy. It requires sensing the inductor current, the input voltage and the output voltage. An amplifier for calculating the average current and a multiplier are needed. However, because of today's advances made in IC technology, these circuits can be integrated in a single chip. Commercial products such as Unitrode-UC3854A/B and SGS-Thomson-L4981A/B are available for the implementation of the average current control.

B. Variable frequency peak current control

Although the average current control is a more desired strategy, the peak current control has been widely accepted because it has a simpler and more efficient control circuit [24-29]. In variable frequency peak control strategy, shown in Fig. 3-4, the output

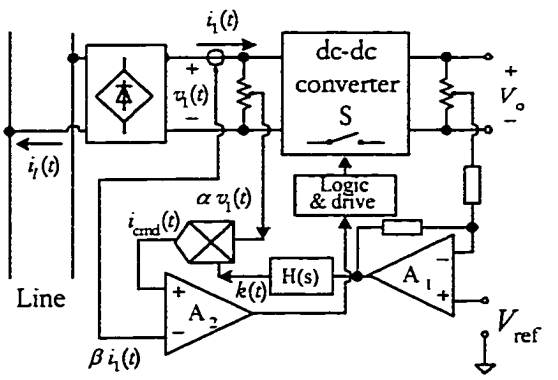


Fig. 3-4 Block diagram for variable frequency peak current control

error signal $k(t)$ is fed back through its outer loop. This signal is multiplied by the line voltage signal $\alpha v_1(t)$ to form a line current command signal $i_{cmd}(t)$ ($i_{cmd}(t) = \alpha k(t) \cdot v_1(t)$). The command signal $i_{cmd}(t)$ is the desired line current shape since it follows the shape of the line voltage. The actual line current is sensed by a transducer, resulting in signal $\beta i_1(t)$ that must be re-shaped to follow $i_{cmd}(t)$ by feeding it back through the inner loop. After comparing the line current signal $\beta i_1(t)$ with the command signal $i_{cmd}(t)$, the following control strategies can be realized, depending on its logic circuit:

-Constant on-time control

Its input current waveform is given in Fig. 3-5(a). Letting the fixed on-time be T_s, the control rules are:

- At $t = t_k$ when $\beta i_1(t_k) = i_{cmd}(t_k)$, S is turned on;
- At $t = t_k + T_{on}$, S is turned off.

-Constant off-time control

The input current waveform is shown in Fig. 3-5(b). Assuming the off-time is T_{off}, the control rules are:

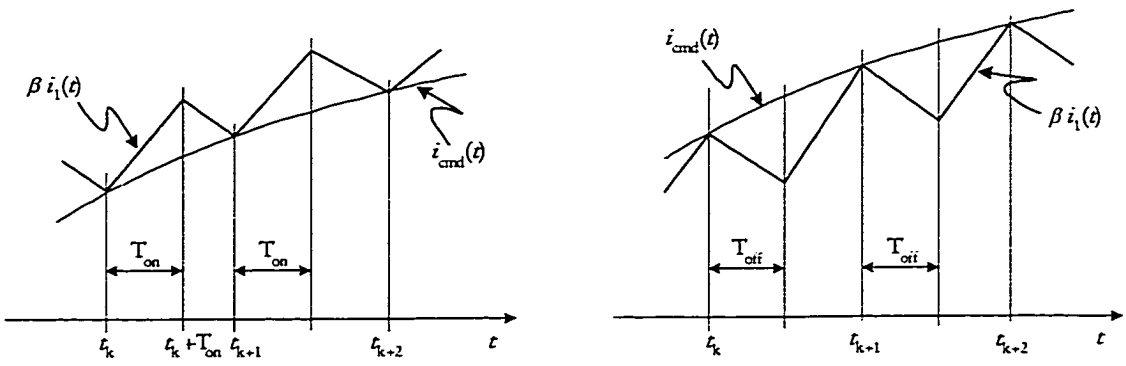


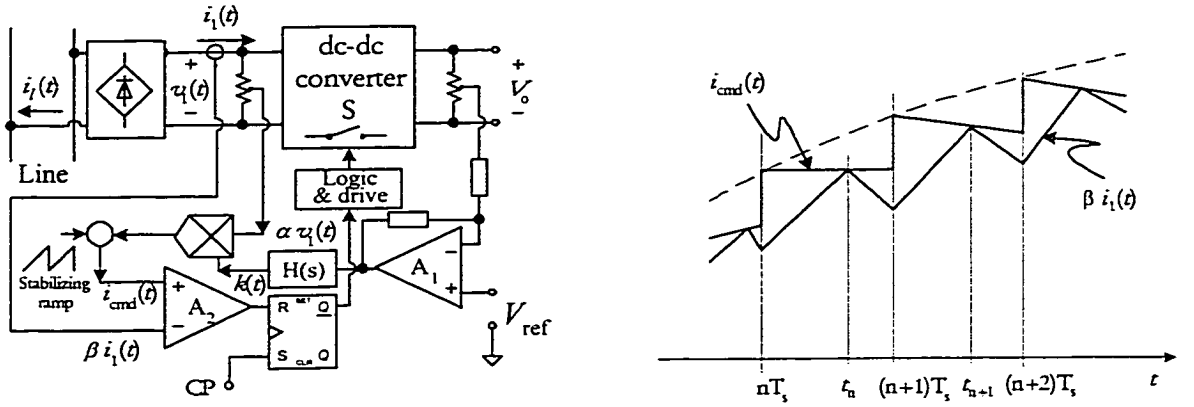
Figure 3-5 Input current waveforms for variable frequency peak current control: (a) constant on-time control; (b) constant off-time control

- At $t = t_k$ when $\beta i_1(t_k) = i_{cmd}(t_k)$, S is turned off;
- At $t = t_k + T_{off}$, S is turned on.

C. Constant frequency peak current control

Generally speaking, to make it easier to design the EMI filter and to reduce harmonics, constant switching frequency AC/DC PFC converter is preferred [24, 26]. Based on the block diagram shown in Fig. 3-4, with T_s is the switching period, the following control rules can be considered to realize a constant frequency peak current control (shown in Fig. 3-6(b)):

- At $t = nT_s$, S is turned on;
- At $t = t_n$ when $\beta i_1(t_n) = i_{cmd}(t_n)$, S is turned off.



(a) (b)

Figure 3-6 Constant frequency peak current control with stabilizing ramp compensation: (a) block diagram; (b) line current waveform

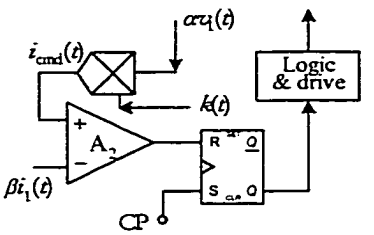


Figure 3-7 Logic circuit for constant frequency peak current control

The logic circuit for the above control rules can be realized by using an R-S flip-plop with a constant frequency setting clock pulse (CP), as shown in Fig. 3-7. Unfortunately, this logic circuit will result in instability when the duty ratio exceeds 50% [24]. This problem can be solved by subtracting a stabilizing ramp signal from the original command signal. Figure 3-6(a) shows a complete block diagram for typical constant frequency peak current control strategy. The line current waveform is shown in Fig. 3-6(b).

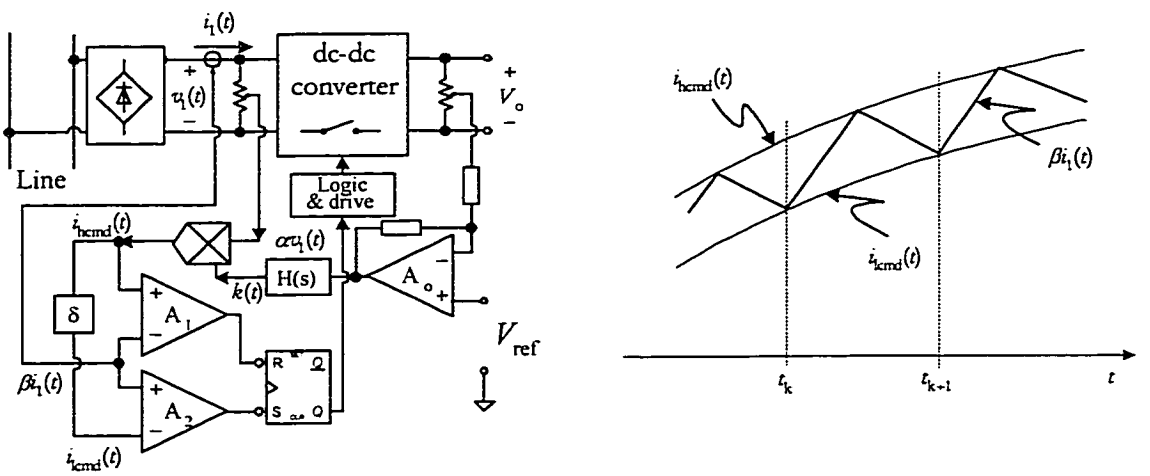
It should be noticed that in both variable frequency and constant frequency peak current control strategies, either the input current or the switch current could be controlled. Thus it makes possible to apply these control methods to buck type converters. There are several advantages of using peak current control:

- The peak current can be sensed by current transformer, resulting in reduced transducer loss;
- The current-error compensator for average control method has been eliminated;
- Low gain in the feedforward loop enhances the system stability;
- The instantaneous pulse-by-pulse current limit leads to increased reliability and response speed.

However the three signals, line voltage, peak current and output voltage signals, are still necessary to be sensed and multiplier is still needed in each of the peak current control method. Comparing with the average current control method, the input current ripple of these peak current control methods may be high when the line voltage is near the peak value. As a result, considerable line current distortion exists under high line voltage and light low operation conditions.

D. Hysteresis control

Unlike the constant on-time and the constant off-time control, in which only one current command is used to limit either the minimum input current or the maximum input current, the hysteresis control has two current commands, $i_{hcmd}(t)$ and $i_{lcmd}(t)$ ($i_{lcmd}(t)=\delta i_{hcmd}(t)$), to limit both the minimum and the maximum of input current. The advantage of using hysteresis control is that if the hyster-band is narrow, it has smaller ripple in the input current [30-34]. However, the narrower the hyster-band, the higher the



(a) (b)

Figure 3-8 Hysteresis control: (a) block diagram; (b) line current waveform

switching frequency. Moreover, the switching frequency varies with the change of line voltage, resulting in difficulty in design of the EMI filter. The circuit diagram and input current waveform are given in Figs. 3-8(a) and (b), respectively. When $\beta i_1(t) \geq i_{hcmd}(t)$, a negative pulse is generated by comparator A_1 to reset the R-S flip-flop. When $\beta i_1(t) \leq i_{lcmd}(t)$, a negative pulse is generated by comparator A_2 to set the R-S flip-flop. The control rules are:

- At $t = t_k$ when $\beta i_1(t_k) = i_{lcmd}(t)$, S is turned on;
- At $t = t_{k+1}$ $\beta i_1(t_{k+1}) = i_{hcmd}(t)$, S is turned off;
- When $\beta i_1(t) = i_{hcmd}(t) = i_{lcmd}(t)$, S stays off or on.

Like the above mentioned peak current control methods, the hysteresis control method has simpler implementation, enhanced system stability, and increased reliability and response speed. In addition, it has better control accuracy than that the peak current control methods have. However, this improvement is achieved on the penalty of wide range of variation in the switching frequency.

E. Charge control

In order to make the average control method to be applicable for buck-derived topologies where the switch current instead of the inductor current needs to be controlled, an alternative method to realize average current control, namely, charge control was proposed by W. Tang, F. Lee, *et al* [35-37]. Since the total charge of the switch current per switching cycle is proportional to the average value of the switch current, the average current can be detected by a capacitor-switch network. Figure 3-9 shows a block diagram for charge control. The switch current is sensed by current transformer T1 and charges the capacitor C_T to form average line current signal. As the switch current increase, the

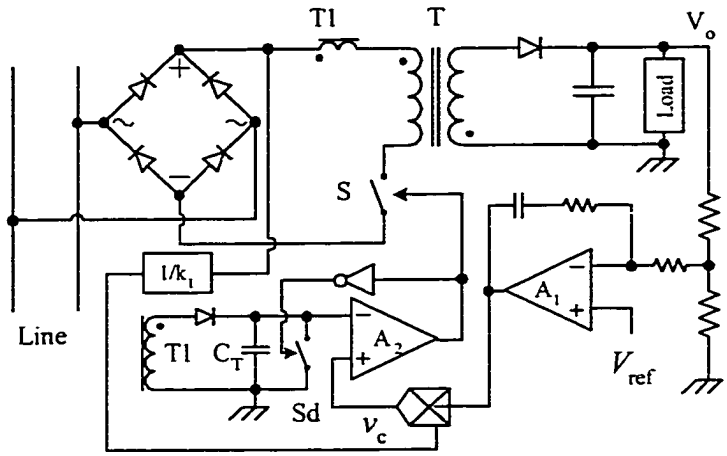


Figure 3-9 Flyback PFC converter using charge control

charge on capacitor C_T also increase. When the voltage reaches the control command v_c, the power switch turns off. At the same time, the switch Sd turns on to reset the capacitor. The next switching cycle begins with the power switch turning on and the switch Sd turning off by a clock pulse.

The advantages of charge control are:

- Ability to control average switch current.
- Better switching noise immunity than peak current control.
- Good dynamic performance.
- Elimination of turn off failure in some converters (e.g. multi-resonant converter) when the switch current reaches its maximum value.

The disadvantages are:

- Synthesis of the reference v_c still requires sensing both input and output voltage and use of a multiplier.
- Subharmonic oscillation may exist.

F. Nonlinear-carrier (NLC) control

To further simplify the control circuitry, recently D. Maksimovic, Y. Jang and R. Erikson proposed a new control method, namely, nonlinear-carrier control [38, 39]. In CCM operation, since the input voltage is related to the output voltage through the conversion ratio, the input voltage information can be recovered by the sensed output voltage signal. Thus the sensing of input voltage can be avoided, and therefore, the multiplier is not needed, resulting in significant simplification in the control circuitry. However, complicated nonlinear-carrier waveform generator and its design are involved. Figure 3-10 shows the block diagram of the nonlinear-carrier charge control [38].

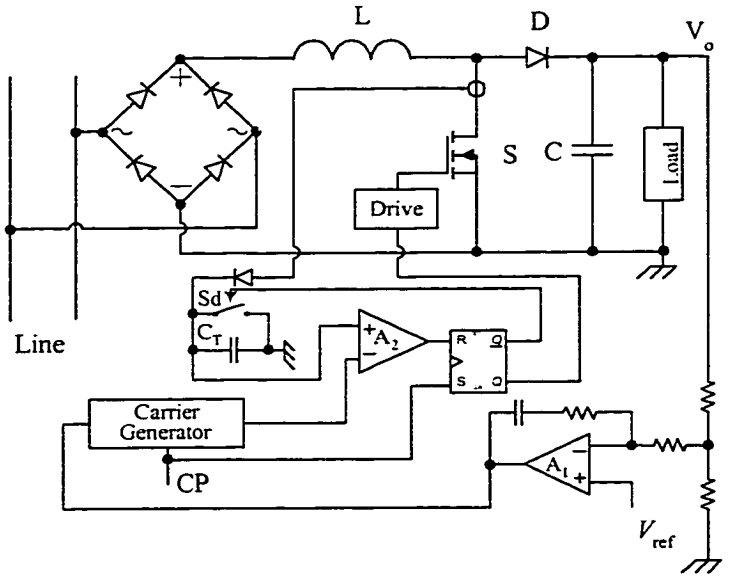


Figure 3-10 Boost PFC converter using nonlinear carrier control

3.3.2 *Voltage Mode Control*

Generally, current mode control is preferred in current source driven converters, as the boost converter. To develop controllers for voltage source driven converter, like the buck converter and to improve dynamic response, voltage mode control strategy was proposed [40, 41]. Figure 3-11 shows the input circuit of an AC/DC converter and its phasor diagram representation, where ϕ is the phase shift between the line current and the capacitor voltage. An L-C network could be added to the input either before a switch mode rectifier (SMR) or after a passive rectifier to perform such kind of control. In boost type converter, the inductor L_i is the input inductor. It can be seen from the phasor diagram that to keep the line current in phase with the line voltage, we can either control the capacitor voltage or the inductor voltage. If the capacitor voltage is chosen as controlled variable, the control strategy is known as delta modulation control.

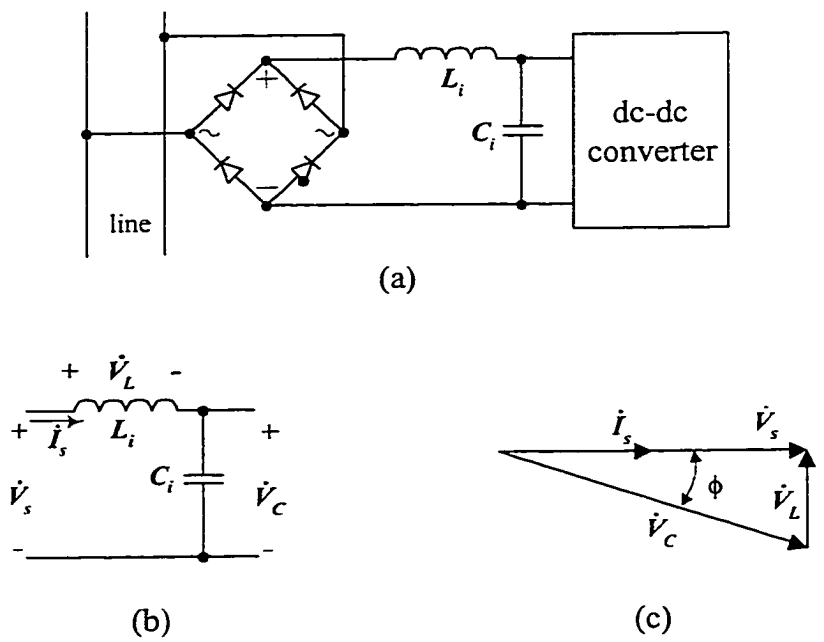


Figure 3-11 Voltage control AC/DC converter: (a) input circuit of voltage control converter; (b) simplified input circuit; (c) phasor diagram

A. Capacitor voltage control

Figure 3-12 gives a switch-mode rectifier (SMR) with power factor correction using capacitor voltage control [40]. The capacitor voltage $v_{c1}(t)$ is forced to track a sinusoidal command signal $v_{c1}^{*}(t)$ to indirectly adjust the line current in phase with the line voltage. The command signal is the product of the line voltage signal with a phase shift of ϕ and the feedback error signal. The phase shift ϕ is a function of the magnitudes of line voltage and line current, therefore the realization of a delta control is not really simple. In addition, since ϕ is usually very small, a small change in capacitor voltage will cause a large change in the inductor voltage, and hence in the line current. Thus it make the circuit very sensitive to parameter variations and perturbations.

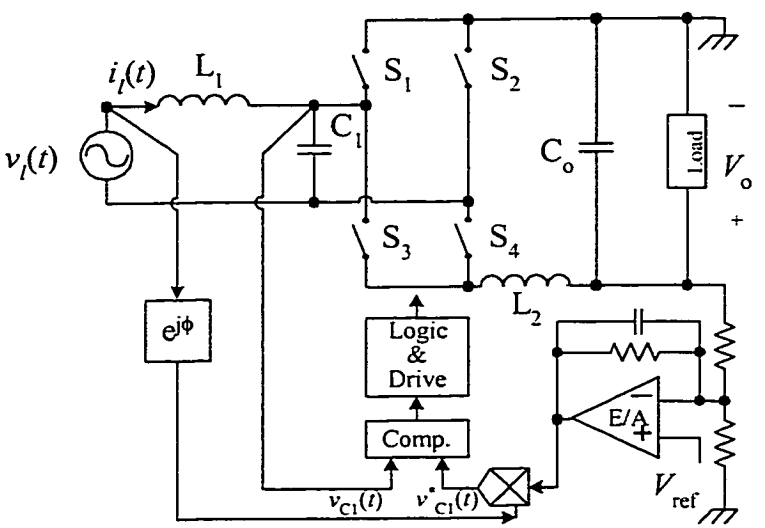


Figure 3-12 Switch-mode rectifier using capacitor voltage control

B. Inductor voltage control

To overcome the above shortcomings, inductor voltage control strategies was reported [41]. Figure 3-13 shows an SMR with power factor correction using inductor voltage control. As the phase difference between the line voltage and the inductor voltage is fixed at 90° ideally, the control circuit is simpler in implementation than that of capacitor voltage control. As the inductor voltage is sensitive to the phase shift ϕ but not sensitive to the change in magnitude of reference, the inductor voltage control method is more effective in keeping the line current in phase with the line voltage. However, in the implementations of both the two kinds of voltage control methods hysteresis technique is normally used. Therefore, unlike the previous current mode control, variable frequency problem is encountered in these control methods.

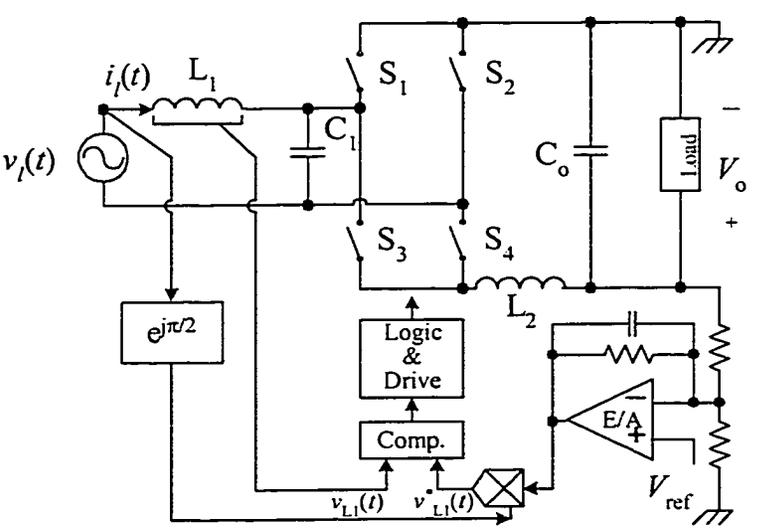


Figure 3-13 Switch-mode rectifier using inductor voltage control

Generally speaking, by using CCM shaping technique, the input current can trace the wave shape of the line voltage well. Hence the power factor can be improved efficiently. However, this technique involves in design of complicated control circuits. Multi-loop control strategy is needed to perform input current shaping and output regulation. In most CCM shaping techniques, current sensor and multiplier are required, which result in higher cost in practical applications. In some cases, variable frequency control is inevitable, resulting in additional difficulties in its closed-loop design. Table 3-1 gives a comparison among these control methods.

Table 3-1 Comparison of CCM shaping techniques

	Average current	VF peak-current	CF peak-current	Hysteresis	Charge	Nonlinear carrier	Capacitor voltage	Inductor voltage
Input ripple	Low	High	High	Low	Low	Low	Low	Low
Control accuracy	Good	Fair	Fair	Good	Medium	Medium	Medium	Medium
Switching frequency	Constant	Variable	Constant	Variable	Constant	Constant	Variable	Variable
Stability	Good	Medium	Medium	Good	Fair	Fair	Fair	Good
Dynamic response	Slow	Slow	Slow	Fast	Fast	Fast	Fast	Fast
Control signal sensed for inner loop	Input current & input voltage	Input (or switch) current & input voltage	Input (or switch) current & input voltage	Input current & input voltage	Input (or switch) current & input voltage	Input (or switch) current	input voltage & capacitor voltage	input voltage & inductor voltage
Inner loop E/A	✓	×	×	✓	×	×	×	×
Multiplier	✓	✓	✓	✓	✓	×	✓	✓

3.4 DCM INPUT TECHNIQUE

To get rid of the complicated control circuit invoked by CCM shaping technique and reduce the cost of the electronic interface, DCM input technique can be adopted in low power to medium power level applications.

In DCM, the inductor current of the core converter is no longer a valid state variable since its state in a given switching cycle is independent of the value in the previous switching cycle [12]. The peak of the inductor current is tracing the line voltage automatically, resulting in sinusoidal-like average input current (line current), shown in Fig. 3-14. This is why DCM input circuit is also called "voltage follower" or "automatic controller." The benefit of using DCM input circuit for PFC is that no feedforward control loop is required. This is also the main advantage over a CCM power factor correction circuit, in which multi-loop control strategy is essential. However, the input inductor operating in DCM can not hold the excessive input energy because it must release all its stored energy before the end of each switching cycle. As a result, a bulky capacitor is used to balance the instantaneous power between the input and output. In

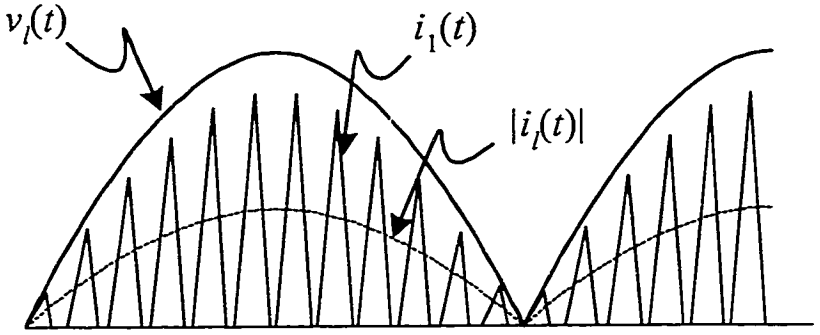


Figure 3-14 Input inductor operating in DCM draws sinusoidal-like average input current (line current)

addition, in DCM, the input current is normally a train of triangle pulses with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current.

In two-stage PFC power supply, the DCM converter is connected in front of the ac line to achieve high input power factor and provide a roughly regulated dc bus voltage, as shown in Fig. 3-15. This stage is also known as "pre-regulator." The duty ratio of the pre-regulator should be maintained relatively stable so that high power factor is ensured. To stabilize the dc bus voltage, a bank capacitor is used at the output of the pre-regulator. The second stage, followed by the pre-regulator, is a DC/DC converter, called post-regulator, with its output voltage being tightly controlled. This stage can operate either in DCM or in CCM. However, CCM is normally preferred to reduce the output voltage ripple.

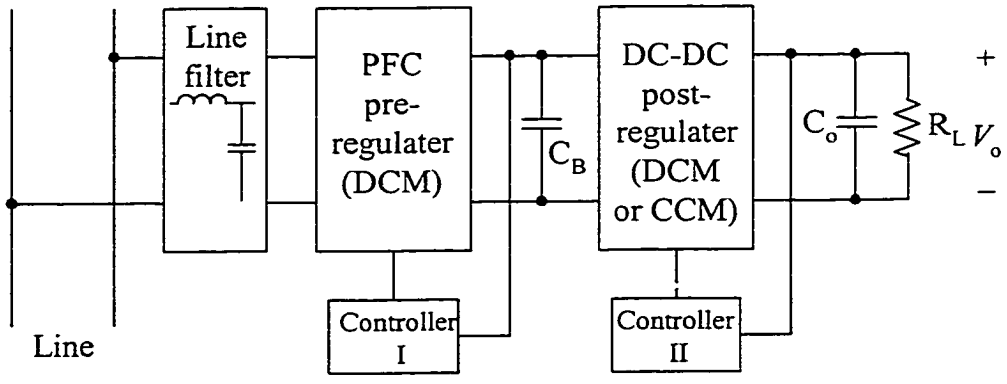


Fig. 3-15 DCM input pre-regulator in two-stage AC/DC power supply

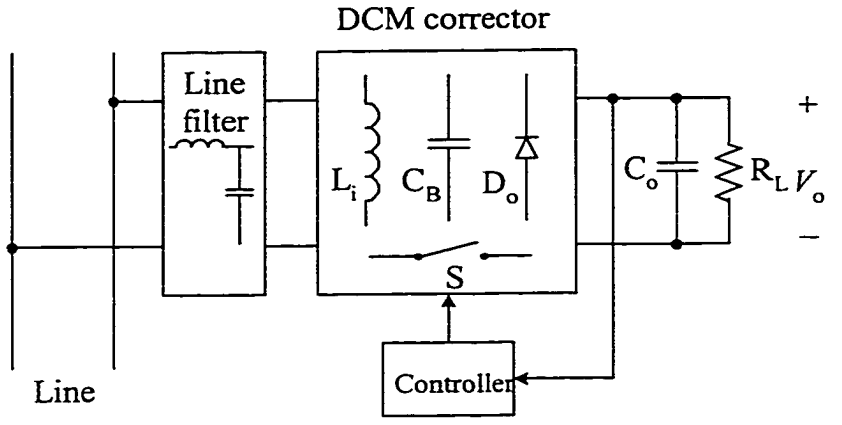
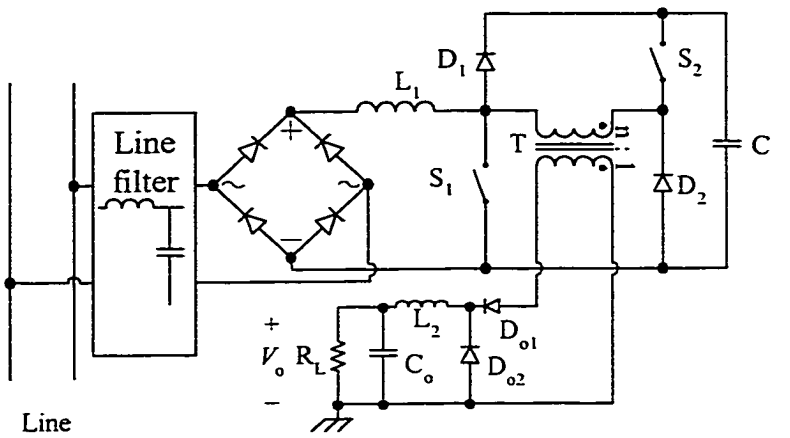


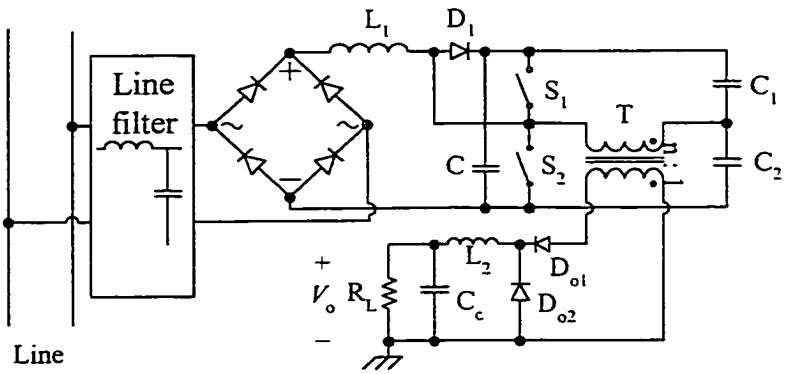
Figure 3-16 DCM input corrector in single-stage AC/DC power supply

DCM input technique has been widely used in one-stage power factor correction circuit configurations. Using a basic converter (usually boost or flyback converter) operating in DCM combining with another isolation converter can form a one-stage power factor correction circuit. A storage capacitor is generally required to hold the dc bus voltage in these combinations. Unlike the two-stage PFC circuit, in which the bus voltage is controlled, the single-stage PFC converter has only one feedback loop from the output. The input circuit and the output circuit must share the same control signal. Figure 3-16 shows the diagram of single-stage circuit.

A number of combinations have been studied by the current researchers [46-48]. Figures 3-17 and 3-18 show a few examples of successful combinations. Since the input circuit and the output circuit are in a single stage, it is possible for them to share the same power switch. Thus it results in single-stage single-switch power factor correction (S^4-PFC) circuit, as shown in Fig. 3-18 [49].



(a)



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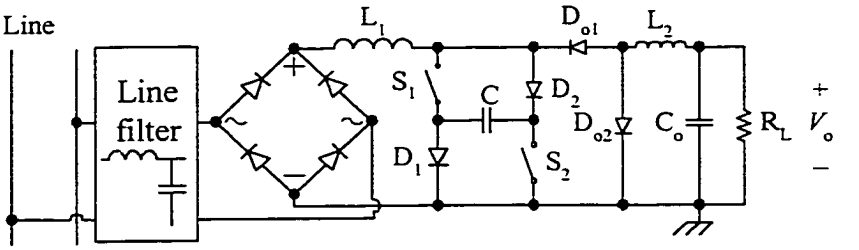


(c)

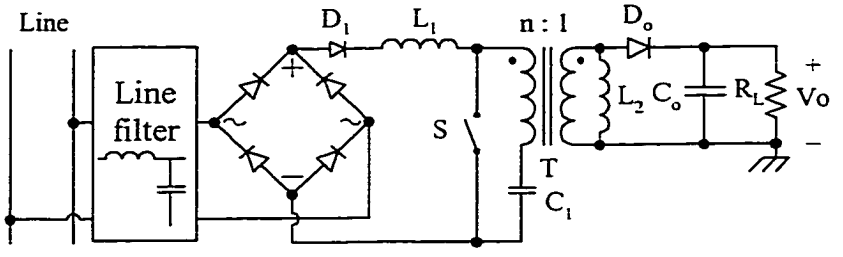
Figure 3-17 Two-switch single stage power factor correctors: (a) Boost-forward converter; (b) Boost-half bridge converter; (c) Sheppard-Taylor converter

Due to the simplicity and low cost, DCM boost converter is most commonly used for unity power factor operation. The main drawback of using boost converter is that it shows considerable distortion of the average line current owing to the slow discharging of the inductor after the switch is turned off.

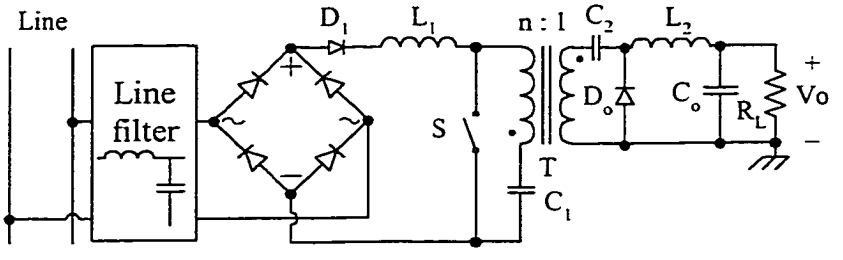
The output DC/DC converter can operate either in DCM or in CCM if small output ripple is desired. If the output circuit operates in CCM, there exists a power unbalance in S^4-PFC converter when the load changes. Because the duty ratio is only sensitive to the output voltage in CCM operation, when the output power (output current) decreases, the duty ratio will keep unchanged. As both the input and the output circuit share the power switch, the input circuit will draw an unchanged power from the ac source. As a result, the input power is higher than the output power. The difference between the input power and the output power has to be stored in the storage capacitor, and hence increasing in the dc bus voltage occurs. With the dc bus voltage's rising, the duty ratio decreases. This process will be finished until a new power balance is built. As we can see, the new power balance is achieved at the penalty of increased voltage stress, resulting in high conduction losses in circuit components. Particularly, the high bus voltage causes difficulties in developing S^4-converter for universal input (input line voltage *rms* value from AC 90V to AC 260V) application.

Recent research on improving the converter performances can be found in the open literature [46, 54-61]. Figure 3-19(a) shows a modified forward converter operating in DCM for PFC [61]. Variable switching frequency control is used to reduce the capacitor voltage [60]. The circuit shown in Fig. 3-19(b) has fast transient response due to both the input boost inductor and the output flyback transformer are operating in DCM

[46]. A modified boost-forward PFC converter was proposed [54], shown in Fig. 3-19(c), in which a negative current feedback is introduced to the input circuit by the coupled windings of forward transformer. A series resonant circuit called charge pump circuit was introduced into S^4-PFC circuit [55], shown in Fig. 3-19(d). As the load decrease, the charge pump circuit can suppress the dc bus voltage automatically.



(a)



(b)

Figure 3-18 Single-stage single-switch power factor correction circuits: (a) boost-flyback combination circuit (BIFRED); (b) boost-buck combination circuit (BIBRED)

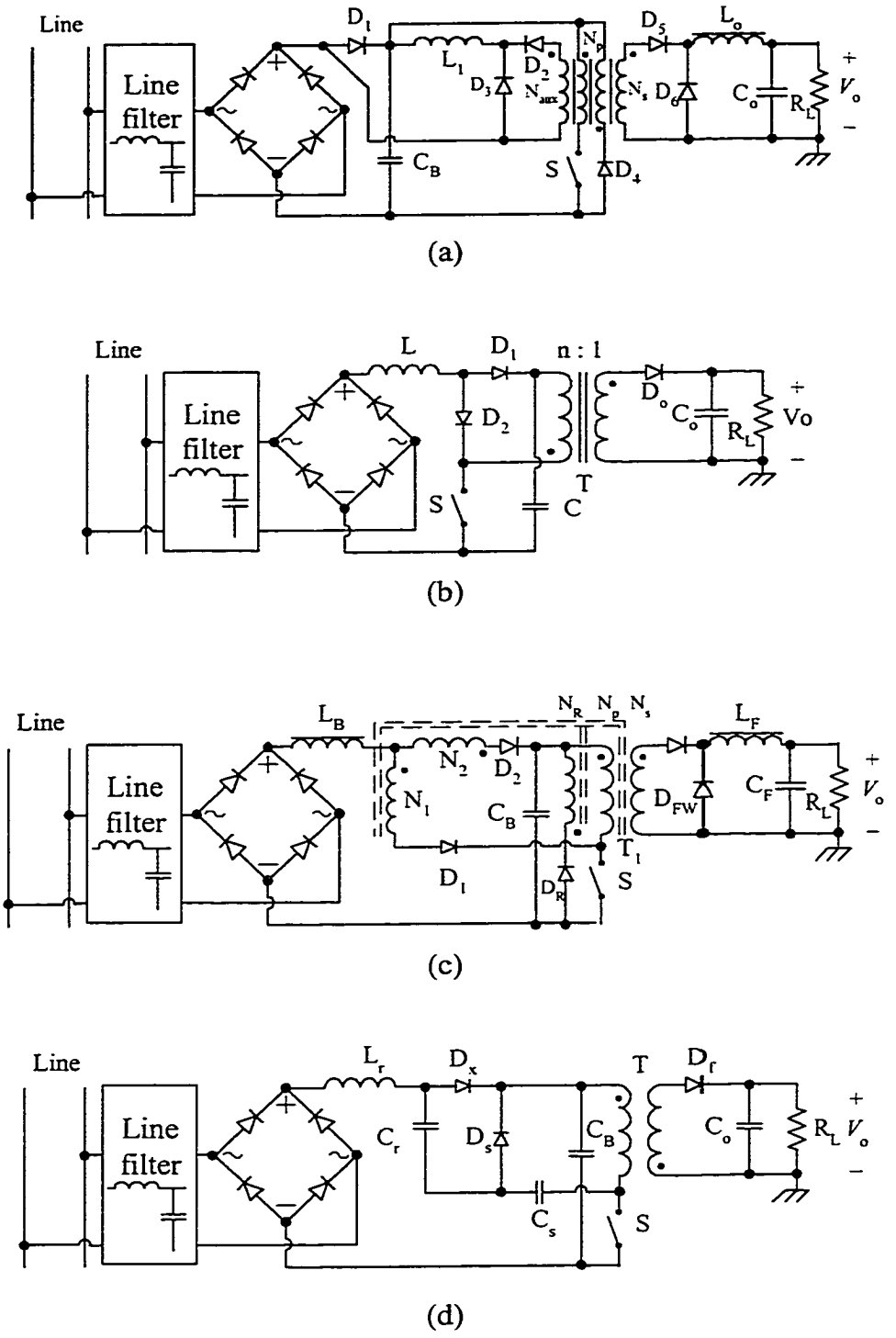


Fig. 3-19 Improved S^4-PFC converters: (a) Modified forward; (b) Boost-flyback combination; (c) Boost-forward PFC circuit with reduced bus voltage; (d) Boost-flyback PFC circuit with Charge pump circuit

3.5 Other PFC Techniques

Extensive research in PFC continues to yield countless new techniques [72-83]. The research topics are mainly focused on improvements of the PFC circuit performs such as fast performs, high efficiency, low cost, small input current distortion and output ripple.

- *Parallel configuration for power factor correction* [75]

In parallel PFC circuit, power from the ac main to the load flows through two parallel paths. The main path is a rectifier, in which power is not processed twice for PFC, whereas the other path processes the input power twice for PFC purpose. High efficiency can be obtained by this method.

- *Second-harmonic-injected method* [76]

In DCM input technique, even the converter operates at constant duty ratio, current distortion still exists. The basic idea of second-harmonic-injected method is compensating the duty ratio by injecting a certain mount of second harmonic into the duty ratio to modify the input I-V characteristic of the input converter. However, the output voltage may be affected by the modified duty ratio.

- *Interleaved method* [77]

An interleaved PFC circuit composed of several input converters in parallel. The peak input current of these converters follow the line voltage and are interleaved. A sinusoidal total line current is obtained by superimposing all the input current of the converters. The advantage of this method is that the converter input current can be easily smoothed by input EMI filter.

3.6 SUMMARY

To reduce losses, and decrease weight and size associated with converting ac power to dc power in linear power supply, switch mode power supplies (SMPS) were introduced. The high non-linearity of this kind of power electronic systems handicaps itself by providing the utility power system with low power factor (PF) and high total harmonic distortion (THD). These unwanted harmonics are commonly corrected by incorporating power factor correction (PFC) technique into the SMPS. This paper gives a technical review of current research in high-frequency power factor correction, including the definition of PF and THD, configuration of PFC circuit, DCM input technique, and CCM shaping technique. The common issue of these techniques is to properly process the power flow so that the constant power dissipation at the output is reflected into ac power dissipation with two times the line frequency. Technically, PFC techniques encounter the following tradeoffs:

(a) simplicity and accuracy: single-stage PFC circuit has simple topology and simple control circuit, but has less control accuracy while two-stage PFC circuit has the contrary performance;

(b) control simplicity and power handling capability: DCM input technique requires no input current control, but has less power handling capability while CCM has multi-loop control and has more power handling capability;

(c) switching frequency and conversion efficiency: to reduce weight and size of the PFC converter, higher switching frequency is desired. However, the associated switching losses result in decrease in conversion efficiency;

(d) frequency response and bandwidth: to have good dynamic response, wider bandwidth is desired, however to achieve high power factor bulk storage capacitor and output capacitor has to be used.

In the past decades, research in PFC techniques has led to the development of more efficient circuits and control strategies in order to optimize the design without compromising the above tradeoffs. Moreover, since the growth in power electronics strongly relies on the development of semiconductor devices, the recent advent of higher rating power devices, it is believed that the switching mode power factor correctors will completely replace the existing passive reactive compesators in power system. In the distributed power system (DPS) where small size and high efficiency are of extreme importance, a new soft-switching technique has been used in designing PFC circuits. With the ever increasing market demanding for ultra-fast computer, the need for low output voltage (typically 3.3V) with high output currents and high efficiency converters has never been greater. Research efforts in developing high-frequency high efficiency power factor correction circuits will continue to grow.

CHAPTER 4

NEW SINGLE-SATAGE SINGLE-SWITCH CONVERTERS WITH HIGH POWER FACTOR AND LOW STORAGE CAPACITOR VOLTAGE

4.1 INTRODUCTION

Generally, the S^4 PFC circuits suffer from high voltage stress on the bulk capacitor, which leads to selection of high voltage rating capacitor in practical design. Since the cost of the bulk capacitor is highly sensitive to the voltage rating, to reduce power supply cost, we desire an S^4 converter topology operating with low bulk capacitor voltage.

In this chapter, we will present two new S^4 PFC converter topologies. The first topology is a DCM-CCM combination of flyback converter and forward converter. Through the discussion of general principle of operation on the basic topologies in Chapter 2, we know that the flyback type input circuit offers the best power factor at the front-end. Nevertheless, the control characteristic is independent of the connection of the bulk capacitor and the output circuit. So, with the flyback type input circuit, it is possible to develop an S^4 converter with low bulk capacitor voltage. The second topology is a DCM-DCM type. Since the bulk capacitor voltage does not change with the load in this type of converter, it is easier to design the converter applicable for universal input. The input circuit is a boost type and the output circuit is a modified forward converter. With

two bulk capacitors to split the input inductor demagnetizing voltage V_1, the voltage stress on each capacitor is reduced.

4.2 A NEW S^4 CONVERTER EMPLOYING FLYBACK INPUT CIRCUIT

4.2.1 The Proposed Converter Topology

The basic circuit schematic of the proposed new single-stage single-switch isolated converter is shown in Fig. 4-1. The input circuit employs a flyback topology and the output circuit is a forward converter. The power switch and the storage capacitor are placed between the two circuits with diodes D_1 and D_2 coordinating their two separate operations.

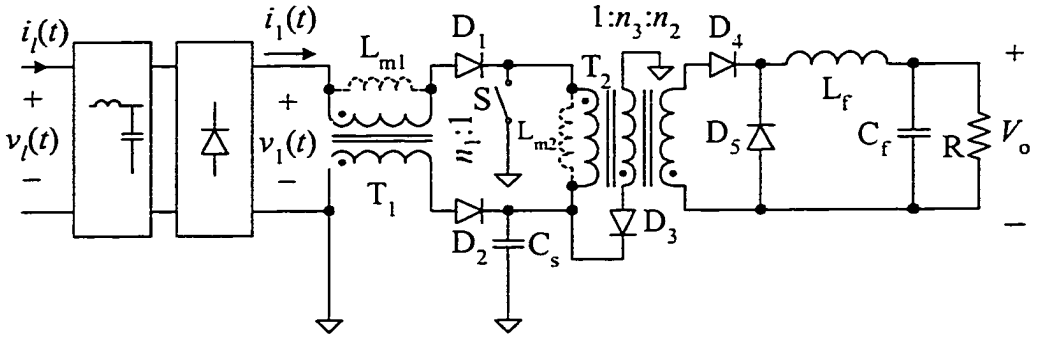


Figure 4-1 Basic circuit schematic of the proposed flyback-forward PFC converter

Table 4-1 Switching periods: time intervals and status of devices

Period	Time interval	Conducting device					
		S	D_1	D_2	D_3	D_4	D_5
P1	$t_0 \le t < t_1$	×	×			×	
P2	$t_1 \le t < t'_2$			×	×		×
	$t'_2 \le t < t_2$				×		×
P3	$t_2 \le t < t_0 + T_s$						×

It can be shown that in steady-state the converter operates in three switching periods during one switching cycle. Table 4-1 shows the three switching periods and their corresponding times and the status of the switching devices.

4.2.2 Principle of Operation

Figure 4-2 shows the equivalent circuits for the three switching periods. At the beginning of Switching period P1, we assume that the power switch is off and all the energy stored in transformers T_1 and T_2 have been completely removed, i.e., all the windings are de-energized. Switching period P1 begins when the power switch is turned on at t = 0 as shown in Fig. 4-3. During P1, since D_1 is conducting, the primary voltage of T_1 becomes the line voltage, $v_l(t)$, causing the transformer T_1 to begin magnetizing. Due to the polarity of the secondary winding of T_1 (flyback transformer), diode D_2 is blocked, resulting in energizing T_1 by the line voltage $v_l(t)$. On the other hand, the capacitor voltage V_{Cs} is applied to the primary winding of T_2, blocking D_3. Because T_2 is a forward transformer, the energy stored in the capacitor C_s is being transferred to the load during this stage. This switching period ends when the power switch is turned off. During Switching period 2, the power switch is turned off and diode D_1 is reverse biased, and the flyback transformer T_1 is de-energized through diode D_2. The energy stored in T_1 is transferred to capacitor C_s. At the same time, the forward transformer is demagnetized by its tertiary winding n_3 and D_3, and the magnetizing energy is fed back to the capacitor C_s. Because of the polarity of the secondary winding n_2, diode D_4 is turned off and diode D_5 is turned on to continue the output filter inductor current. In this period, energy transfer from the line to load is interrupted and energy reduction of the storage capacitor in

Switching period 1 is compensated. When T_1 and T_2 are completely de-energized, i.e. $i_{D3}(t)$ and $i_{D2}(t)$ become zero, the converter's operation enters Switching period 3. In P3, the output filter maintains the output voltage until the next switching cycle begins. Typical steady-state operation waveforms are shown in Fig. 4-3.

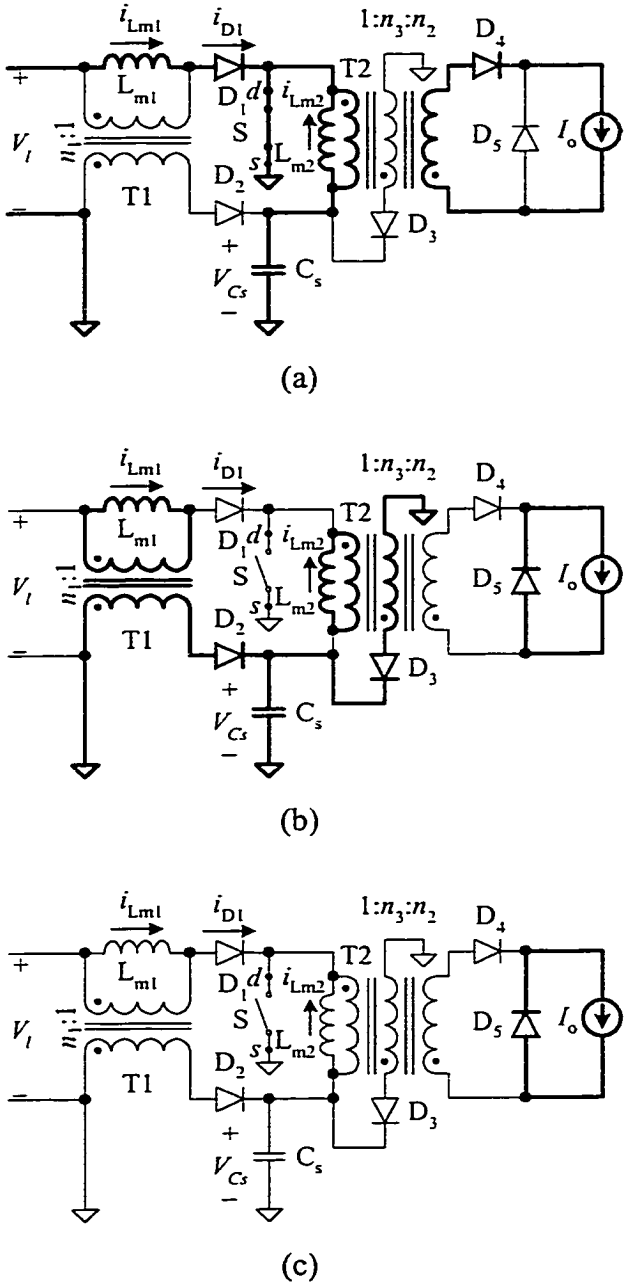


Figure 4-2 Equivalent topologies for the three switching periods: (a) P1(t_0-t_1); (b) P2(t_1-t_2); (c) P3(t_2 - T_s+t_0)

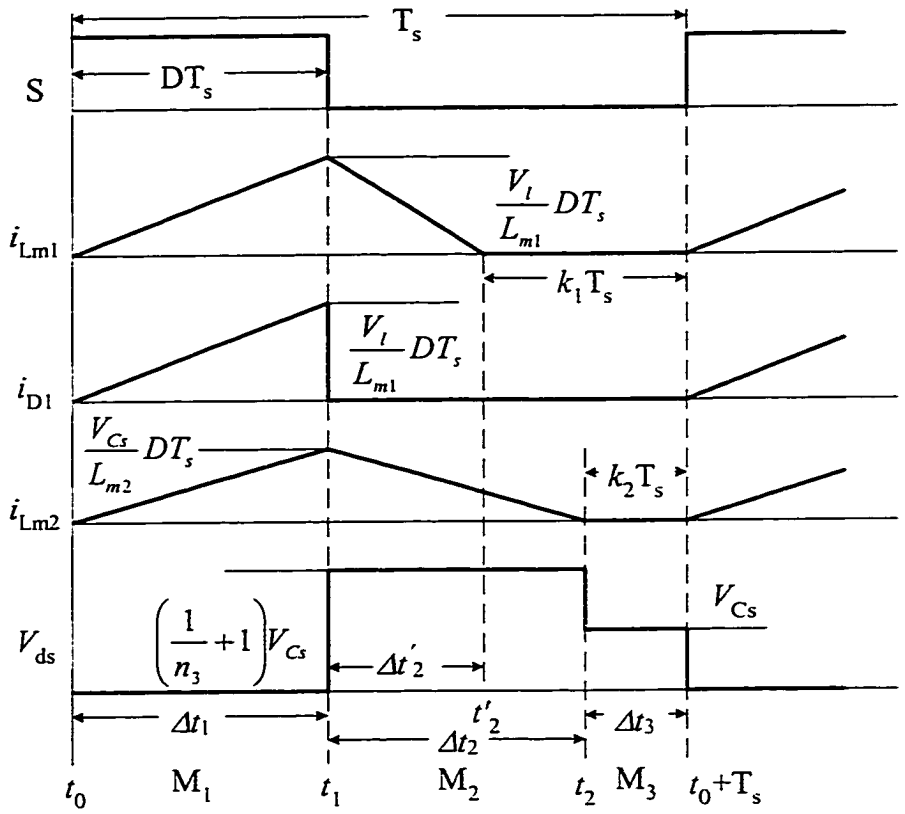


Figure 4-3 Theoretical key waveforms of the proposed converter

4.2.3 Steady-State Analysis

To simplify the steady-state analysis, the following assumptions are made:

1) All circuit components and devices are ideal except magnetizing inductances L_{m1} and L_{m2} are included for transformers T_1 and T_2, respectively;
2) The storage capacitance, C_s, is sufficiently large so that its voltage, V_{Cs}, is considered constant dc;
3) The inductance of the output filter inductor is sufficiently large so that the filter inductor can be considered a current source, I_o;

4) The switching frequency is much higher than the line frequency so that the input voltage of the converter can be considered a constant voltage source, V_l, during the switching cycle.

4.2.3.1 Steady-state waveforms

According to the above assumptions, the three operation switching periods P1, P2 and P3 can be depicted by the equivalent topologies shown in Figs. 4-2(a), (b) and (c), respectively. The thicker lines indicate the conduction paths. The typical key waveforms are shown in Fig. 4-3. Letting $t_0 = 0$, the steady-state waveforms are described as follows:

Switching period 1 ($0 \le t < t_1$) :

Due to the conduction of the power switch S, the line voltage V_l is applied to the magnetizing inductor L_{m1} of T_1 and the capacitor voltage V_{Cs} is applied across L_{m2}. Therefore, we have,

$$i_{Lm1}(t) = i_{D1}(t) = \frac{V_l}{L_{m1}} t \tag{4.1a}$$

$$i_{Lm2}(t) = \frac{V_{Cs}}{L_{m2}} t$$

$$V_{ds}(t) = 0$$

The duration of this stage is

$$\Delta t = DT_s \tag{4.1b}$$

where $D = \frac{t_1}{T_s}$, and t_1 is the time at which S is turned off.

Switching period 2 ($t_1 \le t < t_2$):

Diodes D_2 and D_3 are turned on during this switching period. Reflected V_{Cs} to the primary sides of T_1 and T_2, the magnetizing inductors L_{m1} and L_{m2} voltages are V_{Cs}/n_1 and V_{Cs}/n_3, respectively. The voltage across filter inductor L_f is V_o. Using Fig. 4-2(b), the following expressions are obtained:

$$i_{Lm1}(t)=\begin{cases}\dfrac{V_I}{L_{m1}}DT_s - \dfrac{V_{Cs}}{n_1 L_{m1}}(t-DT_s) & (DT_s \le t \le t_2') \\ 0 & (t_2' < t \le t_2)\end{cases} \tag{4.2a}$$

$$i_{Lm2}(t) = \frac{V_{Cs}}{L_{m2}}DT_s - \frac{V_{Cs}}{n_3 L_{m2}}(t-DT_s)$$

$$V_{ds}(t)=\begin{cases}\left(\dfrac{1}{n_3}+1\right)V_{Cs} & DT_s \le t \le t_2' \\ V_{Cs} & t_2' < t \le t_2\end{cases}$$

The intervals Δt_2 and $\Delta t'_2$ are given by,

$$\Delta t_2 = t_2 - t_1 = n_3 DT_s \tag{4.2b}$$

$$\Delta t_2' = t_2' - t_1 = n_1 \frac{V_I}{V_{Cs}}DT_s \tag{4.2b'}$$

Switching period 3 ($t_2 \le t < T_s$):

During this switching period, both the flyback transformer and the forward transformer have been completely de-energized, resulting in,

$$i_{Lm1}(t) = i_{Lm2}(t) = 0 \tag{4.3a}$$

$$V_{ds}(t) = V_{Cs}$$

The duration in this switching period is given by,

$$\Delta t_3 = T_s - DT_s - \Delta t_2 \tag{4.3b}$$

4.2.3.2 Conversion ratio and storage capacitor voltage

In order to describe the input/output characteristic, let us define the ac/dc conversion ratio as,

$$M \triangleq \frac{V_o}{V_{l,rms}} \tag{4.4}$$

To find the conversion ratio, let's use "approximated rms method". Since the average line current (in the sense of switching cycle) is a linear function of the line voltage, the maximum line current is given by,

$$I_{l,\max} = \frac{D^2 T_s}{2L_{m1}} V_{l,\max} \tag{4.5}$$

As the input power factor is nearly unity, the line current is almost sinusoidal. Therefore the *rms* line current can be easily calculated from Eq. (4.5),

$$I_{l,rms} = \frac{I_{l,\max}}{\sqrt{2}} = \frac{D^2 T_s}{2L_{m1}} V_{l,rms} \tag{4.6}$$

Then, considering input power equal to output power, we have,

$$I_{l,rms} V_{l,rms} = \frac{D^2 T_s}{2 L_{m1}} V_{l,rms}^2 = \frac{V_o^2}{R} \tag{4.7}$$

Solving Eq. (4.7) for $M = V_o/V_{l,rms}$, we obtain,

$$M = \frac{D}{\sqrt{2\tau_n}} \tag{4.8}$$

Where, the normalized load time constant, τn, is given by,

$$\tau_n = \frac{L_{m1}}{R T_s} \tag{4.9}$$

It should be indicated that the conversion ratio expressed in Eq. (4.8) is identical to the one derived by using "DC substitution method" [16].

From Eq. (4.8), a group of curves under different τ_n values can be obtained as shown in Fig. 4-4. The ac/dc conversion characteristic of this converter can be investigated by examining these curves. Furthermore, in steady-state, the output filter inductor must satisfy volt-second balance, which leads to,

$$V_o = D n_2 V_{Cs} \tag{4.10}$$

Therefore, the voltage across capacitor C_s can be found by solving Eqs. (4.8) and (4.10) to yield,

$$V_{Cs} = \frac{V_{l,rms}}{n_2 \sqrt{2\tau_n}} \tag{4.11}$$

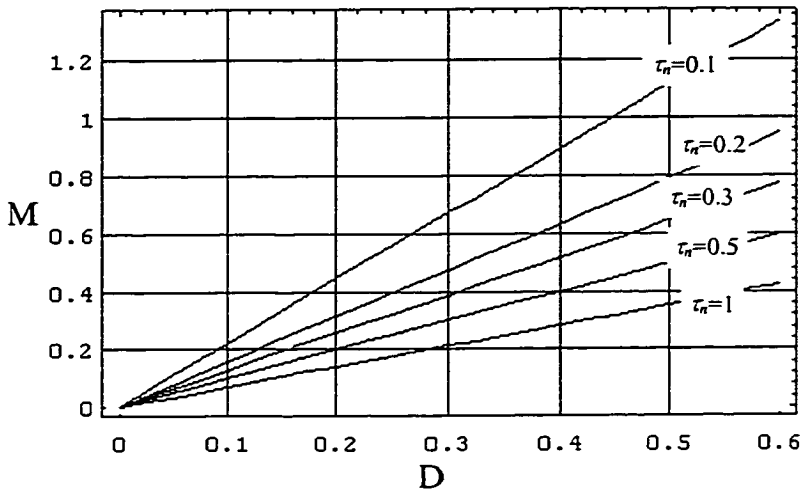


Figure 4-4 AC/DC conversion characteristic of the converter

Generally, in S^4 PFC converter we need a high drain-source switch voltage to demagnetize the input transformer (or inductor) when the switch turns off. Since the proposed converter imposes the primary side voltage of the forward transformer to the storage capacitor voltage, the capacitor voltage could be lower. As it can be seen, the storage capacitor voltage is a function of the line voltage, load and transformer turn ratio n_2. By properly designing the forward transformer, the capacitor voltage V_{Cs} can be kept at a lower level, decreasing the capacitor voltage rating in the practical design.

4.2.3.3 Operation constraints and design equations

Constraint 1: To ensure both the flyback transformer and the forward transformer are completely demagnetized during the interval when the power switch is off, the following volt-second balance equations hold for every switching cycle:

Volt-second balance for L_{m2},

$$V_{Cs} D T_s = \frac{1}{n_3} V_{Cs} (1 - D - k_2) T_s \tag{4.12}$$

where k_2 is duty ratio margin for magnetizing current i_{Lm2} as shown in Fig. 4-3.

Equation (4.12) results in the following design equation for transformer turn ratio n_3:

$$n_3 = \frac{(1 - D - k_2)}{D} \tag{4.13}$$

Because we must have $k_2 > 0$, hence,

$$n_3 < \frac{(1 - D_{max})}{D_{max}} \tag{4.14}$$

Volt-second balance for L_{m1},

$$V_l D T_s = \frac{1}{n_1} V_{Cs} (1 - D - k_1) T_s \tag{4.15}$$

where, k_1 is duty ratio margin for magnetizing current i_{Lm1} as shown in Fig. 4-3.

Therefore,

$$n_1 = \frac{V_{Cs}}{V_l} \frac{(1 - D - k_1)}{D} \tag{4.16}$$

When the peak line voltage occurs, according to Eq. (4.11), we have,

$$\frac{V_{Cs}}{V_{l,max}} = \frac{1}{2 n_2 \sqrt{\tau_n}} \tag{4.17}$$

Therefore, Eq. (4.16) becomes,

$$n_1 = \frac{(1 - D - k_1)}{2 D n_2 \sqrt{\tau_n}} \tag{4.18}$$

or,

$$n_1 < \frac{(1 - D_{\max})}{2 D_{\max} n_2 \sqrt{\tau_n}} \tag{4.19}$$

Constraint 2: In order to achieve a good power factor, the drain to source voltage $v_{ds}(t)$ of the power switch should be always larger than $\left(v_l(t) + \frac{1}{n_1} V_{Cs} \right)$ during demagnetizing T_1 to prevent D_1 from conducting, i.e.,

$$v_{ds}(t) = V_{Cs} + \frac{1}{n_3} V_{Cs} > V_{l,\max} + \frac{1}{n_1} V_{Cs} \tag{4.20}$$

Considering Eqs. (4.17) and (4.19), Eq. (4.20) yields the following design equation for transformer turn ratio n_2:

$$n_2 < \left(1 + \frac{1}{n_3} \right) \frac{1 - D_{\max}}{2\sqrt{\tau_n}} \tag{4.21}$$

Constraint 3:

When the line voltage is interrupted, the output power is supplied by the energy stored in the storage capacitor. According to Eq. (4.10), given the maximum duty ratio, the minimum capacitor voltage to hold a constant output voltage is given by,

$$V_{Cs,\min} = \frac{V_o}{n_2 D_{\max}} \tag{4.22}$$

Since the output energy is equal to the energy reduction in the storage capacitor during the hold-up time T_{hd} (there is no energy injected into C_s), we have

$$\frac{1}{2}C_s\left(\frac{V_o}{n_2 D_{nom}}\right)^2 - \frac{1}{2}C_s\left(\frac{V_o}{n_2 D_{\max}}\right)^2 = \frac{V_o^2}{R}T_{hd} \tag{4.23}$$

therefore,

$$C_s = \frac{2\, n_2^2 T_{hd}}{R\left(\frac{1}{D_{nom}^2} - \frac{1}{D_{\max}^2}\right)} \tag{4.24}$$

where, D_{nom} is nominal duty ratio.

4.2.3.4 Voltage and current stresses

Table 4-2 Voltage and current stresses on switch and diodes

	Voltage stress	Current stress
S	$\left(\frac{1}{n_3}+1\right)V_{Cs}$	$\left(\frac{\sqrt{2}V_{l,rms}}{L_{m1}}+\frac{V_{Cs}}{L_{m2}}\right)DT_s$
D_1	$\left(\frac{1}{n_3}+1\right)V_{Cs}$	$\frac{\sqrt{2}V_{l,rms}}{L_{m1}}DT_s$
D_2	$\sqrt{2}n_1V_{l,rms}+V_{Cs}$	$\frac{1}{n_1}\frac{\sqrt{2}V_{l,rms}}{L_{m1}}DT_s$
D_3	$(1+n_3)V_{Cs}$	$\frac{1}{n_3}\frac{V_{Cs}}{L_{m2}}DT_s$
D_4	$\frac{n_2}{n_3}V_{Cs}$	$\frac{V_o}{R}+(n_2V_{Cs}-V_o)\frac{DT_s}{2L_f}$
D_5	n_2V_{Cs}	$\frac{V_o}{R}+(n_2V_{Cs}-V_o)\frac{DT_s}{2L_f}$

Through steady-state analysis, the voltage and current stresses on each switch were found as listed in Table 4-2.

4.2.4 Design of The Proposed Single Switch Converter

In designing the proposed converter, the following design guideline can be considered:

a) Setting maximum duty ratio:

When the converter operates at minimum input voltage, the duty ratio will be close to its maximum value. Select the maximum duty ratio D_{max} and consider a proper margin.

b) Magnetizing inductance L_{m1} and L_{m2}:

Solving Eq. (4.8) for L_{m1} and considering minimum line voltage operation, we have the design equation for L_{m1}:

$$L_{m1} = \frac{R T_s}{2}\left(D_{\max} \frac{V_{l.rms,\min}}{V_o} \right)^2 \tag{4.25}$$

Since we have the switch current stress,

$$I_{ds,\max} = \left(\frac{\sqrt{2} V_{l.rms}}{L_{m1}} + \frac{V_{Cs}}{L_{m2}} \right) D T_s \tag{4.26}$$

in order for low current stress on the switches, magnetizing inductance L_{m2} should be as large as possible. The selection of L_{m2} should be made considering the trading-off

between current stresses and its physical dimension. To prevent the current stress, caused by $\frac{V_{Cs}}{L_{m2}}$, from being significantly large, we can set

$$L_{m2} \geq 10 L_{m1} \tag{4.27}$$

c) Transform ratios n_1, n_2 and n_3:

When D_{max} is specified, n_3 can be found by Eq. (4.14). Once D_{max} and n_3 are known, transformer turn ratio n_2 can be designed according to Eq. (4.21). It should be indicated that higher n_2 will help reducing the storage capacitor voltage but shorten the hold-up time. Equation (4.19) gives the design criteria for selecting n_1.

d) Selection of capacitor C_s:

Specified a hold-up time T_{hd}, the storage capacitance can be designed refereeing to Eq. (4.24). The voltage rating of the capacitor C_s can be set according to

$$V_{Cs,\max} = \frac{V_{l,rms,\max}}{n_2 \sqrt{2\tau_{n,\min}}} \tag{4.28}$$

e) Selection of output filter inductance L_f and capacitance C_f:

The filter components of L_f and C_f should be chosen in such a way that the corner frequency of the filter is much lower than the switching frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_f C_f}} << f_s \tag{4.29}$$

We set f_s 25~40% higher than f_0, by convention.

f) Selection of the power switch and the diodes:

Stresses on switch and diodes are given in Table 4-2. It should be noted that the maximum voltage stress for each component should be calculated under high-line, low-load operation. The maximum current stress on each component should be determined after comparing different line and load conditions. Based on the maximum voltage and maximum current stresses, proper switching devices can be chosen.

Specific design example:

Let us consider the following parameters for a specific example.

f_l=60Hz; $V_{l,rms}$=110V; $V_{l,rms,\min}$=88V; $V_{l,rms,\max}$=132V;

V_o=50V; R=50Ω; $R_{\max}$= 100Ω; T_{hd} = 20ms; f_s=50kHz.

The design procedure may be summarized as follows:

a) Setting maximum duty ratio:

$D_{\max}$ =0.45

b) Determine inductance L_{m1} and L_{m2}:

By calculating Eqs. (4.25) and (4.27), we obtain L_{m1} = 314μH and L_{m2} = 3.14mH. Therefore, τ_n = 0.315.

c) Determine transformer ratios n_1, n_2 and n_3:

By calculating Eqs. (4.14), (4.21) and (4.19), we set n_3 = 1, n_2 = 0.9 and n_1 = 1.

d) Selection of capacitor C_s:

The maximum storage capacitor voltage occurs when maximum line voltage and minimum load are applied. According to Eqs. (4.11) and (4.28), we have $V_{Cs,nom}$ =

154.2V and $V_{Cs,max}$=261.7V. From Eq. (4.8), the nominal duty ratio is D_{nom} = 0.36. The storage capacitance can be determined by calculating Eq. (4.24),

$$C_s = \frac{2\, n_2^2 T_{hd}}{R\left(\frac{1}{D_{nom}^2} - \frac{1}{D_{max}^2}\right)} = \frac{2\times 0.9^2 \times 20\times 10^{-3}}{50\times\left(\frac{1}{0.36^2} - \frac{1}{0.45^2}\right)} = 233.3\ \mu F$$

Let's chose C_s = 330μF/400V.

e) Selection of output filter inductance L_f and capacitance C_f:

Chose L_f = 1mH and C_f = 220μF/63V.

$$\left(f_0 = \frac{1}{2\pi\sqrt{L_f C_f}} = \frac{1}{2\pi\sqrt{1\times 10^{-3} \times 220\times 10^{-6}}} = 339Hz << 50\text{kHz} \right)$$

f) Stresses on switches:

By calculating Table 4-2, the voltage and current stresses under various line and load conditions are listed in Table 4-3. According to the maximum voltage stress and current stress for each component and considering switching speed, we choose the switch, IXTH20N60, and the diodes: D_1: MUR3080; D_2: MUR850; D_3: MUR160; D_4, D_5: MUR440.

Table 4-3 Theoretical switch and diodes voltage and current stresses

Device	Voltage Stress(V)	Current Stress(A)			
	$V_{l,rms}$=132V R = 100Ω	$V_{l,rms}$=88V R = 100Ω	$V_{l,rms}$=88V R = 50Ω	$V_{l,rms}$=132V R = 100Ω	$V_{l,rms}$=132V R = 50Ω
S	523.4	2.87	4.40	2.87	3.92
D_1	523.4	2.52	3.57	2.52	3.57
D_2	448.4	2.52	3.57	2.52	3.57
D_3	523.4	0.35	0.35	0.35	0.35
D_4	235.5	0.84	1.27	2.07	1.35
D_5	235.5	0.84	1.27	2.07	1.35

4.2.5 Simulation and Experimental Results

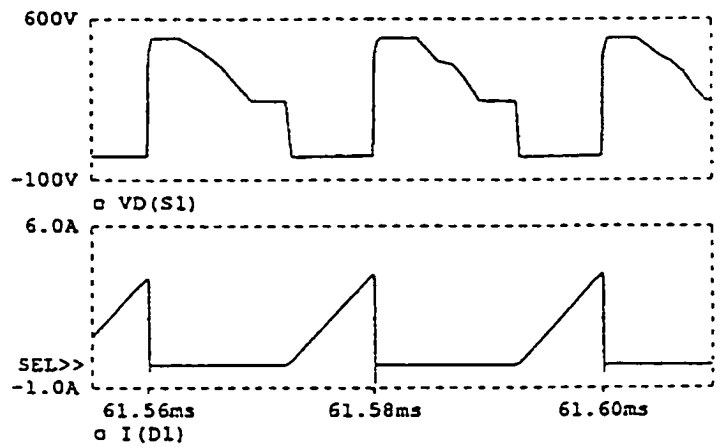
By using the above designed circuit parameters, the closed-loop PSPICE simulation of the proposed single-switch converter schematic was done and the simulation results are shown in Fig. 4-5. An experimental prototype of the converter was built up in the laboratory with the same circuit parameters. The flyback transformer uses QP43220 core (with air gap) and the forward transformer uses ETD-PST39 core. Pulse-width-modulation chip SG3525 was used to achieve closed-loop control. The experimental waveforms of filtered line current, switch voltage and current through diode D_1, shown in Fig. 4-6, were recorded by using hp54542A oscilloscope. It should be pointed out that at different line phase position, the switch waveforms change slightly. The waveforms in Fig. 4-6(a) were recorded at the peak line voltage.

It is clear that both the simulated and the experimental waveforms are in a good agreement. The line current waveform is almost sinusoidal and in phase with the line voltage, proving that a good power factor was achieved by this converter topology.

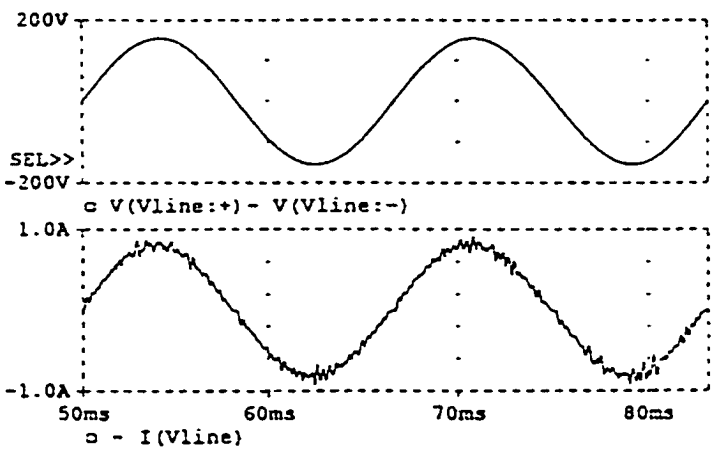
Measured power factor and efficiency under different load conditions are given in Fig. 4-7. It can be seen that for full load, the proposed converter can maintain 99% power factor with the line voltage changing from 85VAC to 135VAC. At the nominal load, higher than 80% overall conversion efficiency (including line filter and a negative temperature start resistor) was achieved. Since the power supply was designed for the nominal operation under 110VAC input/1A output, at 1.5A output, when line voltage decreases below 100V, the 50V output cannot be maintained (due to duty cycle limit). At

110V line input, transient response waveforms corresponding to load changing between 25% and full load were recorded.

Figure 4-8 shows output voltage transient response and Fig. 4-9 shows line current transient response when load changing. The reset time from 25% load to full load is around 50ms and the reset time from full load to 25% load is about 100ms. However, the reset time could be improved by optimizing its control circuit.

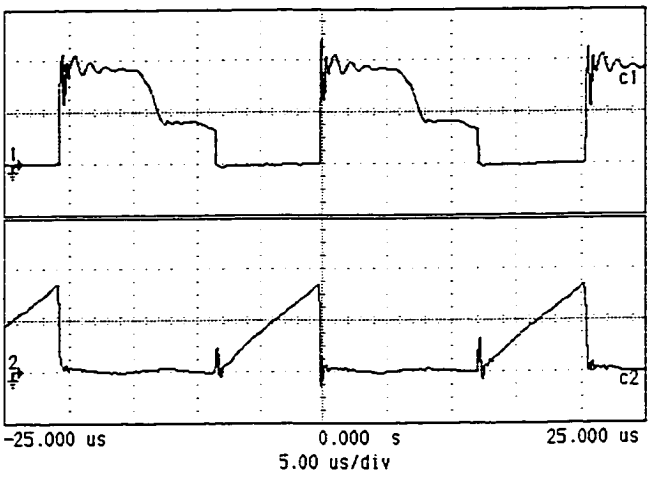


(a)

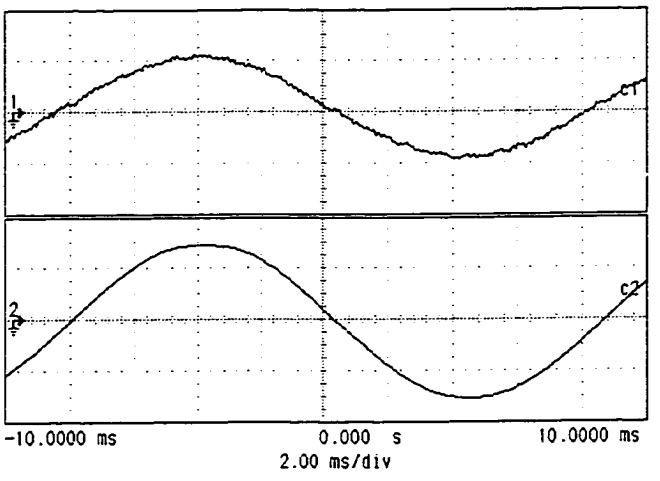


(b)

Figure 4-5 Simulation waveforms of the proposed converter: (a) voltage at the switch and current through D_1; (b) line voltage (top) and filtered input current (bottom)

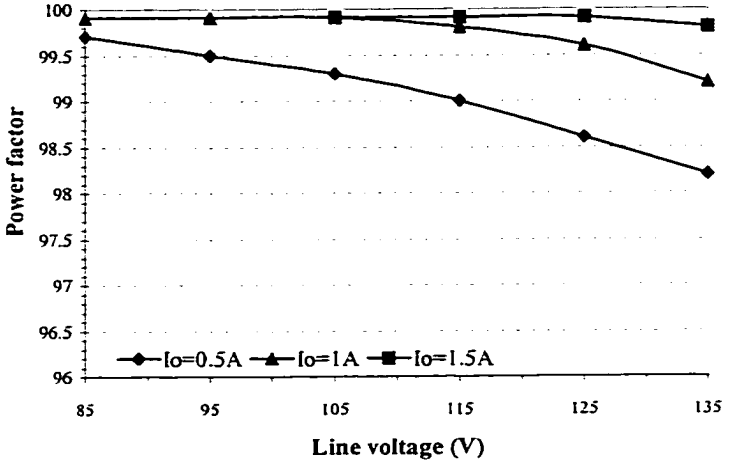


(a)

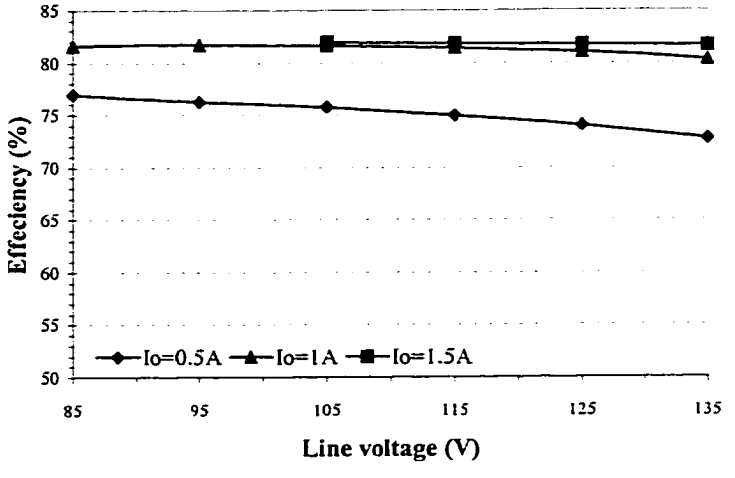


(b)

Figure 4-6 Experimental waveforms under 110VAC input and 1A output of the proposed converter: (a) voltage at the switch (top, 200V/div.) and current through D_1 (bottom, 2A/div.)(Waveforms were recorded at peak line voltage); (b) filtered line current (top, 1A/div.) and line voltage (bottom, 100V/div.)

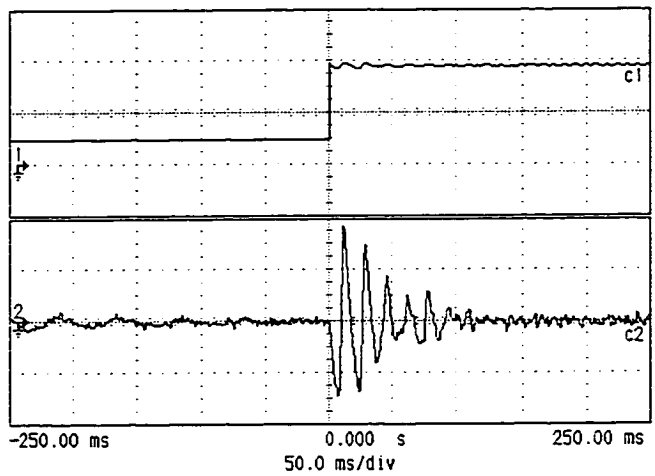


(a)

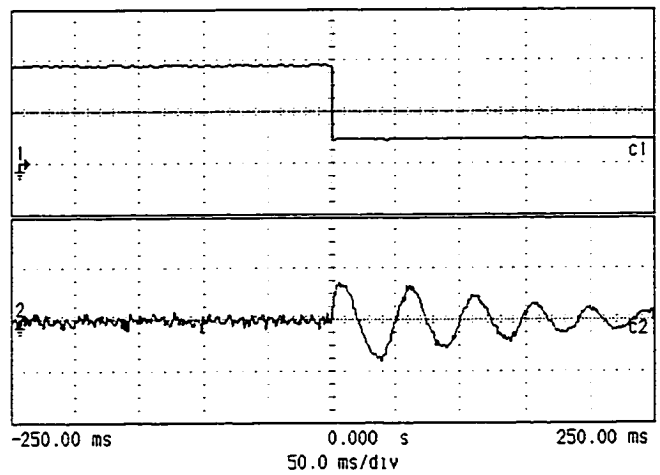


(b)

Figure 4-7 Experimental efficiency and input power factor: (a) input power factor; (b) efficiency

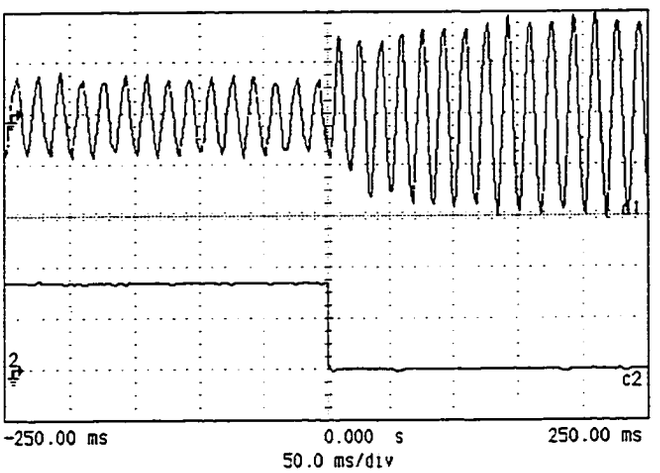


(a)

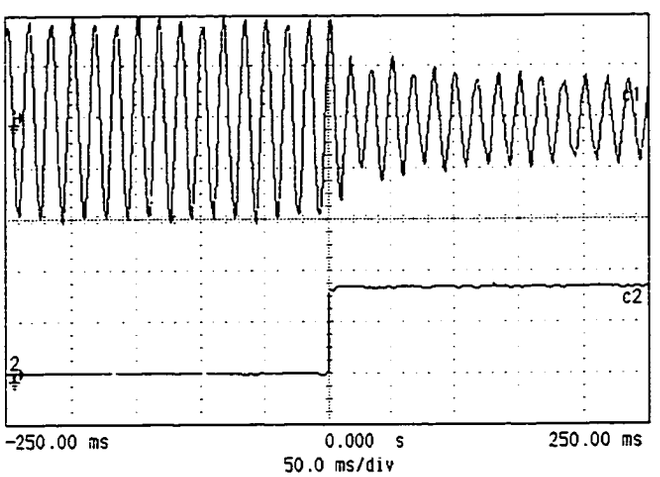


(b)

Figure 4-8 Experimental output voltage transient response at 110VAC line input: (a) 25% load switching to full load (top: load current, 0.5A/div.; bottom: output voltage, 1V/div.); (b) full load switching to 25% load (top: load current, 0.5A/div.; bottom: output voltage, 1V/div.)



(a)



(b)

Figure 4-9 Experimental line current transient response at 110VAC line input: (a) 25% load switching to full load (top: line current, 0.5A/div.; bottom: load change trigger signal); (b) full load switching to 25% load (top: line current, 0.5A/div.; bottom: load change trigger signal)

4.3 A NEW DCM-DCM-S^4 CONVERTER WITH TWO STORAGE CAPACITORS

The remarkable advantages achieved by the converter topology proposed in Section 4.2 are its perfect input power factor and lower storage capacitor voltage. However, the following drawbacks still exist:

a) The unavoidable leakage inductance of the power transformer produces high voltage spike at switching instances, resulting in decreased efficiency.

b) Because it is a DCM-CCM type, the bulk storage capacitor voltage is a function of the load, resulting in difficulty in design it for universal input application.

c) Two transformers are used, which in turn results in increased cost.

d) The input stage is a flyback circuit, which limits the converter power level to low.

A new AC/DC converter will be presented in this section, aimed at overcoming the above difficulties. The proposed S^4 converter utilizes a DCM boost circuit as an input stage to perform PFC and a forward circuit as an output stage to provide electrical isolation. Two storage capacitors have been employed to enhance the PFC capability of the boost circuit and to relieve the voltage spike produced by the power transformer. The voltages across the storage capacitors are kept at lower levels. Theoretical analysis and experimental results show that the converter has enough line regulation capability to be applied to universal input.

4.3.1 Proposed Converter and Its Circuit Operation

The proposed AC/DC converter is shown in Fig. 4-10. The input circuit is a boost circuit (formed by choke inductor L, diode D_1 and switch S). The switched-capacitor network consists of capacitors C_{s1} and C_{s2} and diode D_2, serving as a load to the input

circuit, and as a source to the output forward circuit (formed by transformer Tr and diode D_3). The two primary windings of the forward transformer is designed with the same turn ratio referring to the secondary winding (1:1:*n*). Inductances L_1 and L_2 ($L_1 = L_2$) are the leakage inductances of the forward transformer. It can be shown that, in steady-state, the proposed converter has four switching periods during one switching cycle. Table 4-4 shows the four switching periods of operation and conducting devices during their corresponding time intervals. The equivalent circuits of the four operation topologies are shown in Fig. 4-11 and converter key waveforms are shown in Fig. 4-12.

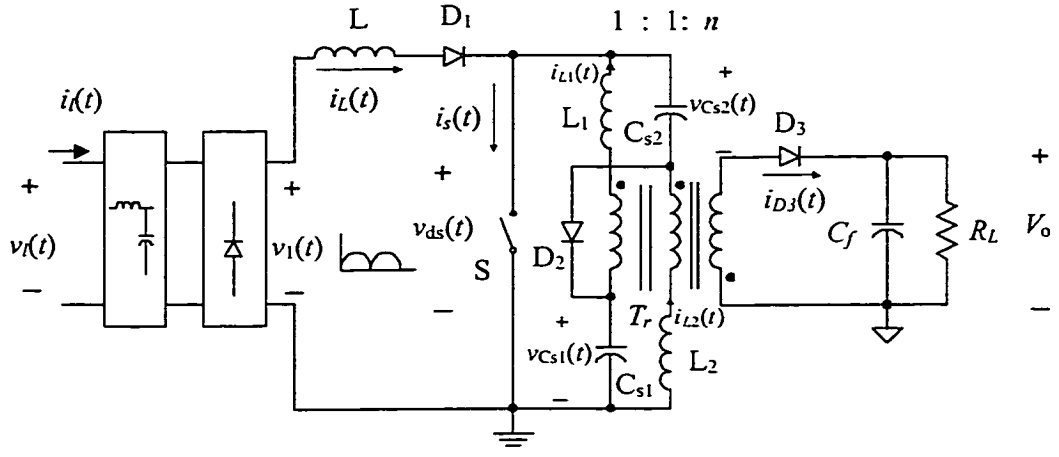


Figure 4-10 Basic circuit schematic of the proposed two-storage capacitor converter

Table 4-4 Switching periods of operation

Period	Time interval	Conducting device			
		S	D_1	D_2	D_3
P1	$t_0 \le t < t_1$	×	×		×
P2	$t_1 \le t < t_2$		×	×	×
P3	$t_2 \le t < t_3$		×	×	
P4	$t_3 \le t < t_0 + T_s$				

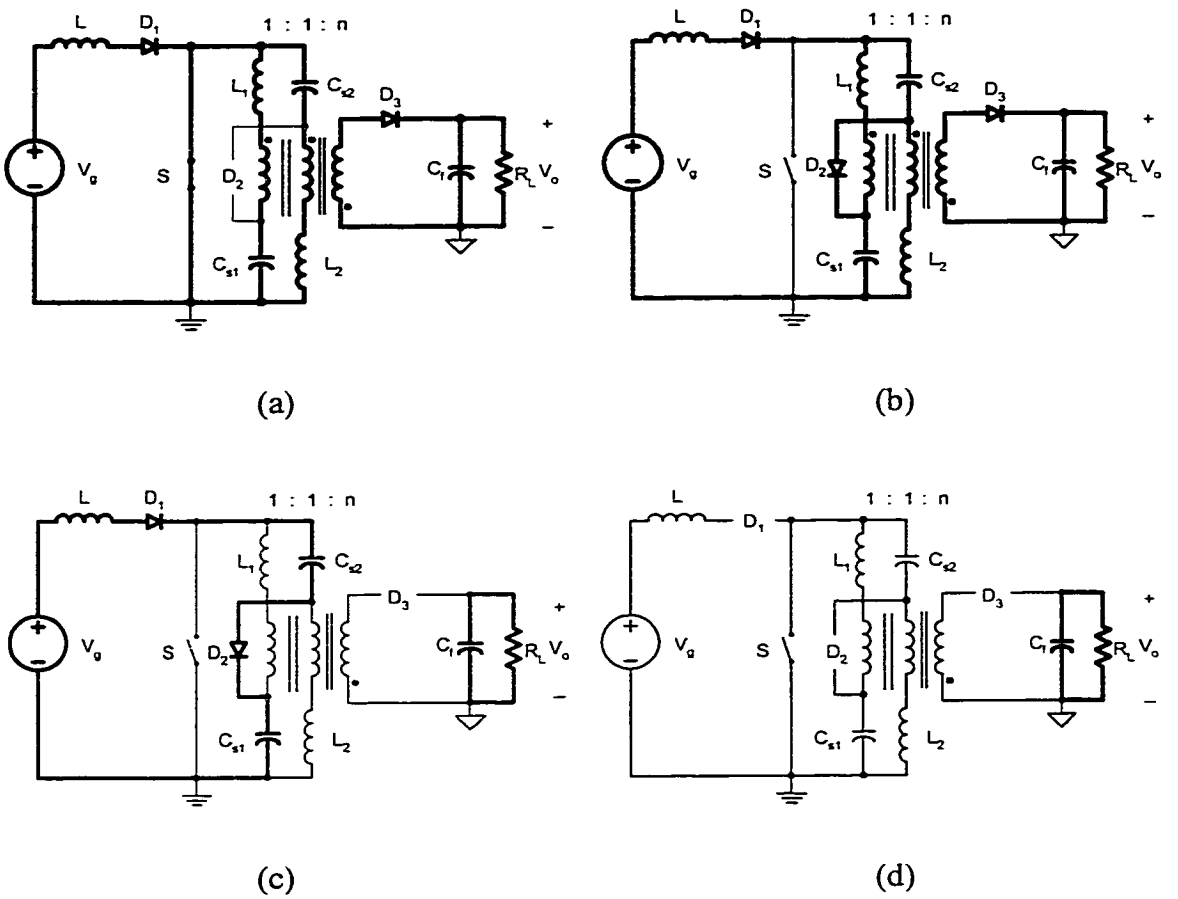


Figure 4-11 Equivalent topologies for the four switching periods: (a) P1($t_0 \le t < t_1$); (b) P2($t_1 \le t < t_2$); (c) P3($t_2 \le t < t_3$); (d) P4($t_3 \le t < t_0 + T_s$)

Notice that in one switching cycle, the line voltage can be considered as a constant voltage, represented by V_g in the equivalent circuits. Capacitors C_{s1} and C_{s2} are designed to be large and equal. Hence, in the steady-state analysis, each capacitor voltage is approximated by a dc source $V_{Cs1} = V_{Cs2} = V_{Cs}$. The four switching periods are discussed as follows:

Switching period 1 begins at $t=t_0$ when the power switch is turned ON. With diode D_1 conducting, the source voltage is applied to the input choke inductor L, causing the current through the inductor increasing linearly. During this period, energy is

transferring from the source to the choke inductor. On the other hand, diode D_2 is blocked by the two capacitor voltages since the positive end of C_{s2} is grounded by the power switch. Thus, the diode splits the primary sides of the forward transformer into two symmetrical branches with one storage capacitor in each. These capacitors (previously charged) feed the primary sides of the forward transformer individually, which is equivalent to using capacitance C_{s1}+C_{s2} to feed the transformer with voltage V_{Cs}, resulting in the energy stored in the two capacitors being transferred to load during this period. This switching period ends at $t = t_1$ when the power switch is turned OFF as shown in Fig. 4-11. During P1, we have,

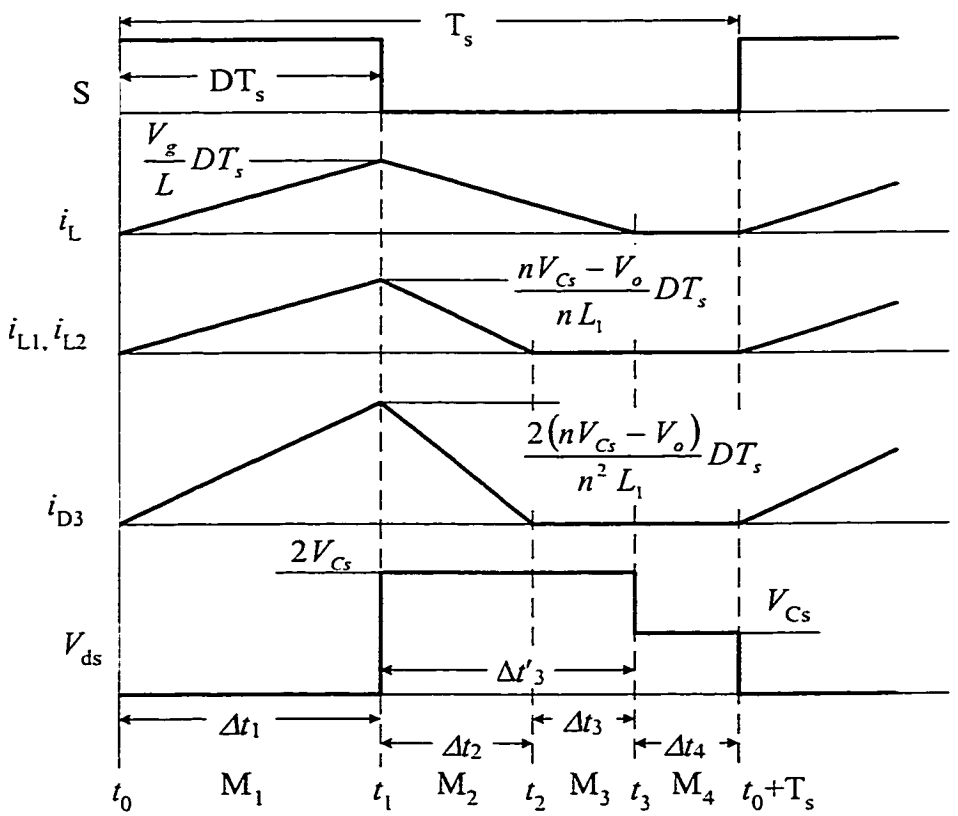


Figure 4-12 Theoretical key waveforms of the proposed converter

$$i_L(t)=\frac{V_g}{L}t\ ;$$

$$i_{L1}(t)=i_{L2}(t)=\frac{nV_{Cs}-V_o}{nL_1}t\ ;$$

$$i_{D3}(t)=\frac{2(nV_{Cs}-V_o)}{n^2L_1}t \qquad (4.30a)$$

$$v_{ds}(t)=0\ .$$

The duration of this stage is

$$\Delta t_1 = DT_s. \qquad (4.30b)$$

Where, $D=\frac{t_1-t_0}{T_s}$ is the duty cycle.

During Switching period 2, the power switch is turned OFF at $t = t_1$ and diode D_2 is turned ON due to a current $i_L + 2\ i_{L1}$ flowing through it. The equivalent topology is shown in Fig. 4-11(b). Under the constraint of KCL, both the storage capacitors, C_{s1} and C_{s2}, are being charged by current $i_L + i_{L1}$ during this operation period. With the inductor current i_L decreasing linearly, magnetic energy stored in the choke is being converted into electric energy and being stored into the storage capacitors. Thus the energy loss of the storage capacitors during P1 is being recovered. At the same time, the forward transformer is being demagnetized through its secondary windings, and its magnetizing energy is fed back to capacitors C_{s1} and C_{s2}. It should be noticed that seen by the output of the boost circuit, $2V_{Cs}$ presents since the two bulk capacitors are charging in serial. Compared with other types of AC/DC PFC converters with the same amount of energy

stored in bulk capacitance C_{s1}+C_{s2}, the proposed converter has a higher voltage to de-energize the choke inductor, resulting in better power factor and regulation capabilities. When the forward transformer is completely demagnetized, i.e. i_{L1} and i_{L2} become zero, the converter's operation enters Switching period 3. Using Fig. 4-11(b), the following expressions are obtained:

$$i_L(t) = \frac{V_g}{L} DT_s - \frac{2V_{Cs} - V_g}{L}(t - DT_s);$$

$$i_{L1}(t) = i_{L2}(t) = \frac{nV_{Cs} - V_o}{nL_1} DT_s - \frac{nV_{Cs} + V_o}{nL_1}(t - DT_s);$$

$$i_{D3}(t) = \frac{2}{n} i_{L1}(t); \qquad (4.31a)$$

$$v_{ds}(t) = 2V_{Cs}.$$

The time interval Δt_2 is given by:

$$\Delta t_2 = t_2 - t_1 = \frac{nV_{Cs} - V_o}{nV_{Cs} + V_o} DT_s. \qquad (4.31b)$$

In Switching period 3, the choke inductor current, I_L, continues to decrease linearly. Owing to the existence of diode D_3, the primaries of the transformer present very high impedance (Fig. 4-11(c)) with the currents through the windings can be negligible. This period ends when the choke inductor current reaches zero. The key voltages and currents in this duration can be described as followed.

$$i_L(t) = \frac{V_g}{L} DT_s - \frac{2V_{Cs} - V_g}{L}(t - DT_s);$$

$$i_{L1}(t) = i_{L2}(t) = i_{D3}(t) = 0; \tag{4.32a}$$

$$v_{ds}(t) = 2V_{Cs}.$$

The time intervals are:

$$\Delta t_3 = \Delta t_3' - \Delta t_2, \tag{4.32b}$$

where,

$$\Delta t_3' = \frac{V_g}{2V_{Cs} - V_g} DT_s. \tag{4.32c}$$

The Switching period 4 between t_3 and t_0+T_s is known as a free-wheeling stage, which is used for regulation purpose. Since the proposed converter has a shorter choke inductor discharging period, a wider free wheeling margin is available for the duty ratio variation to regulate the converter. When the power switch is turned ON again at $t = T_s + t_0$, the converter operation goes into the next cycle. During this period, we have

$$i_L(t) = i_{L1}(t) = i_{L2}(t) = i_{D3}(t) = 0; \tag{4.33a}$$

$$v_{ds}(t) = V_{Cs}.$$

The time interval is given by,

$$\Delta t_4 = T_s - DT_s - \Delta t_2 - \Delta t_3. \tag{4.34b}$$

4.3.2 Steady-State Analysis

4.3.2.1 AC/DC conversion ratio

In order to find out the conversion ratio, let's first find the voltage across the storage capacitor. In steady operation, we have $I_{D3.ave}=\frac{V_o}{R_L}$, where $I_{D3.ave}$ is the average current through diode D_3, which can be determined from the waveform of $I_{D3}(t)$ (Fig. 4-12). By solving the equation for $M_1=\frac{V_{Cs}}{V_o}$, we obtain

$$M_1=\frac{1}{2}\left[\frac{1}{n}+\frac{k n \tau_n}{2D^2}+\sqrt{\left(\frac{1}{n}+\frac{k n \tau_n}{2D^2}\right)^2+\frac{2k\tau_n}{D^2}}\right]. \tag{4.35}$$

Here, D is average duty ratio in a line cycle, $k=\frac{L_1}{L}=\frac{L_2}{L}$ is inductance ratio and $\tau_n=\frac{\tau}{T_s}$ is normalized load, where $\tau=\frac{L}{R_L}$.

It can be shown from Fig. 4-12 that the filtered line current can be expressed as,

$$i_l(t)=\frac{D^2T_s}{L}\frac{V_{Cs}\ v_l(t)}{2V_{Cs}-v_l(t)}. \tag{4.36}$$

Therefore the maximum line current is given by,

$$I_{l.\max}=\frac{D^2T_s}{L}\frac{V_{Cs}\ V_{l.\max}}{2V_{Cs}-V_{l.\max}}. \tag{4.37}$$

Since we have nearly unity power factor, the line current is almost sinusoidal. So, the *rms* value of line current can be approximated by,

$$I_{l\_rms} = \frac{D^2 T_s}{\sqrt{2}L} \frac{V_{Cs}\, V_{l\_rms}}{\sqrt{2}V_{Cs} - V_{l\_rms}}. \tag{4.38}$$

Based on the assumption of lossless converter, we have $P_{in,ave} = P_{out,ave}$, i.e. $V_{l\_rms} \cdot I_{l\_rms} = \frac{V_o^2}{R_L}$. Using this relation in Eq. (4.38) for M, we obtain,

$$M = \frac{1}{2\sqrt{2}} \left(\frac{1}{M_1} + \sqrt{\frac{1}{M_1^2} + 4\frac{D^2}{\tau_n}} \right) \tag{4.39}$$

Here, M_1 is determined by Eq. (4.35).

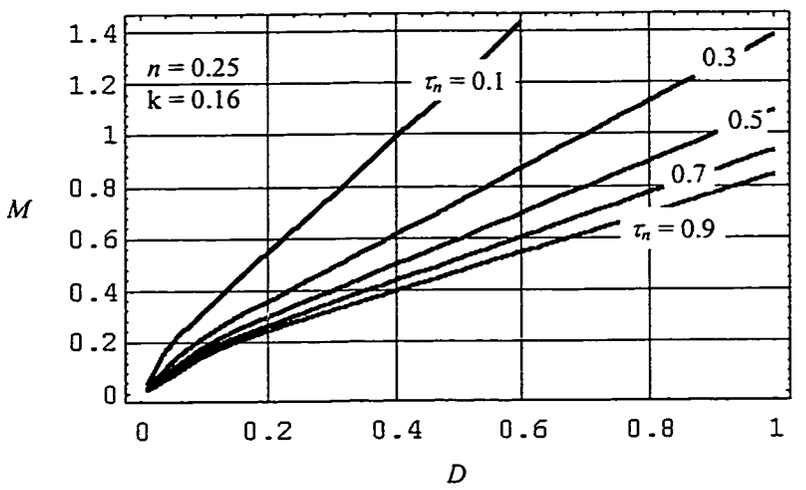


Figure 4-13 AC/DC conversion characteristics of the converter

From Eqs. (4.35) and (4.39), a group of curves showing M vs. D under different τ_n's, can be obtained as shown in Fig. 4-13. The AC/DC conversion characteristics of this converter can be investigated by examining these curves. It can be seen that for a certain load range, AC/DC conversion ratio can be adjusted by changing the duty ratio of its driving signal. We may note that at light load (low τ_n), the proposed converter can operate as both boost and buck converter.

In order to investigate the bulk capacitor voltage variation in terms of line voltage and load, let's solve for M_1 in Eqs. (4.35) and (4.39) to yield,

$$M_1 = \frac{1}{2a_1}\left[-b_1 + \sqrt{b_1^2 - 4a_1c_1}\right], \tag{4.40}$$

where,

$$a_1 = 2nM^2$$

$$b_1 = -\left(\sqrt{2}nM + 2M^2 + \frac{n^2k}{2}\right)$$

$$c_1 = \sqrt{2}M - \frac{nk}{2}$$

By plotting Eq. (4.40), a graph showing M_1 vs. M is given in Fig. 4-14 for n = 0.25 and $k = 0.16$. The bulk capacitor voltage can be determined by $V_{Cs} = M_1 V_o$. It should be pointed out that the voltage ratio M_1 is independent on the load change. Moreover, when conversion ratio M higher than 0.2, the capacitor voltage is almost kept at low level ($V_{Cs} \approx 1/n\ V_o$). Such property of the proposed converter is especially favorable for universal application.

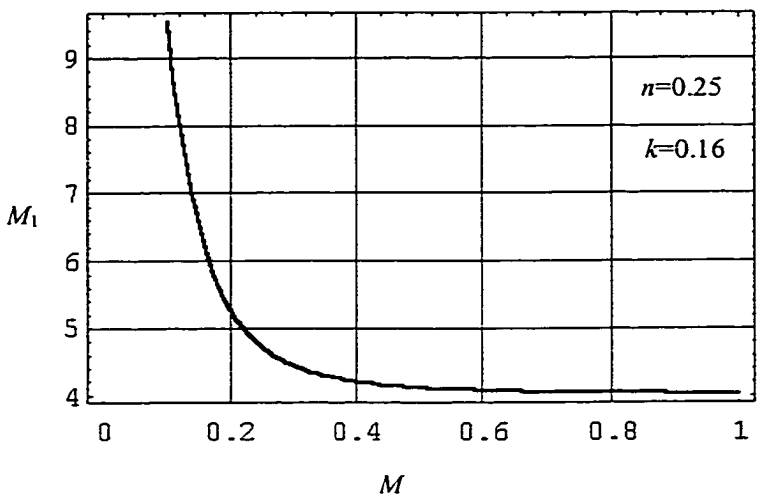


Figure 4-14 Storage capacitor voltage of the converter ($V_{Cs} = M_1 V_o$)

4.3.2.2 Maximum duty ratio and regulation capabilities

According to the key waveforms shown in Fig. 4-12, inequality $\Delta t_1 + \Delta t'_3 \leq T_s$ must be satisfied in the converter operation. Substituting Eqs. (4.30b) and (4.32c) into the above inequality, we obtain

$$D \leq 1 - \frac{1}{\sqrt{2}MM_1}, \tag{4.41}$$

with the maximum duty ratio being given by

$$D_{max} = 1 - \frac{1}{\sqrt{2}MM_1}. \tag{4.42}$$

The maximum duty ratio D_{max} gives an upper limit of the converter duty ratio. In practical design, the nominal operation duty ratio D must be set with enough margin so

that the converter has certain regulation capabilities. It should be noticed from Eq. (4.40) that the voltage ratio M_1 is not a function of load τ_n, therefore the maximum duty ratio is only determined by the conversion ratio M and the converter parameters k and n. Figure 4-15 gives a plot of maximum duty ratio in term of transformer ratio n under different conversion ratios.

In order to study the line and load regulation capabilities, we express the duty ratio in terms of M and τ_n as follows,

$$D = \sqrt{\frac{M\ \tau_n}{2a_2}\left(-b_2+\sqrt{b_2^2-4a_2\,c_2}\right)} \tag{4.43}$$

where,

$$a_2 = 2\sqrt{2}\,M - kn\,;$$

$$b_2 = -4\sqrt{2}M^2 + 4n(k+1)M + \sqrt{2}\,kn^2\,;$$

$$c_2 = -2knM\left(2M+\sqrt{2}\,n\right).$$

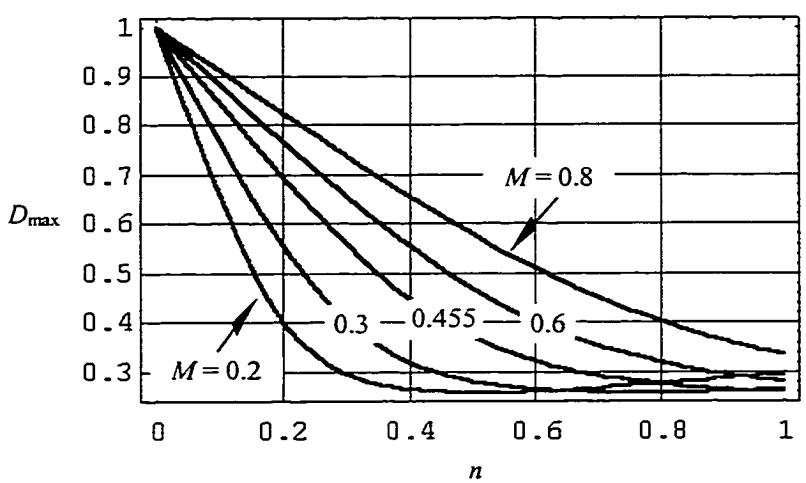


Figure 4-15 Maximum duty cycle vs. transformer ratio under different voltage gain

From Eqs. (4.42) and (4.43), characteristic curves for D vs. M under different loads and D vs. τ_n under different conversion ratios are given in Figs. 4-16 and 4-17, respectively. These figures can be used to examine the regulation capabilities of the converter.

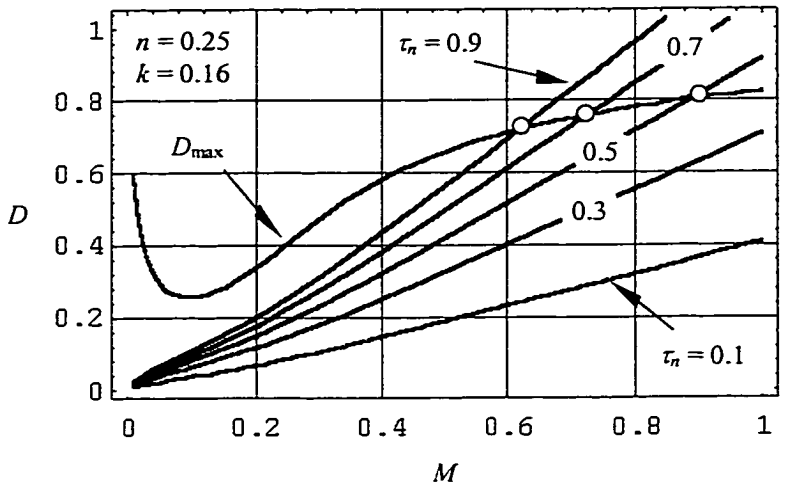


Figure 4-16 Line regulation capability of the converter

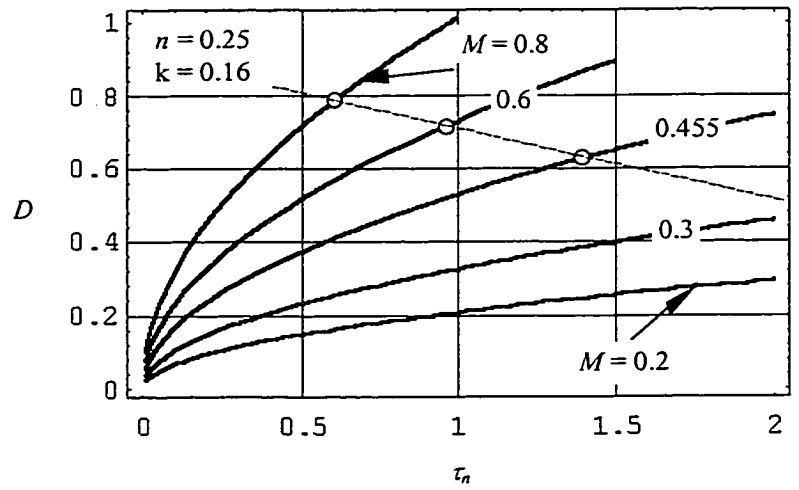


Figure 4-17 Load regulation capability of the converter

Referring to Fig. 4-16, we can investigate the line regulation capability of the proposed AC/DC converter. For example, a converter with V_o = 50V output dc voltage is designed with $n = 0.25$ and $k = 0.16$. At load $\tau_n = 0.5$, the gain M can change between 0.1 to 0.82, which means theoretically, the output can be kept at 50V while the input voltage is changing within the range of 61V ~ 500V. The duty ratio range is between 0.08 to its maximum 0.8. In short, a ±20% variation in the line voltage requires the duty ratio change by 58% to maintain constant output. Similarly, the load regulation capability can be examined by referring to Fig. 4-17. For the above converter example, if M = 0.455 ($V_{l,rms}$=110V, V_o = 50V), theoretically, τ_n can vary between 0.1 to 1.3 with the output voltage being kept at 50V. For ±50% load change, to maintain a constant output, a duty ratio change of 66% is required.

4.3.2.3 Voltage and current stresses and other design equations

Through steady-state analysis, the voltage and current stresses on each switch were found as listed in Table 4-5.

Table 4-5 Voltage and current stresses on switch and diodes

Device	Voltage Stress	Current Stress
S	$2V_{cs}$	$\left(\frac{\sqrt{2}V_{l,rms}}{L}+2\frac{nV_{Cs}-V_o}{nL_1}\right)DT_S$
D_1	V_{cs}	$\frac{\sqrt{2}V_{l,rms}}{L}DT_S$
D_2	$2V_{cs}$	$\left(\frac{\sqrt{2}V_{l,rms}}{L}+2\frac{nV_{Cs}-V_o}{nL_1}\right)DT_S$
D_3	V_o+nV_{cs}	$2\frac{nV_{Cs}-V_o}{n^2L_1}DT_S$

By integrating the current through the output capacitor C_f, the output voltage ripple is given by,

$$\frac{\Delta V_o}{V_o} = \frac{\left(2DM_1 n - 2D - n^2 k \tau_n\right)^2 M_1}{2n L_1 C_f f_s^2 \left(M_1^2 n^2 - 1\right)}. \tag{4.44}$$

The critical choke inductance was found as

$$L_{crit} = \frac{D R_L}{2 f_s M^2}. \tag{4.45}$$

To ensure the converter operating in DCM, the choke inductor must be selected with a value smaller than the critical inductance.

4.3.3 Design Guideline of The Proposed Converter

To design a proposed converter with specifications M, nominal load R_L, output voltage ripple ΔV_o and switching frequency f_s, the following design principles can be applied:

a) Selection of transformer turn ratio n and inductance ratio k:

Selection of transformer turn ratio should be based on the trade off between regulation capabilities and voltage stresses on the devices. According to Eq. (4.35), a low n will result in high voltage across the storage capacitors. Since all the voltage stresses on the switches (S and D_1~D_3) depend on V_{Cs}, we prefer a higher transformer turn ratio. However, a higher n causes the maximum duty cycle to be lower, reducing both the line and load regulation capabilities. Hence, a lower transformer turn ratio is desired in this case. In practical design, a proper value of n should be chosen so that it gives enough regulation capabilities and lower voltage stresses as well. From Table 4-5, it seems that to

relieve high current stresses, we should increase the inductance L_1. But the effect will be very weak because the storage capacitor voltage increases with the increasing of $k = L_1/L$ as it can be seen in Eq. (4.35). In practical design, we prefer a small value of k so that the voltage stresses can be reduced.

b) Setting of nominal duty ratio and normalized load:

When n and k have been chosen, Fig. 4-15 can be generated. The nominal duty ratio can be approximated by

$$D = 0.1 + 0.5\ (D_{\max} - 0.1). \tag{4.46}$$

In the above equation, we assumed that the minimum duty ratio is 0.1. In Fig. 4-17, corresponding to the nominal duty ratio, normalized load τ_n can be found.

c) Selection of choke inductance:

For given τ_n, the value of choke inductance is given by

$$L = \tau_n R_L T_s \tag{4.47}$$

d) Selection of L_1 and L_2:

For a given k, $L_1 = L_2$ can be selected according to

$$L_1 = L_2 = k L. \tag{4.48}$$

e) Selection of the storage capacitance:

To design the storage capacitors, let's consider that due to the missing of one line cycle, an average voltage drop of $k_c V_{Cs}$ on the storage capacitor is allowed, then by analysis we have

$$C_S \geq \frac{T_l}{k_c(2-k_c)R_L M_1^2}, \tag{4.49}$$

where, T_l is the line period. The voltage stress on the storage capacitor is calculated by,

$$V_{Cs} = M_1 V_o, \tag{4.50}$$

where M_1 can be determined by Eq. (4.35). Based on Eqs. (4.49) and (4.50), the storage capacitors can be selected.

f) Selection of output capacitor:

From Eq. (4.44), we get

$$C_f = \frac{\left(2DM_1 n - 2D - n^2 k \tau_n\right)^2 M_1}{2nL_1 f_s^2 \left(M_1^2 n^2 - 1\right)} \frac{1}{\Delta V_o / V_o}. \tag{4.51}$$

For a given design with specified ripple factor, we can find the output capacitance. Together with the output voltage, an output capacitor can be chosen.

g) Selection of switches:

The selection of switches should be based on their voltage and current stresses, which can be calculated according to the equations listed in Table 4-5.

Design example:

Let us consider the following specifications as a design example:

Nominal input voltage:	$V_{l,rms}$= 110V/60Hz;
Input voltage range (rms):	$V_{l,rms}$= 85V ~ 250V;
Output voltage:	V_o=50V ± 2.5%;
Nominal load current:	I_o = 1A;
Switching frequency:	f_s = 50KHz.

For a universal input converter, the design should be based on low line operation ($V_{l,rms}$= 110V). Following the above design guidelines, we obtain the converter parameters as follows.

a) Transformer turn ratio n and inductance ratio k:

To compromise between voltage stress and regulation capabilities, let's select n = 0.25 and k = 0.16, which give a maximum duty ratio of 0.65 and $V_{Cs} \approx$ 200V at M = 0.455.

b) Nominal duty ratio D:

The duty ratio at nominal input is determined by Eq. (4.46):

$$D = 0.1 + 0.5\,(D_{\max} - 0.1) = 0.1 + 0.5\,(0.65 - 0.1) \approx 0.38.$$

From Fig. 4-17, using $M = 0.455$ and $D = 0.38$, we obtain $\tau_n = 0.5$.

c) Choke inductance L:

The choke inductance is hence determined by

$$L = \tau_n R_L T_S = 0.5 \times 50 \times 2 \times 10^{-5} = 500\ \mu\text{H}$$

d) Leakage inductances L_1 and L_2:

We can select L_1 and L_2 as

$$L_1 = L_2 = k\,L = 0.16 \times 500 = 80\ \mu\text{H}$$

e) Bulk capacitor C_s:

Suppose that due to one line cycle missing, an average voltage drop of $0.1V_{Cs}$ on the storage capacitor is allowed, i.e. k_c = 0.1. From Eqs. (4.49) and (4.50), we have $C_s \geq$ 102μF, and V_{Cs} = 207V.

Select C_s = 110μF/250V.

f) Output filter capacitor C_f:

By calculating Eq. (4.51), the output capacitance is $C_f = 5.423\mu F$.

We select $C_f = 10\ \mu F@100V$.

g) Switching devices S, D_1, D_2 and D_3:

From Table 4-5, we calculate the theoretical diode and switch voltage and current stresses as listed in Table 4-4. Considering switching speed, we choose:

S: BUZ91A; D_1, D_2 and D_3: MUR850.

Table 4-6 Theoretical switch and diodes voltage and current stresses

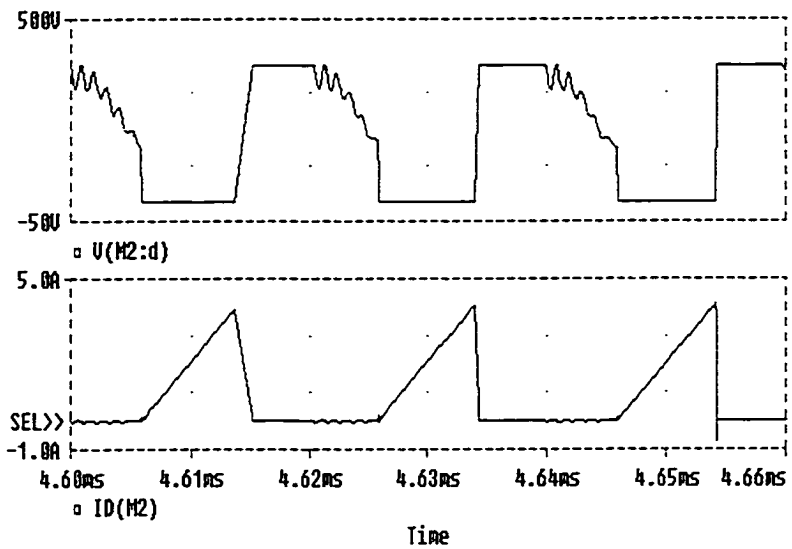
Device	Voltage Stress (V)		Current Stress (A)		
	$V_{l,rms}$=110V	$V_{l,rms}$=264V	$V_{l,rms}$=85V	$V_{l,rms}$=110V	$V_{l,rms}$=264V
S	414	504	3.12	3.69	5.32
D_1	207	252	1.92	2.36	1.94
D_2	414	504	3.12	3.69	5.32
D_3	101.75	113	4.8	5.32	13.52

4.3.4 Simulation and Experimental Results

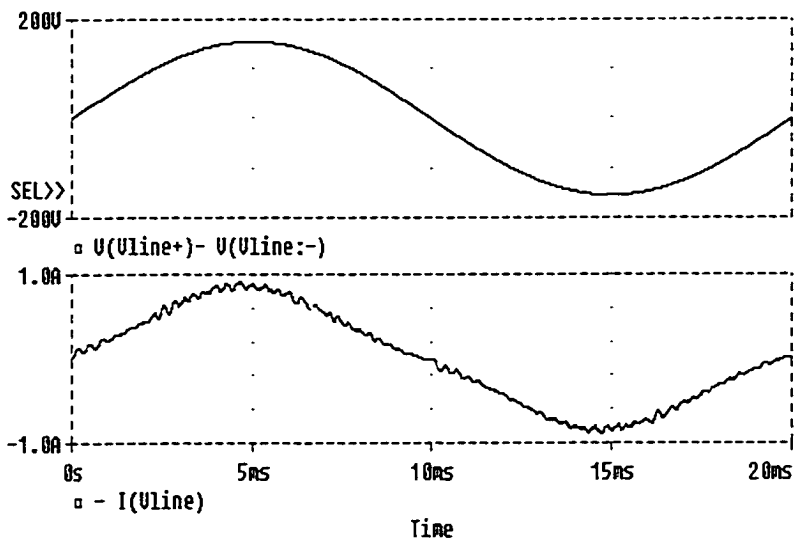
By using the above designed circuit parameters, the closed-loop PSPICE simulation of the proposed single-stage single-switch converter schematic has been carried out and the simulation results are shown in Fig. 4-18.

An experimental prototype of the converter was built up in the laboratory with the same circuit parameters. The forward transformer was created with a Philips ETD-PST39 core. To obtain the designed transformer ratios *n*, the primary windings and secondary winding were built with inductance values 30mH and 1.9mH, respectively. Pulse-width-modulation chip SG3525 was used to achieve closed-loop control. The experimental waveforms of filtered line current, and voltage and current at the switch, shown in Fig. 4-19, were recorded by using hp54542A oscilloscope. Both the simulated and the

experimental waveforms agree well and show that the waveforms of the line current is almost sinusoidal one, proving that a good power factor can be achieved by this converter topology.

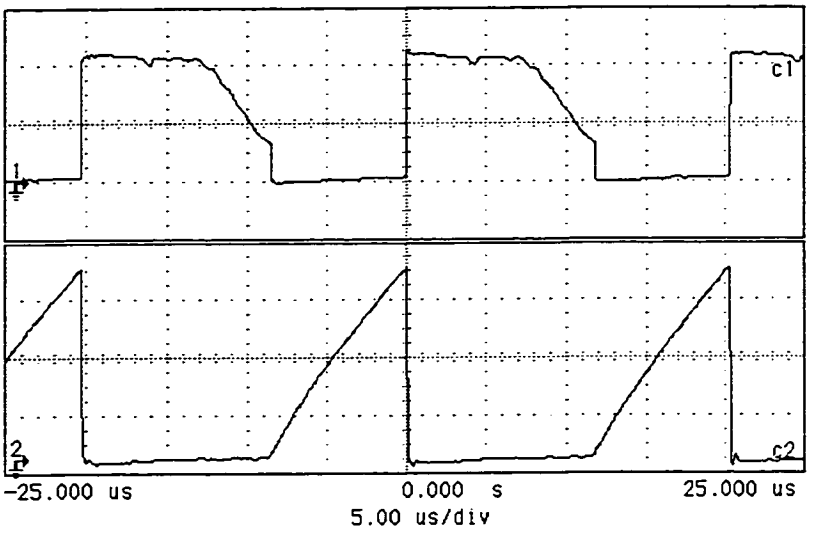


(a)

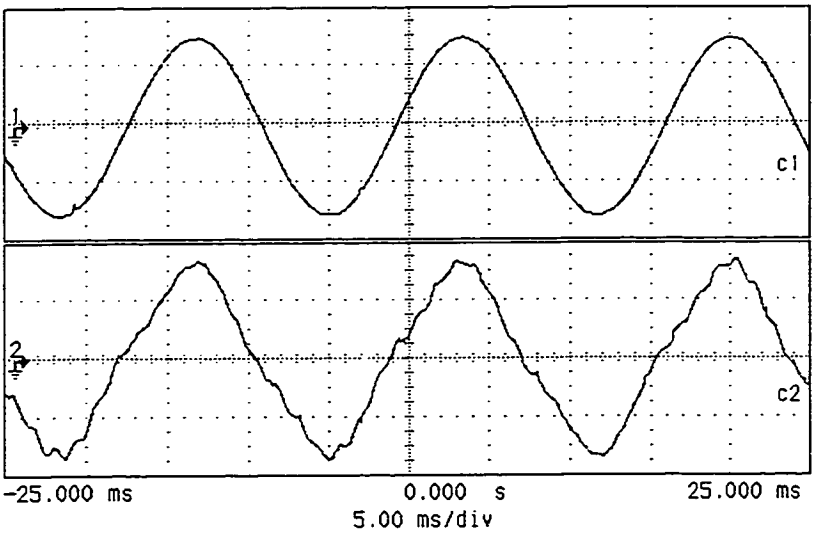


(b)

Figure 4-18 Simulation waveforms of the proposed converter: (a) voltage(upper) and current(lower) at the switch; (b) line voltage and filtered input current of the converter



(a)



(b)

Figure 4-19 Experimental waveforms of the proposed converter: (a) voltage (upper, 200V/div.) and current (lower, 1A/div.) at the switch; (b) line voltage (upper, 100V/div.) and filtered input current (lower, 1A/div.) of the converter

Measured power factor and efficiency are given in Figs. 4-20 and 4-21, respectively. It can be seen that the proposed converter can maintain 99% power factor and 87% efficiency at low line ($V_{l,rms}$ = 110V) operation and 95% power factor and 82% efficiency at high line ($V_{l,rms}$ = 220V) operation, respectively. The line current harmonics and THD under 110VAC input/50W output and 220VAC input/50W output were measured with hp6841A harmonic/flicker test system, shown in Figs. 4-22 and 4-23, respectively. In both 110VAC and 220VAC input cases, all the harmonics are lower than IEC1000-3-2 Class D restriction. The measured bulk capacitor voltage is shown in Fig. 4-24. It is noticed that with the output current changing from 0.5A to 1.5A, only small capacitor voltage change can be seen.

Simulations regarding to the tolerances of leakage inductances and the storage capacitors were performed. For 50% leakage inductance tolerance (L_1=80μH, L_2=40μH), only less than 2V difference in storage capacitor voltages were found. For 10% storage capacitance tolerance, less than 0.5V difference in storage capacitor voltages occurred.

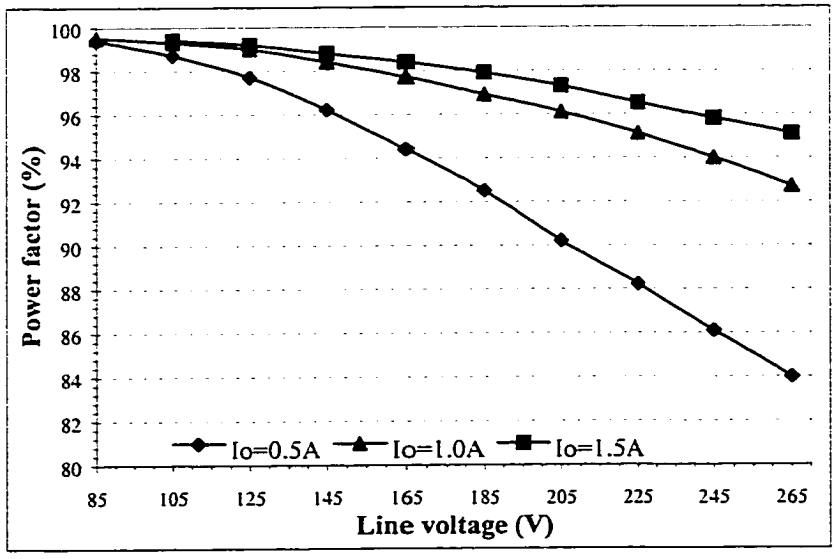


Figure 4-20 Experimental input power factor

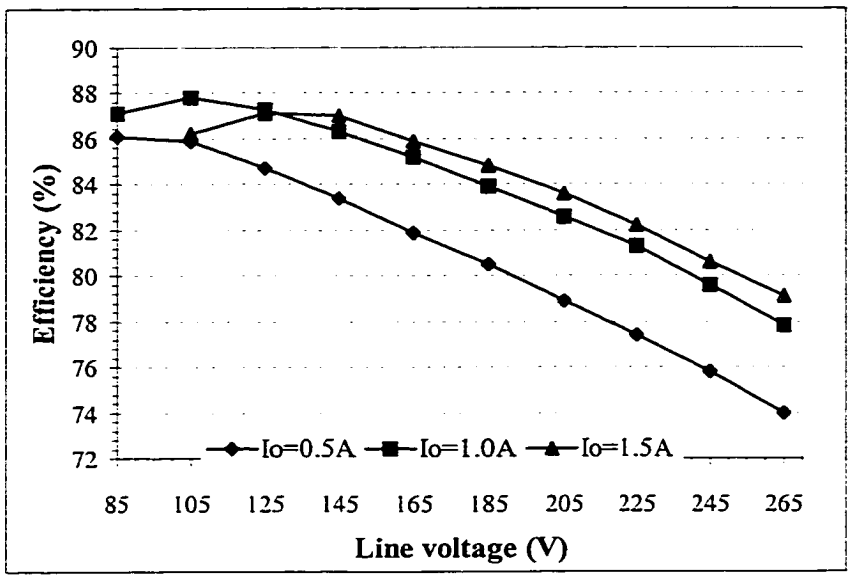


Figure 4-21 Experimental efficiency

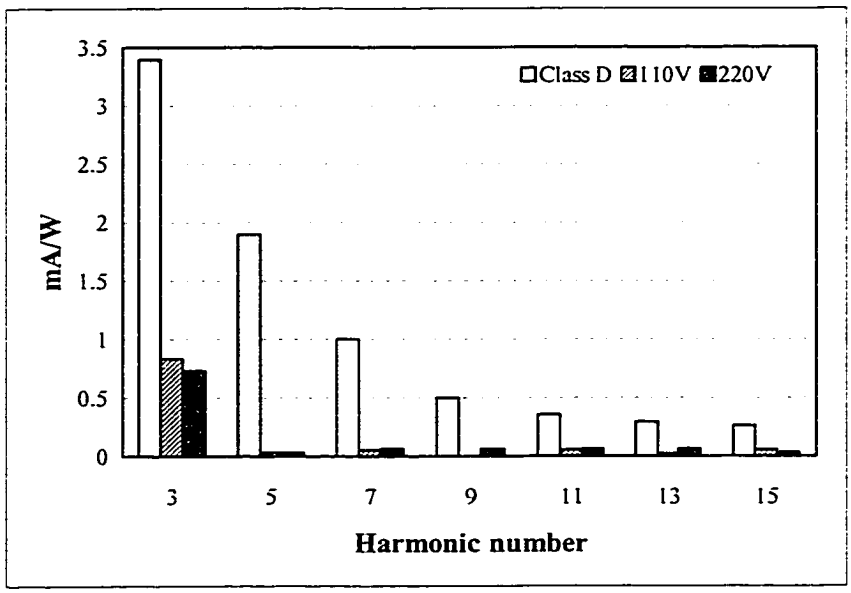


Figure 4-22 Measured current harmonics

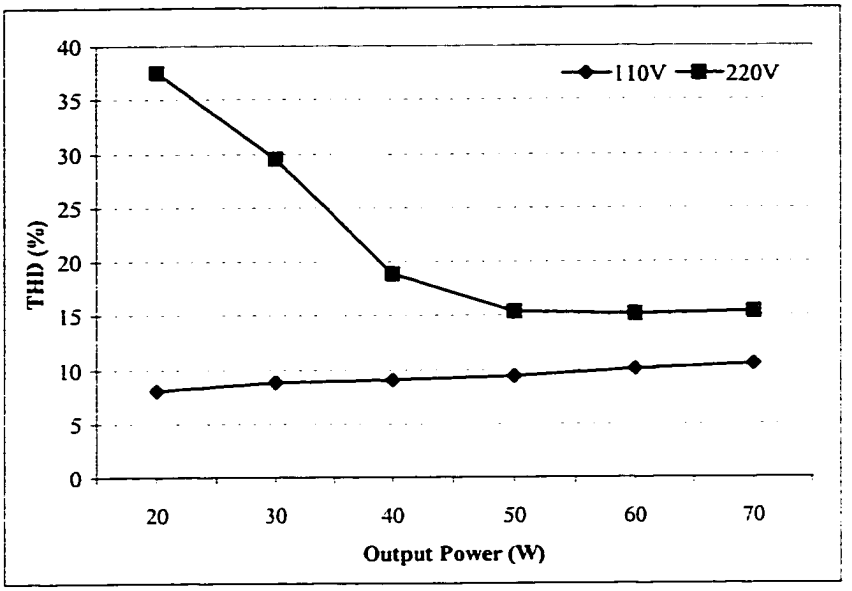


Figure 4-23 Measured THD

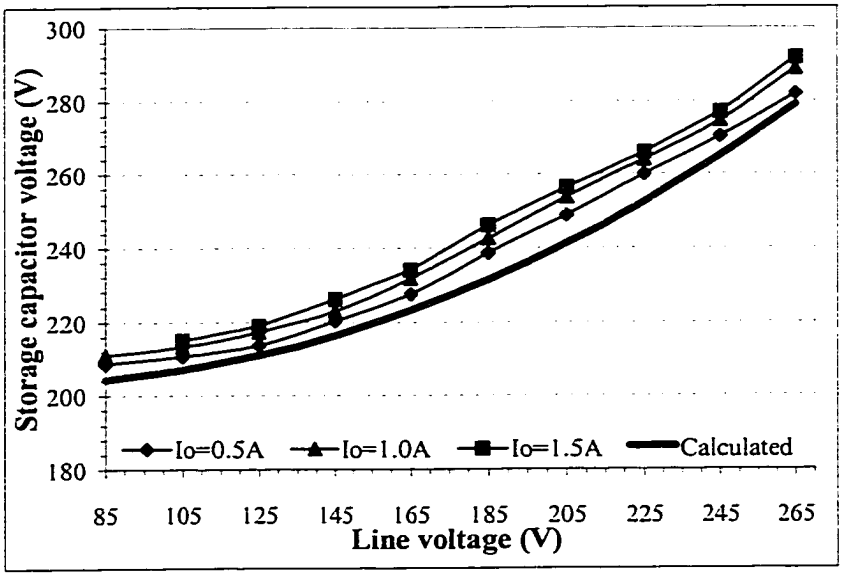


Figure 4-24 Measured storage capacitor voltage

4.4 SUMMARY

Two new single-stage single-switch AC/DC converter topologies with power factor correction have been presented in this chapter. Due to the discontinuous conduction mode operation of the input circuits, the proposed converters draws an almost purely sinusoidal line current, resulting in high input power factor. Both the presented converters can provide output electrical isolation. The storage capacitor voltages can be kept at a low level, reducing the design rating. For the flyback-forward combined converter, when the converter operates at 110VAC line, 80% efficiency and near unity power factor can be achieved. The proposed converter is suitable for low power and low cost applications with low THD and high power factor operation. The boost-forward combined converter is featured with the utilization of switched-capacitor network to improve its performance. As a result, both high power factor and high efficiency were achieved. Wide line regulation capability of this converter topology enables it to be applicable to universal input.

CHAPTER 5

SOFT-SWITCHING SINGLE-STAGE CONVERTER AND LOW VOLTAGE S^4 CONVERTER

5.1 INTRODUCTION

Generally speaking, AC/DC power supply plays a role of interface between the utility and the load. Due to the diversity of the end users, they place different issues for power supply researchers and design engineers. The development of power conversion technique has to be directed to practical applications.

With the residential industry and defense industry continuously demanding for even higher power density, switching mode power supply operating at high-frequency is required because at high switching frequency, the size and weight of circuit components can be remarkably reduced. The advent of power MOSFET makes the device switching speeds of tens of megahertz possible. Unfortunately, the conventional circuit topologies cannot keep the same pace owing to its increasing switching losses at high switching frequency. In practice, due to the fact that power MOSFET is not an ideal switch, during each switching time, energy loss (switching loss) exists. With the increasing of switch frequency, the switching loss becomes intolerable, resulting in very low conversion efficiency. Furthermore, the presence of leakage inductances in the high-frequency transformer and junction capacitances in the semiconductor devices causes the power devices to turn-off and/or turn-on with more energy loss and more noisy. Because of this

reason, switching frequency of the traditional SMPS is limited within 50KHz. In a certain application, the size of power supply corresponding to this frequency can still not be satisfied. To further boost the switching frequency, a new technique, soft-switching technique, was introduced to alleviate the switching loss.

Recently, with the operation frequency of microprocessors boosting to the range of gigahertz, low-voltage power supply is demanded. The traditional integrated circuits powered by 5V DC supply are suitable for high speed operation because of high energy loss, which causes thermal problems, and longer transient time. Many new generation integrated circuits are developed based on low-voltage (typically 3.3V) operation. But the semiconductor companies are targeting chips running at 1.5 to 2 volts to operate at gigahertz speeds. To achieve lower voltage output, the transformer turns ratio would be much high, particularly, when a boost converter is employed in front of the line to improve the input power factor. Such high ratio transformer needs specially designed [84]. Moreover, the control circuit in these converters needs to operate in very mall duty ratio in order to provide high conversion ratio, resulting in limitation in dynamic range and difficulty in stabilizing the systems.

A parallel structure with single-stage (but not single-switch) is proposed to process the input power [85]. Low output voltage is obtained by only taking part of the output voltage of the pre-regulator. Higher efficiency could be achieved since only part of the input power is processed twice. However, a flyback transformer is used in the input circuit to create a lower bus voltage, resulting in higher cost and higher peak input current than that a boost circuit gives. Floating ground is also undesired in this structure.

By extending the switch-capacitor configuration in the basic Cuk converter to a switched-capacitor network, a transformerless DC/DC converter with large conversion ratio was proposed by R. D. Middlebrook [86]. Since the capacitors are charged in series from the input when the switch is turned on and discharged in parallel to the output when the switch is turned off, the switched-capacitor network provides additional voltage step-down conversion. This circuit can operates at high-frequency because it uses switched-capacitor network instead of transformer to enhance its conversion ratio. However, the converter is only suitable for DC/DC application with non-isolation. Active switch count increases with the stage of switched-capacitor network, resulting in more switching loss.

In this chapter, we will develop two converter topologies aim at resolving the above two issues, i.e., soft-switching single-stage PFC converter and low-voltage PFC converter. Both the converter topologies are evolved from the two-capacitor PFC topology presented in Section 4.3, Chapter 4.

5.2 A SINGLE-STAGE PFC CONVERTER WITH ZVS OPERATION

5.2.1 The Proposed ZVS Converter

In Chapter 4, a single-stage single-switch converter with two bulk capacitors was proposed (Fig. 4-10). This converter degrades the cost by using two storage capacitors to share the dc bus voltage. When the switch is turned on, the input inductor draws energy from the line, meanwhile, the storage capacitors C_{S1} and C_{S2} supply power through the transformer. When the switch is turned off, the input inductor current charges the storage capacitors. Near unity power factor can be obtained since the choke inductor operates in DCM.

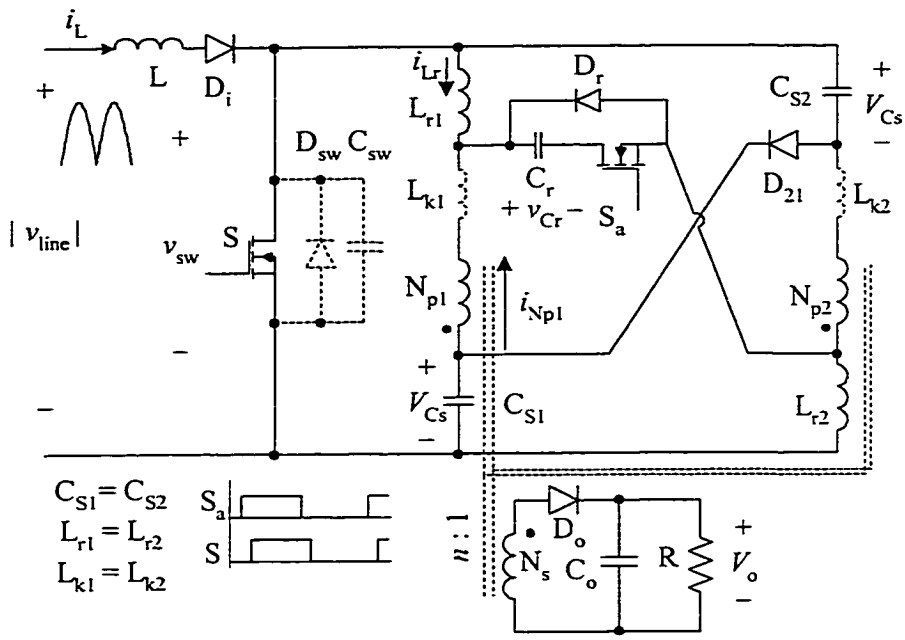


Figure 5-1 The proposed soft-switching PFC converter

However, the circuit described in Fig. 4-10 can not achieve high power density due to the fact that the power switch operates under hard-switching with higher than 400V drain-source voltage. In order to create a ZVS condition for the power switch, an auxiliary switch S_a, two resonant inductors, L_{r1} and L_{r2}, a resonant capacitor C_r, and a diode D_r are introduced, shown in Fig. 5-1. To relieve the capacitive turn on loss on the auxiliary switch, low output capacitance MOSFET should be considered in selecting S_a.

5.2.2 Principle of Operation

In each switching cycle, with the auxiliary switch S_a turning on, a short interval of resonant takes place during which the main switch turns on with ZVS. The cyclic operation of the proposed converter is almost the same as its hard-switching counterpart except that a resonant mode is inserted. The switching waveforms are shown in Fig. 5-2

and the switching periods are described as follows by assuming that capacitor voltages $V_{Cs1} = V_{Cs2} = V_{Cs}$ are constant and the line voltage is V_g in one switching cycle.

Before the auxiliary switch is turned on, the main switch is open, and its output capacitor holds a voltage of $2V_{Cs}$. The resonant inductors carry zero current. Let's start the cyclic operation when the auxiliary switch is turned on at t_0.

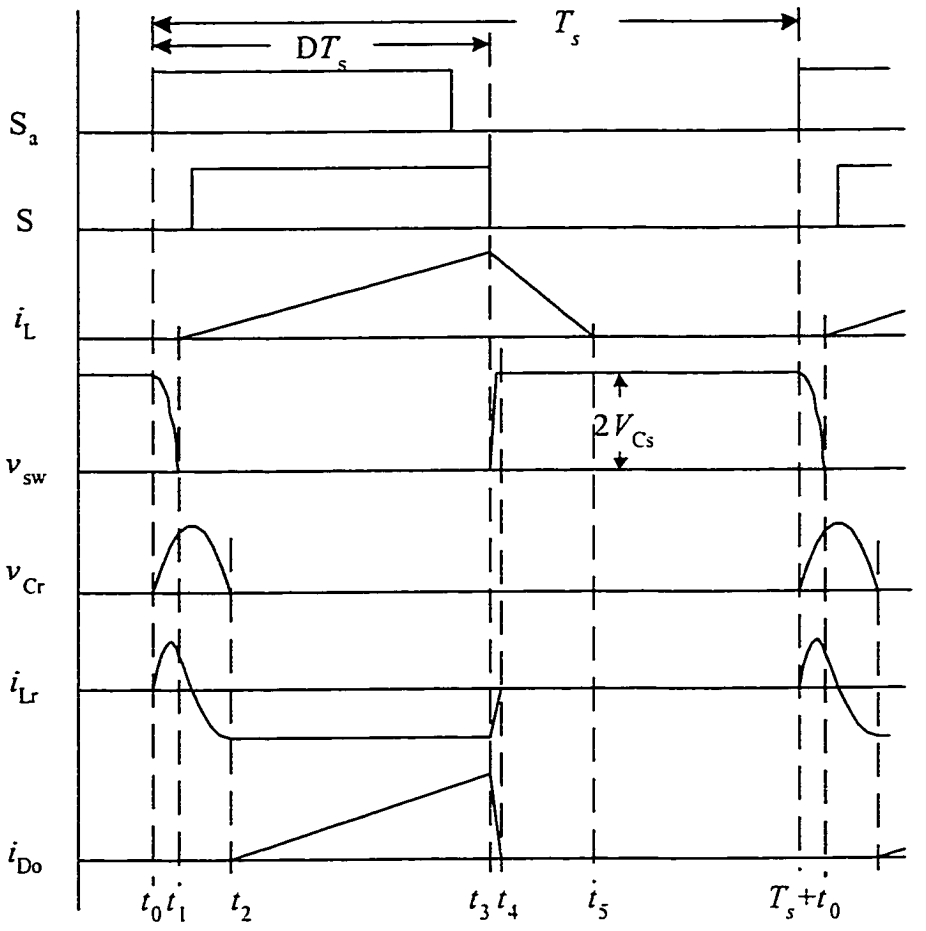


Figure 5-2 Theoretical waveforms of the proposed soft-switching PFC converter

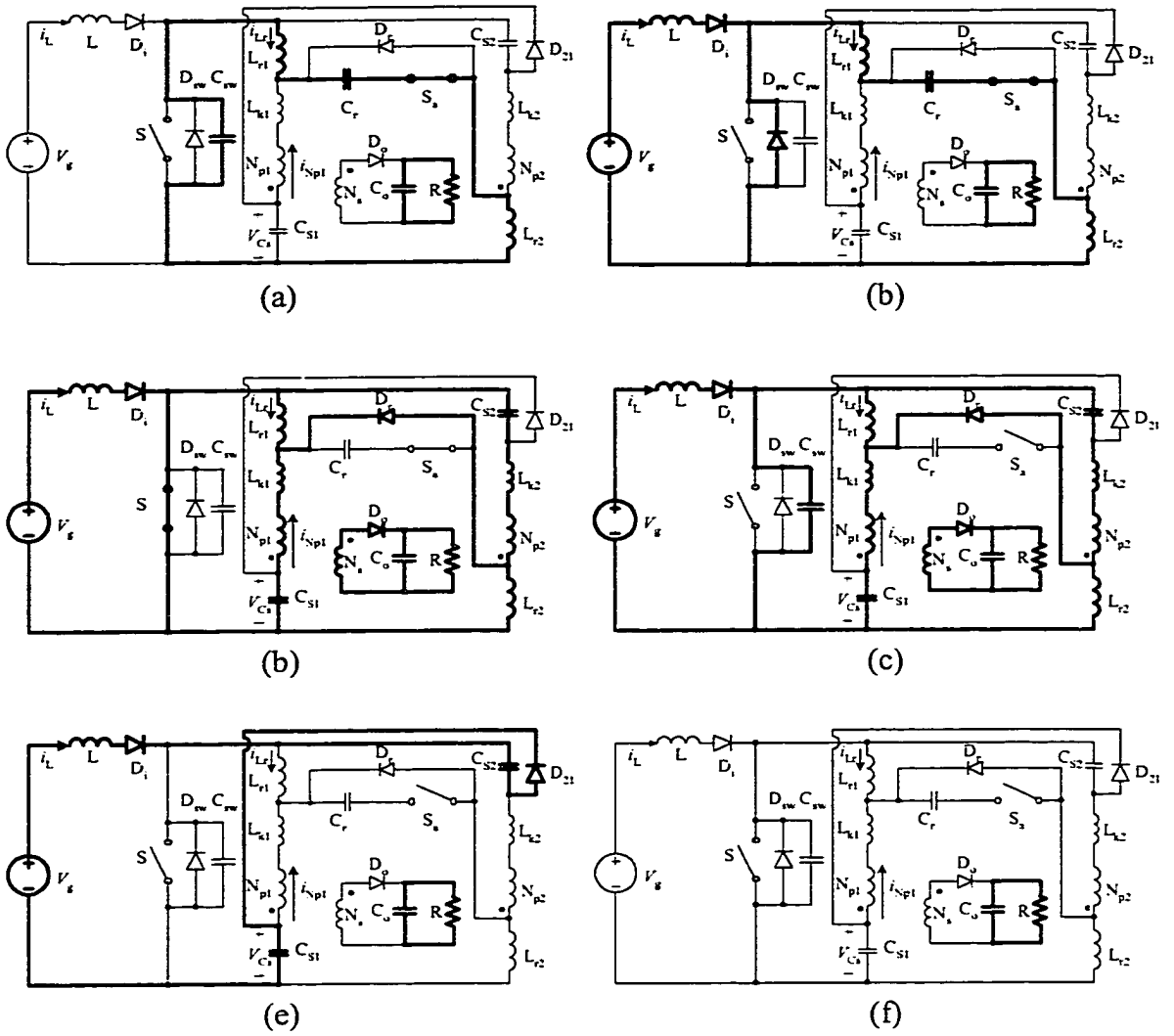


Figure 5-3 Equivalent topologies for the six switching periods: (a) P1($t_0 \sim t_1$); (b) P2($t_1 \sim t_2$); (c) P3($t_2 \sim t_3$); (d) P4($t_3 \sim t_4$); (e) P5($t_4 \sim t_5$); (f) P6($t_5 \sim t_0 + T_s$)

Switching Period 1:

At $t = t_0$, the auxiliary switch S_a is turned on. A resonance takes place firstly among C_{sw}, C_r, L_{r1} and L_{r2}. The thicker line in Fig. 5-3(a) shows the resonance loop during this switching period. The key waveforms are expressed as follows.

$$v_{sw}(t) = \frac{2V_{Cs}}{1+k_c}(1+k_c \cos\omega_0 t); \tag{5.1a}$$

$$v_{Cr}(t) = \frac{2V_{Cs}}{1+k_c}(1-\cos\omega_0 t);$$

$$i_{Lr}(t) = \frac{2V_{Cs}}{Z_0}\sin\omega_0 t;$$

$$i_L(t) = 0;\ i_{Np}(t) = 0.$$

Where,

$$Z_0 = \sqrt{2L_r/C_r}\cdot\sqrt{1+k_c} = Z_1\sqrt{1+k_c}; \tag{5.1b}$$

$$\omega_0 = \sqrt{\frac{1+k_c}{2L_r C_r}}\cdot = \omega_1\sqrt{1+k_c};$$

$$k_c = \frac{C_r}{C_{sw}};\ Z_1 = \sqrt{2L_r/C_r};\ \omega_1 = 1/\sqrt{L_r C_r}.$$

It can be seen from the expression of v_{sw} that in order to create zero-voltage-switching condition for the main switch S, we must design the resonant capacitance C_r to be larger than the output capacitance C_{sw} of the main MOSFET switch, i.e., $C_r/C_{sw} > 1$.

Assuming at $t = t_1$, v_{sw} decreases to zero. The duration of this switching period is given by,

$$\Delta t_1 = t_1 - t_0 = \omega_0^{-1}\left[\pi - \cos^{-1}(1/k_c)\right]. \tag{5.1c}$$

Switching Period 2:

With the switch voltage v_{sw} decreasing to zero, diode D_{sw} conducts. The input inductor L is magnetizing in this period. The resonance continues among C_r, L_{r1} and L_{r2}, as shown in Fig. 5-3(b). During this period, the following expressions were derived:

$$v_{sw}(t)=0; \tag{5.2a}$$

$$v_{Cr}(t)=2V_{Cs}\sqrt{1/k_c}\sin\left[\omega_1(t-t_1)+\beta\right];$$

$$i_{Lr}(t)=\frac{2V_{Cs}}{Z_1}\sqrt{1/k_c}\cos\left[\omega_1(t-t_1)+\beta\right];$$

$$i_L(t)=\frac{V_g}{L}(t-t_1);\ i_{Np}(t)=0.$$

Where,

$$\beta=\tan^{-1}\sqrt{1/(k_c-1)}. \tag{5.2b}$$

In this period, the main switch is turned on with ZVS. This period ends when the resonant capacitor voltage reaches zero. The interval of this period is given by,

$$\Delta t_2=t_2-t_1=\omega_1^{-1}\left(\pi-\tan^{-1}\sqrt{1/(k_c-1)}\right). \tag{5.2c}$$

Switching Period 3:

With the capacitor voltage v_{Cr} resonant to zero, diode D_r turns on. Since S-L_{r2}-D_r-L_{r1}-S forms a freewheeling loop, as shown in Fig. 5-3(c), the resonant inductor keeps a constant current. The auxiliary switch can be turned off with zero-current-switching (ZCS) at anytime when the resonant inductor current i_{Lr} becomes negative. The transformer primary windings N_{p1} and N_{p2} transfer energy to its secondary N_s from energy storage capacitors C_{s1} and C_{s2}, respectively. The input inductor continues magnetizing, absorbing energy from the line. The key waveforms can be described by the following expressions:

$$v_{sw}(t)=0;\ v_{Cr}(t)=0; \tag{5.3a}$$

$$i_{Lr}(t)=-\frac{2V_{Cs}}{Z_1}\sqrt{1/k_c}\ ;\ i_L(t)=\frac{V_g}{L}(t-t_1);$$

$$i_{Np}(t)=\frac{1}{L_k}(V_{Cs}-nV_o)(t-t_2).$$

The duration of this period is determined by the converter duty ratio.

$$\Delta t_3=t_3-t_2=DT_s-\Delta t_1-\Delta t_2. \tag{5.3b}$$

Here the duty ratio D is defined as,

$$D\triangleq(t_3-t_0)/T_s. \tag{5.4}$$

(Assuming the main switch is turned off at $t = t_3$.)

Switching Period 4:

The main switch is turned off. The switch output capacitor C_{sw} is quickly charged to $2V_{Cs}$ by input inductor current i_L and resonant inductor current i_{Lr}, as shown in Fig. 5-3(d), then diode D_{21} starts conducting to clamp the main switch voltage. Assuming the switch voltage reaches $2V_{Cs}$ with zero time, the following equations can be considered to describe the circuit operation:

$$v_{sw}(t)=2V_{Cs};\ v_{Cr}(t)=0; \tag{5.5a}$$

$$i_{Lr}(t)=\frac{V_{Cs}}{L_r}(t-t_3)-\frac{2V_{Cs}}{Z_1}\sqrt{1/k_c};$$

$$i_L(t)=\frac{1}{L}V_g(DT_s-\Delta t_1)-\frac{1}{L}(2V_{Cs}-V_g)(t-t_3);$$

$$i_{Np}(t)=\frac{1}{L_k}(V_{Cs}-nV_o)(DT_s-\Delta t_1-\Delta t_2)-\frac{nV_o}{L_k}(t-t_3);$$

This switching period ends when both the resonant inductor current and the primary winding current reach zero. Because L_r and L_k are very small, the duration of this period can be neglected, i.e.,

$$\Delta t_4 = t_4 - t_3 \approx 0 . \tag{5.5b}$$

Switching Period 5:

Input inductor continues to demagnetize until all the magnetic energy is released to charge the storage capacitors (Fig. 5-3(f)).

$$v_{sw}(t) = 2V_{Cs}\,; v_{Cr}(t) = 0\,; i_{Lr}(t) = 0\,; \tag{5.6a}$$

$$i_L(t) = \frac{1}{L}(D T_s - \Delta t_1) - \frac{1}{L}(2V_{Cs} - V_g)(t - t_3)\,;$$

$$i_{Np}(t) = 0 .$$

The interval of this period is given by,

$$\Delta t_6 = t_6 - t_5 = \frac{V_g}{2V_{Cs} - V_g}(D T_s - \Delta t_1) - \Delta t_5 . \tag{5.6b}$$

Switching Period 6:

With the input inductor current decreasing to zero, diode D_i turns off (Fig. 5-3(g)). All the voltages and currents remain constants. The converter is waiting for the next driving signal S_a to start a new switching cycle. In this period we have,

$$v_{sw}(t) = 2V_{Cs}\,; v_{Cr}(t) = 0\,; \tag{5.7a}$$

$$i_{Lr}(t) = 0;\ i_L(t) = 0;\ i_{Np}(t) = 0 .$$

The interval of this period can be expressed as,

$$\Delta t_7 = T_s - DT_s - \Delta t_5 - \Delta t_6 . \tag{5.7b}$$

5.2.3 Steady-State Analysis

5.2.3.1 Storage capacitor voltage

To improve the input power factor and stabilize the output voltage, two higher value storage capacitors are used in the proposed converter. In steady-state operation, the storage capacitor voltages can be considered as constant. It can be shown that the higher the storage capacitor voltage the higher the input power factor can be obtained. Unfortunately, almost all the components voltage stresses are directly related to the storage capacitor voltage. In practical design, some trade off must be made. In order to look into the storage capacitor voltage, let's define the following voltage ratio:

$$M_1 \triangleq V_o / V_{Cs} . \tag{5.8}$$

At the output stage, we have $\overline{i_{Do}(t)} = V_o / R$ ($\overline{i_{Do}(t)}$ is the average current through the output rectifier diode D_o). By calculating the waveform of $i_{Do}(t)$ (= 2 n $i_{Np}(t)$), it yields,

$$\frac{n}{k_L \tau_n}\left(D - \frac{\Delta t_1 + \Delta t_2}{T_s}\right)^2 \left(1 + \frac{1 - n M_1}{1 + n M_1}\frac{L_r + L_k}{L_k}\right)\left(\frac{1}{M_1} - n\right) = 1. \tag{5.9}$$

Where,

$$k_L = \frac{L_r}{L},\ \tau_n = \frac{\tau}{T_s} \text{ and } \tau = \frac{L}{R}. \tag{5.10}$$

To simplify the analysis, let's assume we design for $L_\tau = L_k$. Solving Eq. (5.9), we obtain,

$$M_1 = \frac{1}{2a}\left(-b + \sqrt{b^2 - 4ac}\right), \tag{5.11}$$

where,

$$a = n\left[1 - \frac{n^2}{k_L \tau_n}\left(D - \frac{\Delta t_1}{T_s} - \frac{\Delta t_2}{T_s}\right)^2\right];$$

$$b = 1 + \frac{4n^2}{k_L \tau_n}\left(D - \frac{\Delta t_1}{T_s} - \frac{\Delta t_2}{T_s}\right)^2;$$

$$c = -\frac{3n}{k_L \tau_n}\left(D - \frac{\Delta t_1}{T_s} - \frac{\Delta t_2}{T_s}\right)^2.$$

Where,

$$\Delta t_1/T_s = 0.5\, f_{n1}\left[1 - \left(\pi\sqrt{1 + 0.5k_c}\right)^{-1} \cos^{-1} 0.5k_c\right]; \tag{5.12}$$

$$\Delta t_2/T_s = 0.5\, f_{n1}\left(\sqrt{1 + 0.5k_c}^{-1} - \pi^{-1} \tan^{-1}\sqrt{0.5k_c - 1}^{-1}\right);$$

$$f_{n1} = 2\pi f_s/\omega_1 = 2\pi\sqrt{2L_r C_r}\, f_s;$$

Figure 5-4 shows Output to storage capacitor voltage ratio under different loads in term of duty ratio. It can be seen that when D>0.2, we have

$$M_1 \approx 1/n. \tag{5.13}$$

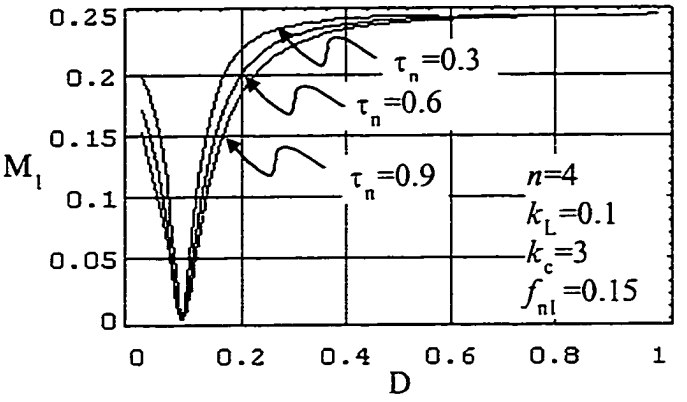


Figure 5-4 Output to storage capacitor voltage ratio

5.2.3.2 AC/DC conversion ratio

According to the definition of duty ratio (Eq. (5.4)) and referring to the waveform of the input inductor current $i_L(t)$ (Fig. 5-2), the absolute value of filtered line current can be expressed as,

$$i_1(t) = \frac{T_s}{L}\left(D - \frac{\Delta t_1}{T_s}\right)^2 \frac{V_{Cs}\, v_1(t)}{2V_{Cs} - v_1(t)}. \tag{5.15}$$

When $v_1(t) = V_{1,max}$, we have,

$$I_{1,max} = \frac{T_s}{L}\left(D - \frac{\Delta t_1}{T_s}\right)^2 \frac{V_{Cs}\, V_{1,max}}{2V_{Cs} - V_{1,max}}. \tag{5.16}$$

Because we assumed that the converter operates under high input power factor, the rms value of line current can be directly written as,

$$I_{1,rms} = \frac{T_s}{\sqrt{2}L}\left(D - \frac{\Delta t_1}{T_s}\right)^2 \frac{V_{Cs}\, V_{1,rms}}{\sqrt{2}V_{Cs} - V_{1,rms}}. \tag{5.17}$$

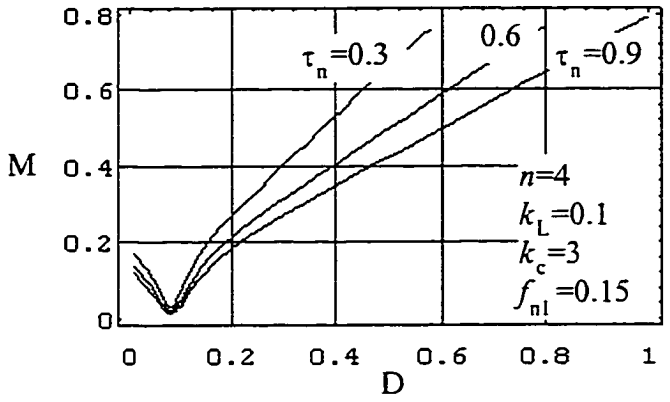


Figure 5-5 AC/DC conversion ratio

Considering power balance ($V_{l,rms}\ I_{l,rms} = V_o^2/R$) in steady-state, the AC/DC conversion ratio is given by,

$$M = \frac{1}{2\sqrt{2}}\left(M_1 + \sqrt{M_1^2 + \frac{4}{\tau_n}(D - \Delta t_1/T_s)^2}\right) \tag{5.18}$$

Figure 5-5 gives the conversion characteristic under deferent load time constants.

5.2.3.3 Limit duty ratios and regulation capabilities

The minimum duty cycle must allow the resonant periods (switching periods 1 and 2) to fulfilled. Therefore,

$$D_{min} = \Delta t_1/T_s + \Delta t_2/T_s \ . \tag{5.19}$$

As the AC/DC converter adopts DCM operation in its input stage to achieve PFC, we must prevent the converter from going into CCM. Under critical conduction mode (CrCM), i.e., $t_5 = T_s$ (referring to Fig. 5-2), we have,

$$\frac{v_1(t)}{L}\left(D_{crit}-\frac{\Delta t_1}{T_s}\right)-\frac{2V_{Cs}-v_1(t)}{L}(1-D_{crit})=0. \tag{5.20}$$

Since $\Delta t_1/T_s \ll D_{crit}$, neglecting Δt_1 and noticing definitions of M and M_1, the maximum duty ratio is found as,

$$D < D_{crit} = 1-\frac{M_1}{\sqrt{2}\,M}, \tag{5.21}$$

or,

$$M > \frac{M_1}{\sqrt{2}(1-D)}. \tag{5.22}$$

5.2.3.4 Critical input inductance and output voltage ripple

To ensure the converter operates in CCM, we must design the input inductance to be less than the critical inductance. It can be shown that under CrCM, the critical input inductance is,

$$L_{crit}=\frac{D_{crit}T_s R}{2M^2}=\frac{\sqrt{2}M-M_1}{2\sqrt{2}M^3}T_s R. \tag{5.23}$$

The output capacitor should be designed to satisfy specified output voltage ripple. Approximately, the output voltage ripple can be expressed as,

$$\frac{\Delta V_o}{V_o}=\frac{(1-D)T_s}{RC_o-0.5(1-D)T_s}. \tag{5.24}$$

5.2.3.5 Practical challenge

Since there exists output capacitance in the auxiliary switch S_a, high peak parasitic ringing occurs during the switch is turned off, resulting in difficulty in selection of the auxiliary switch. To block the auxiliary switch voltage, the resonant tank is modified as shown in Fig. 5-6. Two resonant capacitors are used on each side of the auxiliary switch. Between each resonant capacitor and the switch, two diodes are connected to block the switch voltage at $2V_{Cs}$. The block diodes conduct only a short time in one switching cycle, so only low rating is required.

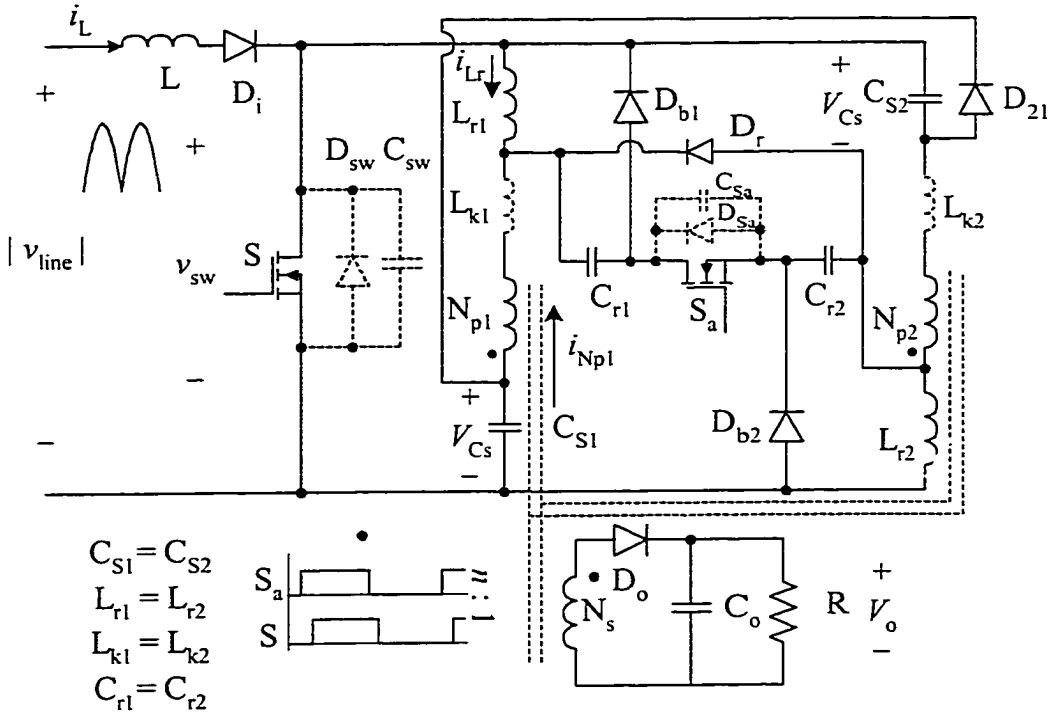


Figure 5-6 Proposed converter with voltage clamp

5.2.4 Design Example

Specifications:

Nominal input voltage: $V_{I,rms}$ = 110V@60Hz;

Output voltage: V_o = 50V±1%;

Nominal load current: I_o = 2A;

Switching frequency: f_s = 300kHz.

Design:

To compromise between voltage stress and regulation capabilities, we set

Transformer ratio: $n = 4$;

Inductance ratio: $k_L = L_r/L = 0.1$;

Capacitance ratio: $k_c = C_r/C_{sw} = 1.5$;

Frequency ratio: $f_{n1} = f_s/f_1 = 0.15$.

According to Eq. (5.14), the storage capacitor voltage $V_{Cs} \approx nV_o$ = 200V. Therefore, we may select the switch type IRF460 (V_{ds} = 500V, C_{sw} = 870pF, I_d = 20.0A) as the main switch. Then we can make the following design:

$C_{r1} = C_{r2} = 2\,C_r = 2\,k_c\,C_{sw} = 2 \times 1.5 \times 870\text{pF} \approx 2.6\text{nF}$;

From $f_{n1} = 2\pi\sqrt{L_r C_r}\, f_s$, we have

$$L_r = \left(\frac{f_{n1}}{2\pi f_s}\right)^2 \frac{1}{C_r} = \left(\frac{0.15}{2\pi \times 300 \times 10^3}\right)^2 \frac{1}{1.3 \times 10^{-9}} \approx 5\mu\text{H};$$

$L = L_r/k_L = 5\mu\text{H}/0.1 = 50\mu\text{H}$.

At Nominal load: $\tau_{n,1} = \frac{L}{R} f_s = \frac{50 \times 10^{-6}}{25} \times 300 \times 10^3 = 0.6$;

At 50% load: $\tau_{n,1} = \frac{L}{R} f_s = \frac{50 \times 10^{-6}}{50} \times 300 \times 10^3 = 0.3$;

Figure 5-5 gives the conversion ratio vs. duty ratio under $\tau_n = 0.3$, 0.6 and 0.9. For nominal load, at M=0.455 (corresponding $V_{l,rms} = 110V$ and $V_o = 50V$) we have D= 0.44.

To design the storage capacitors, let's consider that due to one line cycle missing of line voltage, an average voltage drop of ζV_{Cs} on the storage capacitor is allowed, then by analysis we have

$$C_s = \frac{T_l M_1^2}{\zeta(2-\zeta) R} \tag{5.25}$$

Assuming $\zeta = 0.1$, $C_s = 219.2\mu F$. Set $C_s = 220\mu F/250V$.

According to Eq. (5.24), the output filter capacitor can be designed.

$$C_o = \frac{(1-D)}{R f_s}\left(\frac{1}{\Delta V_o/V_o}+0.5\right) = \frac{(1-0.44)}{25\times 300\times 10^3}\left(\frac{1}{0.02}+0.5\right) \approx 11.3\mu F$$

Select $C_o = 47\mu F/100V$.

5.2.5 Simulation and Experimental Results

The proposed soft-switching PFC converter has been simulated by PSPICE. The simulation waveforms are shown in Fig. 5-7. As it can be seen, zero-voltage turning on for the main switch and zero-current turning off for the auxiliary switch have been achieved. The drain-source voltage of the auxiliary switch, V(Sa), has been successfully clamped under 500V.

An experimental prototype of the proposed soft-switching converter was built in laboratory referring to the above designed parameters. The following types components are used:

Input choke L: 65μH, 547L 55353-A2

Input diode D_i: DSEI60-05A

Main switch S: IRFP460

Auxiliary switch Sa:

Forward transformer T: N_{p1}:N_{p2}:N_s=18:18:6, Philips 3F3 E41/17/12

Storage capacitor Cs: 68μF/380V

Output capacitor Co: 470μF/63V

Resonant inductor Lr: 6μH, LA4229

Resonant capacitor Cr: 3900pF, CDM

Diodes: D21: MUR850; Dr: MUR840; Do: 25CPF16; D_{b1}, D_{b2}: UF4004.

PWM IC chip: UC1825

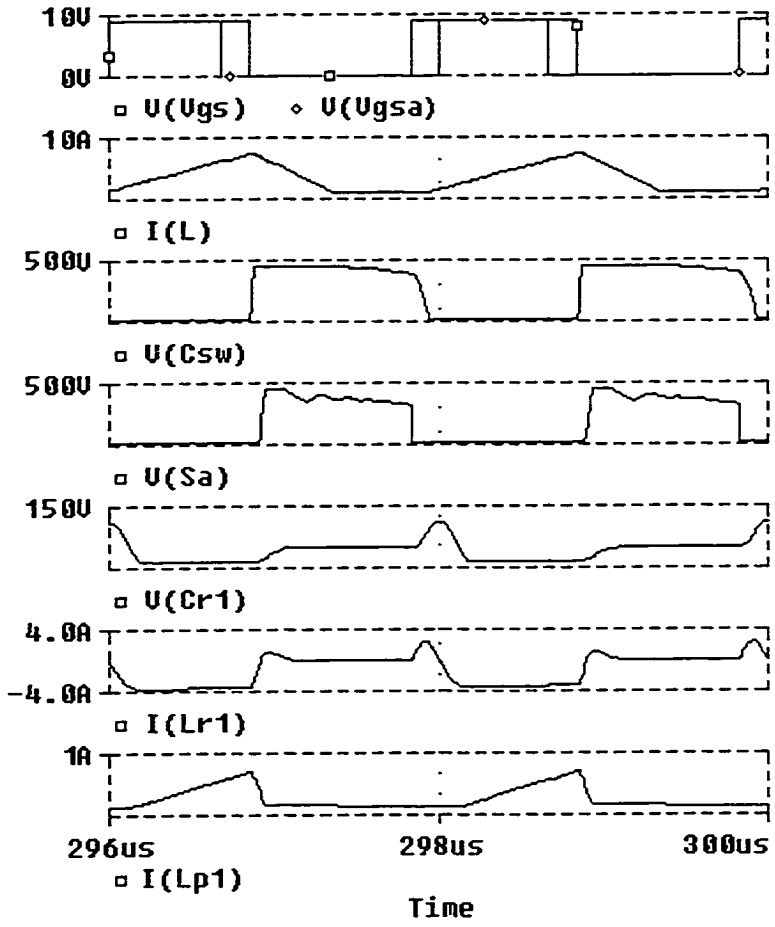
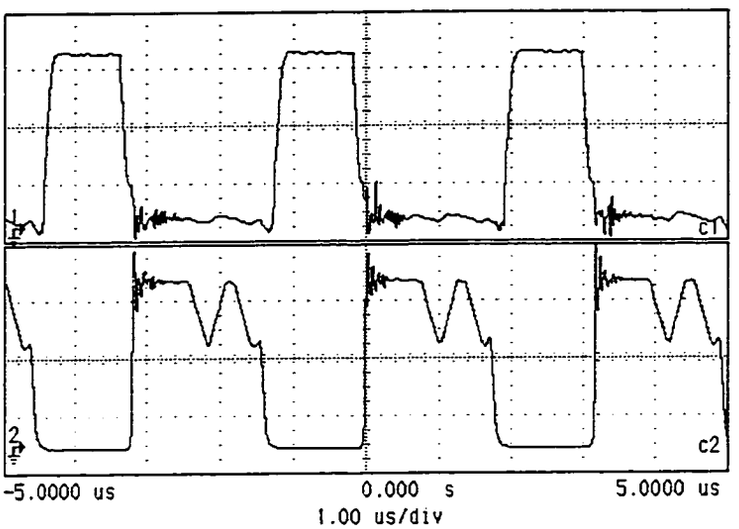


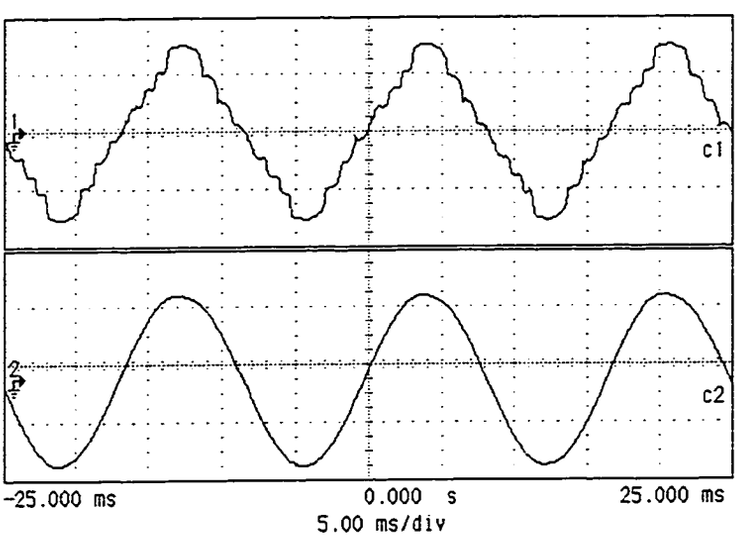
Figure 5-7 Simulation waveforms of the proposed PFC converter

The experimental waveforms were recorded by hp54542A oscilloscope, given in Fig. 5-8. Fig. 5-8(a) shows the switch waveforms of the main switch at the peak line voltage. It is clear that before the drive signal gated the power switch, the drain-source voltage had been brought down to zero by the resonant tank, which means zero-voltage-switching was achieved. Fig. 5-8(b) shows the line current comparing with the line voltage. As we can see, the line current is in phase with the line voltage. Light distortion was seen because of the use of boost type circuit at the converter's input and the affect of line filter.

The measured power factor and efficiency are given in Fig. 5-9. Power factor higher than 93% can be ensured for output from 50W to 100W when line changes from 100V to 120V. At high load, the converter efficiency (including the line filter and the start resistor) is maintained about 80%. At light load, when the line becomes high, the efficiency decreases due to disappear of the ZVS condition.

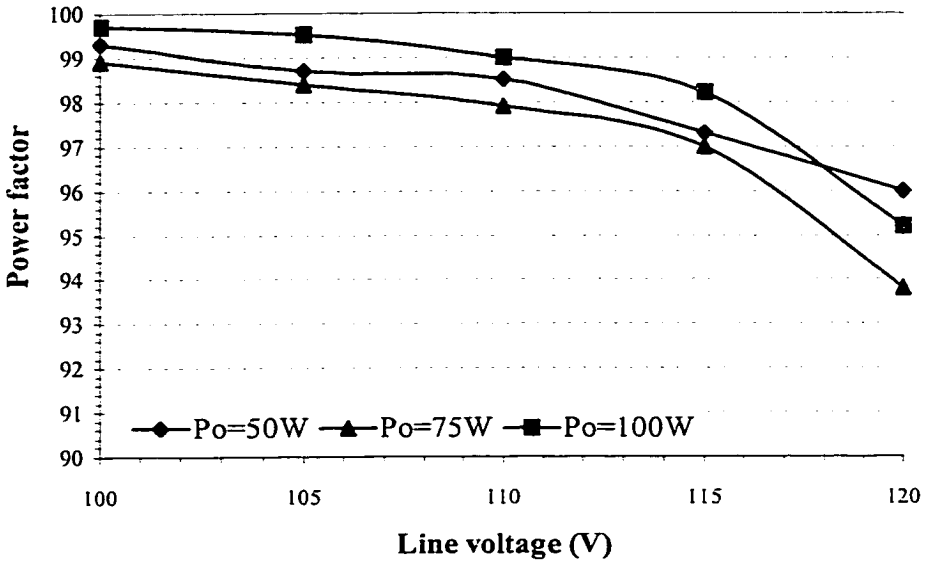


(a)

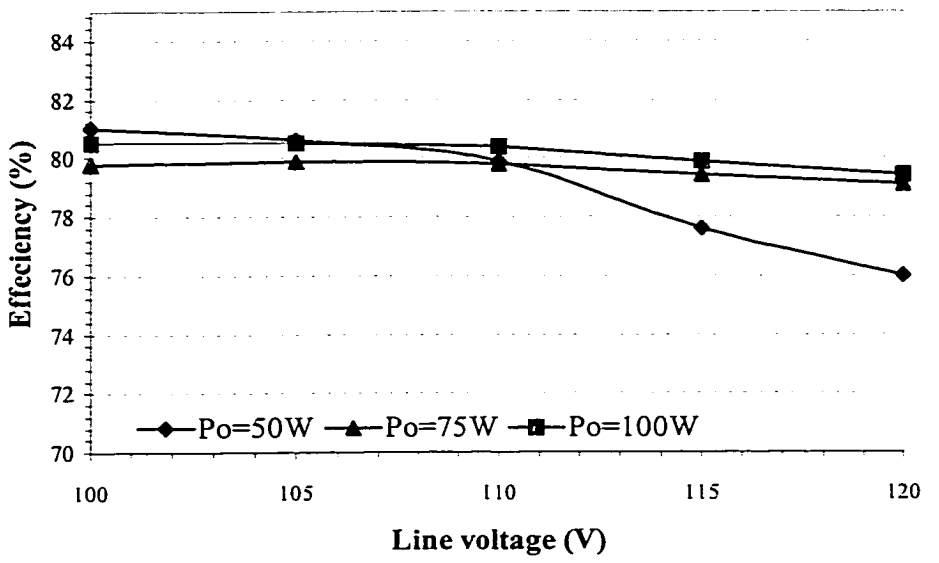


(b)

Figure 5-8 Expreimental Waveforms of the soft-switching PFC converter (recorded under 110VAC input and 100W output): (a) switch waveforms (top: gate signal; bottom: drain-source voltage, 100V/div.); (b) line waveforms (top: line current, 1A/div.; bottom: line voltage, 100V/div.)



(a)



(b)

Figure 5-9 Experimental measurements: (a) power factor; (b) efficiency

5.3 AN AC/DC S4 CONVERTER WITH LOW OUTPUT VOLTAGE

5.3.1 The Proposed Low-Voltage PFC Converter

In this section, we propose a single switch AC/DC PFC isolation converter with low-voltage output. Reviewing the S^4 converter topology proposed in Section 4.3, Chapter 4, Fig. 4-10, where we used two bulk storage capacitors to split the bus voltage, the connection of capacitors can be extended to a switched-capacitor network. The main idea in constructing a low-voltage converter is insertion of such a switched-capacitor step-down network in between the input PFC circuit and the output circuit, shown in Fig. 5-10. The input circuit can still remain a boost circuit operating in DCM to provide near unity input power factor and a dc bus voltage. The switched-capacitor network converts the higher bus voltage to lower level dc voltage when the switch is turned on to drive the forward output circuit. Large conversion ratio comes from three approaches: duty ratio control, switched-capacitor step-down network and step-down transformer. It should be note that the three stages of the converter share the same power switch.

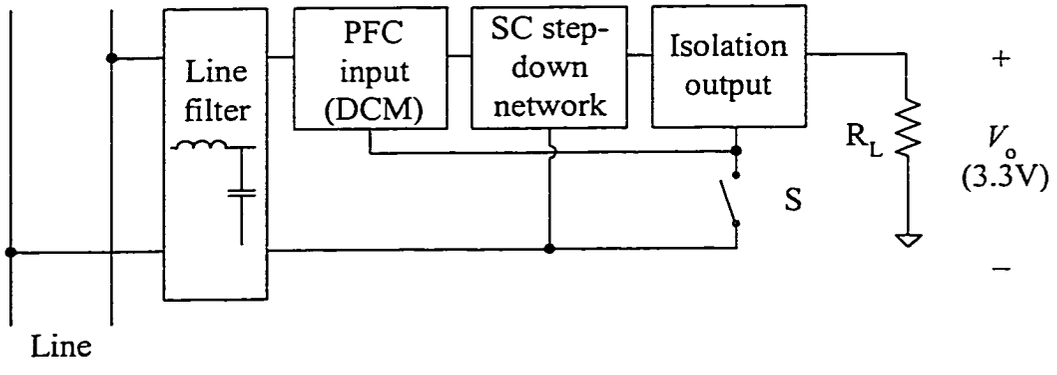


Figure 5-10 Diagram of the proposed AC/DC low-output voltage converter

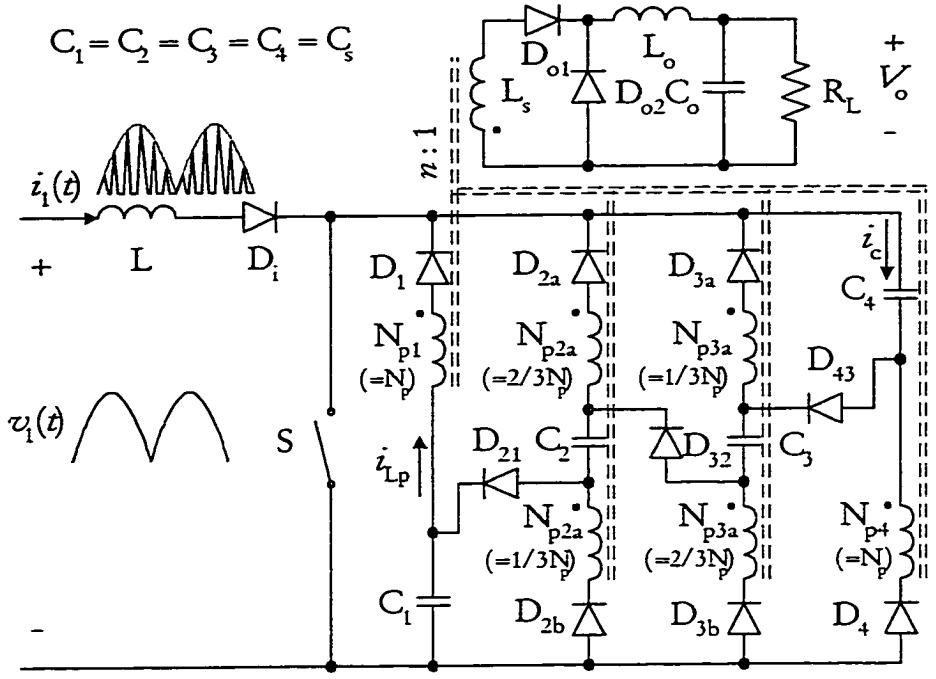


Figure 5-11 The proposed AC/DC converter with four-stage switched-capacitor network

Figure 5-11 shows the proposed converter topology with four-stage step-down switched-capacitor network. The forward transformer has four equal-turn primary windings ($N_{p1} = N_{p2a} + N_{p2b} = N_{p3a} + N_{p3b} = N_{p4} = N_p$) with each of them being connected to one of the capacitors. In order to have equal voltages on the storage capacitors C_1, C_2, C_3 and C_4, each primary winding in the inner branches has been divided into two parts. Note that more stages can be used when even low output voltage is desired.

5.3.2 Principle of Operation

As far as switching cycle operation is concerned, the line voltage can be considered as constant since the switching frequency is much higher than the line frequency. In steady-state, as the storage capacitors are equal and large, we consider the capacitors as dc voltage sources, i.e., $V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{Cs}$. Also, since the output

filter inductance is large, we consider the inductor as a current source I_o. Then the converter operation in one switching cycle can be identified as four switching periods, as shown in Fig. 5-12. To keep generality, we use m to stand for the number of stages of the switched-capacitor network in the following description.

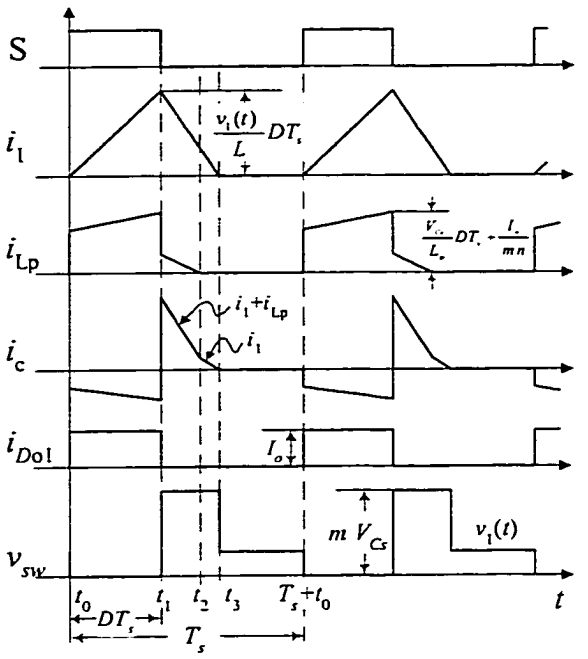


Figure 5-12 Steady-state key waveforms of the low-voltage AC/DC converter

Switching Period 1 (t_0-t_1):

This period begins when the power switch is turned on at t = t_0. With the input inductor L being connected to the line voltage, i_L increases linearly, drawing energy from the line. Meanwhile, closed by the power switch, each primary branch forms an individual loop resulting in the capacitor voltages being applied to each primary winding. Figure 5-13(a) shows the conduction path in this period. Energy stored in the capacitors is transferred to the load through the output forward transformer. The key waveforms are dominated by the following equations:

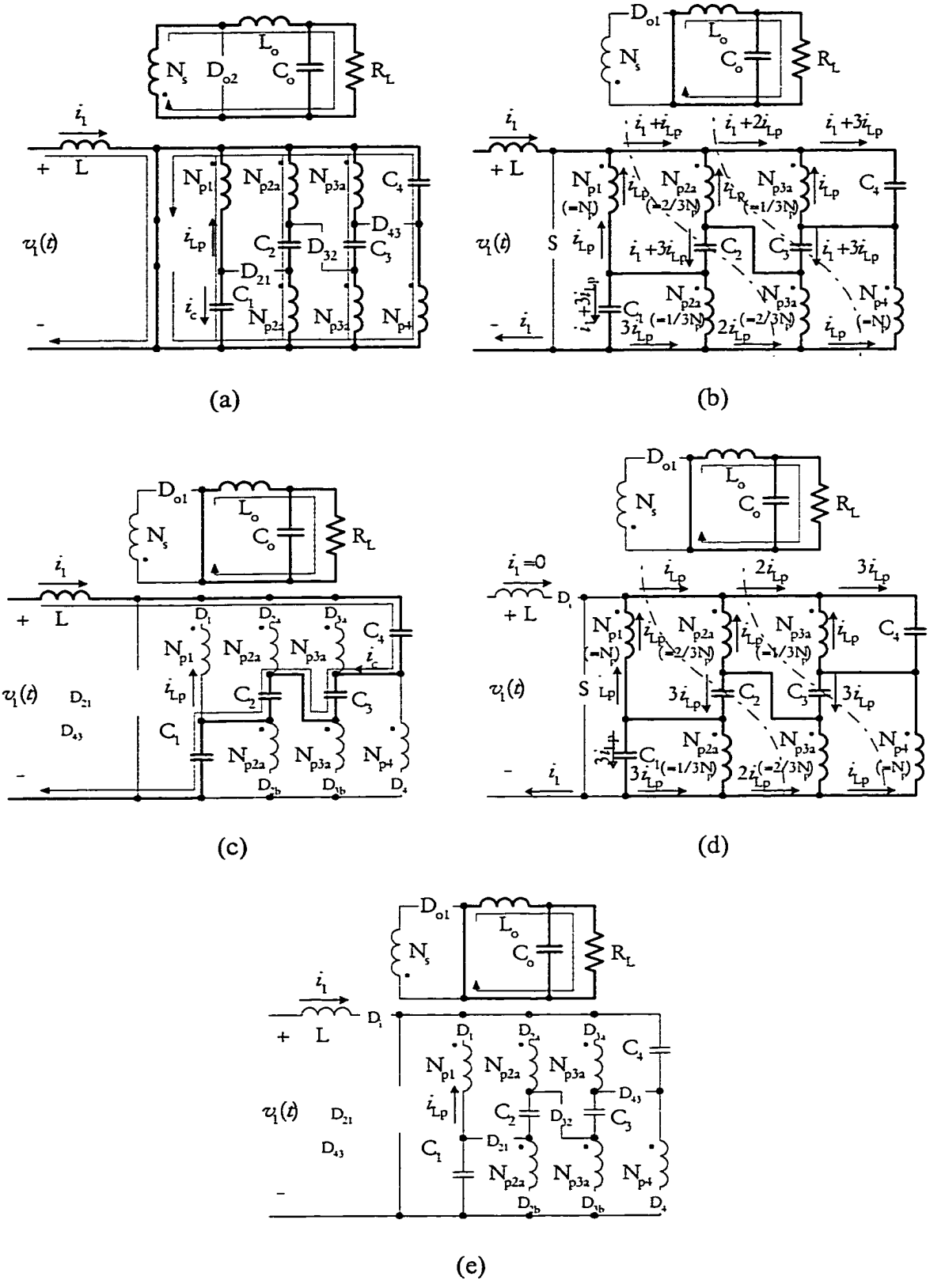


Figure 5-13 Conduction paths for the four switching periods: (a) P1(t_0-t_1); (b) P2(t_1-t_2); (c) P3(t_2-t_3); (d) P3'(t_2-t_3); (e) P4(t_3 - T_s+t_0)

$$i_1(t)=\frac{v_1(t)}{L}t; \tag{5.26}$$

$$i_{Lp}(t) = \frac{I_o}{m\,n} + \frac{V_{Cs}}{L_p}t;$$

$$i_c(t) = -i_{Lp}(t);\ i_{Do1}(t) = I_o;\ v_{sw}(t) = 0.$$

Where L_p is the total magnetizing inductance for each branch winding.

Switching Period 2 (t_1-t_2):

With the power switch being turned off at $t = t_1$, diodes D_{43}, D_{32} and D_{21} turn on. Because the primary windings N_{p1} (=N_p), N_{p2a} (=2/3N_p) and N_{p3a} (=1/3N_p) are connected to $3V_{Cs}$, $2V_{Cs}$ and V_{Cs}, respectively, and the primary windings N_{p2b} (=1/3N_p), N_{p3b} (=2/3N_p) and N_{p4} (=N_p) are connected to V_{Cs}, $2V_{Cs}$ and $3V_{Cs}$, respectively, all the primary winding currents are equal. The cut sets in Fig. 5-13(b) demonstrates that the four storage capacitors have the same amount of charging current $i_1 + 3i_{Lp}$. At the output stage, since the rectifier diode D_{o1} is reverse-biased, the output current I_o is continued through diode D_{o2}. During this switching period, the key waveforms are described by the following expressions:

$$i_1(t)=\frac{v_1}{L}\,DT_s - \frac{1}{L}(mV_{Cs} - v_1)(t - DT_s); \tag{5.27}$$

$$i_{Lp}(t)=\frac{V_{Cs}}{L_p}DT_s - \frac{(m-1)V_{Cs}}{L_p}(t - DT_s);$$

$$i_c(t) = i_1 + (m-1)i_{Lp};$$

$$i_{Do}(t) = 0;\ v_{sw}(t) = mV_{Cs}.$$

Switching Period 3 (t_2-t_3):

This is a continuous charging period. Depending on the line voltage $v_1(t)$, two operation modes can occur:

Mode 1 ($v_1(t) > V_{Cs}$): It can be shown that in this case, the transformer magnetizing inductor currents reach zero earlier than the input inductor current does in switching period 2. Therefore, switching period 3 refers to continuous demagnetizing of the input inductor. The conduction paths for this mode are shown in Fig. 5-13(c). The waveform equations are the same as those in period 2 except that $i_{Lp}(t) = 0$.

Mode 2 ($v_1(t) < V_{Cs}$): The input inductor was demagnetized before the transformer magnetizing currents decrease to zero. The current paths are depicted in Fig. 5-13(d). All the waveform expressions in Period 2 are valid for this period except using $i_1(t) = 0$ instead.

Switching Period 4 (t_3 - T_s+t_0):

Both the input inductor and the forward transformer have been demagnetized. The switch voltage takes the higher voltage between $v_1(t)$ and V_{Cs}. (Practically the switch voltage **tends** to be the higher voltage due to the existence of output capacitance of the switch.) When the power switch is turned on again, a new cycle begins. The key waveforms in this period are given by,

$$i_1(t) = 0;\ i_{Lp}(t) = 0;\ i_c(t) = 0;\ i_{Do}(t) = 0; \tag{5.28}$$

$$v_{sw}(t) = \begin{cases} v_1 & v_1 > V_{Cs} \\ V_{Cs} & V_{Cs} > v_1 \end{cases}.$$

5.3.3 Steady-State Analysis

5.3.3.1 Output to storage capacitor voltage ratio

The storage capacitor voltage plays very important role in the circuit operation, power factor correction and components selection. To find the relationship between the storage capacitor voltage and circuit parameters, let's define output to storage capacitor voltage ratio as,

$$M_1 \triangleq \frac{V_o}{V_{Cs}} \tag{5.29}$$

Considering volt-second balance at the output filter inductor L_o, we have,

$$\left(V_{Cs}/n - V_o\right) D T_s = V_o \left(1 - D\right) T_s$$

which leads to

$$M_1 = \frac{D}{n}, \tag{5.30}$$

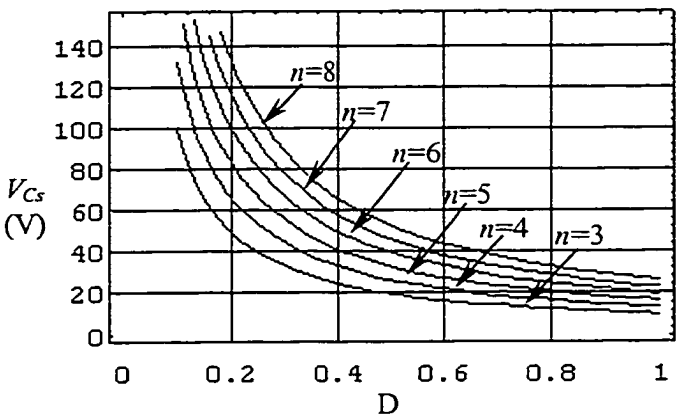


Figure 5-14 Storage capacitor voltage vs. duty ratio

or $$V_{Cs}^{\cdot} = \frac{n}{D} V_o . \tag{5.31}$$

As it can be seen, the storage capacitor voltage strongly depends on the duty ratio and transformer turn ratio. Figure 5-14 shows the storage capacitor voltages under different transformer turn ratios.

5.3.3.2 AC/DC conversion ratio

In order to find the AC/DC conversion ratio, let's first calculate the line current. Because there exists a line filter in front of the input stage (not shown in Fig. 5-11), the line current at each switching cycle can be approximated by the average value of the converter input current over switching cycle. By inspecting the current waveform $i_l(t)$, we found the absolute value of line current as

$$\left| i_l(t) \right| = \frac{D^2 T_s}{2 L} \frac{m V_{Cs} v_1(t)}{m V_{Cs} - v_1(t)} . \tag{5.32}$$

Equation (5.32) shows that the maximum line current $I_{l,max}$ occurs when the input voltage $v_l(t)$ equals to the maximum line voltage $V_{l,max}$, i.e., at $v_l(t) = V_{l,max}$, we get,

$$I_{l,\max} = \frac{D^2 T_s}{2 L} \frac{m V_{Cs} V_{l,\max}}{m V_{Cs} - V_{l,\max}} . \tag{5.33}$$

Since the converter operates under high input power factor, it is reasonable to assume the line current a sinusoidal one. Thus, we can use $I_{l,\max} = \sqrt{2}\, I_{l,rms}$ to fine the rms value of line current:

$$I_{l.rms} = \frac{D^2 T_s}{2\ L} \frac{m V_{Cs} V_{l.rms}}{m V_{Cs} - \sqrt{2}\ V_{l.rms}}. \tag{5.34}$$

Having obtained the effective line current, Eq. (5.34), we can solve for the conversion ratio from the power balance equation. For an ideal power stage, we have

$$V_{l.rms} \cdot I_{l.rms} = V_o^2 / R. \tag{5.35}$$

Then the conversion ratio is given by

$$M = \frac{D}{\sqrt{2}\, n\, m} \left(1 + \sqrt{1 + \frac{n^2 m^2}{\tau_n}} \right) \tag{5.36}$$

where

$$\tau_n = \frac{\tau}{T_s} \text{ and } \tau = \frac{L}{R} \tag{5.37}$$

are normalized load time constant and load time constant, respectively.

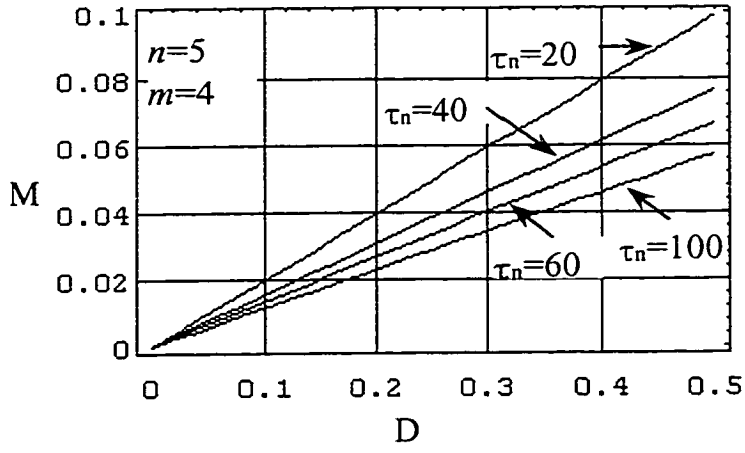


Figure 5-15 AC/DC conversion ratio vs. duty ratio

Equation (5.36) shows that to decrease the conversion ratio, we can raise the product of m and n. By plotting Eq. (5.36), we obtain a chart for conversion ratio vs. duty ratio under τ_n = 20, 40, 60, 100, as shown in Fig. 5-15. For an AC110V to 3.3V converter, M=0.03. If we select mn=20(e.g., m=4, n=5), the estimated duty ratio range is from 0.15 to 0.28 for the load change form 10Watts to 50Watts (τ_n = 20 to 100, L=450μH, f_s=50kHz). The control circuit can easily manage such duty ratio variation.

5.3.3.3 Limit duty ratio and regulation capabilities

The regulation capabilities of the proposed converter depend on the conversion characteristic given by Eq. (5.36) as well as its available duty ratio range. To achieve high input power factor, the input inductor L must operate in DCM. Referring to the waveform $i_1(t)$ given in Fig. 5-12, $t_3 < T_s$ must be satisfied, i.e.,

$$\frac{m V_{Cs} D T_s}{m V_{Cs} - v_1} < T_s . \tag{5.38}$$

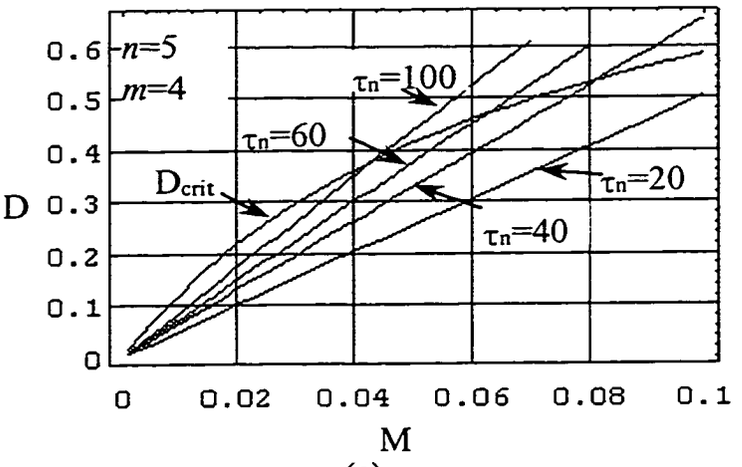
Derivation from Eq. (5.38) leads to,

$$D < D_{crit} = \frac{m n M}{\sqrt{2} + m n M} \tag{5.39}$$

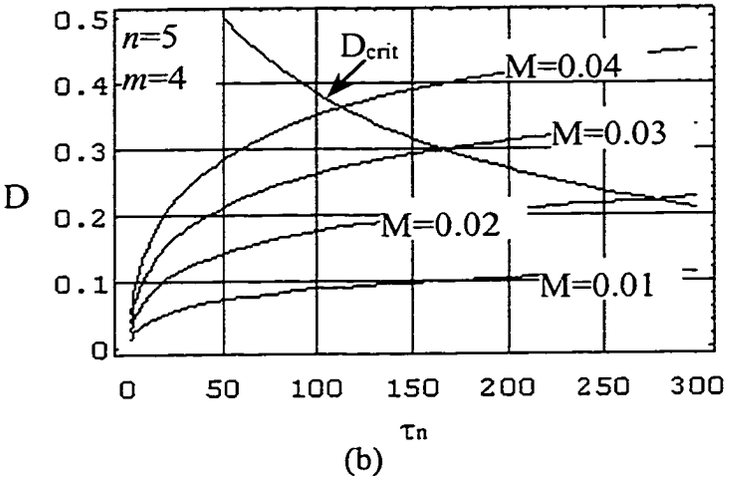
In order to inspect the regulation capabilities of the converter, we rewrite the conversion characteristic Eq. (5.36) as,

$$D = \frac{\sqrt{2}\, m n M}{1 + \sqrt{1 + m^2 n^2 / \tau_n}} . \tag{5.40}$$

Two plots can be generated from Eqs. (5.39) and (5.40). Figure 5-16(a) represents line regulation capability by giving available duty ratio range with conversion ratio M changing for a given load τ_n, while the load regulation capability can be anticipated by Fig. 5-16(b) through changing load τ_n for the given ratio M.



(a)



(b)

Figure 5-16 Regulation capabilities of the proposed converter:
(a) line regulation; (b) load regulation

5.3.3.4 Critical input inductance and output voltage ripple

Proper design of input inductor should be made such that when the peak of line voltage occurs, the inductor still operates in DCM. Suppose the inductor operates in CrCM at peak line voltage, the peak current of input inductor is given by,

$$I_{l.max} = \frac{V_{l.max}}{L} D T_s .$$

Therefore, by calculating the average inductor current at the peak line voltage, the maximum line current is found as,

$$I_{l.max} = \frac{V_{l.rms}}{\sqrt{2}\, L} D T_s . \tag{5.41}$$

Applying Eq. (5.41) to power balance equation, $I_{l,rms}\, V_{l,rms} = V_o^2/R$, we obtain,

$$L_{crit} = \frac{D_{crit}\, T_s\, R}{2 M^2} = \frac{m\, n\, R\, T_s}{2 M \left(m\, n\, M + \sqrt{2} \right)} . \tag{5.42}$$

The output ripple of the proposed converter is the same as that of a buck converter, which is given by,

$$\frac{\Delta V_o}{V_o} = \frac{1 - D}{8 L_o\, C_o\, f_s^2} \tag{5.43}$$

5.3.4 Design Example

Specifications:

Nominal input voltage: $V_{l,rms}$ = 110V@60Hz;

Output voltage: $V_o = 3.3V \pm 0.5\%$;

Nominal output power: $P_{o,nom} = 30W$;

Output power range: 10W-50W;

Switching frequency: $f_s = 50kHz$.

Design:

To compromise among circuit complexity (stage of switched-capacitor network), transformer turn ratio and duty ratio, we set transformer ratio n = 5 and stage number of SC network m = 4. The conversion ratio is $M = V_o/V_{I,rms} = 0.03$. Then the critical input inductance can be computed according to Eq. (5.42):

$$L_{crit} = \frac{m\,n\,R_{\min}\,T_s}{2M\left(m\,n\,M+\sqrt{2}\right)} = \frac{4\times5\times0.2179\times20\times10^{-6}}{2\times0.03\times\left(4\times5\times0.03+\sqrt{2}\right)}$$

$$= 721.2\mu H.$$

Set $L = 450\mu H$.

Based on the above values, normalized load time constant, duty ratio and storage capacitor voltage under different output power are calculated and the results are listed in Table 5-1.

Table 5-1 Calculated circuit parameters

Output Power	$R = V_o^2/P_o$	τ_n (Eq.(13))	D (Eq.(16))	V_{Cs} (Eq.(6))
10W	1.089Ω	20.66	0.154	107.2V
30W	0.363Ω	62.0	0.228	72.5V
50W	0.218Ω	103.26	0.265	62.4V

According to Eq. (5.43), the LC product can be found:

$$L_oC_o = \frac{1-D}{8f_s^2\,\Delta V_o/V_o} = \frac{1-0.228}{8\times\left(50\times10^3\right)^2\times0.5\%} = 7.725\times10^{-9}.$$

Set $C_o = 100\mu F$ and $L_o = 80\mu H$.

In order to design the storage capacitors, we set capacitor voltage drop tolerance for one line cycle missing. Presume that voltage drop of ζV_{Cs} on the storage capacitor occurs due to one line cycle, the correspond storage capacitance is given by,

$$C_s = \frac{2D^2 T_l}{m n^2 R \zeta (2-\zeta)} \quad . \tag{5.44}$$

For example, for ζ = 0.1, we need storage capacitance Cs = 251μF. We may set Cs = 300μF/150V.

5.3.5 Simulation and Experimental Verifications

The above design example converter was simulated on Pspice software package. Figure 5-17(a) shows the simulated input current waveform over one line cycle. The detailed input inductor current and voltage across the switch are shown in Fig. 5-17(b). It can be seen that the envelope of the input current follows the sinusoidal line voltage, implying high power factor at the line side through the line filter. At the output, 3.3V DC voltage is obtained on a 0.45Ω resistor (about 25Watts).

An example 15W~50W 50kHz converter was built in laboratory. The experimental prototype was designed with 4-stage switched-capacitor network (m=4). The transformer turn-ratio n = 5 was selected. In the construction of the prototype, the following components were used:

Input choke L: 450μH, MPP core
Diodes D_i, D_{21}, D_{32} and D_{43}: MUR840
Diodes D_1, D_{2a}, D_{2b}, D_{3a}, D_{3b} and D_4: EGP50GL
Main switch S: IRFP460
Output rectifier switches S_{o1} and S_{o2}: F1010N

Forward transformer T: Philips 3C85 ETD-PST39

Storage capacitor C_1, C_2, C_3 and C_4: 390μF/180V

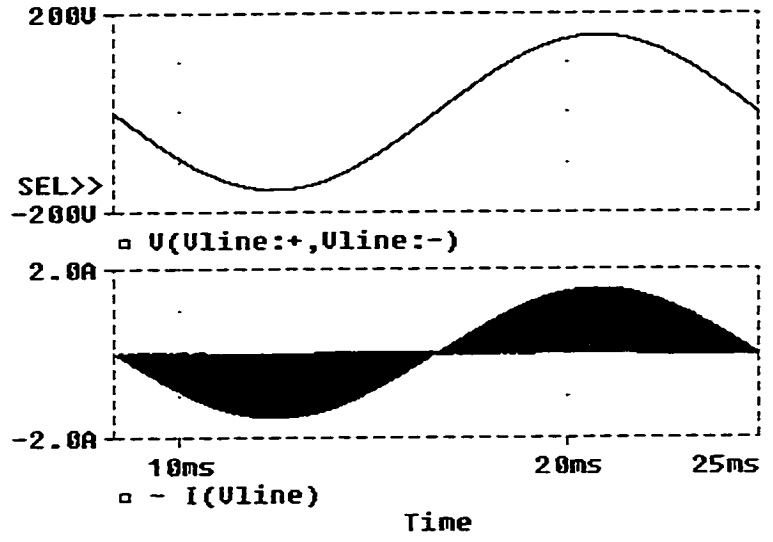
Output capacitor C_o: 470μF/10V

Output inductor L_o: 100μH, MPP core

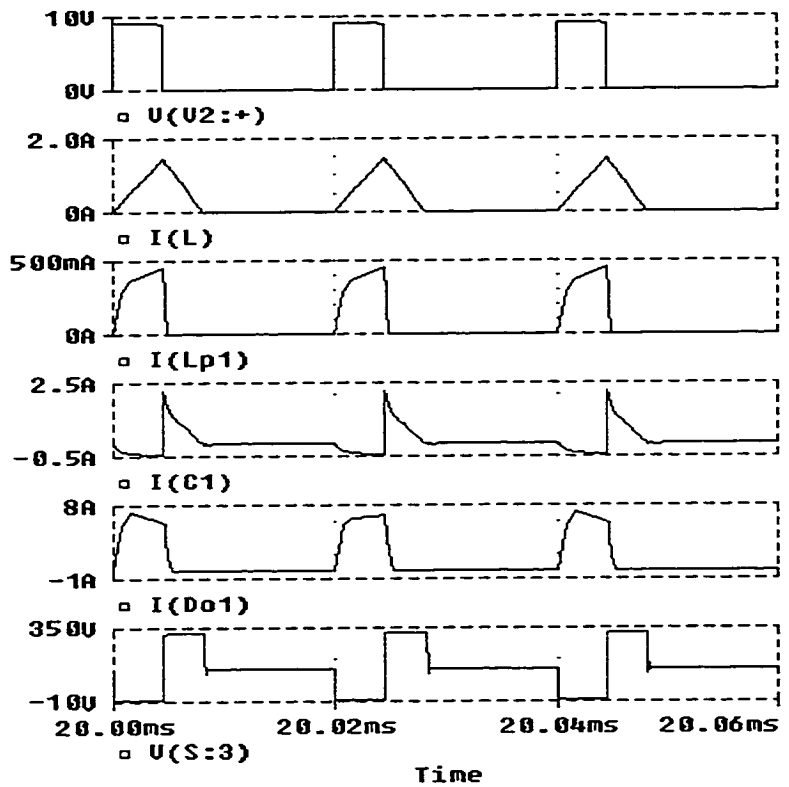
PWM IC chip: UC3525A

Experimental waveforms were recorded by hp54542A oscilloscope. Figure 5-18 shows the filtered input current waveform over line cycle. It can be seen that the input current follows the sinusoidal line voltage very well, implying high power factor at the line side. The detailed input inductor current, drain to source switch voltage and switch current are shown in Fig. 5-19. The waveforms were recorded at the peak line voltage. It can be seen that the waveforms agree very well with the theoretical waveforms and the simulated waveforms.

In the experiment, ±20% line voltage variation at 110VAC was considered. Under different load currents, input power factor and efficiency were measured and the measurements were plotted in Figs. 5-20 and 5-21, respectively. The measured power factor at 16A load constantly maintains above 98.5%. At light load, the power factor decreased to 97% when the line voltage increased to 135V. The measured overall efficiency of the experimental prototype is around 75% at heavy load. At light load, the efficiency is more sensitive to the line voltage change. The bulk storage capacitor voltage was also monitored in the experiment. Figure 5-22 gives the plot of the capacitor voltage comparing with the theoretical calculation result at 12A output current. Since the converter belongs to DCM-CCM type, the capacitor voltage increases with the load becoming light.



(a)



(b)

Figure 5-17 Simulation waveforms of the low-voltage AC/DC converter: (a) line current comparing with the line voltage; (b) switching waveforms

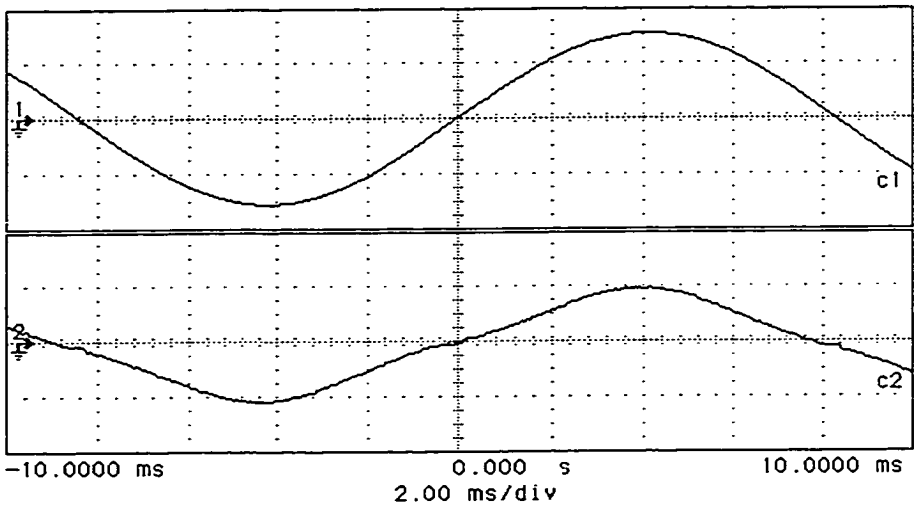


Figure 5-18 Experimental line voltage (upper, 100V/div.) and line current (lower, 1A/div.) waveforms

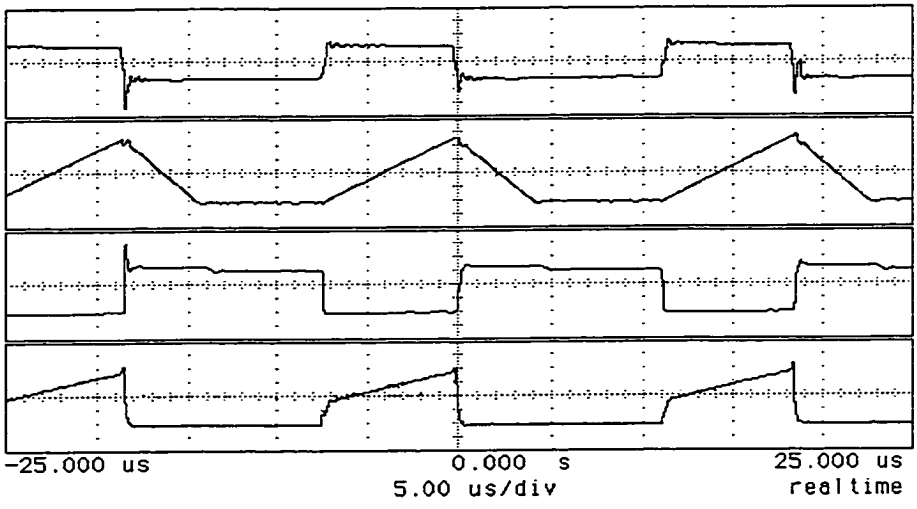


Figure 5-19 Experimental waveforms under 110VAC input and 8A output (from top, trace1: gate signal for the power switch; trace2: input inductor current, 2A/div.; trace3: drain-source voltage of power switch, 400V/div.; trace4: drain current of power switch, 4A/div.)

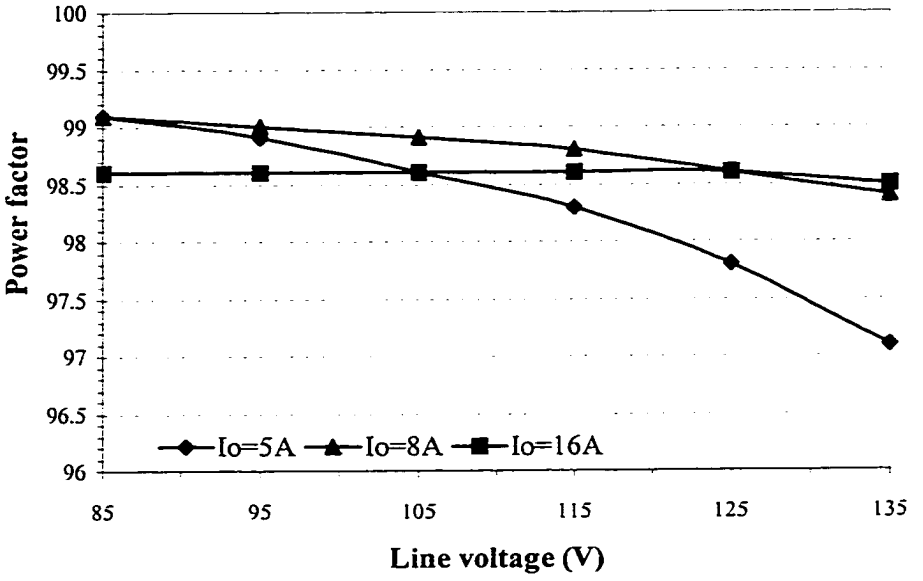


Figure 5-20 Measured power factor of the AC/DC 3.3V converter

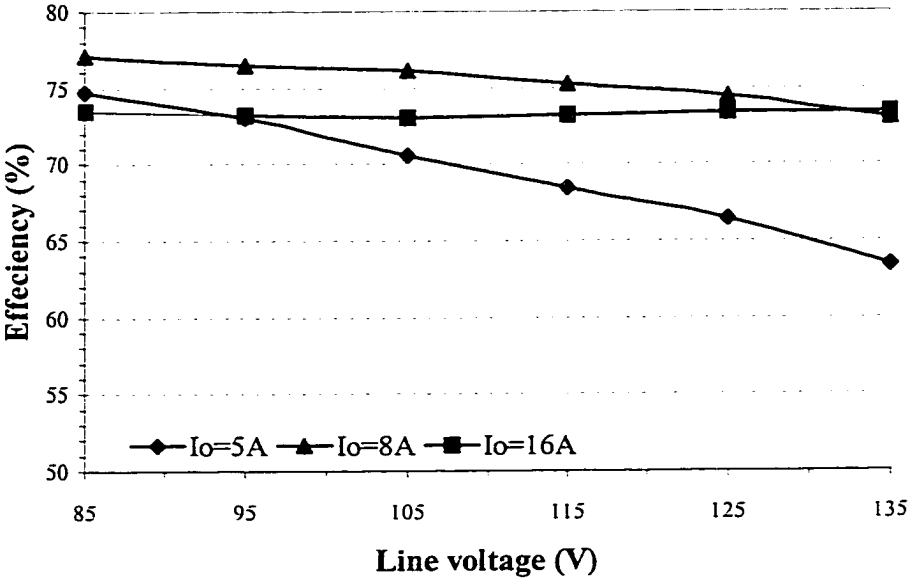


Figure 5-21 Measured efficiency of the AC/DC 3.3V converter

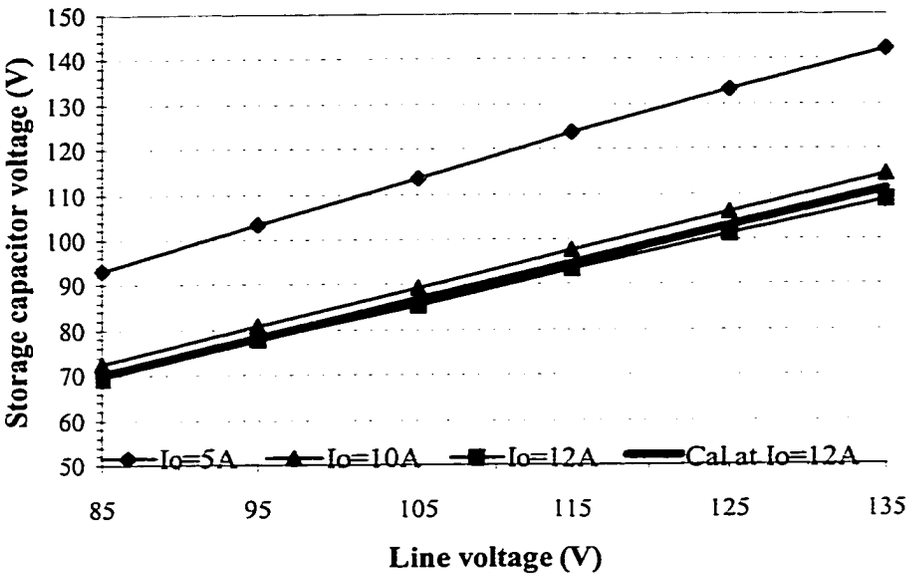


Figure 5-22 Measured storage capacitor voltage comparing with calculation at I_o=12A

5.4 SUMMARY

A single-stage power factor correction converter with soft-switching is proposed in this chapter. By introducing resonant modes to the two-capacitor converter presented in Chapter 4, zero-voltage-switching for the main switch and zero-current-switching for the auxiliary switch are obtained. As a result, high switching losses have been relieved so that the proposed single-stage power factor correction converter can operate in high-frequency with smaller size magnetic components.

By generalize the structure of the two-capacitor converter to n-capacitor network, new AC/DC converter topology with large conversion ratio is derived. The low output voltage is suitable for integrated circuit application. Also the proposed converter provides near unity power factor. The switched-capacitor network inserted in between the input boost circuit and the output forward circuit is able to split the bus voltage into low level,

which can be handled by lower turn ratio of the forward transformer. The input stage, switched-capacitor step-down stage and output stage share the same power switch, resulting in higher efficiency, low cost and high power density.

CHAPTER 6

CONCLUSIONS

The advanced semiconductor technology enables power electronic systems to interface wide range of electrical and electronic consumer. The massive use of low power factor power electronic systems impacts the utility quality by injecting harmonic currents. The treatment, i.e. power factor correction or harmonic reduction, has been always accompanied by the challenge in cost effectiveness.

Generally to say, performing AC/DC power conversion with power factor correction is to buffer the power flow from the line in AC form to load in DC form. It is difficult to achieve this by passive method since none of the storage component can completely buffer (compensate) the unbalanced power flow at line frequency. Therefore the expectation for the solution has been placed on active method. At high-frequency, i.e. by active method, it is possible to "correct" the input current waveform cycle by cycle. As a result, the active method can buffer the power flow much well than the passive method could. Research on active power factor correction has been concentrated on two fundamental technologies: control technology and circuit topology technology. However, analysis and design optimization of the active power factor correction circuits are also difficult issues to be resolved since the operation is a high-frequency one riding on the fundamental frequency.

This dissertation mainly emphasizes on the circuit topology technology. Analysis and design issues are also tackled. The general principle of power factor correction has been studied systematically. Some new methods for analysis and design of AC/DC single-switch single-stage converter have been proposed. Based on the review of recent techniques in single-phase active power factor correction, new types of AC/DC single-stage single-switch converter topologies have been proposed. Variation versions of one of the new converters have been developed for specific applications.

The original contributions of this dissertation are summarized as follows:

[1]. Development of new theories to analyze AC/DC converters.

a) For basic converters operating in CCM, PWM switch model can be applied. Converter transfer function and impedance refer to each basic converter topology can be obtained based on large signal equivalent circuit. By properly design control circuit, the converter impedance can be controlled to approach a constant resistance in steady-state. For basic converter operating in DCM, input I-V characteristic curve can be employed to investigate input power factor correction capability.

b) A general method, namely, "approximated rms method", to determine AC/DC conversion ratio for S^4 converter has been proposed. Comparing with the existing "DC substitution method", the proposed method has better accuracy at light load and/or high duty ratio operation.

c) A unified approach to analyze the line and load regulation capabilities of an AC/DC DCM input converter has been proposed. "Peak critical mode" (PCrM) operation was defined. The maximum operation duty ratio D_{max} is determined by looking for the

intersection of DCM operation and PCrM operation. This analysis approach provides power supply designer a convenient way to optimize converter design.

[2]. Development of new type of S^4 converter topologies to reduce bulk capacitor voltage:

a) By combining flyback circuit and forward circuit, an S^4 converter topology is derived. Due to the excellent power factor correction capability of flyback circuit when operating in DCM, the proposed converter operates in unity power factor. The storage capacitor voltage can be suppressed within low level by design.

b) Another S^4 converter topology is a combination of boost circuit and forward circuit. The unique feature of this converter topology is that it uses two bulk capacitors to split the bus voltage. Therefore the voltage stress on each capacitor is half of the bus voltage, resulting in low cost design. Since this topology belongs to a DCM-DCM combination, the capacitor voltages are independent of the load change. When the operation duty ratio larger than 0.2, the capacitor voltage mainly depends on the output voltage. Thus, universal input application can be easily realized by the proposed topology. Another advantage of this topology is that no additional demagnetizing winding is needed for the forward circuit. The leakage inductances of the forward transformer become parts of the circuit operation parameters. The voltage stress on the switch is automatically clamped at the bus voltage, resulting in significant improvement in conversion efficiency.

[3]. Development of single-stage converters for particular applications:

a) By introducing a resonant tank, the above two-capacitor converter has been developed into a high-frequency soft-switching one. The high switching frequency

operation of this converter implies small size and light weight. Increase in cost for such kind of power supply is unavoidable because of the introduction of additional components and selection of high-frequency transformer core. It is this payment that brings us the high power density.

b) The structure of configuring the two-capacitor S^4 converter can be generalized as insertion of an n-stage step-down switched-capacitor network between the input and output circuits. For low-voltage application, more stages of switched-capacitor network can be considered. The benefit from doing so is that we can overcome the difficulty in the design of high turn ratio transformer and use low price bulk capacitors.

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