FLYBOOST DERIVED SINGLE STAGE POWER FACTOR CORRECTION CONVERTER

By

WEIHONG QIU
B.S. University of Xiangtan, 1991
M.S. University of Nanjing Aeronautics & Astronautics, 1994

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer science
at the University of Central Florida
Orlando, Florida

Summer Term
2003

Major professor: Issa Batarseh

ABSTRACT

Power Factor Correction (PFC) scheme is necessary for lots of electric equipment with AC input as power source to meet the harmonic requirement of several standards. By integrating a PFC cell with a DC-DC conversion cell, single stage PFC scheme is attractive to low power application because of its low component count and low cost. But, typical single stage PFC converters suffer from high voltage and high current stresses, which block their way to practical applications.

Flyboost-derived single stage PFC converter can transfer input power directly to output end with portion of input power proceeded by the active switch only once. And the intermediate bus voltage is also automatically limited to specific value determined by circuit parameters. So this scheme can reduce the voltage and current stresses on power components, and better performance can be achieved with low cost.

Lots of single-stage PFC converter schemes can be derived by integrating flyboost PFC circuit with basic DC-DC conversion circuits. Two good topologies were studies in detail to show advantages of this scheme. The operations of those topologies were discussed, and power flow analysis approach was implemented to obtain critical equations for practical design. Optimal design procedure was developed and verified by prototypes and experiments. Experimental results show their superiorities over counterpart single-stage PFC schemes. Low components count and good performance makes them suitable for low power low cost universal input application.

Considering the influence of leakage inductance of flyback transformer, the operation of non-ideal flyback circuit is very complex due to its several operational modes. Based on detailed operation analyses, one unified average Pspice model was developed for non-ideal flyback circuit, which is also suitable for flyboost PFC scheme. By combining this average model with average models of basic DC-DC converters, the average model for flyboost-derived single stage PFC converters were developed. This average model can reduce the total simulation time significantly. And one special simulation procedure was developed to perform AC small signal analysis for flyboost-derived PFC topologies. Simulation results show special characteristics of flyboost-derived topologies, which provide design guide for practical applications.

TO MY GRANDFATHER

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor, Dr. Issa Batarseh, for his guidance, inspiration and support during the course of this work. I would not have been able to complete my research without his extensive knowledge and creative thoughts. Through his enthusiasm and personality, he also gained my most sincere admiration.

I also thank many of my collegues at UCF, Dr. Shiguo Luo, Dr. Wei Gu, and Dr. Wenkai Wu, Dr. Chris Iannello, Dr. Peter Kornetzky and Dr. Zaki Moussaoui for many enlightening discussions; Their invaluable suggestions were so helpful to my research.

My experience at UCF has been a great period in my life. I am grateful to have the chance to combine enjoyable education and productive research atmosphere through the dynamic group at UCF. I wish to thank my fellow researchers, Dr. Hong Mao, Khalid Krustom, Songquan Deng, Jia Luo, Jaber Abu Qahouq, Nattorn Pongratananukul, Enrique Tenicela, Joy Mazumdar and Duy Bui Quang for their help and cooperation.

And I would like to express my deep appreciation to Ms. Elizabeth Plaisted for her invaluable editing work of my dissertation.

Finally, my heartfelt appreciation goes to my parents and my wife for their love.

This work has been supported by an NSF grant, a NASA STTR research grant, and the University of Central Florida.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

Power conversion system designs are becoming increasingly important in state-of-the-art electronics systems, especially in information system applications. Poor power quality in many power conversion systems has caused many problems as mentioned in recent surveys and industrial reports. Power factor correction techniques, which can improve the power quality of power conversion system, have become an attractive alternative due to several regulations that have been effected recently.

Many Power Factor Correction (PFC) AC/DC converters schemes have been proposed in recent years. Classified by the system configurations, these techniques can be divided into two categories, two-stage and single-stage schemes. For low power applications, including electronic ballasts for fluorescent lamps, the single stage approach is especially attractive due to its simple power stage and control circuit. But there are some issues existing in the single stage PFC converter, such as high DC bus voltage, high current stress and voltage stress over main switch components. A lot of topologies were proposed to solve one or some of those issues in order to achieve better performance. Those approaches are surveyed in this chapter.

1.1 Background

The power converter is a necessary part in lots of electronic equipment to convert utility line voltage to a voltage suitable for other parts in the electronic equipment. In conventional power conversion systems, a simple rectifier bridge directly connected with a bulky capacitor is used. But this kind of topology draws pulsed current from the utility line with poor power factor, typically 0.6. In order to limit the influence of the power conversion system on utility line, some standards, including IEC 555, have specified requirements for harmonic contents in the line current drawn by the electronic equipment.

There are two different approaches for meeting those requirements: the passive power filter and the active Power Factor Correction (PFC) circuit. Although they can achieve high efficiency, passive power filter are not commonly used due to their bulky size and weight. They can be found in some applications where there is a very strict EMI requirement. However, the active power factor correction circuit has drawn a lot of attention due to its high performance and compact size. Many products that use an active PFC circuit have appeared in the market recently.

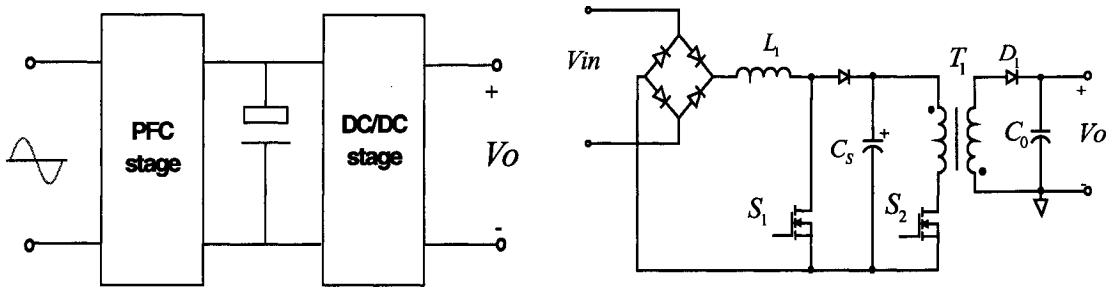
In this chapter, conventional technologies of the active PFC converter are reviewed. Some common issues in single stage power factor correction circuit are discussed, and some available solutions are provided.

1.1.1 Conventional Power Factor Correction converter

In the past several years, many topologies and control approaches have been presented in the active PFC area. According to its topology, the active PFC converter can be divided into categories:

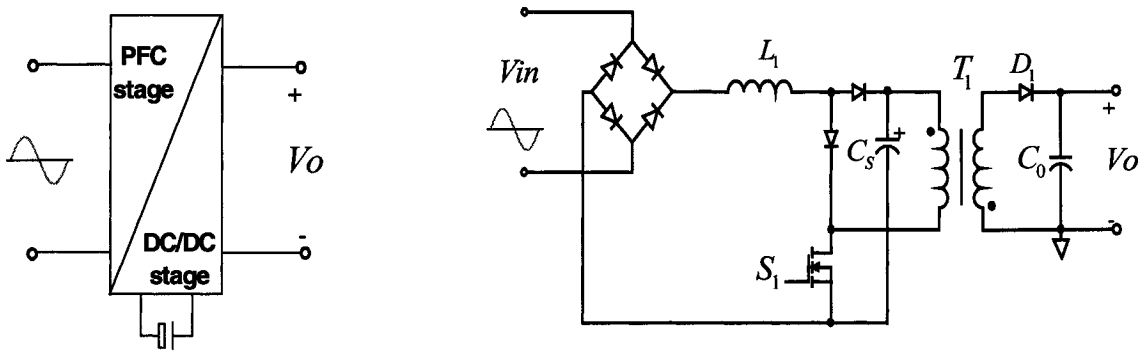
a. *Two-stage PFC converter*: Consists of a PFC stage and a DC/DC conversion stage. The PFC stage will convert the utility line voltage to a constant DC voltage with a high power factor. The DC/DC conversion stage will convert that constant DC voltage to the desired voltage with tight output voltage regulation. These two stages can be optimally designed since they operate independently. This approach is commonly used in high power applications. The scheme and typical topology are shown in Fig. 1-1; its advantages include superior performance and flexible design configuration, but its cost is high due to its complex configuration.

b. *Single stage PFC converter*: The PFC stage and DC/DC conversion stage in this approach are integrated into one stage with single controller and shared active switches. Normally the controller is designed to achieve only the tight output regulation, while a high power factor is achieved through specified topologies with automatically waveform shaping function, such as boost topology with constant duty cycle control. The single stage PFC converter is more attractive for low power applications because of its simple configuration and low cost. Here some deep researches will be conducted on it. The scheme and typical topology are shown in Fig. 1-2.



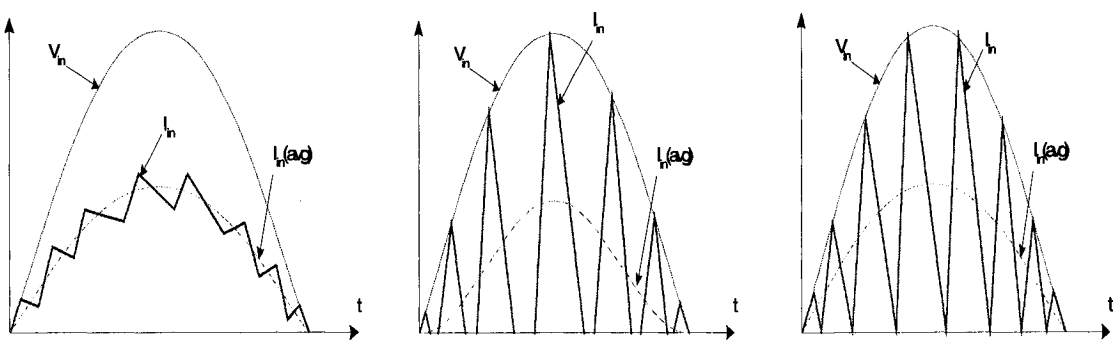
(a) Scheme (b) typical topology

Fig. 1-1 Two-stage PFC converter



(a) Scheme (b) typical topology

Fig. 1-2 Single stage PFC converter



(a) CCM (b) DCM (c) boundary mode

Fig. 1-3 Current waveform at different mode

PFC converter can be divided into three categories based on the conduction mode of PFC stage as shown in Fig. 1-3:

a. *Continuous Conduction Mode (CCM):* In this mode, the PFC stage runs at CCM. This approach is typically used in high power two stage PFC converter, since the current stress on the active switches is lowest. With specifically designed IC chips, a very high power factor can be achieved easily. CCM operation can be applied to the single stage PFC circuit as mentioned in [1], but the configuration and control method are too complicated and too high cost.

b. *Discontinuous Conduction Mode (DCM):* In this mode, the PFC stage runs at DCM. This method is commonly used in a single stage PFC converter, since it is easy to get high power factor for some topologies when constant duty cycle control is implemented. Although the current stress on the active switch is much higher than its counterpart at CCM and intermediate bus voltage is out of active control, it draws a lot of attention due to its simplicity and low cost.

c. *Boundary conduction mode*: This PFC stage runs at boundary conduction mode, the mode between CCM and DCM, which is when the new switching cycle begins once the line current reaches zero. With only a few components and simple control IC, this approach can achieve high performance without the diode reverse recovery problem that exists in CCM. This approach provides an excellent tradeoff between high performance and low cost, so it is common in low and medium power two stages PFC converters, such as in electronic ballast for fluorescent lamp applications.

1.1.2 Single stage Power Factor Correction converter

In this section, the research mainly focuses on the single stage PFC converter. The simplest single stage PFC converter uses the flyback converter directly. With simple configuration and control circuit, high power factor was achieved easily. Other familiar topologies, such as isolated Cuk and Sepic (without intermediate bulk capacitor), can also gain good power factor and the desired isolated output. Unfortunately, the main drawback of this kind of topology is the output voltage regulation. The high double-line-frequency ripple in output voltage limits the application of single stage converters.

In order to get tight regulation, an intermediate bus capacitor must be used since the input power will be pulsating when the power factor is unity. In [1], a family of single stage PFC topologies was achieved by integrating PFC cell and DC/DC cell with one controller and shared active switches. In this topology type, the PFC cell should have automatic waveform shaping function, which means that sinusoid input current waveform should be achieved without active control. As analyzed in [1], DCM boost topology under constant duty cycle control will generate sinusoid current waveform that follows the input voltage waveform. So the controller of this kind of topology will only need to be designed to maintain tight output regulation.

Many topologies, including DCM boost, buck-boost, and flyback, have the automatic waveform shaping function, as presented in [1-14]. All of those topologies can achieve high power factor under constant duty cycle control. Just integrated those PFC topologies with any other DC/DC topologies, many single stage power factor correction circuits can be achieved.

Although the previously mentioned approach is very simple and low cost, it is far from perfect: it suffers from high voltage stress, high current stress and high intermediate bus voltage. In order to relieve the circuit from those drawbacks, a lot of modified single stage topologies were presented with different features, as presented in [15], with different drawbacks. You have to make the tradeoff depending on your specified applications.

1.1.3 Key issues in single stage Power Factor Correction converter

The single stage PFC topologies are very simple and attractive for low cost application. However, this topology suffers from the following drawbacks:

a. High intermediate bus voltage. As discussed in [15], the high intermediate bus voltage in the simple single stage PFC circuit is unavoidable because this voltage is out of active control. Although intermediate bus voltage can be independent from the load condition by running both PFC cell and DC/DC cell at DCM, it must change widely in order to get power balance between input and output for universal voltage applications. The high voltage rating capacitor will increase the converter cost largely. Some modified topologies or control methods can eliminate those problems at a price of lower power factor or higher complexity. Those options will be discussed in the following section.

b. High voltage stress over active switch. High intermediate bus voltage brings high voltage stress on switch components. So high voltage rated components are required, resulting in high cost and low efficiency.

c. High current stress. Since topologies with automatically waveform shaping function always run at DCM, the current stress on active switches is much higher. These active switches in a typical single stage PFC circuit need to process all output power twice, which results in increased current stress also. Although single stage PFC converter may save one or more active switches, the processed power is same as two-stage PFC circuit. It is difficult to get high efficiency.

d. Complex configuration. Because PFC cell and DC/DC cell are integrated into one cell, it is difficult to get optimized design. It causes problems in the analysis of this kind of topology, as discussed in [15].

In next two sections, some solutions to above issues are discussed, and a family of PFC circuit with flyboost PFC cell is included also to show its features.

1.1.4 Intermediate bus voltage control

In two-stage PFC circuit, there is a separate controller to keep the intermediate bus voltage constant. So the DC/DC stage design can be optimized. While in single stage PFC circuit, the only control is to obtain tight output voltage regulation. There is no active control over the intermediate bus voltage, since both PFC cell and DC/DC cell share active switches and single control loop. As discussed in [15-19], the intermediate bus voltage is an important issue in single stage PFC circuit, because it determines the voltage rating of bulk capacitor and switch components.

As presented in [15], the typical equation for intermediate bus voltage of flyback + flyback PFC converter operating under DCM+DCM was presented as:

$$V_{Bus} = V_{in} * \sqrt{\frac{L_2}{2 * L_1}} \tag{1.1}$$

While at DCM+CCM operation, it equals:

$$V_{Bus} = \frac{1}{n}\left(V_{in}\sqrt{V_o / 4 f_s L_1 I_o} - V_o \right) \tag{1.2}$$

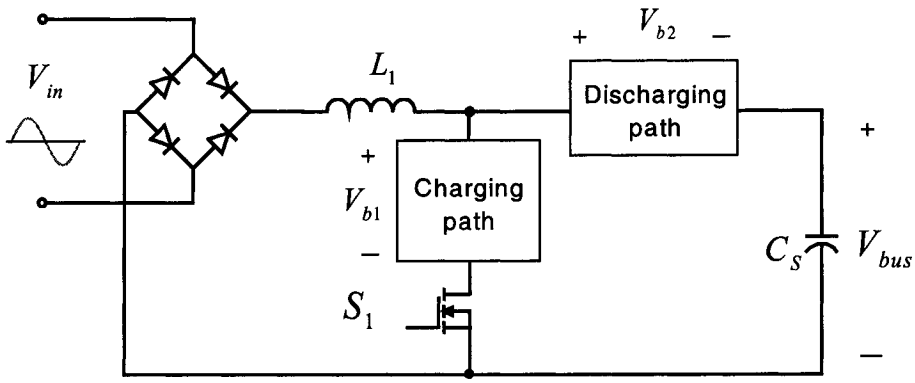
From the above equations, we have found that the intermediate bus voltage depends on circuit parameters, input voltage and load condition when DC/DC conversion cell operates under CCM. While DC/DC conversion cell operates under DCM, the voltage will only depend on parameters and input voltage. A very high intermediate bus voltage will be expected when DC/DC conversion cell operates under CCM at light load. There are some approaches that may eliminate these problems, such as varied frequency control. But its complexity and EMI issue make it impractical. So, in order to keep this voltage in reasonable range, both PFC and DC/DC cell should operate at DCM in simple PFC circuit, although it increases current stress over switch components. Through this method, the intermediate bus voltage will be independent of the load condition.

From the DCM+DCM equation, we find that the intermediate bus voltage will change linearly according to the input voltage without any relationship with load condition. For universal line voltage applications, it may cause many problems for circuit design, since the line voltage will change from 85Vrms to 265Vrms. The reason for such a high intermediate bus voltage is that the circuit needs to balance the input power and output at any load and line voltage condition, and also keep input inductor operating under DCM.

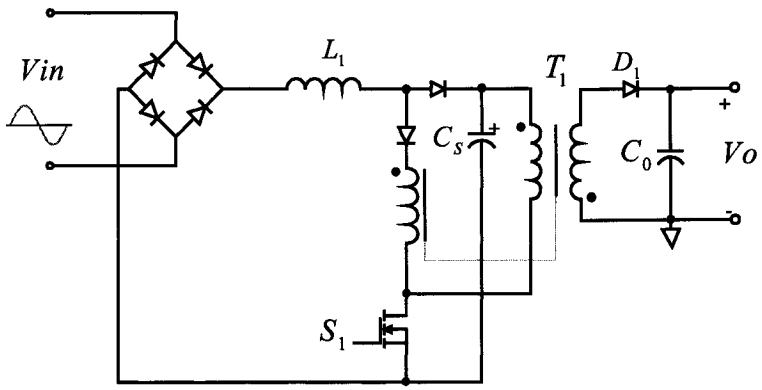
In order to limit the range of this voltage, several methods were presented in [14-19]. Good review of all methods was provided in [14]. The main concept of those approaches is to add a block cell in boost inductor charging or/and discharging path. Those blocks will transfer some power to output, reduce the effective charging voltage and/or increase effective discharging voltage across input inductor; so lower intermediate bus voltage can be expected.

From Fig. 1-4, the effective charging voltage across boost inductor L_1 during switch ON period is $V_{in}(t) - V_{b1}$, and discharging voltage during switch OFF period is $V_{bus}+V_{b2}-V_{in}(t)$. By adding two blocking voltage, the effective charging voltage reduces while effective discharging voltage increases. So lower intermediate bus voltage can keep PFC inductor under DCM. Bifred topology in [20-22] is also a good example of this concept, since there is a blocking cell located in boost inductor discharging path.

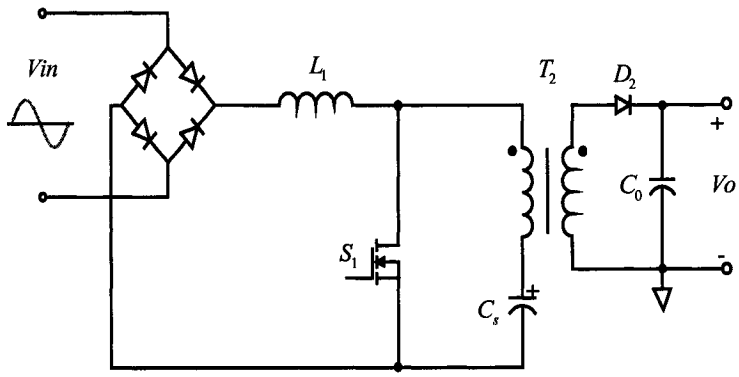
Typically, those blocking voltage is achieved by adding an extra winding to the main transformer, referred as magnetic switch or DC bus voltage feedback in [16-19]. Those windings will transfer some power directly to the output end and reduce the effective input power in one line cycle. So it breaks the original power balance across the intermediate bus capacitor and keeps the intermediate bus in a reasonable range. And another advantage of this concept is that the DC/DC cell can operate at CCM to reduce current stress on the switch component without punishment of high voltage stress at light load condition.



(a) Voltage blocking scheme



(b) Typical topology



(c) BIFRED

Fig. 1-4 blocking cell in boost inductor path to reduce intermediate bus voltage

But its disadvantage is also obvious: when the input voltage is less than V_{b1}, there will be no input current. So it will deteriorate the input current waveform and reduce power factor. And complex transformer configuration is another drawback. So the improvement is achieved at a price of performance deterioration.

In [23], another effective method, referred to flyboost PFC scheme, was proposed to reduce the voltage and current stress. By adding a winding to PFC inductor, the intermediate bus voltage is limited less than $V_{in} + n*V_o$. And DC/DC cell also can operate at CCM to reduce current stress. Based on the flyboost PFC scheme, a family of single stage PFC converter can be derived, as discussed in [23-29]. And implementing this concept to Bifred topology, the so-called Bi-Flyback topology in [29] will have even lower intermediate bus voltage. In following chapters, two typical flyboost-derived single stage PGC topologies are studied in detail.

1.1.5 Parallel power flow PFC converter

In order to get low cost high performance topology, voltage stress and current stress on power components should be as low as possible. High current stress means high current rating components, high cost and low efficiency. For a good topology, the current stress should be as less as possible under the condition of meeting all other requirements. Here, some solutions to reduce the current stress are discussed.

Firstly, the influence of operation mode is studied. DCM operation always means higher RMS value than CCM operation when the average value is same. So the best choice is to let the circuit operate at CCM. But, as mentioned in last section, most of single stage PFC circuit needs to operate at DCM+DCM (both cells at DCM) in order to

get high power factor and reasonable bus voltage range. So the current stress is pretty high in most single stage PFC circuit.

For PFC cell, classic single stage PFC topologies with automatically waveform shaping function require the inductor to operate under DCM in order to get high power factor. Some topologies can run at CCM still with good power factor. But the circuit configurations or/and it control method were too complex. There is no other good choice for simple low cost single stage PFC circuit. So PFC cell has to operate at DCM for low cost and simple circuit.

As for the DC/DC cell, operation at DCM is required just to limit the intermediate bus voltage range under different load condition. If there is another good way to disconnect the relationship between the intermediate bus voltage and load condition, DC/DC cell can run at CCM to reduce the current stress.

So a good operation mode for single stage PFC circuit is DCM+CCM, with an effective method limiting the intermediate bus voltage. The topologies presented in next two chapters are under DCM+CCM.

Secondarily, power flow in single stage PFC circuit is analyzed. Assume that both the input voltage and input current are sinusoid waveform and power factor is 1. Then the input power is equal to 2*Po*sin(2*w*t), as shown in Fig. 1-5. The input power is also sinusoid waveform. In order to get tight output voltage regulation, there should be a stored device to store energy of P1 in Fig. 1-5 when instantaneous Pin is higher than output power. Then the stored power is transferred to output when instantaneous input power is less than output power.

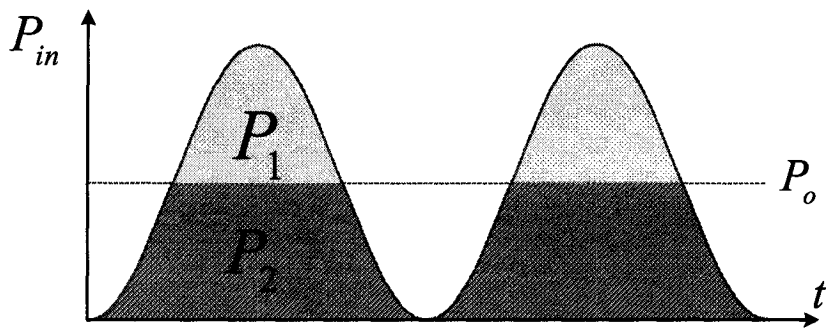


Fig. 1-5 input power waveform for unity power factor

Classic since single stage PFC circuit is just an integration of PFC cell and DC/DC cell in corresponding two-stage PFC cell, so the active switch needs to process all output power separately in the PFC cell and in DC/DC cell like in two-stage PFC converter. It means that active switch needs to process all output power twice: first convert input power to stored DC power, and then convert stored DC power to output power. Fig. 1-6 (a) and (b) shows the power flow in two-stage PFC circuit and single stage PFC circuit. The equation of efficiency of those circuits is same:

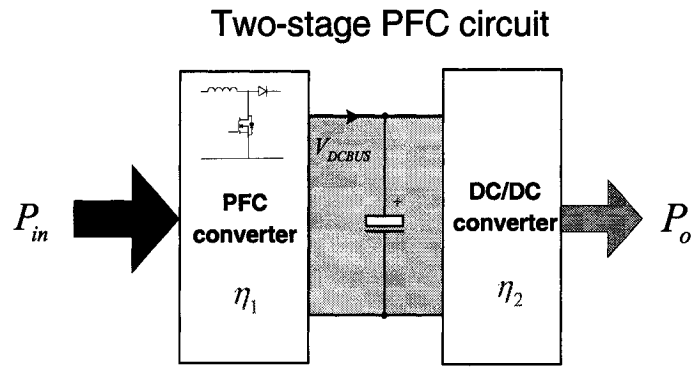
$$\eta = \eta_1 * \eta_2 \tag{1.3}$$

In each power processing, there are some power losses dissipated as heat. So the efficiency of the conversion system is low. If some power can be transferred to output direct through PFC cell, the power processed by DC/DC cell will be less, which means that the power losses in DC/DC cell can be reduced. This concept is shown in Fig. 1-6(c). The equation of efficiency of this concept is:

$$\eta = \eta_1 * \eta_2 + \eta_1 * k * (1 - \eta_2) \tag{1.4}$$

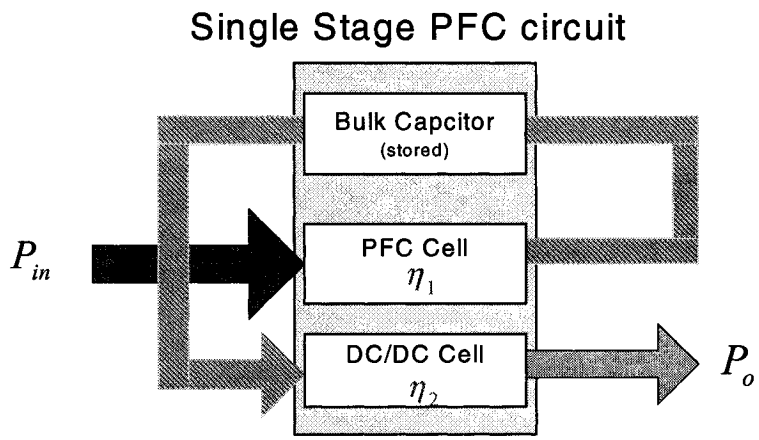
K is the ratio of direct transferred power versus whole power.

It is clear that the efficiency of this method is higher than conventional method. And the current stress is also reduced since the power processed in DC/DC cell is reduced. Now the issue is how many power should be directly transferred to output without deterioration to input current waveform, and how to do it.



$$P_o = P_{in} * \eta_1 * \eta_2$$

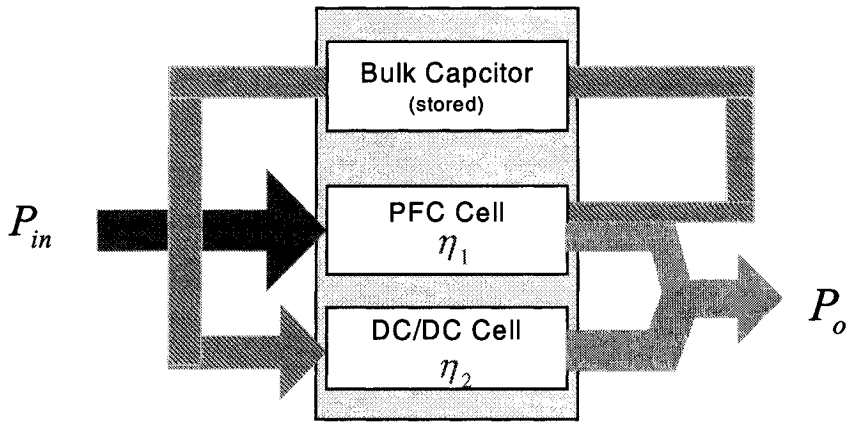
(a) Two-stage PFC



$$P_o = P_{in} * \eta_1 * \eta_2$$

$$\eta = \eta_1 * \eta_2$$

(b) Single stage PFC



$$P_o = P_{in} * \eta_1 * k + P_{in} * \eta_1 * \eta_2 * (1 - k)$$

$$\eta = \eta_1 * \eta_2 + \eta_1 * k * (1 - \eta_2)$$

(c) Single stage PFC with direct power transfer

Fig. 1-6 Power flow chart

In order to keep tight output voltage regulation, power transferred to output end should always be equal to load power at any time. In order to get high efficiency, the best way is to transfer all input power direct to output end when instantaneous input power is less than output power, and transfer extra power to output from intermediate bus capacitor, and transfer exact output power to output end directly and store extra power in intermediate bus capacitor. According to this idea, P2, in Fig. 1-5, can be transferred to output directly without influence to output voltage regulation. And P1 needs to be stored in bulk capacitor and transferred to output when P2 is less than Po. It is easy to calculate that P2 is 68% of Po, and P1 is 32% of Po. It means that 68% of output power is processed by active switch only once, and only 32% of output power is handled twice. The output power is processed 1.32 times by active switches, instead of 2 times in

conventional single stage PFC circuit. This method is the best method for single stage PFC circuit, as far as power processing is considered.

Since there are two power flow paths in the abovementioned concept, it is referred to "parallel power transfer" in [30-35]. Based on its operation features, it also is called "direct power transfer" in [23].

Based on this concept, some topologies were presented recently. In [30], by using two separate cells in primary side, exact value of P1 and P2 were transferred to output end. Although high efficiency was achieved, its complicated configuration is its main drawback.

In [31], this concept was applied to secondary side. Another independent DC/DC converter is added to conventional PFC circuit to store and transfer P1. High power factor and efficiency were reported. But the disadvantage is its complexity and high cost.

In [32], some simple topologies based on parallel power transfer concept were proposed. By properly merging two conventional topologies, those topologies also achieve parallel power transfer. Simple circuit and control was their advantage. But those topologies brought high current harmonic content that reduced the power factor. Although the power factor still met the regulations, it is not a good choice.

Basically, a lot of topologies in [14] with extra winding in boost loop to block charging/discharging voltage also have this function. In [33], a lot of parallel power transfer topologies were reviewed in detail.

By the way, parallel power transfer also means that it breaks the power balance across intermediate bus capacitor. So some topologies with parallel power transfer can also limit the intermediate bus voltage.

1.1.6 Average Model for switching mode power supply

In switching mode power supply design, the transfer function of the converter is important. Based on the transfer function, optimal compensation circuit can be designed to achieve better transient response. Due to its switching characteristics, the circuit configuration changes when the switch is ON or OFF. The power supply system is the non-linear time-variant system. So conventional linear control theory cannot be implemented to switching mode power supply design.

In switching mode power supply, there is one important feature that makes it different to other non-linear time-variant system. The time constant of the inductor and capacitor is much longer than the switching period. The L-C works like lower frequency filter for the system. Based on this characteristic, the averaging modeling concept was proposed to model the switching mode power supply system in [34]. The basic concept of the average modeling is to find out the averaged characteristics of the system in one switching cycle. Then the linear equivalent system is obtained by the small signal perturbation is applied around the steady state operation point. This linear equivalent can be used for the AC analysis of the switching mode power supply.

The average modeling was discussed in a lot of papers for different topologies, such as in [34-42]. For different topologies, one average model had to be derived. Then the PWM switch model in [35-37] provided one unified model just for the non-linear time-variant part of the power supply: the switch and diode. The model then was put back to the original circuit with all other parts, such as inductor and capacitor in the same position untouched. The PWM switch model is good for simulation. The Switch Inductor Model (SIM) in [38-40] implements one block to replace the inductor, the switch and

diode. One feature of SIM is its automatic mode transition. By limiting the maximum diode conduction time to (1-D)*Ts, the model works for CCM and DCM. It simplifies the simulation procedure.

The modeling for power factor correction converter is little different to the DC-DC converter. Average modeling concept can also applied here. In DC-DC converter, the averaging procedure is performed over one switching cycle. For PFC converter, the averaging procedure is over one line cycle, assumed that the control loop response very slow. In [41-45], the average modeling method for power factor correction converter was discussed.

Once the average model is developed, simulation software, such as Pspice, can be implemented to find the transfer function of the power supply. Pspice can perform bias point calculation to find out the steady state operation point, and then perform small signal AC analysis.

1.2 Dissertation Outline

The objective of dissertation is to study the flyboost derived single stage Power Factor Correction converters. By implementing direct power transfer, flyboost derived PFC schemes can achieve better performance comparing to other single stage PFC schemes. The operation and characteristics of this scheme was discussed in detail, and two typical examples were studies with experimental results. And practical design

procedure was proposed. The average model was developed and implemented to perform the AC small signal analysis of flyboost derived PFC converters.

The dissertation is organized into seven chapters as following:

Chapter 2 will discuss on the operation and features of the flyboost PFC cell by one simple example;

Chapter 3 focuses on the analysis and design of the flyboost-parallel/series forward single stage PFC converter;

Chapter 4 will discuss on the operation and characteristics of Bi-flyback single stage PFC converter;

Chapter 5 will focus on the control method for Bi-flyback PFC converter, and valley-switching control technique is discussed in detail;

Chapter 6 will discuss on the average modeling of the flyboost PFC cell and flyboost-derived single stage PFC converter;

Chapter 7 provides the conclusions of this dissertation.

CHAPTER 2

DIRECT POWER TRANSFER FLYBOOST PFC CELL

2.1 Introduction

One of common characteristics in conventional PFC cell topologies, such as Boost, buck-boost, and flyback topologies, is that there is only one power flow path. This means that the active switch must process all output power twice, as discussed in previous chapter. Some modified topologies can carry out direct power transfer function with higher efficiency and limited intermediate bus voltage, but input current waveform is deteriorated and power factor performance is lessened.

In [23], another approach was proposed to carry out this function with little influence on this current waveform. The main idea is to add an extra winding to input inductor to get another power flow path directly to output. Based on this concept, a PFC cell with direct power transfer was presented, called as flyboost in [23]. As shown in figure 2-1, Flyboost PFC cell consists of a boost converter with an additional winding added to the boost inductor.

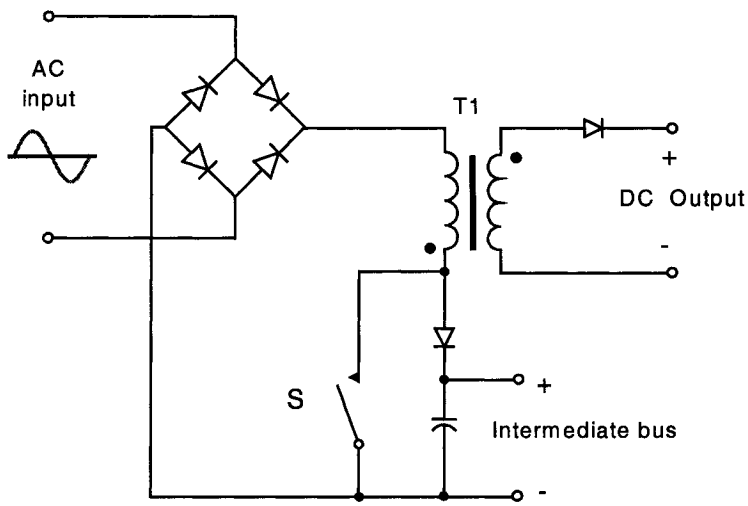


Fig. 2-1 Flyboost PFC cell

Based on this PFC cell, a family of single stage Power Factor Correction topologies can be derived, as illustrated in [23]. All those topologies can transfer some input power directly to output, and limit maximum intermediate bus voltage. In this chapter, one simple example is implemented to discuss the operation of flyboost PFC cell, and power flow analysis approach is proposed to obtain the equation of the intermediate bus for practical design.

2.2 Flyboost-flyback single stage PFC

The simplest DC-DC converter is flyback. Here, flyback DC-DC cell is integrated with flyboost PFC cell to form a new single stage PFC converter. The topology is shown in Fig. 2-2, which consists of a flyboost PFC cell and a flyback converter cell. The flyboost PFC cell includes flyboost transformer T_1, input bridge rectifier, diode D_1, D_2,

D_3 and main switch S. The flyback converter cell is comprised of flyback transformer T_2, diode D_4 and main switch S. Both cells share only main switch and the controller.

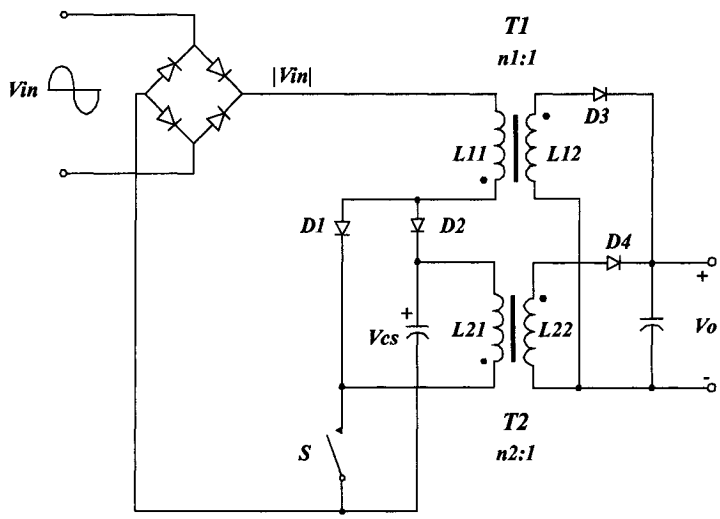


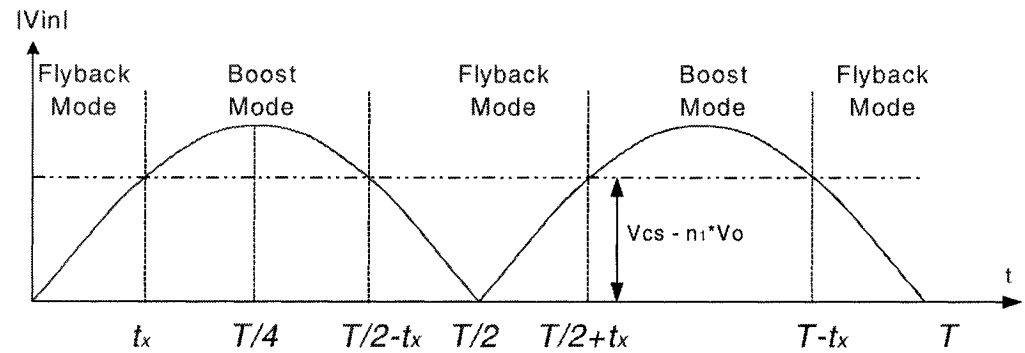
Fig. 2-2 An example of Flyboost PFC circuit

According to the operation of the flyboost transformer T_1, the proposed PFC cell operates in two different modes in one line cycle, as shown in Fig. 2-3. These two modes of operations are discussed as follows:

a). Flyback mode: When $v_{in}(t) < V_{DC,bus} - n_1 * V_o$, ($n_1$: turn ratio of T_1), T_1 operates as a flyback transformer. When main switch S is ON, T_1 is charged by rectified line voltage linearly. When S is OFF, T_1 will discharge all of its stored magnetizing power to output. So T_1 magnetizing power stored during main switch ON period is directly transferred to output, resulting in this part of power being processed only once.

b). Boost mode: When $v_{in}(t) >= V_{DC,bus} - n_1 * V_o$, T_1 works as a boost inductor. When S is ON, T_1 is charged by rectified line voltage linearly. When S is OFF, T_1 will discharge all of its magnetizing power to DC bus capacitor. The power stored in DC bus

capacitor will be transferred to output by DC/DC conversion cell, with this part of power being processed twice.



$$|V_{in}(t_x)| = V_{DC,bus} - n_1 * V_o$$

Fig. 2-3 Operation mode of Flyboost PFC cell in one line frequency cycle

According above discussion, Flyboost PFC cell operates like boost PFC cell or flyback PFC cell at different period in one line cycle. Since high power factor can be achieved by both DCM flyback PFC cell and DCM boost PFC cells, high power factor can also be expected from flyboost PFC cell. Integrating flyboost PFC cell with a DC/DC conversion cell, tight output regulation will also be achieved.

Parameters in figure 2-2 are defined as:

- Flyboost transformer T_1: Turn ratio n_1:1; primary inductance L_{11}, secondary inductance L_{12}
- Flyback transformer T_2: Turn ratio n_2:1; primary inductance L_{21}, secondary inductance L_{22}
- |Vin(t)|: rectified instantaneous input voltage
- V_{cs}: storage capacitor voltage on high voltage side

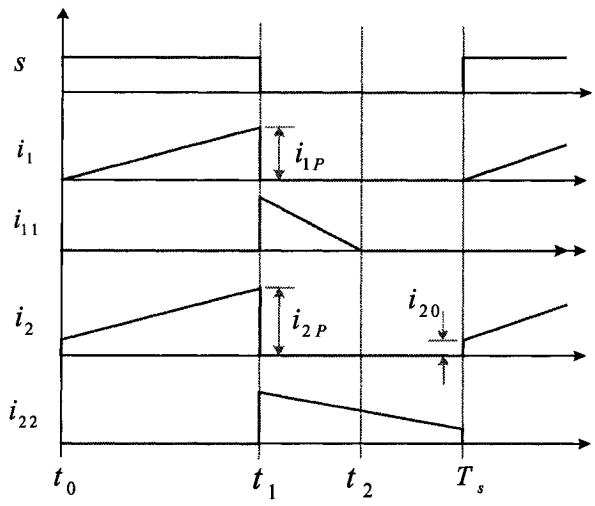
- V_o: output voltage

In the following analysis, we assume that:

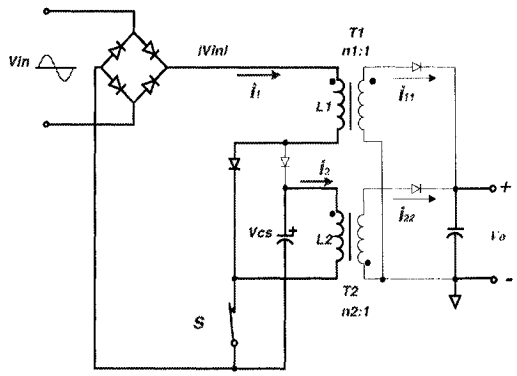
- No leakage inductance in two transformers
- V_{cs} (voltage across storage capacitor) and output V_o are constant
- All switch components are ideal
- Input voltage is constant during each switching cycle
- Flyboost operates at DCM, Flyback runs at CCM

2.2.1 Flyback Operational Mode Analysis

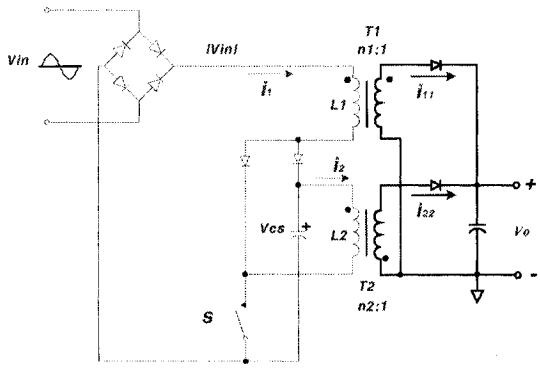
When the line voltage is low, $|V_{in}(t)| < V_{cs} - V_o * n_1$, the flyboost power factor correction cell works as flyback transformer. During the switch on period, the current in flyboost transformer will increase linearly and the energy is stored as magnetizing energy. During the switch off period, the stored magnetizing energy will be transferred to the load. Meanwhile, the flyback converter cell will deliver some power to load also in order to keep the total power transferred by PFC cell and flyback cell in one switching cycle equal to the output power. By this way, the output voltage ripple will be minimized. Operation waveforms and equivalent circuits during this mode are shown in figure 2-4.



a. Operation waveform



b. Equivalent circuit during ON period



c. Equivalent circuit during OFF period

Fig. 2-4 Operation of flyback mode

Interval 1 ($t_o \sim t_1$): the main switch is turned on at t_o, the rectified line voltage |Vin| is applied to L_{11}, the primary winding of flyboost transformer T_1. The current in L_{11}, i_{L11} in Fig. 2-4, will increase linearly, and the energy is stored in flyboost transformer. And the voltage across storage capacitors is applied to flyback transformer, T_2, which will cause the current in output filter (i_2 in Fig. 2-4) to increase linearly. Since PFC cell operates at DCM, i_{L11} will increase from zero.

$$\frac{d}{dt}(i_{L11}) := \frac{|Vin(t)|}{L11} \tag{2.1}$$

$$\frac{d}{dt}(i_{L21}) := \frac{Vcs}{L21} \tag{2.2}$$

Interval 2 ($t_1 \sim t_2$): the main switch is turned off at t_1, T_1 will discharge through its secondary winding L_{12} and delivery stored magnetizing energy to the output. The current in the flyboost transformer secondary winding (i_{L12}) will decrease linearly. And the current in T_2 (i_{L22}) will also decrease linearly.

At t_2, all magnetizing energy in flyboost transformer T_1 is transferred to the load, i_{L12} reaches zero and the block diode D_3 will prevent the current from becoming negative. And the current in flyback transformer L_{22} continues to decrease.

$$\frac{d}{dt}(i_{L12}) := -\frac{Vo}{L12} \tag{2.3}$$

$$\frac{d}{dt}(i_{L22}) := -\frac{Vo}{L22} \tag{2.4}$$

Interval 3 ($t_2 \sim Ts$): i_{L12} stays at zero. And the current in flyback transformer T_2 i_{L22} continues to decrease until the switch is turned on at T_s and a new cycle begins.

$$\frac{d}{dt}(i_{L12}) := 0 \tag{2.5}$$

$$\frac{d}{dt}(i_{L22}) := -\frac{Vo}{L22} \tag{2.6}$$

2.2.2 Boost Operational Mode Analysis

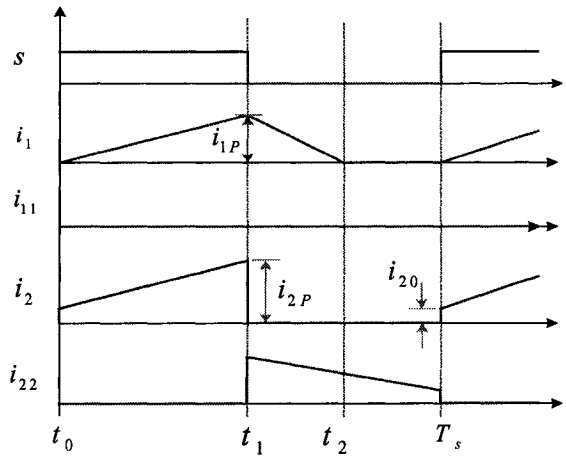
When line voltage is higher than V_{cs}- V_o* n_1, flyboost transformer T_1 works as boost inductor. During the switch ON period, the current in flyboost transformer T_1 will increase linearly, then decrease and transfer power to storage capacitors during the switch off period. The flyback converter cell will deliver all required power to the load to minimize the output voltage ripple.

Interval 1 ($t_o \sim t_1$): the main switch is turned on at t_o, the line voltage is applied to flyboost transformer. The current in the primary winding of flyboost transformer, i_{L11} in Fig. 2-5, will increase linearly. And the voltage across storage capacitors will be applied to transformer, T_2, which will cause the current i_{L21} in Fig. 2-5 to increase linearly also. Under full load condition Flyboost transformer will runs as a boost inductor at DCM, while flyback converter cell will run at CCM to reduce current stress on main switch.

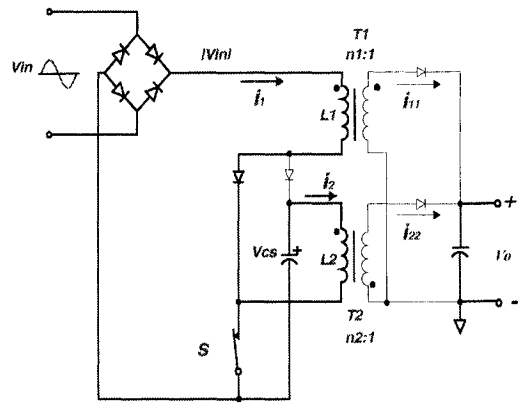
$$\frac{d}{dt}(i_{L11}) := \frac{|Vin(t)|}{L11} \tag{2.7}$$

$$\frac{d}{dt}(i_{L21}) := \frac{Vcs}{L21} \tag{2.8}$$

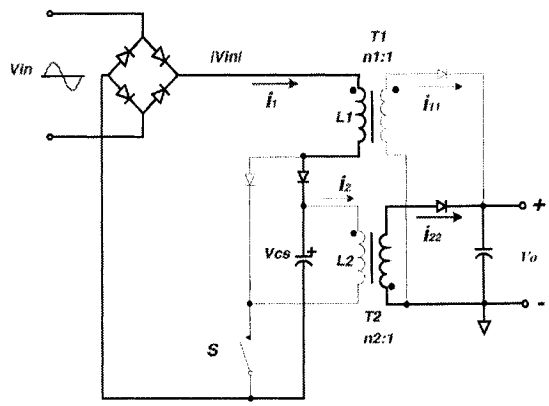
Interval 2 ($t_1 \sim t_2$): the main switch is turned off at t_1. The current in the flyboost (i_{L11}) will decrease linearly and discharge energy to storage capacitors. And the current in flyback (i_{L22}) will also decrease linearly. At t_2, the current in the flyboost (i_{L11}) reaches zero.



a. Operational waveform



b. Equivalent circuit during ON period



c. Equivalent circuit during OFF period

Fig. 2-5 Operation of flyback mode

$$\frac{d}{dt}(i_{L11}) := |Vin(t)| - Vcs \tag{2.9}$$

$$\frac{d}{dt}(i_{L22}) := -\frac{Vo}{L22} \tag{2.10}$$

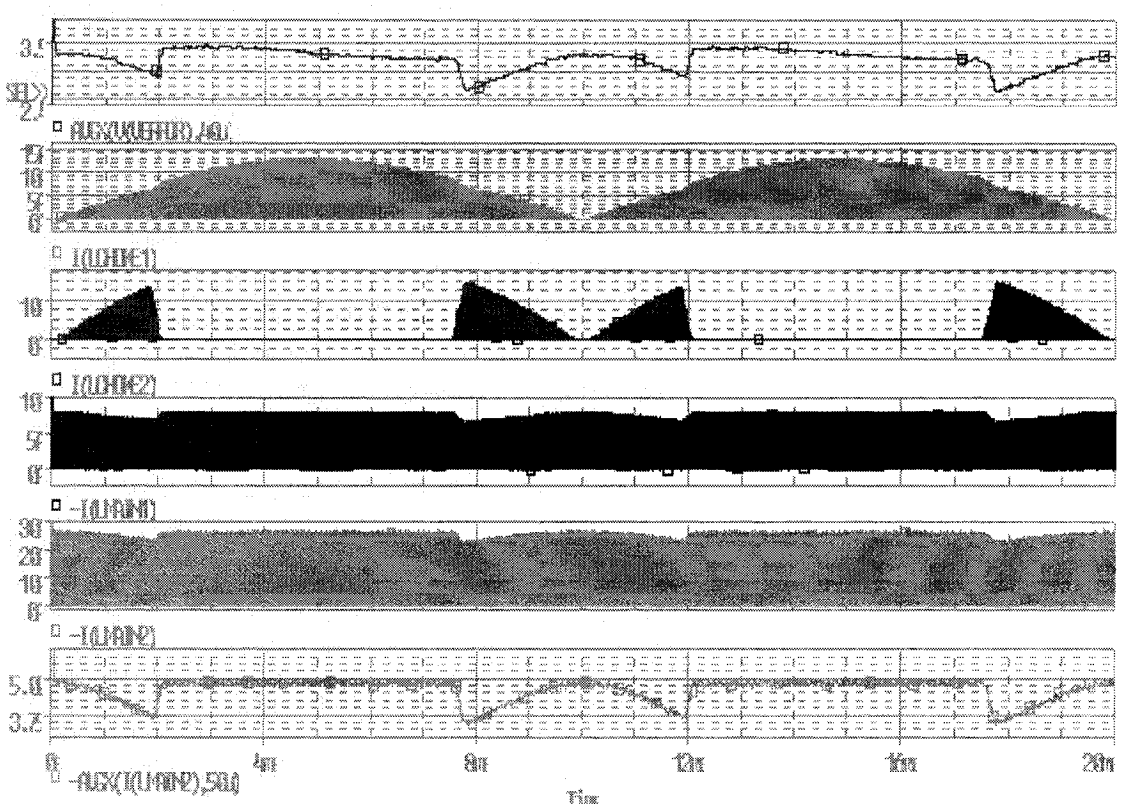
Interval 3 ($t_2 \sim t_3$): i_{L12} stays at zero. And the current in flyback transformer T_2 i_{L22} continues to decrease until the switch is turned on at t_3. Then a new switching cycle will begin.

$$\frac{d}{dt}(i_{L12}) := 0 \tag{2.11}$$

$$\frac{d}{dt}(i_{L22}) := -\frac{Vo}{L22} \tag{2.12}$$

The operation of this topology in Fig. 2-2 was simulated in OrCAD Pspice®. Some simulation results are shown in Fig. 2-6 . Those results verified the correction of above analysis. Some simulation results are shown in Fig. 2-6. In this simulation, simple output voltage feedback controller is used. The duty cycle (trace 1) is changing according to average i_{L22} value (trace 6) in order to keep the sum of i_{L12} and i_{L22} equal to output current.

In Fig. 2-6, we can clearly see there are two different operation modes in this topology. And the input current waveform still follows voltage change with little distortion, which means high power factor achieved at input end.



From top to bottom:

Trace 1: duty cycle (D)

Trace 2: T1 primary current (i_{L11})

Trace 3: T1 secondary current (i_{L12})

Trace 4: T2 primary current (i_{L21})

Trace 5: T2 secondary current (i_{L22})

Trace 6: Average T2 secondary current (i_{L22}) over each switching cycle

Fig. 2-6 Operational waveform in one line cycle by simulation

2.3 Power Flow Analysis

Since there are two different operational modes in flyboost derived PFC topology, conventional analysis methods can be adopted directly. For large signal analysis, the parameters can be determined through power flow analysis. However, it is a challenge to find an effective analysis method for small signal analysis.

In the following section, power flow analysis method is applied to analyze the topology in Fig. 2-2. In this analysis, only DCM+CCM operation is analyzed. However, other combination operation modes, such as DCM+DCM and DCM+CCM/DCM can gained easily according to same analysis method. The power flow chart is shown in Fig. 2-7.

For simplicity, the following assumptions are given:

- Ideal components, without switching characteristics, leakage inductance, parasitic parameters, etc.
- Input voltage is constant during each switching cycle;
- Switching frequency is much higher than line frequency;
- Sum of value over switching cycle can be converted to integration over time;
- Vcs, DC bus voltage, is constant, meaning that the charging energy and discharging energy to DC bus capacitor should be equal for each *line cycle;*
- Tight output regulation. It means the charging energy and discharging energy to output capacitor should be equal for each *switching cycle;*

The main concepts in this method are:

- Calculate total power transferred by two paths, which should be equal to output power, and obtain instantaneous duty cycle for each switching cycle;
- Calculate the charging and discharging power of the intermediate bus capacitor. These power should remain equal to keep the intermediate bus voltage constant. This equation can be used to obtain the intermediate bus voltage under different circuit parameters.

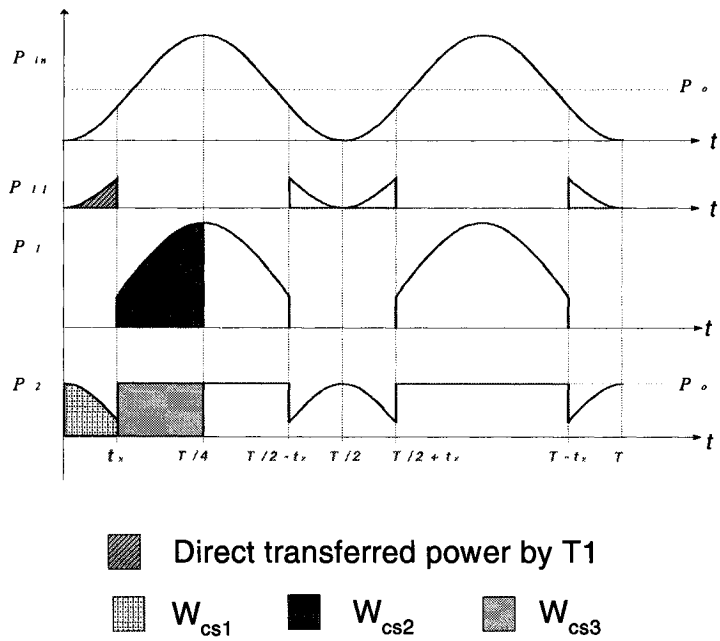


Fig. 2-7 Power flow map of flyback-flyback topology

It is preferred to let DC-DC flyback cell operate under CCM, because the RMS current through power components is minimum. Here, we begin to analyze with DC-DC flyback cell operating under CCM. Other operation mode analysis will discuss later.

If DC-DC flyback cell operates under CCM for the whole line cycle and intermediate bus voltage is constant, the duty cycle should be constant also to achieve constant output voltage:

$$D = \frac{n_2 * V_o}{V_{cs} + n_2 * V_o} \tag{2.13}$$

Since operation mode is changing based on the instantaneous input line voltage, the power transfer path is also different in flyback and boost modes. We need to analyze the power flow separately in two modes.

2.3.1 Flyback Mode Power Flow Analysis

During Flyback mode, two flyback transformers are charged during ON period, and T_1 is entirely discharged during OFF period in each switching cycle, but T_2 will not completely discharged since it operates at CCM. And all stored magnetizing energy in T_1 transformers are transferred to output end directly, and some of T_2 will be transferred to output also. So there are two power paths for output. And DC bus capacitor (intermediate bus capacitor) is only discharged, no charging energy in flyback mode.

The following equation shows the current in T_1 primary winding when switch is turned off at t_1

$$i_{1p} := \frac{V_g \cdot D \cdot T_s}{L_1} \tag{2.14}$$

The following equation shows stored magnetizing energy in T_1 transformers when switch is turned off at t_1.

$$W_1 := \frac{L_1 \cdot i_{1p}^{\ 2}}{2} \tag{2.15}$$

By combining Eqs. 2-14 and 2-15, we obtain:

$$W_1 := \frac{V_g^{\ 2} \cdot D^2 \cdot T_s^{\ 2}}{2 \cdot L_1} \tag{2.16}$$

All power processed in this mode is transferred to load. In order to keep tight output voltage regulation, i.e. V_O constant, the total power transferred by T_1 and T_2 should be equal to output power in each switching cycle. The power transferred by T_1 is equal to:

$$P_1 = \frac{W_1}{T_S} = \frac{V_g^{\ 2} D^2 T_S}{2L_1} \tag{2.17}$$

So the power processed by T_2 in one switching cycle is:

$$P_2 = P_o - P_1 = P_o - \frac{V_g^{\ 2} D^2 T_S}{2L_1} \tag{2.18}$$

In whole flyback mode, total energy transferred by flyback transformer T_2 is from DC bus capacitor, and is equal to:

$$W_{cs1} := \sum_{t=0}^{t_x} P_2 \cdot T_s \tag{2.19}$$

When the switching period is much less than line period, the above sum equation can be converted to the following integration equation:

$$W_{cs1} := \int_0^{t_x} \left(P_o - \frac{V_g^{\ 2} \cdot D^2 \cdot T_s}{2 \cdot L_1} \right) dt \tag{2.20}$$

The input voltage can be described as:

$$V_g := V_p \cdot \sin(w \cdot t) \tag{2.21}$$

So the total discharging energy from intermediate bus capacitor during flyback mode is equal to:

$$W_{cs1} := P_o \cdot t_x - \frac{V_p^2 \cdot D^2 \cdot T_s}{2 \cdot L_1} \int_0^{t_x} \sin(w \cdot t)^2 \, dt \tag{2.22}$$

The above equation can be simplified as:

$$W_{cs1} := P_o \cdot t_x - \frac{V_p^2 \cdot D^2 \cdot T_s}{2 \cdot L_1} \left(\frac{t_x}{2} - \frac{\sin(2 \cdot w \cdot t_x)}{4 \cdot w} \right) \tag{2.23}$$

2.3.2 Boost Mode Power Flow Analysis

Under boost mode, two flyback transformers are charged during ON period, and T_1 entirely is discharged its magnetizing energy to DC bus capacitor during OFF period in each switching cycle. All output power is from DC bus capacitor through T_2. And DC bus capacitor is discharged by T_2, and charged by T_1 at this mode.

The average input current in one switching cycle is

$$i_1(avg) := \frac{D^2 \cdot T_s}{2 \cdot L_1} \cdot \frac{V_{cs} \cdot V_g}{V_{cs} - V_g} \tag{2.24}$$

So the average input power in one switching cycle is

$$P_1 := V_g \cdot i_1(avg) \tag{2.25}$$

By combining Eq. 2.24 and 2.25, we obtain:

$$P_1 := \frac{D^2 \cdot T_s}{2 \cdot L_1} \cdot \frac{V_{cs} \cdot V_g^2}{V_{cs} - V_g} \tag{2.26}$$

The energy transferred by T_1 from input is stored completely in DC bus capacitor in whole Boost mode, which is equal to:

$$W_{cs2} := \sum_{t=t_x}^{\frac{T}{4}} P_1 \cdot T_s \tag{2.27}$$

Based on the assumption, the above equation can be converted to integration equation. By combining Eqs. 2.21 and 2.26, it yields:

$$W_{cs2} := \int_{t_x}^{\frac{T}{4}} \frac{D^2 \cdot T_s}{2 \cdot L_1} \cdot \frac{V_{cs} \cdot V_p{}^2 \cdot \sin(w \cdot t)^2}{V_{cs} - V_p \cdot \sin(w \cdot t)} dt \tag{2.28}$$

All output power is transferred via T_2. So, for each switching cycle, P_2 is equal to P_o. The energy transferred by T_2 is totally from DC bus capacitor in whole boost mode, which is equal to:

$$W_{cs3} := \sum_{t=t_x}^{\frac{T}{4}} P_2 \cdot T_s \tag{2.29}$$

Since P_2 is equal to output power P_o, so,

$$W_{cs3} := P_o \cdot \left(\frac{T}{4} - t_x \right) \tag{2.30}$$

2.3.3 Final equation of Power Flow Analysis

For each line cycle, the discharging and charging energy from and into DC bus capacitor should be balanced to keep V_{cs} constant. So:

$$W_{cs2} = W_{cs1} + W_{cs3} \tag{2.31}$$

Use above equation, we get:

$$\int_{t_x}^{\frac{T}{4}} \frac{T_s}{2 \cdot L_1} \cdot \frac{n_2^2 \cdot V_o^2}{(V_{cs} + n_2 \cdot V_o)^2} \cdot \frac{V_{cs} \cdot V_p^2 \cdot \sin(w \cdot t)^2}{V_{cs} - V_p \cdot \sin(w \cdot t)} dt = P_o \cdot \frac{T}{4} - \frac{V_p^2 \cdot T_s}{2 \cdot L_1} \cdot \frac{n_2^2 \cdot V_o^2}{(V_{cs} + n_2 \cdot V_o)^2} \cdot \left(\frac{t_x}{2} - \frac{\sin(2 \cdot w \cdot t_x)}{4 \cdot w} \right) \tag{2.32}$$

In the above equation, tx is the boundary time for flyback mode and boost mode. In first quarter of line period, Vin(t) is equal to Vcs – Vo*n1 at t_x. So the boundary time for two modes is given by:

$$t_x = \arcsin\left(\frac{V_{cs} - n_1 \cdot V_o}{V_p} \right) \tag{2.33}$$

Since the operation of this circuit is symmetrical over the line period, it is easy to obtain all mode boundary point for this topology, as shown in Fig. 2-7.

2.3.4 Conditions fro DCM+CCM Operation

The above analysis is based on this assumption: T_1 always runs at DCM, while T_2 operates at CCM. In order to use those equations, we need to make sure the operation mode is correct for the specified circuit parameters.

For PFC transformer T_1, the heavy load and high charging voltage happens at T/4, while $V_{in}(t) = V_{peak}$. The charging voltage for T_1 is V_{in}, while the discharging voltage is Vcs-Vin, so we get:

$$V_p \cdot D = (V_{cs} - V_p) \cdot D1 \tag{2.34}$$

So,

$$D1 := \frac{V_p \cdot D}{V_{cs} - V_p} \tag{2.35}$$

In order to keep T_1 under DCM, D_1 should be less than 1-D, so:

$$D < \frac{V_{cs} - V_p}{V_{cs}} \tag{2.36}$$

And, the duty cycle depends on DC/DC cell, which is constant:

$$D = \frac{n_2 \cdot V_o}{V_{cs} + n_2 \cdot V_o} \tag{2.37}$$

Combining the above equations, the condition for T_1 under DCM is given by:

$$V_{CS}^{\ 2} - V_{CS}V_P - n_2 V_P V_O > 0 \tag{2.38}$$

According to power flow chart in Fig. 2-7, the lightest load of DC/DC transformer T_2 happens at the mode boundary t_x. If T_2 runs under CCM at t_x , it will operate under CCM at any time. According to current waveform at CCM, we found that:

$$i_{22}(avg) > \frac{1}{2} \cdot \Delta i_{22} \cdot (1 - D) \tag{2.39}$$

while, i_{22} is the current through T_2 secondary winding current. And

$$\Delta i_{22} := n_2 \cdot \Delta i_2 \tag{2.40}$$

Δi_{22} is the current ripple in T_2 secondary winding, and Δi_2 is the current ripple in T_2 primary winding. The current ripple of T_2 during switch ON period is given by:

$$\Delta i_2 = \frac{V_{CS} D T_S}{L_2} \tag{2.41}$$

The power transferred by T_2 is equal to:

$$P_2 = V_O i_{22}(avg) \tag{2.42}$$

Combining Eqs. 2.37 and 2.39 - 2.42, we obtain the minimum power for T_2 under CCM is:

$$P_2 > \frac{n_2^2 \cdot V_{cs}^2 \cdot V_o^2 \cdot T_s}{2L_2 \cdot (V_{cs} + n_2 \cdot V_o)^2} \tag{2.43}$$

At mode boundary t_x, the direct transferred power by T_1 is equal to:

$$P_1(t_x) = \frac{V_g^2(t_x) D^2 T_S}{2L_1} \tag{2.44}$$

Since power transferred by T_2 is the difference between output power an direct power transferred by T_1, we obtain the equation for P_2 as follows:

$$P_2(t_x) = P_o - \frac{V_g(t_x)^2 \cdot D^2 \cdot T_s}{2 \cdot L_1} \tag{2.45}$$

At mode boundary t_x, the input voltage is equal to V_{cs}-n_1V_o. direct transferred power by T_1 is equal to:

$$P_o - \frac{(V_{cs} - n_1 \cdot V_o)^2 \cdot T_s}{2 \cdot L_1} \cdot \frac{n_2^2 \cdot V_o^2}{(V_{cs} + n_2 \cdot V_o)^2} > \frac{n_2^2 \cdot V_{cs}^2 \cdot V_o^2 \cdot T_s}{2L_2 \cdot (V_{cs} + n_2 \cdot V_o)^2} \tag{2.46}$$

Finally we obtain the requirement for T_2 under CCM by combining above equations as follows:

$$2L_1L_2P_o(V_{CS} + n_2V_O)^2 - L_2T_s(n_2V_OV_{CS} - n_1n_2V_o^2)^2 - L_1T_sn_2^2V_{CS}^2V_o^2 > 0 \tag{2.47}$$

Those equations describe the relationship between intermediate bus voltage and other circuit parameters. But they are transcendental equations and are difficult to solve. Next chapter we will discuss in detail about how to solve those equations numerically by math software, such as MathCAD.

2.4 Summary

By adding one winding to boost inductor, flyboost PFC cell can transfer some input power directly to output end. So the total power proceeded by power stage is reduced. There are two operation modes in one line cycle: flyback mode and boost mode. The period length of each mode depends on the input voltage, output voltage, intermediate bus voltage, and turn ratio of flyboost transformer. When the intermediate bus voltage goes high, the period of flyback mode increases, resulting in more power to output and less power to the bus capacitor. So it can limit the maximum intermediate bus voltage. Through one simple example, the operation of flyboost PFC cell was discussed in detail in this chapter. And one special analysis method, power flow method, was implemented to obtain critical equations for this kind of topology.

CHAPTER 3

FLYBOOST PARALLEL/SERIES FORWARD SINGLE STAGE PFC CONVERTER

3.1 Introduction

In previous chapter, Flyboost, the direct power transfer PFC cell, was introduced with one simple example. In actual application, that circuit suffers from very high voltage stress for universal application, even with the automatic voltage limit function. In this chapter, one practical topology is discussed in detail with design guide and experimental results.

The single stage Russian PFC topology in Fig. 3-1 shows some advantages due to its automatic voltage clamp function. When the main switch is on, two primary winding of DC-DC transformer T1 work in parallel to power the output inductor, like typical forward; while the main switch is turned off, two primary winding work in series to discharge the magnetizing energy back to intermediate bus caps, resulting in clamped voltage across main switch. The DC-DC circuit in Russian topology is called parallel/series forward converter. The maximum voltage stress should be always equal to the sum of two caps voltage, independent of the transformer leakage inductor. If we can control the intermediate bus voltage, then the voltage stress over the main switch is also

under control. In traditional Russian PFC topology, the voltage is controlled by letting the PFC cell and DC-DC cell operate under DCM. This method is simple and effective, but resulting in very high current stresses on main switch and secondary diodes. This disadvantage makes it impractical, especially for mediate power level, such as 200w.

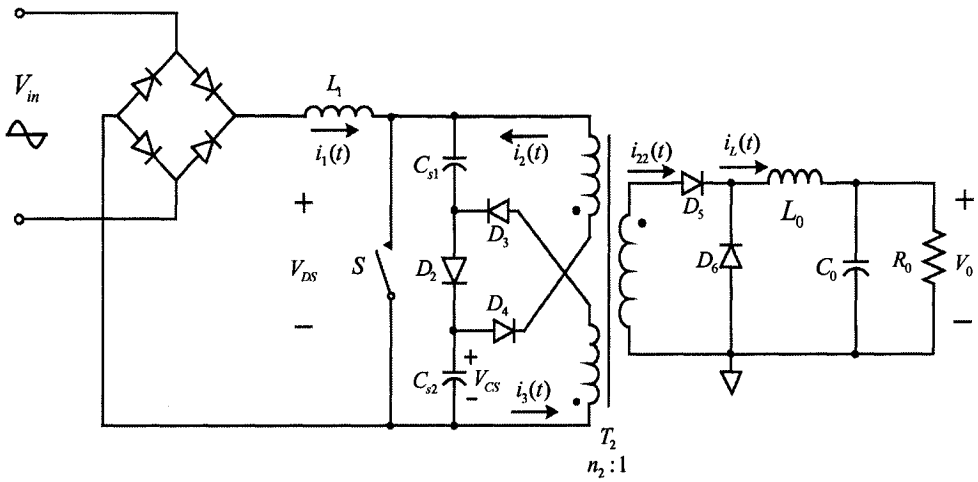


Fig. 3-1. Russian single stage PFC converter

In this chapter, this topology is integrated with flyboost PFC cell to achieve better results. As discussed in previous chapter, flyboost PFC can let the DC-DC cell operate under CCM and limit the intermediate bus voltage at the same time. The flyboost-parallel/series forward single stage PFC topology, shown in Fig. 3-2, inherits the advantage from both ideas.

The topology shown in Fig. 3-2 is based on the flyboost PFC scheme and a parallel/series forward DC/DC conversion cell. The flyboost PFC cell, including transformer T_1, input bridge rectifier, two intermediate bus capacitors (C_{s1} and C_{s2}), diode D_1 and D_2, and active switch S, operates in DCM to achieve high power factor and

transfers some input power to the output directly. The parallel/series forward DC-DC conversion cell, which consists of bus capacitors (C_{s1} and C_{s2}), forward transformer T_2, output inductor L_o, output capacitor C_o, diodes and switch S, converts the stored intermediate bus voltage to the output and achieves tight output voltage regulation. Both cells share bus capacitors, the only active switch S and controller.

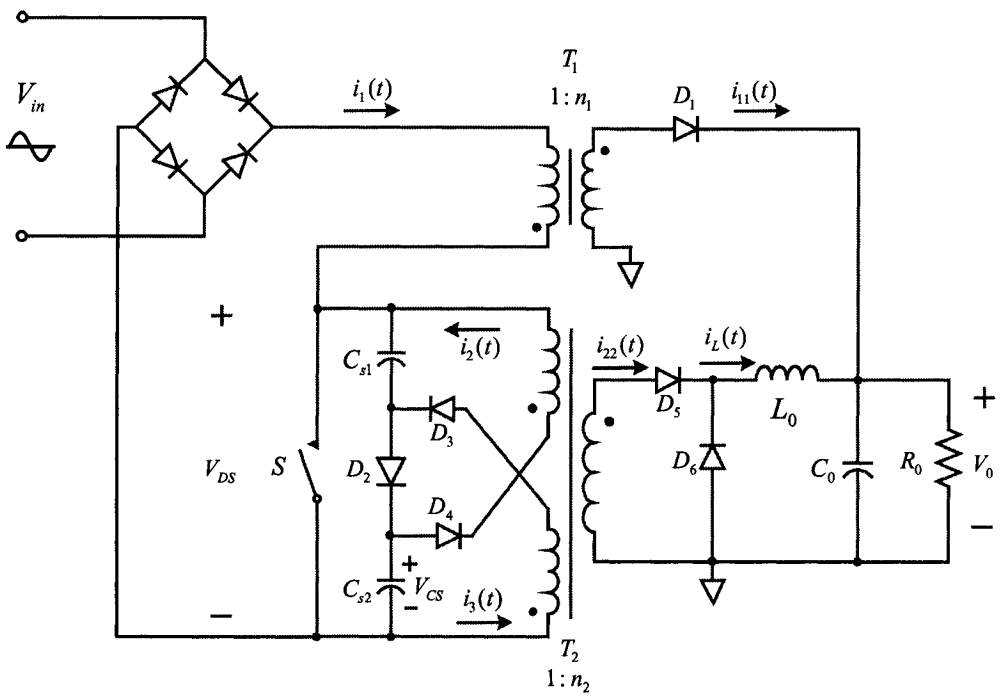


Fig. 3-2. flyboost-parallel/series forward single stage PFC converter

The operation of this topology is discussed in detail below, and design procedure is provided with one example. And experimental results from the example prototype are given to verify the analysis and design.

3.2 Operation Description

Just like typical single-stage PFC topologies, the flyboost PFC cell and DC-DC conversion cell in this topology operate independently, although both cells share the only one switch. But the operation of this topology differs from other typical schemes by its special operation modes and parallel power flow feature. There are two different modes in one line cycle, depending on the instantaneous input voltage and the bus voltage, as shown in Fig. 3-3(a). When input voltage is low, diode D_1 in transformer T_1 secondary side will conduct during switch OFF interval, and T_1 works like a flyback transformer. It is referred to flyback mode; while input voltage goes higher, T_1 will operate like a boost inductor to charge intermediate bus capacitors. It is called as boost mode.

In the following discussion, the DCM operation will be assumed for the PFC cell to achieve high power factor, and the CCM operation for the DC-DC conversion cell to reduce the current stress on the switches. To simplify the analysis, all components here are assumed to be ideal without parasitic parameters, and the ripple voltage across bulky capacitors is neglected.

Following are the detailed operation description of the above topology in one switching cycle for each different operation mode.

3.2.1 Flyback operation mode

When rectified line voltage $|V_{in}(t)|$ is less than V_{bus}-n_1V_o (V_{bus}: bus voltage, equal to the sum of the voltage across two intermediate bus capacitors; n_1: the turn ratio of T1; V_o: output voltage), Transformer T_1 works like a flyback transformer to discharge all stored input power directly to the load. And this portion of load power is processed by the active switch S only once. Meanwhile, DC-DC cell will deliver some power from bus capacitors to the load to keep tight output voltage regulation. The operational waveforms are shown in Fig. 3-3(b).

Interval 1 ($t_o \sim t_1$): Switch S is turned on at t_o. The rectified line voltage $|V_{in}(t)|$ is applied to primary winding of T_1. The current in T_1, i_1 in Fig. 3-3(b), increases linearly. Since PFC cell operates in DCM, i_1 starts increasing from zero. The bus capacitors voltage V_{CS} is applied to output inductor Lo through transformer T_2, causing its current i_L to linearly increase also. The special configuration of parallel/series forward conversion cell will automatically keep the voltage across two bus capacitors always balanced: since the higher voltage in one capacitor will keep another capacitor from discharging during interval, it will bring down the higher voltage to equal to another voltage. So we assume those capacitor voltages are same and equal to half of bus voltage. Based on above analysis, we have:

$$L_1 \frac{di_1(t)}{dt} = |V_{in}(t)| \tag{3.1}$$

$$L_O \frac{di_L(t)}{dt} = \frac{V_{cs}}{n_2} - V_O = \frac{V_{bus}}{2n_2} - V_O \tag{3.2}$$

where L_1 is the primary inductance of transformer T_1, Lo is output filter inductor, n2 is the turn ratio of T_2.

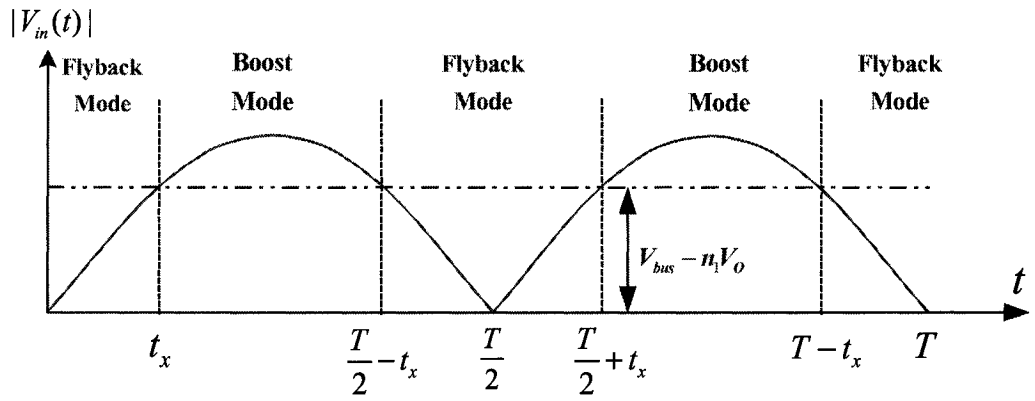
Interval 2 ($t_1 \sim t_2$): S is turned off at t_1. T_1 discharges through its secondary winding and deliveries its stored magnetizing energy to the load, resulting in the voltage across T_1 primary winding clamped to $n_1 V_o$. The current in output inductor L_o will flow through freewheel diode D_6. Transformer T_2 will reset its magnetizing energy to bus capacitors through diode D_2-D_4, thanks to its special circuit configuration. And the voltage across switch S is clamped by two bus capacitors, resulting in switch S free of spike voltage caused by leakage inductance existing in other topologies. We have:

$$L_{11}\frac{di_{11}(t)}{dt} = -V_O \tag{3.3}$$

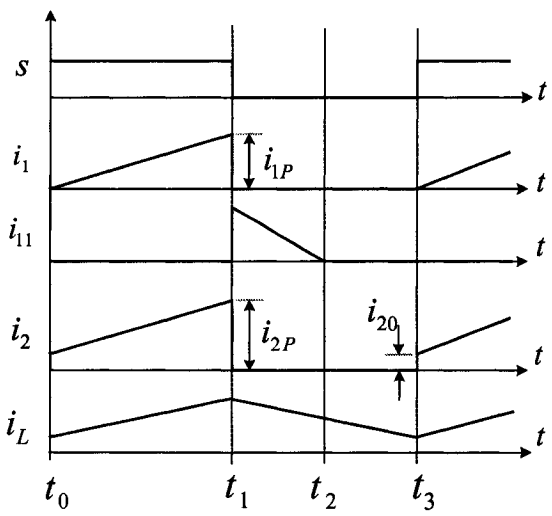
$$L_O\frac{di_L(t)}{dt} = -V_O \tag{3.4}$$

where L_{11} is the secondary inductance of transformer T_1.

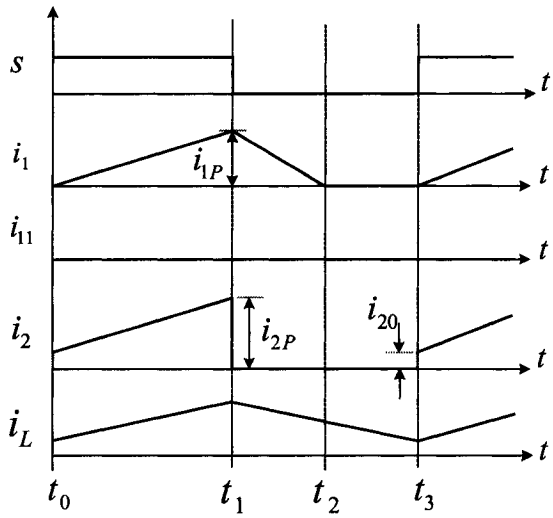
Interval 3 ($t_2 \sim t_3$): At t_2, all magnetizing energy in T_1 is transferred to the load. Current i_{11} through T_1 secondary winding reaches zero, and diode D_1 keeps it from going negative. Transformer T_2 continues to reset through bus capacitors. Since the magnetizing and demagnetizing voltage over transformer T_2 are the same bus capacitor voltage, the maximum allowable duty cycle of this topology is limited to 0.5. The current in inductor L_O continues to decrease complying with Eq. (3.4), until the switch is turned on at t_3. At $t=t_3=t_o+T_S$, the switching cycle repeats.



(a) Operational mode in one line period



(b) Flyback mode



(c) Boost mode

Fig. 3-3. Operation mode and waveforms

3.2.2 Boost operation mode

When instantaneous input voltage goes higher, and $|V_{in}(t)|$ is higher than V_{bus} - n_1V_o, the voltage across transformer T_1 primary winding is clamped to $V_{bus}-|V_{in}(t)|$ during S OFF interval, which will be less than n_1V_o. It means that diode D_1 in T_1 secondary discharging path will not conduct. T_1 works like a boost inductor and discharges its magnetizing energy to both bus capacitors via D_2. And DC/DC cell will deliver all output power from bus capacitors to the load.

Under this mode, the input power is stored in bus capacitors, and then transferred to the load by DC/DC cell, resulting in this portion of power being processed twice by switch S. The operational waveforms are shown in Fig. 3-3(c). The operation during interval 1 and interval 3 under boost mode are exactly the same as under flyback mode discussed above. So only interval 2 is described here as following:

Interval 2 ($t_1 \sim t_2$): Switch S is turned off at t_1. T_1 current i_1 will decrease linearly. The current in output inductor L_o will flow through freewheel diode D_6. Transformer T_2 will reset its magnetizing energy to bus capacitors through diode D_2-D_4. We have:

$$L_1 \frac{di_1(t)}{dt} = -\left(V_{bus} - |V_{in}(t)|\right) \tag{3.5}$$

$$L_O \frac{di_L(t)}{dt} = -V_O \tag{3.6}$$

3.3 Steady-State Analysis

In this section, this parallel PFC topology is analyzed to get its characteristics under steady state.

3.3.1 Mode boundary

Depending on the discharging path of T_1, there are two different operation modes for this topology over each line period. Based on the operation analysis above, rectified input voltage is equal to V_{bus}-n_1V_o at boundary of two modes. In first quarter of line period, the boundary time for two modes is given by:

$$t_x = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{bus} - n_1 V_o}{V_p}\right) \tag{3.7}$$

where V_p is the peak value of input voltage which is,

$$v_{in}(t) = V_p \sin(\omega t) \tag{3.8}$$

Since the operation of this circuit is symmetrical over the line period, it is easy to obtain all mode boundary condition, as shown in Fig. 3-3(a).

3.3.2 Condition for PFC cell under DCM

In order to achieve high power factor and reduce the peak current stress, PFC cell should always operate under DCM for this single stage PFC topology. The maximum

charging voltage and the minimum discharging voltage across transformer T_1, and the maximum power processed by PFC cell all happen at time T/4, when input voltage reaches its peak value V_P. So PFC cell will operate under DCM for the entire line period if it operates under DCM at time T/4.

With PFC cell under DCM, the current through transformer T_1 primary winding, i_1 in Fig. 3-3(c), should reach zero before a new switching cycle begins, which means that:

$$t_2 - t_1 \le t_3 - t_1 \tag{3.9}$$

At T/4, PFC cell operates in Boost mode, and the charging voltage across transformer T_1 is V_p (input voltage peak value), while discharging voltage is V_{bus}-V_p. Under steady state operation, the volt-second balance across transformer results in:

$$V_p(t_1 - t_0) = (V_{bus} - V_p)(t_2 - t_1) \tag{3.10}$$

while:

$$t_1 - t_0 = DT_s \text{, and } t_3 - t_1 = (1-D)T_s \tag{3.11}$$

Combining Eqs. (3.9), (3.10), and (3.11), we obtain the following condition for PFC cell in DCM:

$$V_{bus} \ge \frac{V_P}{1-D} \tag{3.12}$$

If Parallel/Series Forward DC/DC cell operates under CCM operation, we can obtain the duty cycle by using volt-second balance limitation of output inductance and Eqs. (3.2) and (3.4), which is equal to:

$$D = \frac{2n_2 V_o}{V_{bus}} \tag{3.13}$$

From Eqs. (3.12) and (3.13), we obtain:

$$V_{bus} \geq V_P + 2n_2 V_o \tag{3.14}$$

So the intermediate bus voltage should always be higher than the sum of the input voltage peak value and the reflected output voltage across transformer T2 in order to keep PFC cell in DCM.

3.3.3 Intermediate bus voltage

The voltage across intermediate bus capacitors is a very important parameter, because it determines the voltage stress on all power components. According to its operation features, the power flow analysis approach is used here to get the equation for intermediate bus voltage. The main idea of this approach is:

- The total charging energy and total discharging energy of intermediate bus capacitors in each line period should be balanced, because the intermediate bus voltage is constant under steady-state condition.
- Tight output voltage regulation means almost constant output voltage. So the charging energy and discharging energy of output capacitor should be equal for each switching period.
- Since the operation is symmetric in line period, only first quarter of line period need to be analyzed. In the following analysis, we assume the DC-DC conversion cell operates under CCM and PFC cell under DCM.

According to analysis in last section, all input power during flyback mode ($0 \sim t_x$) is transferred to the load. When the switch turns off at t_1, the stored magnetizing energy in T_1 is given by,

$$W_{T1} = \frac{L_1 I_{1,peak}^{\ 2}}{2} = \frac{D^2 T_s^{\ 2}}{2L_1} \langle V_{in}(t) \rangle_{T_s}^{\ 2} \tag{3.15}$$

$\langle v_{in}(t) \rangle_{T_s}$ is the input voltage over each switching cycle, which can be assumed to be constant in one switching cycle, since switching frequency is much higher than line cycle.

So the total input energy during entire flyback period ($0 \sim t_x$) is equal to,

$$W_{T1,Flyback} = \sum_{t=0,T_s,2T_s,\ldots}^{t_x} W_{T1} \tag{3.16}$$

Because the switching frequency is very higher, normally several ten kHz, the above summation equation can be converted to the following integration equation,

$$W_{T1,Flyback} = \int_0^{t_x} \frac{W_{T1}}{T_s} dt = \frac{D^2 T_s}{2L_1} \int_0^{t_x} v_{in}(t)^2 dt \tag{3.17}$$

During Boost period ($t_x \sim T/4$), all input power is transferred to bus capacitors. The average input power in one switching cycle is,

$$P_{T1} = V_{in} I_{in,avg} = \frac{D^2 T_s}{2L_1} \frac{V_{bus} \langle V_{in}(t) \rangle_{T_s}^{\ 2}}{V_{bus} - \langle V_{in}(t) \rangle_{T_s}} \tag{3.18}$$

Similarly, the total input energy under Boost mode ($t_x \sim T/4$) can be calculated by,

$$W_{T1,boost} = \int_{t_x}^{\frac{T}{4}} P_{T1} dt = \frac{V_{bus} D^2 T_s}{2L_{PF}} \int_{t_x}^{\frac{T}{4}} \frac{v_{in}(t)^2}{V_{bus} - v_{in}(t)} dt \tag{3.19}$$

In steady-state, the average input power should be equal to the output power, which results in,

$$\frac{4}{T}\left(W_{T1,boost} + W_{T1,flyback}\right) = P_o \tag{3.20}$$

Substituting Eqs. (3.17) and (3.19) in Eq. (3.20) yields,

$$\int_{t_x}^{\frac{T}{4}} \frac{V_{bus} \sin(\omega t)^2}{V_{bus} - V_p \sin(\omega t)} dt - \frac{P_o T L_1 V_{bus}^{\ 2}}{8 T_s n_2^{\ 2} V_p^{\ 2} V_o^{\ 2}} + \frac{t_x}{2} - \frac{\sin(2\omega t_x)}{4\omega} = 0 \tag{3.21}$$

The above equation is only viable when DC-DC cell under CCM. We can see that the bus voltage will vary according to the load change, like other typical single stage PFC scheme. The voltage will stop changing once DC-DC cell enters DCM.

When DC-DC cell operates in DCM, duty cycle need to be determined first. Detailed calculation procedure is ignored for simplification. Here only final equation is given as:

$$\int_0^{t_x} \frac{L_1 V_{bus}(V_{bus} - 2n_2 V_o)}{4L_o n_2^{\ 2} V_P^{\ 2} \sin(\omega t)^2 + L_1 V_{bus}(V_{bus} - 2n_2 V_o)} dt = \int_{t_x}^{\frac{T}{4}} \frac{4L_o n_2^{\ 2} V_P^{\ 2} \sin(\omega t)^2}{L_1 (V_{bus} - 2n_2 V_o)\left(V_{bus} - V_p \sin(\omega t)\right)} dt - \frac{T}{4} + t_x \tag{3.22}$$

Those equations show the interrelationship between intermediate bus voltage and other circuit parameters. They are transcendental equations that can be solved by some mathematical software, such as MathCAD®. Some calculation are presented here to describe the characteristics of this parallel PFC topology.

In actual applications, the leakage inductance of flyboost PFC transformer plays an important role in intermediate bus voltage. In Appendix A, the equations for Flyboost transformer with leakage inductance are derived in detail. Here only the final equations are used to calculate the intermediate bus voltage for different operation condition.

Firstly, the relationship between intermediate bus voltage, input voltage and transformer parameters. This relationship defines the maximum allowable Flyboost transformer magnetizing inductance, which determines the current stresses on power components and conversion efficiency. In order to achieve high power factor and keep input current under control, the flyboost cell should always run under DCM. Based on above analysis, there is a minimum bus voltage to keep flyboost under DCM. We can choose those flyboost parameters, which keep the intermediate bus voltage just a little higher than the minimum value. Figure 3-4 shows the MathCAD document to calculate the relations.

MathCAD Calculation sheet for intermediate bus voltage

Parameters of the circuit:

Input: $V_p := 375$ $T := \frac{1}{50}$ $w := \frac{2\cdot\pi}{T}$

Output: $V_o := 28$ $P_o := 150$

Conversion efficiency: $\eta := 0.8$

Switching frequency (MHz): $F_s := 0.1$ $T_s := \frac{1}{F_s}$

Flyboost transformer:

Primary magnetizing inductance (uH): $L_1 := 50$

The rate of leakge inductance and L1: $n_k := 0.1$

Turn ratio (primary:secondary): $n_1 := 3$

DC-DC parallel/series forward cell:

Transformer turn ratio (primary:secondary): $n_2 := 1.5$

Output inductor (uH): $L_o := 100$

Initial guess value for variables:

Intermediate bus voltage: $V_{bus} := 700$

Mode boundary: $t_x := 0.003$

Duty cycle: $D := 0.3$

Define solve block:

Given

$$V_{bus}\cdot(1+n_k)\cdot\int_{t_x}^{\frac{T}{4}}\frac{\sin(w\cdot t)^2}{V_{bus}-V_p\cdot\sin(w\cdot t)}\,dt = \frac{P_o}{\eta}\cdot\frac{T\cdot(L_1+n_k\cdot L_1)^2}{2\cdot {V_p}^2\cdot D^2\cdot T_s\cdot L_1} - \left(\frac{t_x}{2}-\frac{\sin(2w\cdot t_x)}{4w}\right)\ldots$$

$$+ n_k\cdot(n_1\cdot V_o - V_{bus})\cdot\int_0^{t_x}\frac{\sin(w\cdot t)^2}{V_{bus}-n_1\cdot V_o - V_p\cdot\sin(w\cdot t)}\,dt$$

$$t_x = \frac{1}{w}\cdot\operatorname{asin}\left(\max\left(0,\min\left(1,\frac{V_{bus}-\frac{L_1+n_k\cdot L_1}{L_1}\cdot n_1\cdot V_o}{V_p}\right)\right)\right) \qquad D = \frac{2n_2\cdot V_o}{V_{bus}}$$

$F1(V_p, n_1) := \text{Find}(V_{bus}, D, t_x)$

Intermediate bus voltage: $V_{ccm}(V_{in}, n_1) := F1(V_{in}\cdot 1.414, n_1)_0$

Min Voltage for DCM: $Vmin(Vin) := Vin\cdot 1.414 + 2\cdot n_2\cdot V_o$

Fig.3-4. MathCAD sheet for intermediate bus voltage under CCM

Figure 3-5 shows the bus voltage over input voltage when DC/DC cell under CCM, calculated from above MathCAD calculation sheet. We can see that the bus voltage increases almost linearly with input voltage, and increase with turn ratio of transformer T_1. The curve labeled "min for DCM" in Fig. 3-5 means the minimum voltage required to keep PFC cell under DCM. We can see that if the bus voltage meets the requirement at lowest input voltage, it will always be meet. So our design consideration can be focused on lowest line voltage condition.

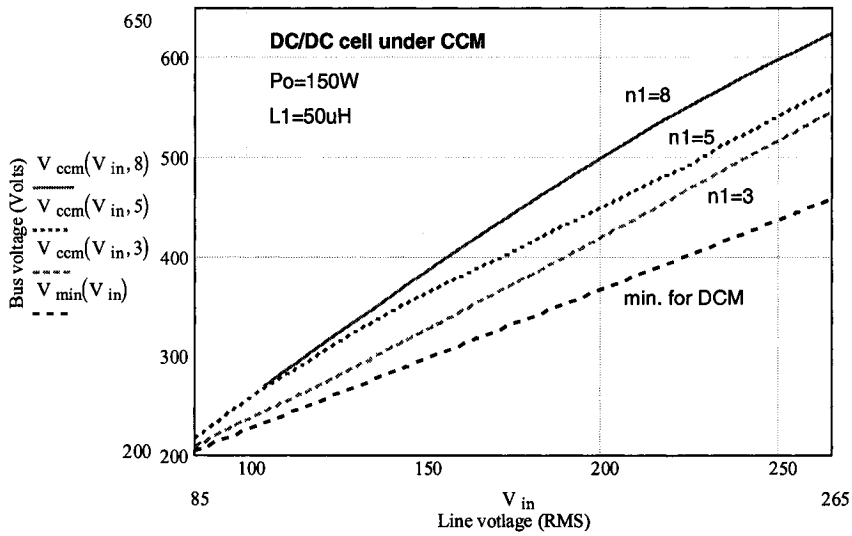


Fig.3-5. Bus voltage Vs line voltage with DC/DC cell under CCM

The maximum bus voltage is the one important parameter in single stage PFC converter. The voltage reaches its maximum value when input voltage is at its maximum and output load is very low. This voltage depends on PFC cell parameters and output inductor. Based on the above equations, MathCAD can be implemented to calculate the intermediate bus voltage under different condition like in Fig. 3-6.

MathCAD Calculation sheet for intermediate bus voltage

Parameters of the circuit:

Input: $V_p := 375$ $T := \frac{1}{50}$ $w := \frac{2 \cdot \pi}{T}$

Output: $V_o := 28$

Switching frequency (MHz): $F_s := 0.1$ $T_s := \frac{1}{F_s}$

Flyboost transformer:

Primary magnetizing inductance (uH): $L_1 := 50$

The rate of leakge inductance and L1: $n_k := 0.1$

Turn ratio (primary:secondary): $n_1 := 3$

DC-DC parallel/series forward cell:

Transformer turn ratio (primary:secondary): $n_2 := 1.5$

Output inductor (uH): $L_o := 100$

Initial guess value for variables:

Intermediate bus voltage: $V_{bus} := 700$

Mode boundary: $t_x := 0.003$

Define solve block:

Given

$$\frac{T}{4} - t_x = -\int_0^{t_x} \frac{(L_1 + n_k \cdot L_1)^2 \cdot (V_{bus} - 2 \cdot n_2 \cdot V_o) - \frac{4 \cdot L_o \cdot n_2^2 \cdot n_k \cdot L_1 \cdot V_p^2 \cdot \sin(w \cdot t)^2}{V_{bus} - n_1 \cdot V_o - V_p \cdot \sin(w \cdot t)}}{(V_{bus} - 2 \cdot n_2 \cdot V_o) \cdot (L_1 + n_k \cdot L_1)^2 + \frac{4 \cdot L_o \cdot n_2^2 \cdot V_p^2 \cdot \sin(w \cdot t)^2}{V_{bus}} \cdot \left(L_1 - \frac{n_k \cdot L_1 \cdot n_1 \cdot V_o}{V_{bus} - n_1 \cdot V_o - V_p \cdot \sin(w \cdot t)} \right)} dt \ldots$$

$$+ \int_{t_x}^{\frac{T}{4}} \frac{4 \cdot L_o \cdot n_2^2}{(L_1 + n_k \cdot L_1) \cdot (V_{bus} - 2 \cdot n_2 \cdot V_o)} \cdot \frac{V_p^2 \cdot \sin(w \cdot t)^2}{V_{bus} - V_p \cdot \sin(w \cdot t)} dt$$

$$0 \le t_x \le \frac{T}{4} \qquad t_x = \frac{1}{w} \cdot \operatorname{asin}\left(\max\left(0, \min\left(1, \frac{V_{bus} - \frac{L_1 + n_k \cdot L_1}{L_1} \cdot n_1 \cdot V_o}{V_p} \right) \right) \right)$$

$F2(L_o, L_1, n_1, V_p, V_{bus}, t_x) := \text{Find}(V_{bus}, t_x)$

Intermediate bus voltage: $V_{dcm}(L_o, L_1, n_1) := F2(L_o, L_1, n_1, V_p, V_{bus}, t_x)_0$

Fig.3-6. MathCAD sheet for intermediate bus voltage under DCM

Figure 3-7 illustrates the bus voltage over output inductance when DC/DC cell under DCM, obtained from above MathCAD file. This figure shows the maximum bus voltage since the bus voltage under DCM is higher than under CCM, and it does not change with load change. We can see that the bus voltage increase with transformer T1 turn ratio n1 and output inductance Lo, reverse with T1 primary inductance L1. Hence, in order to achieve lower bus voltage, L1 should be as big as possible, while n1 and Lo should be as small as possible.

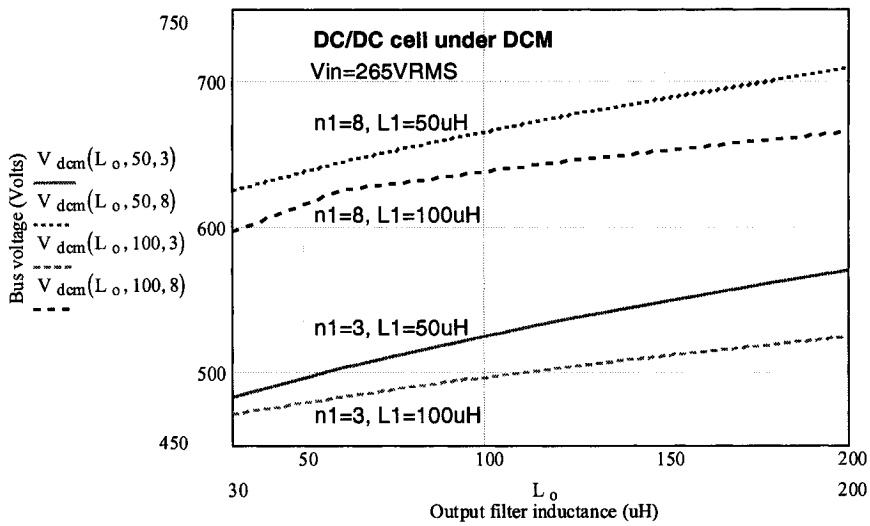


Fig.3-7. Bus voltage Vs output inductance with DC/DC cell under DCM

One of interesting parameters is the direct transferred power from input to output end. The more direct transferred power, the less current stresses on power components, resulting in higher efficiency. Based the above equations, MathCAD can be implemented to carry out this analysis. Figure 3-8 shows the document for this calculation.

MathCAD Calculation sheet for direct transferred power

Parameters of the circuit:

Input: $V_p := 375$ $T := \frac{1}{50}$ $w := \frac{2\cdot\pi}{T}$

Output: $V_o := 28$ $P_o := 150$

Conversion efficiency: $\eta := 0.8$

Switching frequency (MHz): $F_s := 0.1$ $T_s := \frac{1}{F_s}$

Flyboost transformer:

Primary magnetizing inductance (uH): $L_1 := 50$

The rate of leakge inductance and L1: $n_k := 0.1$

Turn ratio (primary:secondary): $n_1 := 3$

DC-DC parallel/series forward cell:

Transformer turn ratio (primary:secondary): $n_2 := 1.5$

Output inductor (uH): $L_o := 100$

Initial guess value for variables:

Intermediate bus voltage: $V_{bus} := 600$

Mode boundary: $t_x := 0.003$

Duty cycle: $D := 0.3$

Direct transferred power: $P_{direct} := 1.649\times 10^{-5}$

Define solve block:

Given

$$V_{bus}\cdot\int_{t_x}^{\frac{T}{4}} \frac{(1+n_k)\cdot\sin(w\cdot t)^2}{V_{bus}-V_p\cdot\sin(w\cdot t)}\,dt = \frac{P_o}{\eta}\cdot\frac{T\cdot(L_1+n_k\cdot L_1)^2}{2\cdot V_p{}^2\cdot D^2\cdot T_s\cdot L_1} - \frac{P_{direct}}{D^2} - n_k\cdot V_{bus}\cdot\int_0^{t_x}\frac{\sin(w\cdot t)^2}{V_{bus}-n_1\cdot V_o-V_p\cdot\sin(w\cdot t)}\,dt$$

$$D = \frac{2n_2\cdot V_o}{V_{bus}} \qquad t_x = \frac{1}{w}\cdot\asin\left(\max\left(0,\min\left(1,\frac{V_{bus}-\frac{L_1+n_k\cdot L_1}{L_1}\cdot n_1\cdot V_o}{V_p}\right)\right)\right)$$

$$P_{direct} = D^2\cdot\int_0^{t_x}\left(1-\frac{n_k\cdot n_1\cdot V_o}{V_{bus}-n_1\cdot V_o-V_p\cdot\sin(w\cdot t)}\right)\cdot\sin(w\cdot t)^2\,dt \qquad V_{bus} > V_p + 2\cdot n_2\cdot V_o$$

$$F3(V_p, n_1) := \mathrm{Find}(V_{bus}, D, t_x, P_{direct})$$

Percentage of direct transferred power:

$$P_{ccm}(V_{in}, n_1) := \frac{2}{T}\cdot\frac{2V_{in}{}^2\cdot T_s\cdot L_1}{(L_1+n_k\cdot L_1)^2}\cdot\frac{F3(V_p,n_1)_3}{P_o}\cdot\eta\cdot 100$$

Fig.3-8. MathCAD sheet for direct transferred power

Figure 3-9 shows the result of direct transferred power percentage over input voltage and turn ratio n_1. Smaller n_1 means lengthened flyback mode, more direct transferred power via T_1. And at high line voltage, more power is transferred through T_1 directly to load. It can improve the efficiency at high line voltage end, and limit the maximum bus voltage, since more input power is transferred to output instead of stored in bus capacitors.

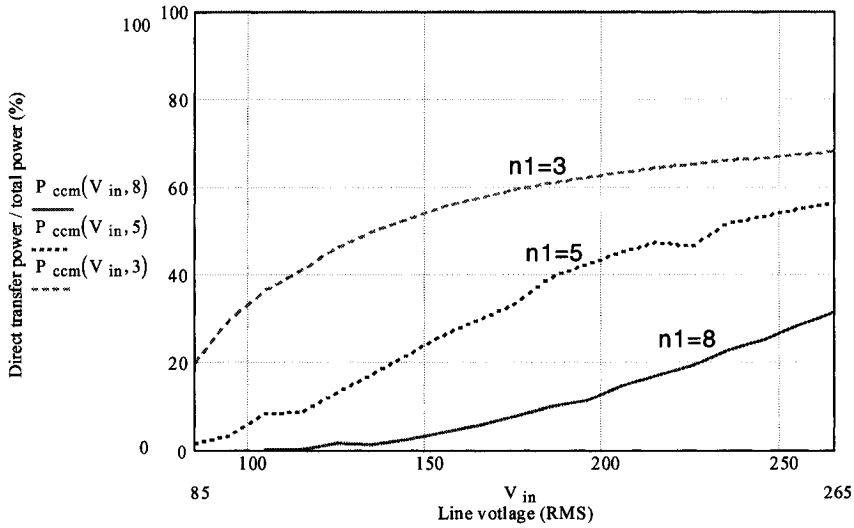


Fig.3-9. Direct transferred power percentage over input voltage

From above analysis, we can see that the turn ratio n_1 is a very important parameter. It should be as small as possible to achieve higher efficiency and lower bus voltage. If bus voltage is too low, it may let PFC cell enter CCM. Since there is no active control over PFC cell, it will cause very high non-controlled peak current through power components if PFC cell enters CCM. It limits the minimum n_1 value.

3.3.4 Features

By adding another discharging path to PFC inductor, the proposed topology benefits from following features:

- Parallel Power Transfer: At flyback mode, the input power is directly transferred to the load. This part of power is processed by switch only once. It results in lower current stress on power components, and higher efficiency.
- Automatic intermediate bus voltage limiting: Only when the rectified input voltage is higher than V_{cs} - n_1*V_o, the bus capacitors can be charged by the input power. The higher DC bus voltage, the less charging power to bus capacitors. And the maximum DC bus voltage is limited to ($V_{in,peak}$ + n_1*V_o) for any load condition. So it will limit the voltage stress on the power components.
- Automatic voltage clamping: when switch S is turned off, its voltage is clamped by the intermediate bus voltage through diode D_2. So the switch is free of voltage spike caused by leakage inductance.

3.4 Practical Design Considerations

In practical design, there are some considerations needed attention, including controller and leakage inductance. Here those issues are discussed in detail. And one design example is presented to show the design procedure.

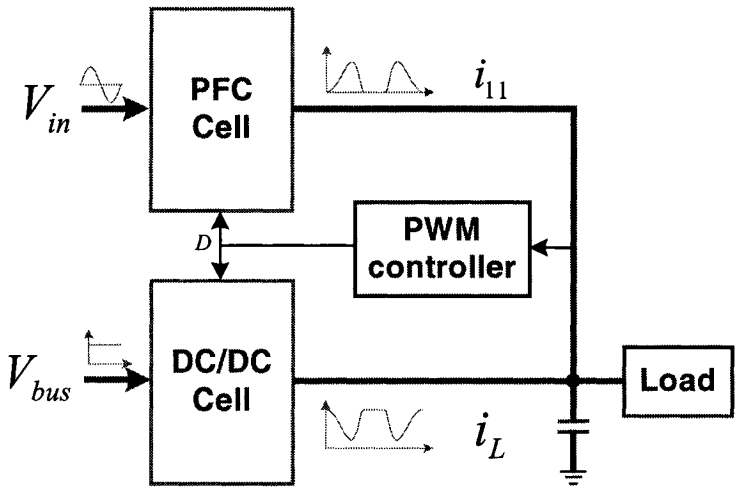
3.4.1 Controller design

When operating under DCM, the PFC cell will automatically achieve high power factor, as other single stage PFC schemes. So there is no active control required for high power factor. The controller can be optimally designed only to meet output voltage requirement based on DC-DC conversion cell.

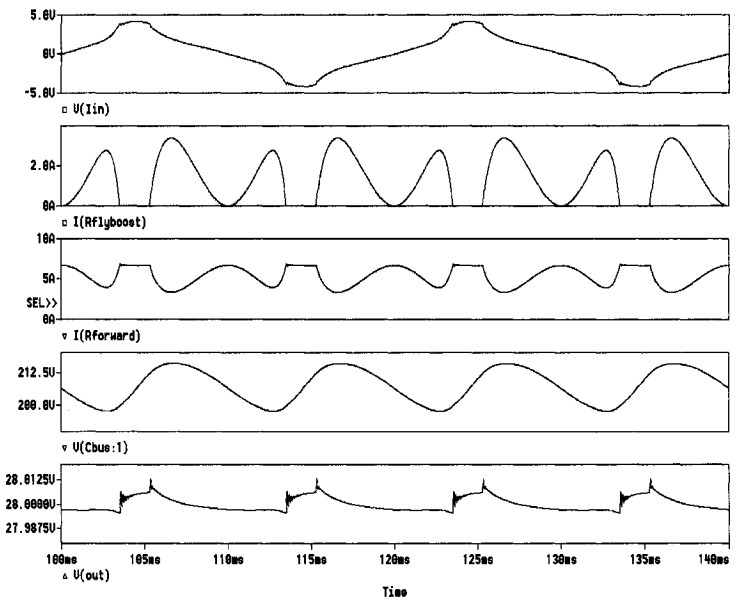
But since there are two load power flow paths, its operation is a little different. Figure 3-10(a) shows the block diagram of this parallel scheme, in which we separate PFC cell and DC-DC cell to two independent and parallel converters. So we can treat it like two parallel converters: one with sinusoid input voltage and pulsing output current; another with constant DC input voltage. Those converters share one controller.

Based on this analysis, we built the averaging model of this topology by Switched Inductor Model approach. Detailed modeling procedure will discuss later. The simulation result by Pspice® is shown in Fig. 3-10(b).

In Fig. 3-10(b), we can see that there are clearly two operation modes. And the output current from PFC cell is pulsing according to input voltage, while the output current from DC-DC cell vary in reverse direction to keep output voltage constant. There is small twice time line frequency ripple in output voltage, about 17.2mVp-p or 0.06% for 28VDC output, which is caused by ripple voltage across bus capacitor. The changing of PFC cell current causes some ripple in output voltage, but its influence is very small.



(a) Block diagram



(b) Simulation result

Trace 1: Input current Trace 2: T1 secondary current (i_{11})

Trace 3: DC-DC cell current i_L Trace 4: bus voltage ripple (Vp-p=18V)

Trace 5: output voltage ripple (Vp-p=17.2mV)

Fig. 3-10. Parallel power transfer

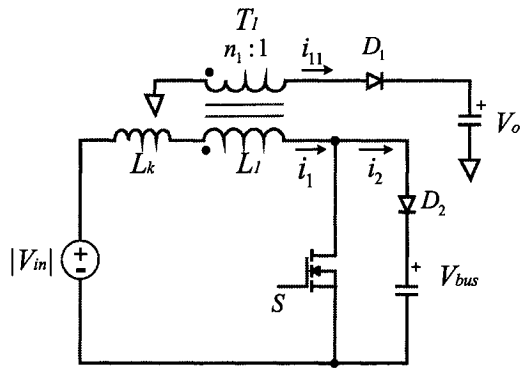
For simplicity, we can think it in this way: the controller just controls the DC-DC cell to achieve tight output voltage regulation, while the power transferred by parallel PFC cell will reduce the actual instantaneous load on DC-DC converter. It means we can regard the parallel PFC converter as a DC-DC converter with instantaneously changing load. The output voltage ripple will depend on the load regulation capability of the DC-DC converter.

Typical voltage mode and current mode PWM control IC can be used here. In our design, current mode control IC UC3844 is chosen because of its cycle-to-cycle current limit function and fast transient response feature.

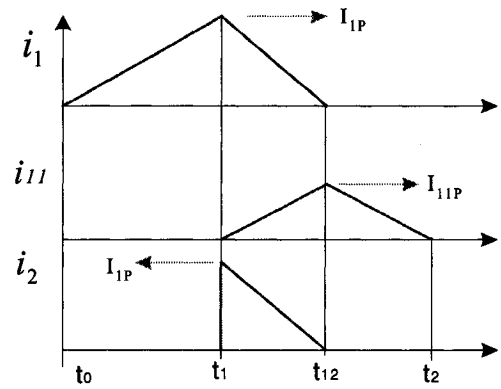
3.4.2 Influence of transformers' leakage inductance

Since transformer T_2 primary windings in DC-DC cell are clamped by two bus capacitors during switch S OFF period, T_2 leakage inductance will not bring voltage spike problem over the switch and its influence can be neglected.

But the leakage inductance of transformer T_1 in PFC cell will cause some influence needed some attention. Figure 3-11(a) shows the equivalent circuit of the PFC cell, where two bus series-connected capacitors are replaced by one capacitor, and L_k represents leakage inductance of T_1.



(a) Equivalent circuit of PFC cell



(b) Operational current waveform

Fig. 3-11. Influence of leakage inductance of PFC transformer T_1

The influence of T_1 leakage inductance happens during S off interval. When S is OFF at t_1, leakage inductor L_k of T_1 will keep the current flowing through D_2 to bus capacitor. The voltage across L_k and T_1 will be V_{bus}-$|V_{in}(t)|$. If T_1 discharges its magnetizing energy to bus capacitor, the voltage across its primary winding will be (V_{bus}-$|V_{in}(t)|$)$L_1/(L_1+L_k)$. When this voltage is higher than n_1V_o, T_1 will discharge its magnetizing energy to output through D_1 and its primary winding voltage is clamped to

n_1V_o. It is referred to flyback mode. If $(V_{bus}-|V_{in}(t)|)L_1/(L_1+L_k)$ is less than n_1V_o, then no current flow through D_1, as in boost mode discussed in section 3.2.

The operation under boost mode is the same as without leakage inductance, except for the inductance value is changed. Under flyback mode, the operation is somehow different to the above analysis. The typical operational waveforms are showed in Fig. 3-11(b).

During t_1-t_{12}, we have

$$L_k \frac{di_1(t)}{dt} = -\left(V_{bus} - |V_{in}(t)| - n_1 V_o\right) \tag{3.23}$$

$$\frac{di_{11}(t)}{dt} = n_1\left(\frac{V_{bus} - |V_{in}(t)| - n_1 V_o}{L_k} - \frac{n_1 V_0}{L_1}\right) \tag{3.24}$$

During t_{12}-t_2, we have

$$i_1(t) = 0 \tag{3.25}$$

$$L_{11}\frac{di_{11}(t)}{dt} = -V_O \tag{3.26}$$

From above equation, we can calculate the power to bus capacitor and to the load, and modify equations in last section to get more accurate equations to include leakage inductance. The modified equation for CCM is given as:

$$\int_{t_x}^{\frac{T}{4}} \frac{(L_1+L_k)V_{bus}\sin(\omega t)^2}{L_k\left(V_{bus}-V_p\sin(\omega t)\right)}dt - \int_0^{t_x} \frac{L_k\left(n_1V_o - V_{bus}\right)\sin(\omega t)^2}{L_k\left(V_{bus}-n_1V_o-V_p\sin(\omega t)\right)}dt = \frac{P_oT\left(L_1+L_k\right)^2}{2T_sL_1V_p^2D^2} - \frac{t_x}{2} + \frac{\sin(2\omega t_x)}{4\omega} \tag{3.27}$$

Comparing to previous analysis in section 3.3, we can see that there will always be some current to charge intermediate capacitors, even under flyback mode. It will bring follow influence to this topology:

- Smooth the transition procedure from flyback mode to boost mode, since the leakage inductor limits the current transmitting from T_1 primary side to its secondary side. It will bring benefits to the control design, since the actual load of the DC-DC cell is not changed abruptly;
- Relieve the recovery trouble of secondary diode D_1, because leakage inductor L_k will limit the di/dt value of T_1 secondary current. It will relieve the EMI issue;
- Increase the maximum intermediate bus voltage, since there are always some current to charge the bus capacitor under both flyback and boost mode. But we can reduce the turn ratio of T_1 to eliminate this influence.

3.4.3 Magnetizing inductance of T_1 primary winding

This magnetizing inductance will influence the maximum bus voltage V_{bus} value and current stresses on power switches, as discussed in section 3.3. The higher the inductance value, the lower the V_{bus} and the current stresses. But it should also be low enough to keep the PFC cell operating under DCM at full load condition. The primary inductance and turn ratio of T_1 needs to be optimized to achieve the lowest bus voltage. Steady-state equations of bus voltage obtained in last section can be implemented here to find the optimized parameters. It is shown in the later example design.

3.4.4 Intermediate bus voltage

The voltage stresses on all power switches depend on this voltage. So it should be as low as possible to reduce the voltage rating of power components, which will result in low cost and higher efficiency. However, V_{bus} should be high enough to keep PFC under DCM at the lowest input voltage and full load.

3.4.5 DC/DC conversion cell

The DC/DC cell can be designed following typical forward converter design procedure. It prefers to let it operate under CCM at heavy load condition to reduce the current stress, and under DCM at light load to reduce the maximum bus voltage.

3.5 Design example

Here one design example is given to show the optimized design procedure for this parallel PFC converter. The design specifications are listed as following:

- Input voltage range: 85V ~ 265VRMS
- Output voltage: 28VDC
- Output power: 150W
- Switching frequency: 100kHz

Since the bus voltage is the most important parameter in this application, out optimized goal is to achieve the lowest bus voltage. The design procedure is given as:

3.5.1 Determine the maximum duty cycle

The maximum duty cycle should be less than 0.5 in order to reset transformer T_2 during main switch off period, just like typical forward converter. In order to have some room for transient response, we choose it to be 0.42 at the lowest line input.

3.5.2 Determine the minimum bus voltage at low line

Based on Eq. (3.12), we can calculate the required minimum bus voltage to keep PFC cell under DCM at the lowest input voltage and full load condition. When the lowest line voltage is 85VAC, the minimum bus voltage is equal to:

$$V_{bus(\min)} = \frac{V_p}{1 - D_{\max}} = \frac{85 \cdot 1.414}{1 - 0.42} = 207V$$

3.5.3 Design the parallel/Series forward DC-DC cell

Once the minimum bus voltage and the maximum duty cycle are obtained, the parameters of DC-DC cell are determined. Assume DC-DC cell operates under CCM at full load condition. Based on Eq. (3.13), the turn ratio of DC-DC transformer T_2 can be obtained by:

$$n_2 = \frac{D_{\max} V_{bus(\min)}}{2(V_o + V_{diode})} = \frac{0.42 \cdot 207}{2(28 + 0.7)} = 1.51$$

V_{diode} is the voltage drop across secondary diode, assuming to be equal to 0.7V. Other parameters of DC/DC cell, including output capacitor and inductor, can be

determined following conventional forward converter design procedure. Here, we select 100uH for output inductance.

3.5.4 Design the PFC transformer T_1

According to above analysis, T_1 primary inductance, L_1, should be as high as possible, while its turn ratio, n_1, should be as small as possible. And the critical operation condition happens at full load and the lowest line voltage. In order to achieve optimized parameter, we can put all parameters obtained above into Eq. (3.27) to get the interrelationship curve between L_1 and n_1. In order to get more accurate result, the calculation includes the influence of leakage inductance, which is assumed to be 10% of primary inductance. Figure 3-12 shows the MathCAD calculation sheet.

Fig. 3-13 shows the calculation result. From this figure, we find the best parameter should be around this point: L_1=57uH and n_1=4. But this pair parameter will leave little voltage margin for 600V power MOSFET. We select L_1=50uH and n_1=3 here as a tradeoff. Adding the leakage inductance, the total inductance value of T_1 primary winding is 55uH.

MathCAD calculation sheet for interlationship between L1 and n1

Parameters of the circuit:

Input: $V_p := 120$ $T := \frac{1}{50}$ $w := \frac{2 \cdot 3.14159}{T}$

Output: $V_o := 28$ $P_o := 150$

Conversion efficiency: $\eta := 0.8$

Switching frequency (MHz): $F_s := 0.1$ $T_s := \frac{1}{F_s}$

Flyboost transformer:

Primary magnetizing inductance (uH): $L_1 := 50$

The rate of leakge inductance and L1: $n_k := 0.1$

Turn ratio (primary:secondary): $n_1 := 4$

DC-DC parallel/series forward cell:

Transformer turn ratio (primary:secondary): $n_2 := 1.5$

Output inductor (uH): $L_o := 100$

Initial guess value for variables:

Intermediate bus voltage: $V_{bus} := 207$

Mode boundary: $t_x := 0.0025$

Duty cycle: $D := 0.4$

Given

$$\frac{D^2 \cdot T_s \cdot V_{bus} \cdot V_p^2}{2 \cdot (L_1 + n_k \cdot L_1)} \cdot \int_{t_x}^{\frac{T}{4}} \frac{\sin(w \cdot t)^2}{V_{bus} - V_p \cdot \sin(w \cdot t)} dt = \frac{P_o}{\eta} \cdot \frac{T}{4} - \frac{V_p^2 \cdot D^2 \cdot T_s \cdot L_1}{2 \cdot (L_1 + n_k \cdot L_1)^2} \int_0^{t_x} \sin(w \cdot t)^2 dt \ldots$$

$$0 < D < 0.5 \qquad + \frac{n_k \cdot L_1 \cdot T_s \cdot (n_1 \cdot V_o - V_{bus}) \cdot V_p^2 \cdot D^2}{2 \cdot (L_1 + n_k \cdot L_1)^2} \cdot \int_0^{t_x} \frac{\sin(w \cdot t)^2}{V_{bus} - n_1 \cdot V_o - V_p \cdot \sin(w \cdot t)} dt$$

$$t_x = \frac{1}{w} \cdot \operatorname{asin}\left(\max\left(0, \min\left(1, \frac{V_{bus} - \frac{L_1 + n_k \cdot L_1}{L_1} \cdot n_1 \cdot V_o}{V_p}\right)\right)\right) \qquad D = \frac{2 n_2 \cdot V_o}{V_{bus}} \qquad V_{bus} > \frac{V_p}{1 - D} \qquad 0 \le t_x \le \frac{T}{4}$$

$F8(L_1, n_1, V_p, P_o, D, V_{bus}, t_x) := \text{Find}(L_1, n_1, t_x)$

PFC transformer magnetizing inductance $L(n_1) := F8(L_1, n_1, V_p, P_o, D, V_{bus}, t_x)_0$

Fig.3-12. MathCAD sheet for interrelationship between L_1 and n_1

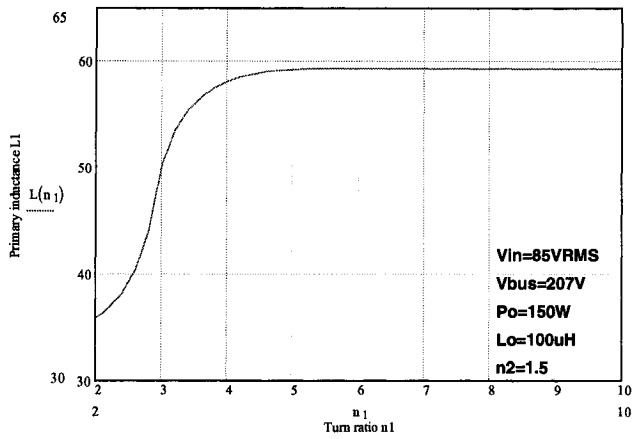


Fig. 3-13. Interrelationship between L1 and n1

3.5.5 Check the maximum bus voltage at high line voltage

The maximum bus voltage occurs at the highest line voltage and light load condition. We can use Eq. (3.22) to calculate this value, with results shown in Fig. 4. We can see that the maximum bus voltage for above parameters is about 520V. It leaves 80V margin for 600V power MOSFET.

3.6 Experimental Verifications

A 150w@28VDC prototype based on above parameters was built in the lab. Figure 3-14 shows the picture of the prototype. On the left side, there are input rectifier, common and differential input filters. In the front middle, the vertical small PCB is the controller based on UC3842. Behind the control board, there are two intermediate bus caps, main switch with heat sink, flyboost transformer, DC-DC transformer. On the right

side of the prototype, there are output inductor, output caps, and output fast recovery diode with heat sink. In order to simplify test and measurement, there are a lot of test point and spare space.

Figure 3-15 shows the input voltage and current waveforms for 110VAC input and 28VDC/150W output. The measured Power factor of input current is 99.6%, with the 6.4% THD (total harmonic distortion). The measured efficiency is about 82%. The input current waveform is very close to perfect sinusoidal waveform and in phase with input voltage waveform.

Figure 3-16 shows the input voltage and current waveforms for 110VAC input and 28VDC 75W output. The measured Power factor of input current is 96.7%. Due to direct power transfer feature, the input current waveform is completely different to typical single stage PFC converter. The top of the current is flat with reduced peak current. It will help to reduce the current stress over power stage components.

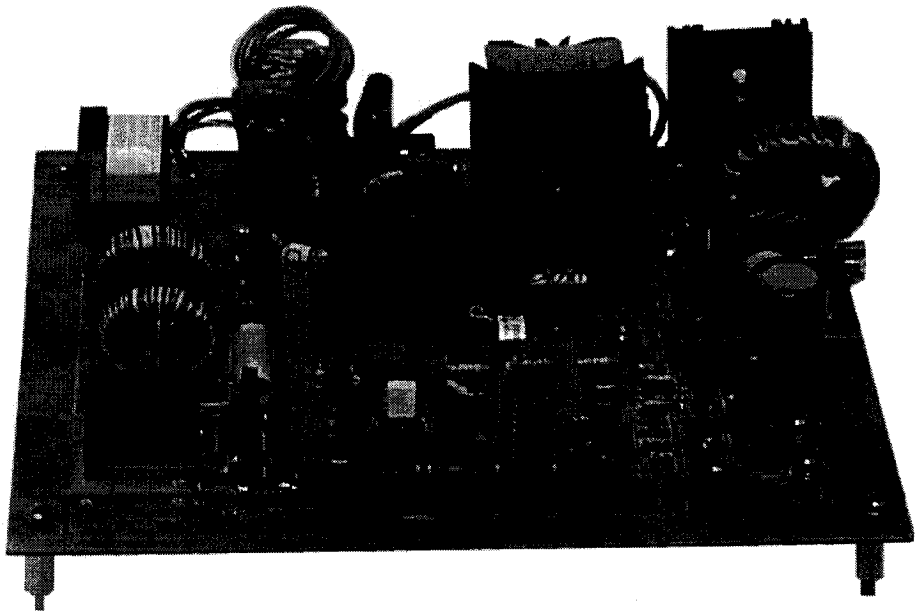
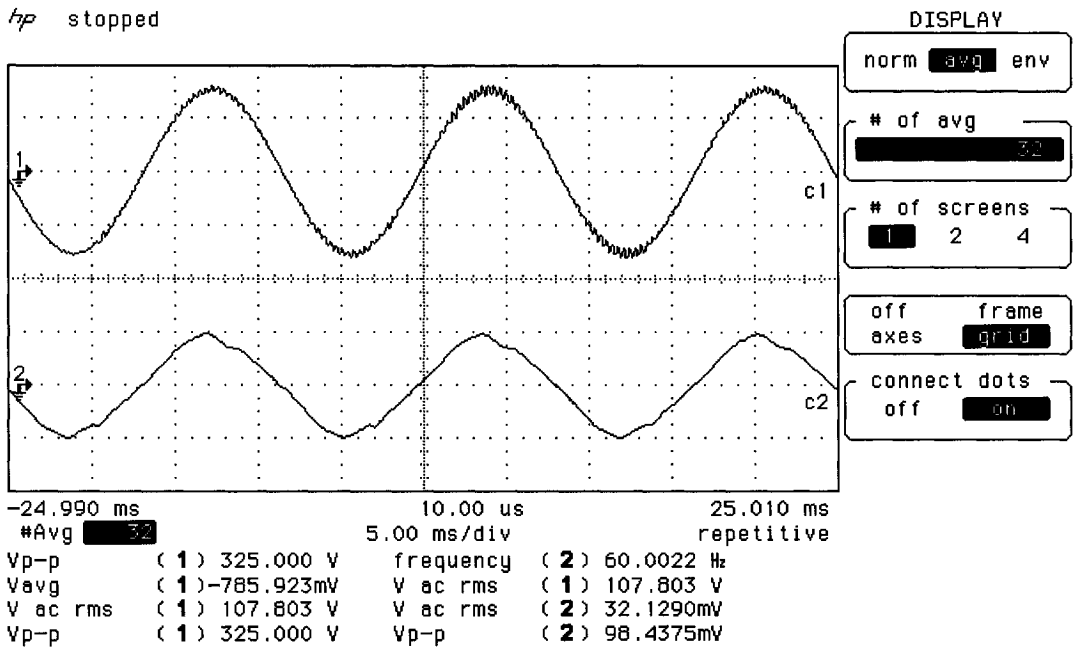
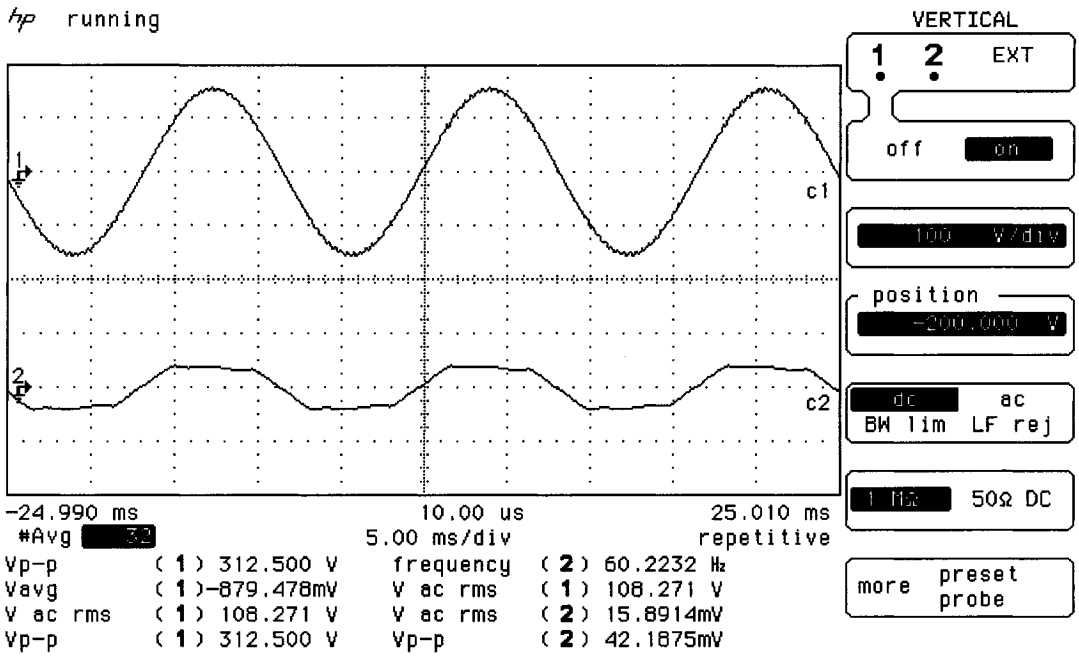


Fig. 3-14. Prototype based on the flyboost parallel/series forward converter.



Upper trace: Line voltage (100V/div) Bottom trace: Line current (2A/div)

Fig. 3-15 Measured waveform at 110V AC input and 150W output

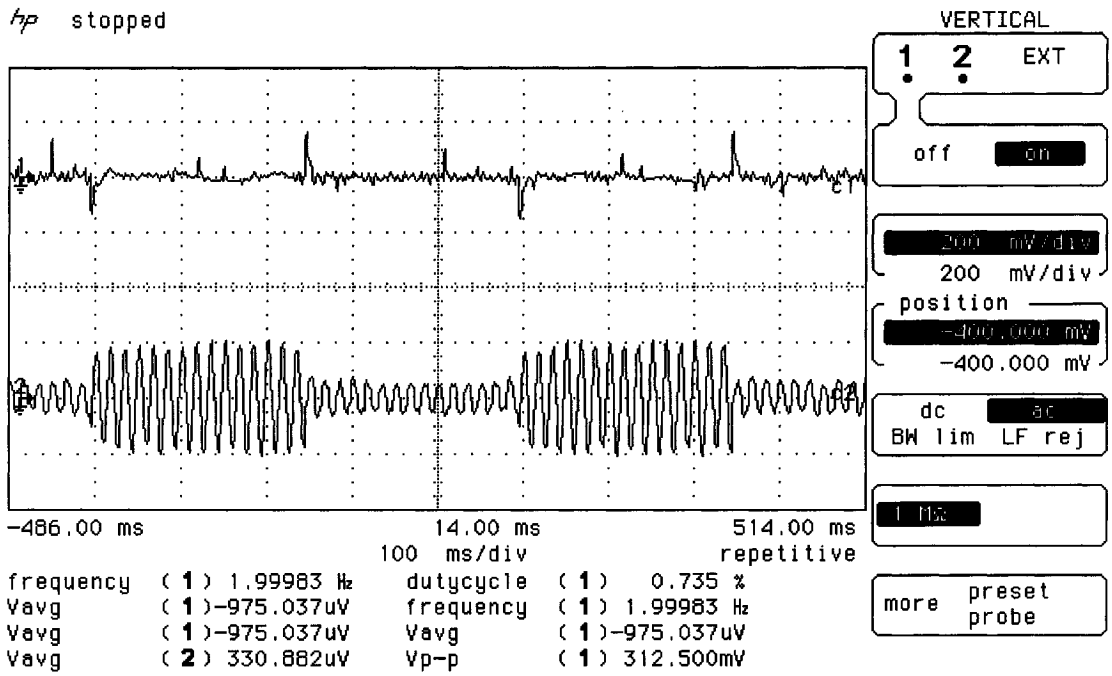


Upper trace: Line voltage (100V/div) Bottom trace: Line current (2A/div)

Fig. 3-16 Measured waveform at 110V AC input and 75W output

One concern about the direct power transfer PFC scheme is the output low frequency ripple and transient response. Because there are two parallel power transfer paths, and some input pulsing power is transferred to output end. So it is true that output ripple consists of input low frequency ripple. But the control loop bandwidth of this topology is designed to be high enough to minimize this low frequency ripple. And fast transient response is also achieved by wide loop gain bandwidth.

In order to verify this feature, step-changing load between 40w and 140w is applied to this prototype, and Fig. 3-17 shows the measured output voltage ripple and input current. the input voltage and current waveforms for 110VAC input and 28VDC/75W output. The steady state output voltage is very small. And the voltage spike due to dynamic load is about 312mV, only 1.1% of output voltage.



Upper trace: output voltage ripple Bottom trace: input current

Fig. 3-17 dynamic load testing

Figure 3-17 also shows the change of input current under transient load condition. The change of the input current waveform is smooth, without overshoot and undershoot spike. So the impact to input voltage is very small.

The measured the maximum intermediate bus voltage is about 520V for universal input (85Vrms to 265Vrms) applications. So the voltage across each intermediate bus cap is about 260V, and 300V-rating bulk cap can be chosen for this application. The voltage stress on main switch is 520V, with 80V margin for popular and cheap 600V rating power MOSFET.

Those test data verify the operation of this single stage power factor correction converter. It is clear that this parallel single stage PFC converter can achieve good power factor with high efficiency.

3.7 Summary

There are several advantages in parallel/series forward DC-DC conversion topology, especially its automatically voltage clamp feature. In this chapter, this circuit is integrated with flyboost PFC cell to form one single stage PFC converter. The flyboost parallel/series forward PFC converter inherits advantages from both basic circuit, and better performance can be achieved.

Detailed operation and steady state analysis of this topology was provided in this chapter. One design procedure was proposed, and one prototype was developed. Experimental results verified the scheme and analysis method.

Based on the analysis and experimental results, this scheme shows better performance comparing to counterpart schemes. The good performance and low cost makes it an attractive scheme for low to median power universal input applications.

CHAPTER 4

BI-FLYBACK SINGLE STAGE PFC CONVERTER

4.1 Introduction

Compared to two-stage power factor correction (PFC) scheme, the biggest challenge for single stage PFC converter is the stress over power stage components. Even though single stage PFC converter integrates the AC-DC stage and DC-DC stage to reduce the total component count, the total proceeded power by the power stage components in single stage PFC scheme is almost the same as in two-stage scheme. This means that the same power is preceded by fewer components. Therefore the voltage and / or current stresses over single stage PFC scheme will be higher than two-stage scheme. As discussed in previous chapter, there is only one active control loop that is responsible for output voltage. So there is no active control over the intermediate bus voltage, and typical single stage PFC scheme operates under discontinuous conduction mode (DCM) in order to let the intermediate in a suitable range. DCM operation in single stage PFC scheme will cause even higher current stresses.

Higher voltage and / or current stresses require power components with higher power rating. Components with higher power rating normally have poor electrical

parameter. For example, the conductive resistance, $R_{ds,on}$, of 800V MOSFET is much higher than 600V MOSFET with same current rating, and it is also more expensive. In order to make single stage scheme suitable for practical application, the voltage and current stresses must be reduced to the level comparable with two-stage scheme.

In the previous chapters, direct power transfer or parallel power transfer concept with reduced the voltage stresses and current stresses was discussed in detail. This concept can really improve the performance of single stage PFC scheme. By carefully designing the flyboost PFC cell, the intermediate bus voltage can be controlled to be less than $V_{in,peak}+n_1V_o$. For universal input voltage application, this voltage still creates problems for the bulk capacitor. The peak value of the maximum universal input voltage is 375V (equal to 265V*1.414). Normally n_1V_o will be chosen to be equal to the peak value of the minimum input voltage, which is about 120V (85V*1.414). So the intermediate bus voltage will be around 495V (375V+120V), and the minimum voltage requirement for intermediate bus capacitor is about 500V, even with flyboost PFC cell.

Unfortunately, the maximum voltage of the economical bulk capacitor available in today's market is only 450VDC. So two capacitors connected in series are necessary for universal input applications even with flyboost PFC cell. Like the series / parallel forward single stage PFC scheme in previous chapter, the intermediate bus voltage is about 520VDC, and two capacitors are used in series. This solution is not acceptable for some applications due to high cost and large size of bulk capacitor.

So for low cost applications, a voltage reduction solution should be introduced to relieve the intermediate bus voltage. The bus voltage must be controlled to be less than 450VDC at all operation conditions.

The intermediate bus voltage is largely dependant on the PFC cell. For most of single stage PFC scheme, PFC cell operates under DCM to achieve good power factor at input end, which requires the intermediate bus to be high enough to completely discharge PFC inductor/transformer. Some single stage PFC schemes let the PFC cell operate under CCM. But this required special design to achieve higher power factor. Our discussion here will focus on DCM PFC schemes.

Boost topology is the most popular PFC scheme, for both single-stage and two-stage schemes. Most single stage scheme just integrates boost topology with other DC-DC topology. Flyboost PFC cell can be considered as a derived scheme from boost topology. For boost topology, its output voltage (bus voltage) will be at least $V_{in}/(1-D)$. This is the minimum bus voltage required for basic boost steady-stage operation. In order to reduce the bus voltage, voltage source should be introduced to boost inductor charging and / or discharging path as discussed in Chapter 1. A better solution is to add the voltage source in discharging path since it will not influence input current waveform.

Bifred topology, as shown in Fig. 4-1 is a good scheme for universal input voltage applications because of its high power factor and low bus voltage. The DC-DC stage transformer is located in boost inductor charging path. So the intermediate bus voltage can be reduced by the value that is equal to the reflected output voltage by DC-DC transformer. When DC-DC cell operates under DCM, the intermediate bus can be less than 400VDC, but the power component in this topology suffers from high current stresses because the DC-DC cell has to operate under DCM to limit the maximum intermediate bus voltage.

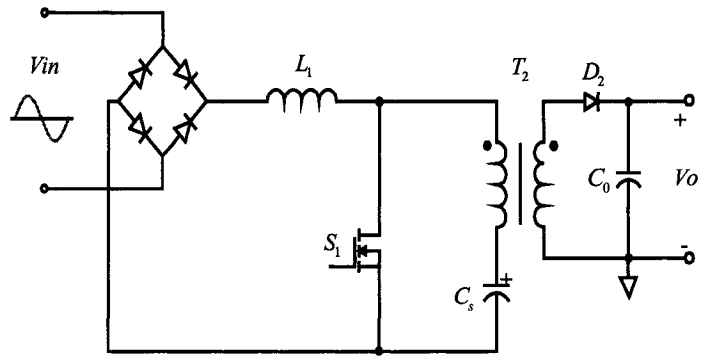


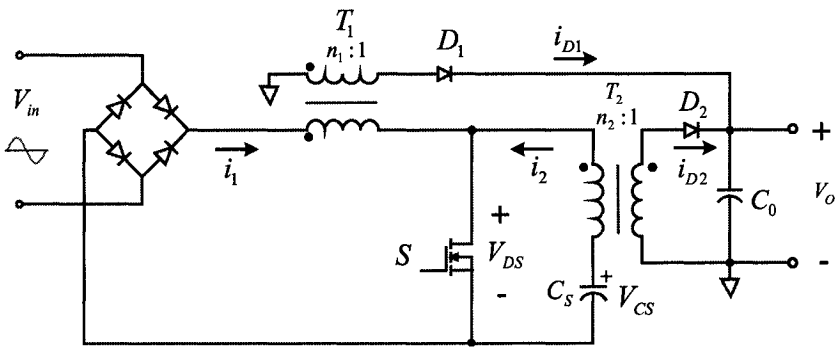
Fig. 4-1. Bifred topology for single stage PFC applications

In this chapter, Bi-flyback topology is introduced for single stage PFC application. This topology is derived from Bifred and Flyboost scheme. It inherits advantages from both schemes to achieve better results. Fig. 4-2(a) shows the basic topology. In order to clearly explain its operation, simplified topology is shown in fig. 4-2(b) with input rectifier section replaced by the voltage source |Vin|. It is clear that this topology consists of two flyback circuits: the first flyback circuit includes transformer T_1, diode $_{D1}$ and switch S, while the secondary flyback circuit is composed of transformer T_2, diode D_2 and switch S. Both flyback circuits share the main switch and output capacitors, which is why this topology is named as Bi-flyback.

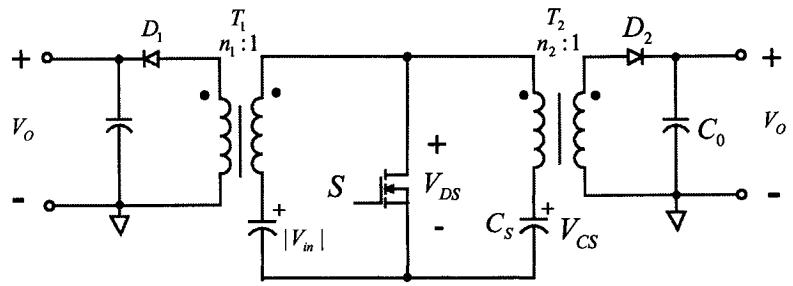
Because two flyback circuits share the main switch, their operations are intermingled with each other, which make its operation complex. However this feature helps this topology overcome the main drawbacks existing in other single stage PFC circuit. Aside from the advantages of the direct power transfer mentioned in the last chapter, this topology can also get the intermediate bus voltage as low as the peak voltage of input voltage. It means the maximum intermediate bus voltage can be less than 400VDC for universal voltage applications, and the voltage stress across main switch will

be less than 600VDC. Both the 450V bulk capacitor and 600V economical MOSFET can be implemented here to meet low cost requirements.

In this chapter, this proposed topology is studied in detail, some control scheme are discussed, and experiments of one prototype is included to show its effectiveness.



(a) Basic topology



(b) Simplified topology

Fig. 4-2. Bi-flyback topology

4.2 Operation Descriptions

In this section, the operation of Bi-Flyback topology is discussed in detail, and some features are derived. As in the previous chapter, the following assumptions are made in order to simplify the analysis:

- No leakage inductance in two transformers
- Voltage across intermediate bulk capacitor (Vcs) is constant
- Output capacitor (Vo) is constant
- All switch components are ideal, without parasitic parameters
- Input voltage is constant during each switching cycle

The Bi-flyback topology in Fig. 4-2(a) consists of two flyback circuits: The first PFC flyback circuit, called PFC flyback here, is composed of transformer T_1, rectifier input bridge, diode D_1, output filter capacitor C_o and power MOSFET S; This cell is the same cell as flyboost PFC cell. The second flyback circuit, called DC-DC flyback, includes transformer T_2, intermediate bus capacitor C_S, diode D_2, output filter capacitor C_o and Power MOSFET S. The first flyback will operate under DCM to achieve high power factor and low current harmonic like most single stage PFC circuit, which means that the current in transformer T_1 is discontinuous. The secondary flyback will operate under CCM to reduce the current stress on MOSFET and diode.

The DC-DC flyback circuit operates like conventional DC-DC flyback circuit, i.e. the transformer will be charged and discharged alternatively. For PFC flyback circuit, its

operation is more complex. The charge path is a simple one, but there are two different discharging paths: one is to output capacitor through secondary diode D_1; another is to intermediate bulk capacitor through transformer T_2. PFC flyback transformer will always look for the low voltage path to discharge its stored magnetizing energy, so the discharging path keeps changing in one line voltage cycle, depending on instantaneous input voltage and intermediate bus voltage.

When the PFC flyback transformer discharges its magnetizing energy to the output capacitor, it works like typical flyback transformer. If it discharges to bulky capacitor, it will be a boost inductor. When T_1 operates like flyback transformer, it is referred to as flyback mode, and as boost mode when T_1 works as boost inductor. So there are two operation modes for this topology:

a). Flyback mode: When $|v_{in}(t)| < V_{CS} + (n_2 - n_1)*V_o$, ($n_1$: turn ratio of T_1, n_2: turn ratio of T_2, V_{CS} is the intermediate bus voltage), PFC flyback transformer T_1 operates as a flyback transformer. When main switch S is ON, T_1 is charged by rectified line voltage linearly. When S is OFF, T_1 will discharge all of its stored magnetizing power to output capacitor through secondary diode D_1. The magnetizing power stored in T_1 during main switch ON period is directly transferred to output, resulting in this part of power being processed only once. The voltage across T_1 primary winding during main switch OFF state will be n_1*V_o.

b). Boost mode: When $|v_{in}(t)| >= V_{CS} + (n_2 - n_1)*V_o$, T_1 works as a boost inductor. When S is ON, T_1 is charged by rectified line voltage linearly. When S is OFF, T_1 will discharge all of its magnetizing power to DC bus capacitor through DC-DC flyback transformer T_2. The current through T_2 will be reflected to output, causing this part power

to be processed once. The power stored in DC bus capacitor will be transferred to output by DC-DC conversion cell, with this part of power being processed twice. The voltage across T_1 primary winding during main switch OFF state will be $V_{CS} + n_2*V_o - |V_{in}|$, which is less than n_1*V_o.

The operation modes over one line cycle are shown in Fig. 4-3.

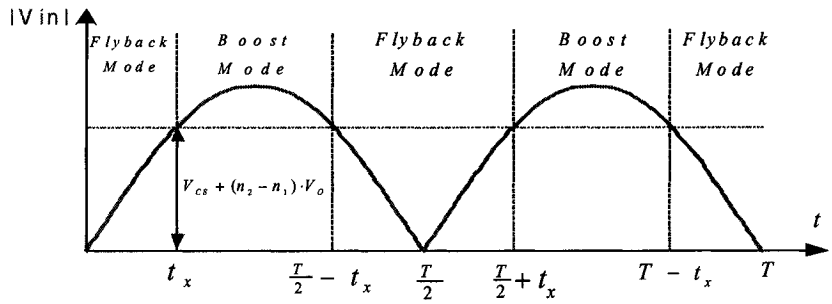


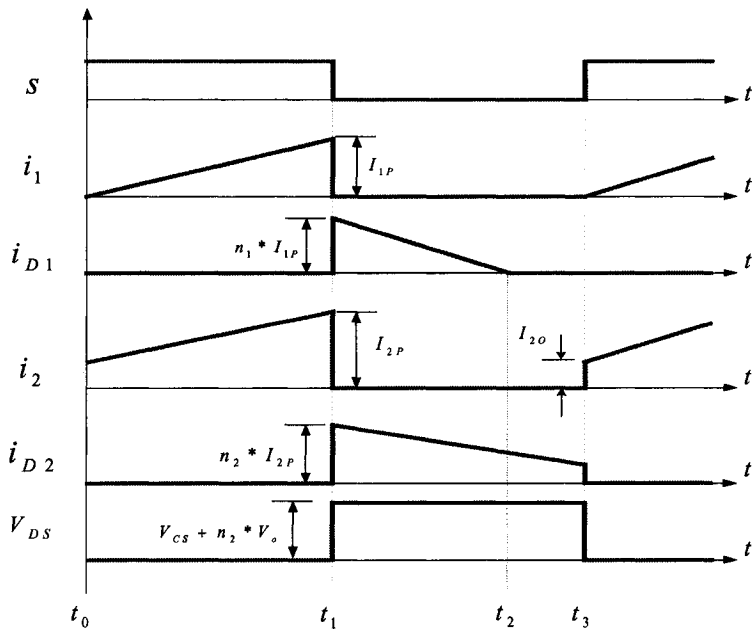
Fig. 4-3 Operation mode in one line cycle

The boundary time for two operation modes is when instantaneous input voltage is equal to $V_{cs}+(n_2 - n_1)*V_o$. When instantaneous input voltage is less than that voltage, Bi-Flyback will operate at Flyback mode; it will run under boost mode, while instantaneous input voltage is higher than that critical value. Detailed analysis of its operation is provided below. This topology will automatically control the intermediate bus voltage like other topologies with flyboost PFC cell, and more power is directly transferred to output through transformer T_2 in this topology, since some input power is transferred to output under boost mode.

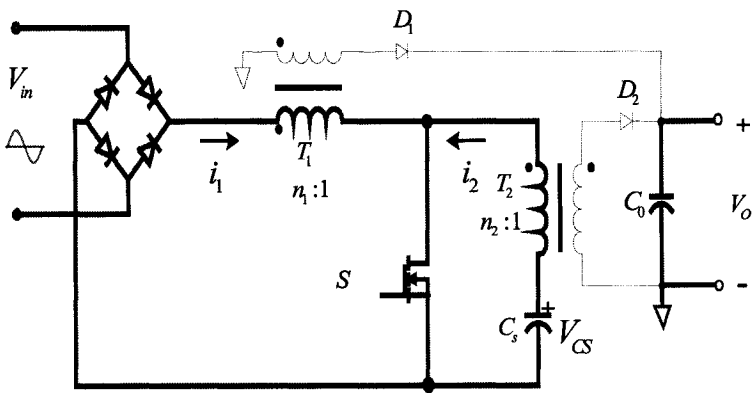
The operations of two different modes are described respectively. The following discussion details the operation of the Bi-flyback topology.

4.2.1 Flyback Mode Operation

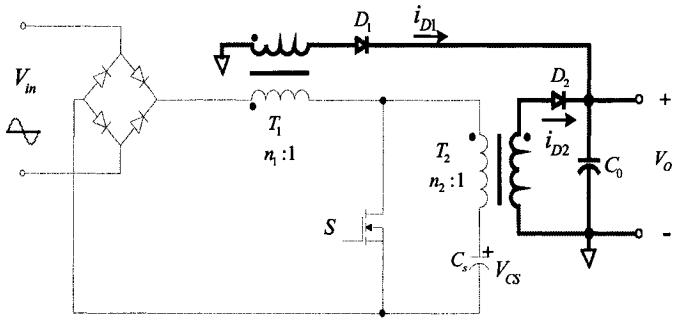
When rectified line voltage $|V_{in}(t)|$ is less than $V_{CS}+n_2V_o-n_1V_o$ (n_1: the turn ratio of T_1, n_2: the turn ratio of T_2), Transformer T_1 works like a flyback transformer, and the topology operates like two independent flyback converters.



(a) Operation waveforms



(b) Equivalent circuit during ON period



(c) Equivalent circuit during OFF period

Fig. 4-4. Operation of flyback mode

All input power during this mode is directly transferred to the load through T_1. Meanwhile, the DC-DC flyback cell will deliver some power from intermediate capacitor to load, in order to keep tight output voltage regulation. The equivalent circuits and operational waveforms are shown in Fig. 4-4.

We assume that PFC flyback will operate under DCM, and DC-DC flyback will operate under CCM. So each switching cycle can be divided into three operation intervals:

Interval 1 ($t_o \sim t_1$): the main switch is turned on at t_o, the rectified line voltage |Vin| is applied to the primary winding of PFC flyback transformer T_1. The current in T_1, i_1 in Fig. 4-4, will increase linearly, and the input power is stored in flyboost transformer as magnetizing energy. The voltage across storage capacitors is applied to DC-DC flyback transformer T_2, which will cause its current (i_2 in Fig. 4-4) to linearly increase as well. Since PFC cell operates at DCM, i_1 will increase from zero. i_2 will increase from some value because DC-DC cell is assumed to operate under CCM.

Based on above analysis, the following equation can be obtained:

$$\frac{di_1}{dt} = \frac{|V_{in}|}{L_1} \tag{4.1}$$

$$\frac{di_2}{dt} = \frac{V_{cs}}{L_2} \tag{4.2}$$

$$i_1(t_0) = 0 \tag{4.3}$$

$$i_2(t_0) = i_2(0) \tag{4.4}$$

$$i_1(t_1) = \frac{DT_S |V_{in}(t)|}{L_1} \tag{4.5}$$

$$i_2(t_1) = \frac{DT_S V_{CS}}{L_2} + i_2(0) \tag{4.6}$$

$$\Delta t_1 = t_1 - t_0 = DT_S \tag{4.7}$$

Where, D is duty cycle, and Ts is the switching cycle, L_1 is the primary magnetizing inductance of transformer T_1, and L_2 is the primary inductance of transformer T_2, i_1 and i_2 are the currents through T_1 and T_2 primary winding respectively.

Interval 2 ($t_1 \sim t_2$): the main switch is turned off at t_1, PFC flyback transformer T_1 will discharge through its secondary winding and deliver its stored magnetizing energy to the output through diode D_1, since the voltage across T_1 will be less in this path than another boost discharging path. Output voltage is applied to T_1 secondary winding, and the current in the PFC transformer secondary winding (i_{D1}) will decrease linearly. The current in DC-DC flyback transformer T_2 secondary winding (i_{D2}) will decrease linearly also, since output voltage is applied to T_2 secondary winding.

At t_2, all magnetizing energy in PFC flyback transformer $_{T1}$ is transferred to the load, and its current i_{D1} reaches zero. The block diode D_1 will prevent this current from

going to negative. The current in DC-DC flyback transformer T_2 (i_{D2}), will continue to decrease.

The voltage across switch S, V_{DS}, is equal to $V_{CS}+n_2V_o$, which is higher than $|V_{in}(t)|+n_1V_o$. The input rectifier bridge is blocked by the voltage difference between input and V_{DS}.

Based on above analysis, the following equation can be obtained:

$$\frac{di_{D1}}{dt}=\frac{V_o}{L_{11}} \tag{4.8}$$

$$\frac{di_{D2}}{dt}=\frac{V_o}{L_{22}} \tag{4.9}$$

$$i_{D1}(t_2)=0 \tag{4.10}$$

$$i_{D2}(t_2)=n_2 i_2(t_1)-\frac{\Delta t_2 V_O}{L_{22}} \tag{4.11}$$

$$\Delta t_2=t_2-t_1=\frac{n_1 i_1(t_1) L_{11}}{V_0} \tag{4.12}$$

Where, L_{11} is the secondary magnetizing inductance of transformer T_1 ($=L_1/n_1/n_1$), and L_{22} is the secondary inductance of transformer T_2 ($=L_2/n_2/n_2$), i_{D1} and i_{D2} are the currents through T_1 and T_2 secondary winding respectively.

Interval 3 ($t_2 \sim t_3$): At t_2, all magnetizing energy in T_1 is transferred to the load. Current i_{D1} reaches zero and diode D_1 keeps it at zero. Output voltage is still applied to T_2 secondary winding, so the current in T_2 secondary winding, i_{D2}, continues to decrease until the switch is turned on at t_3. Then a new switching cycle begins. Switching period T_S is equal to t_3-t_0.

$$\frac{di_{D1}}{dt} = 0 \tag{4.13}$$

$$\frac{di_{D2}}{dt} = \frac{V_o}{L_{22}} \tag{4.14}$$

$$i_{D1}(t_3) = 0 \tag{4.15}$$

$$i_{D2}(t_3) = n_2 i_2(t_1) - \frac{(\Delta t_2 + \Delta t_3) V_O}{L_{22}} = n_2 i_2(0) \tag{4.16}$$

$$\Delta t_2 = t_3 - t_2 = T_S - \Delta t_2 - \Delta t_1 \tag{4.17}$$

When the input goes up, Bi-flyback enters Boost mode.

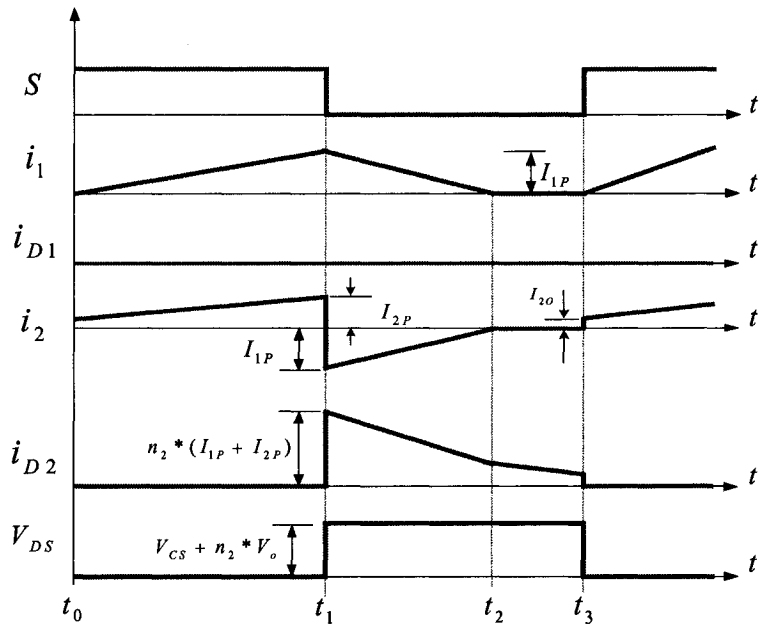
4.2.2 Boost Mode Operation

When rectified line voltage is higher than $V_{cs}+(n_2 - n_1)*V_o$, flyboost transformer T_1 works as boost inductor. During the switch on period, the current in flyboost transformer T_1 will increase linearly, then decrease and transfer all stored power to intermediate bus storage capacitors during the switch off period. The flyback converter cell will deliver required power to the load to minimize the output voltage ripple. The equivalent circuits and operational waveforms are shown in Fig. 4-5.

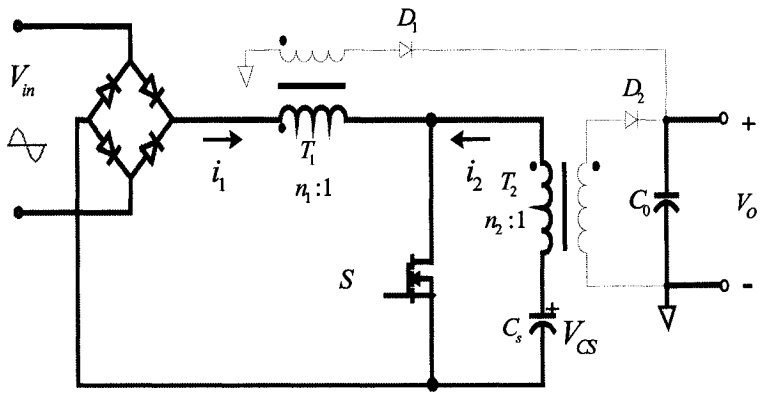
Similarly, we assume that PFC flyback will operate under DCM, and DC-DC flyback will operate under CCM. Each switching cycle can be divided into three operation intervals:

Interval 1 ($t_o \sim t_1$): during interval 1, the main switch is turned on at t_o, the line voltage is applied to PFC flyback transformer. The current in the primary winding of PFC flyback transformer, i_1 in Fig. 4-5, will increase linearly. And the voltage across

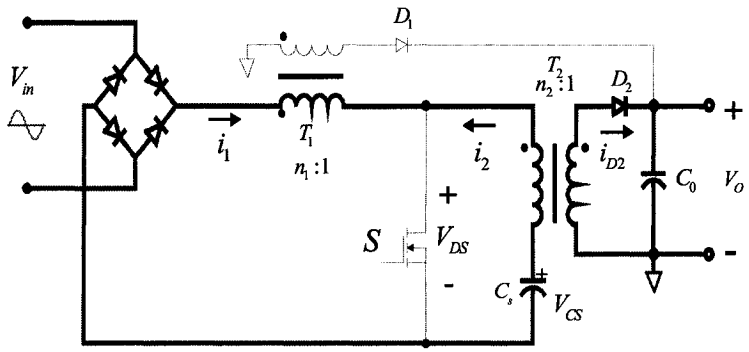
intermediate bus capacitor is applied to DC-DC flyback transformer T_2, which will cause the current i_2 in Fig. 4-5 to increase linearly also. The current equations are the same as in flyback mode, as listed in Eq. (4.1) – Eq. (4.7).



(a) Operation waveforms



(b) Equivalent circuit during ON period



(c) Equivalent circuit during OFF period

Fig. 4-5 Operation of boost mode

Interval 2 ($t_1 \sim t_2$): the main switch is turned off at t_1. The current in the PFC flyback (i_1) will decrease linearly and discharge energy to intermediate bus capacitor, since the voltage across T_1 will be less than n_1*V_1 in this path. Since PFC flyback transformer T_1 discharges through DC-DC transformer T_2 primary winding, the current in secondary winding of DC-DC flyback transformer T_2 (i_{D2}) consists of two parts: magnetizing current of T_2 and reflected current of T_1, i.e. $i_{D2} = n_2*i_1 + i_{22}$. And the magnetizing current of T_2, i_{22}, will decrease linearly since reflected output voltage is applied to T_2 secondary winding.

At t_2, all magnetizing energy in transformer T_1 is transferred to the intermediate capacitor and output, and i_1 reaches zero. The input rectifier bridge will prevent this current from going to negative. And the current in transformer T_2 (i_{D2}) will continue to decrease.

The voltage across T_2 primary winding is n_2V_o, so the voltage across S, V_{DS}, is equal to $V_{CS}+n_2V_o$. The voltage across transformer T_1 primary winding is $V_{CS}+n_2V_o-|V_{in}(t)|$.

$$\frac{di_1}{dt} = \frac{V_{cs} + n_2 \cdot V_o - |V_{in}|}{L_1} \tag{4.18}$$

$$\frac{di_{22}}{dt} = \frac{V_o}{L_{22}} \tag{4.19}$$

$$i_{D1}(t_2) = 0 \tag{4.20}$$

$$i_{D2}(t_2) = n_2 i_2(t_1) - \frac{\Delta t_2 V_O}{L_{22}} \tag{4.21}$$

$$\Delta t_2 = t_2 - t_1 = \frac{i_1(t_1) L_1}{V_{CS} + n_2 V_0 - |V_{in}|} \tag{4.22}$$

The discharge path of transformer T_1 includes the reflected output voltage by transformer T_2. Compared to typical boost topology, the effective discharging voltage over Bi-flyback topology is increased by this reflected voltage, so the required voltage across its intermediate capacitor C_{CS} to keep T_1 under DCM can be reduced by the value of n_2V_o.

Interval 3 ($t_2 \sim t_3$): At t_2, i_1 reaches zero and the input rectifier bridge prevents it from going negative. And i_{D2}, which only consists of magnetizing current of T_2 in this interval, continues to decrease until the switch is turned on at t_3. At $t=t_3=t_o+T_S$, the switching cycle repeats. The current equation is the same as in flyback mode, as listed in Eq. (4.13) – Eq. (4.17).

As illustrated in Fig. 4-3, these two operation modes will appear alternatively in one line voltage cycle. In actual circuit, the leakage inductance in two transformers will make the operation more complex, and there will be only one interval to discharge the energy in the leakage inductance.

4.3 Steady State Analyses

For practical design, the voltage stresses and current stresses are important for device selection and cost calculation. In this section, the steady state characteristics of Bi-flyback topology are studied to obtain some important parameters of Bi-flyback topology.

4.3.1 Mode Boundary

According to the discharging path of T_1, there are two different operation modes over one line period. Based on the operation analysis in last section, rectified input voltage is equal to $V_{CS}+(n_2-n_1)V_o$ at the boundary point of two modes.

In first quarter of line period, the boundary time for two modes is given by:

$$t_x = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{cs}+n_2V_o-n_1V_o}{V_p}\right) \tag{4.23}$$

Because,

$$v_{in}(t) = V_p \sin(\omega t) \tag{4.24}$$

Since the operation of this circuit is symmetrical over the line period, it is easy to obtain all of the mode boundary point for this topology, as shown in Fig. 4-3.

For actual circuit, the mode boundary is different from the above result, because the leakage inductance of PFC transformer T_1 will affect the transition from one mode to another, like other flyboost-derived topologies discussed in previous chapters.

4.3.2 Stead-State Equation for Intermediate Bus Voltage

The intermediate bus voltage is the most important parameter for single stage PFC circuit design, because it determines the voltage rating for most of power stage components, including MOSFET, intermediate capacitor, and output diode. In this section, the intermediate bus voltage in Bi-flyback topology is derived.

Since there are two different operational modes in this kind of topology with flyboost PFC cell, conventional analysis methods cannot be adopted directly. For large signal analysis, the circuit parameters can be determined through power flow analysis. For small signal analysis, the method discussed in previous chapter can be used.

In this section, power flow analysis method is applied to analyze the Bi-flyback topology to find out the equation for the intermediate bus voltage. Here only DCM+CCM operation is analyzed. Other combination operation modes, such as DCM+DCM and DCM+CCM/DCM can be found according to the same analysis method.

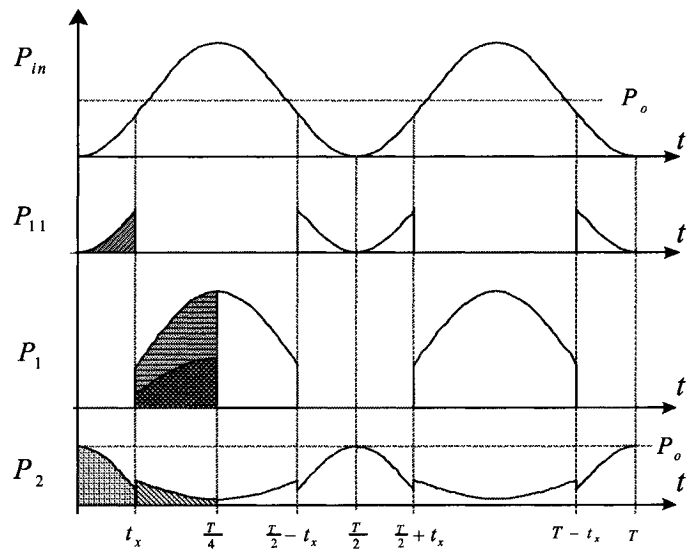
Since higher power factor is the goal of single-stage PFC scheme, the input current waveform of single-stage PFC converter should be very close to sinusoidal waveform. Here we assume that the input current is perfect sinusoidal waveform and synchronous with the input voltage. Then the input power waveform will be sinusoidal also, since,

$$P_{in}(t) = V_{in,peak} I_{in,peak} \sin^2(\omega t) = V_{in,peak} I_{in,peak} \left[0.5 - 0.5\cos(2\omega t)\right] \qquad (4.25)$$

According to analysis in last section, during flyback mode, all input power is transferred to the load; during boost mode, some input power is stored in intermediate bus capacitor and some is transferred to the load through T_2. Magnetizing power

delivered by T_2 is controlled to keep total transferred power from input and intermediate bus equal to output power, in order to keep tight output voltage regulation.

The power flow over one line cycle is shown in Fig. 4-6.



Direct transferred power by T1 Direct transferred power by T2

W_{cs1}: discharging W_{cs2}: discharging W_{cs3}: charging

P_{in}: Input power P_{11}: Power transferred by T_1 in flyback mode

P_2: Power delivered by T_2 P_1: Power transferred by T_1 in boost mode

Fig. 4-6 Power flow over a line period

Because the operation of the proposed topology is symmetrical, only operation in the first quarter of line period needs to be analyzed. In order to simplify the analysis, we assume that:

- All circuit components are ideal, so all parasitic parameters, such as leakage inductance, input / output capacitance of MOSFET, reverse recovery of diode, are neglected.
- Switching frequency is much higher than line frequency, and the input voltage can be assumed to be constant in one switching period;
- The intermediate bus capacitor is large enough to assume that its voltage is constant over one line cycle. In order to keep its voltage constant, the charging energy and discharging energy of intermediate bus capacitor in each line period should be balanced;
- Tight output voltage regulation to keep output voltage constant. So the charging energy and discharging energy of output capacitor in each switching period should be equal.

DC-DC conversion cell of the proposed topology in Fig. 4-2(a) is a typical flyback topology. When it operates in CCM, the duty cycle should be constant for the entire line period to achieve tight output regulation. According to flyback circuit formula, the duty cycle is given by:

$$D = \frac{n_2 V_o}{V_{cs} + n_2 V_o} \tag{4.26}$$

During the flyback mode ($0 \sim t_x$), in a given switching cycle, transformer T_1 is charged by rectified input voltage during switch ON period, and is completely discharged to the load during switch OFF period. According to the operation waveform in Fig. 4-4(a), the peak current through PFC transformer T_1 at t_1 can be given by:

$$I_{1P} = i_1(t_1) = \frac{DT_S}{L_1} V_{in,T_s} \tag{4.27}$$

where L_1 is the primary inductance of T_1, T_s is switching period, and v_{in,T_s} is the moving average value of the input voltage over each switching cycle.

Because there is not input current during switch OFF period, the average input current in one switching cycle is yielded as:

$$i_{1(avg)} = \frac{(t_1 - t_0)}{2T_s} I_{1P} = \frac{v_{in,T_s} D^2 T_s}{2L_1} \tag{4.28}$$

So when switch is turned off at t_1, the magnetizing energy stored in T_1 is equal to

$$W_1 = \frac{L_1 I_{1P}^{\ 2}}{2} = \frac{D^2 T_s^2}{2L_1} v_{in,T_s}^{\ 2} \tag{4.29}$$

The above magnetizing energy in T_1 is completely transferred to the load during switch OFF period. In order to keep tight output voltage regulation, i.e. V_o to be constant, the total power delivered respectively by T_1 and T_2 should be equal to output power in each switching cycle.

So the power delivered by T_2 in one switching cycle is:

$$P_2 = P_o - \frac{W_1}{T_s} = P_o - \frac{D^2 T_s}{2L_1} v_{in,T_s}^{\ 2} \tag{4.30}$$

Under flyback mode, all power delivered by T_2 is from intermediate bus capacitor. So the total discharging energy from intermediate bus capacitor during flyback mode ($0 \sim t_x$) is given by:

$$W_{cs1} = \sum_{t=0}^{t_x} P_2 T_s \tag{4.31}$$

where t_x is the boundary time between flyback mode and boost mode, with $v_{in}(t_x) = V_{CS}+(n_2 - n_1)V_o$.

Since switching frequency is much higher than line frequency, the summation Eq. (4.31) can be converted to integration equation over time. Combining with Eq. (4.30) and replacing v_{in,T_s} by $v_{in}(t)$, the above equation can be converted to:

$$W_{cs1} = \int_0^{t_x} P_2 dt = \int_0^{t_x} \left(P_o - \frac{D^2 T_s}{2L_1} v_{in}(t)^2 \right) dt \tag{4.32}$$

In the boost mode (t_x~T/4), both PFC and DC-DC transformers are charged during ON period, and T_1 is completely discharged through T_2 primary winding and intermediate bus capacitor, while T_2 will discharge some magnetizing energy to load during OFF period in each switching cycle.

According to Fig. 4-5, the discharging period (t_1~t_2) of transformer $T_1$is equal to:

$$t_2 - t_1 = \frac{I_{1P} L_1}{V_{cs} + n_2 V_o - v_{in,T_s}} \tag{4.33}$$

The operation of two modes during switch ON period ($t_0 \sim t_1$) is the same, so Eq. (4.27) is also effective in boost mode. Based on Eqs. (4.27) and (4.33), the average input current flowing through T_2 and intermediate bus capacitor in one switching cycle is yielded as:

$$i_{1(avg)} = \frac{(t_2 - t_1)}{2T_s} I_{1P} = \frac{D^2 T_s}{2L_1} \frac{v_{in,T_s}^{\ 2}}{V_{cs} + n_2 V_o - v_{in,T_s}} \tag{4.34}$$

So the average input power, P_{1a}, charged to intermediate bus capacitor in one switching cycle is given by:

$$P_{1a} = V_{cs} i_{1(avg)} = \frac{D^2 T_s}{2L_1} \frac{V_{cs} v_{in,T_s}^{\ 2}}{V_{cs} + n_2 V_o - v_{in,T_s}} \tag{4.35}$$

During boost mode ($t_x \sim T/4$), total charging energy from input to intermediate bus capacitor is given by:

$$W_{cs3} = \int_{t_x}^{\frac{T}{4}} P_{1a} dt = \int_{t_x}^{\frac{T}{4}} \frac{D^2 T_s}{2L_1} \frac{V_{cs} v_{in}(t)^2}{V_{cs} + n_2 V_o - v_{in}(t)} dt \tag{4.36}$$

And the average input power, P_{1b}, directly transferred to load by T_2 during S OFF period in one switching cycle is:

$$P_{1b} = n_2 V_o i_{1(avg)} = \frac{D^2 T_s}{2L_1} \frac{n_2 V_o v_{in,T_s}^{\ 2}}{V_{cs} + n_2 V_o - v_{in,T_s}} \tag{4.37}$$

Since the sum of P_{1b} and delivered magnetizing power of T_2 should be equal to output power, the transferred magnetizing power of T_2 during S OFF period is equal to:

$$P_{2b} = P_o - P_{1b} = P_o - \frac{D^2 T_s}{2L_1} \frac{n_2 V_o v_{in,T_s}^{\ 2}}{V_{cs} + n_2 V_o - v_{in,T_s}} \tag{4.38}$$

In the boost mode, all transferred magnetizing energy in T_2 is the discharging energy from intermediate bus capacitor. So the total discharging energy from intermediate bus capacitor during boost mode ($t_x \sim T/4$) is given by:

$$W_{cs2} = \int_{t_x}^{\frac{T}{4}} P_{2b} dt = \int_{t_x}^{\frac{T}{4}} \left(P_o - \frac{D^2 T_s}{2L_1} \frac{n_2 V_o v_{in}(t)^2}{V_{cs} + n_2 V_o - v_{in}(t)} \right) dt \tag{4.39}$$

In steady state, the voltage across intermediate bus capacitor is constant, so its charging and discharging energy should be balanced in each line period, i.e.

$$W_{CS1} + W_{CS2} = W_{CS3} \tag{4.40}$$

Combining Eqs. (4.24), (4.26), (4.32), (4.36) and (4.39), yields the equation of intermediate bus voltage given by:

$$\frac{T_s n_2^2 V_p^2 V_o^2}{L_1(V_{cs}+n_2V_o)}\int_{t_x}^{\frac{T}{4}}\frac{\sin(\omega t)^2}{V_{cs}+n_2V_o-V_p\sin(\omega t)}dt=\frac{P_oT}{2}-\frac{T_s n_2^2 V_p^2 V_o^2}{L_1(V_{cs}+n_2V_o)^2}\left(\frac{t_x}{2}-\frac{\sin(2\omega t_x)}{4\omega}\right)$$

(4.41)

The above equation is only applicable with the condition that DC-DC flyback cell operates in CCM during entire line period. When load is very light or inductance of T2 primary winding is low, DC-DC flyback cell may enter DCM.

In DCM, the duty cycle will keep changing according to input instantaneous voltage in order to achieve tight output voltage regulation. Since the power processed by DC-DC flyback conversion cell under DCM can be easily calculated, the equation can be obtained through the following steps:

a) Calculate the power directly transferred to load by PFC cell in one switching cycle;

b) Calculate the power transferred to load by DC-DC flyback cell in one switching cycle;

c) The sum of power obtained in steps a) and b) should be equal to output power for each switching cycle. So duty cycle can be derived from this relationship;

d) Calculate the charging and discharging energy of intermediate capacitor in one line period, using the same method as in the above CCM analysis;

e) The charging and discharging energy should be balanced for each line period. And the final equation for the intermediate bus voltage is achieved.

We just gave the final equation for both PFC cell and DC-DC conversion cell under DCM operation as follow:

$$\int_0^{t_x} \frac{L_1 V_{CS}}{L_1 V_{CS}^{\ 2} + L_2 V_P^{\ 2} \sin(\omega t)^2} dt = \int_{t_x}^{\frac{T}{4}} \frac{L_2 V_P^{\ 2} \sin(\omega t)^2 - L_1 V_{CS}\left(V_{CS} + n_2 V_o - V_p \sin(\omega t)\right)}{n_2 L_2 V_o V_P^{\ 2} \sin(\omega t)^2 + L_1 V_{CS}^{\ 2}\left(V_{CS} + n_2 V_o - V_p \sin(\omega t)\right)} dt \tag{4.42}$$

There is another popular operation condition: in which the DC-DC conversion cell operates in CCM for some time and in DCM for the rest of one line period. In most cases, the DC-DC flyback transformer enters DCM during flyback mode. The following descriptions will focus on this operation condition.

Because of small PFC inductance, the input current is increasing very fast when input voltage is high. This causes the direct transferred power to be very high. The required power from DC-DC cell is so low that DC-DC conversion cell will enter DCM. So there will be two operation modes for DC-DC conversion cell in one line cycle as shown in Fig. 4-7. When the DC-DC delivered power is higher than critical power Pc, DC-DC cell runs under CCM, otherwise it will be under DCM.

In order to use the power flow analysis method, the boundary point between CCM and DCM need to be determined. The calculation method is to find the point when the duty calculated from DCM mode equation is equal to the duty result from CCM mode equation. We can find out this point (t_y) using the above equation. Here is the final result:

$$t_y = \frac{1}{\omega} \sin^{-1}\left(\sqrt{\frac{2L_1 L_2 P_O \left(V_{cs} + n_2 V_o\right)^2 - \left(n_2 V_o V_{CS}\right)^2 T_S L_1}{\left(n_2 V_o V_P\right)^2 T_S L_2}} \right) \tag{4.43}$$

The boundary point (t_x) for flyback mode and boost mode is the same as before:

$$t_x = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{cs} + n_2 V_o - n_1 V_o}{V_p}\right) \tag{4.44}$$

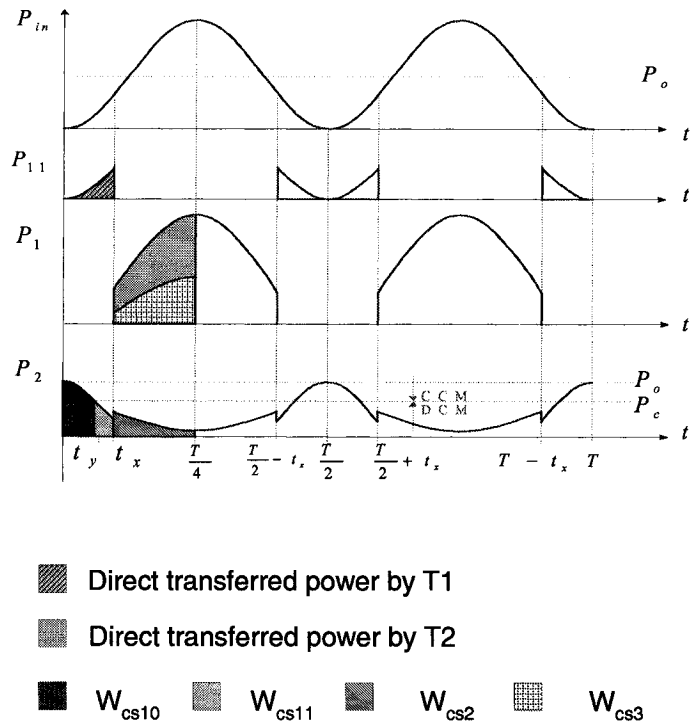


Fig. 4-7 Power flow over a line period

Then we can calculate the power flow during period 0~t_y using CCM method, and using DCM method from t_y to t_x. Under whole boost mode, the circuit will operate under DCM. The final equation for intermediate bus voltage is given by:

$$\int_{t_x}^{\frac{T}{4}} \frac{P_O L_2 V_P^2 \sin(\omega t)^2 - P_O L_1 V_{CS}\left(V_{CS} + n_2 V_o - V_p \sin(\omega t)\right)}{n_2 L_2 V_o V_P^2 \sin(\omega t)^2 + L_1 V_{CS}^2\left(V_{CS} + n_2 V_o - V_p \sin(\omega t)\right)} dt =$$

$$P_O t_y + \int_{t_y}^{t_x} \frac{L_1 V_{CS} P_O}{L_1 V_{CS}^2 + L_2 V_P^2 \sin(\omega t)^2} dt - \frac{V_P^2 T_S}{2L_2}\left(\frac{t_y}{2} - \frac{\sin(2\omega t_y)}{4\omega}\right)\left(\frac{n_2 V_O}{V_{CS} + n_2 V_O}\right)^2 \tag{4.45}$$

Those equations show the relationship between intermediate bus voltage and other circuit parameters. It is a transcendental equation that can be solved by mathematical software, such as MathCAD©.

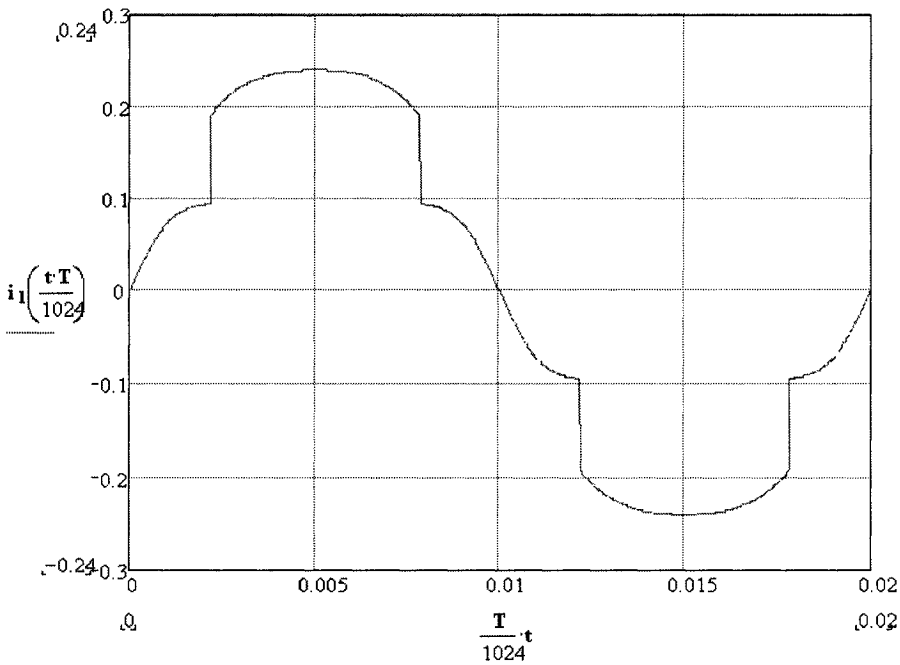
Under flyback mode, the input current is the average T_1 primary winding current that occurs only during interval $1(t_0 \sim t_1)$. This is given by:

$$i_{1(avg,flyback)} = \frac{(t_1 - t_0)}{2T_s} I_{1P} = \frac{v_{in,T_s} D^2 T_s}{2L_1} \tag{4.46}$$

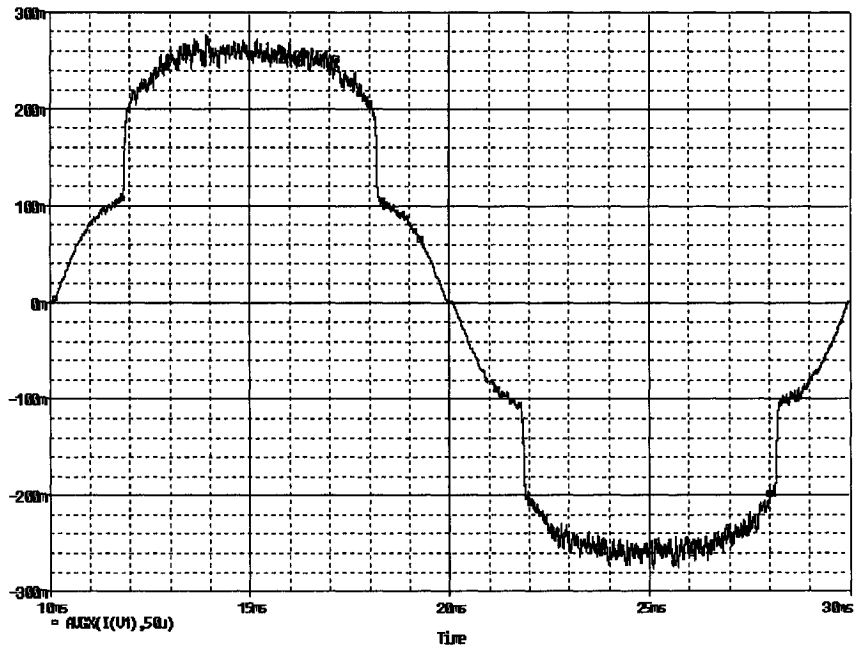
Under Boost mode, the input current is also the average T_1 primary winding current that occurs during interval 1 $(t_0 \sim t_1)$ and interval 2 $(t_1 \sim t_2)$, and it is given by:

$$i_{1(avg,boost)} = \frac{(t_2 - t_0)}{2T_s} I_{1P} = \frac{D^2 T_s}{2L_1} \frac{v_{in,T_s}^{\ 2}}{V_{cs} + n_2 V_o - v_{in,T_s}} + \frac{v_{in,T_s} D^2 T_s}{2L_1} \tag{4.47}$$

Figure 4-8 shows the input current waveforms obtained from OrCAD© Pspice simulation and MathCAD calculation. These results match each other very well, which verify the analysis method.



(a) MathCAD calculation result



(b) OrCAD Pspice simulation result

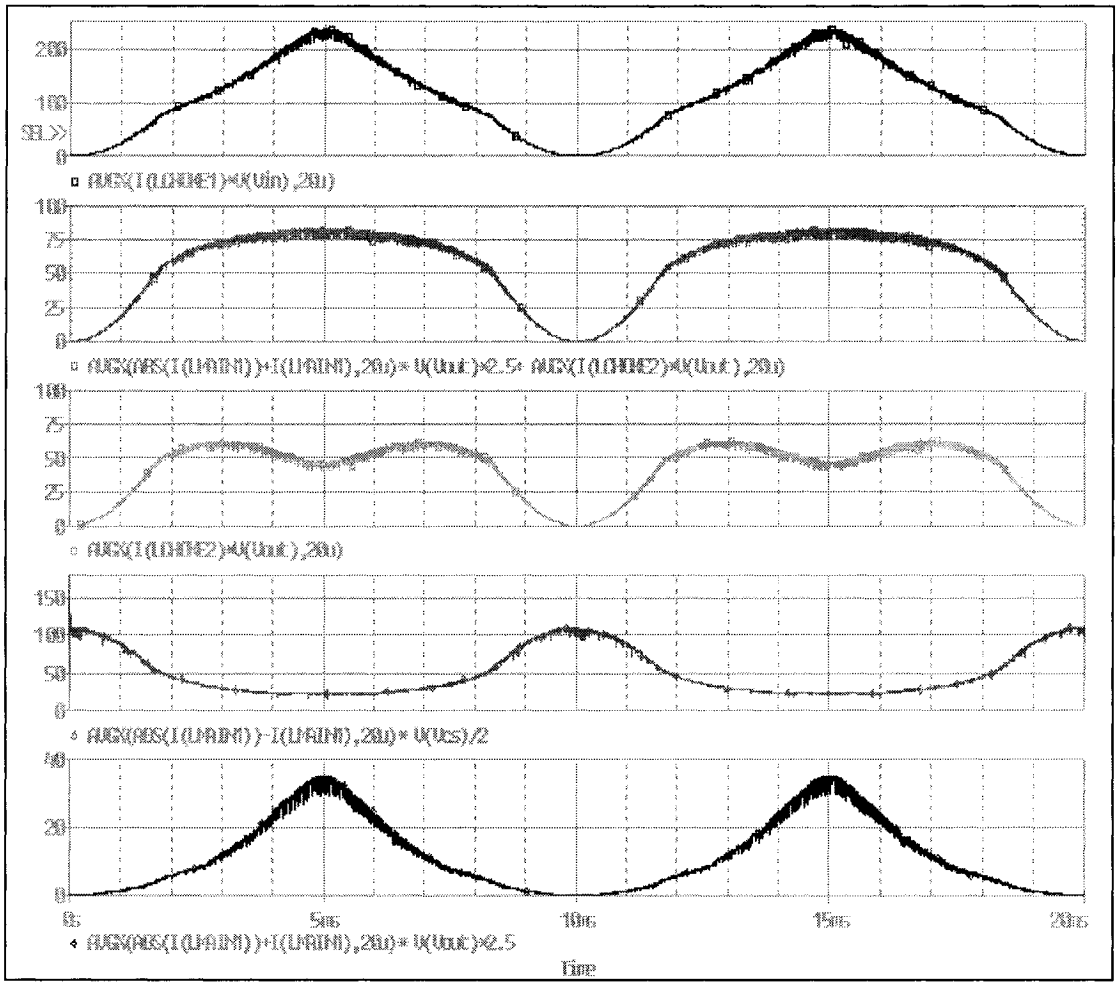
Fig. 4-8 Input current waveform obtained by MathCAD and Pspice

Due to its complex operation mode, the power flow analysis equation is also very complex, and it is time-consuming to build the solution software. Other simulation methods can be used to analyze this topology. For instance, the features of this topology can be easily illustrated by OrCAD Pspice, and all parasitic parameters, such as leakage inductance can be easily considered. But it is still difficult to build the simulation circuit and perform the simulation. There are two clocks in PFC circuit: line period, and switching period. In order to get steady state results, the total simulation time should be at least several line cycle (several hundred ms) long, while the required simulation step should be shorter than switching period (several microsecond). Therefore simulation also requires lots of time.

Figure 4-9 shows the simulation results referring to the power flow mount from each power path. In this simulation, the leakage inductance of both transformers is taken into consideration, so there is always some direct power transferred by DC-DC transformer T_2. Since the input current is not ideal sinusoidal waveform, the total power is also not sinusoidal waveform.

According to simulation results, over 50% of output power is directly transferred from input end, which means that the power processed by MOSFET is much less than other single-stage PFC scheme.

The sum of the power delivered by intermediate bus (trace D in Fig. 4-9) and the direct transferred power (trace B in Fig. 4-9) is constant and equal to the load power at any time in one line cycle. This verifies that our above assumptions are correct.



Traces from top to bottom:

a. Input power

b. Total direct transferred input power (52%)

c. Direct input power transferred by T_1 (41%)

d. Power transferred by T_2 (48%)

e. Direct input power transferred by T_2 (11%)

Fig. 4-9 Power flow analysis result by OrCAD Pspice

4.3.3 Condition for PFC cell in DCM

In order to achieve high power factor, PFC cell should always operate under DCM. The maximum charging voltage and the minimum discharging voltage across transformer T_1, and the maximum power processed by PFC cell all happen at T/4, when $V_{in}(T/4)=V_P$. Therefor PFC cell will operate in DCM for the entire line period if it operates in DCM at T/4.

In order to keep PFC cell in DCM, the current i_1 in Fig. 4-5(a) in transformer T_1 should reach zero before a new switching cycle begins, which means that:

$$t_2 - t_1 \le t_3 - t_1 \tag{4.49}$$

while:

$$t_3 - t_1 = (1-D)T_s \tag{4.50}$$

Combining Eqs. (4.26), (4.33), (4.49) and (4.50), we obtain the following condition for PFC cell in DCM:

$$V_{CS} \ge V_P \tag{4.51}$$

where V_p is the peak value of input voltage.

So the intermediate bus voltage should always be higher than the peak value of input voltage in order to keep PFC cell in DCM. For universal voltage application, the bus voltage can be controlled to be just a little higher than the peak of input voltage (about 400V). So 450VDC capacitor can be used in this topology.

4.3.4 Features of Bi-flyback topology

By adding another voltage source in discharging path to PFC inductor, the proposed topology benefits from following features:

a) *The maximum intermediate bus voltage is limited.* Only at boost mode when input voltage is higher than $V_{CS}+n_2V_o-n_1V_o$, intermediate bus capacitor C_s is charged by input power. Under flyback mode, the capacitor is not discharged by DC-DC cell. The higher intermediate bus voltage, the less charging power. So the maximum intermediate bus voltage will be limited to $V_{in,peak} + n_1V_o - n_2V_o$. By carefully selecting transformer turn ratio n_1 and n_2, the maximum intermediate bus voltage can be set to a little higher than the peak value of input voltage to achieve low voltage stresses and high power factor. For universal voltage ($85\sim265V_{AC,RMS}$) applications, the maximum intermediate bus voltage can be controlled to less than 400VDC, allowing single commercial 450VDC capacitor to be used in this topology. Since the maximum intermediate bus voltage is limited, DC-DC conversion cell can operate in CCM for low current stresses, without high voltage problem at light load, as those that exist in the conventional single-stage PFC converter.

b) *Part of the load power is processed by the main switch only once.* In the flyback mode, all input power is directly transferred to load by T_1. In the boost mode, some input power is directly transferred to the load by T_2, and some input power is stored in intermediate bus capacitor and then delivered to the load by DC-DC cell. So the total power processed by active switch is less than that in conventional single-stage PFC converter. This will lower current stresses on power components and improve efficiency.

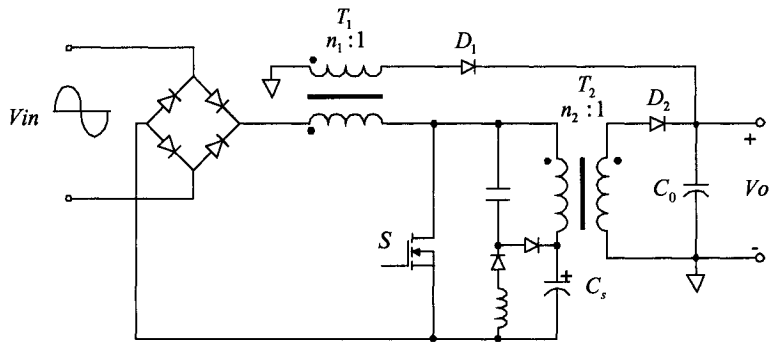
4.4 Experimental results

There are some practical issues existing in Bi-flyback prototype. One of those issues is that the leakage inductance of both transformers will cause very high voltage spike when the power switch is turned off. This is a typical issue in DC-DC flyback topology. In order to eliminate this voltage spike, snubber circuit is necessary for the practical prototype. Conventional RCD snubber circuit used popular in flyback topology can be used in Bi-flyback converter. But the power losses on the snubber circuit in Bi-flyback may be a little higher than in the simple flyback topology, and snubber capacitance needs to be a little bigger, because there are two flyback transformers.

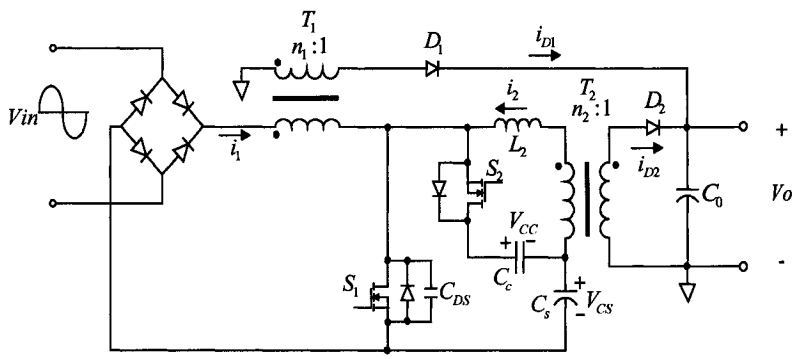
In order to reduce the snubber power losses, figure 4-10 shows two low loss snubber solutions. In Fig. 4-10(a), low loss snubber circuit is adopted. The energy in snubber capacitor will be recycled back to the main circuit. So there should be no power loss if MOSFET and diode are ideal and there is no conductive resistance. But in practical applications, snubber circuit will cause high current pulse on MOSFET when MOSFET is turned ON. This high current pulse causes extra power losses on the MOSFET that compensate the recycled snubber power, resulting in the almost same efficiency as RCD snubber. And the parameter design also does not easily meet wide voltage applications.

Figure 4-10(b) illustrates the solution with one active clamp circuit as snubber circuit. By adding one more active switch, the snubber energy can be implemented to

carry out zero voltage switching on the main switching. The performance and efficiency of this solution is better than other solution. The issues in this solution are the cost and the complicated circuit. Since the additional MOSFET is ground floating, the driver circuit is a challenge or costly.



(a) With low loss snubber circuit



(b) With active clamp circuit

Fig. 4-10 Bi-flyback PFC converter with snubber circuit

One 150W/28VDC universal input single stage PFC converter prototype based on Fig. 4-10(b) was built to verify the operation of the proposed Bi-flyback topology.

The main design specifications are:

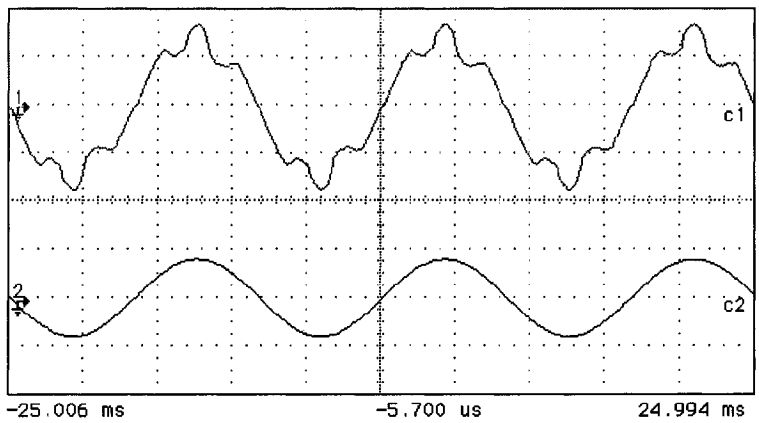
- Input: 85~265$V_{AC,RMS}$
- Output: 28VDC @ 150W
- Switching frequency: 200kHz
- T_1: primary inductance L_1 = 30uH, turn ratio n_1 = 4
- T_2: primary inductance L_2 = 375uH, turn ratio n_2 = 3.8

The main components include:

- MOSFET S1: IXFH20N60 (600V, 20A)
- MOSFET S2: IRFBC30 (600V 5A)
- PFC cell series fast recovery diode: DSEI 8-06 (600V, 8A)
- Secondary Schottky diode D_1&D_2: 30CPQ150 (150V, 15A x 2)
- Storage capacitor C_S: 150uF / 450V
- Clamp capacitor C_C: 0.1uF / 200V
- Controller IC: UC3842 with some logic gate for additional switch timing

Figure 4-11 shows experimental waveforms of input current and voltage at 100W output and 110$V_{AC,RMS}$ input. The input current waveform is not perfect sinusoidal waveform because of the two operation modes and direct power transfer feature. But the power factor is still above 0.98, high enough to meet the standard requirement.

Figure 4-12 and Table 1 shows the variation of intermediate bus voltage versus output power at different input voltage conditions. The maximum voltage across intermediate capacitor is about 390VDC for universal input voltage and all load condition. Therefore one 450V capacitor can be used in this topology.



Top: current (1A/div) Bottom: voltage (200V/div)

Fig. 4-11. Input current and input voltage at 100W output and 110V input

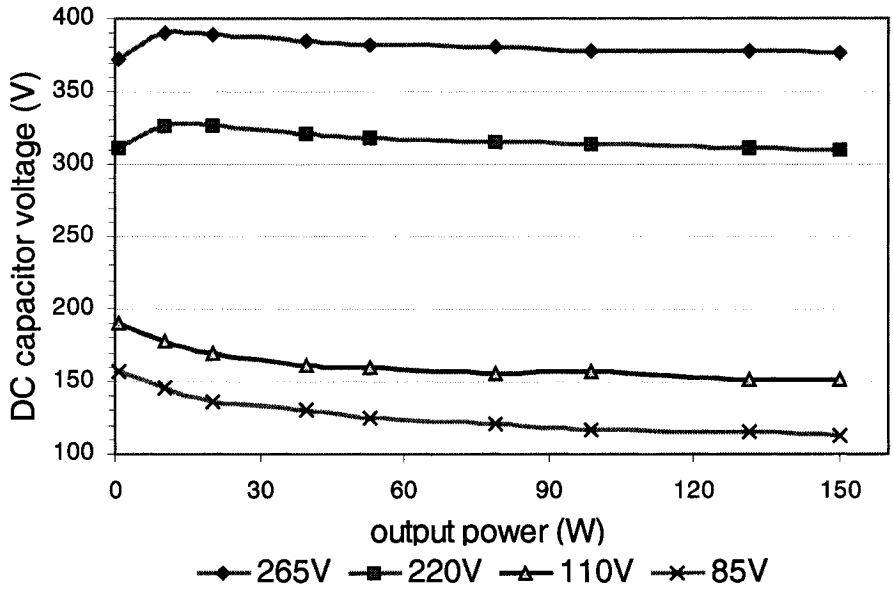


Fig. 4-12. Measured intermediate bus voltage versus output power

Figures 4-13 and 4-14 show the measured power factor and efficiency versus input voltage at 150W load. The measured power factor is 0.974 with 83.2% efficiency at 110V input and 150W load.

Detailed tested data are given in Tables 4.1 & 4.2.

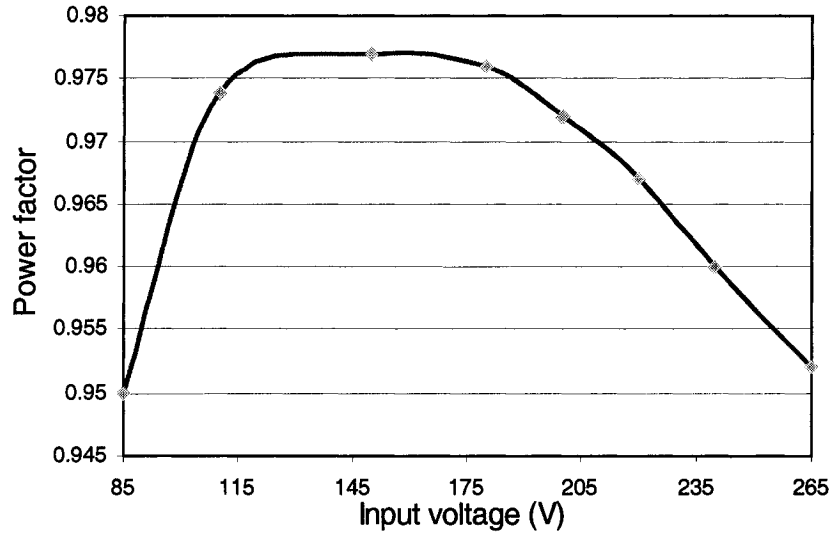


Fig. 4-13. Measured power factor at 150W load

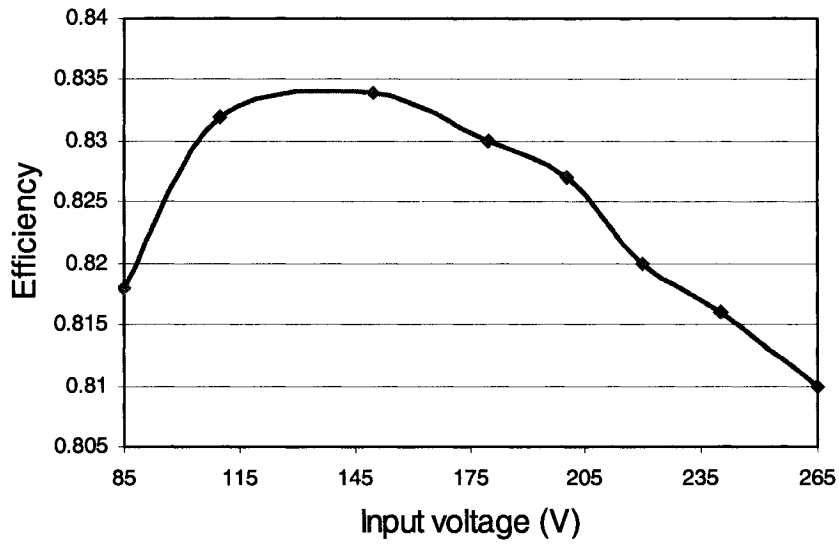


Fig. 4-14. Measured efficiency at 150W load

Table 4.1 Measured bus voltage (Volts) at different operation condition

Po	Vcs (265Vin)	Vcs (220Vin)	Vcs (110Vin)	Vcs (85Vin)
150w	375.7	310.2	151.7	112.9
132w	378.1	311.5	151.8	115.1
100w	378.1	314.5	156.4	116.6
80w	381.0	315.9	156.2	121.3
50w	382.2	318.7	159.9	124.6
40w	385.0	320.6	161.8	130.8
20w	389.0	326.3	169.8	136.8
10w	390.7	326.9	178.4	145.5
1w	372.5	310.5	190.2	157.5

Table 4.2 Experimental results of Bi-flyback topology

Vin	Power factor (150W)	Power factor (100W)	Efficiency (150W)	Efficiency (100W)
85	0.950	0.987	0.818	0.836
110	0.974	0.980	0.832	0.839
150	0.977	0.962	0.834	0.836
180	0.976	0.950	0.830	0.827
200	0.972	0.941	0.827	0.820
220	0.967	0.938	0.820	0.813
240	0.960	0.928	0.816	0.804
265	0.952	0.915	0.810	0.795

4.5 Summary

In this chapter, one very simple single stage PFC topology was proposed. By integrating two simple flyback circuits together, Bi-flyback single stage PFC converter can achieve good power factor with intermediate bus voltage only little higher than input voltage peak value. This feature makes it very attractive for low power low cost universal voltage applications. The operation of this scheme was discussed in detail. And power flow approach was implemented to perform steady state analysis. Detailed test results were included to show its good performance.

CHAPTER 5

CONTROL APPROACHES FOR BI-FLYBACK CONVERTER

5.1 Introduction

For typical single stage PFC scheme, there is only one active switch and one control loop. This main goal of the controller is to achieve tight output voltage regulation. Normally there is still a separate or "independent" DC-DC cell in typical single stage PFC scheme, and its operation is almost independent to the combined PFC cell as discussed in chapter 1. So the controller can be the same as the corresponding DC-DC converter. When the intermediate bus voltage is constant, the duty cycle of single stage PFC scheme will be constant for constant output voltage under steady state. When PFC cell operates under DCM with constant duty cycle, the average input current over switching period will be very close to ideal sinusoidal waveform if the intermediate bus voltage is higher enough. This is the foundation of the operation of typical single stage PFC scheme.

So there are not special requirement on typical single stage PFC scheme. The control scheme in DC-DC converter can be implemented in corresponding single stage PFC converter without change.

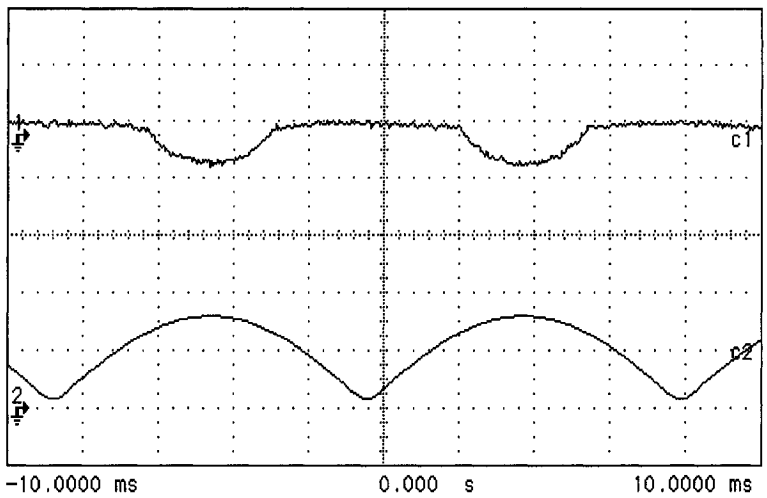
For single stage PFC with direct power transfer or parallel power transfer, the operation is a little different to typical single stage PFC scheme, because some input power is transferred to output directly. So the actual delivered power by DC-DC cell will not be the same as load power. Even for constant load current, the power delivered by DC-DC cell may keep changing in one line cycle, as discussed in previous chapter. So the duty cycle need to keep changing to achieve tight output voltage.

Figure 5-1 shows the measured waveforms from Bi-flyback converter with conventional voltage control mode. The error amplifier output signal will be compared with sawtooth waveform in the controller to achieve the proper PWM signal. This waveform also illustrates the actual duty value.

When rectified input voltage is low, the direct transferred power is low, resulting that DC-DC flyback cell operates under CCM. So the duty cycle will be constant when the intermediate bus voltage and output voltage is constant (almost). It results in constant output signal from error amplifier.

When input voltage goes higher, more input power is direct transferred to the output end. And the direct transferred power keeps changing based on instantaneous input voltage. The DC-DC flyback circuit will enter DCM and the actual delivered power will keep changing also. So the output signal from error amplifier will keep changing to adjust the duty cycle in order to achieve constant output voltage (constant power). In Fig. 5-1, the error amplifier output signal is changing in the opposite direction of input voltage, during the high value period of input voltage.

The measured input current waveform and power factor is very good when conventional voltage mode controller is adopted for Bi-flyback PFC scheme.



Upper waveform: error amplifier output signal

Bottom waveform: rectified input voltage

Fig. 5-1 duty cycle waveform for voltage mode control

Actually, peak current mode control method is more popular in low power DC-DC application, because it provides fast transient response and automatically over-current protection. Normally the current signal is obtained by adding one resistor in series with the main switch. By comparing the switch peak current with the error signal from error amplifier, the controller will achieve constant duty cycle and constant peak current under steady state condition for conventional DC-DC converter.

In single stage PFC converter, there is only one main switch for both DC-DC and PFC cell. So the current through the switch is the sum of DC-DC circuit and PFC circuit. For steady state condition, the DC-DC peak current through the only switch should be constant, while the peak current of PFC circuit varies to follow the changing instantaneous input voltage. If the peak switch current is controlled to be constant, the

DC-DC circuit will not be able to achieve constant output voltage. So it seems that it is trouble to apply peak current control to single stage PFC converter.

But we found it is possible to implement current mode control approach to single stage PFC converter, if the bandwidth of the controller is high enough to let the duty cycle follow the instantaneous input voltage change. Because the input voltage frequency is only 50Hz or 60Hz, it is easy to meet the requirement by designing the bandwidth of controller to several kHz.

During practical experiments, both voltage mode and current mode control methods were tested respectively on Bi-flyback topology. The tested results, including input current waveform and power factor, are very similar to each other. So current mode can be implemented in single stage PFC application. Since the inductor current is controlled directly by current mode controller, it will ease the compensation circuit and protection design. So it prefers to use current mode in Bi-flyback topology.

Flyback is the most popular topology for low cost application due to its low component counts. Normally current mode control is implemented in flyback topology. Recently, valley switching technique was introduced to achieve better performance from this simple topology. By discharging the MOSFET capacitor through transformer magnetizing inductance before the MOSFET is turned on, valley switching technique can significantly reduce the turn-on switching losses. It results in better efficiency.

Technically, all single-stage PFC converters, which use flyback topology as its DC-DC stage, can use valley switching technique to achieve improved efficiency. This technique was applied to a single-stage PFC topology with higher efficiency in [????].

But the power factor and Total Harmonic Distortion (THD) of that topology is not very good due to its topology configuration.

Here, valley switching technique is applied to the Bi-flyback topology for better performance. Detailed operation principle descriptions and simulation results are included to verify this approach.

5.2 valley switching control approach

If flyback topology operates under DCM, there will be one period that both primary MOSFET and secondary diode are OFF, after the magnetizing current in flyback transformer becomes zero. During this period, the magnetizing inductance of flyback transformer primary winding will resonate with the MOSFET output capacitor. This resonance results in the voltage across the MOSFET oscillating around the bus voltage. Valley switching technique will turn on the MOSFET at the valley point of the oscillating voltage, so the turn-on switching losses of MOSFET can be reduced.

If the MOSFET is turned on at the first valley point, which means that MOSFET is turned on shortly (quarter of the free resonant period) after the magnetizing current decreases to zero, flyback converter will operate almost at the boundary of Continuous and Discontinuous Conduction Mode (CCM / DCM). According to input voltage and output power value, the switching frequency will vary to keep valley switching condition. Control IC with this technique is available in today's market with low cost, which makes it very suitable for low power and low cost applications.

Bi-flyback topology is redrew in Fig. 5-2(a), in which the output capacitor of MOSFET is shown as C_{ds}. The operation of Bi-flyback topology under valley switching control method is the same as that under conventional PWM control, except for the turn-on time of each switching cycle.

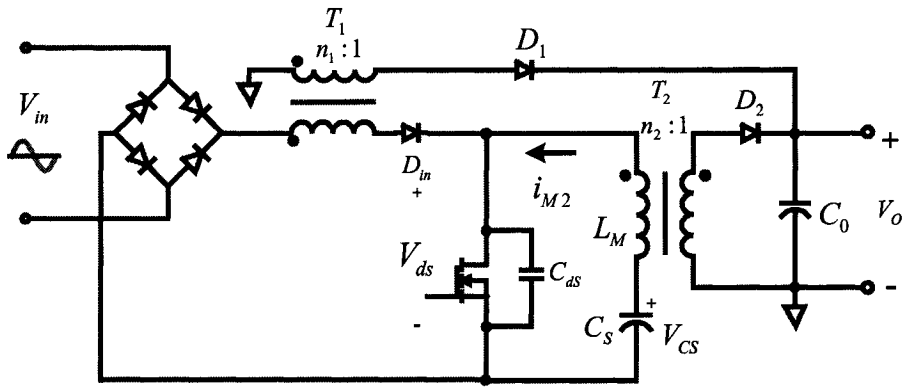
In order to simplify the analysis, we assume that input rectifier and secondary diode are ideal components without parasitic parameters. And the intermediate bus capacitor is large enough to keep its voltage constant. Even though there are two flyback circuits and two operation modes in this topology, the turn-on time depends on the DC-DC flyback. Following is the description about the operation when Bi-flyback topology operates under boost mode. The flyback mode operation is similar.

Following is the description about the operation in one switching cycle.

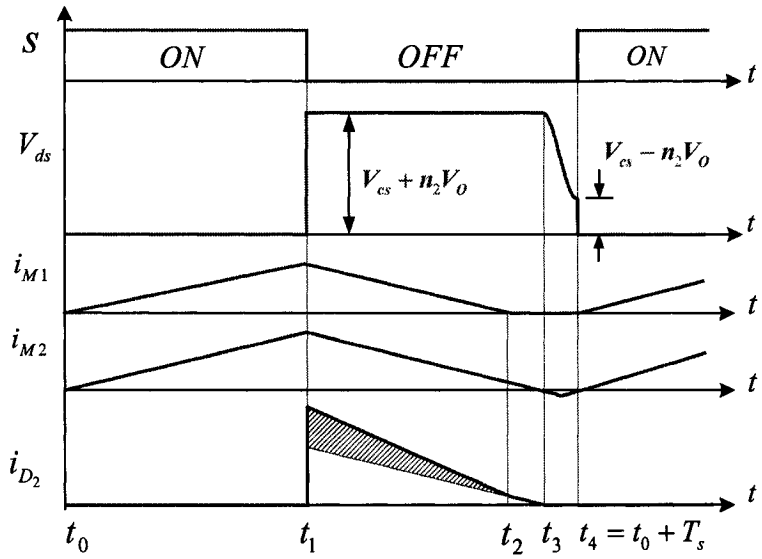
Interval 1 ($t_0 \sim t_1$): the main switch is turned on at t_0, the line voltage is applied to PFC flyback transformer. The current in the primary winding of PFC flyback transformer, i_{M1} in Fig. 5-2, will increase linearly. And the voltage across intermediate bus capacitor is applied to DC-DC flyback transformer T_2, which will cause the current i_{M2} in Fig. 5-2 to linearly increase also.

Interval 2 ($t_1 \sim t_2$): the main switch is turned off at t_1, both magnetizing currents begin to decrease and transformers are discharging. At t_2, the magnetizing current i_{M1} in T_1 decreases to zero, and input rectifier bridge will keep it at zero. The output capacitor voltage of MOSFET S will be charged to $V_{CS}+n_2V_o$ (n_2: turn ratio of T_2, V_o: output voltage) at t_1 and stays at this voltage during this interval.

Interval 3 ($t_2 \sim t_3$): The magnetizing current i_{M2} in T_2 continues to decreases until it reaches zero at t_3. The voltage across the output capacitor of MOSFET S stays at $V_{CS}+n_2V_o$ during this interval.



(a) Topology



(b) Operational waveforms

Fig. 5.2 Bi-flyback single-stage PFC converter

Interval 4 ($t_3 \sim t_4$): Once the magnetizing current of T_2 reaches zero, the secondary diode D_2 will turn off, and secondary circuit will not work until next switching cycle. During this interval, the output capacitor of MOSFET and transformer T_2 magnetizing inductor will form a free resonant circuit as shown in Fig 5-3, since we assume that the intermediate bus voltage is constant. Because the voltage across MOSFET capacitor ($V_{dS} = V_{CS}+n_2V_o$) is higher than intermediate bus voltage (V_{CS}), it will cause the transformer current to increase in the opposite direction.

$$\frac{di_{M2}}{dt} = \frac{V_{cs} - V_{ds}}{L_M} \tag{5.1}$$

$$\frac{dV_{ds}}{dt} = i_{M2} \tag{5.2}$$

If we turn on the MOSFET when its voltage reach the first valley point as shown in Fig. 5-2(b), this interval will last for one quarter of the free resonance period:

$$\Delta t = t_4 - t_3 = \frac{T}{4} = \frac{\pi\sqrt{L_M C_{ds}}}{2} \tag{5.3}$$

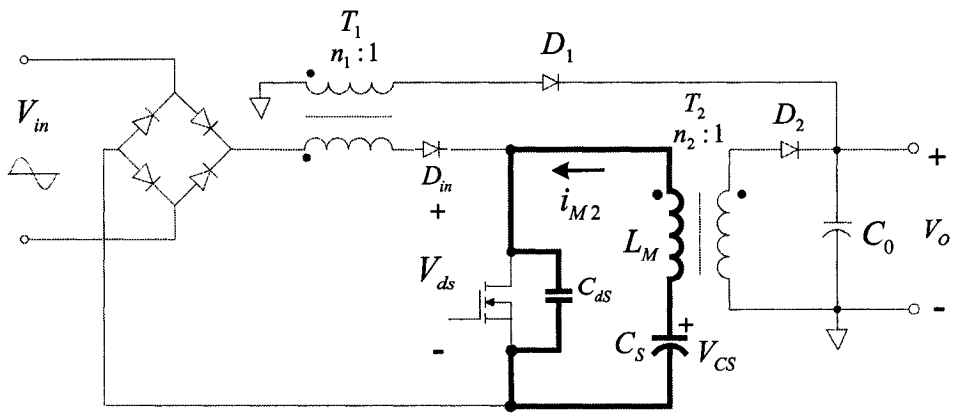


Fig. 5-3 Equivalent circuit during free resonant interval

Assume that all components are ideal without power loss, the voltage across MOSFET will oscillate between the peak value $V_{cs}+n_2V_o$ and the valley value $V_{cs}-n_2V_o$. If the MOSFET is turned on at the valley voltage point with the voltage equal to $V_{cs}-n_2V_o$, the turn-on switching losses associated with MOSFET capacitor will be reduced.

When MOSFET is turned ON, all energy in its output capacitor C_{ds} will be dissipated in MOSFET. This kind of power loss is referred as turn-on switching loss, which can be described as:

$$P_{turn-on} = \frac{F_{sw} C_{ds} V_{ds}^{\ 2}}{2} \tag{5.4}$$

where F_{sw} is the switching frequency of the converter.

For conventional CCM flyback operation, MOSFET will turn on when its voltage is equal to $V_{cs}+n_2V_o$, the turn-on switching power loss is:

$$P_{turn-on,1} = \frac{F_{sw} C_{ds} \left(V_{cs} + n_2 V_O\right)^2}{2} \tag{5.5}$$

When valley switching technique is implemented and the MOSFET is turned on with its voltage equal to $V_{cs}-n_2V_o$, the turn-on switching power loss is given by:

$$P_{turn-on,2} = \frac{F_{sw} C_{ds} \left(V_{cs} - n_2 V_O\right)^2}{2} \tag{5.6}$$

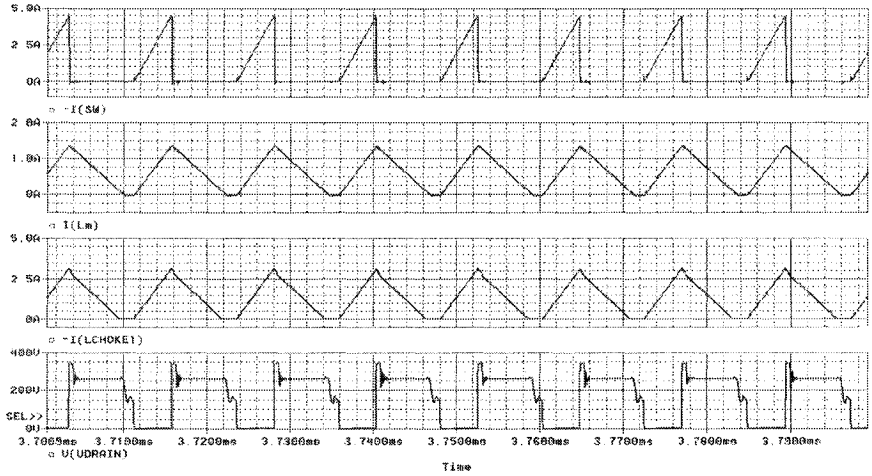
Comparing the Eqs. (5.5) and (5.6), we can find that the switching power losses can be reduced in valley switching approach. For some applications, the turn-on switching losses can totally be eliminated like Zero-Voltage-Switching (ZVS) technique, if n_2V_o is equal to or higher than V_{cs}.

The magnetizing current i_{M2} of T_2 is almost at the boundary of continuous and discontinuous condition, which means that T_2 operates at critical conduction mode as

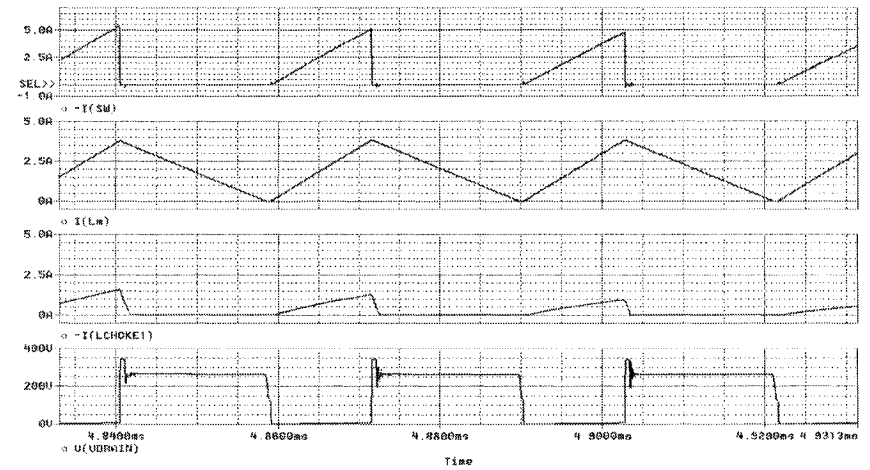
discussed above. This operation mode brings several advantages: easy compensation circuit design since it is DCM; lower RMS current stresses since it is almost CCM comparing to other DCM operation.

Simulation results are shown in Figs. 5-4 and 5-5 for a 90W@20VDC output universal input application. Figures 5-4 (a) and (b) show the key operational waveforms when input voltage is close to its peak and zero value respectively. It is clear illustrated that the switch is turned on at the valley point of its voltage. Transformer T_2 magnetizing current is at boundary condition. When input voltage is close to its peak value, the input current is close to critical conduction mode also, as shown in Fig. 5-4 (a).

Figure 5-5(a) shows the operational waveforms with valley switching technique over half line cycle, while Fig. 5-5(b) shows the waveform for fixed frequency PWM control method for comparison purpose. The input current waveforms under both control approaches are almost the same, resulting in the same high power factor and low THD. But the switch current waveforms are different, which will affect the conduction losses and turn-off switching losses of the switch. Comparing to conventional PWM method in Fig. 5-5(b), the peak switch current in Fig. 5-5(a) decreases when input voltage goes higher and witching frequency increases. It results in reduced turn-off switching losses in valley switching method, because turn-off switching losses are dependent on the peak current and switching frequency. The RMS values of switch current are almost the same in two control approaches, resulting in the same conduction losses. Since both turn-on and turn-off switching losses are reduced, the efficiency of valley switching technique can be improved.



(a) when input voltage close to its peak value

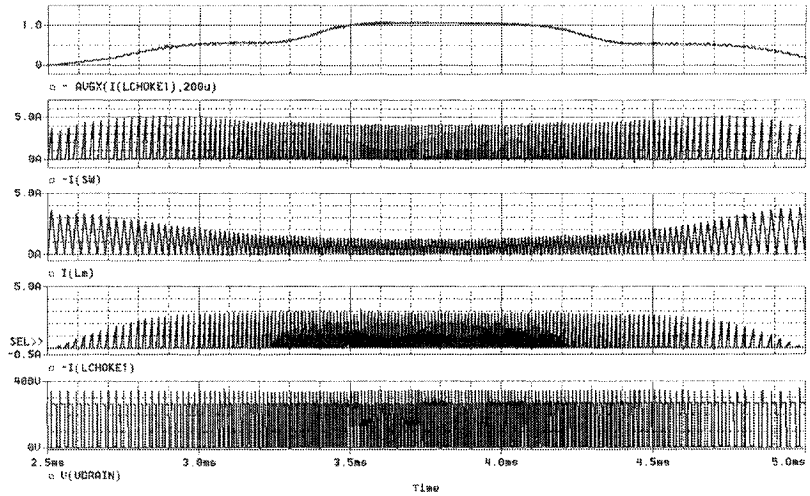


(b) when input voltage close to zero

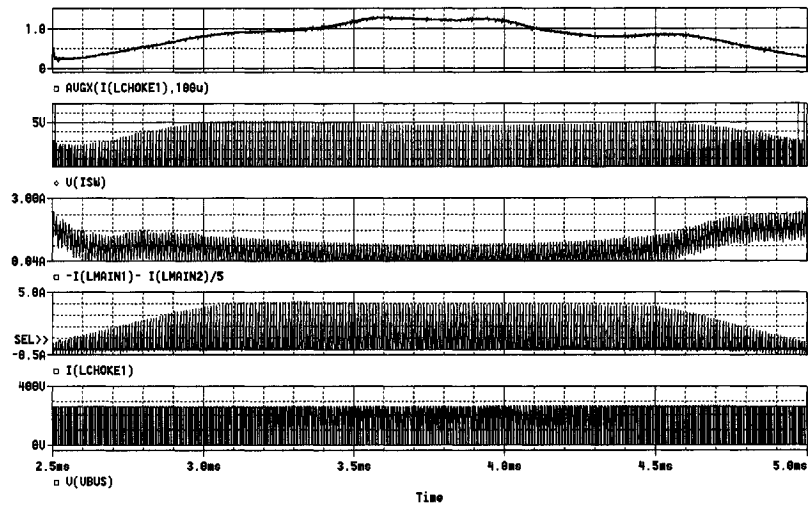
Traces from top to bottom:

a. Switch current
b. T_2 magnetizing current (i_{M2})
c. T_1 magnetizing current (i_{M1})
d. Voltage across Switch (V_{ds})

Fig. 5-4 Simulated operational waveforms over switching cycle



(a) Valley switching method



(b) Conventional PWM method

Traces from top to bottom:

a. Input current
b. Switch current
c. T2 magnetizing current (iM2)
d. T1 magnetizing current (iM1)
e. Voltage across Switch (Vds)

Fig. 5-5 Operational waveforms over half line period

As discussed above, some input power is directly transferred to the output, such as the shadowed portion in current i_{D2} in Fig. 5-2 (b), so the actual load on the DC-DC flyback circuit is varying. Because the switching frequency with valley switching technique is dependent on the load, the switching frequency will keep changing in one line cycle. The direct transferred power is low, when input voltage is near zero, so the delivered power by DC-DC cell is higher and the switching frequency will be low. As the input voltage increase, more power is direct transferred to output end, and the switching frequency will increase. The maximum switching frequency can still be designed to be equal to or less than in conventional PWM control by properly choosing the circuit parameter and skipping some oscillation cycle.

5.3 Experimental Verification

One 20VDC/90W prototype based on the Bi-flyback topology in Fig. 5-2 (a) with valley switching technique was built to verify the operation. The components in this prototype include:

- MOSFET Q_1: FB9N65A (650V, 9A)
- Input Fast diode D_{in}: DSEI 8-06 (600V, 8A)
- Secondary diode D_1 & D_2: MBR20-200CT (200V, 20A)
- Storage capacitor Cs: 450V 100uF
- Clamp capacitor Cc: 10nF
- Transformer T_1: primary inductance 90uH, turn ratio 7:1

- Transformer T_2: primary inductance 500uH, turn ratio 5:1
- Controller IC: NCP1205

Figure 5-6 shows the input current waveform with power factor equal to 0.97, which excels the industrial requirements. This result is similar to that with conventional PWM control method.

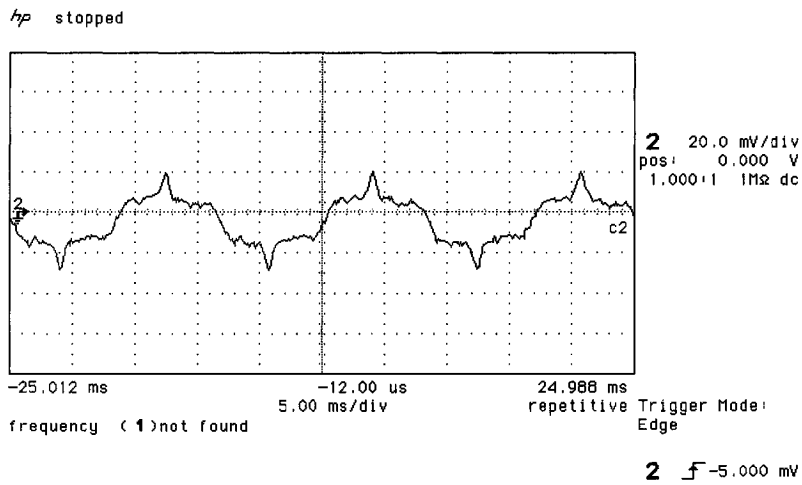
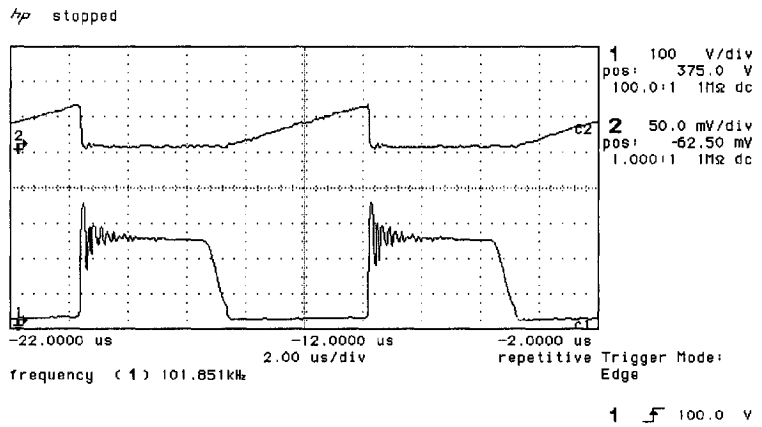


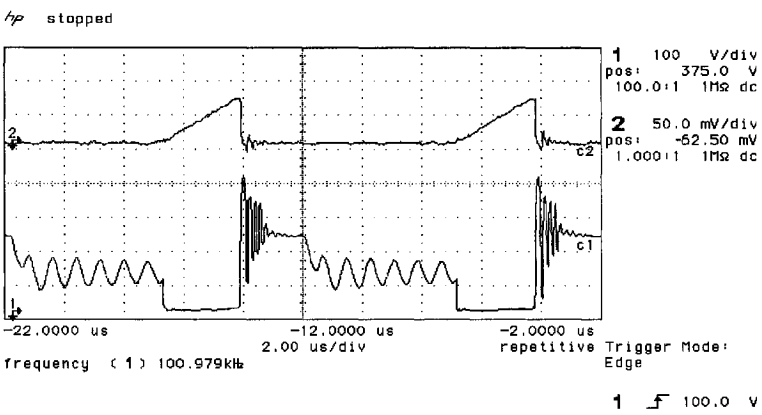
Fig. 5-6 Input current waveform

The voltage and current waveforms of the main switch are shown in Fig. 5-7. When the instantaneous input voltage is near zero, the voltage across the switch is reduced to zero before it is turned on, as shown in Fig. 5-7(a). It is because that the reflected output voltage by transformer T_2 (n_2*V_o) is higher than intermediate bus voltage, and the resonance between switch parasitic capacitor and transformer T_2 magnetizing inductance will bring the voltage across switch to or below zero. So the switch is almost under zero voltage switching condition.

When input voltage goes higher, more input power will be directly transferred to the output. So the actual power processed by DC-DC flyback circuit is reduced, which will reduce the duty cycle also at this time, as shown in Fig. 5-7(b). In order to limit the maximum switching frequency, the turn-on time is not at the first valley voltage point. Some oscillation cycles are skipped before the MOSFET is turned on.



(a) when input voltage close to zero



(b) when input voltage close to its peak value

Top trace: switch current, bottom trace: switch voltage V_{ds}

Fig. 5-7 Operational waveforms over switching cycle

5.4 Summary

Due to its special configuration, typical DC-DC control method can be implemented in flyboost derived single stage PFC converters. Valley switching control approach is good for flyback converter due to its simplicity and soft-switching feature. In this chapter, this control method was implemented to Bi-flyback topology to reduce the turn-on switching losses. The cycle-skip technique was chosen to limit the maximum switching frequency.

CHAPTER 6

AVERAGE MODEL OF FLYBOOST PFC CIRCUIT

6.1 Introduction

The single stage PFC converter integrates the PFC cell and DC-DC conversion cell. This integration simplifies the circuit to achieve low cost. But it makes the analysis of this kind of circuits difficult, especially for AC small signal analysis. AC small signal analysis is important to find out the converter transfer function, which is important for the crossover frequency and phase margin of converter design.

For typical single stage PFC converter, the input energy is transferred to the intermediate bus capacitor through PFC cell, and then transferred to output by DC-DC cell. Normally the PFC cell and DC-DC cell work independently. So the average model can be achieved by averaging the circuit parameters over input line period. This modeling method was used popularly.

For the single stage PFC converter with direct power transfer or parallel power transfer, there is some input power directly transferred to the output end. The direct power transfer happens in some interval during one line period. And it depends on the instantaneous input, output and intermediate bus voltage. And the controller should

respond very fast to any deviation of output voltage to remove any low frequency ripple. So the crossover frequency of the loop will be much higher than the line frequency. It makes the above average method impractical to analysis the AC characteristics of this kind of converter. In flyboost derived single stage PFC converters, such as Bi-flyback converter in previous chapter, there are two operational modes, depending on the instantaneous input voltage. To analysis this converter, special modeling method is required.

In this chapter, one average modeling method is applied to achieve the average model for flyboost derived single stage PFC converter. The method is to find out the unified average model over the switching period, which can represent all operation modes. Once the average model is obtained, the AC small signal analysis is performed at different intervals over the line period to figure out the transfer function at that interval. Then the crossover frequency and phase margin for different interval can be checked for proper controller design.

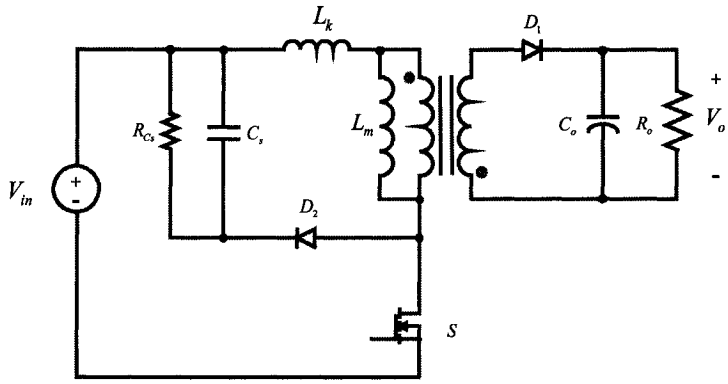
6.2 Operation analysis of non-ideal flyback circuit

In real circuit, flyback transformer always has some leakage inductance, which will cause high voltage spike on the main switch. And it also affects the operation of the flyback circuit. Fortunately, the leakage inductance is small enough to be neglected for most cases, if good snubber is included.

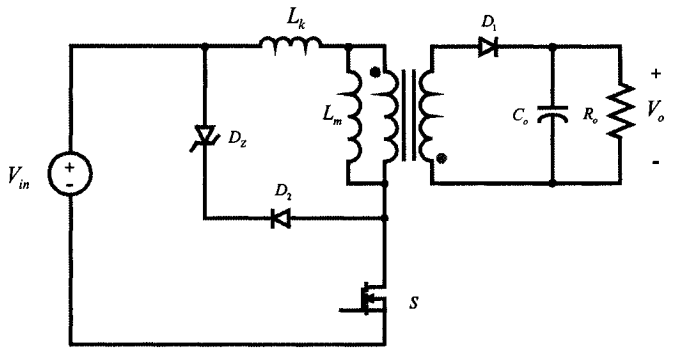
When flyback circuit is used as flyboost PFC cell, the leakage inductance plays an important role to the operation of the circuit. It will smooth the transition procedure between flyback mode and boost model. In this section, the operation of flyback circuit with leakage is discussed in details.

Figure 6-1 shows the typical flyback converter. There are two types of popular snubber circuit for non-ideal (real) flyback converter with leakage inductance: RCD snubber in Fig. 6-1(a) and Zener diode snubber in Fig. 6-1(c). For steady state analysis, we can assume that the voltage across the capacitor and Zener is constant and can be replaced by a constant voltage source. In order to protect the main switch S from over-voltage damage when it is turned off, the diode D_2 will conduct to clamp the voltage to a constant voltage source, snubber capacitor C_S or Zener D_Z. So we can simplify those typical flyback circuit into a 5-terminal circuit to analyze its operation, which is used in below analysis. Three voltage sources, V_{in}, V_{bus} and V_o, are connected to the block circuit to form a complete flyback circuit.

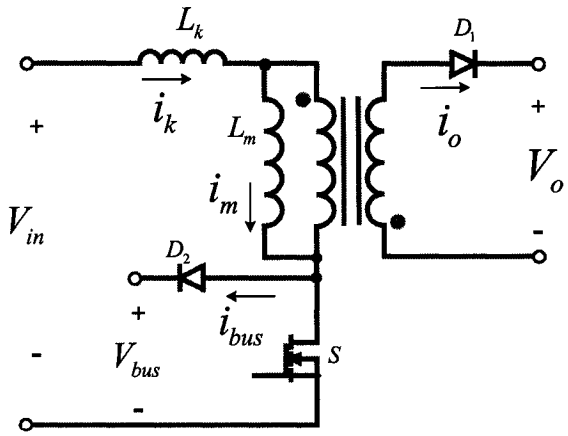
There are only two operation modes in simple flyback circuit when leakage is neglected: CCM and DCM, depending on the current waveform in the magnetizing inductor of flyback transformer. But the operation of non-ideal flyback circuit is much complicated. Under steady state, there are three operation modes depending on the current waveform in magnetizing inductor. And if the leakage inductor is large enough, it may operate as boost circuit, which adds another two operation modes.



(a) With R-C-D snubber



(b) With Zener diode snubber



(c) Non-ideal Flyback block circuit

Fig. 6-1 Typical flyback circuit

Pspice switching model of non-ideal flyback circuit based on Fig. 6-1 was developed for simulation. All operation conditions were tested to look for possible operation modes with corresponding operation waveforms. Those operation modes are discussed in detail below. For simplification, the operation mode is defined by the current conduction mode of magnetizing inductor and leakage inductor of flyback transformer. For example, flyback CCM+DCM means that the transformer operates like a transformer, with magnetizing inductor operating under CCM and leakage inductor operating under DCM.

6.1.1 Flyback DCM+DCM

Firstly, one simple operation mode is analyzed here. The transformer is assumed to operate like typical flyback transformer. Later the operational condition for each mode will be discussed. When the load is not heavy enough to keep flyback transformer magnetizing current continuous, the current in leakage inductor is also discontinuous. This operation mode is referred to be Flyback DCM+DCM.

There are four operational intervals as shown in Fig. 6-2:

Interval 1 ($t_0 \sim t_1$): Switch S is turned on at t_0. The input voltage V_{in} is applied to primary winding of flyback transformer, which includes magnetizing inductor L_m and leakage inductor L_k. The input voltage across those inductors is related to their inductance value. The current in both inductors is identical. Since both inductors operate in DCM, the current starts linearly increasing from zero. As shown in Fig. 6-2, the currents are given by:

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k} V_{in} \tag{6.1}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k} V_{in} \tag{6.2}$$

While, L_m is the magnetizing inductance, L_k is the leakage inductance, i_m is the current through L_m, and i_k is current through L_k.

When the S is turned off at t_1, the current through both inductors reaches the peak value, which is equal to:

$$I_{m1} = \frac{V_{in} D_{on} T_s}{L_m + L_k} \tag{6.3}$$

Where, D_{on} is the duty cycle, and T_s is the switching period.

The current to V_{bus} and V_o is equal to 0 during this interval, like typical flyback circuit.

Interval 2 ($t_1 \sim t_2$): Switch S is turned off at t_1. The magnetizing inductor will discharge to output through transformer secondary winding, while leakage inductor discharge through V_{bus}. Once the secondary diode D_1 in Fig. 6-2.(c) conducts, the voltage across L_m is clamped to nV_o (V_o: output voltage, n: transformer turn ratio). So the voltage across L_k can be derived from its discharge loop. The equations for the current are:

$$L_m \frac{di_m}{dt} = -nV_o \tag{6.4}$$

$$L_k \frac{di_k}{dt} = V_{bus} - V_{in} - nV_o \tag{6.5}$$

And we define,

$$D_{lk} = \frac{t_2 - t_1}{T_s} \tag{6.6}$$

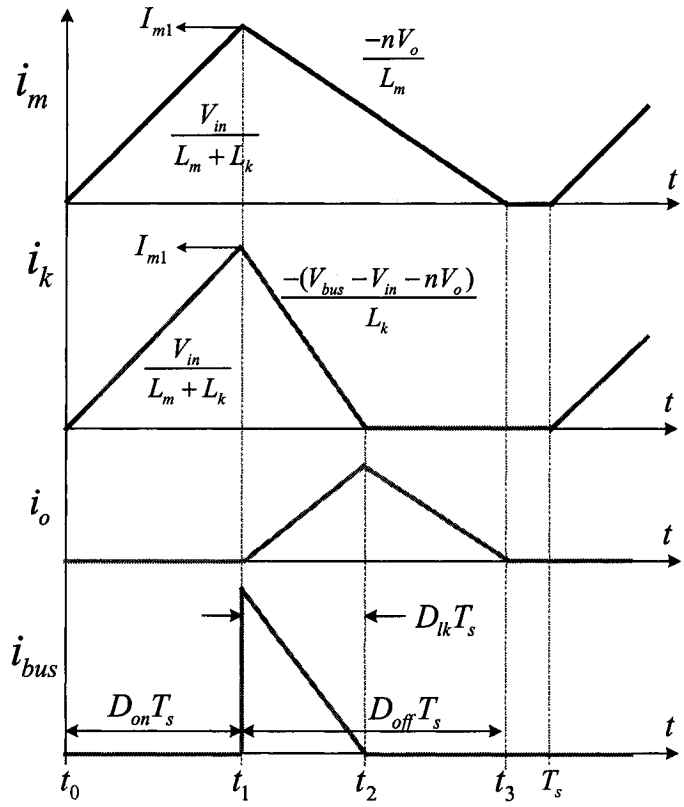


Fig. 6-2 Operation waveforms of flyback DCM+DCM mode

The current flowing through D_2, i_{bus}, is equal to i_k during this interval, while the current flowing through D_1, i_o, is equal to the product of transformer turn ratio and the difference between i_m and i_k.

Interval 3 ($t_2 \sim t_3$): The current i_k goes to zero at t_2, and diode D_2 will keep it at zero. The magnetizing inductor still discharges its current to output until its current reaches zero also at t_3. The voltage across L_k is zero, while the voltage across L_m is nV_o. And we define,

$$D_{off} = \frac{t_3 - t_2}{T_s} \tag{6.7}$$

Interval 4 (t_3 ~T_S): During this interval, all currents are zero, and the voltage across both inductors are zero also. The main switch S is turned again at T_S, and a new switching cycle begins.

In order to obtain its average model, the average parameter of this mode need to be derived. The average voltage across L_m in one switching period can be derived by dividing the sum of all volt-second products across L_m during four intervals by the switching period T_s, which is equal to:

$$E_{Lm} = \frac{L_m}{L_m + L_k} V_{in} D_{ON} - n V_o D_{OFF} \tag{6.8}$$

Similarly, The average voltage applied to L_k is given by:

$$E_{Lk} = \frac{L_k}{L_m + L_k} V_{in} D_{ON} - (V_{bus} - V_{in} - n V_o) D_{LK} \tag{6.9}$$

The average current parameters can be derived from Fig. 6-2. Below is the final result:

$$I_m = I_{m1}\left(D_{ON} + D_{Off}\right)/2 \tag{6.10}$$

$$I_k = I_{m1}\left(D_{ON} + D_{lk}\right)/2 \tag{6.11}$$

$$I_o = n\left(I_m - I_k\right) \tag{6.12}$$

$$I_{bus} = I_{m1} D_{lk}/2 \tag{6.13}$$

6.2.2 Flyback CCM+DCM

Flyback CCM+DCM happens when the output load increases to some level that the current through the magnetizing inductor becomes continuous, and current through L_k still discontinuous. As shown in Fig. 6-3, there are four operation intervals in this mode. The leakage inductor will cause some delay for the current transition between transformer primary winding and secondary winding.

Interval 1 ($t_0 \sim t_1$): Switch S is turned on at t_0. The input voltage V_{in} is applied to magnetizing inductor L_m and leakage inductor L_k. The current in magnetizing inductor starts with some current at t_0 because it is under continuous conduction mode. Leakage current, i_k, will increase from zero since it is discontinuous. Before i_k reaches the same value as the current in magnetizing inductor (i_m), the secondary winding of flyback transformer have to flow some current, which is equal to the difference between the magnetizing current i_m and leakage inductor current i_k. So the voltage across the magnetizing inductor is equal to the reflected output voltage, $n*V_o$. The voltage across leakage inductor is the sum of V_{in} and $n*V_o$. Based on those analyses, we can get:

$$L_m \frac{di_m}{dt} = -nV_o \tag{6.14}$$

$$L_k \frac{di_k}{dt} = V_{in} + nV_o \tag{6.15}$$

And the current through secondary diode D_1 is equal to:

$$i_o = n \cdot (i_m - i_k) \tag{6.16}$$

At t_1, the current in leakage and magnetizing inductor is equal to the same value, I_{m2} in Fig. 6-2. We define,

$$D_{out} = \frac{t_1 - t_0}{T_s} \tag{6.17}$$

Interval 2 ($t_1 \sim t_2$): From t_1 on, the current in both inductors will be identical, with the input voltage applied to both inductors corresponding to their inductance value. The interval is like the interval 1 in flyback DCM+DCM mode. So we also get:

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k} V_{in} \tag{6.18}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k} V_{in} \tag{6.19}$$

The S is turned off at t_2. And this interval is equal to:

$$t_2 - t_1 = (D_{on} - D_{out}) T_s \tag{6.20}$$

The current to V_{bus} and V_o is equal to 0 during this interval, like typical flyback circuit.

Interval 3 ($t_2 \sim t_3$): From t_3 on, the magnetizing inductor will discharge to output through transformer secondary winding, while leakage inductor discharge through V_{bus}, exactly like the interval 2 in flyback DCM+DCM mode. So,

$$L_m \frac{di_m}{dt} = -nV_o \tag{6.21}$$

$$L_k \frac{di_k}{dt} = V_{bus} - V_{in} - nV_o \tag{6.22}$$

$$D_{lk} = \frac{t_3 - t_2}{T_s} \tag{6.23}$$

The current flowing through D_2, i_{bus}, is equal to i_k during this interval, while the current flowing through D_1, i_o, is equal to the product of transformer turn ratio and the difference between i_m and i_k.

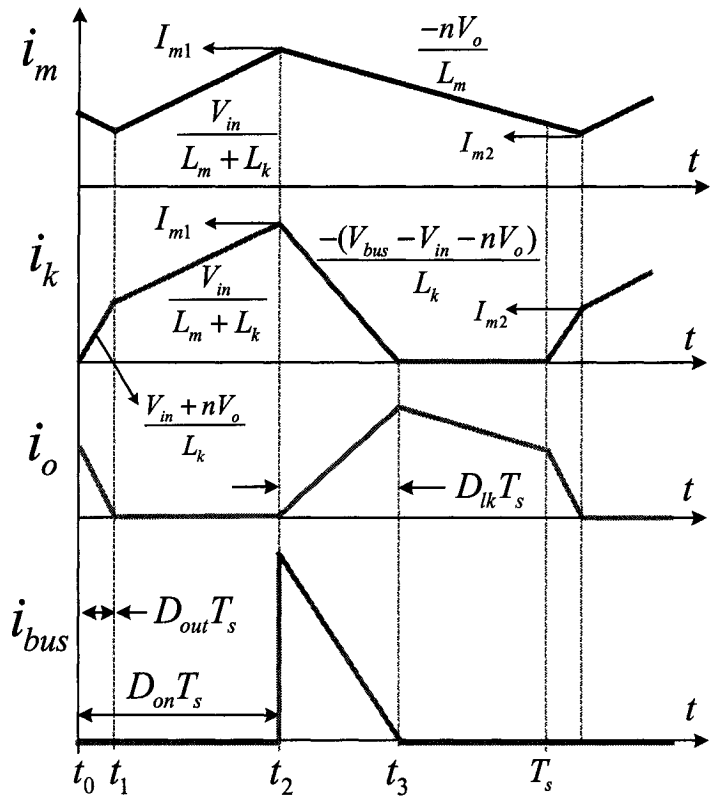


Fig. 6-3 Operation waveforms of flyback CCM+DCM mode

Interval 4 (t_3 ~T_S): The current i_k goes to zero at t_2, and diode D_2 will keep it at zero. The magnetizing inductor continues to discharge to output until the main switch S is turned on T_S. We have:

$$L_m \frac{di_m}{dt} = -nV_o \tag{6.24}$$

Also we need to obtain the average parameter for this mode. Using the waveform in Fig. 6-3 and the above equation, we can obtain the important parameters like in flyback DCM+DCM mode.

The average volt-second across L_m in one switching period is equal to:

$$E_{Lm} = \frac{L_m}{L_m + L_k} V_{in} (D_{ON} - D_{out}) - nV_o (1 - D_{ON}) \tag{6.25}$$

The average voltage applied to L_k is given by:

$$E_{Lk} = (V_{in} + nV_o) D_{out} + \frac{L_k}{L_m + L_k} V_{in} (D_{ON} - D_{out}) - (V_{bus} - V_{in} - nV_o) D_{LK} \tag{6.26}$$

The average current parameters can be derived from Fig. 6-3:

$$I_m = \frac{I_{m1} + I_{m2}}{2} \tag{6.27}$$

$$I_m = I_{m1} - \frac{1}{2} \frac{V_{in} (D_{ON} - D_{out}) T_S}{L_m + L_k} \tag{6.28}$$

$$I_k = I_{m2} D_{ON} / 2 + I_{m1} (D_{ON} + D_{lk} - D_{out}) / 2 \tag{6.29}$$

$$I_o = n(I_m - I_k) \tag{6.30}$$

$$I_{bus} = I_{m1} D_{lk} / 2 \tag{6.31}$$

6.2.3 Flyback CCM+CCM

During start-up or high load on the bus circuit (snubber), the non-ideal flyback converter may enter one condition that both leakage and magnetizing inductor operate

under CCM. As shown in Fig. 6-4, there are three operation intervals in this mode, which are discussed below.

Interval 1 ($t_o \sim t_1$): Switch S is turned on at t_o. The input voltage V_{in} is applied to magnetizing inductor L_m and leakage inductor L_k. Because the current in magnetizing inductor is higher that the current in leakage inductor, there still exists a current-transition interval, which is like the interval 1 in flyback CCM+DCM. So all equations in that interval is applicable here. So we have:

$$L_m \frac{di_m}{dt} = -nV_o \tag{6.32}$$

$$L_k \frac{di_k}{dt} = V_{in} + nV_o \tag{6.33}$$

$$i_o = n \cdot (i_m - i_k) \tag{6.34}$$

$$D_{out} = \frac{t_1 - t_0}{T_s} \tag{6.35}$$

Interval 2 ($t_1 \sim t_2$): From t_1 on, the current in both inductors will be identical, with the input voltage applied to both inductors corresponding to their inductance value. The interval is like the interval 2 in flyback CCM+DCM mode. So we also get:

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k} V_{in} \tag{6.36}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k} V_{in} \tag{6.37}$$

$$t_2 - t_1 = (D_{on} - D_{out}) T_s \tag{6.38}$$

Interval 3 ($t_2 \sim T_S$): At t_2, the main switch is turned off. The magnetizing inductor will discharge to output through transformer secondary winding, while leakage inductor discharge through V_{bus}. When the switch is turned on at T_s, there are some current in both leakage and magnetizing inductor. Like previous mode, we have:

$$L_m \frac{di_m}{dt} = -nV_o \tag{6.39}$$

$$L_k \frac{di_k}{dt} = V_{bus} - V_{in} - nV_o \tag{6.40}$$

The average volt-second across L_m in one switching period is equal to:

$$E_{Lm} = \frac{L_m}{L_m + L_k} V_{in}(D_{ON} - D_{out}) - nV_o(1 - D_{ON}) \tag{6.41}$$

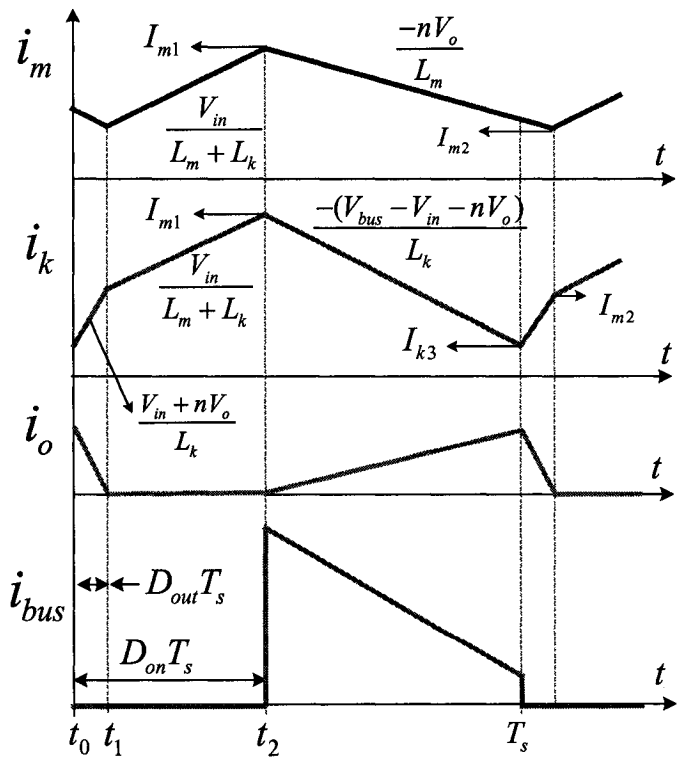


Fig. 6-4 Operation waveforms of flyback CCM+CCM mode

The average voltage applied to L_k is given by:

$$E_{Lk} = (V_{in} + nV_o)D_{out} + \frac{L_k}{L_m + L_k} V_{in}(D_{ON} - D_{out}) - (V_{bus} - V_{in} - nV_o)(1 - D_{ON}) \tag{6.42}$$

The average current parameters can be derived from Fig. 6-4:

$$I_m = \frac{I_{m1} + I_{m2}}{2} \tag{6.43}$$

$$I_m = I_{m1} - \frac{1}{2} \frac{V_{in}(D_{ON} - D_{out})T_S}{L_m + L_k} \tag{6.44}$$

$$I_k = I_{m1}(1 - D_{out})/2 + I_{m2}D_{ON}/2 + I_{k3}(1 - D_{ON} + D_{out})/2 \tag{6.45}$$

$$I_o = n(I_m - I_k) \tag{6.46}$$

$$I_{bus} = (I_{m1} + I_{k3})(1 - D_{ON})/2 \tag{6.47}$$

In some rare case, the current in leakage inductor may not be able to reach the same value as one in magnetizing inductor during the S ON interval. If so, interval 2 will no exist with $D_{out}=D_{on}$. The operation waveform is shown in Fig. 6-5. Some attentions need to handle this mode.

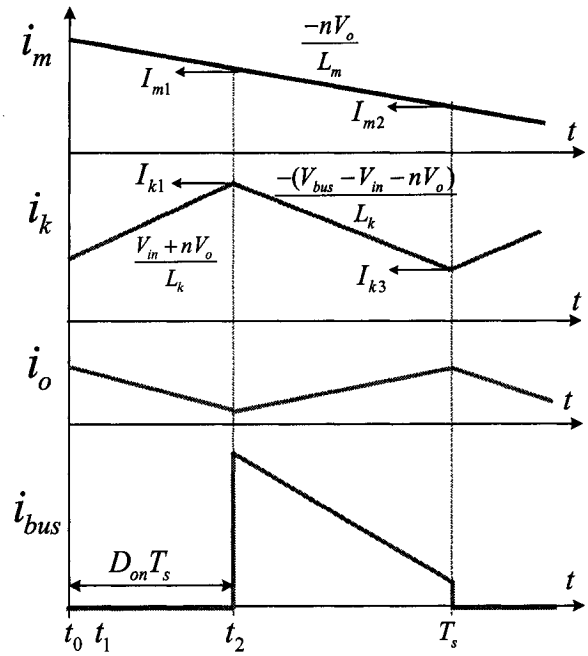


Fig. 6-5 Special operation case for flyback CCM+CCM mode

6.2.4 Boost DCM+DCM

During start-up, heavy load for bus terminal or for PFC application, non-ideal flyback converter may operate like boost converter, without any current transferred to secondary output end. Firstly, we discuss on DCM+DCM. As shown in Fig. 6-6, there are three operation intervals in this mode. The leakage inductor will cause some delay for the current transition between transformer primary winding and secondary winding.

Interval 1 ($t_o \sim t_1$): Switch S is turned on at t_o. The input voltage V_{in} is applied to magnetizing inductor L_m and leakage inductor L_k. The current in magnetizing and leakage current will both increase from zero. We can get:

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k} V_{in} \tag{6.48}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k} V_{in} \tag{6.49}$$

Interval 2 ($t_1 \sim t_2$): The main switch is turned off at t_1, the inductors will discharge their current to bus terminal like typical boost. So we also get:

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k}(V_{in} - V_{Bus}) \tag{6.50}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k}(V_{in} - V_{bus}) \tag{6.51}$$

Interval 3 ($t_2 \sim T_S$): The S is turned off at t_2. And the current through both inductors are kept at zero.

The average volt-second across L_m in one switching period is equal to:

$$E_{Lm} = \frac{L_m}{L_m + L_k} V_{in} D_{ON} - \frac{L_m}{L_m + L_k}(V_{bus} - V_{in}) D_{off} \tag{6.52}$$

The average voltage applied to L_k is given by:

$$E_{Lk} = \frac{L_k}{L_m + L_k} V_{in} D_{ON} - \frac{L_k}{L_m + L_k}(V_{bus} - V_{in}) D_{off} \tag{6.53}$$

The average current parameters can be derived from Fig. 6-6:

$$I_m = I_k = I_{m1} \frac{D_{ON} + D_{off}}{2} \tag{6.54}$$

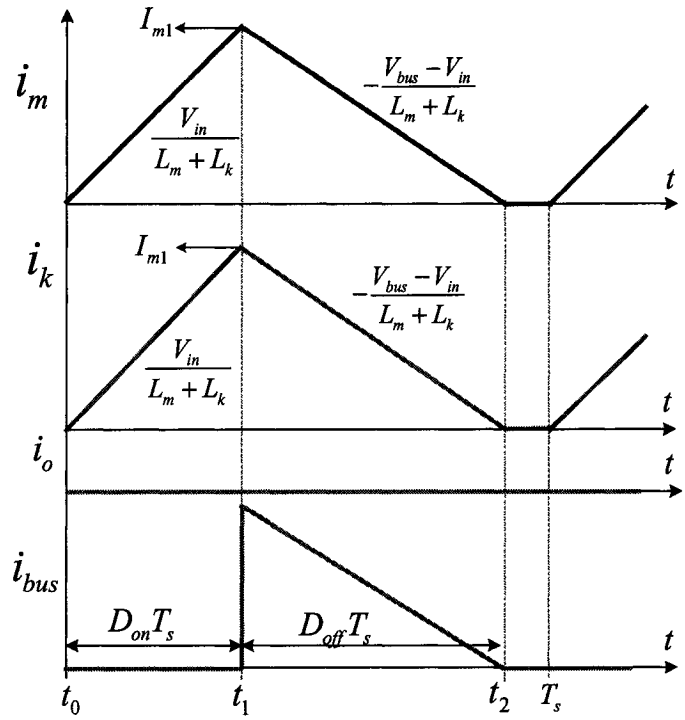


Fig. 6-6 Operation waveforms of Boost DCM+DCM mode

6.2.5 Boost CCM+CCM

Under this mode, the transformer primary winding operate like typical CCM boost. Figure 6-7 shows the typical operational waveform.

Interval 1 ($t_o \sim t_1$): Switch S is turned on at t_o. The input voltage V_{in} is applied to magnetizing inductor L_m and leakage inductor L_k.

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k} V_{in} \tag{6.55}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k} V_{in} \tag{6.56}$$

Interval 2 ($t_1 \sim T_S$): The main switch is turned off at t_1, the inductors will discharge their current to bus terminal until a new switching cycle begins at T_s.

$$L_m \frac{di_m}{dt} = \frac{L_m}{L_m + L_k}(V_{in} - V_{Bus}) \tag{6.57}$$

$$L_k \frac{di_k}{dt} = \frac{L_k}{L_m + L_k}(V_{in} - V_{bus}) \tag{6.58}$$

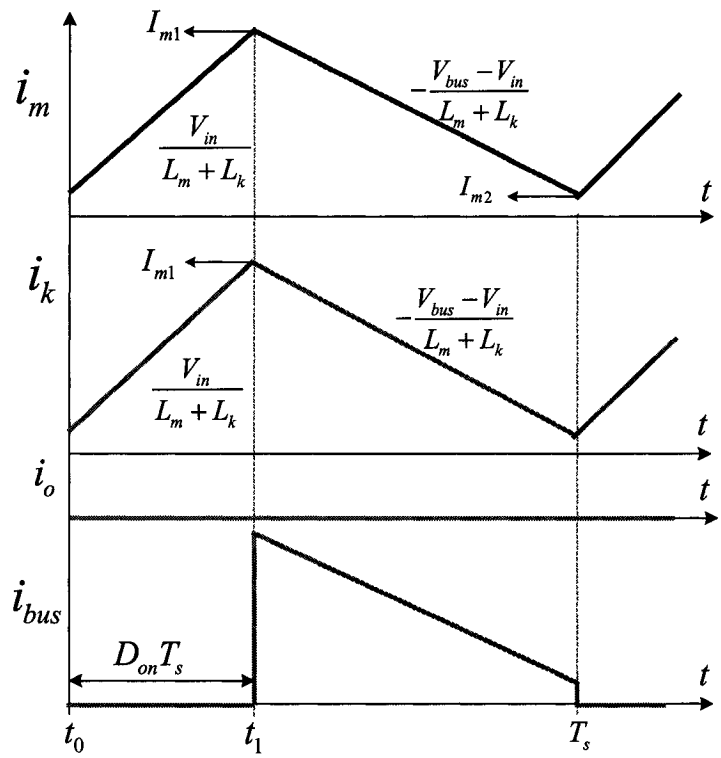


Fig. 6-7 Operation waveforms of Boost CCM+CCM mode

The average volt-second across L_m in one switching period is equal to:

$$E_{Lm} = \frac{L_m}{L_m + L_k} V_{in} D_{ON} - \frac{L_m}{L_m + L_k}(V_{bus} - V_{in})(1 - D_{ON}) \tag{6.59}$$

The average voltage applied to L_k is given by:

$$E_{Lk} = \frac{L_k}{L_m + L_k} V_{in} D_{ON} - \frac{L_k}{L_m + L_k} (V_{bus} - V_{in})(1 - D_{ON}) \tag{6.60}$$

The average current parameters can be derived from Fig. 6-7:

$$I_m = I_k = \frac{I_{m1} + I_{m2}}{2} \tag{6.61}$$

6.3 Average model for non-ideal flyback circuit

So far, the popular and effective AC analysis method of switching power supply is through the average model. The average modeling method of switching circuit is to find the averaged value of the switching parameters over one switching cycle, and then replace the original circuit by the averaged circuit. The average model can perform DC, transient and small signal AC analysis.

As discussed before, all fundamental converter topologies can be modeled by only averaging the operational parameters of switching components (MOSFET and diode) and inductors, while leaving capacitor, load and other components untouched. Like in switch Veippien model or Switching Inductor Model, the voltage across inductors is averaged over one switching cycle to generate a voltage-control-voltage source. This voltage-control-voltage source is then applied to the inductor. Based operational waveforms, the averaged current and voltage parameters for the switching terminals are achieved. Then controlled voltage source and current sources are developed to represent the average characteristics of original switching components. Those controlled voltage/current

sources and inductor consist of the average block model, which can be put back to original circuit to get a complete average model of the converter.

Here, the same method is implemented to develop the average model for non-ideal flyback circuit. Like in other average model, the switching components and inductors are separated from other circuits to form a block circuit, which is shown in Fig. 6-1(c). Once we get the average model for that block circuit, we can put it back to original circuit, shown in Fig. 6-1(a, b), to form the average model for the whole converter, which includes output capacitor, load and compensator etc.

As discussed in last section, there are totally five operation modes for non-deal flyback converter. Comparing to fundamental converter topologies, such as buck and boost, the non-ideal flyback circuit is more complicated, because of more operation modes and complicated current waveforms. The average model should be able to fit for all operation modes, which means that this model can operate like DCM boost under one operational condition, and it can also operate like CCM flyback under another condition. Like the SIM modeling method, one average model is need to be developed for each operation mode, and then those average models should be merged together to get a unified average model to represent all operation modes.

By carefully analyzing those operational waveforms discussed in last section, we found it was possible to merge those operation modes together. For example, the DCM+DCM flyback mode can be described as a special DCM+DCM flyback mode, if we assume that I_{m2} and D_{out} is equal to zero while D_{off} is less than $1-D_{on}$. And the flyback mode changes to boost mode if the slopes of magnetizing inductor current during S OFF interval is the same as that of leakage inductor current.

The fundamental method of the average model is to find the average voltage applied to each inductor, and the average current through each terminal. The known parameters include inductor average current, terminal voltage, and duty cycle. Based on those parameters, the period for each operational interval can be derived. Once the period value is obtained, we can use them to find the average voltage to the inductors and average current through each terminal. So the major job is to find the correct equations for the interval period calculation based on the terminal voltage and average current through inductors.

Firstly we define some terms for the model:

D_{off1}: the ratio of the period needed to totally discharge magnetizing inductor and the switching period;

D_{off}: the ratio of the actual discharging period of magnetizing inductor and the switching period;

D_{leak1}: the ratio of the period needed to totally discharge leakage inductor and the switching period;

D_{leak}: the ratio of the actual discharging period of leakage inductor and the switching period;

D_{out}: the ratio of the period needed to totally discharge magnetizing inductor and the switching period;

D_{off}: the ratio of the period needed for the output terminal current to reduce to 0 and the switching period, shown in Fig. 6-4;

If the magnetizing current is continuous, D_{off1} will be longer than 1-D_{on}. If one limit function is implemented here to limit the maximum value of D_{off} to 1-D_{on}, then D_{off} can be used to represent both DCM and CCM. So we get:

$$D_{off} = \min\left(1 - D_{ON}, D_{off1}\right) \tag{6.62}$$

According to Fig. 6-2, when the magnetizing inductor current is discontinuous, its peak current is equal to:

$$I_{m1} = \frac{V_{in} D_{on} T_s}{L_m + L_k} \tag{6.63}$$

And the average current through magnetizing inductor is equal to:

$$I_m = \frac{I_{m1}\left(D_{on} + D_{off1}\right)}{2} \tag{6.64}$$

Based on Eqs. 6.63 and 6.64, we can get:

$$D_{off1} = \frac{2I_m\left(L_m + L_k\right)}{V_{in} D_{on} T_s} - D_{on} \tag{6.65}$$

When the magnetizing inductor current is continuous, the peak current through magnetizing inductor will be larger than the value obtained by Eq. 6.63. So the results obtained from Eq. 6.65 will be larger than 1-D_{on}. Then, the actual D_{off} value for both modes can be derived by Eq. 6.62. The DCM and CCM mode for magnetizing inductor is merged together by this equation.

The similar procedure can be implemented to leakage inductor, even though the current waveform of leakage inductor is more complicated. Based on Eq. 6.29, we can get:

$$D_{leak1} = \frac{2I_m - I_{m2}D_{on}}{I_{m1}} + D_{out} - D_{on} \tag{6.66}$$

And this value will be larger than 1-D_{on} when leakage inductor is under CCM, so the unified equation for D_{leak} is given by:

$$D_{leak} = \min\left(1 - D_{ON}, D_{leak1}\right) \tag{6.67}$$

Since those equations do not relate to the voltage across those inductors during S OFF interval. So those equations are valid for both flyback mode and boost mode.

Based on Fig. 6-4, we can obtain the period for current transition:

$$D_{out} = \frac{I_{m2} - I_{k3}}{V_{in} + nV_o} \frac{L_k}{T_s} \tag{6.68}$$

Considering the special case in Fig. 6-5, the maximum value should be limited to D_{on}. So the final equation is given by:

$$D_{out} = \min\left(\frac{I_{m2} - I_{k3}}{V_{in} + nV_o} \frac{L_k}{T_s}, D_{on}\right) \tag{6.69}$$

Under boost mode, the current in magnetizing and leakage inductors are identical, which means that I_{m2} is equal to I_{k3}, resulting D_{out} equal to zero. So this equation is also viable in Boost mode.

Once the interval period is known, based on the analysis and waveforms discussed in last section, we can obtain the equations for the current through each terminals of the block:

$$I_{in} = I_k \tag{6.70}$$

$$I_{bus} = \frac{I_{k1} + I_{k3}}{2} D_{leak} \tag{6.71}$$

$$I_o = n\left(I_m - I_k\right) \tag{6.72}$$

The peak value of leakage inductor current, I_{k1}, is equal to the peak value of magnetizing current, I_{m1}, except for the special case in Fig. 6-5. The unified equation for the peak value is:

$$I_{k1} = \min\left(I_{k3} + \frac{V_{in} + nV_o}{L_k} D_{on} T_s, I_{m1} \right) \tag{6.73}$$

Finally, equations for the voltage across the inductors are needed to figure out. Based on the operational waveforms, it is easy to find out the voltage during D_{out} and D_{on} interval. During Don interval, the input voltage is divided by the magnetizing and leakage inductor according to their inductance. And there is not D_{out} interval (D_{out}=0) for boost mode. So the voltage during those intervals are the same for both flyback and boost modes.

The voltage equation for S OFF interval is complicated. For flyback mode, the slew rate of the current slope for magnetizing and leakage inductor are different. When the output voltage increase, the slew rate of magnetizing current increase, while the slew rate of leakage current decrease. When those slew rates become equal to each other, the circuit enters boost mode. So we can use the limit function to merge flyback mode and boost mode.

Under flyback mode, the voltage across magnetizing inductor during S OFF interval is nV_o, while it is $(V_{bus}-V_{in})L_m/(L_m+L_k)$. The unified equation is given by:

$$V_{Lm} = \min\left(\frac{L_m}{L_m + L_k}(V_{bus} - V_{in}), nV_o\right) \tag{6.74}$$

Similarly, the unified equation for voltage across leakage inductor is given by:

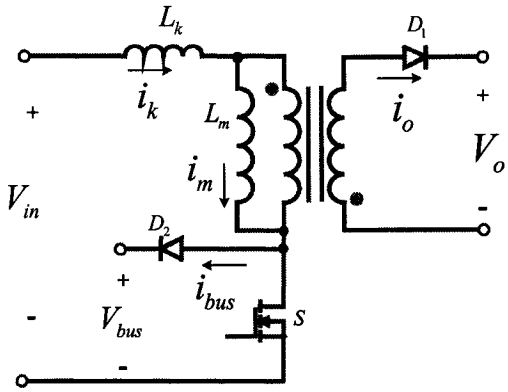
$$V_{Lk} = \max\left(\frac{L_k}{L_m + L_k}(V_{bus} - V_{in}), V_{bus} - V_{in} - nV_o\right) \tag{6.75}$$

The average voltage for the inductor can be obtained by dividing the sum of the product of the voltage and interval period by the switching period. The final equation is:

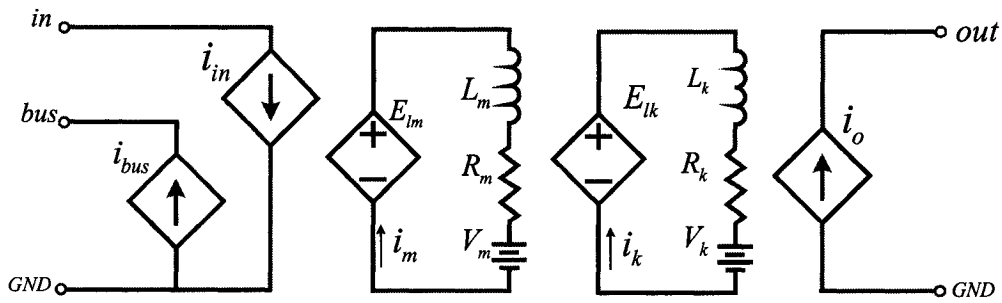
$$E_{Lm} = \frac{L_m V_{in}(D_{on} - D_{out})}{L_m + L_k} + V_{lm} \cdot (D_{off} + D_{out}) \tag{6.76}$$

$$E_{Lk} = \frac{L_k V_{in}(D_{on} - D_{out})}{L_m + L_k} + D_{out}(V_{in} + nV_o) + V_{lk} \cdot D_{leak} \tag{6.77}$$

Now, all average parameters for the non-ideal flyback block circuit in Fig. 6-8(a) are available. The average model of this block circuit is shown in Fig. 6-8(b). The resistors in series with inductors, R_m and R_k in Fig. 6-8 (b), represent the DC resistance of the inductor. The 0V voltage sources, V_m and V_k in Fig. 6-8 (b), are used to obtain the inductor current for other calculation purpose. The controlled voltage and current sources, E_{lm}, E_{lk}, i_{in}, i_{bus}, and i_o in Fig. 6-8(b), are based the equations obtained above.



(a) Non-ideal flyback block circuit

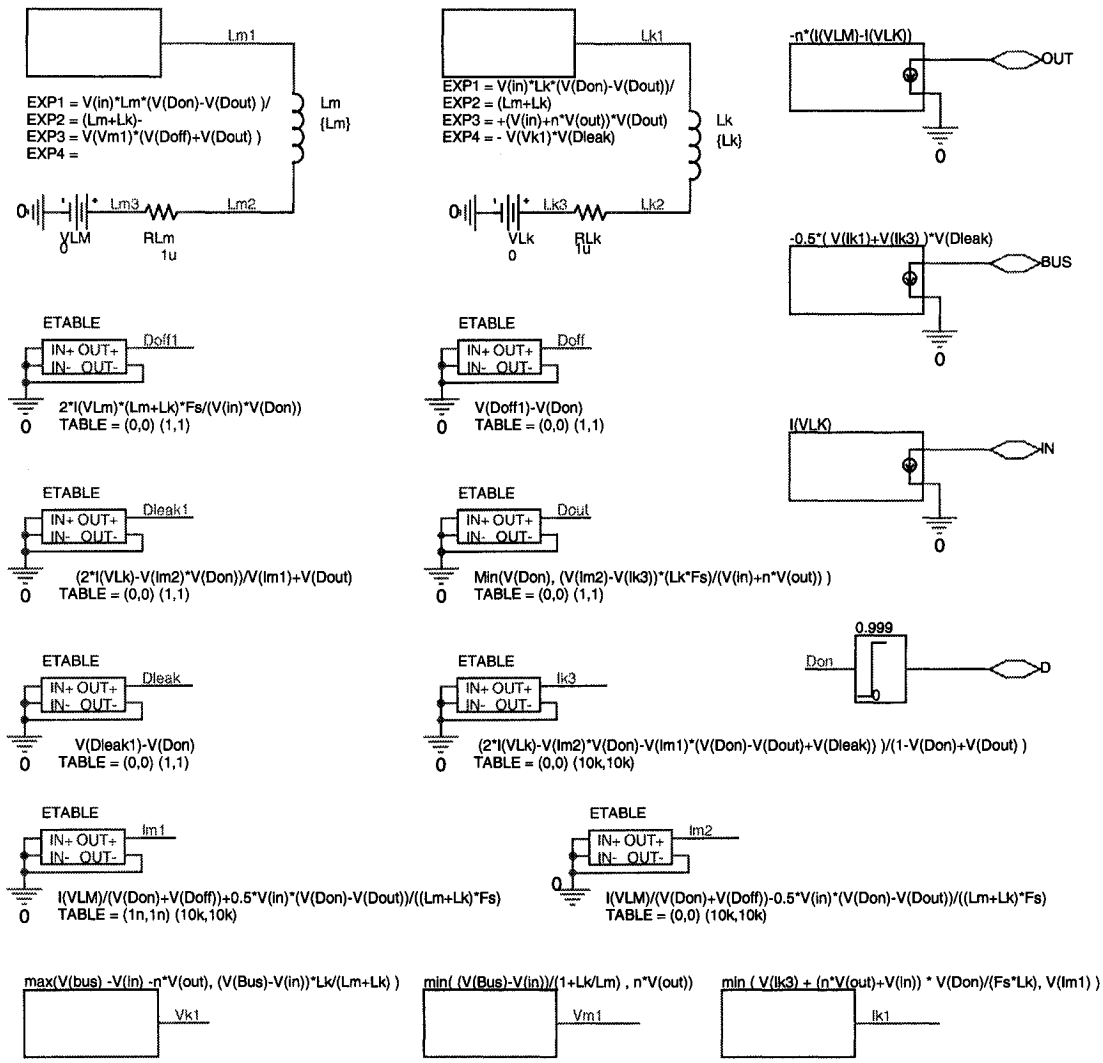


(b) Average model

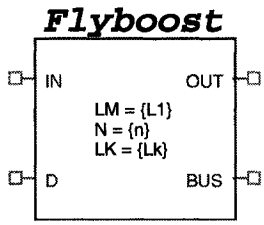
Fig. 6-8 Non-ideal flyback block circuit

Using the ABM function block, the average model is developed in OrCAD Pspice, shown in Fig. 6-9(a). This model can be used as a sub-circuit for the whole converter circuit. The sub-circuit block is shown in Fig. 6-9(b). The netlist of the sub-circuit is shown in Fig. 6-10. Since this block circuit operates like flyback and boost, it is defined as flyboost circuit, like we discussed in previous chapters.

Once the average model of this block circuit is available, it will be easy to figure the average model for those topologies derived from this basic circuit, such as Bi-flyback single stage PFC converter in precious chapter.



(a) Average model equations



(b) Sub-circuit block model in Pspice

Fig. 6-9 Average model of non-ideal flyback block circuit in Pspice

```
* Average model for non-ideal flyback circuit
* University of Central Florida
* May, 2003

.SUBCKT Flyboost BUS D IN OUT  PARAMS: n=5 Lk=99u Lm=500u Fs=100k

* Limit duty cycle input value to between 0 and 0.99
E_LIMIT1   DON    0       VALUE {LIMIT(V(D),0,0.99)}

* Calculation for peak current parameters
E_ABM1     IK1    0       VALUE {min( V(Ik3) + (n*V(out)+V(in))* V(Don)/(Fs*Lk), V(Im1) ) }
E_E6       IM1    0       TABLE {I(V_VLM)/(V(Don)+V(Doff))+0.5*V(in)*(V(Don)-
                          + V(Dout))/((Lm+Lk)*Fs)} ((1n,1n)(10k,10k))
E_E3       IM2    0       TABLE {I(V_VLM)/(V(Don)+V(Doff))-0.5*V(in)*(V(Don)-
                          + V(Dout))/((Lm+Lk)*Fs)} ((0,0)(10k,10k))
E_E8       IK3    0       TABLE {(2*I(V_VLk)-V(Im2)*V(Don)-V(Im1)*(V(Don)-
                          + V(Dout)+V(Dleak)))/(1-V(Don)+V(Dout))}   ( (0,0) (10k,10k) )

* Calculation for the period of different intervals
E_E4       DOUT   0       TABLE { min(V(Don),(V(Im2)-(Ik3))*(Lk*Fs)/(V(in)+n*V(out)))}
                          + ((0,0)(1,1))
E_E5       Dleak1 0       TABLE { (2*I(V_VLk)-V(Im2)*V(Don))/V(Im1)+V(Dout) } ( (0,0) (1,1) )
E_E7       DLEAK  0       TABLE { V(Dleak1)-V(Don) } ( (0,0) (1,1) )
E_E1       DOFF1  0       TABLE { 2*I(V_VLm)*(Lm+Lk)*Fs/(V(in)*V(Don)) } ( (0,0) (1,1) )
E_E2       DOFF   0       TABLE { V(Doff1)-V(Don) } ( (0,0) (1,1) )

* Calculation of the controlled voltage source for magnetizing and leakage inductors
E_ABM3     VM1    0       VALUE { min( (V(Bus)-V(in))/(1+Lk/Lm) , n*V(out))   }
E_ABM2     VK1    0       VALUE { max(V(bus)-V(in)-n*V(out), (V(Bus)-V(in))*Lk/(Lm+Lk) ) }


* Magnetizing inductor circuit
E_A1       LM1    0       VALUE { V(in)*Lm*(V(Don)-V(Dout) )/(Lm+Lk)-
                          + V(Vm1)*(V(Doff)+V(Dout) ) }
R_RLM      LM3    LM2     1u
L_LM       LM1    LM2     {Lm}
V_VLM      LM3    0       0

* Leakage inductor circuit
E_A2       LK1    0       VALUE { V(in)*Lk*(V(Don)-(Dout))/(Lm+Lk)+
                          +(V(in)+n*V(out))*V(Dout)-V(Vk1)*V(Dleak) }
L_LK       LK1    LK2     {Lk}
R_RLK      LK2    LK3     1u
V_VLK      LK3    0       0

* Calculation for the current through terminals
G_ABMI3    IN     0       VALUE { I(V_VLK) }
G_ABMI1    OUT    0       Value { -n*(I(V_VLM)-I(V_VLK))}
G_ABMI2    BUS    0       VALUE { -0.5*( V(Ik1)+V(Ik3) )*V(Dleak) }

.ENDS Flyboost
```

Fig. 6-10 Netlist of the average model of non-ideal flyback block circuit

6.4 Validation of Average model for non-ideal flyback circuit

The developed average model can perform DC and AC analysis for non-ideal flyback circuit. But its correctness and accuracy should be validated before we can use it. Since this model represents the operational characteristics of the non-ideal flyback converter, the simulation results from this model should be the same as those from models by other method. For example, the DC analysis results by the average model should be the same as the switching Pspice model. Because SIMPLIS software can perform AC analysis directly from switching model, it is chosen for comparison of AC analysis.

6.4.1 Verification of DC analysis by switching Pspice model

In this section, the DC operation simulation is tested and compared with the results from switching Pspice model. Figure 6-11 shows the average model of non-ideal flyback converter. The flyboost sub-circuit block includes the flyback transformer with leakage and switching components. The diode D_1 and D_2 in Fig. 6-11 is used to represent the voltage drop of diodes in actual circuit.

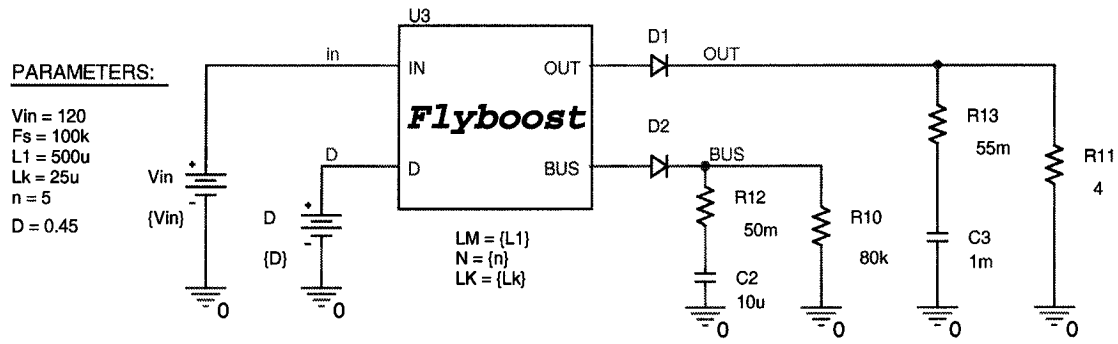


Fig. 6-11 Average model of non-ideal flyback converter

In the switching model, the non-ideal flyback transformer is represented by one ideal transformer and one leakage inductor in series with ideal transformer primary winging, as shown in Fig. 6-12. The same circuit parameters, such as input voltage and load resistor are used in this model as in average model.

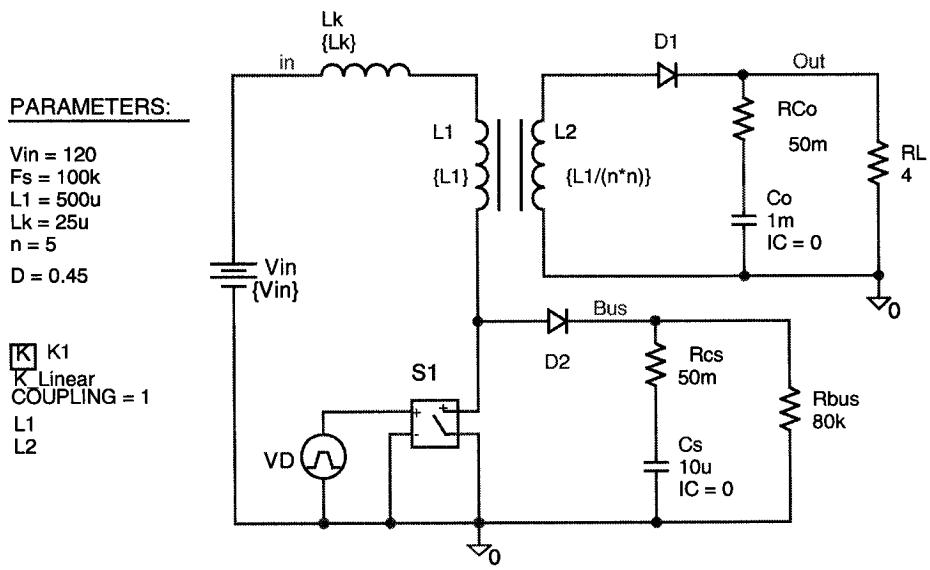
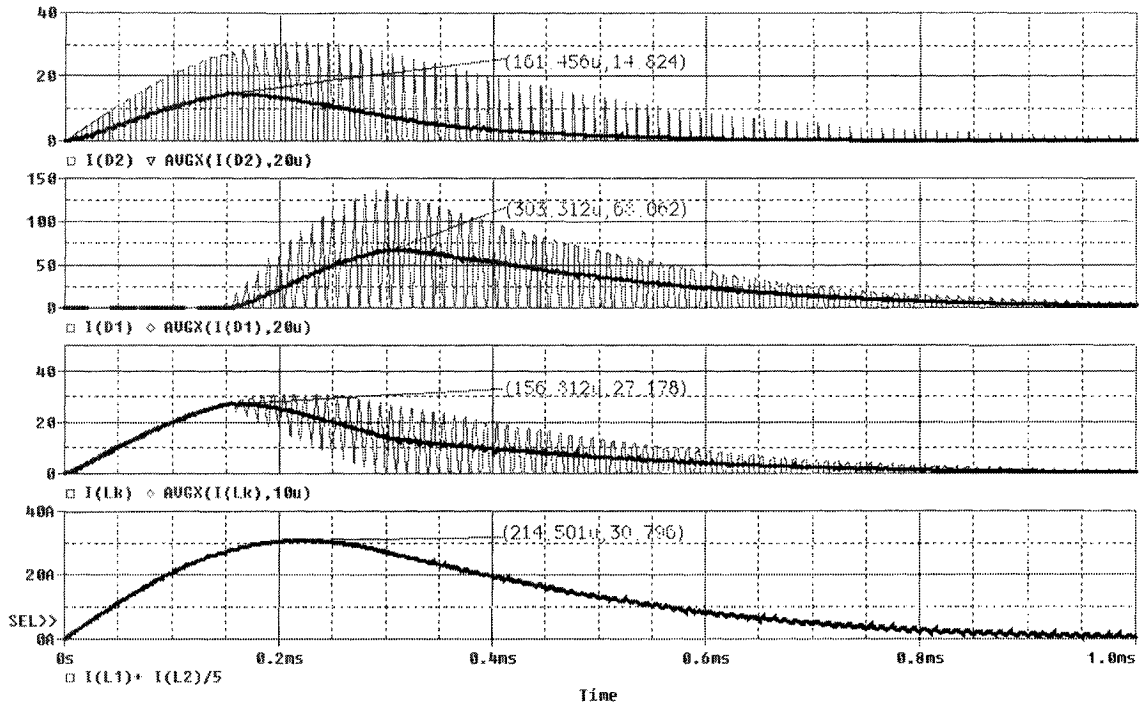


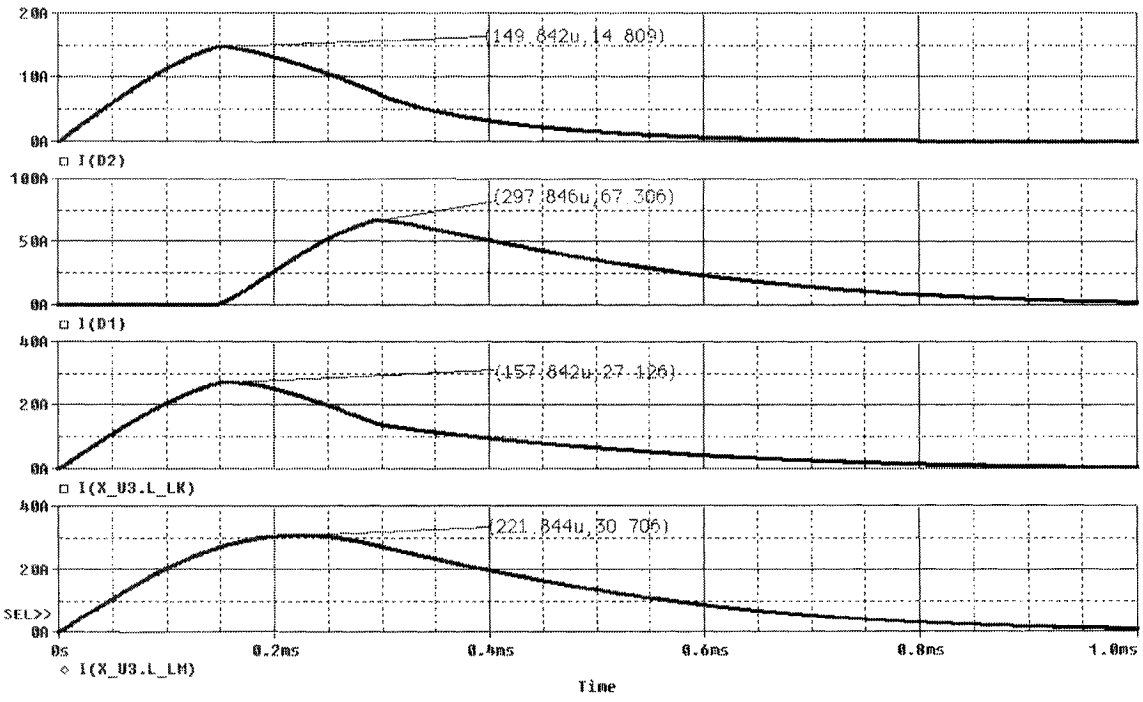
Fig. 6-12 switching model of non-ideal flyback converter

The start-up procedure of this circuit is simulated to test the DC operation. During start-up procedure, the circuit needs to charge the snubber capacitor Cs before providing current to output. When capacitor Cs is charged from zero voltage, the circuit works like boost under CCM. Then it operates like flyback, through Flyback CCM+CCM, flyback CCM+DCM, flyback DCM+DCM. So this simulation can test most of the operation of the circuit.

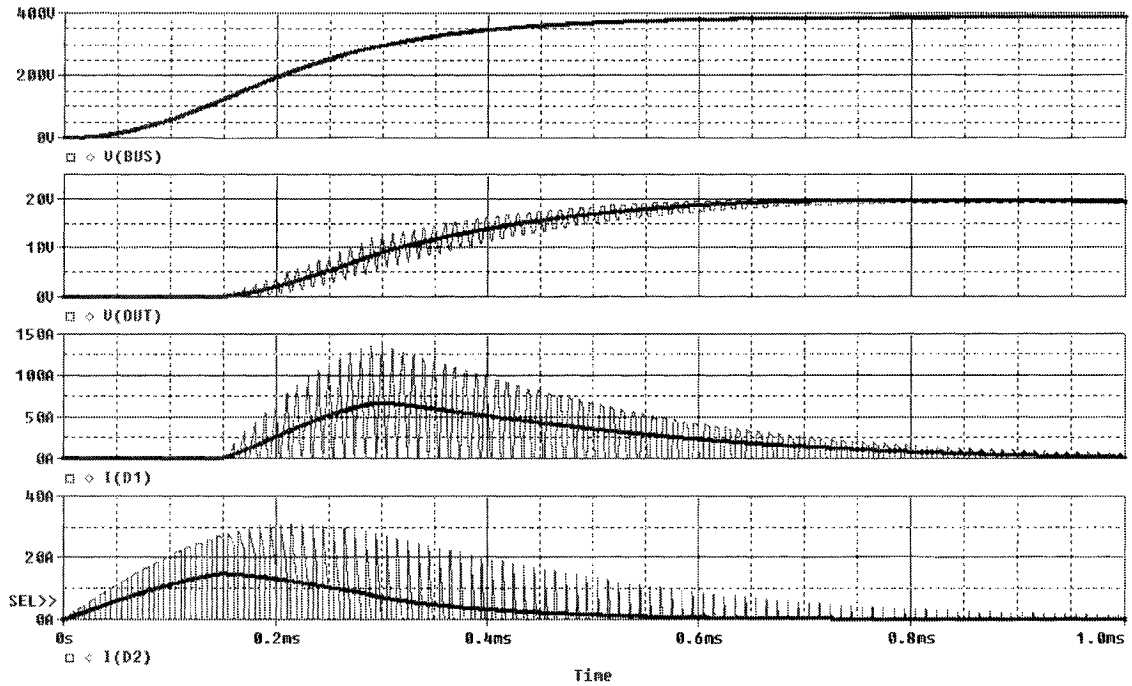
The simulation results from both models are shown in Fig. 6-13. In Fig. 6-13(a), the current waveform from switching model is shown. The average current waveforms of switching model are illustrated by the AVGX function. For example, AVGX(I(D2), 20u) is to calculate the average value of each 20us (two switching cycle), which represent the instantaneous average value of the current through D_2. Figure 6-13(b) shows the corresponding current waveforms obtained from average model. The peak value and time of each current waveform are labeled in those drawing. The results correspond with each other very well.



(a) Current and its average waveform in switching model



(b) Current waveforms in average model



(c) Average model results appended with the switching model results

Fig. 6-13 Simulation results comparison between average model and switching model

In Fig. 6-13(c) illustrates the voltage and current waveforms from both models. The "Append waveform..." function is used here to put the waveforms from both models in the same drawing. The results from average model are close to the switching model, or are located in the middle of the results from switching model.

Based on those simulation results, the average model developed in previous section can correctly and exactly represent the DC operation of the circuit.

6.4.2 Verification of AC analysis by SIMPLIS

SIMPLIS (SIMulation for Piecewise-LInear System) is a simulation package especially for switching power supplies. By using simplified piecewise-linear to represent

the non-linear feature of typical switching components, such as MOSFET and diode etc, SIMPLIS can perform the simulation faster than SPICE based simulation tools. One of the special and useful features of SIMPLIS is its SIMPLIS-FX analysis function. SIMPLIS-FX is a special small signal analysis tool that can free you from developing average model for switching power supplies. By adding a small perturbation directly to steady-state circuit and calculating the response, SIMPLIS-FX can obtain the small signal frequency-domain characteristics from time domain analysis. Once the time domain model (switching model) is developed, it can perform time domain (steady state and transient) and frequency domain (small signal AC) analysis. So it can be used to analyze the frequency characteristics of any kind of switching topologies under any operation condition. And its accuracy is within 0.5dB and 1 degree.

As discussed above, the operation of the non-flyback converter is complicated due to too many operation modes. In order to obtain the unified average model, every mode operation has to be considered. But the special feature of SIMPLIS can avoid this trouble by directly performing small signal AC analysis on the switching model. In this section, SIMPLIS is implemented to verify the result from the average model of non-ideal flyback circuit developed in last section.

Figure 6-14 shows the schematic drawing of flyback circuit in SIMPLIS. Simple switch model and piecewise linear resistor model are used to replace the actual MOSFET and diode. By setting the ON-resistance to be very low and OFF-resistance very high, those components represent the ideal switching characteristics of MOSFET and diode.

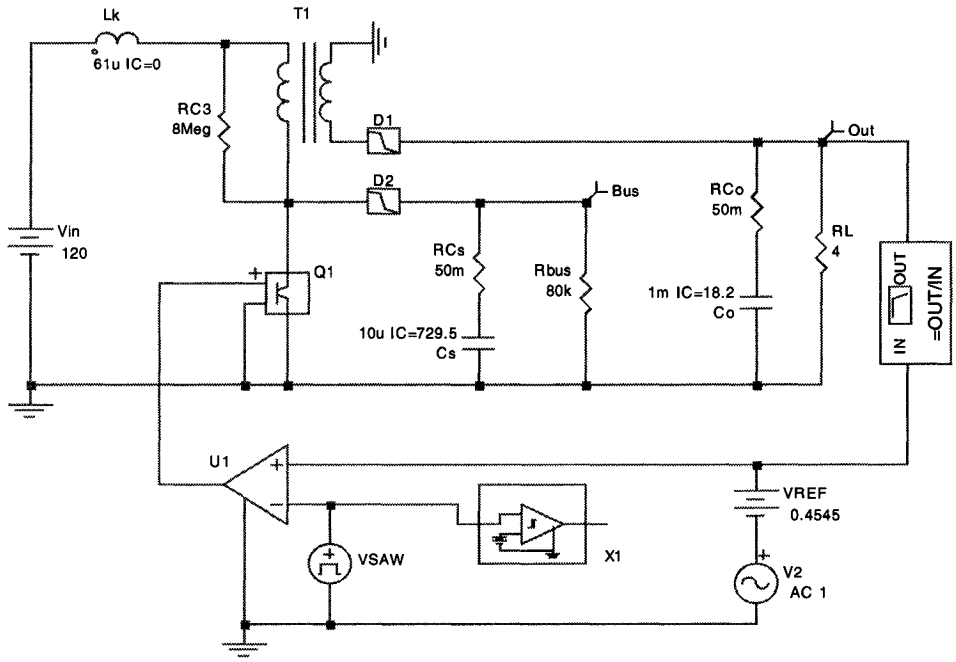
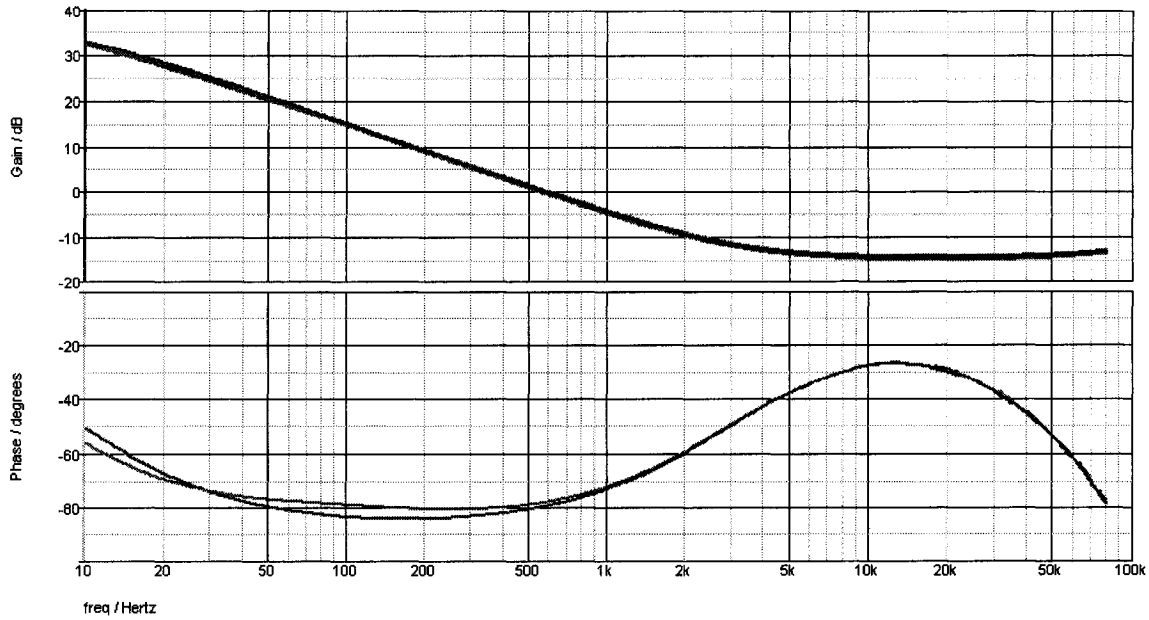


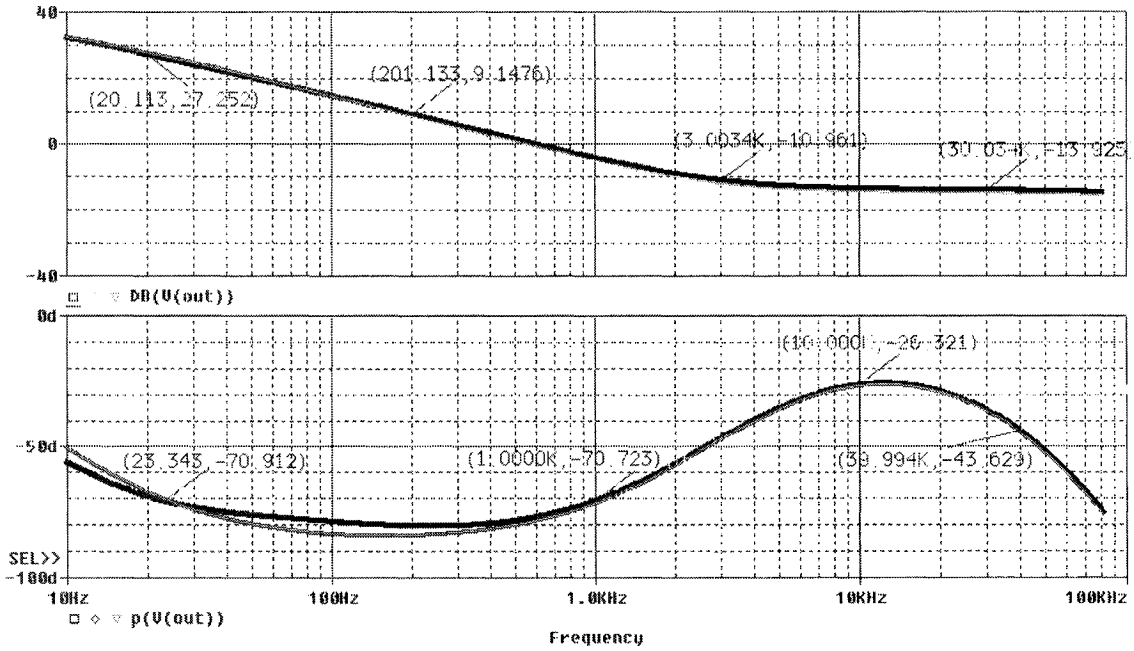
Fig. 6-14 Simulation circuit for non-ideal flyback by SIMPLIS

The small signal AC analysis results from average Pspice model developed in last section and switching SIMPLIS model are shown in Fig. 6-15, 6-16 and 6-17. The AC small signal analysis results are shown in Fig. 6-15 for flyback DCM+DCM operation. It clearly shows that the leakage inductor will not affect the AC gain and phase of the non-ideal flyback converter. But it will affect the DC gain of the converter, since some input power is transferred to snubber circuit by the leakage inductor.

Figure 6-16 shows the results for flyback CCM+DCM operation. The leakage inductor works like damping resistor to the flyback converter. The higher leakage inductance, the lower Q value of the converter. And Fig. 6-17 shows results for CCM Boost mode. The results from Pspice average model and SIMPLIS switching model correspond very well to each other, which mean the average Pspice model is correct.

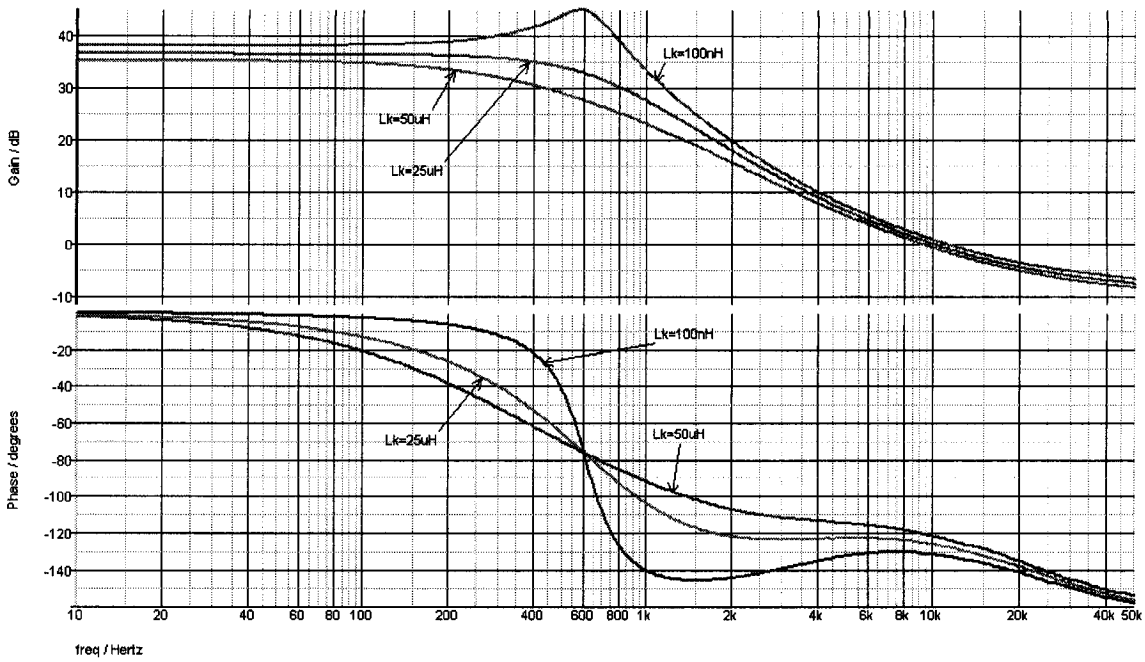


(a) SIMPLIS simulation results

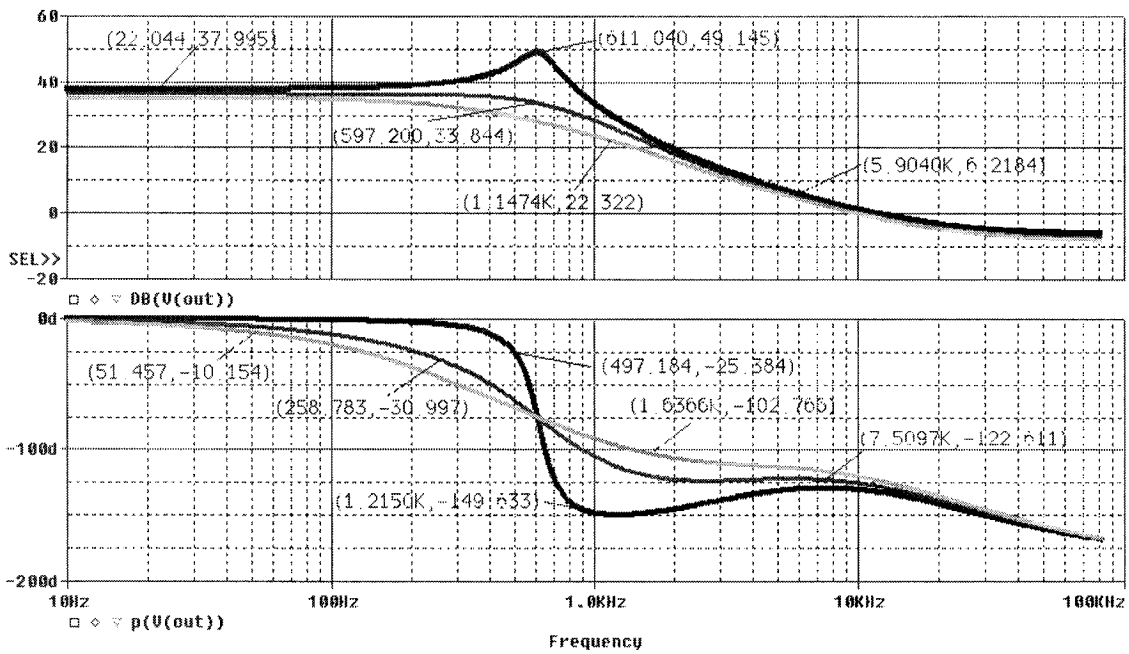


(b) Average model simulation results

Fig. 6-15 Simulation results comparison for Flyback DCM+DCM operation with RL=40 ohm, Rbus=80k, D=0.245, and Lk=100nH, 25uH, 50uH respectively

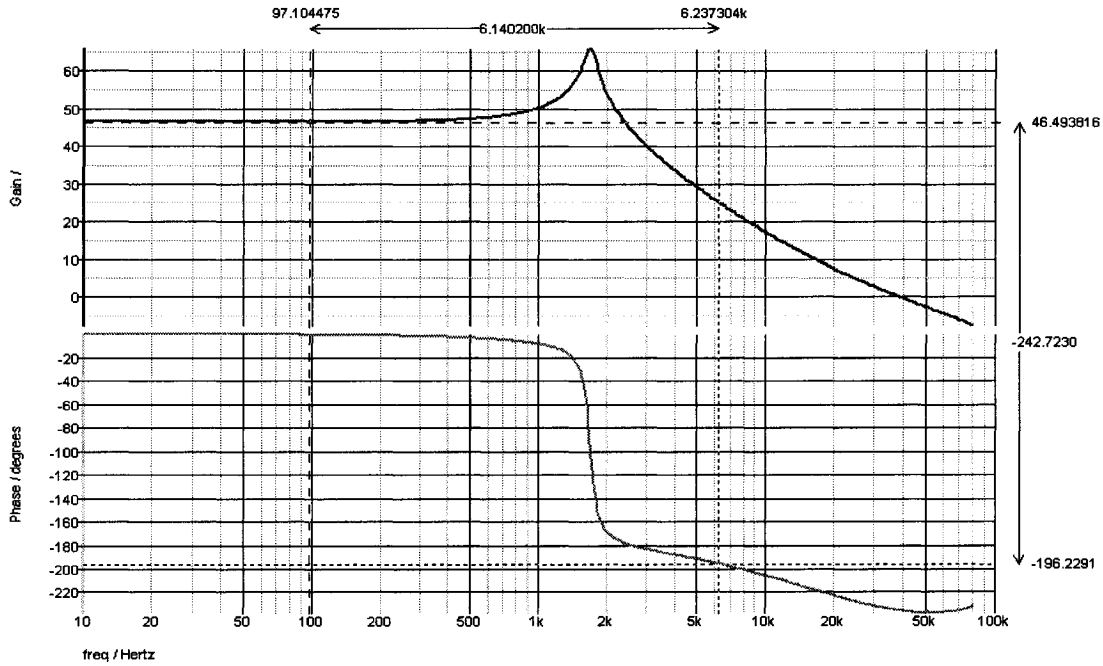


(a) SIMPLIS simulation results

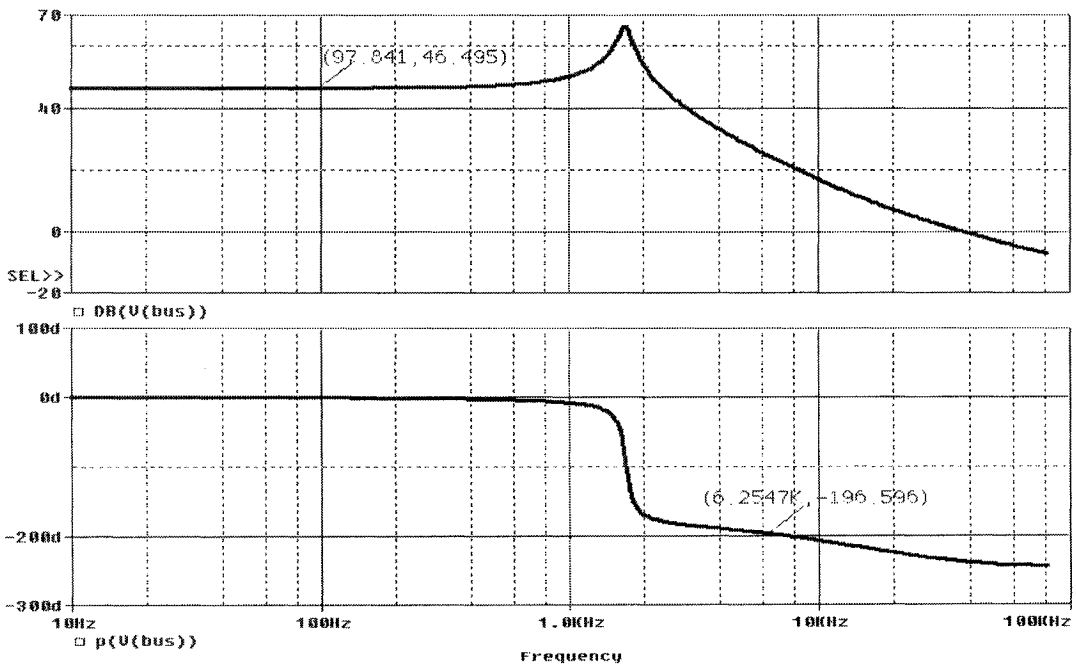


(b) Average model simulation results

Fig. 6-16 Simulation results comparison for Flyback CCM+DCM operation with RL=4 ohm, Rbus=80k, D=0.45, and Lk=100nH, 25uH, 50uH respectively



(a) SIMPLIS simulation results



(b) Average model simulation results

Fig. 6-17 Simulation results comparison for Boost CCM+CCM operation with RL=4Meg, Rbus=100 ohm, D=0.245 and Lk=1uH

6.5 Average model for Flyboost-parallel/series forward single stage PFC converter

The flyboost PFC cell, discussed in chapter 2, is actually a flyback circuit with special boost operation period. Depending on the instantaneous voltage, it works like flyback in some interval and like boost in other interval during one line period.

The non-ideal flyback model developed above includes all possible operation modes of the flyback circuit. So it can be implemented here to develop the average model for flyboost-derived single stage PFC converter.

In this section, the average model of flyboost – parallel/series forward single stage PFC converter, shown in Fig. 3-2, will be developed based the non-ideal flyback model.

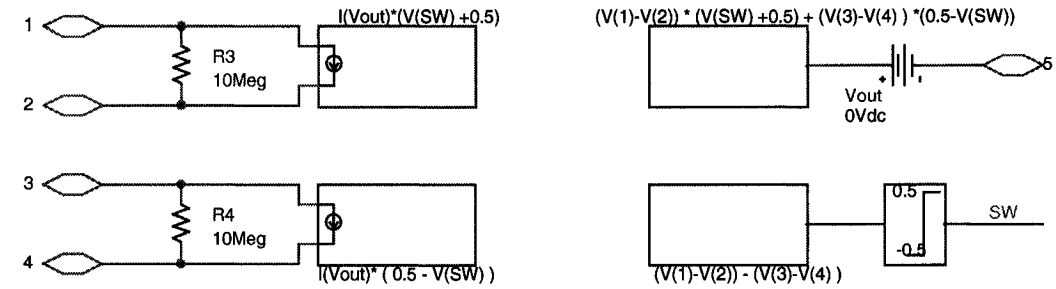
6.5.1 Derivation of the average model

The flyboost – parallel/series forward single stage PFC converter consists of two parts: flyboost cell and parallel/series forward cell. Although those two parts share one switch, their operations are independent. So this topology can be separated to two simple circuits: flyboost and parallel/series forward. The flyboost cell can be represented by the non-ideal flyback model. The parallel/series forward circuit is a special forward circuit. It can be represented by one special parallel-series transformer model and one ideal forward model. Once all models are ready, the final model can be obtained by connecting them together according to the original circuit connection.

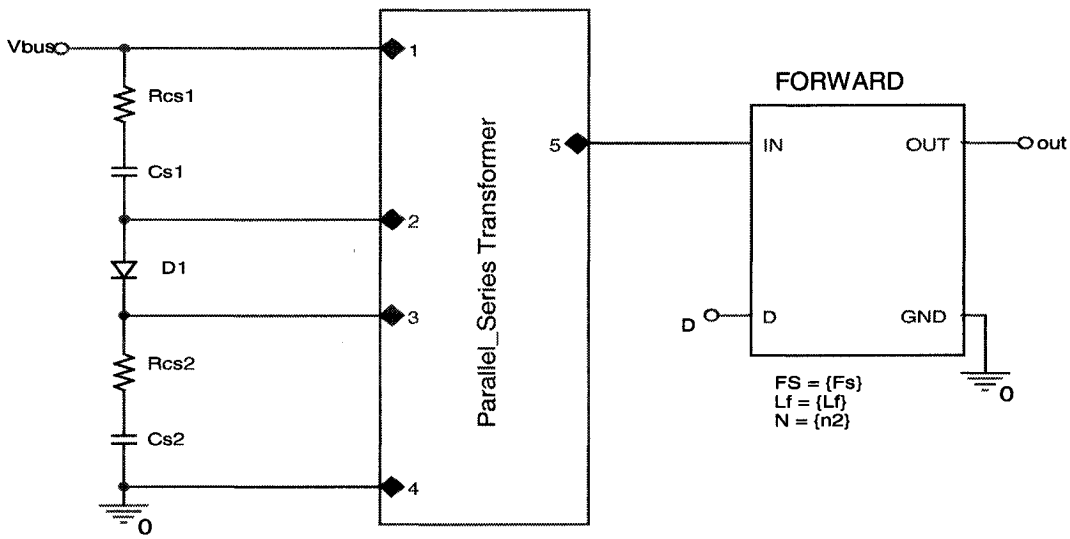
The non-ideal flyback model and ideal forward model are already available. Only the special parallel-series transformer model is needed to develop. Based on the operation analysis in Chapter 3, the parallel/series forward circuit will discharge the bus capacitors

in parallel during ON period, while the capacitor with higher voltage will provide the power to output. During OFF period, the forward transformer magnetizing current and current from flyboost circuit will charge two capacitors in series. The parallel-series transformer will carry out the function. According its function, it can be modeled by ABM (Analog Behavior Model) components like in Fig. 6-18(a). To simplify the operation, we assume that both capacitors will provide current to output when the voltage difference of those capacitors is less than 0.5V. This assumption will replace the non-linear switching characteristics of this circuit by linear transition feature. It will improve the convergence issue during simulation, while still keeping the high accuracy.

Integrating this parallel-series transformer model with capacitors and conventional forward converter model, the parallel/series forward circuit model is shown in Fig. 6-18(b). The diode D1 between two intermediate bus capacitors represents the diode voltage drop in switching model. It can be removed to simply this circuit. Based the schematic drawing in Fig. 3-2, the final model for this single stage PFC converter can be obtained by integrating the model in Fig. 6-9 and Fig. 6-18, as shown in Fig. 6-19. The output of the ABS block is the absolute value of the input signal. It is used to represent the input rectifier in the actual circuit. In order to keep constant output voltage, the duty cycle need to change in one line period. So close loop control is necessary for the analysis. The OP_AMP U4 circuit in the bottom represents for the compensation circuit to close the loop.



(a) Parallel-series transformer model



(b) Final model of parallel-series forward converter

Fig. 6-18 Average model for parallel/series forward converter

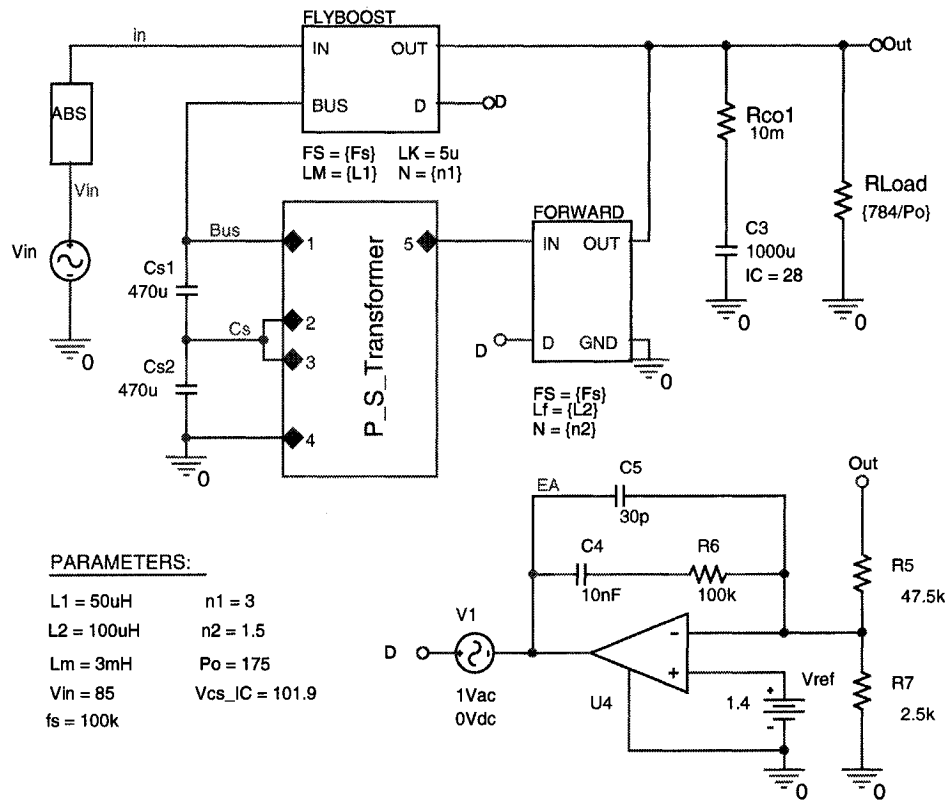


Fig. 6-19 Average model of flyboost-parallel/series forward PFC converter

6.5.2 DC operation analysis by the average model

One benefit of the average model is the reduced simulation time. In switching model, the simulation has to calculate several points in each switching period. For PFC circuit, the switching frequency is much higher than the input line frequency. And the simulation for many line frequency cycles is necessary to find steady state operation point. So it will make the simulation a very time-consuming procedure. By removing the switching characteristics, the average model does not need to simulate the switching cycle operation. So it speeds the simulation procedure. In this section, both switching and average models are implemented to perform the DC analysis of the flyboost -

parallel/series forward PFC converter. The simulation results are compared to verify the correctness of the average model.

The switching model of the converter is shown in Fig. 6-20, based on the schematic drawing in Fig. 3-2. All values are set to the same as in the average model in Fig. 6-19.

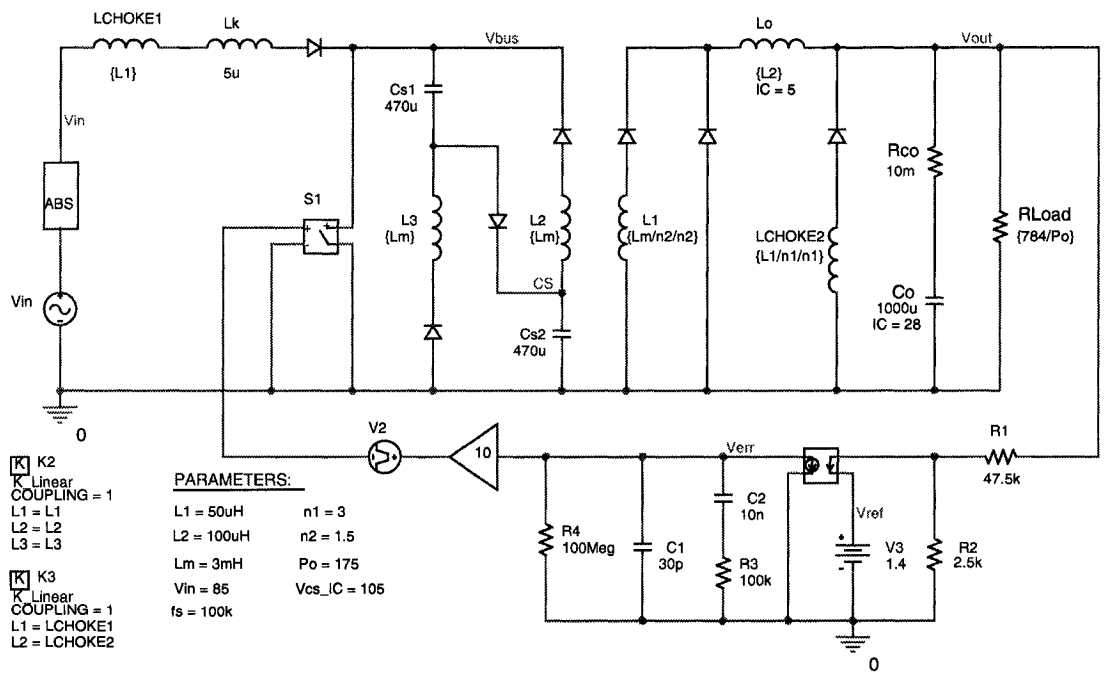
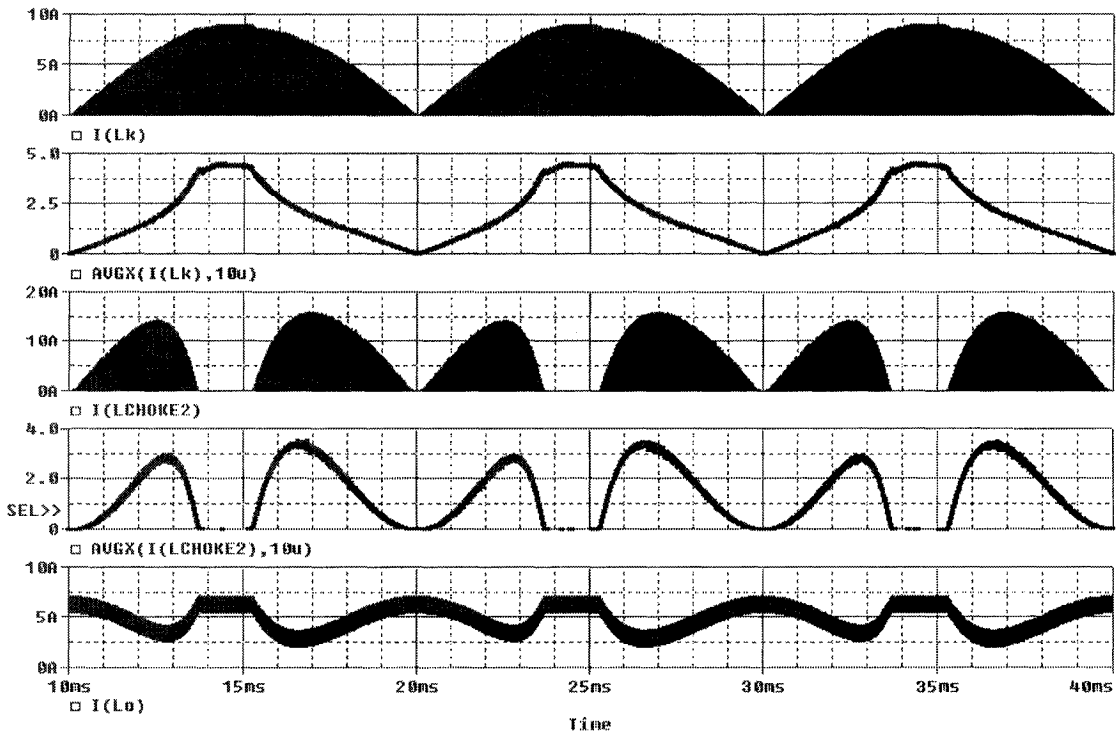
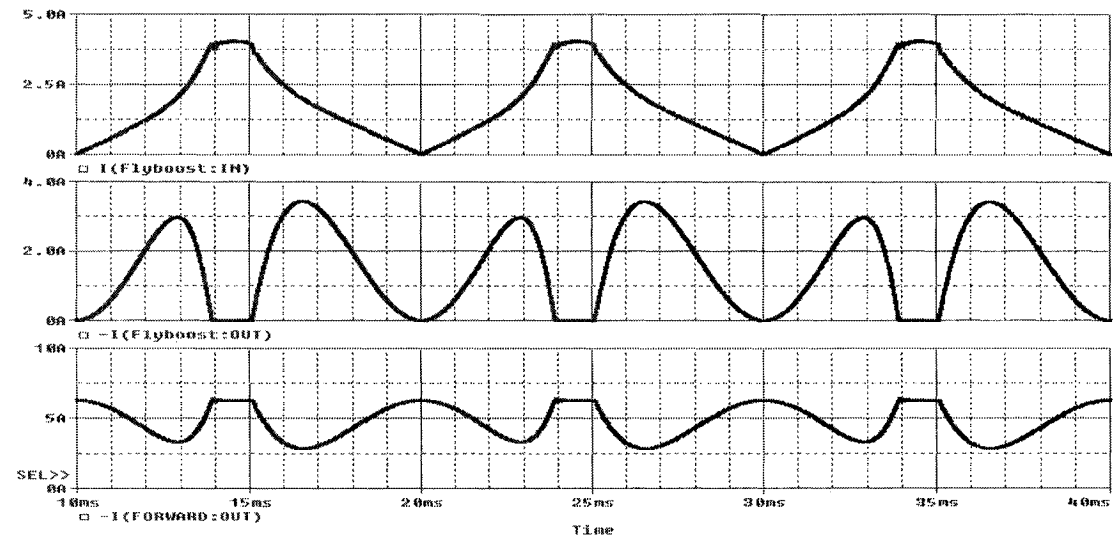


Fig. 6-20 Switching model of flyboost-parallel/series forward PFC converter

The simulation results are shown in Fig. 6-21. Avgx function is used to obtain the average waveforms from switching model results. The results from switching model and average model correspond each other very well, which verify the correctness of the model.



(a) Simulation results by switching model



(b) Simulation results from average model

Fig. 6-20 Comparison of simulation results from average and switching model

6.5.3 AC analysis by the average model

One important application of the average model is to perform AC small signal analysis. This analysis can figure out the transfer function and provide guide for compensation circuit design. But the flyboost derived single stage PFC converter is different form other kind of topologies due to its direct power transfer or parallel power transfer feature. This special feature brings lots of advantage, and also increases the difficulty of analysis.

For typical topologies, there is only one steady state operation mode for the given circuit parameters and operational condition. It means that the operational values, such as duty cycle and inductor current, are constant once the circuit reaches its steady state condition. For typical PFC converter, including two-stage and single-stage, the input current is sinusoidal waveform and keeps changing according to instantaneous input voltage. The average modeling is not a good method for AC analysis. For typical single stage PFC converter, the operation of PFC cell is totally independent of the operation of DC-DC cell. The operational parameters of DC-DC conversion cell will maintain almost constant for the whole line period. So the average model can be developed over the line frequency.

But for flyboost-derived single stage PFC converter, there are two different operation modes (flyback mode and boost mode) in one line cycle. The input current keeps changing to achieve high power factor like other typical single stage PFC converter. And there is some input power that is directly transferred to the output end through flyboost cell. The current from flyboost cell to output follows the change of

instantaneous input voltage. And the current provided by DC-DC cell has to change also to keep constant output voltage, as shown in Fig. 6-21. And there is not direct transferred power under boost operational mode. The effective operation circuit configuration also changes for different operational modes. As discussed in previous chapter, the diode in the flyboost secondary side will not conduct under boost mode. For some topologies, such as Bi-flyback converter, the duty cycle also keeps changing in one line period to achieve constant output voltage.

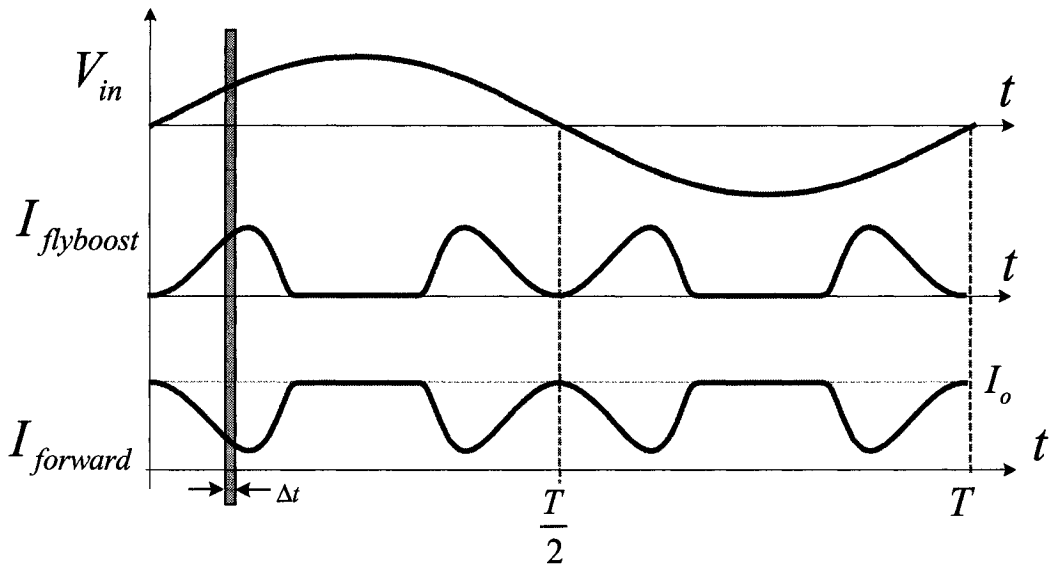


Fig. 6-21 Operational waveform in one line cycle

So, there is not steady state condition for line period. It means that the average model over line cycle is not practical for this kind of topologies. So the average model should not be based on the line period like other typical single stage PFC converter. But it is possible to obtain the average model over the switching period.

In flyboost-derived single stage PFC converter, the control loop should respond very fast to adjust the duty cycle to maintain the constant output. It also means that the bandwidth of the control loop should be much higher than the line frequency. Now let us discuss on the one short time interval, such as Δt in Fig. 6-21. Assume that Δt is much longer than the switching period, and much shorter than the line period. This assumption is reasonable, since the switching frequency is normally over 50kHz, while the line frequency is 50 or 60Hz. During this short time interval, we can assume that the input voltage is constant. Because the controller bandwidth is very high, the circuit will reach and maintain steady state condition during this short interval. So we can use DC voltage source to replace the AC input voltage. Then the circuit becomes one equivalent DC-DC converter. We can consider the operation mode, circuit configuration, and operation parameters will be unchanging during this interval. The average modeling method can be applied to this equivalent DC-DC converter.

Based on the above assumption, we can obtain the average model for each short time interval by replacing the AC input voltage source by one equivalent DC voltage source. Because the operation mode is different for different intervals in one line cycle, the average model should be able to automatically choose the correct operation mode (or operational circuit configuration) for that interval. So one unified model is required. Once this unified model is developed, AC small signal analysis can be performed for each interval.

Due to its symmetric characteristics, only quarter of line period is necessary to be analyzed for flyboost-derived PFC converter. By performing a series of AC small signal analysis in that quarter line period, a series of transfer functions of the converter are

available. Those transfer functions represent the converter characteristics during different interval in one line cycle. Those results can be used for controller design. For actual compensation circuit design, the transfer function under the worst case should be considered for optimal performance with enough phase margins.

The average model for non-ideal flyback converter developed in last section works for all possible operation modes. This model can choose the proper mode according to its terminal voltages. It meets the requirement of automatic mode transition. So the average model developed in last section can be used to perform AC small signal analysis for each short time interval. The model will be the same as the model in Fig. 6-19, except that the sinusoidal input voltage source is replaced by DC voltage source. The DC voltage source represents the specific instantaneous input voltage at that specific interval.

For comparison purpose, the transfer function of parallel/series forward DC-DC converter is shown in Fig. 6-22. By removing the flyboost circuit and input rectifier circuit in Fig. 6-19, the average model of parallel/series forward DC-DC converter is ready for analysis. Two different bus capacitor values, 100uF and 100F respectively, are used to study the influence of the capacitance. When Cs=100F, the capacitor operates like voltage source. From the simulation results in Fig. 6-22, we find that the capacitor really affects the transfer function by changing the double pole frequency and phase at low frequency.

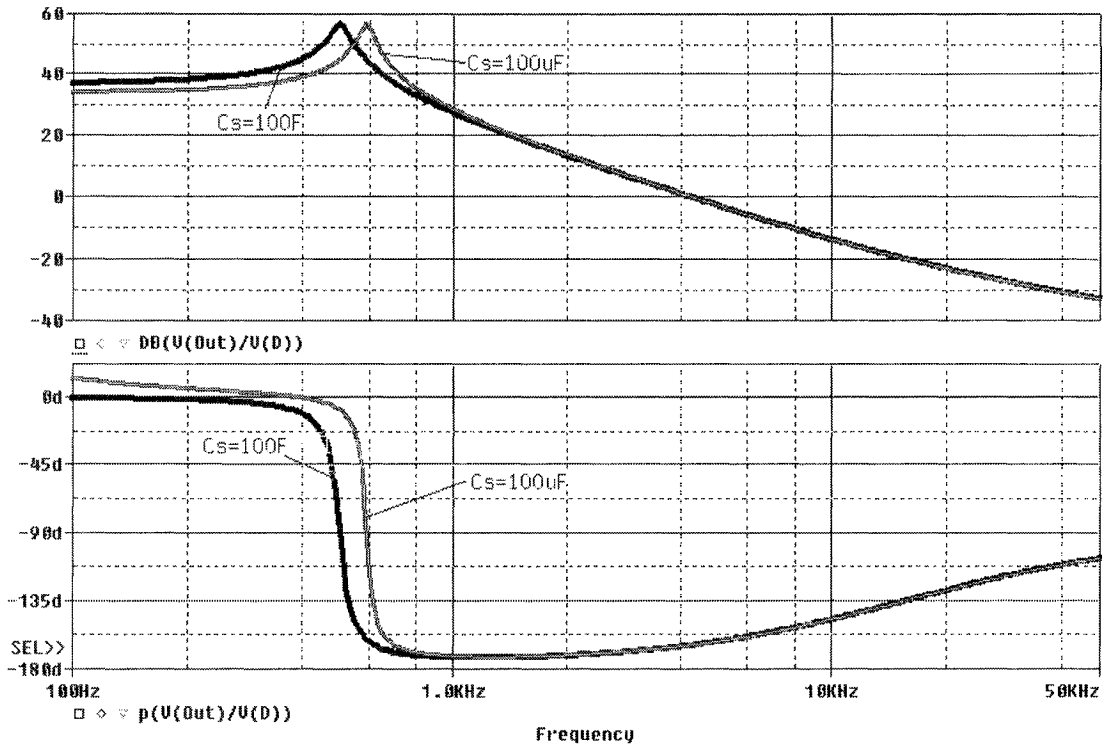


Fig. 6-22 Transfer function of Parallel-series forward with different capacitor

One simulation result for the flyboost-parallel/series forward PFC converter, with zero input voltage and bus capacitance equal to 100uF, is also included in Fig. 6-22. This result is overlaid with the result of the DC-DC converter with 100uF bus capacitor. This meets our expectation, since flyboost-parallel/series forward PFC converter should operate exactly like the corresponding parallel/series forward DC-DC converter, when input voltage is zero and flyboost PFC circuit does not affect the operation.

AC small signal analysis is to analyze the frequency response of one system that is perturbed by one small AC signal around its steady state operation point. In OrCAD Pspice simulation, the bias point analysis is to find the steady state operation point of the circuit. Then AC analysis is performed to find the frequency response.

Because of the automatically mode transition feature of this average model, there are lots of non-linear ABM components, such as comparators and "IF" function. Those non-linear components make it very difficult to find the solution for the bias point analysis. It is referred to convergence trouble. It happens frequently for simulation.

Fortunately, OrCAD provides the initial condition setting and save/load bias point function. The initial condition (IC) setting function can set the node voltage or inductor current to a specific value. The save bias point function can save the simulation data of the transient analysis. And the load bias point function can use the saved bias point file for a new simulation.

For DC transient analysis, there are a few chances to meet convergence trouble. So it provides one solution to the convergence trouble under AC analysis. The following simulation procedure can be used to perform AC analysis:

a. Perform DC transient analysis on the average model in Fig. 6-19, and record the intermediate bus voltage at different instantaneous input voltage;
b. Replaced the AC input voltage, Vin in Fig. 6-19, by one DC voltage source with its voltage equal to the input voltage at the interested interval;
c. Change the capacitance of the intermediate bus capacitors, Cs1 and Cs2, to very high value, such as 1000F; And use the recorded bus voltage as its initial condition value;
d. Perform DC transient analysis on this circuit, and save the final steady state simulation data into a bias point file;
e. Open the saved bias point file, and change ".NODESET" to ".IC";

f. Change the capacitance of the intermediate bus capacitors, Cs1 and Cs2, back to its original value;

g. Perform the AC analysis with loading the saved bias point file.

During DC transient analysis at step a and d, the bias point calculation need to be bypassed by choosing the "skip the initial transient bias point calculation" in the simulation setting to avoid convergence problem. By changing the capacitance to very high in step c, which means it works like constant voltage source, the bus voltage can be kept almost unchanged during the DC transient analysis in step d. So the final steady state results can be found for the specific bus voltage. And ".NODESET" command line in the saved bias point file will let Pspice use the bias point file data as the guess value to calculate the new bias point. The ".IC" command line will let Pspice use the bias point file data as the new bias point for the AC analysis. The convergence trouble can be avoided effectively by step e.

By repeating the above procedure with different input voltage, the transfer function of the converter at different interval in one line period can be obtained. One example is shown in Fig. 6-23 for the circuit parameters shown in Fig. 6-19. The transfer function is calculated for different interval at 0, T/24, T/12, T/8, T/6, 5T/24, T/4 respectively (T: line period). The worse case of phase delay happens at t=0, 5T/24 and T/4. At t=0, the circuit is one parallel/series forward DC-DC converter with flyboost out of work. When t=5T/24 and T/4, the circuit is under boost mode. Under boost mode, there is no direct power transferred to output directly. There is only parallel/series forward cell that provide current to output. For controller, the circuit under boost mode is

similar to parallel/series forward converter. So their transfer functions are close to each, as illustrated in Fig. 6-23.

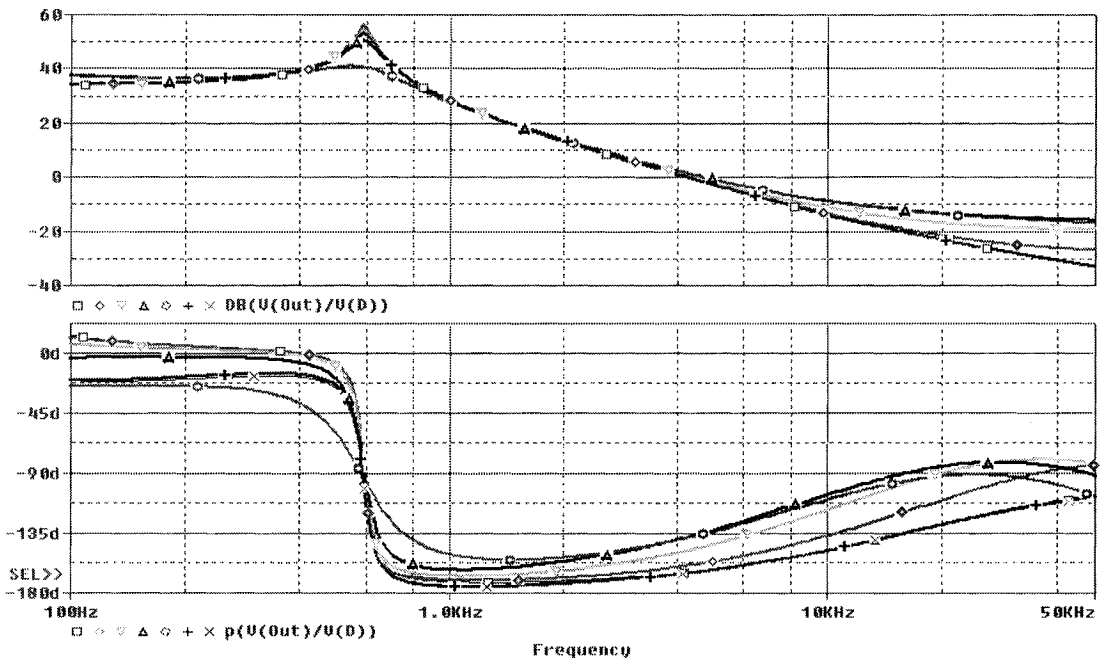


Fig. 6-23 Transfer function of flyboost- Parallel/series forward PFC converter at different interval in one line period

For the compensation circuit design, the optimal parameters should be able to guarantee that there are enough phase margins for all cases. It is not easy to analyze and design since the transfer function is not constant at different interval in one line period. As mentioned above, the worse case happens at t=0 when the circuit operates like the equivalent parallel/series forward DC-DC converter. So if the compensation circuit parameter can provide enough phase margin for equivalent DC-DC converter, the phase margin for the PFC converter should be enough. So the compensation design of PFC converter can be simplified to the compensation design of equivalent DC-DC converter.

6.6 Average model for Bi-flyback single stage PFC converter

In last section, the average model of flyboost-parallel/series forward PFC converter is developed. The simulation results show that its AC small signal characteristics depend mainly on the parallel/series DC-DC circuit. It is because that the DC-DC circuit provides most of the output power, while PFC circuit directly transfers some input power only in some period in one line cycle. The operation of Bi-flyback single stage PFC converter in Chapter 4 is different because the flyboost PFC cell provide most of the output power and direct power transfer happens in the whole line cycle. So its AC small signal characteristics should be different to its corresponding DC-DC circuit. In this section, the average model of Bi-flyback PFC converter is developed and studies.

6.6.1 Derivation of the average model

The Bi-flyback single stage PFC converter consists of two flyback circuits, as shown in Fig. 4-2. Under flyback mode, two circuits operate independently. Under boost mode, those two flyback circuits' operation is interweaved with each other: the PFC cell current flows through the primary winding of DC-DC cell transformer and is reflected to output. We can build one model based on the operation of the complete Bi-flyback circuit. But it is time-consuming. Since we already have flyboost PFC cell and conventional flyback converter, it will be easy to build the average model based on those basic models available.

By carefully studying the operation of Bi-flyback converter under Boost mode, we found that the DC-DC cell works like one transformer for PFC cell. So we can use one ideal transformer with the same turn ratio as the DC-DC cell transformer to represent the function of the DC-DC cell under boost mode. By this way, the operation of two flyback circuits is separate now, and the average model of Bi-flyback converter can be developed easily from basic models.

The final average model is shown in Fig. 6-24. The ideal transformer T1 consists of voltage-control-voltage source and current-control-current to represent ideal transformer function. The turn ratio of T1 is equal to the turn ratio of DC-DC flyback circuit. And compensation circuit is included for close loop analysis.

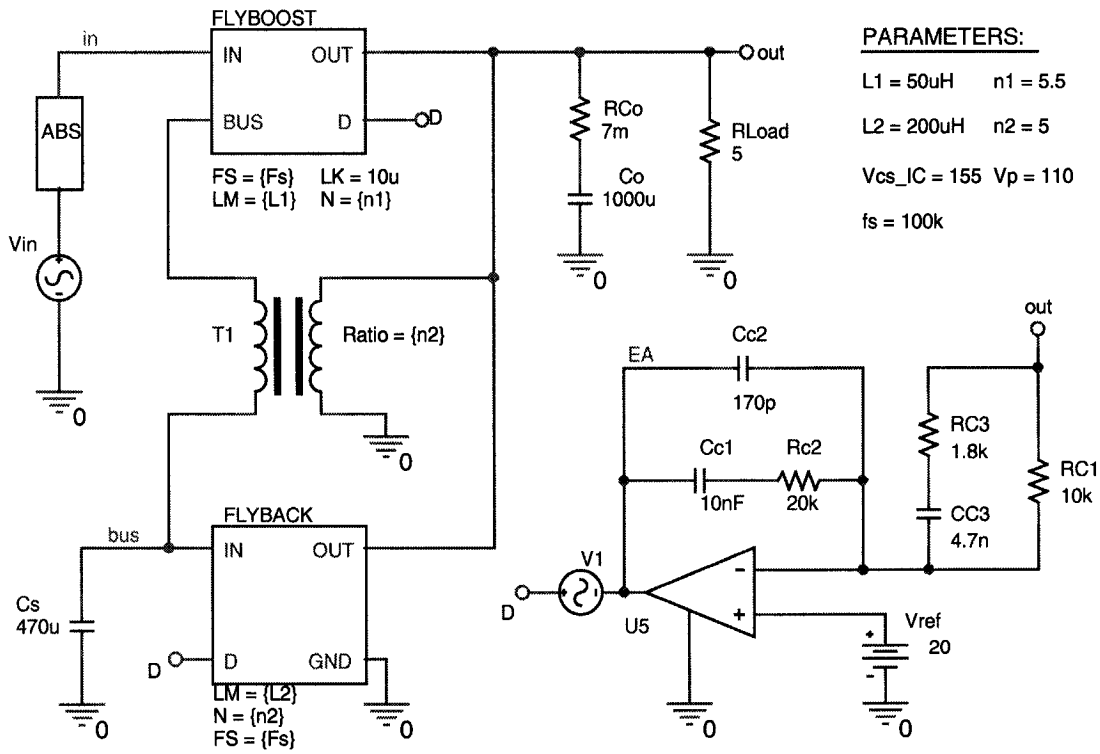


Fig. 6-24 Average model for Bi-flyback PFC converter

6.6.2 DC operation analysis by the average model

In this section, both switching and average models of Bi-flyback PFC converter are used to perform the DC analysis, and the simulation results are compared to verify the correctness of the average model.

Based on the topology in Fig. 4-2, the switching model of Bi-flyback converter is shown in Fig. 6-25, with the same parameters as the average model in Fig. 6-24. The current-control-current source F1 represents the function of ideal error-amplifier. The circuit at the bottom represents the function of the compensator and PWM modulator.

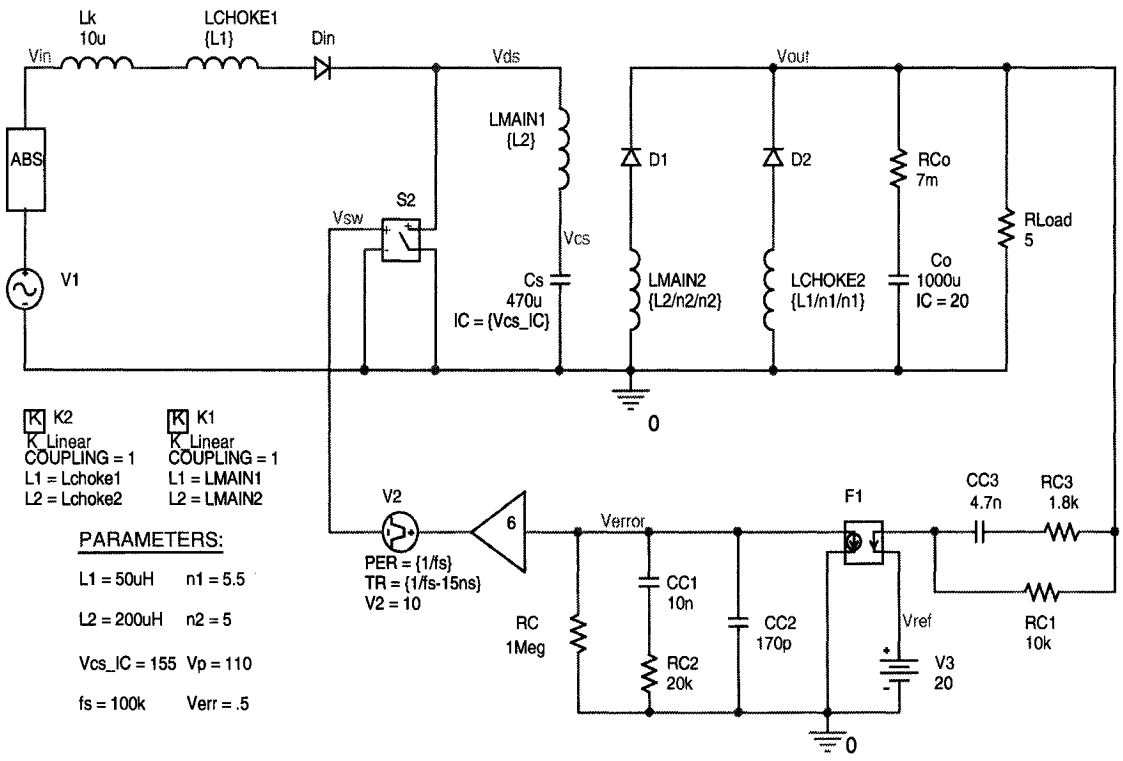
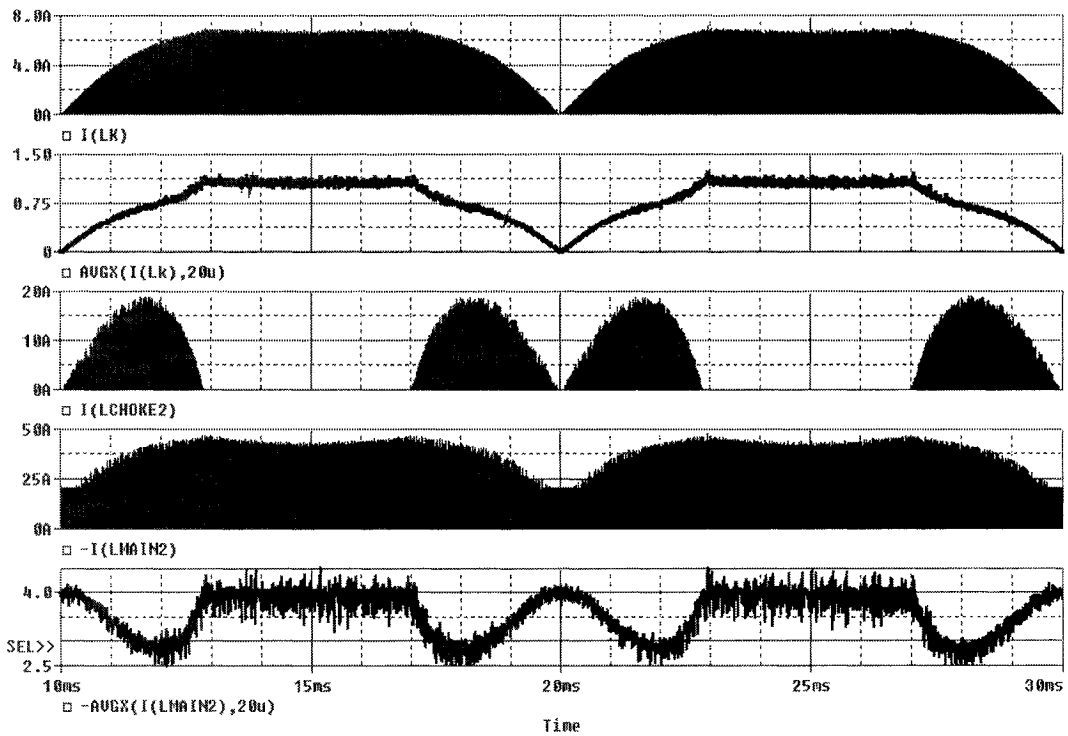
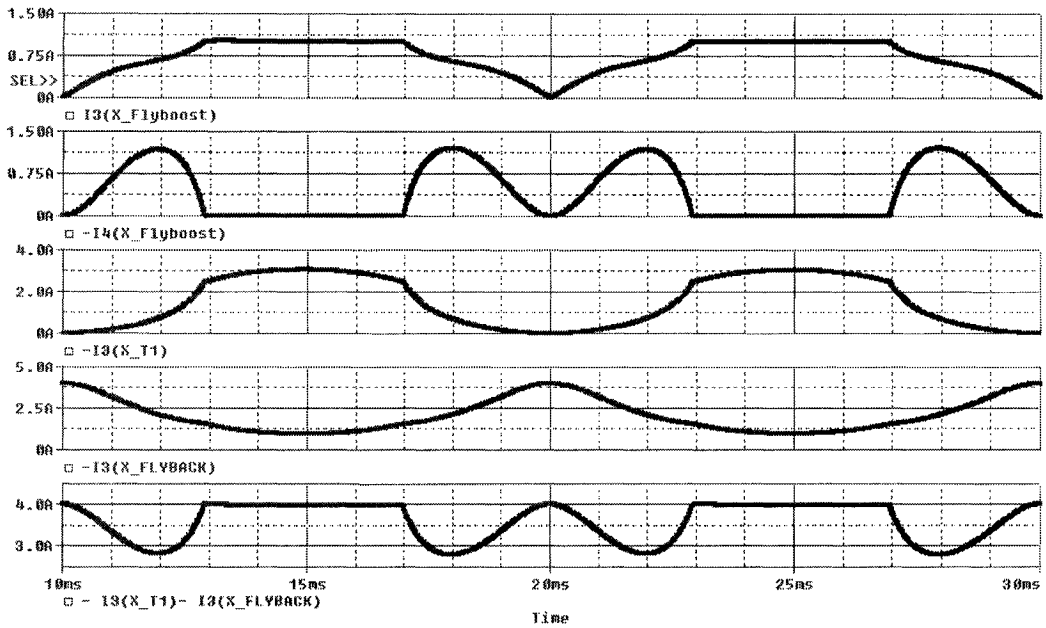


Fig. 6-25 Switching model of Bi-flyback PFC converter

The simulation results from both models are shown in Fig. 6-26. For comparison purpose, the Avgx function is used to obtain the average waveforms from switching model results. There Because of DCM operation, the current waveform changes in wide range. There still exist noise after averaging by the Avgx function. But its trend of the waveform is clear. From those simulation results, it is clear that the switching model and average model correspond each other very well, which verify the correctness of the average model.



(a) Simulation results by switching model



(b) Simulation results from average model

Fig. 6-26 Comparison of simulation results from average and switching model

6.6.3 AC analysis by the average model

The simulation procedure in last section needs for the AC analysis simulation of Bi-flyback converter. For comparison reason, one switching model is built in SIMPLIS to perform AC analysis also, as shown in Fig. 6-27. In SIMPLIS model, the input AC voltage source and intermediate bus capacitor are replaced by DC voltage source. It will bring some difference comparing to the Pspice average model with the actual bus capacitor.

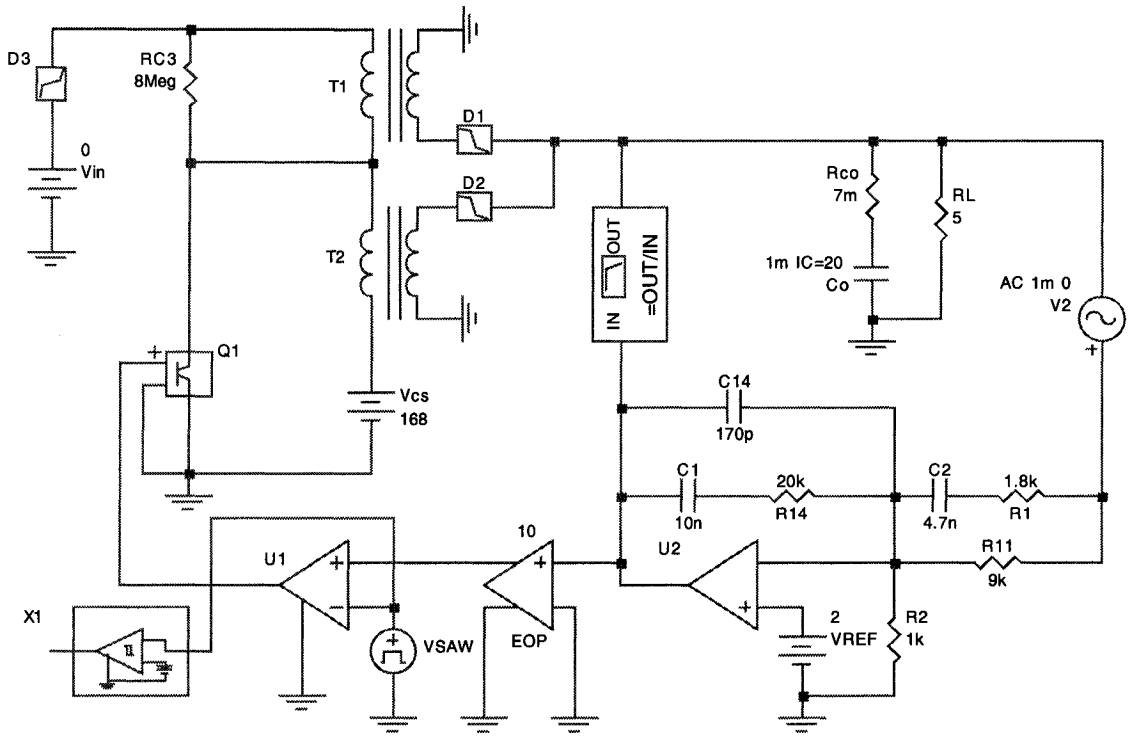
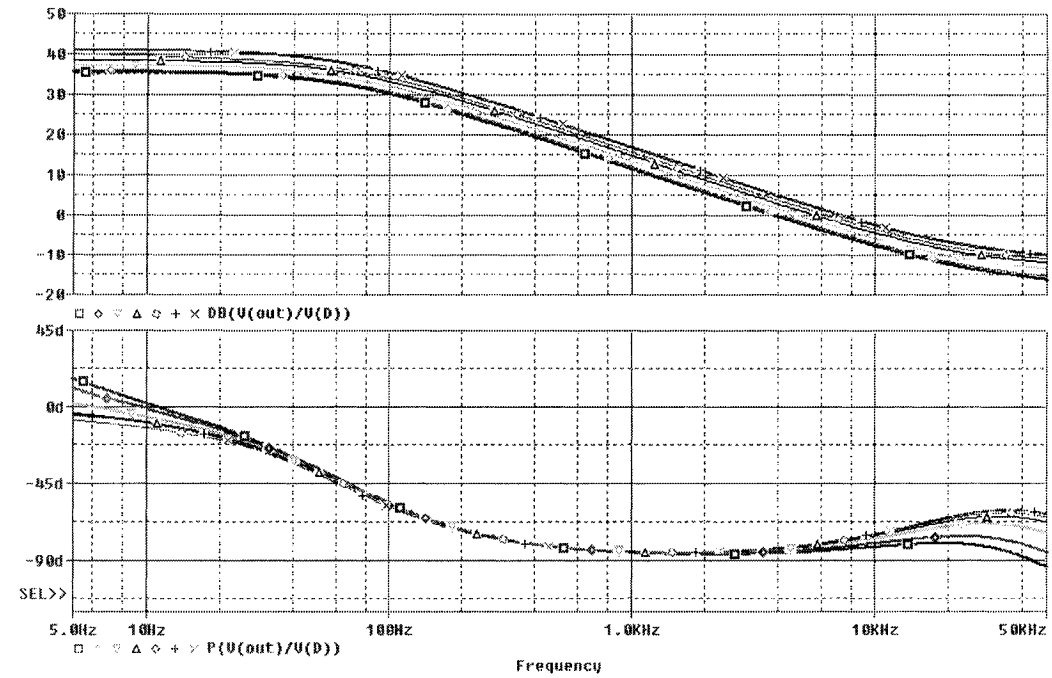
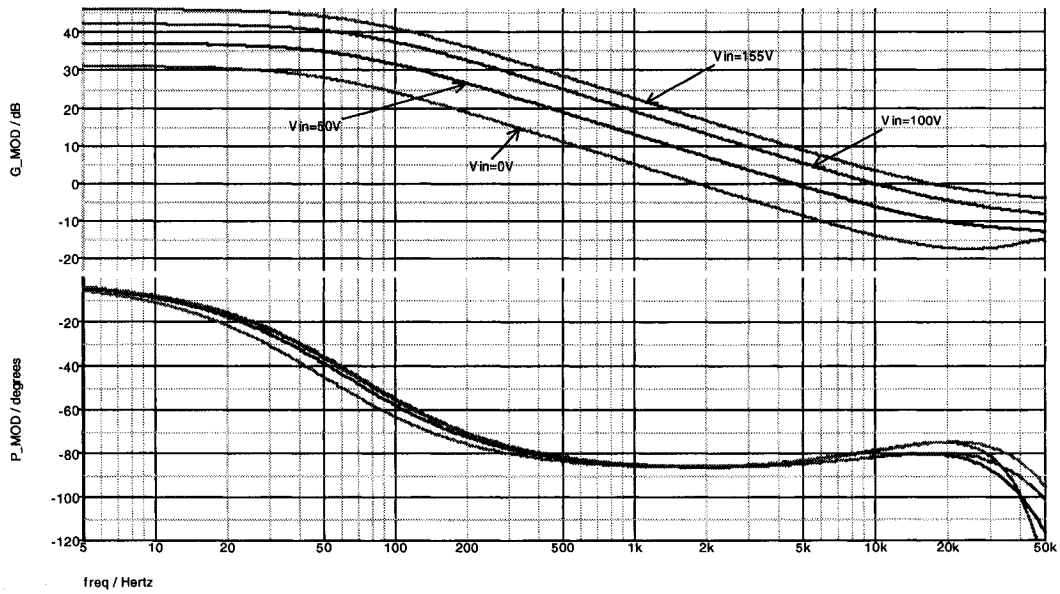


Fig. 6-27 SIMPLIS model of Bi-flyback PFC converter

The simulation results are shown in Fig. 6-28. And the results from both models are close to each other, which mean that the average model of Bi-flyback converter is correct. As shown in the results, the gain of the transfer function is changed at different intervals during one line cycle. The maximum gain happens when the input voltage reaches its peak value. The phase is almost the same for different intervals. During compensation design, the gain variation needs to be considered.



(a) Simulation results from Pspice average model



(b) Simulation results from SIMPLIS model

Fig. 6-28 Transfer function of Bi-flyback PFC converter

6.7 Summary

The operation of non-ideal flyback circuit is complex because of the leakage inductance of the transformer. Based detailed operation analysis, one unified average model was developed for non-ideal flyback circuit. It also works for flyboost PFC circuit. Based on this model, the average model for flyboost derived single stage PFC converter can be developed. Two examples were included in this chapter. The simulation results of those average models were verified by SIMPLIS switching models.

CHAPTER 7

CONCLUSION

In the pass decade, lots of single stage PFC topologies were proposed for low cost applications. In typical single stage PFC converter, the input power is converted to high bus voltage and stored in intermediate bus capacitors by PFC cell, and all output power is provided by DC-DC conversion cell from intermediate bus capacitors. Since there is only one stage, the active switch have to handle the PFC current and DC-DC current at the same time. And the input power is proceeded twice by the active switch. So the current stresses on the active switch is very high. Because there is not active control method for the intermediate bus capacitor, which is controlled only by the circuit parameters, most of single stage schemes suffer from higher voltage stresses. The high voltage and current stresses put higher requirement on the selection of the power stage components and reduce the conversion efficiency, which make most of single stage PFC schemes incompetent for practical applications.

In this dissertation, one direct power transfer PFC cell, flyboost PFC cell, was discussed in detail in Chapter 2. This special PFC cell can transfer some input power to output end directly. The DC-DC conversion cell only needs to provide portion of output power. So the total proceeded power by the active switch is reduced. And this special

PFC cell can also automatically limit the maximum intermediate bus voltage. So this scheme can reduce the voltage and current stresses on the power stage components, resulting in better performance. The operation and feature of Flyboost PFC cell was discussed in Chapter 2 with one simple example.

Based on flyboost PFC cell, two single stage PFC topologies were discussed in Chapter 3 and 4 respectively. In Chapter 3, one single stage PFC topology, integrated the flyboost PFC cell with parallel/series forward DC-DC cell, was studies in detail. With only one active switch, this topology can achieve about 82% efficiency for universal input applications. Special circuit configuration also prevents voltage spike over the active switch when it is turned off. This topology is suitable for 100-200W universal applications.

Bi-flyback in Chapter 4 is one simple single stage PFC converter with more advantage over other schemes. By combining two flyback circuits together, Bi-flyback topology can transfer more power directly to output with little distortion on the input current waveform. The intermediate bus voltage is kept just a little higher than the input peak value. For universal input application, the maximum bus voltage can be limited to less than 400VDC. So one 450VDC bulk capacitor can be used here to reduce the cost. And the voltage stress over the MOSFET is less than 520V, which make the popular 600V rating MOSFET suitable for this topology. So the total coat of this scheme is very low, making it one competent scheme for 75-150W universal applications.

The control approach for the single stage PFC converter is one challenge. The only one control loop needs to keep output voltage regulated and the average input current following the change of input voltage. In Chapter 5, the control scheme was

discussed in detail. Typical voltage mode and peak current mode control scheme can be implemented to those proposed single stage PFC topologies. Valley switching technique is one special soft-switching technique for flyback circuit. This idea is implemented to Bi-flyback for better performance.

In Chapter 6, the average model for flyboost PFC cell is developed for the AC small signal analysis. Based on detailed operational analysis of flyback circuit with leakage inductance, one unified average model was developed for non-ideal flyback converter. This model is also applicable to Flyboost PFC cell. Integrated this developed model with basic DC-DC conversion models, the average model of two flyboost-derived single stage PFC converters were developed for AC analysis. The AC small signal analysis shows some difference between the single stage PFC converter and its basic DC-DC converter. This model can be used for optimal control design.

In this dissertation, the flyboost PFC scheme is studied in detail with some experimental results. Two potential schemes, discussed in Chapter 3 and 4, have the potent for practical application due to their low cost and high performance. There are several issues that need to improve:

a. Optimal control scheme: In chapter 5, some control approaches were discussed and one soft switch approach was tested. But those control methods are optimal for DC-DC applications. For single stage PFC converter, there are some special characteristics that require the special control approach to achieve optimal performance.

b. Better snubber circuit for Bi-flyback: In practical application, snubber circuit is very important for Bi-flyback circuit, because there are two flyback

transformers. The active clamp circuit is the best solution with the price for higher cost and more components count. For low cost practical application, a good topology with simple solution is needed.

c. Hold-on time requirement: In order to meet hold-on time requirement, the intermediate bus capacitance should be high. For Bi-flyback scheme, the bus voltage is equal to the input peak voltage, which it is double the value for low line voltage in typical two-stage PFC scheme. One solution is needed to boost the bus voltage of Bi-flyback scheme at low line voltage.

LIST OF REFERENCES

[1] R. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in Proc. IEEE PESC, 1994, pp. 1137–1144.

[2] R. Redl and L. Balogh, "Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage," in Proc. IEEE APEC, 1995, pp. 454–458.

[3] J. Qian and F. C. Y. Lee, "A high-efficiency single-stage single-switch high-power-factor AC/DC converter with universal input," Power Electronics, IEEE Trans., July 1998, vol. 13, pp. 699–705.

[4] Watson, R.; Hua, G.C.; Lee, F.C., "Characterization of an active clamp flyback topology for power factor correction applications" Power Electronics, IEEE Trans., Jan. 1996, Vol.11, PP. 191-198.

[5] Huai Wei; Batarseh, I., "Comparison of basic converter topologies for power factor correction" in Proc. IEEE Southeastcon, 1998, pp: 348 -353

[6] Zhang, M. M. Jovanovic, and F. C. Lee, "Comparison between CCM single-stage and two-stage boost PFC converters," in Proc. IEEE APEC, 1999, pp. 335–341.

[7] Deng, E.; Cuk, S. "Single switch, unity power factor, lamp ballasts" in Proc. IEEE APEC, 1995. VOL. 2, pp. 670 -676

[8] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch power-factor-correction AC/DC converters with DC-bus voltage feedback for universal line applications," Power Electronics, IEEE Trans., Nov. 1998, vol. 13, pp.1079–1088.

[9] M. H. L. Chow, Y. S. Lee, and C. K. Tse, "Single-stage single-switch isolated PFC regulator with unity power factor, fast transient response and low voltage stress," in Proc. IEEE PESC, 1998, pp. 1422–1428.

[10] M. H. L. Chow, K. W. Siu, C. K. Tse, and Y.-S. Lee, "A novel method for elimination of line-current harmonics in single-stage PFC switching regulators," Power Electronics, IEEE Trans., Jan. 1998, vol. 13, pp. 75–83.

[11] H. Matsuo, L. Tu, F. Kurokawa, and H. Watanabe, "A novel soft-switching buck-boost type AC–DC converter with high power efficiency, high power factor and low harmonic distortion," in Proc. IEEE PESC, 1998, pp. 1030–1035.

[12] M. Daniele, P. Jain, and G. Joos, "A single stage power factor corrected AC/DC converter," in Proc. INTELEC, 1996, pp. 256–262.

[13] P. K. Jain, J. R. Espinoza, and N. A. Ismail, "A single-stage zero-voltage zero-current-switched full-bridge DC power supply with extended load power range," IEEE Trans. Ind. Electron, Apr. 1999, vol. 46, pp. 261–270.

[14] Chongming Qian and Keyue Smedley, "A Topology Survey of Single-Stage Power Factor Corrector with a Boost Type Input-Current-Shaper," in Proc. IEEE APEC, 2000, pp. 460-467

[15] Shiguo Luo; Huai Wei; Guangyong Zhu; Batarseh, I., "Several schemes of alleviating bus voltage stress in single stage power factor correction converters" IEEE PEDS, 1999. Vol. 2, pp921 –926

[16] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control," in Proc. IEEE APEC, 1994, pp. 569–575.

[17] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch power-factor-correction AC/DC converters with DC-bus voltage feedback for universal line applications," IEEE Trans. Power Electron, Nov. 1998, vol. 13, pp. 1079–1088.

[18] H. Watanabe, Y. Kobayashi, Y. Sekine, M. Morikawa, and T. Ishii, "The suppressing harmonic currents, MS (magnetic-switch) power supply," in Proc. INTELEC, 1995, pp. 783–790.

[19] G.-W. Moon, "Novel single-stage, single-switch, AC/DC converter with magnetic energy feedback technique for power factor correction," Proc. Inst. Elect. Eng., Jan. 1999, vol. 146, pp. 111–16.7,

[20] Madigan, M.; Erickson, R.; Ismail, E., "Integrated high quality rectifier-regulators", in Proc., IEEE PESC 1992, pp1043 -1051

[21] Willers, M.J.; Egan, M.G.; Murphy, J.M.D.; Daly, S., "A BIFRED converter with a wide load range", IECON 1994, vol. 1, pp226 -231

[22] Willers, M.J.; Egan, M.G.; Daly, S.; Murphy, J.M.D., "Analysis and design of a practical discontinuous-conduction-mode BIFRED converter", Industrial Electronics, IEEE Transactions on, Vol. 46, Aug. 1999, pp724 -733

[23] Luo, Shiguo, "Front-end converters design and system integration techniques in distributed power systems", PhD dissertation, Univ. of Central Florida, 2001

[24] Shiguo Luo; Weihong Qiu; Wenkai Wu; Batarseh, I., "Flyboost Power Factor Correction Cell and Its Applications in Single-Stage AC-DC Converters", in Proc., IEEE PESC 2002, pp1375-1380

[25] Jin, C.; Ninomiya, T., "A novel soft-switched single-stage AC-DC converter with low line-current harmonics and low output-voltage ripple", in Proc., IEEE PESC 2001, pp660-665

[26] Weihong Qiu; Wenkai Wu; Shiguo Luo; Peter Kornetzk; Batarseh, I., "Practical Design Considerations of a Single-stage Single-switch Parallel PFC Converter for universal voltage applications", IEEE IAS 2002 Annual Meeting, pp 2133-2140

[27] Wenkai Wu; Weihong Qiu; Khalid Rustom; Shiguo Lu; Batarseh, I., "Universal Input Single-Stage PFC AC/DC Converter with Reduced DC-Bus Voltage Stress", in Proc., IEEE PESC 2002, pp1351-1356

[28] Khalid Rustom; Wenkai Wu; Weihong Qiu; Batarseh, I., "Asymmetric Half Bridge Soft-Switching PFC Converter with Direct Energy Transfer", in Proc., IEEE PESC 2002, pp676-681

[29] Weihong Qiu; Wenkai Wu; Shiguo Luo; Wei Gu; Batarseh, I., "A Bi-flyback PFC converter with low intermediate bus voltage and tight output voltage regulation for universal input applications", in Proc., IEEE APEC 2002, pp256 –262

[30] Y. Jiang and F. C. Lee, "Single-stage single-phase parallel power factor correction scheme," in Proc. IEEE PESC 1994, pp1145–1151

[31] O. García, J.A. Cobos, P. Alou, R. Prieto, J. Uceda, S. Ollero, "A New Family of Single Stage AC/DC Power Factor Correction Converters with Fast Output Voltage Regulation", in Proc. IEEE PESC 1997, pp536-542

[32] Javier Sebastian, Pedro J. Villegas, Fernando Nuno, Oscar Garcýa, and Jaime Arau, "Improving Dynamic Response of Power-Factor Preregulators by Using Two-Input High-Efficient Postregulators", Power Electronics, IEEE Trans., Nov. 1997, vol. 12, pp. 1007-1016

[33] O. García, J.A. Cobos, R. Prieto, P. Alou, J. Uceda, "Power Factor Correction: A Survey", in Proc. IEEE PESC 2001, pp8-13

[34] Middlebrook, R. D., and Cuk, S; "A general unified approach to modeling switching-converter power stages", in Proc. EEE PESC, 1976, pp18-34

[35] Vorperian, V.; "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode" Aerospace and Electronic Systems, IEEE Trans., Vol.26, May 1990, pp 490 -496

[36] Vorperian, V.; "Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode" Aerospace and Electronic Systems, IEEE Trans., Vol.26, May 1990, pp 497 -505

[37] Ben-Yaakov, S.; Vorperian, V.; "Modeling the switch of PWM convertors (comments, with reply, on `Simplified analysis of PWM converters using models of PWM switch' by V. Vorperian) " Aerospace and Electronic Systems, IEEE Trans., Vol.28, July 1992, pp 921 -925

[38] Ben-Yaakov, S.; "The unified switched inductor model" Electrical and Electronics Engineers in Israel, 1991. Proceedings., 17th Convention of , March 1991, pp 320 - 323

[39] Ben-Yaakov, S.; "Average simulation of PWM converters by direct implementation of behavioral relationships" in Proc. IEEE APEC, 1993, pp 510 -516

[40] Edry, D.; Hadar, M.; Mor, O.; Ben-Yaakov, S.; "A SPICE compatible model of tapped-inductor PWM converters" in Proc. IEEE APEC, 1994, pp 1021 -1027 vol.2

[41] Zhu, G.; Wei, H.; Kornetzky, P.; Batarseh, I., "Small-signal modeling of a single-switch AC/DC power-factor-correction circuit" Power Electronics, IEEE Trans., Vol. 146, Nov. 1999, pp 1142 –1148