# TOPOLOGY AND CONTROL INVESTIGATION FOR LOW-VOLTAGE HIGH–CURRENT ISOLATED DC-DC CONVERTERS

By

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**DISSERTATION APPROVAL**

The members of the Committee approve the dissertation entitled **Topology and Control Investigation for Low-voltage High–Current Isolated DC-DC converters** by Hong Mao, defended on April 06, 2004.

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It is recommended that this dissertation be used in partial fulfillment of the requirements for the degree of Doctor of Philosophy from the School of Electrical Engineering and Computer Science in the College of Engineering and Computer Science.

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# ABSTRACT

(Advisor: Dr. Issa Batarseh)

High conversion efficiency and fast transient response at high switching frequency are the two main challenges for low-voltage high-current DC-DC converters, which are the motivations of the dissertation work.

To reduce the switching power loss, soft switching is a desirable technique to keep power loss under control at high switching frequencies. A Duty-Cycle-Shift (DCS) concept is proposed for half-bridge DC-DC converters to reduce switching loss. The concept of this new control scheme is shifting one of the two symmetric PWM driving signals close to the other, such that ZVS can be achieved for the lagging switch due to the shortened resonant interval.

By applying a basic DCS concept to a conventional half-bridge DC-DC converter, Zero-Voltage-Switching is achieved for one of the two primary switches. To achieve ZVS for the other switch, a ZVS half-bridge topology is proposed. Basically, by adding an active branch to the conventional half-bridge topology, the leakage inductance energy is trapped during the freewheeling time, and the energy is released to achieve ZVS for the other switch. In addition, a modified ZVS half-bridge topology is proposed to ground the auxiliary switch, and thus, a simple drive circuitry can be applied to the auxiliary switch.

Leakage inductance leads to ringing issue in a half-bridge DC-DC converter. An active-clamp snubber topology is presented in the half-bridge DC-DC converters to recycle the leakage inductance energy and attenuate the ringing. Since dissipative snubbers are removed, a converter can operate more efficiently.

Body-diode reverse-recovery-related loss in SRs increases with the switching frequency. To reduce this reverse-recovery loss, two passive snubber circuits are proposed for SR rectifiers in a current dubler rectifier. The proposed snubbers attenuate reverse recovery ringing and higher efficiencies are achieved.

A unified DC model is derived based on the state-space average equation, which is suited for both symmetric and asymmetric half-bridge DC-DC converters. Furthermore, the DC analysis is conducted based on the unified DC model for symmetric and asymmetric half-bridge DC-DC converters with current-doubler rectifier. The AC model of isolated DC-DC converters is also established, and output impedance is analyzed for the purpose of transient response investigation.

A two-stage approach is a trade-off between conversion efficiency and fast transient response. Full-Duty-Cycle (FDC) two-stage architecture is proposed to achieve desirable open-loop output impedance and fast transient response. Class-D resonant converters are investigated and recognized as potential topologies to reduce switching loss and SR conduction loss. Considering the limited regulation capability of class-D resonant converters, low-Q SRC and LLC resonant converters are proposed as candidate topologies in two-stage approaches.

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*Hong Mao*

*March 2004*

*To my wife - Yangyang*

*To my parents – Taichun Mao*
*Xueqin Hou*

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# 1. INTRODUCTION

## 1.1 Research Background and Motivation

The advances in VLSI (very large scale integration) technologies impose a new challenge for delivering high-quality power to digital ICs. As more and more transistors are integrated into the integrated circuit chip, and with the transistors operating at higher switching frequencies, the power level to supply the chip is significantly increasing [A1-A3].

Recently, solutions based on distributed power system (DPS) architectures [A4-A6] are becoming very popular, especially in multi-board electronic equipment. This technique divides the power conversion scheme from the input source to the load in two stages. The first stage generates an intermediate voltage bus from the AC mains. This DC bus supplies power to the load through different DC-DC converters, located on the same board where the supplied circuits are connected. These DC-DC converters are normally referred to as On Board Converters (OBC).

A typical scheme showing a distributed architecture is shown in Fig. 1.1 [A4]. Distributed architectures present many advantages compared with centralized solutions. These advantages could be summarized as follows [A7]:

- Improved quality of output voltage
- Easier thermal management
- Easier partial redundancy
- Higher power density

- Simpler and cheaper wiring
- Improved reliability

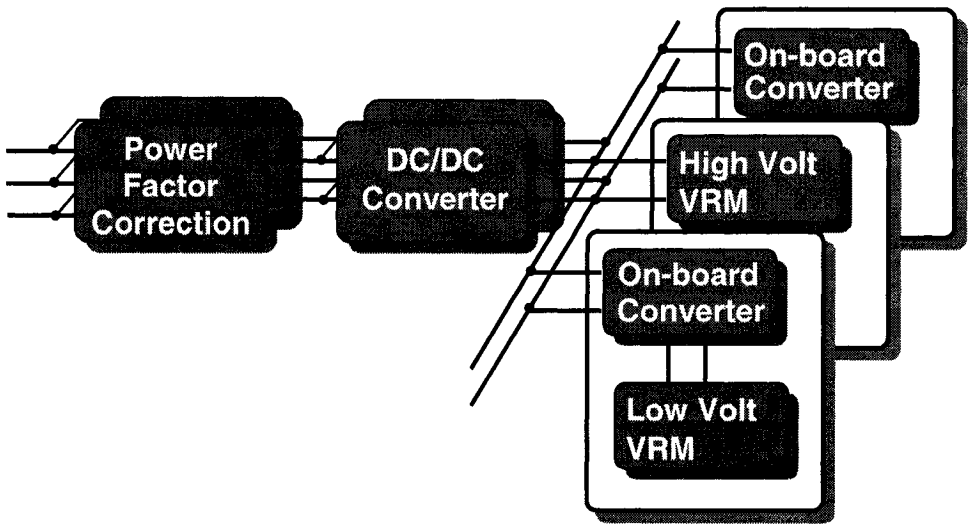



Fig. 1.1 Architecture of distributed power system (DPS)

In distributed power architecture, there is a very important converter that is the last one in the power chain — it is the On Board Converter (OBC). The OBCs supply power directly to the load (IC and microprocessor) and is mounted on the same PCB. Generally, the input voltage bus of OBCs range from 36V~75V with nominal 48V input.

Size is the main concern in the design of on board converters for distributed power supplies. These converters should be as small as possible in order to use them as another component in the design of the load PCB. One idea to reduce the size of a DC-DC converter is to increase switching frequency, because this way the value of reactive components is lower. Transformers, inductors and capacitors become smaller as the

switching frequency increases if their size is dependent on their reactive value. However, this trend is reversed when their size depends on their power losses. The main trend in the design of on-board DC-DC converters in the last years was aimed at very high switching frequencies and at modifying the power circuits to keep switching losses under control.

Lower power consumption implies higher functional integration, hence the voltage supplying integrated circuits gradually decreased because power consumption in an integrated circuit decreases significantly with the reduction of supply voltage. This way, the density of integration circuits keeps increasing and the ICs may operate at higher speed [A1-A3]. However, lower-voltage and higher-current powering requirements pose challenges for the power management designer. For example, according to the Intel roadmap, microprocessors requiring 1V and 100~130A will be available in the market in the next two to four years [A1]. This increase of load current and reduction of its voltage are also accompanied by an increased transient current slew rate at the processor power bus.

With lower voltage, the performance of electronic circuits will improve, but the design of low voltage power converters will be much more difficult, mainly due to the lower efficiency of the low voltage solution. Lower efficiency leads to thermal management difficulties, which prevent size reduction of OBCs.

Some manufactures offer small OBCs featuring very high power densities. However, these converters usually need a large heat sink to obtain high reliability. In most applications, the size of both the converter and the heat sink should be taken into account. These losses are the main constraint in the design if small OBCs are working at high switching frequencies. Efficiency is a key parameter, including view of how good

the power conversion is and also the quality of the thermal management. Through advanced technologies, OBCs can achieve high efficiency such that the heat sink can be removed and the converter size is significantly reduced. Fig. 1.2 illustrates the main topics that affect the size of On Board Converters [A7].

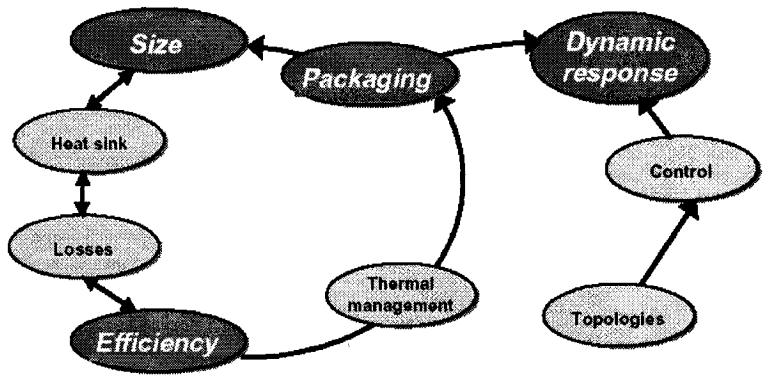



Fig. 1.2 Main factors affecting the design of low output voltage OBCs

With lower output voltage, the conduction loss in the output stage rectifiers becomes more significant and results in considerably reduced efficiency. The efficiency improvement of on-board low-voltage DC-DC converters mainly depends on the components, especially semiconductors [A8-A10]. However, topology and control design is very important for the converter performance based on a specific level of components [A11-A20]. Especially, power stage topologies based on soft-switching/resonant approaches have been recently investigated for high-power density high-efficiency applications [A11-A20]. Advanced topology technology is one of the main approaches to reduce DC-DC converter size and increase power density [A23-A30]. Moreover, with higher switching frequencies, passive components value (such as L and C) can be used

under certain current and voltage ripples. Thus, the related filter phase delay is reduced and better transient response can be achieved.

A low voltage may be achieved through two on-board DC-DC converters in a series. As shown in Fig. 1.1, following the first on-board DC-DC converter, a low voltage Voltage Regulator Module (VRM) is utilized to further step down the voltage. Usually, the second-stage VRM is non-isolated [A2]. Generally, high-density low-voltage on-board DC-DC converters can be divided into two categories: isolated DC-DC converters and non-isolated DC-DC converters. Non-isolated topologies are usually used for 5V~12V input bus applications while isolated topologies are suited for high-input voltage applications such as 48V nominal input, wherein the isolation transformer provides electrical isolation between inputs and outputs. Moreover, the transformer helps to step down the input voltages to output with increased duty cycle. In this way, converter switching and conduction losses are reduced, and higher efficiency can be achieved [A14-A15].

## 1.2 Review of Non-Isolated Multiphase VRM Technology

A typical example of non-isolated on-board DC-DC converters is the Voltage Regulator Module (VRM) for computer microprocessors. The centralized silver box is a typical power source in computer systems. However, with lower voltage and higher current demands, the parasitic resistance and inductance between the centralized silver box and the microprocessor have a severe, negative impact on power quality. It is not practical to use the centralized silver box to provide power directly to the microprocessor [A12].

The power supply architecture must be changed. The point-of-load regulation system is used to deliver highly accurate voltage to the microprocessor, where a dedicated DC-DC converter, the VRM, is placed close to the microprocessor in order to minimize the parasitic impedance between the VRM and microprocessors. Fig. 1.3 shows the power delivery architecture for low-end computer systems, where the on-board VRM is supplied by 5V or 12V input voltage.

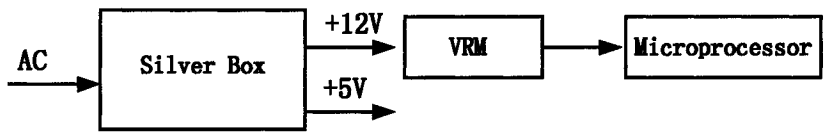



Fig. 1.3 Power delivery architecture for low-end computer systems

Most of today's VRMs draw power from the 12V output of a silver box due to the voltage drop through 5V voltage bus. To achieve fast transient response and better thermal management, the multi-phase buck converter techniques are widely employed in industry. Conventional multi-phase VRMs employ PI controllers for voltage regulation. However, PI compensators limit the transient response of the control loop and the system. Hysteretic voltage control can improve the transient response owing to the bang-bang control concept [A30].

Non-isolated DC-DC converters are generally buck-derived type. To reduce the output current ripple and for better thermal management, interleaved multi-channels are employed [A12, A14]. An interleaved multi-channel buck converter is shown in Fig. 1.4, which consists of N identical buck converters with interconnected inputs and outputs.

The duty cycle of adjacent channels have a phase shift of 360°/N. The main benefit of multiphase technology is the ripple cancellation effect, which enables the use of small inductance to both improve transient response and minimize the output capacitance [A12].

Multiphase converters interleave the inductor currents in individual channels and therefore greatly reduce the total current ripples flowing into the output capacitance. With the current ripple reduction, the output voltage ripples are greatly reduced, which enables the use of very small inductance to improvement response. Therefore small output capacitance can be used to meet the transient requirements. The reduced output voltage ripples also allow more tolerance for voltage variations during the load transient, because the voltage ripple will consume a smaller part of the total voltage tolerance budget and output capacitance.

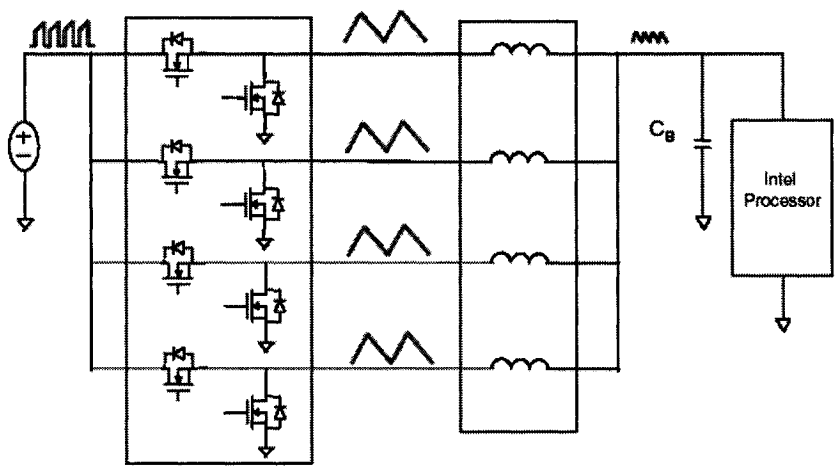



Fig. 1.4 Interleaved multi-channel architecture

Recently, multiphase converters have been widely used for 12V-input VRMs as a standard practice. Correspondingly, many semiconductor companies, such as Intersil, Semitech, National Semiconductor, on Semiconductor, Analog Devices and Voltera, have produced dedicated control chips for multiphase VRMs.

## 1.3 Review of Technology in Isolated DC-DC Converters

The non-isolated 12V input buck converters are required to have high step-down ratios when their output voltage is very low, which makes the converters to operate at small duty cycles and asymmetric transient responses [A14]. With the increase of the required power levels, the 12V input bus voltage may not be able to satisfy the requirements any longer, because the increased distribution loss degrades efficiency. In this case, 48V input-voltage isolated converters are more efficient than 12V input non-isolated VRs, especially for "server" and "workstation" computer systems [A15]. With the isolation transformer, the duty cycle can be optimized and better efficiency is expected [A15]. More importantly, the 48V voltage bus reduces the distribution conduction losses due to the low voltage drop than 12V voltage bus. Generally, for data power systems, the on-board DC-DC converter has a relatively stable input voltage of 48V; for telecom power systems, the input voltage ranges from 36V to 75V. Nominal 48V input voltage bus is more suitable for point-of-load, on-board DC-DC converters. From this point of view, higher-input-voltage isolated DC-DC converters are prevailing in telecom and datacom applications.

### 1.3.1 State-of-the-Art Rectifiers

Without exception, isolation transformers are indispensable parts in isolated DC-DC converters. The conversional isolated Pulse-Width-Modulation (PWM) DC-DC converter structure is shown in Fig. 1.5, which consists of three parts: PWM converter, isolated transformer and rectifier. PWM converter behaves as an inverter to generate AC voltage or current that is applied to transformer primary winding. The transformer delivers AC voltage or current from the primary side to the secondary side and provides electrical isolation. With a transformer turns ratio, the converter may work at a desirable duty cycle and achieve good efficiency. AC voltages or currents are delivered to the transformer secondary side, and through the rectifier, a DC voltage can be obtained from the output. Hence, the energy processing in a DC-DC converter is DC-AC-transformer-AC-DC.

Conventional voltage-driven rectifiers are shown in Fig. 1.6, where inductor(s) are added to the transformer secondary side because a voltage source cannot be applied to a capacitor directly. Forward rectifier is a "half-wave" rectification type, which means the transformer output current is asymmetric with unidirectional DC current with AC components; thus transformer windings and rectifier utilization are limited. All other rectifiers and transformers are symmetric with bi-directional current, and transformer magnetics resets itself without external winding or circuitry.

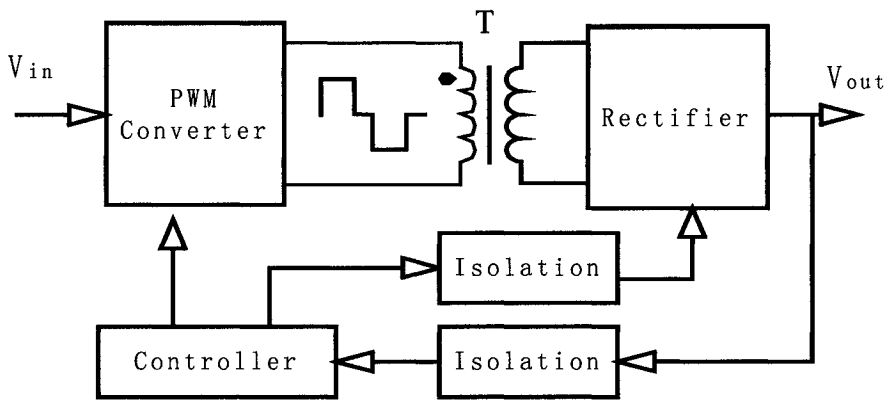



Fig. 1.5 Architecture of conventional PWM isolated DC-DC converters

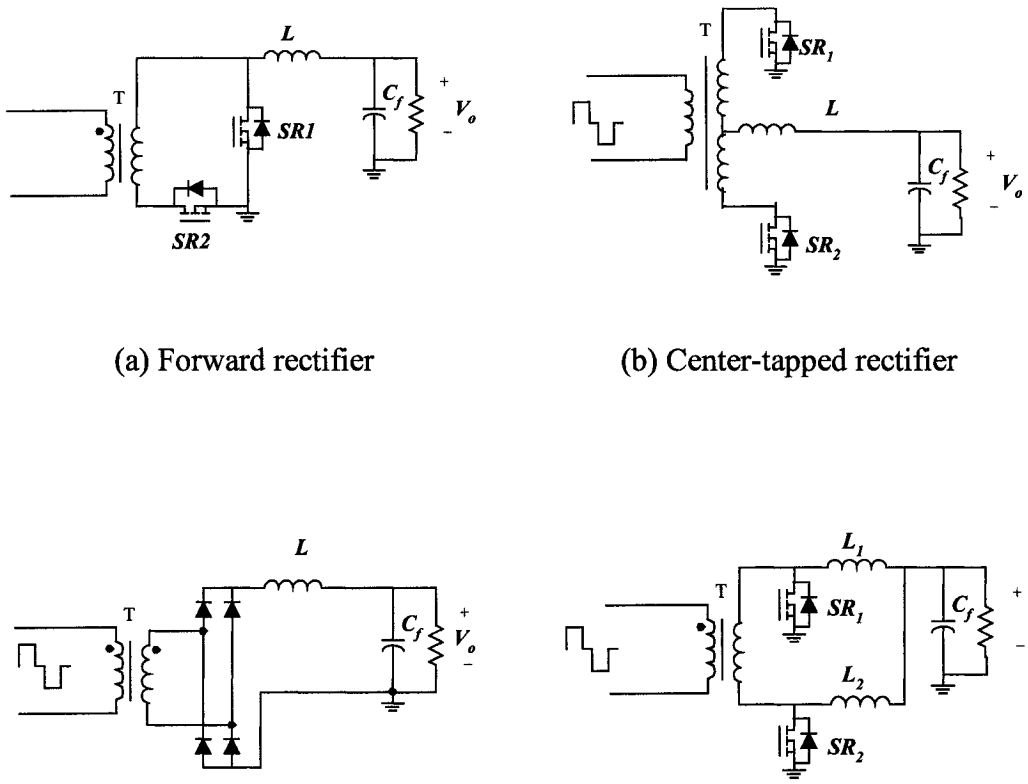
PWM converters in Fig. 1.5 can be a variety of state-of-the-art topologies, such as forward, flyback, two-switch forward, push pull, half bridge and full bridge. Those topologies can be buck type or boost type according to the fact that filter inductor(s) are located at inputs or output. Correspondingly, they can be called current-fed or voltage-fed DC-DC converters. In general, a current-fed PWM converter generates an AC current feeding to a transformer. Likewise, a voltage-fed PWM converter generates an AC voltage feeding to a transformer. Correspondingly, voltage-driven rectifiers are connected with the transformer secondary side for voltage-fed (buck-derived) converters; current-driven rectifiers are connected with the transformer secondary side for current-fed (buck-derived) converters.

Among those secondary-side rectification topologies, the forward topology [A13, A18, A24, A25, A26, A34] has the simplest structure. However, it is the least suitable for low-voltage high-current applications. Namely, the forward topology requires a larger filter inductance and exhibits larger rectification losses than a center-tapped or current-

doubler rectifier [A41]. In fact, in the center-tapped topology, the frequency of the output-filter-inductor voltage waveforms is twice the switching frequency, while in the forward topology it is equal to the switching frequency. As a result, the required value of the filter inductance in the center-tapped topology is significantly smaller than that in the forward rectifier. A center-tapped rectifier is a popular rectification topology and is a kind of "full-wave" rectifier. The drawback of the center-tapped rectifier is that the transformer is tapped and two secondary windings carry output currents alternatively. In other words, the transformer windings are not fully utilized [A32].

Compared to center-tapped topology, a full-bridge rectifier reduces secondary-side windings to one. Also, the winding carries AC current, and it increases transformer utilization [A32, A33]. However, since output current goes through two rectifier diodes (or synchronous rectifiers), the rectifier conduction loss is significant at low-voltage-output applications due to the increased forward voltage drop across rectifiers. The full-bridge rectifier is usually used for higher output voltage applications.

For low-voltage and high current applications, the current-doubler rectifier is widely used in industry and recognized as a good rectification topology [A32-A34, A41]. Since the current through the transformer secondary winding is half the output current, the current-doubler rectifier minimizes the secondary-winding *rms* current and conduction losses. Since two filter inductors share the output current, easier design and better thermal management for output inductors is achieved [A41]. Moreover, the current-doubler scheme minimizes the number of high-current interconnections to simplify the secondary layout and further reduce the layout-related losses.




(a) Forward rectifier (b) Center-tapped rectifier

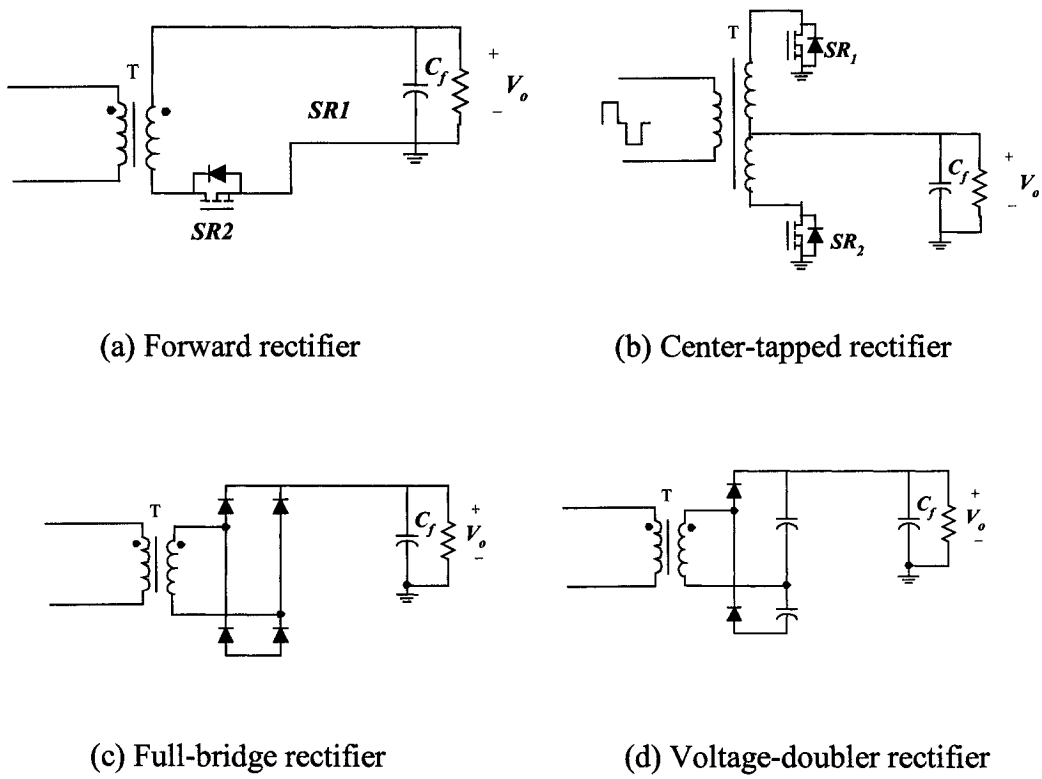
(c) Full-bridge rectifier (d) Current-doubler rectifier

Fig. 1.6 Voltage-driven rectifiers

As mentioned above, if an AC current source is connected to a transformer primary winding, a current-driven transformer and corresponding rectifier should be applied to this kind of PWM converter. Fig. 1.7 shows four types of conventional current-driven rectifiers. Similar to the voltage-driven rectifier, there are four typical rectification types, wherein forward rectifier is asymmetric, and others are symmetric. In forward rectifier, a reset scheme has to be applied to the transformer.

In current-driven rectifiers, because transformers work as current sources, the secondary filter inductors in voltage-driven rectifiers can be removed. In fact, the filter

inductor is moved to the transformer primary side. Because the DC-DC converter input is a voltage source, to form a current source input, an inductor has to be placed in the primary side. The inductor is actually a filter inductor. It should be noted that for low-voltage high-current output applications, putting inductor in the primary is good, because primary circuitry has higher voltage and lower current stresses, which means smaller current flows through the primary filter inductor. In that case, low-current inductors are easier to design than high-current inductors. However, compared with PWM voltage-driven rectifiers, the filter inductor in the PWM current-driven rectifiers freewheels on the primary side. Therefore, during switch-off periods, no power supplies the output capacitors, which results in discontinuous output currents and larger output voltage ripples. Actually, the flyback converter falls into this category of current-fed rectifiers.




(a) Forward rectifier

(b) Center-tapped rectifier

(c) Full-bridge rectifier

(d) Voltage-doubler rectifier

Fig. 1.7 Current-driven rectifiers

To achieve a continuous power-supplying output capacitor and load, full duty cycle can be applied to primary switches. In other words, the freewheeling period of the primary inductors is eliminated [A42-A43]. An example of this is shown in Fig.1.8 [A42], where two DC-DC converter stages are in series to provide a step-down low-voltage conversion. Secondary stage is a current-fed push-pull topology with a center-tapped current-driven rectifier on the secondary side. Push pull topology operates at 50 percent duty cycle, thus the first-stage buck converter is responsible for voltage regulation. A control loop is closed through the first stage. Actually, an output filter capacitor and load can be reflected to the transformer primary side as a capacitor paralleled with a resistor. The secondary stage is just like a DC transformer.

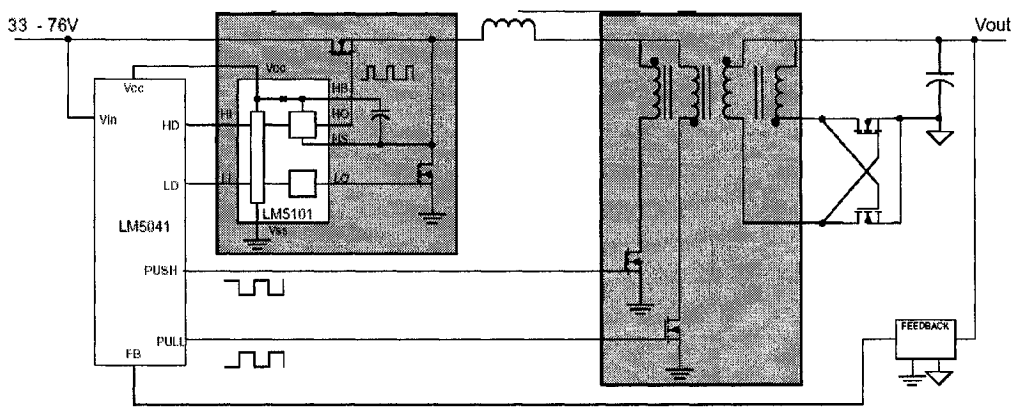



Fig. 1.8 An application of a center-tapped current-driven rectifier

### 1.3.2 State-of-the-Art PWM DC-DC Converters

In low-voltage applications, buck-derived DC-DC topologies prevail in commercially available products. Those topologies include flyback, forward, push pull, half bridge and full bridge.

Flyback topology is an isolated buck-boost topology. The advantages of this topology are simple structure and low cost. The transformer magnetizing inductance is charged and stores energy when the primary switch is turned on, and the stored energy is transferred to the output capacitor when the primary switch is turned off. Because there is no power supplying output capacitor and load, the output current is discontinuous, which results in large output current and voltage ripple. For low-voltage high-current applications, this feature could be a disaster, because the energy stored in the output capacitor is proportional to the square of output voltage value and a discontinuous current results in large output voltage ripple [A38]. Generally speaking, flyback topology is not suitable for low-voltage high-current applications.

Forward topology is the simplest among buck-derived topologies [A24, A25, A26, A34, A35]. It requires a single switch and therefore finds applications at lower power levels than those commonly encountered in the half-bridge and full-bridge configurations. The main disadvantage of the forward topology is its unidirectional core utilization and rectifier configuration, which leads to higher current ripples and bulky core size. However, as mentioned, forward topology is still widely utilized in industry because of its simplicity, especially in lower power levels.

Forward topology is obtained by adding an isolation transformer in the basic buck DC-DC converter. The steady-state voltage across any transformer or inductor must be

zero, otherwise the core will saturate. In the push-pull, half-bridge and full-bridge systems, this volt-second balance naturally occurs because of the symmetry of the alternating positive and negative waveforms applied to the windings. In a single ended forward converter, this volt-second balance doesn't happen naturally. Specific provision must be made to reset the core by allowing the voltage across the windings to back-swing during the switch "off" time so that the reverse volt-seconds equal and cancel the volt-seconds applied during the "on" time. With a variety of magnetics reset provisions [A21-25], there are many derivative forward converters as shown in Fig 1.9.

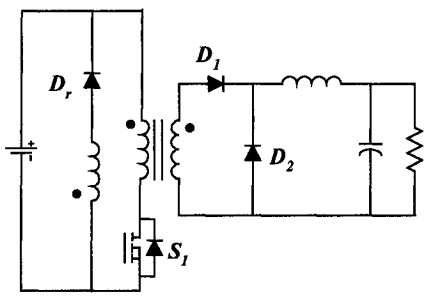
In Fig. 1.9(a), an additional winding and a diode Dr in series are added to reset the transformer core by recycling the transformer magnetizing energy. Diode $D_1$ is used to block the reverse voltage when the transformer back swings. If the turns ratio between the primary wining and reset winding is 1:1, the forward converter must operate at a duty cycle below 50 percent to avoid transformer saturation. In this case, the primary switch withstands twice the input voltage. In Fig. 1.9(b), a passive RCD voltage clamp snubber circuit is applied to reset the transformer, where all magnetizing energy is transferred in the snubber capacitor and dissipated in the snubber resistor. Obviously, a RCD clamp circuit has lower efficiency than a reset-winding forward converter. However, the transformer design is much easier because the third winding and corresponding coupling requirement are eliminated.

Replacing the RCD snubber with an active clamp snubber circuit, an active-clamp forward converter is formed as shown in Fig. 1.9(c) [A26, A35]. It should be noted that a grounded P-channel MOSFET is used as an active switch to simplify the driving circuitry. In the active-clamp forward, the auxiliary switch can recycle magnetizing energy back to

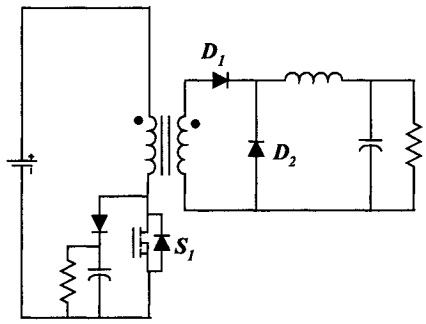
input voltage bus. Most importantly, main switch can achieve zero-voltage-switching by utilizing magnetizing and leakage inductance energy. Therefore, the topology can be used in higher switching frequency than conventional forward topologies. Fig. 1.9(d) shows a derivative active-clamp forward converter: flyback-forward converter [A13], where the energy transfer becomes bi-directional, and transformer utilization is improved. It should be noted that a DC current bias exists in the magnetizing inductance in this topology, thus the transformer should be carefully designed.

As discussed above, in active-clamp forward topologies some kinds of lossless snubbers are used to reset and recycle magnetizing energy. The only disadvantage is that an additional switch complicates the power stage and driving circuitry. Fig. 1.9(e) shows a lossless passive LCD snubber forward converter, where the magnetizing energy is transferred into the capacitor when the switch is off; when the switch is on, the capacitor energy is transferred into the snubber inductor. Later on, when the switch is off, the energy is recycled back to the input voltage source through the diode $D_{r1}$. Theoretically, the snubber is lossless and the converter may achieve high efficiency.

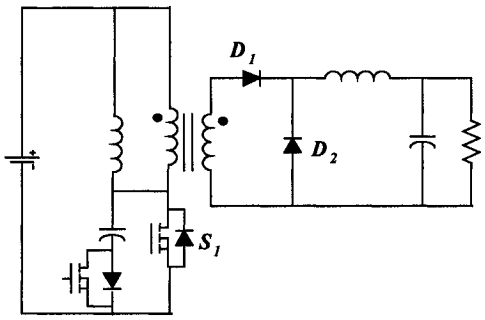
In the passive and active clamp snubber circuitry discussed above, main switch voltage stress exceeds input voltage. Higher voltage stress means higher on-resistance and conduction loss. Fig. 1.9(f) shows a two-switch forward converter, where the transformer core is reset by clamping the transformer primary winding to the input voltage bus using two diodes. Since the voltage across two main switches is less than the input voltage, when compared with active-clamp converters, this two-switch forward topology is more reliable [A11].



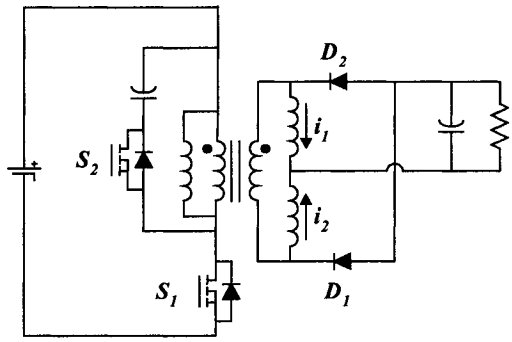

(a) Forward topology with a reset winding



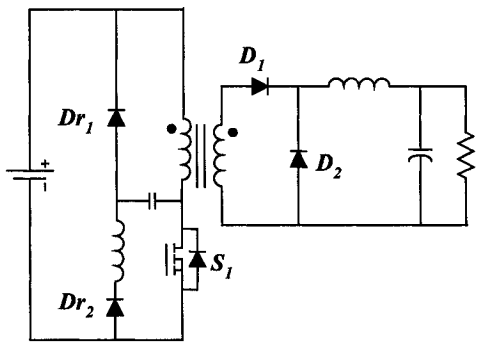

(b) RCD clamp forward topology



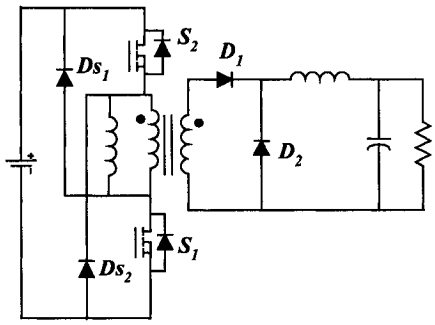

(c) Active-clamp forward topology




(d) Flyback-forward DC-DC topology




(e) LCD clamp forward topology




(f) Two-switch forward converter

Fig. 1.9 A variety of forward DC-DC topologies

In the topologies of forward converters previously discussed, the converters operate at asymmetric conditions; the energy delivery in the transformer is unidirectional. In other words, voltage and current stresses are unevenly distributed between the main switch and the active-clamp switch, which results in higher stress on switches and rectifiers compared to symmetric half-bridge and full-bridge converters. The voltages across the switches are higher than the input DC voltage, which increase the on-state resistance of switches.

Unlike flyback and forward topologies, push-pull, symmetric half-bridge and full-bridge DC-DC topologies [A15, A27, A33] have symmetric architectures on both the primary side and the secondary side, and therefore they are found in higher power level applications. For low voltage and high current applications, both center-tapped and current-doubler rectifiers are widely employed in the secondary side.

Push-pull topology is shown in Fig. 1.10. Push-pull topology almost has the same complexity as the half-bridge topology. However, in the half-bridge topology, capacitor(s) are needed in addition to the two main switches, while in the push-pull topology, center-tapped transformer winding is needed. Push-pull topology is suitable for low input voltage, and it tends to exhibit low primary-side conduction losses, since at any given instant only one switch is connected in series with the DC source. The push-pull configuration is prone to transformer saturation problems, since it cannot be guaranteed that the forward voltage drops and conduction time of two switches are exactly equal. For wide input voltage applications, push-pull topology has to operate at hard switching, and the ringing related to leakage inductance is a problem. In addition, higher voltage-rating

MOSFETs have to be selected for switches, because the theoretical minimum drain-to-source voltages seen by primary MOSFETs are twice the DC input voltage.

The half-bridge converter is also a push-pull version of the buck regulator. As shown in Fig.1.11, there are two configurations with a current-doubler rectifier. In fact, the center-tapped rectifier also can be applied to the transformer secondary winding. The key advantage of the half-bridge topology against the push-pull center-tap configuration is that the switch voltage ratings are cut in half (although the current is doubled). Moreover, the voltage applied to the transformer primary winding is cut in half, and less transformer primary turns are needed to step-down to the same output voltage level. For low output voltage applications, this is a desirable advantage since transformer secondary winding is single turn. In addition, current doubler rectification is good for stepping voltage down because the duty cycle is always less than 0.5.

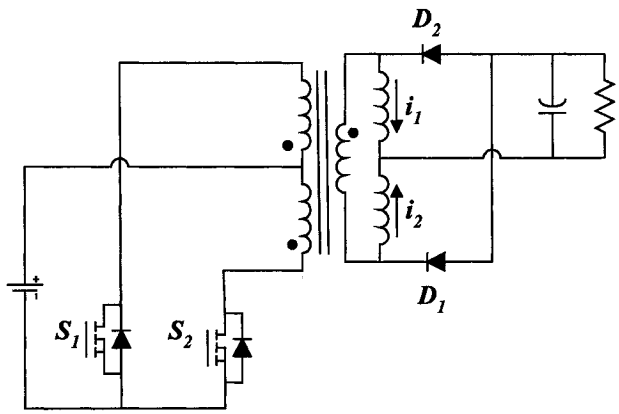
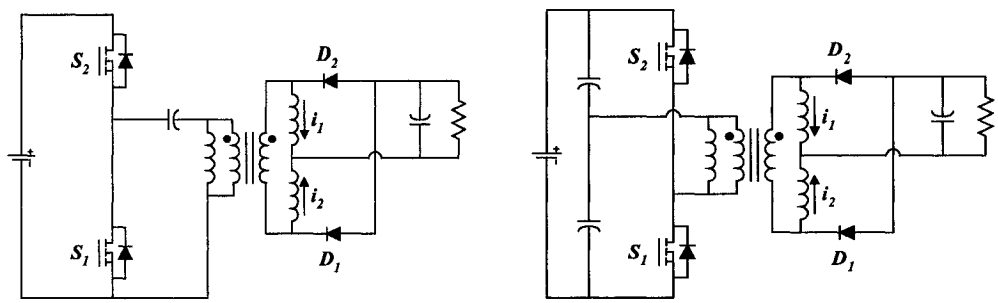



Fig. 1.10 Push-pull DC-DC converter

There are two conventional control schemes for the half-bridge converter, which are symmetric control and asymmetric (complimentary) control. The main drawback of the conventional symmetric control is that both primary switches in the converter operate at hard switching condition. Moreover, during the off-time period of two switches, the oscillation between the transformer leakage inductance and junction capacitance of the switches results in energy dissipation and EMI emissions due to the MOSFETs body diodes reverse recovery [A44~A46]. To suppress the ringing, resistive snubbers are usually added. As a result, energy in the transformer leakage inductance is significantly dissipated in snubbers. Therefore, the symmetric-controlled half bridge is not a good candidate for high-switching frequency power conversion [A45].

The asymmetric (complementary) control was proposed to soften switching behavior of the half-bridge switches [A47, A48]. Two driving signals are complementarily generated and are applied to high-side and low-side switches. Thus, two switches may turn on at ZVS conditions owing to the fact that the transformer primary current charges and discharges the junction capacitance. However, asymmetric stress distribution on the corresponding components may occur due to the asymmetric duty cycle distribution for the primary two switches [A49]. In other words, current stresses in two primary switches are not identical; voltage and current stresses on secondary rectifiers are not equal. As a result, diodes or synchronous rectifiers with higher withstanding voltage are needed at the penalty of degrading the performance and efficiency of the rectifier stage [A45, A46, A49]. Furthermore, the DC gain ratio of the converter is nonlinear, thus higher duty cycle variation is needed for the same input voltage variation in comparison with the symmetric control scheme, which makes the

converter operate further beyond optimum operating point at high input voltage [A49]. Therefore, the complementary (asymmetric) PWM control is more suitable for applications where input voltage is fixed. As a solution to reduce the duty cycle variation for wide input voltage range, an asymmetric transformer turns ratio — together with integrated-magnetic structure — is proposed in [A49], such that rectifiers with lower withstanding voltage may be used to improve the performance. However, the power delivery for the transformer and current stresses in the switches and rectifiers is still uneven [A49].




(a) (b)

Fig. 1.11 Half-bridge DC-DC converters

Full-bridge topology is a good candidate for higher power levels, because the current stresses are evenly distributed between four switches, and the transformer core and rectifiers are bi-directional and well utilized [A15, A33, A50]. A full-bridge converter is shown in Fig. 1.12. The voltage stress applied to four main switches is equal to input voltage, while the current stress through switches is half the current in a half-

bridge converter for the same output power level and same input voltage. Therefore, the full bridge has the voltage stress of half bridge and the current stress of the push-pull converter.

Phase-shifted full bridge [A15, A33, A50] is one of the most attractive zero-voltage-switching techniques since it allows all switches to operate at Zero-Voltage-Switching (ZVS) by utilizing transformer leakage inductance and junction capacitance of MOSFETs without adding an auxiliary switch. Actually, in a phase-shifted full-bridge converter, the leakage inductance energy is trapped by two up-switches or down-switches to achieve ZVS for lagging leg switches. Basically, four primary switches can achieve ZVS. At light load, the ZVS switching is always lost. That is not a big issue because the soft switching is not dispensable at a light load. It should be noted that when a full-bridge converter operates at a wide range of input voltage at high line input, the effective duty cycle becomes so small that the recycling interval increases leading to more conduction loss.

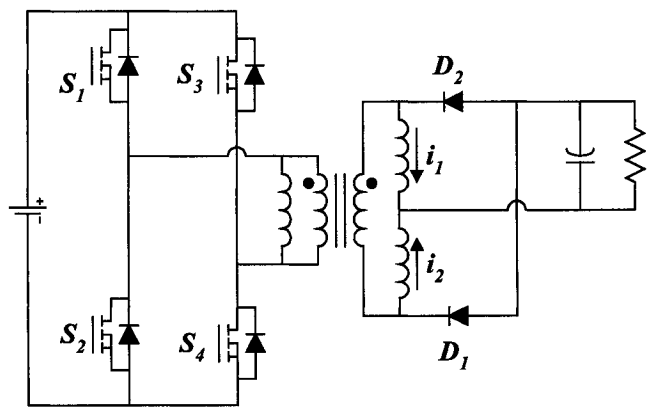



Fig. 1.12 Full-bridge DC-DC converters

In all topologies discussed above, the complexity of the full bridge is highest due to its large switch count and complicated control and driving [A44~A45]. Half-bridge topology is an attractive topology for middle power levels owing to its simplicity compared with the full-bridge topology. Although the full-bridge topology offers both the current stress of the push-pull topology and the low voltage stress of the half-bridge topology, the half-bridge topology is a preferred choice because of its lower component count and overall simplicity. However, in [A42], phase-shift controlled full-bridge topology is recognized as the best choice at high frequencies where soft switching of the primary switches is required to maintain efficiency.

## 1.4 Dissertation Outline

This dissertation consists of five chapters. They are organized as follows.

Chapter 1 is the background review of the existing on-board DC-DC converter technologies and the technical challenges for low-voltage high-current DC-DC converter designs. Size is the main concern in the design of on-board converters for distributed power supplies. One idea to reduce the size of a DC-DC converter is to increase switching frequency, because the value of reactive components is lower. Transformers, inductors and capacitors become smaller as switching frequency increases if their size is dependent on their reactive value. However, switching loss increases with switching frequency. When the switching frequency is increased to a certain level, the converter size depends on the power losses. These losses are the main constraint in the design of small OBCs working at high switching frequencies.

The main trend in the DC-DC converter design in the last years was aimed at very high switching frequencies and at modifying the power circuits to keep switching losses under control. To reduce the switching power loss, soft switching is a desirable technique to reduce power loss and increase converter power density.

For non-isolated OBC converters, multiphase converters interleave the inductor currents in individual channels and therefore greatly reduce the total current ripples flowing into the output capacitance. With the current ripple reduction, the output voltage ripples are greatly reduced, which enables the use of very small inductance to improve response. Therefore, small output capacitance can be used to meet the transient requirements.

For low-voltage and high-current isolated DC-DC converters, secondary power loss dominates overall power losses. In the dissertation, a variety of rectification architectures are reviewed for low-voltage and high-current applications. Current-doubler and center-tapped rectifiers are recognized as the suitable topologies for low-voltage and high-current rectifiers. In addition, state-of-the-art topologies such as flyback, forward, half-bridge, full-bridge and push pull — associated with as their derivative topologies — are reviewed.

Soft-switching techniques are the prevailing solution to reduce switching losses, which have been intensively investigated in the last two decades. In Chapter 2, a Duty-Cycle-Shift (DCS) concept is proposed for half-bridge DC-DC converters to reduce switching loss. The concept of this new control scheme is shifting one of the two symmetric PWM driving signals close to the other, such that ZVS may be achieved for the lagging switch due to the shortened resonant interval.

By applying a basic DCS concept to a conventional half-bridge DC-DC converter, Zero-Voltage-Switching is achieved for one of the two primary switches. To achieve ZVS for the other switch, a ZVS half-bridge topology is proposed in the dissertation. By adding an active branch to the conventional half-bridge topology, the leakage inductance energy is trapped during the freewheeling time, and the energy is released to achieve ZVS for the other switch. In addition, all auxiliary switches can achieve soft switching. With proposed techniques, converter efficiency is improved, and it allows the converter to operate at a higher switching frequency.

In the proposed ZVS half-bridge topology, the auxiliary switch is floating to the ground. A modified ZVS half-bridge topology is proposed to ground the auxiliary switch, and thus a simple drive circuitry can be applied to the auxiliary switch. For low voltage applications, to reduce the freewheeling conduction in the diode of the auxiliary branch, a synchronous rectifier is presented with simplified driving circuitry.

All topologies based on a DCS concept are verified by experimental results. The DCS concept is successfully demonstrated in an industry demo prototype.

In Chapter 3, two snubber topologies are proposed. For conventional half-bridge DC-DC converters, the leakage inductance results in ringing issues during the off-time interval. To dampen the ringing, dissipative snubbers such as RC and RCD snubbers are widely utilized. In the dissertation, an active-clamp snubber topology is presented in half-bridge DC-DC converters to recycle the leakage inductance energy and attenuate the ringing. Since dissipative snubbers are removed, a converter can operate more efficiently.

For low-output-voltage applications, SR losses account for a high portion of overall conversion losses. Body-diode reverse-recovery-related loss in SRs increases with the

switching frequency. To reduce this reverse-recovery loss, two passive snubber circuits are proposed for SR rectifiers. The proposed snubbers attenuate reverse recovery ringing, and higher efficiencies are achieved.

Chapter 4 mainly focuses on the modeling of the half-bridge DC-DC converter. A unified DC model is derived based on the state-space average equation, which is suited for both symmetric and asymmetric half-bridge DC-DC converters.

A half-bridge DC-DC converter with current-doubler rectifier is actually a two-channel isolated buck converter. Because peak-current-mode control cannot be directly applied to half-bridge DC-DC converter, the current sharing between two inductors is an issue. By solving the DC model, the DC current solution is obtained. The solution shows that the DC current sharing in the two inductors mainly depends on duty cycles and inductor DCRs in the converter, and SR on-resistances have no impact on the current sharing. The analysis also shows that a DC magnetizing current exists in the transformer of the asymmetric half-bridge DC-DC converter, and that the inductor currents are unbalanced if two inductor DCR values are asymmetric.

To solve the DC imbalance issue of the inductor currents, a simple modification is applied to the half-bridge DC-DC converter. Simulation and an established DC model verify that the current sharing between the two inductors can be achieved even under asymmetric DCR values, and the DC bias of transformer magnetizing current is eliminated.

The AC model is established based on a closed-loop controlled system. For a current change disturbance, the closed-loop output impedance determines output voltage

overshoots and undershoots. Closed-loop output impedance is analyzed based on the AC model, and some important conclusions are given, which are the base of Chapter 5.

For one-stage approaches of DC-DC conversion, a converter has functions of regulation and isolation. In the two-stage approaches, regulation and isolation are separated from the other. In Chapter 5, two-stage Voltage Regulator (VR) architecture and Intermediate Bus Architecture (IBA) for datacom applications are reviewed.

Full-Duty-Cycle (FDC) two-stage architecture is proposed to achieve desirable open-loop output impedance. Since the filter inductance can be minimized in the FDC converter, the open-loop output impedance is becoming first-order, and it may compete with closed-loop controlled converters. FDC converters are potential candidate topologies for two-stage approaches.

High-switching frequency reduces magnetic and passive filter size. In Chapter 5, some resonant converters are investigated and recognized as potential topologies for two-stage approaches. SRC and LLC resonant converters can reduce the body diode crossover conduction loss of synchronous rectifiers. PRC and LCC converters can soften the reverse recovery of body diodes in SR rectifiers.

The conclusion is given in Chapter 6.

# 2. HALF-BRIDGE DC-DC CONVERTERS BASED ON THE DUTY-CYCLE-SHIFT (DCS) CONCEPT

## 2.1 Introduction

To further increase the processing speed and decrease the power consumption in VLSI (Very Large Scale Integration) Integrated Circuits, the operating voltages of ICs keep decreasing. Lower power consumption implies higher functional integration, better thermal management and more reliability. However, increased processing speed and transistor integration density keeps increasing the power level instead of decreasing it with reduced operating voltage. These factors pose big challenges to power management. One of the challenges is the low operating voltage. Lower operating voltage means lower conversion efficiency for DC-DC converters due to semiconductor voltage drop. The second challenge is that the estate budgeted for power management doesn't increase with the raised power level of power converters. Therefore, power density of power supplies is strongly demanded. To achieve this goal, reduced sizes of passive components and high efficiency power conversion are the solutions. To reduce the volume of passive components, such as magnetics cores and capacitors, switching frequency has to be pushed higher. However, switching-related losses have significant impact on conversion efficiency.

Soft-switching techniques are the prevailing solution to reduce switching losses, which has been intensely investigated in the last two decades. Some of the invented techniques in recent years, such as active-clamp forward converter and full-bridge phase-shifted converter, have been widely applied to isolated DC-DC conversion products. Several techniques for high-frequency DC-DC conversion have been proposed to reduce

component stresses and switching losses while achieving high-power density and improved performance [B1-B11]. Among them, the phase-shifted zero-voltage-switching (ZVS) full bridge [B1~B3] is one of the most attractive techniques, since it allows all switches to operate at ZVS by utilizing transformer leakage inductance and MOSFETs' junction capacitance without adding an auxiliary switch. However, the complexity of the full bridge technique is among the highest of the conventional topologies due to its large switch count and complicated control and driving. Active-clamp forward topology [B4~B6] is another typical way to successfully realize ZVS for the switches by utilizing the leakage inductance, magnetizing inductance and junction capacitance. However, the topology of the converter is asymmetric and the energy delivery is unidirectional. In other words, voltage and current stresses are unevenly distributed, resulting in the individual switch and rectifier stresses being higher compared with symmetric half-bridge and full-bridge converters. This disadvantage limits the power level of the active-clamp forward topology applications. In addition, DC bias of magnetizing current may exist in the transformer [B5].

The half-bridge (HB) DC-DC converter is an attractive topology for middle power level applications, attributing to its simplicity. There are two conventional control schemes for the HB DC-DC converter, namely symmetric control and asymmetric (complimentary) control. The main drawback of the conventional symmetric control is that both primary switches in the converter operate at hard switching condition. Moreover, during the off-time period of two switches, the oscillation between the transformer leakage inductance and junction capacitance of the switches results in energy dissipation and EMI emissions due to the reverse recovery of MOSFETs body diodes. To

suppress the ringing, resistive snubbers are usually added. As a result, energy in the transformer leakage inductance is significantly dissipated in snubbers. Therefore, the symmetric-control half bridge is not a good candidate for high-switching frequency power conversion.

The asymmetric (complementary) control was proposed to achieve ZVS operation for HB switches [B7~B11]. Two drive signals are complementarily generated and applied to high-side and low-side switches. Thus, the two HB switches may be turned on at ZVS conditions, attributing to the fact that the transformer primary current charges and discharges the junction capacitance. However, asymmetric stress distribution on the corresponding components may occur due to the asymmetric duty cycle distribution for the two primary switches. In other words, current stresses in the two primary switches are not identical, and voltage and current stresses on secondary rectifiers are not equal. As a result, diodes or synchronous rectifiers with higher voltage rating are needed at the penalty of degrading the performance and efficiency of the rectifier stage [B10]. Furthermore, the DC gain ratio of the converter is nonlinear, thus higher duty cycle variation is needed for the same input voltage variation in comparison with symmetric PWM control scheme. This makes the converter operate further beyond the optimum operating point at high input voltage [B10]. Therefore, the complementary (asymmetric) PWM control is more suitable for applications where the input voltage is fixed. As a solution to reduce the duty cycle variation for wide input voltage range, an asymmetric transformer turns ratio together with integrated-magnetic structure, was proposed in [B10], such that rectifiers with lower withstanding voltage may be used to improve the

performance. However, the power delivery of the transformer and current stresses in the switches and rectifiers are still uneven [B10].

In this chapter, a new control concept, known as "Duty-Cycle-Shift PWM" (DCS PWM) control, is proposed and applied to the conventional HB DC-DC converters to achieve ZVS for one of the two switches without adding extra components or asymmetric penalties of the complementary control. The concept of this new control scheme shifts one of the two symmetric PWM driving signals close to the other, such that ZVS may be achieved for the lagging switch due to the shortened resonant interval. Unlike the asymmetric control, the width of the duty cycle for the two switches is kept equal, such that all corresponding components work at the conditions with even stresses, as is the case with the symmetric control scheme.Moreover, based on the DCS PWM control, two half-bridge DC-DC converter topologies are proposed to achieve ZVS for the other switch and auxiliary switch by adding an auxiliary switch and diode in the conventional half bridge. ZVS for the other switch is achieved by utilizing the energy trapped in the leakage inductance. In addition, the proposed topology with DCS PWM control eliminates the ringing resulting from the oscillation between the transformer leakage inductance and the switches junction capacitance during the off-time period. Therefore, the proposed converter has a potential to operte at higher efficiencies and switching frequencies.

## 2.2 Duty-Cycle-Shift Concept

Fig. 2.1 shows the half-bridge DC-DC converter with current doubler rectifier. The ideal waveforms for the symmetric PWM control is sketched in Fig. 2.2 (a), where $L_{k,}$ is

the leakage inductance, ip and $i_M$ are the transformer primary-side input and magnetizing currents, respectively and $i_{D1}$ is the forward current through rectifier diode $D_1$. Besides the hard switching, conventional symmetric PWM control has transformer-leakage-inductance related disadvantages. During the off-time period when both switches are off, the energy stored in the transformer leakage inductance may be recycled to primary DC bus through the body diodes of MOSFETs. However, because of the reverse recovery current of the body diodes, the oscillation between the transformer leakage inductance and the MOSFETs junction capacitance is significant on the primary side. To suppress the ringing, snubber circuits usually are necessary to add, but losses dissipated in the snubber become dramatically large, especially at high input current and high switching frequencies.

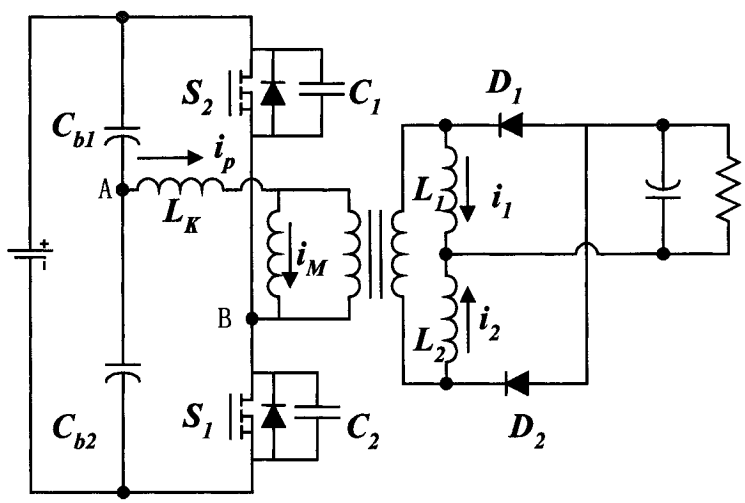



Fig. 2.1 Half-bridge DC-DC converter with current doubler rectifier

### 2.2.1 Proposed DCS PWM Control Scheme

Fig. 2.2 (b) shows the key waveforms of the half-bridge converter with the proposed DCS PWM control. Based on symmetric PWM control, $S_2$ driving signal $V_{gs2}$ is shifted

left such that the $V_{gs2}$ rising edge is close to the falling edge of $S_1$ driving signal $V_{gs1}$. When $S_1$ is turned off, the transformer primary current charges the junction capacitance of switch $S_1$ and discharges the junction capacitance of switch $S_2$. After the voltage across drain-to-source of $S_2$ drops to zero, the body diode of $S_2$ conducts to carry the current. During the body diode conduction period, $S_2$ may be turned on at zero-voltage switching. No ringing occurs during the transition period.

Fig. 2.3 shows a possible modulation approach for realization of DCS PWM control scheme. Where, Vsaw is the SAW carrier waveform for modulation and Vc and –Vc are control voltages derived from the front voltage or current controller. By modulating Vc and –Vc, driving signals for $S_1$ and $S_2$ can be generated, respectively. Because the falling time of the SAW waveform is short, the falling edge of $S_1$ is always close to the rising edge of $S_2$, which provide a possibility of ZVS for $S_2$.

This modulation method differs from the conventional symmetric PWM method in that the direction of variation of the two duty cycles is opposite as shown in Fig. 2.3(b) by the arrows on the driving signals' waveforms. In other words, since Vc and –Vc are symmetrically centered around zero, the duty cycle of $S_1$ is regulated by moving its rising edge left and right, while the duty cycle of $S_2$ is regulated by moving its falling edge right and left, keeping $S_1$ and $S_2$ with the same duty cycle.

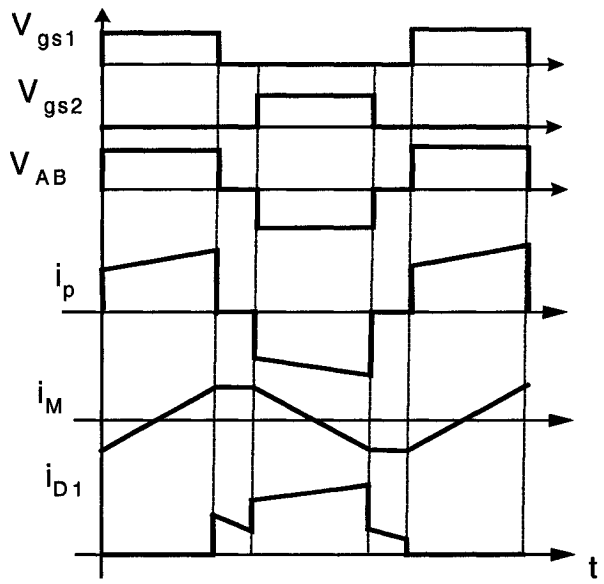



Fig. 2.2 (a) Waveforms of conventional HB DC-DC converters

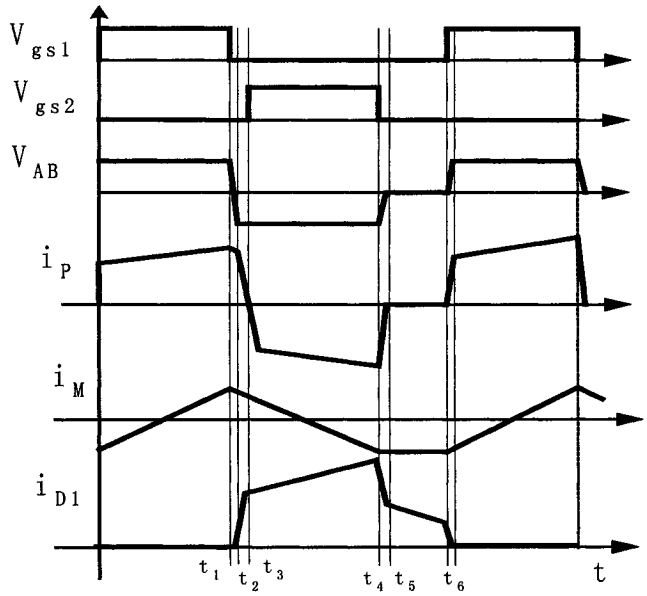



Fig. 2.2 (b) Waveforms of DCS HB DC-DC converters

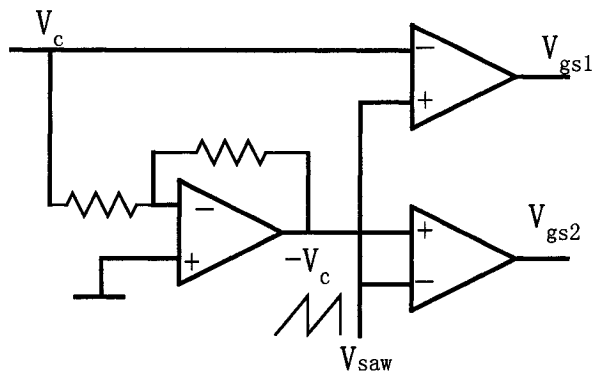



Fig. 2.3 (a) Modulation circuits

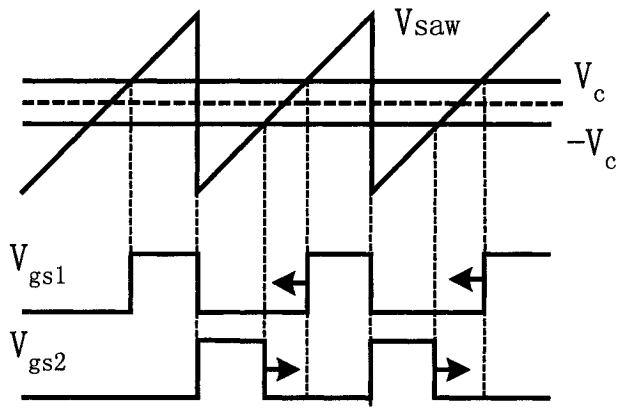



Fig. 2.3 (b) Key waveforms

Fig. 2.3 A DCS PWM modulation scheme

### 2.2.2 Principle of Operation

To simplify the analysis of operation, components are considered ideal except as indicated otherwise. The main operation modes are described as follows, and the main equivalent circuits for main operation modes are shown in Fig. 2.4.

***Mode 1*** *($t < t_1$)*: Initially, $S_1$ is conducting, and the input power is delivered to the output. $L_1$ is charged, and $L_2$ freewheels through $D_2$.

***Mode 2*** *($t_1 < t < t_2$)*: $S_1$ is turned off at $t = t_1$, causing the primary current $i_p$ to charge $C_1$ and discharge $C_2$. During the interval, the reflected secondary inductor current dominates the primary current $i_p$. Thus, $C_2$ may be discharged to zero at wide load range, which means wide ZVS range can be achieved for $S_2$.

***Mode 3*** *($t_2 < t < t_3$)*: When the voltage across $C_2$ is discharged to zero at $t = t_2$, the body diode of $S_2$ conducts to carry the current, which provides ZVS condition for switch $S_2$. During this period, leakage inductance is reset, and secondary current $i_1$ and $i_2$ freewheel through $D_1$ and $D_2$, respectively.

***Mode 4*** *($t_3 < t < t_4$)*: $S_2$ is turned on with ZVS at $t = t_3$; the primary current decreases to zero and then becomes negative. When the negative peak current is equal to the reflected $L_2$ current, the diode $D_2$ is blocked and the converter starts to deliver power to the output. The inductor $L_2$ is charged, and inductor $L_1$ current continues to freewheel.

***Mode 5*** *($t_4 < t < t_5$)*: $S_2$ is turned off at $t = t_4$, causing the primary current $i_p$ to charge $C_2$ and discharge $C_1$. When the secondary $D_1$ and $D_2$ start to freewheel, leakage inductance and junction capacitance of switches $S_1$ and $S_2$ start to oscillate on the primary side. During the interval, the body diodes may be involved, which worsen the ringing and results in reverse recovery losses. (The ringing waveforms are not shown in the Figure)

***Mode 6*** *($t_5 < t < t_6$)*: The oscillation comes to the end with equal voltage across switches $S_1$ and $S_2$. On the secondary side, $L_1$ and $L_2$ keep freewheeling. At $t = t_6$, $S_1$ is turned on again going back to Mode 1.

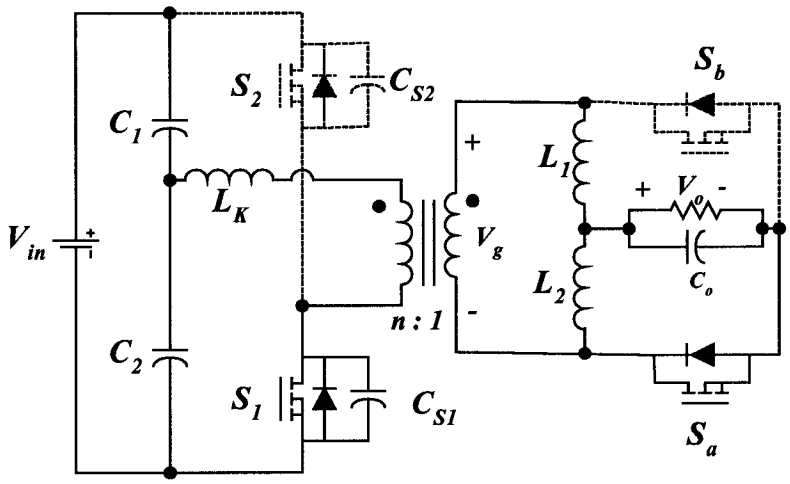



Fig. 2.4 (a) Mode 1

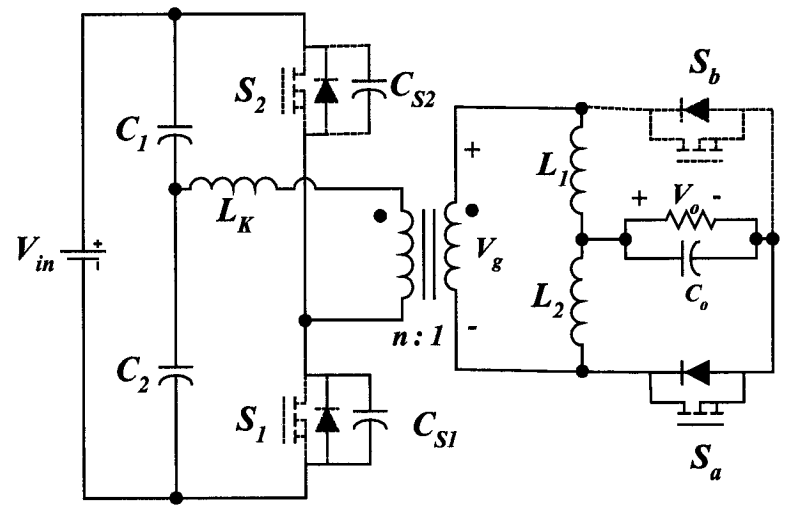



Fig. 2.4 (b) Mode 2

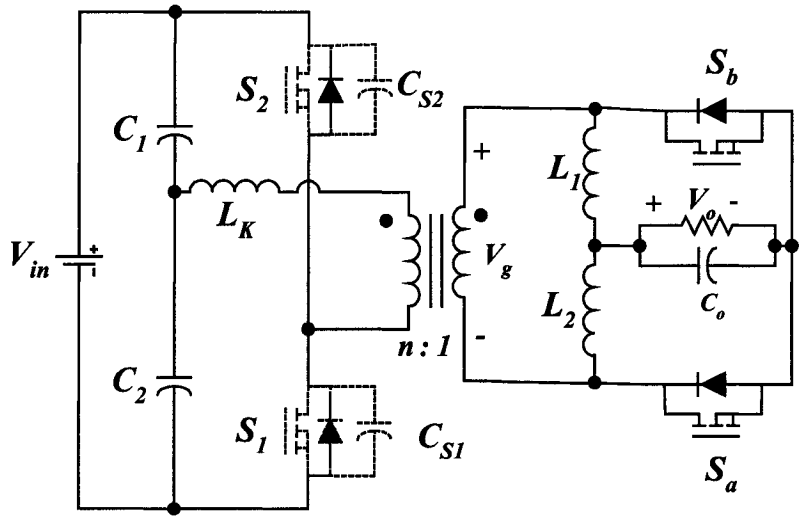



Fig. 2.4 (c) Mode 3

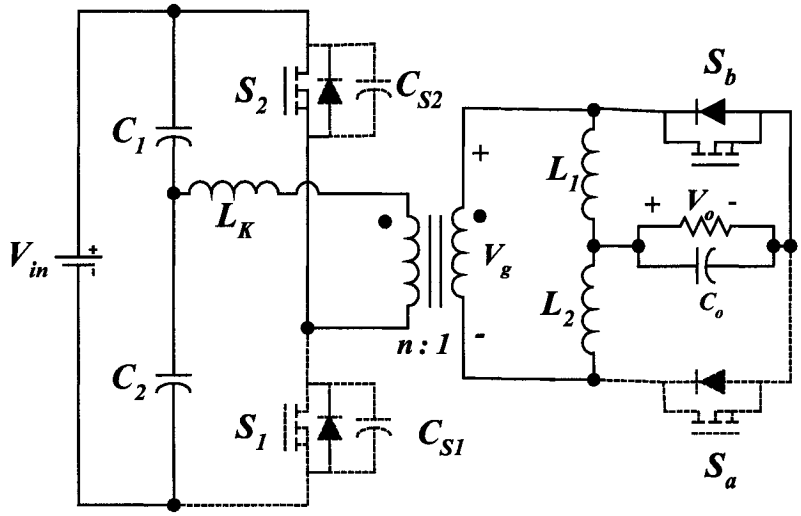



Fig. 2.4 (d) Mode 4

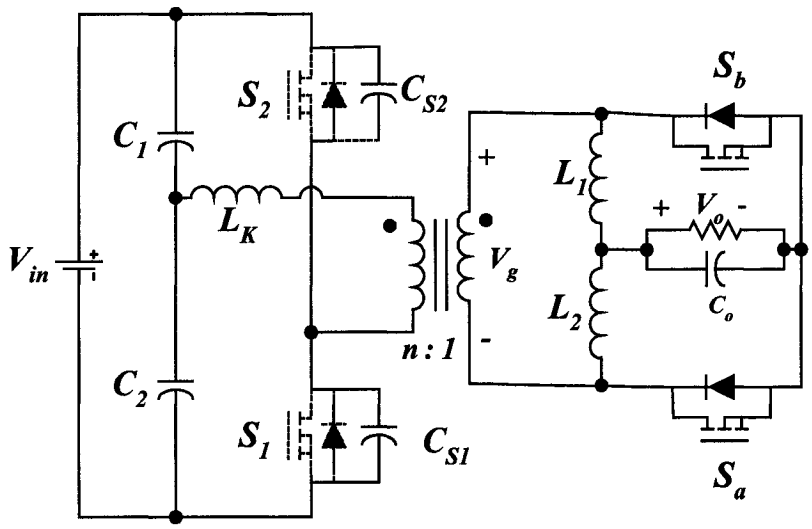



Fig. 2.4 (e) Mode 5

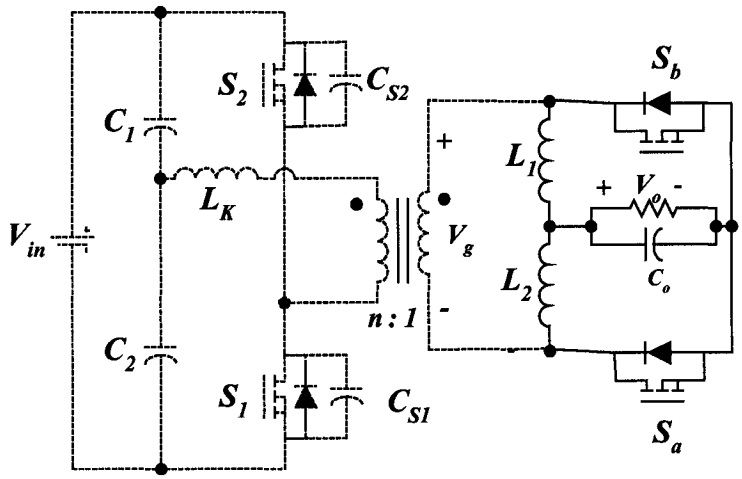



Fig. 2.4 (f) Mode 6

Fig. 2.4 Operation Modes Analysis

### 2.2.3 Main Features Compared with Symmetric and Asymmetric PWM Control

Compared with the conventional symmetric PWM control, DCS PWM controlled HB has the same voltage and current stresses in the primary switches. Although the

transformer voltage and current waveforms are different from those of the symmetric PWM control, the voltage-second value and magnetizing B-H loop of the transformer are identical. The peak and *rms* currents through the transformers are also the same for both schemes. Hence, there is no change in characteristics or design of the transformer from the symmetric PWM control to DCS PWM control.

On the secondary side, as shown in Fig. 2.2, even though the currents through the rectifiers have different waveforms in the two schemes, the peak and *rms* values of the waveforms are equal. Moreover, the inductors voltage-second value, current peak and current *rms* values are the same for both schemes. Therefore, the voltage and current stresses for the secondary-side switches and inductors are the same for both schemes. Consequently, there is no change in the components selection or converter design with the change of control scheme from symmetric PWM control to the proposed DCS PWM control.

As mentioned above, both symmetric PWM and DCS PWM have even voltage and current stresses in corresponding components due to the identical duty cycle width for the two switches. Hence, there are no asymmetric penalties in asymmetric PWM control, which allows DCS PWM control to be employed in applications for wide input voltage range. Furthermore, in the DCS PWM control, ZVS for switch $S_2$ is achieved without adding additional components. In addition, wide ZVS range operation may be achieved, because the secondary inductor current is reflected to transformer primary side to the discharge the output capacitor of switch $S_2$ to create ZVS condition for switch $S_2$. Because switching losses and transformer leakage-inductance-related losses are reduced, higher efficiency is expected with the DCS PWM control method.

A comparison between the asymmetric HB, symmetric HB and DCS HB under same design conditions is shown in Table 2.1, where N is the transformer turns ratio, D is the duty cycle of the switch $S_1$, $I_o$ is the load current, $V_{in}$ is the input voltage and $V_{out}$ is the output voltage. The filter inductance and output capacitance values are assumed large enough such that the inductor currents and output voltage are regarded as a constant current source and a constant voltage source, respectively. From Table 2.1, it can be observed that DCS HB has the same stress distribution as the symmetric HB, while asymmetric HB has asymmetric stress distribution, DC bias of the magnetizing current and nonlinear DC gain. These features make asymmetric HB unsuitable for applications with wide input voltage range.

In the DCS controlled HB converter, the current waveforms and values through inductors $L_1$ and $L_2$ are same as those of the symmetric HB converter. In the symmetric HB converter, the inductor current ripples are interleaved, thus the output current ripple cancellation is achieved in the whole duty cycle range ($0<D<0.5$). In other words, output current ripple is always smaller than individual inductor current ripple. However, in the DCS HB converter, the current cancellation is weakened due to the shifted duty cycle. Analysis shows that the current cancellation takes effect only at the duty cycle range of $0.33<D<0.5$, which means the current cancellation is lost at the duty cycle range of $0<D<0.33$.

Table 2.1 Comparisons of half bridge converters under several control schemes

| | Symmetric HB | Asymmetric HB | DCS HB |
|---|---|---|---|
| DC gains | $V_{out}=\frac{DV_{in}}{2N}$ | $V_{out}=\frac{D(1-D)V_{in}}{N}$ | $V_{out}=\frac{DV_{in}}{2N}$ |
| DC bias of magnetizing current | $I_{DC}=0$ | $I_{DC}=\frac{(1-2D)}{2}I_O$ | $I_{DC}=0$ |
| Stresses of switch $S_1$ | $V_{ds1}=V_{in}$<br>$Irms=\frac{I_o}{2N}\sqrt{D}$ | $V_{ds1}=V_{in}$<br>$Irms=\frac{I_o(1-D)\sqrt{D}}{N}$ | $V_{ds1}=V_{in}$<br>$Irms=\frac{I_o}{2N}\sqrt{D}$ |
| Stresses of switch $S_2$ | $V_{ds1}=V_{in}$<br>$Irms=\frac{I_o}{2N}\sqrt{D}$ | $V_{ds2}=V_{in}$<br>$Irms=\frac{I_oD\sqrt{1-D}}{N}$ | $V_{ds1}=V_{in}$<br>$Irms=\frac{I_o}{2N}\sqrt{D}$ |
| Stresses of rectifier $D_1$ | $V_{d1}=\frac{V_{in}}{2N}$<br>$Irms=\frac{I_o}{2}\sqrt{2D+1}$ | $V_{d1}=\frac{(1-D)V_{in}}{N}$<br>$Irms=I_o\sqrt{1-D}$ | $V_{d1}=\frac{V_{in}}{2N}$<br>$Irms=\frac{I_o}{2}\sqrt{2D+1}$ |
| Stresses of rectifier $D_2$ | $V_{d2}=\frac{V_{in}}{2N}$<br>$I_{rms}=\frac{I_o}{2}\sqrt{2D+1}$ | $V_{d1}=\frac{DV_{in}}{N}$<br>$I_{rms}=I_o\sqrt{D}$ | $V_{d2}=\frac{V_{in}}{2N}$<br>$I_{rms}=\frac{I_o}{2}\sqrt{2D+1}$ |

### 2.2.4 Experimental Verification of the Proposed DCS Concept

An experimental prototype with 3.3V/25A output and 36V~75V input voltage range was built in a laboratory to evaluate the proposed concept. Considering the low-voltage application, synchronous rectifiers are used instead of the rectifier diodes. For the experimental prototype, IRFS59N10D is used for switch $S_1$ and $S_2$, and Si4420DY is used for synchronous rectifiers. For comparison purpose, symmetric control and the proposed duty-cycle-shifted control are applied to the same power stage, respectively.

For duty-cycle-shifted control, the driving signals are generated using the modulation circuit described in Fig. 2.3, and considering that switch $S_2$ is turned *on* at zero voltage, an extra capacitor is paralleled with $S_2$ to reduce the turn-off losses. An RC snubber is paralleled with $S_1$ to damp the oscillation between leakage inductance and capacitance when $S_2$ is turned off. For symmetric control scheme, RC snubbers are used in parallel with $S_1$ and $S_2$, respectively.

Figure 2.5 shows the experimental waveforms of gate signals of switch $S_1$ and $S_2$ for duty-cycle-shifted control scheme. Fig. 2.6 shows the zero-voltage-switching waveforms of switch $S_2$. Fig. 2.7 shows the transformer primary voltage and current at full load in conventional symmetric half-bridge converter. It can be observed that there is significant ringing during the freewheeling period of time when both switches are off. By applying the DCS control to the half-bridge converter, the ringing and freewheeling frequency are reduced by half. The corresponding transformer primary voltage and current waveforms are shown in Fig. 2.8.

Fig. 2.9 through Fig. 2.12 show the efficiency comparison between conventional symmetric control and DCS control at switching frequencies of 100kHz, 200kHz, 300kHz and 400kHz, respectively. It is clear that the improvement in efficiency increases with the switching frequency, and at 400kHz, efficiency improvement is up to 1.6 percent. This is because switching losses and transformer leakage inductance related losses are proportional to the switching frequency.

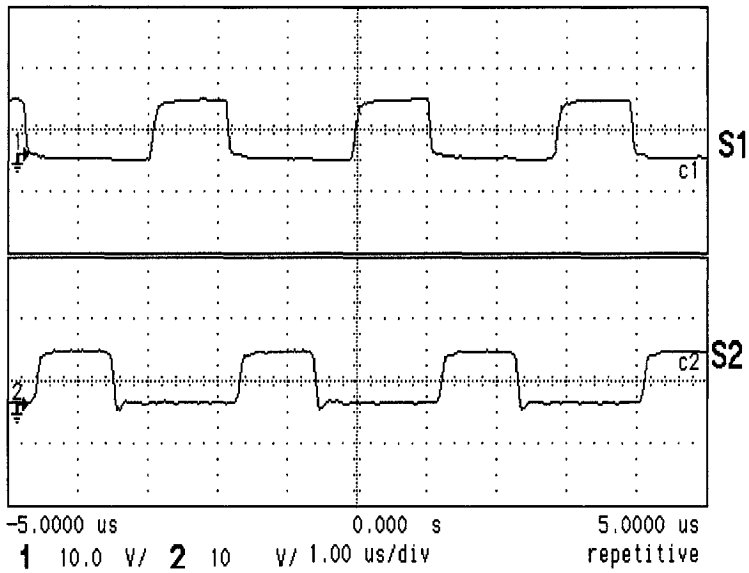



Fig. 2.5 Gate signals of $S_1$ and $S_2$

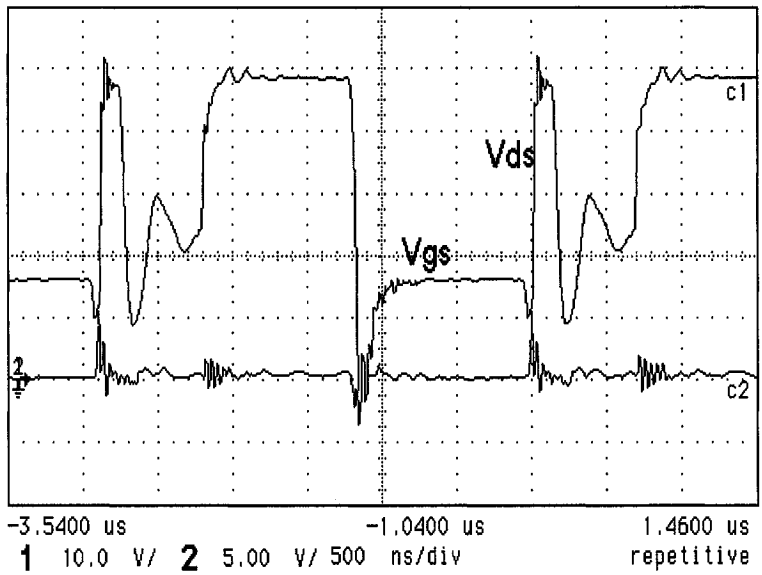



Fig. 2.6 Zero-voltage-switching of switch $S_2$

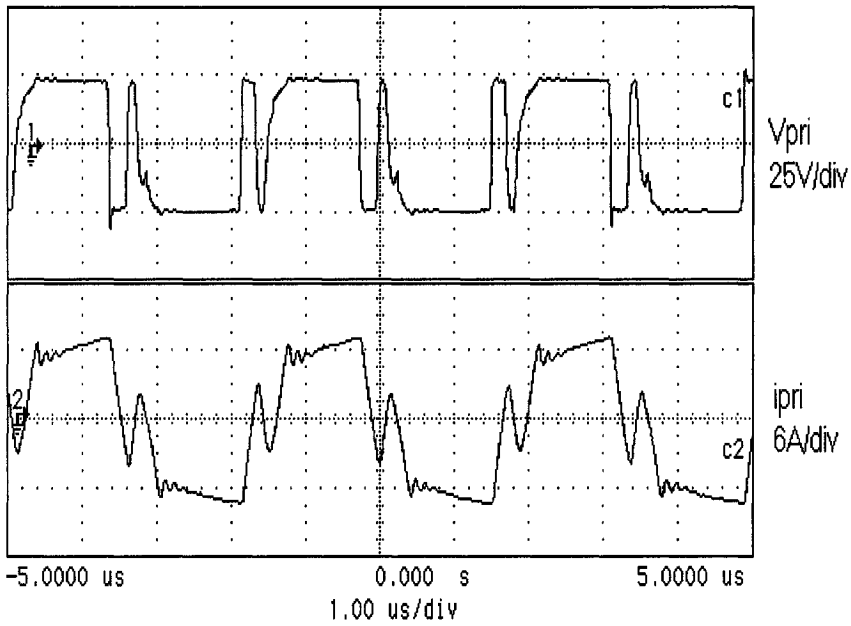



Fig. 2.7 Transformer waveforms of conventional symmetric control

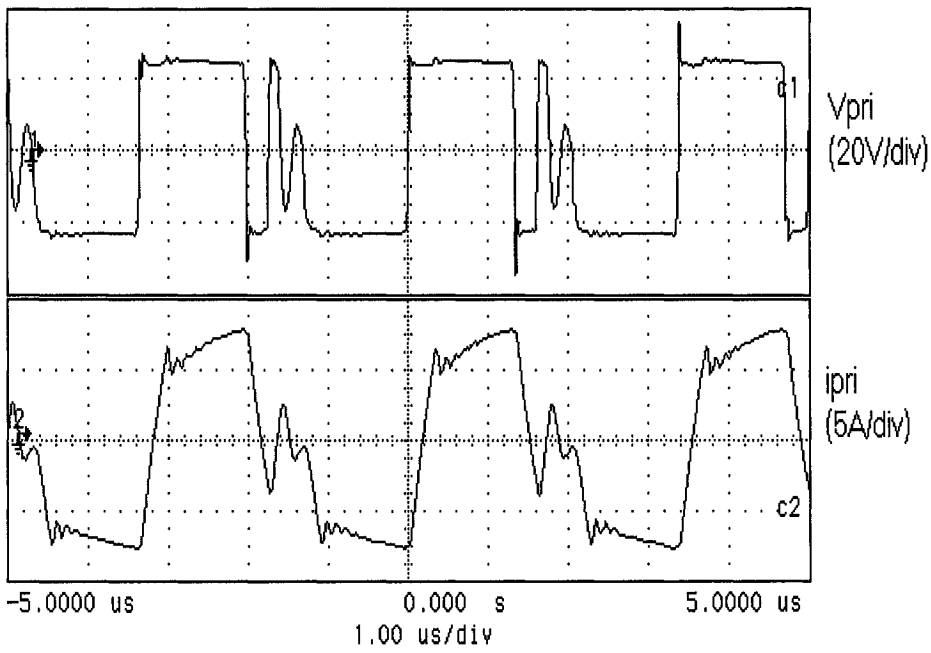



Fig. 2.8 Transformer waveforms of duty-cycle-shift control

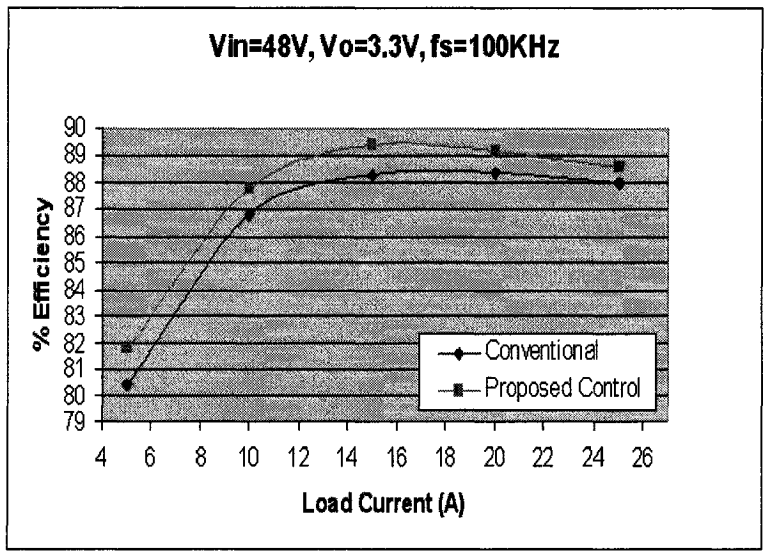



Fig. 2.9 Efficiency comparison at 100KHz

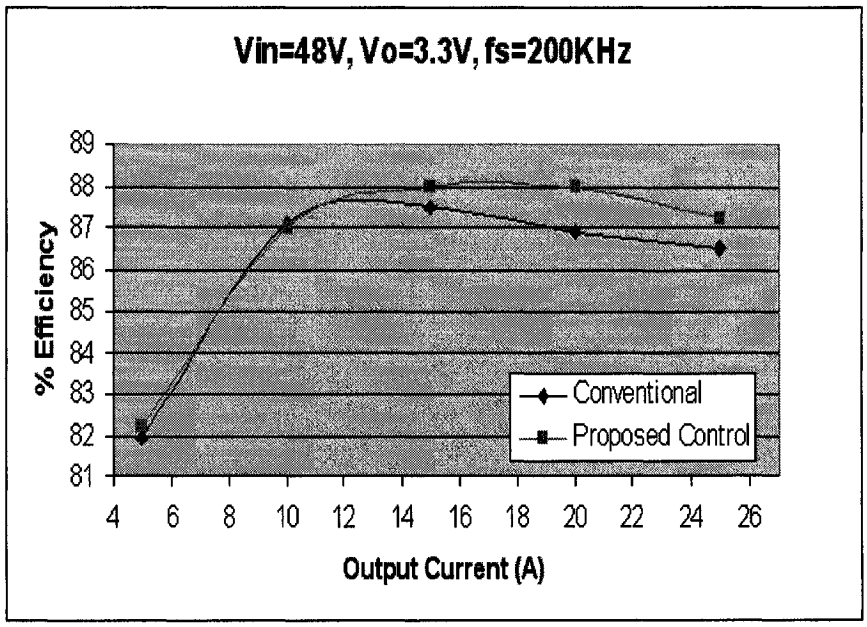



Fig. 2.10 Efficiency comparison at 200KHz

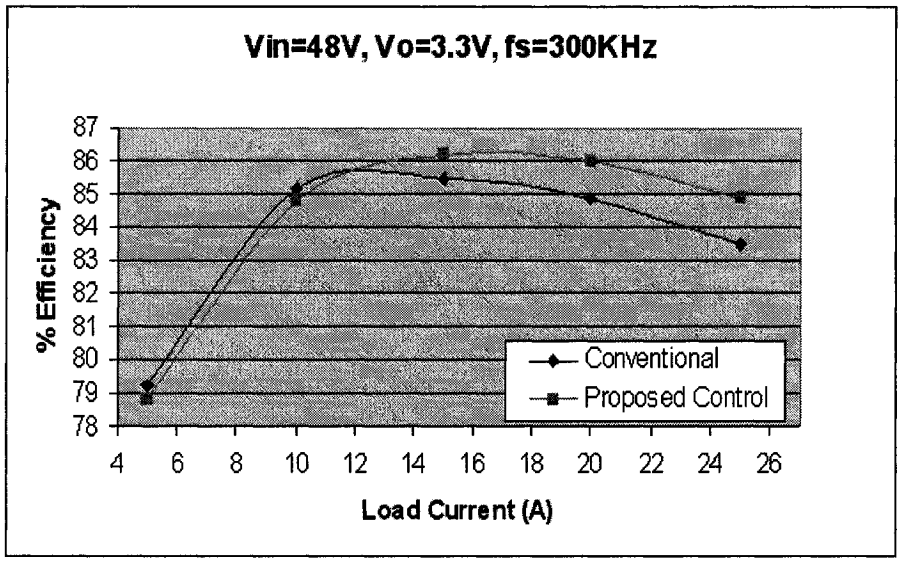



Fig. 2.11 Efficiency comparison at 300KHz

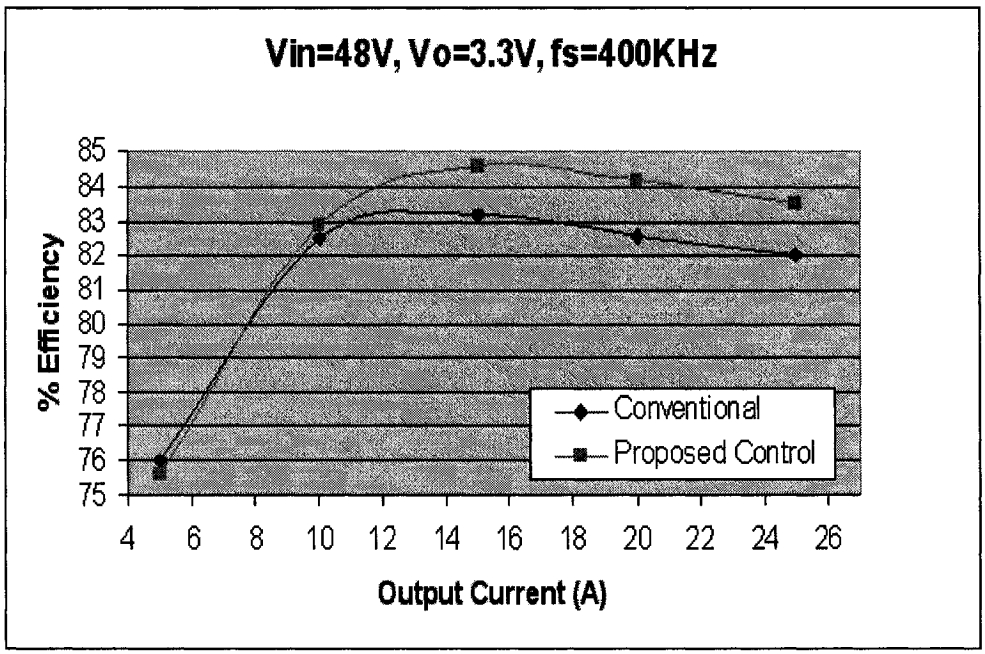



Fig. 2.12 Efficiency comparison at 400KHz

### 2.2.5 Summary

A simple and effective PWM control method known as Duty-Cycle-Shift (DCS) control method was proposed to reduce switching losses and transformer-leakage-inductance-related losses in the half-bridge DC-DC converter topology. Using this proposed scheme and by shifting one of the symmetric PWM driving signals, Zero-Voltage-Switching (ZVS) is achieved for one of the switches without adding extra components and without adding asymmetric penalties of the complementary duty cycle control. This control concept reduces the switching losses and transformer leakage-inductance-related losses. These losses significantly degrade the converter efficiency, especially when operating in high switching frequencies. Moreover, two modulation schemes to generate the required driving signals were also presented.

Experimental results showed that the proposed control scheme improves the efficiency up to 1.6 percent at 400kHz switching frequency when compared to the conventional symmetric PWM control. Efficiency improvement is expected at higher switching frequencies.

## 2.3 Zero-Voltage-Switching DCS Half-Bridge DC-DC converter

In Section 2.2, a DCS concept was presented. Applying this concept to conventional half-bridge DC-DC converter topology, one of two primary switches achieves Zero-Voltage-Switching (ZVS) and leakage-inductance-related ringing is partially eliminated. In this section, based on DCS concept, a new ZVS half-bridge DC-DC topology is proposed to achieve full soft switching for all primary-side switches.

### 2.3.1 Proposed Topology and Control

As described in the previous section, the ZVS of switch $S_2$ is achieved by using the DCS PWM control concept. However, switch $S_1$ still operates at hard-switching condition and half of the ringing exists during the freewheeling period of time. To solve these problems, a new ZVS topology is proposed as shown in Fig. 2.13, where $L_k$ is the transformer leakage inductance, $C_1$, $C_2$ and $C_3$ can be external capacitors or junction parasitic capacitance of the associated MOSFETs, and $C_4$ is the external capacitor across the diode $D_3$. The key waveforms of the proposed topology are shown in the Fig. 2.14.

Basically, energy stored in the leakage inductance can be employed to discharge junction capacitance to achieve ZVS. However, in a conventional half-bridge converter, during the freewheeling period of time, the energy in the leakage inductance cannot be stored. The only way to store energy in an inductor is to short the inductor and let the inductor freewheel through a low resistance path. In fact, by shorting the transformer primary side in the phase-shift full-bridge converter, the leakage inductance energy is trapped for ZVS.

According to the same "trapping" concept, auxiliary switch $S_3$ and diode $D_3$ are added in the conventional half-bridge converter to provide a path for the leakage inductance current during the period when both $S_1$ and $S_2$ are off (off-time interval). In other words, leakage inductance energy is trapped via the added path during the off-time interval until it is needed. As shown in Fig. 2.14, before $S_1$ is turned on, $S_3$ is turned off to release the trapped energy in the leakage inductance to discharge the output capacitances of switches to create ZVS for switch $S_1$.

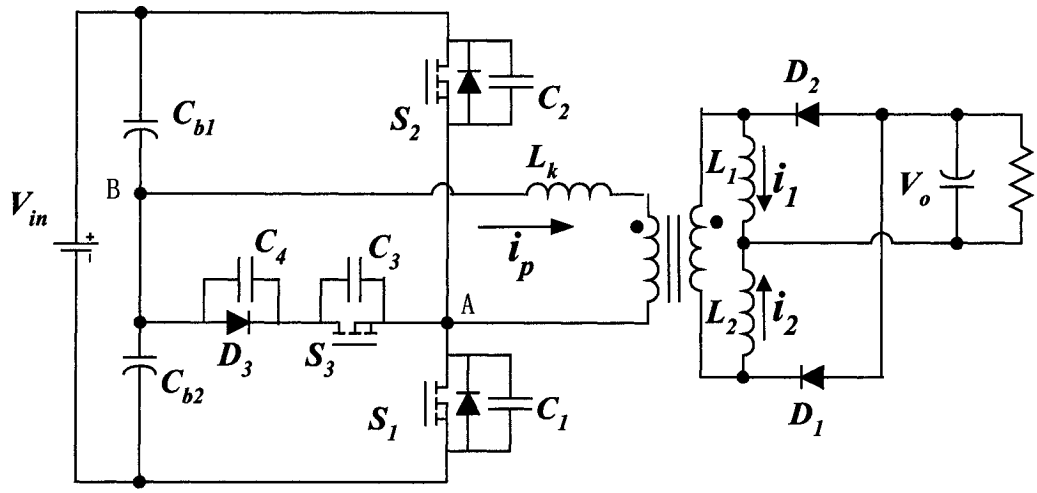



Fig. 2.13 Proposed DCS controlled ZVS half-bridge converter

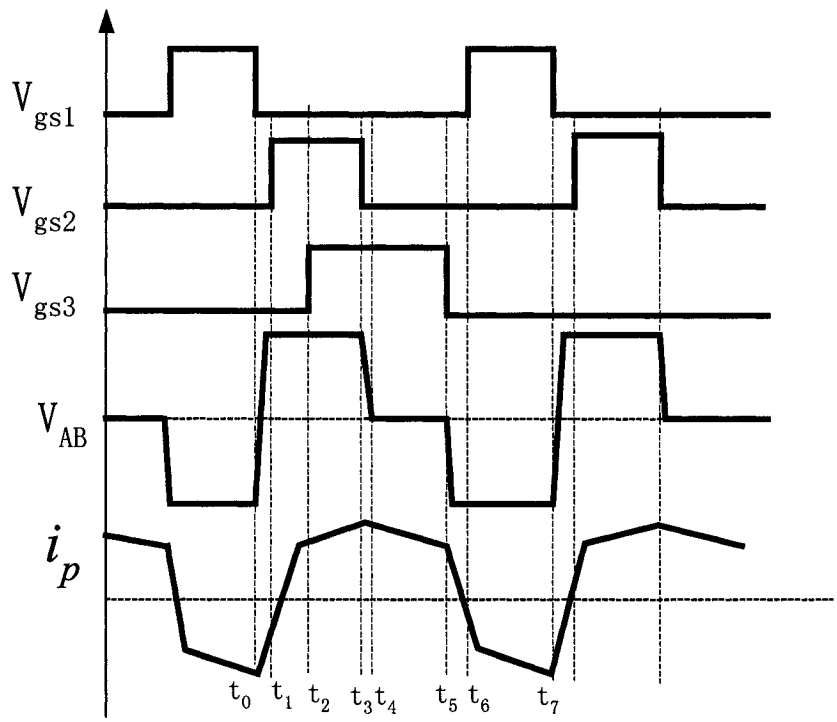



Fig. 2.14 Key waveforms of the proposed ZVS half-bridge converter

### 2.3.2 Principal of Operation

To simplify the analysis of operation, components are considered ideal except as indicated otherwise. The main equivalent circuits for main operation modes are shown in Fig. 2.15.

***Mode 1*** ($t_0 < t < t_1$): Before this mode, $t < t_0$, $S_1$ was turning on and the transformer delivers power to the output. At $t = t_0$, $S_1$ is turned off, causing the current $i_p$ to charge $C_1$ and $C_4$ and discharge $C_2$ and $C_3$.

***Mode 2*** ($t_0 < t < t_1$): When the $C_3$ voltage is discharged to zero, the body diode of switch $S_3$ conduct to continually charge $C_4$. Then, the voltage across $C_2$ is discharged to zero, and the body diode of $S_2$ conducts to carry the current, which provides ZVS condition for the switch $S_2$. During this interval, inductor current $i_1$ and $i_2$ freewheel through $D_2$ and $D_1$, respectively.

***Mode 3*** ($t_1 < t < t_3$): $S_1$ is turned on with ZVS at $t = t_1$, and the transformer leakage inductance current is reset to zero and reverse-charged. When the transformer primary current reaches the reflected current of $i_2$, diode $D_1$ is locked and the inductor $L_2$ starts to charge. At $t = t_2$, switch $S_3$ is turned on with zero voltage and zero current, i.e. ZVZCS.

***Mode 4*** ($t_3 < t < t_4$): At $t = t_3$, $S_2$ is turned off, the primary transformer current discharges $C_1$ and $C_4$ while charging $C_2$.

***Mode 5*** ($t_4 < t < t_5$): At $t = t_4$, the voltage across $C_4$ is discharged to zero forcing the leakage inductance current to flow through $D_3$ and $S_3$. During this interval, the leakage inductance current freewheels through $D_3$ and $S_3$ such that the energy in the leakage inductance is trapped. On the secondary side, inductor $L_1$ and $L_2$ currents freewheel through $D_2$ and $D_1$, respectively.

***Mode 6*** ($t_5 < t < t_6$): At $t = t_5$, $S_3$ is turned off, causing $C_2$ and $C_3$ to be charged and $C_1$ to be discharged by the leakage inductance current.

***Mode 7*** ($t_5 < t < t_6$): When the voltage across $C_1$ is discharged to zero, the body diode of $S_1$ conducts to recycle the energy in the transformer leakage inductance.

***Mode 8*** ($t_6 < t < t_7$): At $t = t_6$, $S_1$ is turned on with ZVS, and then the leakage inductance current is reset to zero and reverse-charged. When the transformer primary current increases to the reflected current of $i_1$, $D_2$ is blocked and the converter starts to deliver power to the output.

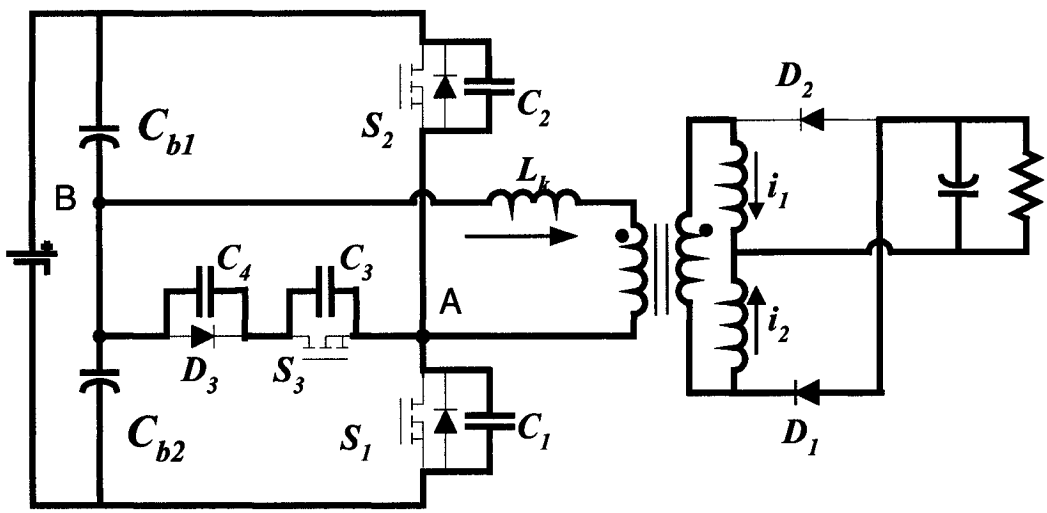



Fig. 2.15 (a) Mode 1

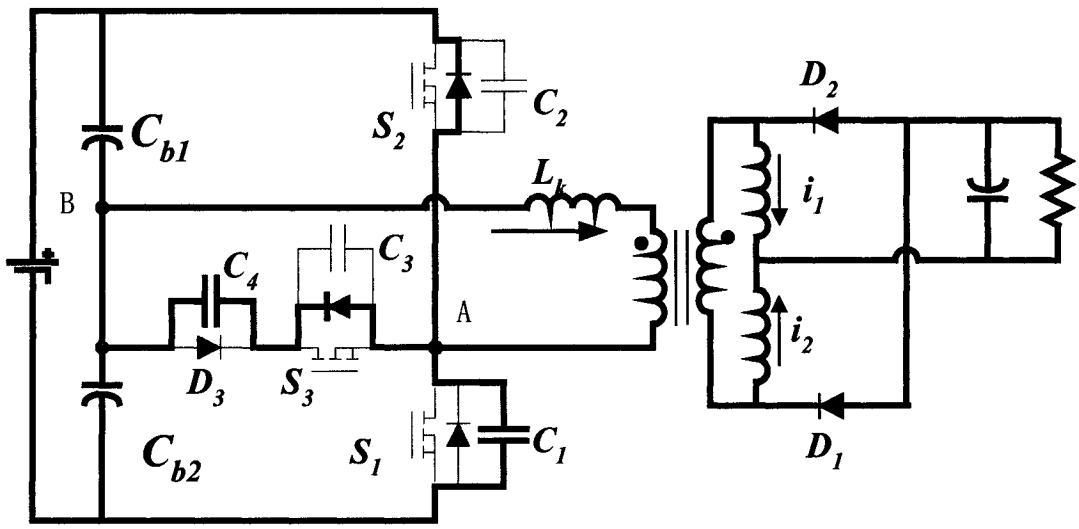



Fig. 2.15 (b) Mode 2

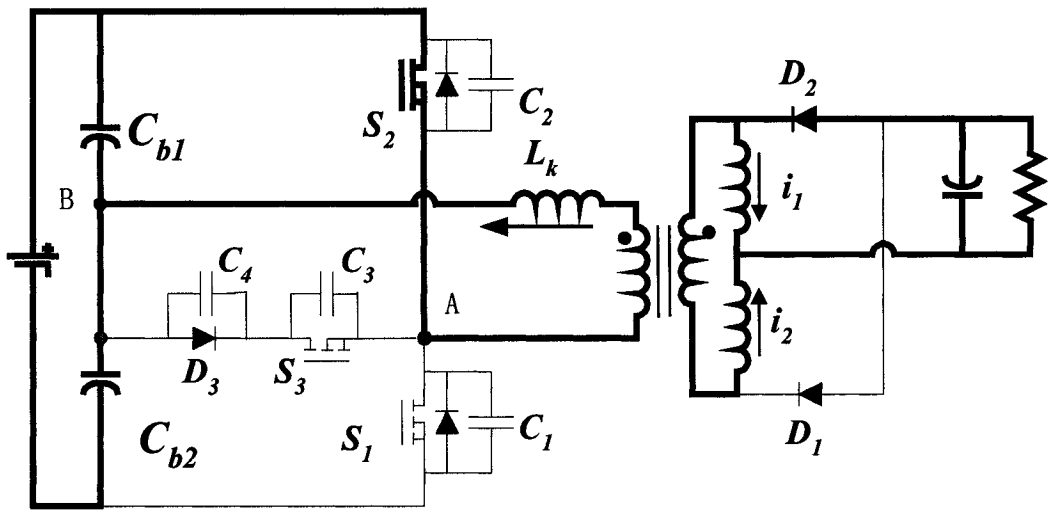



Fig. 2.15 (c) Mode 3

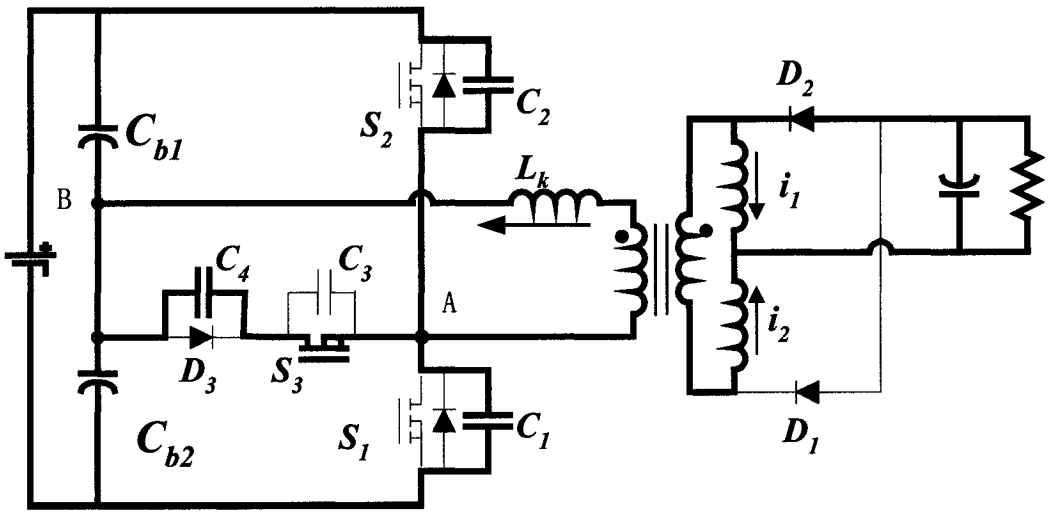



Fig. 2.15 (d) Mode 4

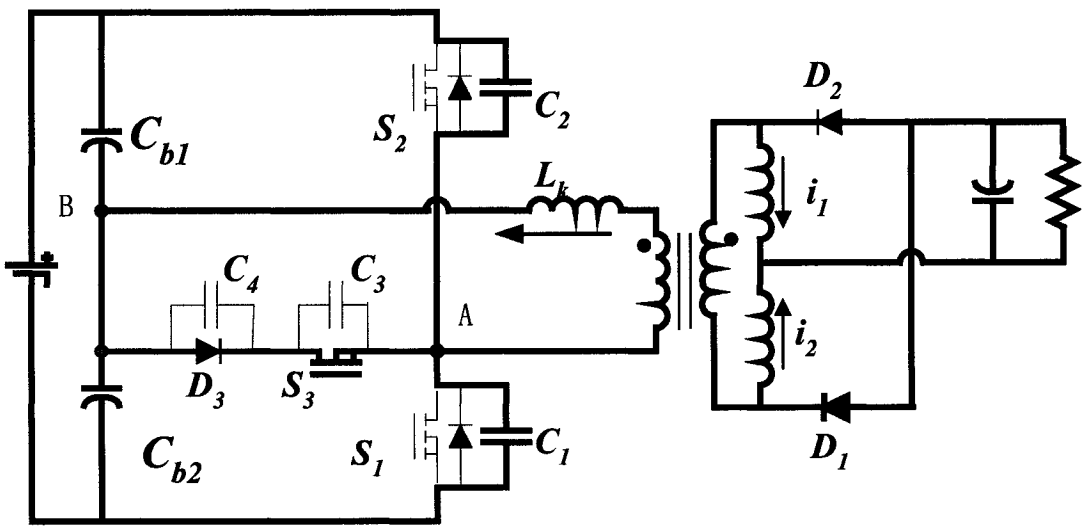



Fig. 2.15 (e) Mode 5

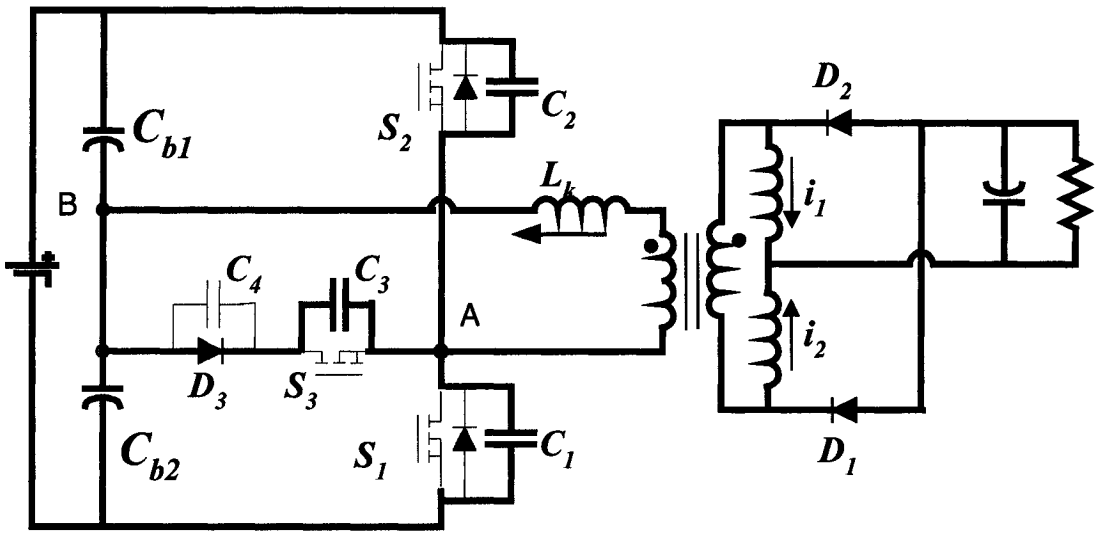



Fig. 2.15 (f) Mode 6

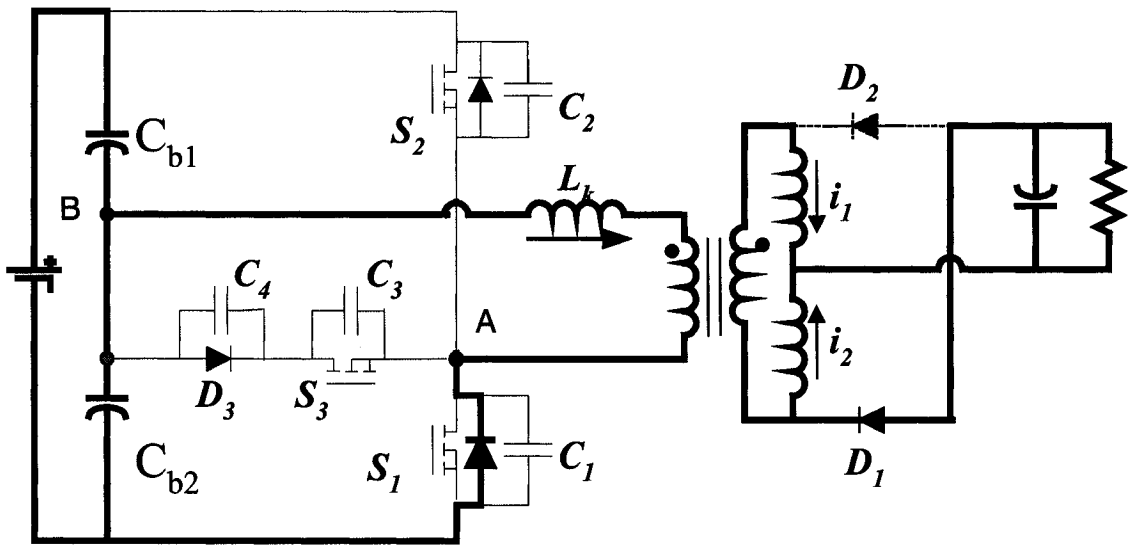



Fig. 2.15 (g) Mode 7

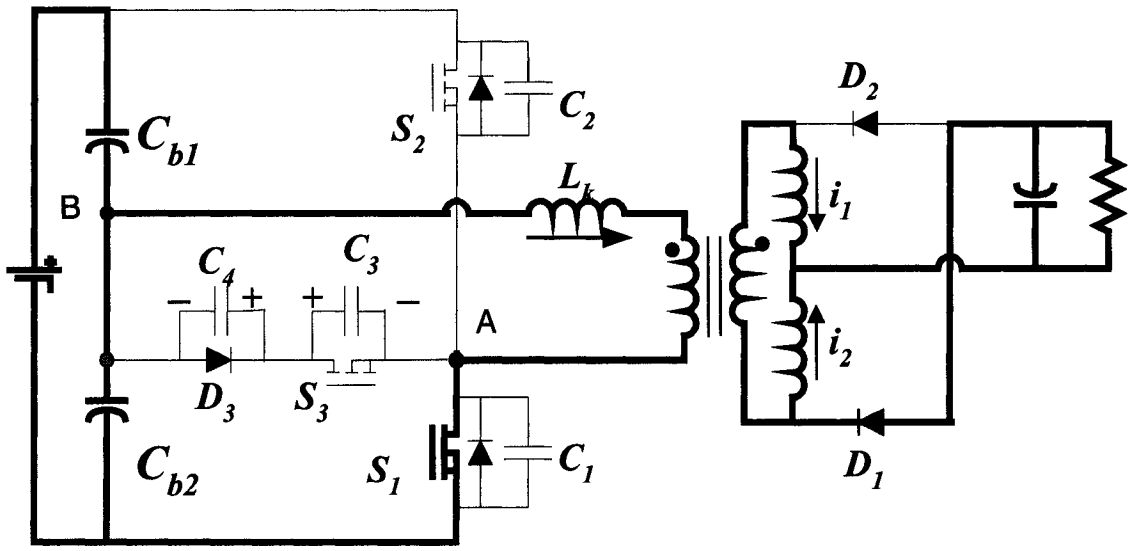



Fig. 2.15 (h) Mode 8

Fig. 2.15 Operation mode analysis

### 2.3.3. Features of the Proposed Topology

#### 2.3.3.1 Generation of Driving Signals

Driving signals of switch $S_1$ and $S_2$ are generated as discussed in Chapter 2.2 for the DCS PWM modulation method and as shown in Fig. 2.3. The timing of the driving signal for switch $S_3$ is not critical due to the fact that switch $S_3$ may be turned on at any time during the interval when switch $S_2$ is on. Driving signal for switch $S_3$ is simply obtained only by inverting the driving signal of switch $S_1$ and adding some delay time at the rising edge.

#### 2.3.3.2 Voltage and Current Stresses

With DCS PWM control, the duty cycle width of the two half-bridge main switches are identical, and the voltage across the two leg-capacitors are equal. Thus, all voltage

and current stresses in the corresponding components are evenly distributed. The asymmetric problems incurred with complimentary PWM control are eliminated. Concerning the voltage and current stresses in auxiliary switch $S_3$ and diode $D_3$, the voltage stresses are only half that of the main switches, and the current stresses are the same as those of the main switches. It is noted that there is no reverse recovery problem for the diode $D_3$, and that switch $S_3$ operates at ZVZCS turn-on and nearly ZVS turn-off.

#### 2.3.3.3 ZVS Range for Main Switch $S_1$ and $S_2$

In the phase-shifted full-bridge converter, the load current reflected to the primary side is used to achieve the ZVS for the leading-leg switches [B3]. Similarly, in the proposed topology, the reflected secondary inductor current may be used to achieve ZVS of switches. Specifically, the ZVS of switch $S_2$ is achieved by the same manner as that of the leading-leg switches in the phase-shift full-bridge converter, thus the realization of ZVS is easy to obtain. However, the ZVS behavior of switch $S_1$ is not exactly the same as that of lagging-leg switches in the phase-shift full-bridge converter. The ZVS range equation for two topologies is compared as follows:

In a full-bridge converter, in order to achieve ZVS of lagging-leg switches, the energy stored in the leakage inductance has to be large enough to charge and discharge output capacitance [3]. Neglecting the transformer winding capacitance, the energy stored in the leakage inductance $L_k$ has to satisfy [B3]:

$$E = \frac{1}{2} L_k I_p^2 \geq \frac{1}{2} (C_1 + C_2) V_{in}^2 \qquad (2\text{-}1)$$

Where, $I_p$ is the current through the transformer primary winding at the time when one of the lagging switches is turned off and $C_1$ and $C_2$ are the output capacitance across the switches, respectively.

Assuming C1 = $C_2$ = C, it follows that:

$$E = \frac{1}{2} L_k I_p^2 \geq C V_{in}^2 \qquad (2\text{-}2)$$

In the proposed topology, when switch $S_2$ is turned off, reflected secondary inductor current discharges $C_1$ and $C_4$ and charges $C_2$ until:

$$v_{c1} = v_{c2} = \frac{V_{in}}{2} \text{ and } v_{c4} = 0 \qquad (2\text{-}3)$$

For this interval, because the primary current is the reflected output current, equation (2-3) is easily satisfied in a wide load range. After the freewheeling mode, switch $S_3$ is turned off, and the energy stored in the transformer leakage inductance is released to continue discharging $C_1$ and charging $C_2$ and $C_3$. In order to achieve ZVS for $S_1$, the energy in the leakage inductance $L_k$ has to satisfy:

$$E = \frac{1}{2} L_k I_p^2 \geq \frac{1}{8} V_{in}^2 (C_1 + C_2 + C_3) \qquad (2\text{-}4)$$

Where, $C_3$ is the junction capacitance of switch $S_3$. Assuming $C_1 = C_2 = C_3 = C$, it follows that:

$$E = \frac{1}{2} L_k I_p^2 \geq \frac{3}{8} C V_{in}^2 \qquad (2\text{-}5)$$

Comparing equation (2-2) and (2-5), it is assumed that output capacitances across the switches in the proposed converter is equal to those of the full bridge and that the energy stored in the leakage inductance is equal for the two topologies. The ZVS of switch $S_1$ in the proposed topology is more easily achieved than that of the lagging-leg switches in the full bridge.

2.3.3.4 ZVS and ZCS behavior of the switch $S_3$

Concerning the switching behavior of switch $S_3$, the ZVS of the switch $S_3$ depends on the capacitance of $C_3$ and $C_4$. In the analysis, it is assumed:

$$V_{cb1} = V_{cb2} = \frac{V_{in}}{2} \tag{2-6}$$

In Mode 8, shown in Fig. 2.14, the voltages across $C_3$ and $C_4$ are:

$$V_{c3} = \frac{V_{in}}{2}; V_{c4} = 0 \tag{2-7}$$

After $S_1$ is turned off, the capacitor $C_3$ is discharged, and capacitor $C_4$ is charged as shown in Mode 1 of Fig. 2.14. Because $C_3$ and $C_4$ are in series, the voltage across $C_3$ is:

$$v_{c3}(t) = \frac{V_{in}}{2} - \frac{1}{C_3}\int i_c dt \tag{2-8}$$

The voltage across $C_4$ is:

$$v_{c4}(t) = \frac{1}{C_4}\int i_c dt \tag{2-9}$$

It can be noted that the voltage $v_{c3}$ is discharged to zero, if the following inequality is satisfied:

$$v_{c4}(t) \le \frac{V_{in}}{2} \tag{2-10}$$

Then, the body diode of switch $S_3$ conducts to carry the current to charge $C_4$ continually until:

$$V_{c4}(t) = \frac{V_{in}}{2} \tag{2-11}$$

After that, the voltage across $C_4$ is clamped at the half of the input voltage, and the $C_3$ voltage keeps zero, thus the switch $S_3$ may be turned on at zero voltage. From equation (2-8) through (2-10), the ZVS condition for the switch $S_3$ can be derived as:

$$C_4 \geq C_3 \tag{2-12}$$

To achieve ZVS, an extra capacitor is added across the diode $D_3$. When $S_3$ is turned on at ZVS also, there is no current flowing through the switch $S_3$, thus Zero-Voltage Zero-Current Switching (ZVZCS) is achieved for the switch $S_3$.

### 2.3.4. Experimental Verification of Proposed Topology

An experimental prototype with 3.3V/25A output and 36V~75V input voltage was built in the laboratory to evaluate the proposed DCS PWM control and ZVS topology. For comparison, the symmetric PWM control and DCS PWM control are separately applied to the same conventional half-bridge prototype as shown in Fig. 2.1, and the DCS PWM control is applied to the proposed ZVS half-bridge topology shown in Fig. 2.4. Because of the low output voltage, synchronous rectifiers were used instead of the rectifier diodes in the converter. To make the comparison fair, closed-voltage-loop control is employed to tightly regulate the output voltage. In the prototype, IRFS59N10D is used for switch $S_1$ and $S_2$, 30CTQ060S is selected for $D_3$, Si4470EY is used for $S_3$ and Si4420DY is used for the synchronous rectifiers. The transformer turns ratio is 4:2 and the measured primary-side leakage inductance is 180nH.

Fig. 2.16 shows the experimental gate signals of the switches $S_1$, $S_2$ and $S_3$. Fig. 2.17 shows the transformer primary voltage and current waveforms. Clean waveforms are observed, since the leakage inductance ringing is clamped.

Fig. 2.18 shows the gate signal and the drain-to-source voltage waveforms of switch $S_1$. It is clear that switch $S_1$ turns on at zero voltage. Fig. 2.19 shows gate signal and

drain-to-source voltage waveforms of switch $S_2$. It is clear that switch $S_2$ turns on at zero voltage switching. ZVS waveforms of switch $S_3$ can be observed in Fig. 2.20.

As the experimental verification, all primary-side switches operate at ZVS condition, and the leakage-inductance-related ringing and reverse recovery losses in the primary side are almost eliminated. Therefore, higher efficiency and an ability to operate at higher switching frequency are expected with the DCS PWM control and the proposed DCS-PWM-control based ZVS topology.

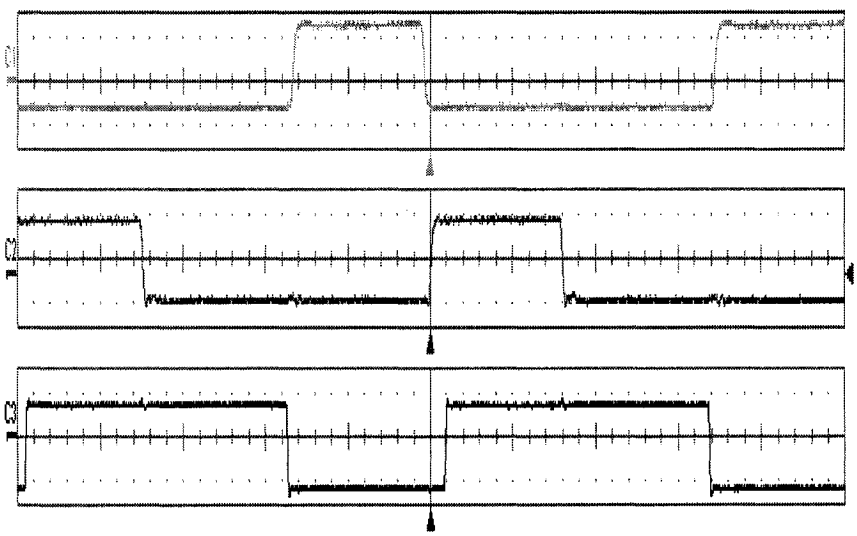


Fig. 2.16 Gate drive signals of switch $S_1$, $S_2$ and $S_3$

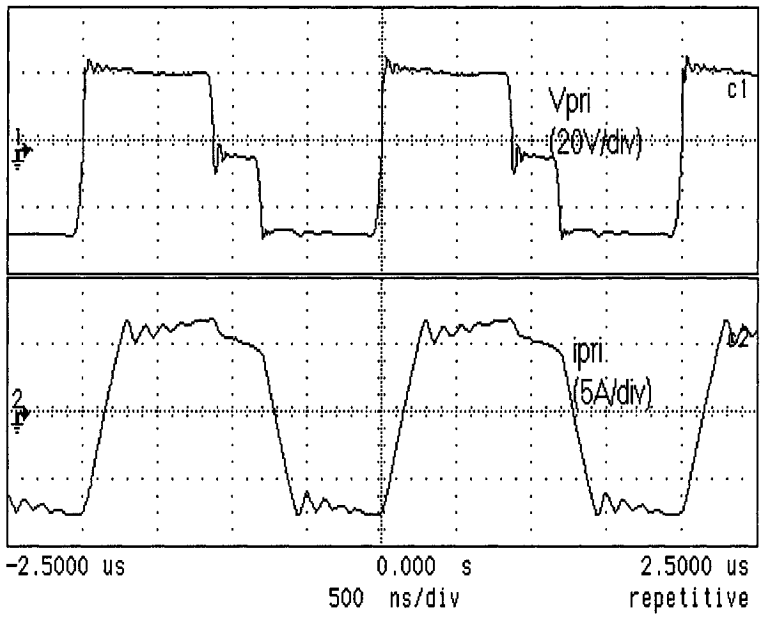



Fig. 2.17 Transformer voltage and current

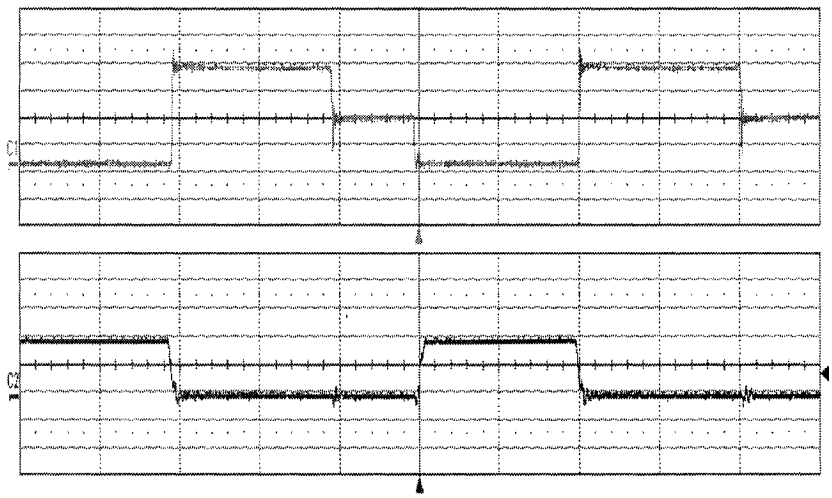


Fig. 2.18 ZVS waveforms of the switch $S_1$

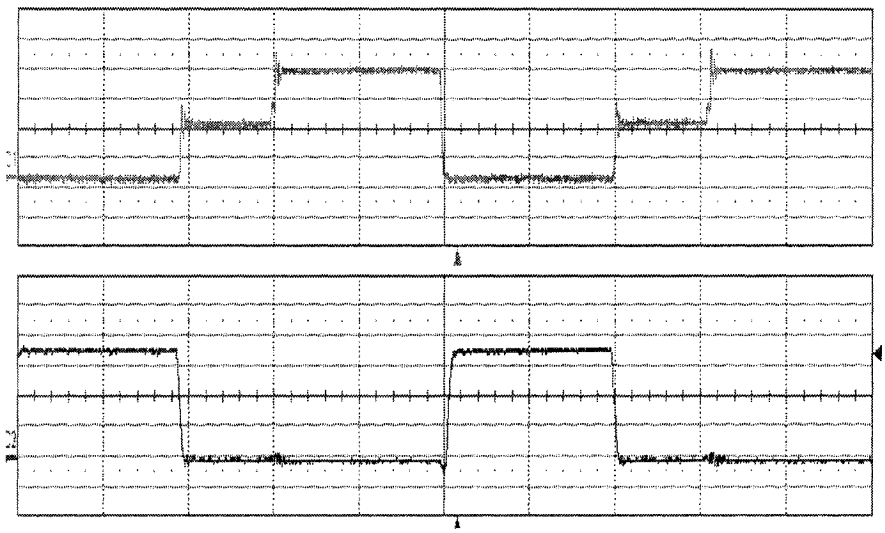


Fig. 2.19 ZVS waveforms of switch $S_2$

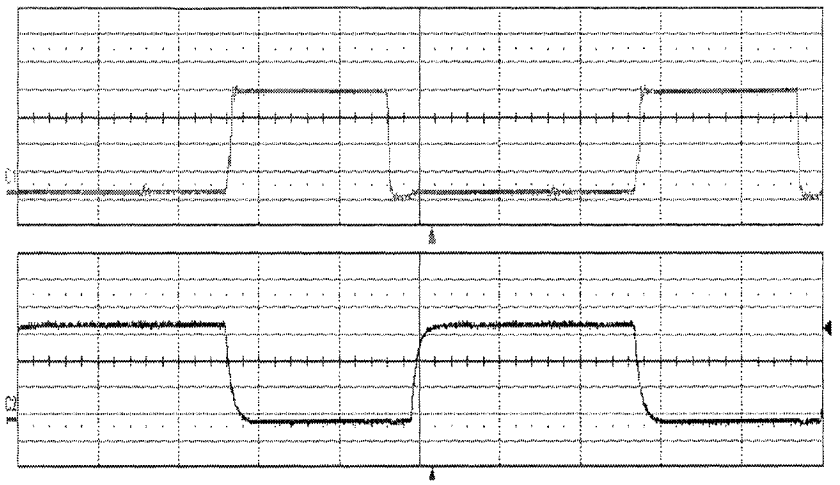


Fig. 2.20. ZVS waveforms of switch $S_3$

The efficiency values were measured for three experimental cases: conventional half bridge with symmetric PWM control, conventional half bridge with DCS PWM control, and the proposed ZVS topology with DCS-PWM control. Fig. 2.21 and Fig. 2.22 show the efficiency comparison curves at 200kHz and 400kHz switching frequencies, respectively. From these figures, it can be observed that the DCS PWM control improves the efficiency of conventional half bridge converter, and the DCS-PWM-based ZVS half

bridge topology further improves the efficiency. With the increase in switching frequency, efficiency improvement becomes more significant. At 400kHz switching frequency, the efficiency of the DCS-PWM-based ZVS half bridge topology is 4 percent higher than that of the symmetric PWM controlled half-bridge converter. This is because switching losses and leakage-inductance-related losses in a conventional half bridge are positively proportional to switching frequency. In the proposed ZVS half bridge, the losses were almost eliminated. Hence, the DCS-PWM-based ZVS topology is a good candidate for higher frequency applications.

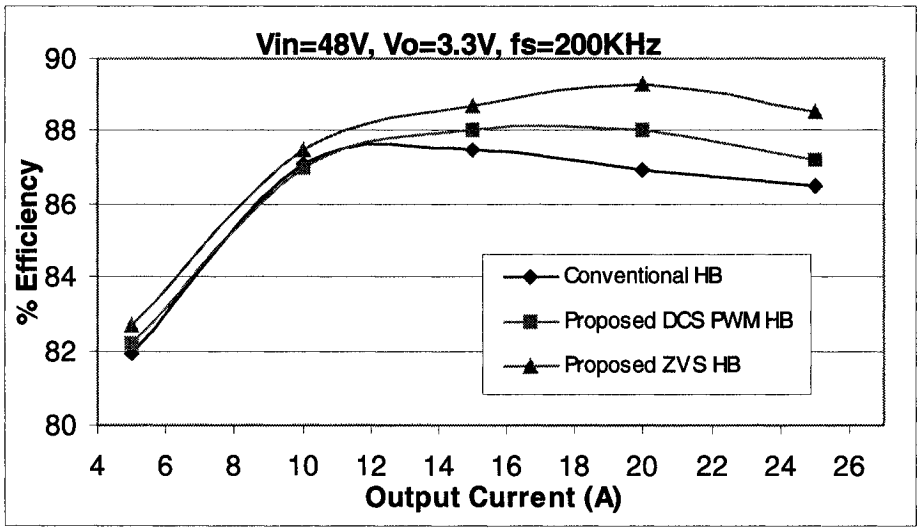



Fig. 2.21 Efficiency comparison at the switching frequency of 200kHz

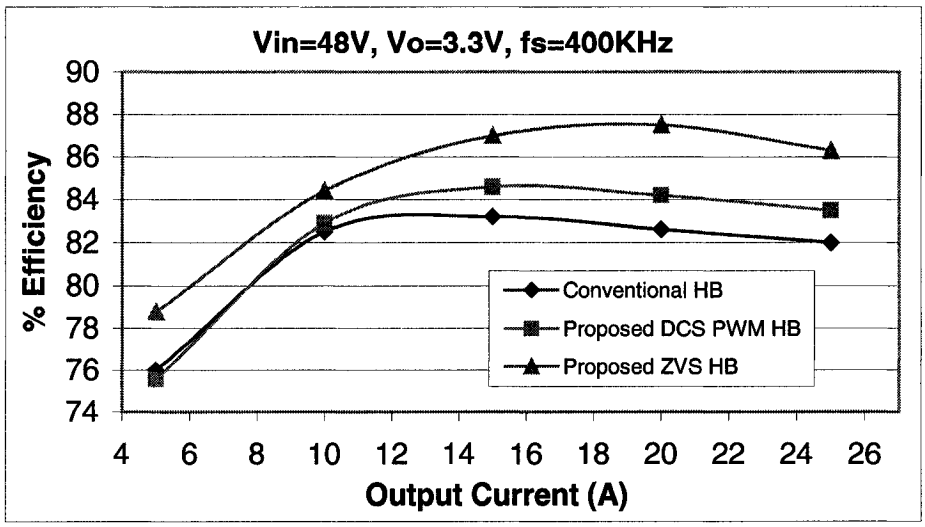



Fig. 2.22 Efficiency comparison at the switching frequency of 400kHz

### 2.3.5. Test Results of the Developed Industry Demo Prototype

In the previous sections, the experimental results are based on the prototypes developed in the university lab. Because of the limited facilities, the overall prototype performance is not good enough. A 1V/50A industry prototype was developed based on the DCS concept, wherein multiplayer and planner magnetics techniques were utilized, and the prototype is well optimized now. Some experimental results are shown in this section.

Fig. 2.23 shows photos of the prototype. Fig. 2.24 through Fig. 2.27 show the experimental waveforms, and clean waveforms can be seen in those figures. Fig. 2.28 shows the prototype efficiency curves, where high efficiencies are achieved. Fig. 2.29 shows the overall power loss, and the thermal picture is shown in Fig. 2.30. From test results above, it can be seen that the prototype has extremely high efficiency and good thermal management.

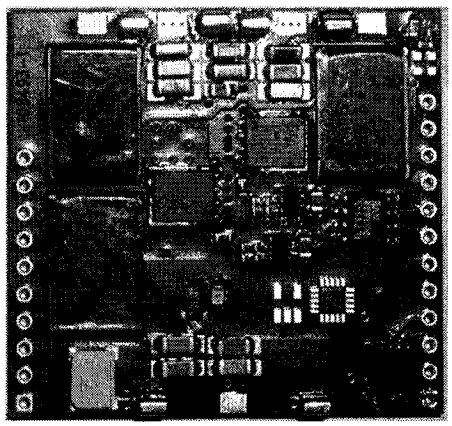


Fig. 2.23 (a) Bottom

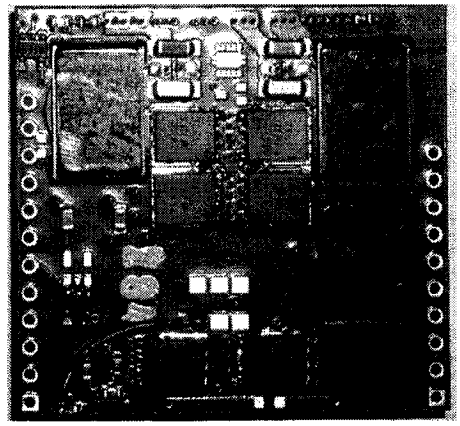


Fig. 2.23 (b) Top

Fig. 2.23 Photos of the prototype

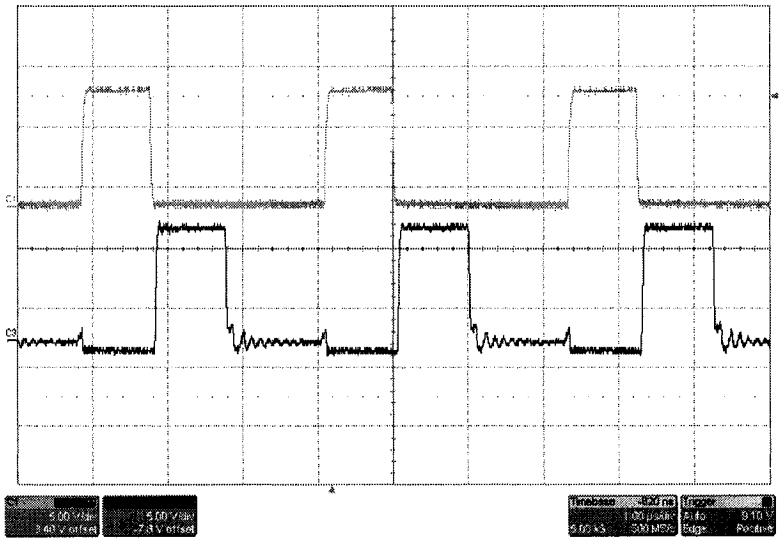


Fig. 2.24 Gate drive voltage waveforms of primary switches

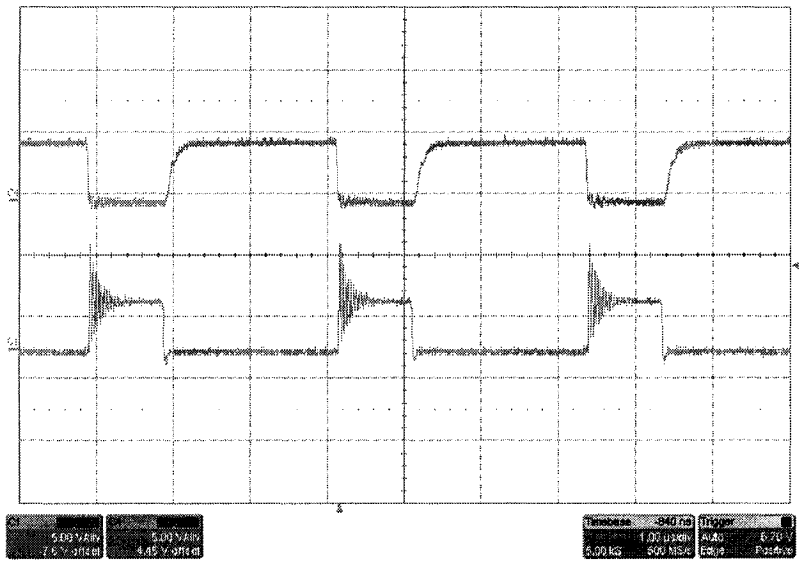


Fig. 2.25 Waveforms of SR gate and $V_{ds}$

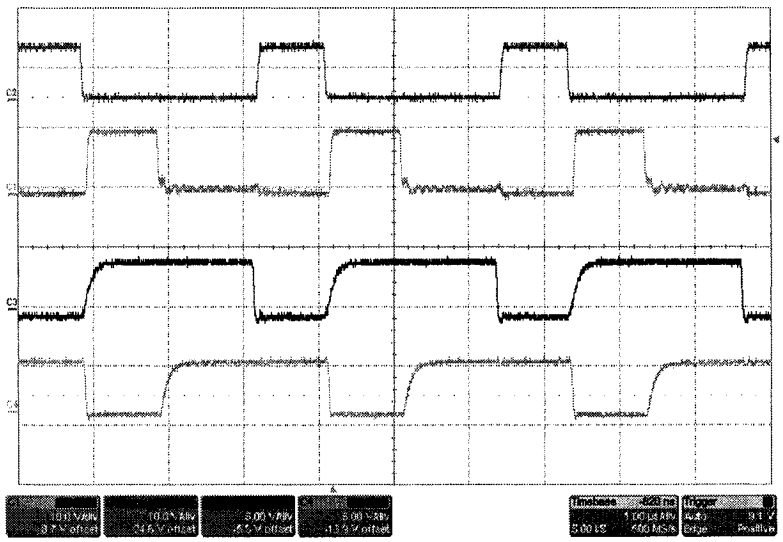


Fig. 2.26 Waveforms of primary and secondary switch gate voltages

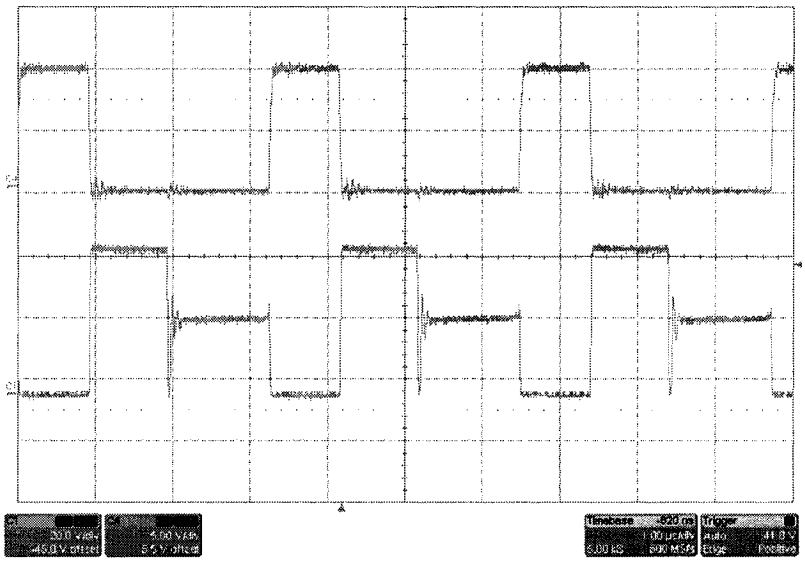


Fig. 2.27 ZVS waveforms of a primary switch

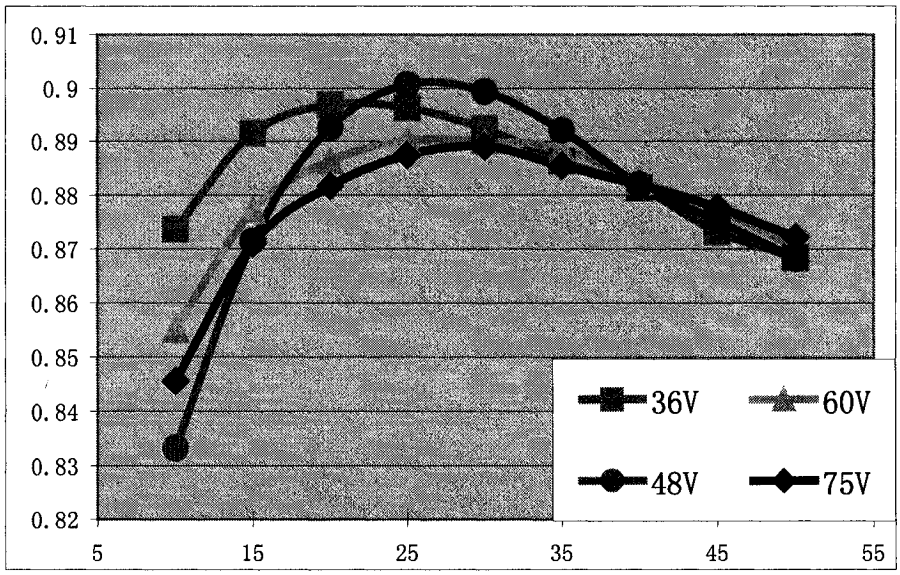



Fig. 2.28 Prototype efficiency

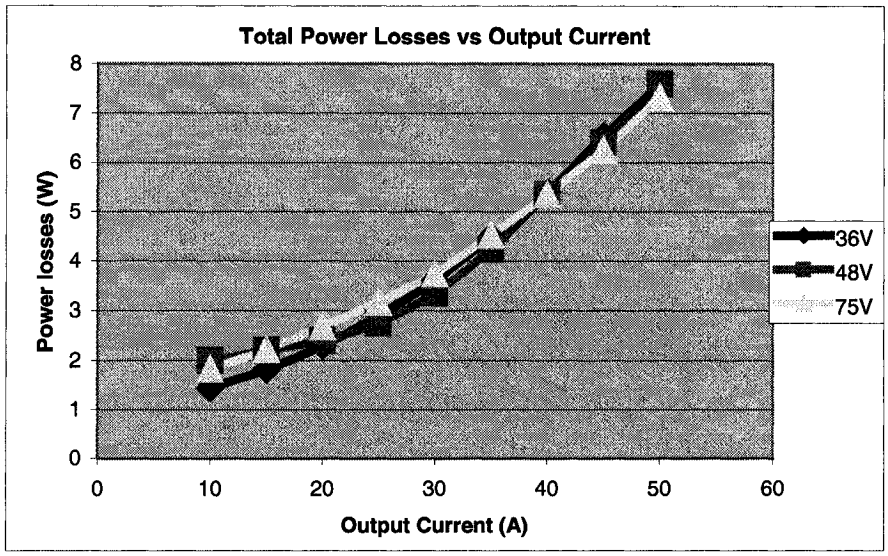



Fig. 2.29 Prototype total power loss

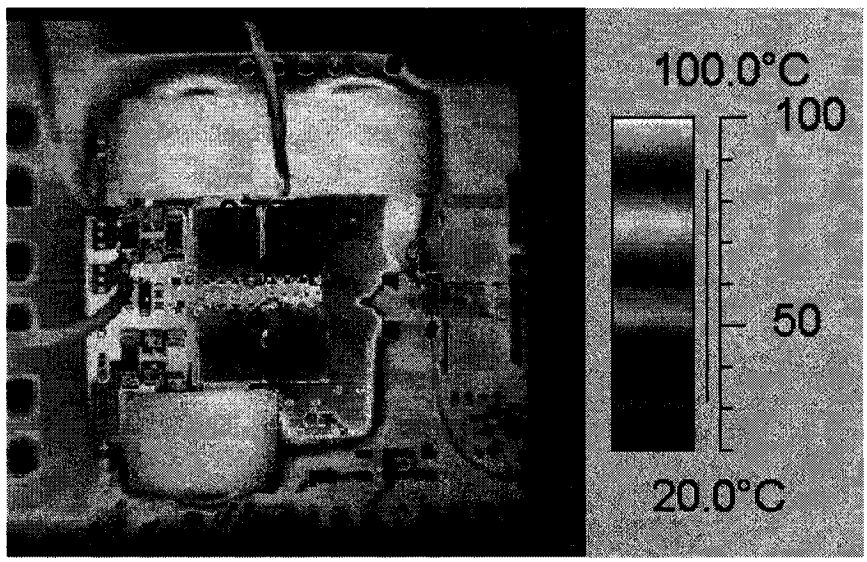



Fig. 2.30 Prototype thermal picture

## 2.4 Modified ZVS Half-Bridge DC-DC Topology Based on DCS Concept

In this section, a modified ZVS half-bridge DC-DC converter topology is proposed. The main improvements are that the auxiliary switch is grounded instead of floating, and the circuitry is simplified.

### 2.4.1 Introduction

For the DCS HB DC-DC converter proposed in the previous sections, the added switch $S_3$ is floating to the ground and the bootstrap technique is usually used to drive floating switches. To simplify the architecture, a modified DCS ZVS HB DC-DC converter is proposed as shown in Fig. 2.31, where $S_1$ and $S_2$ are two main switches, and an auxiliary branch consists of $S_3$ and $D_3$. It is noted that the switch $S_3$ is grounded instead of floating in Fig. 2.13, and thus the drive circuitry becomes simple and reliable. The principle of operation is similar to the previous topology described in section 2.3, and the key waveforms are shown in Fig. 2.32, where the driving signal of switch $S_2$ is shifted left close to the falling edge of $S_1$ driving signal so that $S_2$ may achieve ZVS. During the on time of switch $S_2$, switch $S_3$ turns on with ZVZCS. The transformer leakage inductance current freewheels through the auxiliary branch when switch $S_2$ turns off. Later on, switch $S_3$ turns off, and the leakage inductance energy is released to achieve ZVS for switch $S_1$.

### 2.4.2 Principle of Operation

To simplify the analysis of operation, components are considered ideal except as indicated otherwise. The primary equivalent circuits for the main operation modes are shown in Fig. 2.33.

***Mode 1*** ( $t_0 < t < t_1$ ): At $t = t_0$ , $S_1$ turns on with ZVS. During the interval, the transformer primary current $i_p$ was positive, and the secondary side diode $D_2$ was reverse-biased.

***Mode 2*** ($t_1 < t < t_2$): At $t = t_1$, $S_1$ turns off causing the current $i_p$ to charge $C_1$ and discharge $C_2$.

***Mode 3*** ($t_1 < t < t_2$): When the voltage across $C_2$ is discharged to zero, the body diode of $S_2$ conducts to carry the current, which provides ZVS condition for the switch $S_2$. During this subinterval, the secondary side current $i_1$ and $i_2$ freewheel through $D_2$ and $D_1$, respectively.

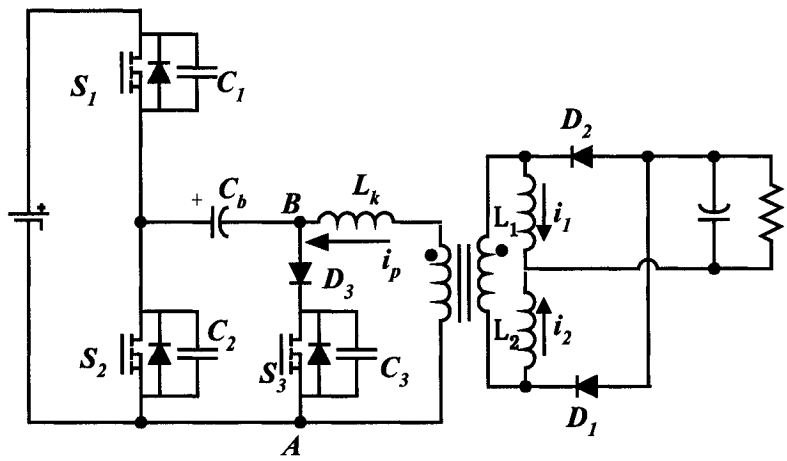



Fig. 2.31 Modified ZVS DC-DC HB converter

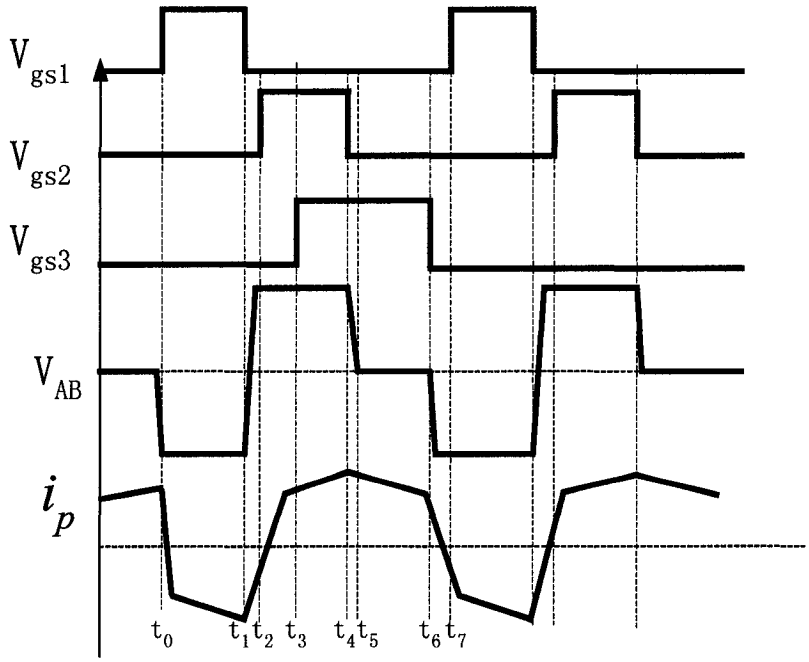



Fig. 2.32 Waveforms of the modified ZVS DC-DC HB converter

***Mode 4*** ($t_2 < t < t_3$): $S_2$ is turned on with ZVS at $t = t_2$, which causes the transformer leakage inductance current to be reset to zero and reverse-charged, while the output inductor currents keep freewheeling.

***Mode 5*** ($t_2 < t < t_4$): When the primary transformer current reaches the reflected current of $i_2$, diode $D_1$ is blocked and the inductor $L_2$ is charged. At $t = t_3$, the switch $S_3$ turns on with ZCS, because $D_3$ is reverse-biased and no current goes through $S_3$ until $S_2$ is turned off.

***Mode 6*** ($t_4 < t < t_5$): At $t = t_4$, $S_2$ is turned off, and the primary transformer current discharges $C_1$ while charging $C_2$.

***Mode 7*** ($t_5 < t < t_6$): At $t = t_5$, the voltage across $C_2$ is charged to the voltage across the capacitor $C_b$, and then the leakage inductance current flows through $D_3$ and $S_3$. During

this interval, the leakage inductance current freewheels through $D_3$ and $S_3$ such that the energy in the leakage inductance is trapped. On the secondary side, inductor $L_1$ and $L_2$ currents freewheel through $D_2$ and $D_1$, respectively.

***Mode 8*** ($t_6 < t < t_7$): At $t = t_6$, $S_3$ is turned off, causing $C_2$ and $C_3$ to be charged and $C_1$ to be discharged by leakage inductance current.

***Mode 9*** ($t_6 < t < t_7$): When the voltage across $C_1$ is discharged to zero, the body diode of $S_1$ conducts to recycle the energy in the transformer leakage inductance and offer a ZVS condition for switch $S_1$. Then it returns to Mode 1.

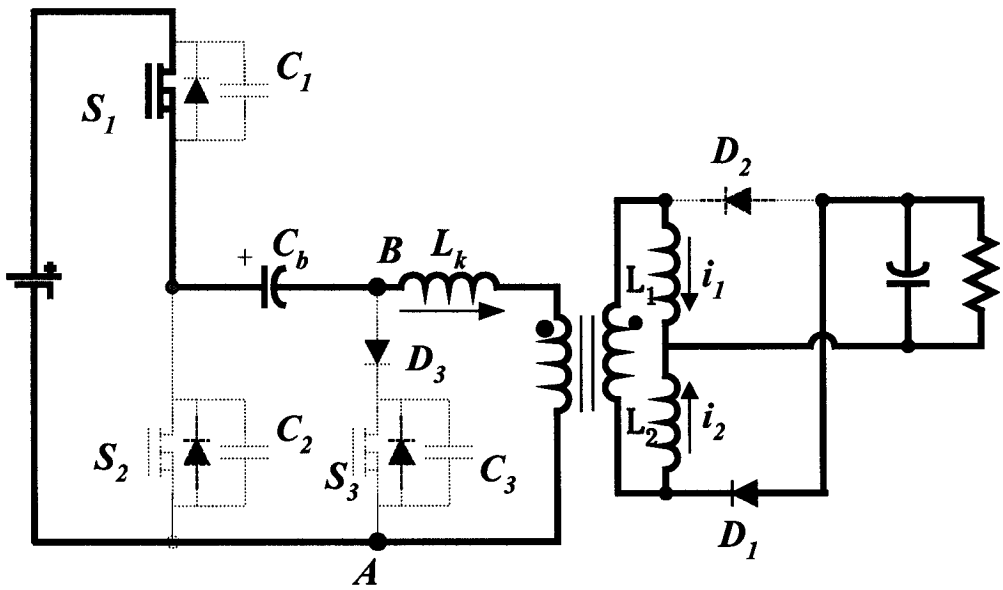



Fig. 2.33 (a) Mode 1

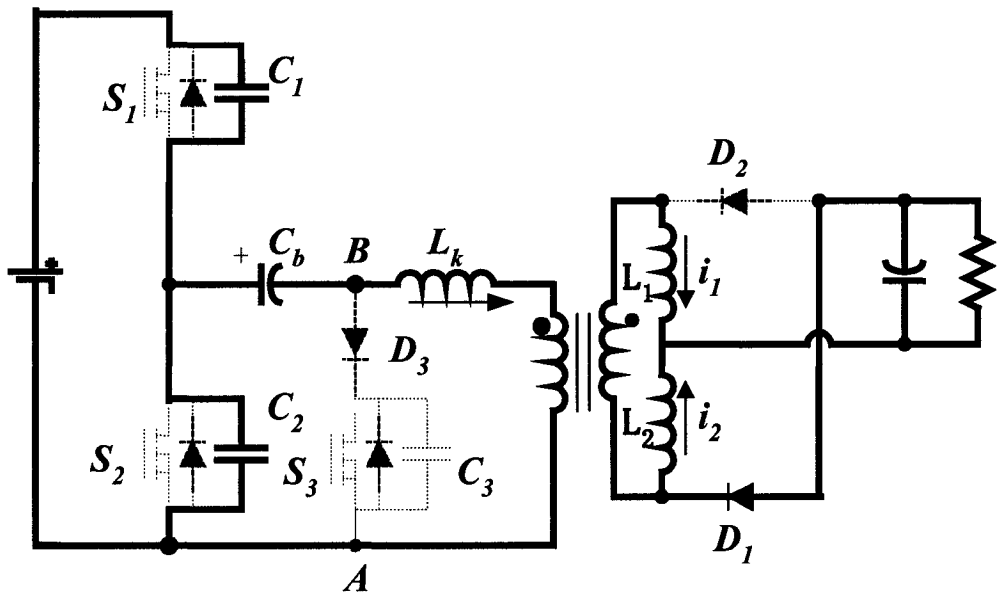



Fig. 2.33 (b) Mode 2

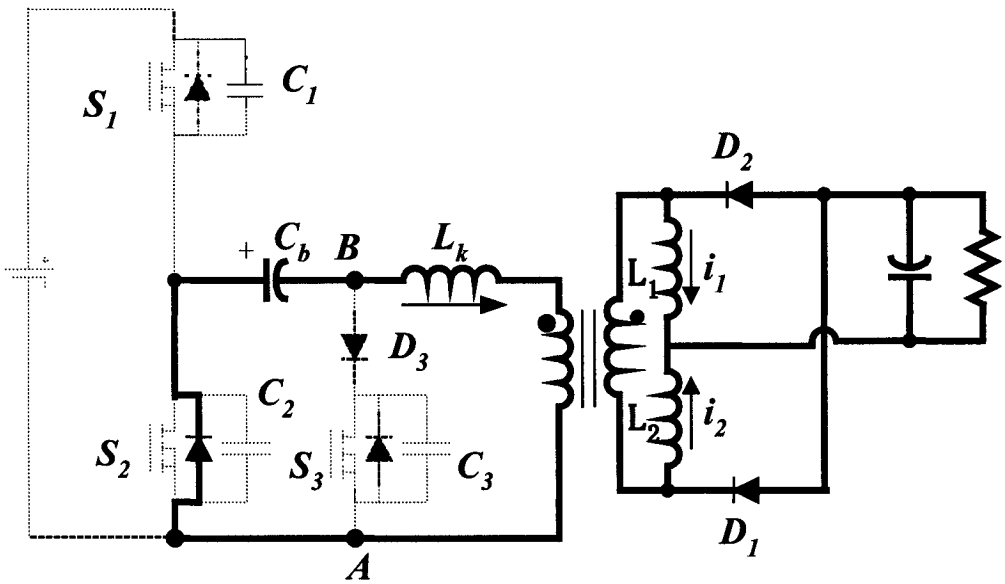



Fig. 2.33 (c) Mode 3

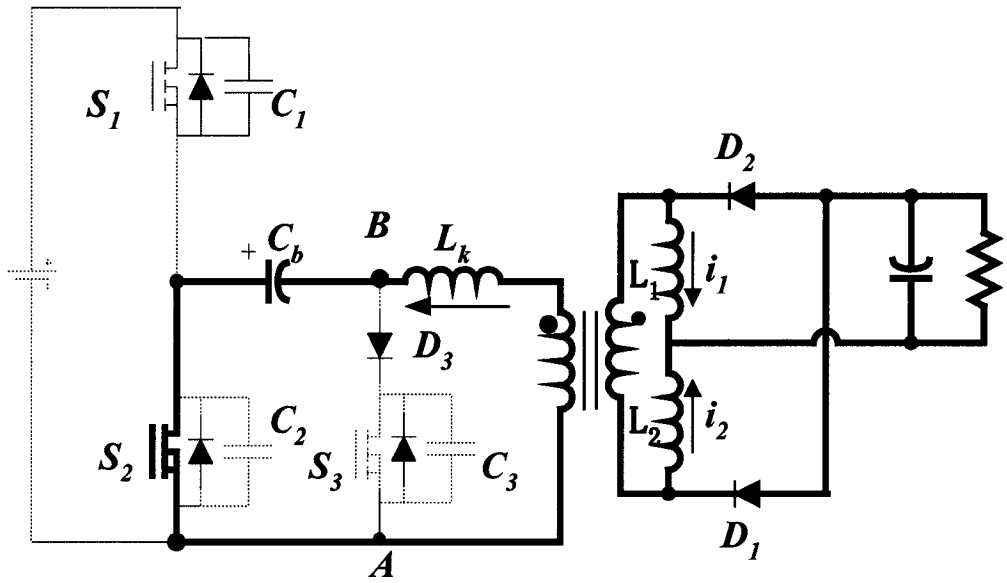



Fig. 2.33 (d) Mode 4

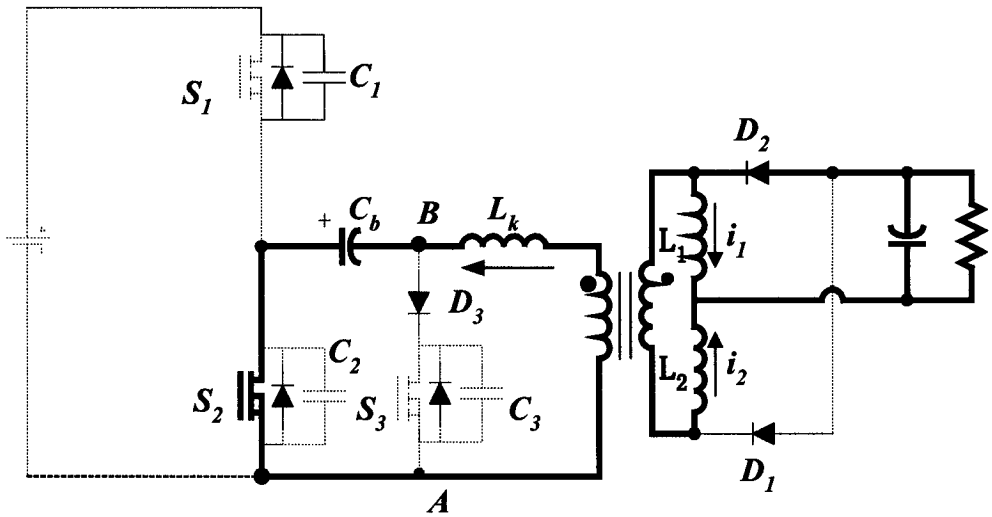



Fig. 2.33 (e) Mode 5

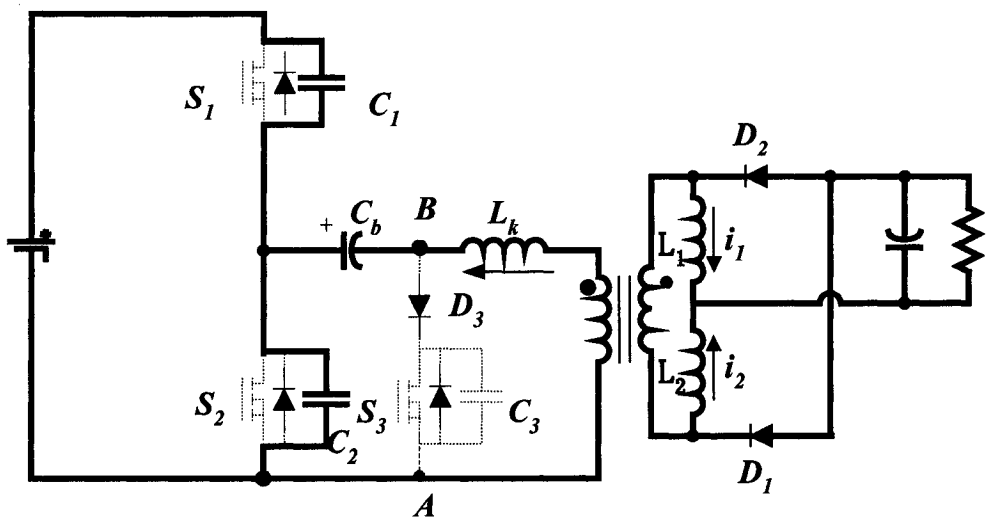



Fig. 2.33 (f) Mode 6

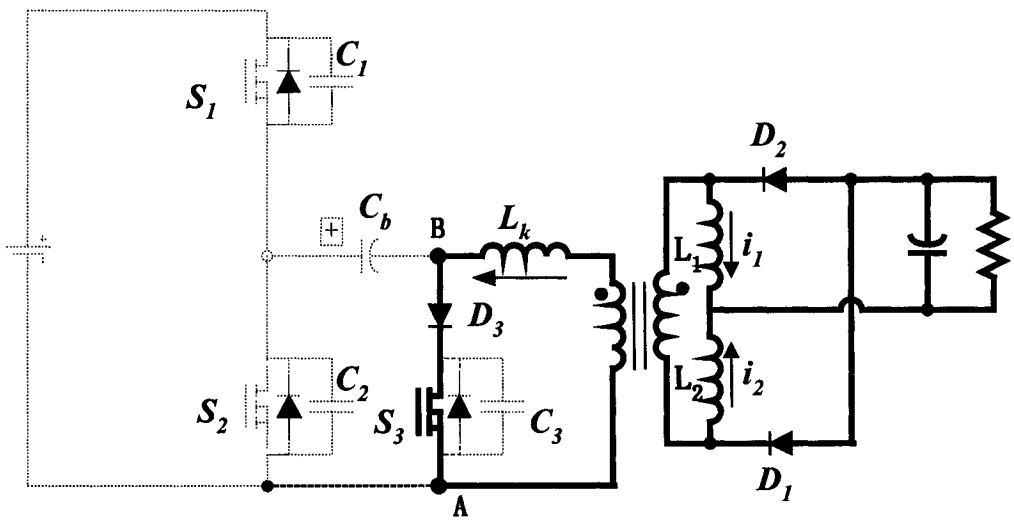



Fig. 2.33 (g) Mode 7

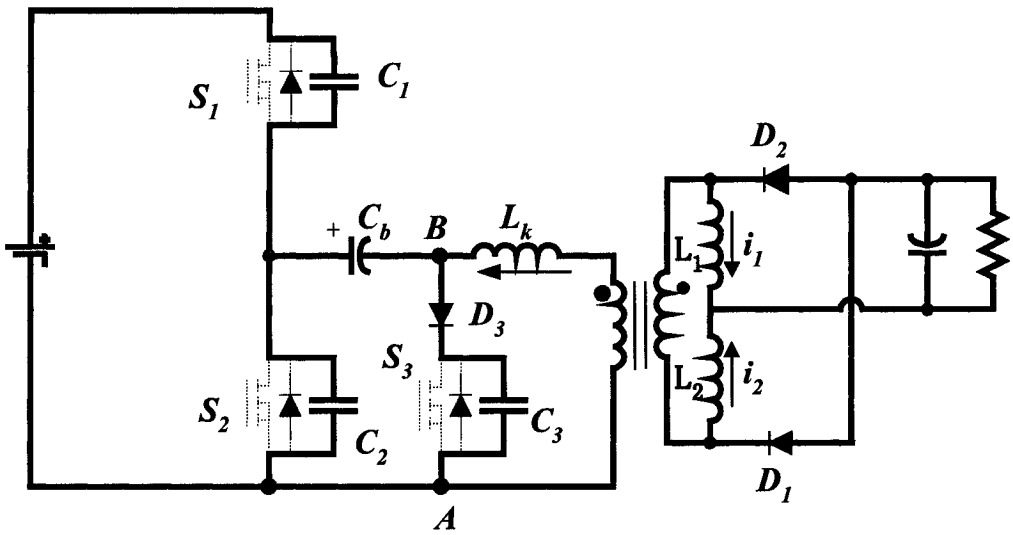



Fig. 2.33 (h) Mode 8

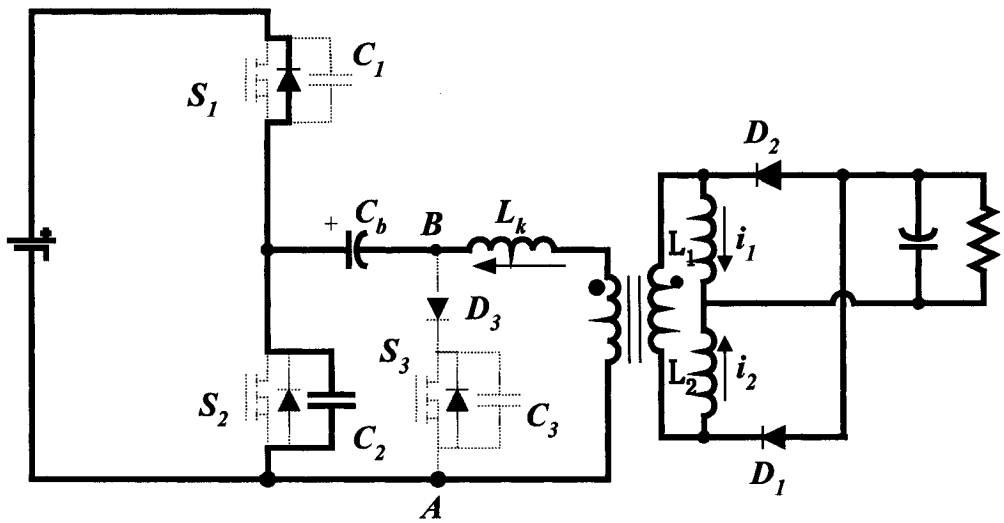



Fig. 2.23 (i) Mode 9

Fig. 2.33 Operational modes

### 2.4.3 Experimental Verification

A quarter-brick prototype with 3.3V/35A output and 36~75V input was built to verify the proposed modified HB DCS DC-DC converter. The prototype is shown in Fig. 2.34. Synchronous rectifiers are used on the secondary side to reduce the conduction losses. On the primary side, two MOSFETs are paralleled as a main switch. On the secondary side, each channel has two MOSFETs (Si7892). When operating at 400kHz with 48V input, the experimental waveforms are shown in Fig. 2.35, and the converter efficiency is measured as shown in Fig. 2.36. At high line, the converter has decreased efficiency because of the increased circulating energy.

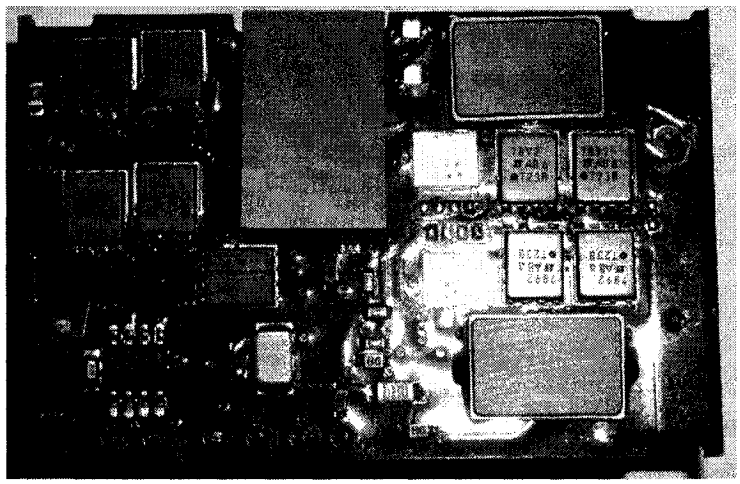


Fig. 2.34 Quarter-brick prototype photo

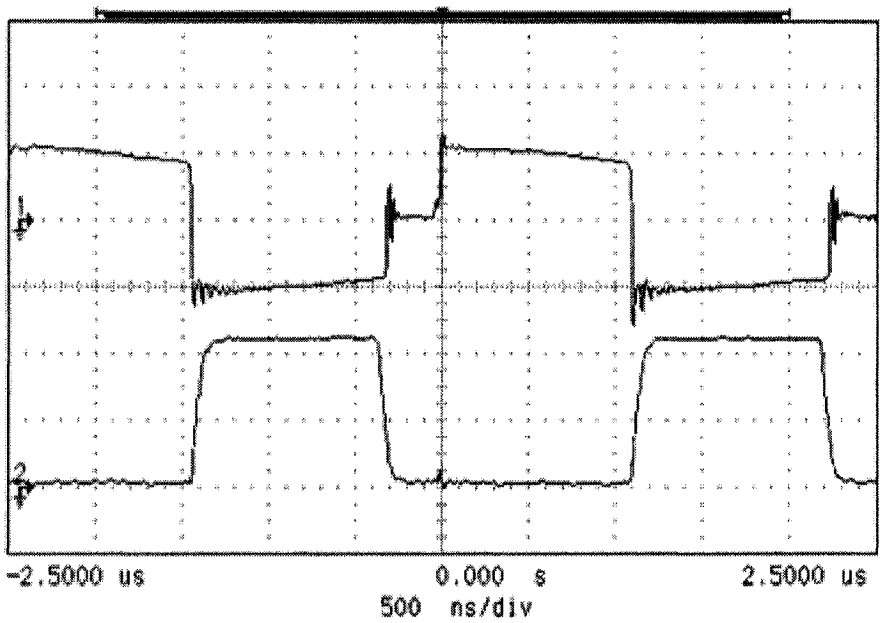



Fig. 2.35 (a) ZVS waveforms of switch $S_2$

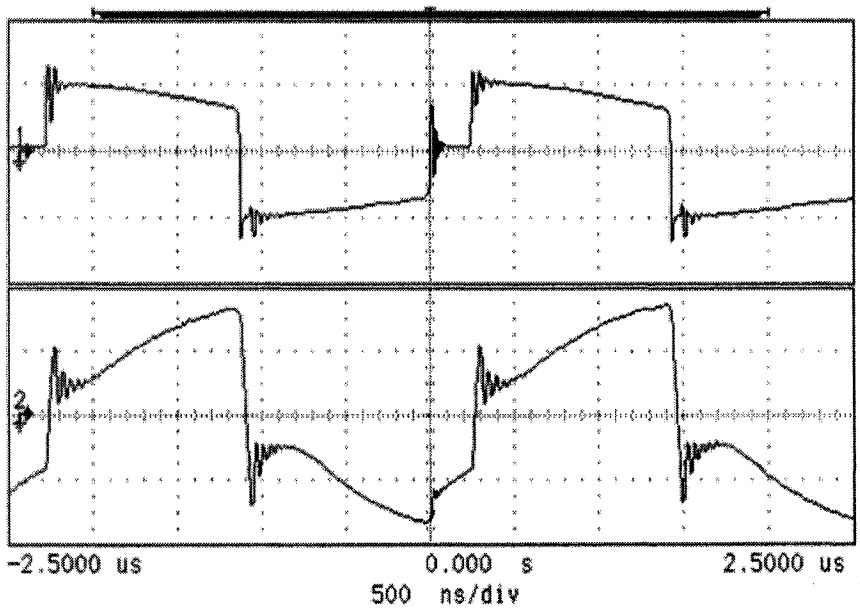



Fig. 2.35 (b) Transformer primary voltage and current

Fig. 2.35 Waveforms of the prototype

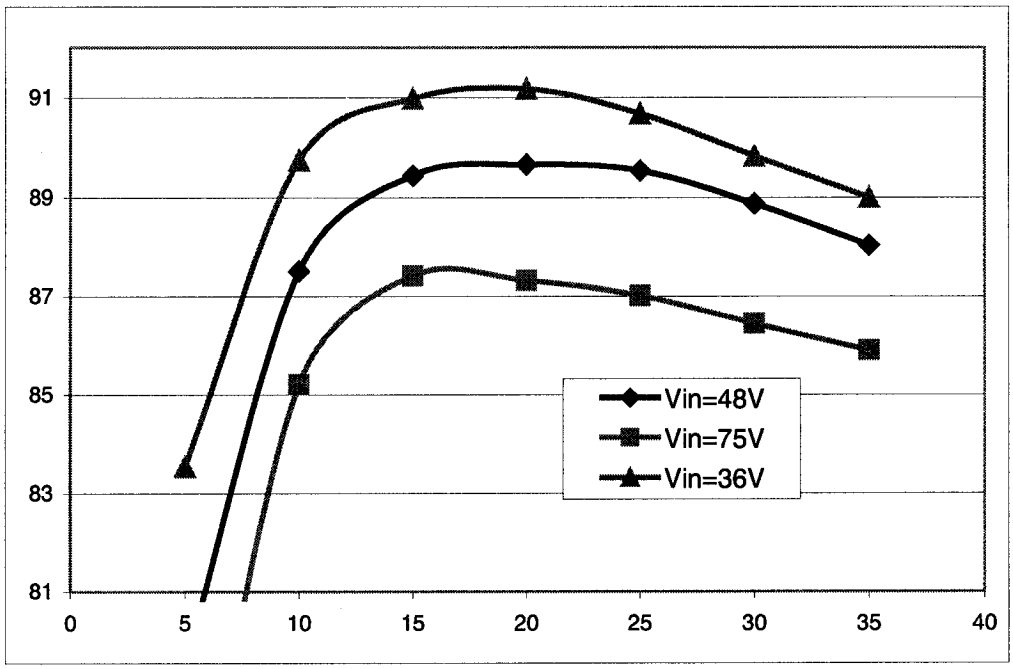



Fig. 2.36 Measured efficiency of the prototype

### 2.4.4 Summary

In this section, the modified DCS half-bridge DC-DC converter was proposed to achieve soft switching of the switches and to reduce the leakage-inductance-related losses. The auxiliary switch can be driven easily because it is grounded. The theoretical analysis and experimental results show that the proposed topology may achieve high efficiency at high switching frequencies.

## 2.5 Synchronous Rectification to Reduce Primary Circulating Conducting Loss

In the previous topologies proposed in this chapter, during the freewheeling period, the leakage inductance current freewheels through the added auxiliary branch, which consists of a switch and a diode. Generally, for 48V input "brick" applications, the conduction loss in diodes is larger than that in a MOSFET. When a converter operates in

a wide range of input voltage, the duty cycle becomes very small at high line. That means the freewheeling period become significant, and the freewheeling conduction loss in the middle branch increases, especially in the diode. To reduce the conduction loss in the diode, synchronous rectification technique can be used in the middle branch to reduce conduction loss. In this section, synchronous rectifiers are applied to ZVS topologies based on the DCS concept.

To simplify the figures, only primary-side circuitry is shown in the following topology figures. As shown in Fig. 2.37, to reduce the conduction loss through the diode $D_4$, a MOSFET $S_4$ replaces the diode $D_4$. Like driving timing in a synchronous rectifier, when switch $S_4$ body diode starts carrying current, switch $S_4$ is turned on with Zero-Voltage-Switching. Before a reverse voltage is applied to switch $S_4$, the switch is turned off, thus the current in the MOSFET is transferred to the body diode. Therefore, the current that is supposed to flow through a diode is carried in the MOSFET. For "brick" DC-DC converter applications, a MOSFET conduction loss is less than a diode, so that freewheeling conduction loss is reduced. The corresponding gate drive waveforms are shown in Fig. 2.38, where the yellow shaded area indicates the SR $S_4$ conduction interval.

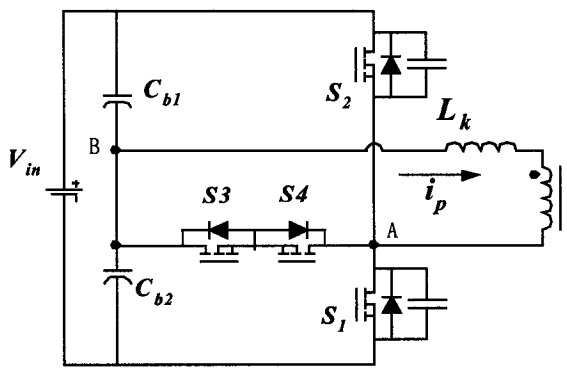



Fig. 2.37 DCS HB converter with synchronous rectification

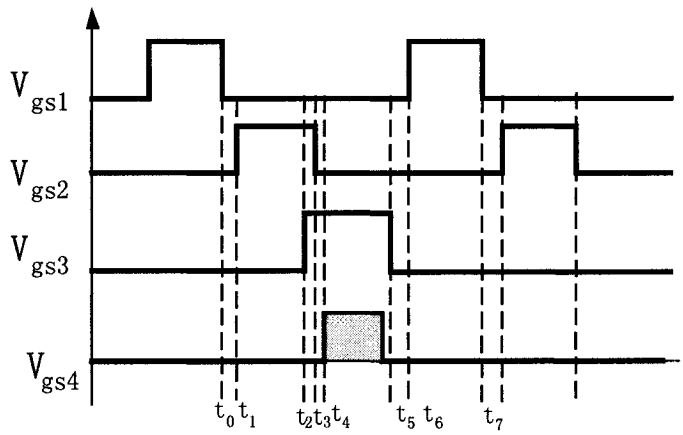



Fig. 2.38 Gate drive waveforms

In Fig. 2.37, switches $S_3$ and $S_4$ have a common source, so the gate drive can be implemented using the same power supply bias. However, two driving signals are generated separately. To simplify the driving and control, a modified SR structure is shown in Fig. 2.39, and the corresponding waveforms are shown in Fig. 2.40.

Let's review the timing of the switches $S_3$ and $S_4$. Since switch $S_3$ can be turned on at any time during the interval when switch $S_2$ is on, switch $S_4$ can turn on just before switch $S_3$ is turned off. For switch $S_4$, when switch $S_3$ is turned off, the switch $S_4$ can be turned on. In other words, the critical timing sequence is that switch $S_4$ turns on just before $S_3$ turns off, and switch $S_3$ turns on just after $S_3$ turns off. In this case, we may generate two gate drive signals for $S_3$ and $S_4$ from the same signal source, and $S_4$ gate drive signal can be derived by delaying the gate signal of switch $S_3$. In Fig. 2.40, the delay is achieved with the use of a resistor in series with the $S_4$ gate. The resistor associated with the gate parasitic capacitance is actually a RC delay network. By changing the resistor value, the delay time can be designed.

The SR technique can be also used for the grounded DCS ZVS HB DC-DC converter. The topologies are shown in Fig. 2.41 and Fig. 2.42, respectively. The gate drive waveforms of the converter shown in Fig. 2.41 are the same as shown in Fig. 2.38. The converter shown in Fig. 2.42 has corresponding waveforms as shown in Fig. 2.40.

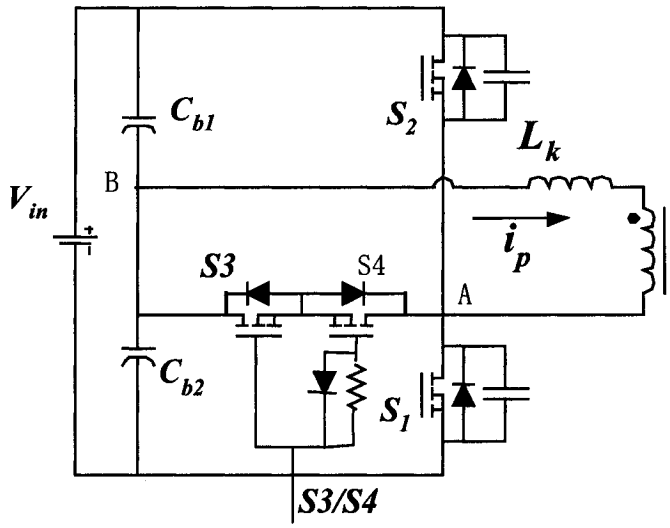



Fig. 2.39 DCS HB converter with tied-gate SR

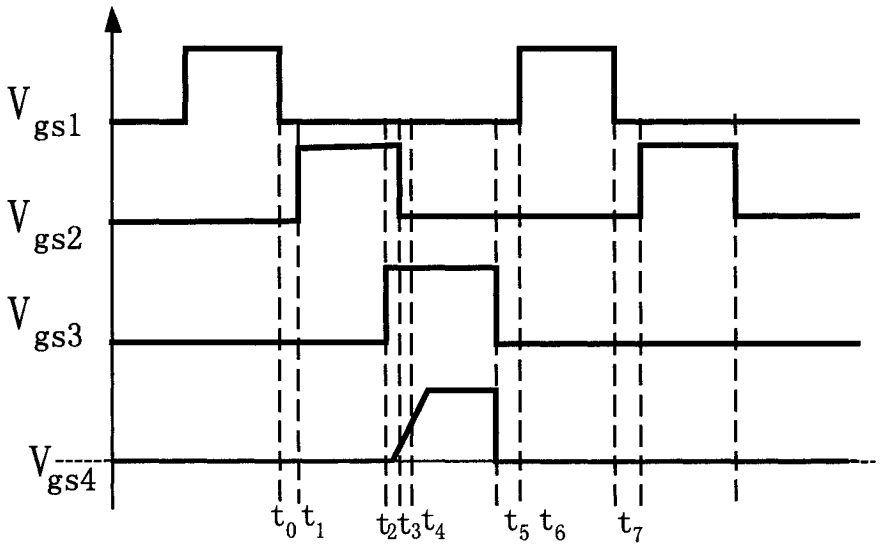



Fig. 2.40 Waveforms of DCS HB converter with tied-gate SR

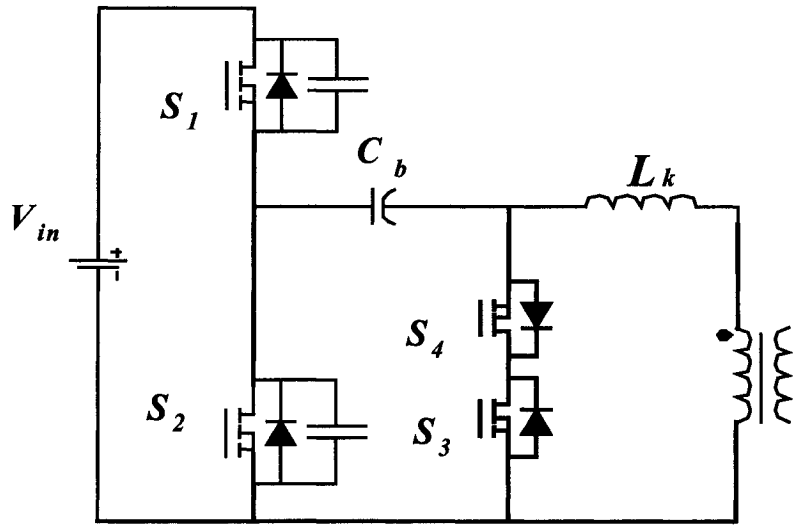



Fig. 2.41 Modified DCS HB converter

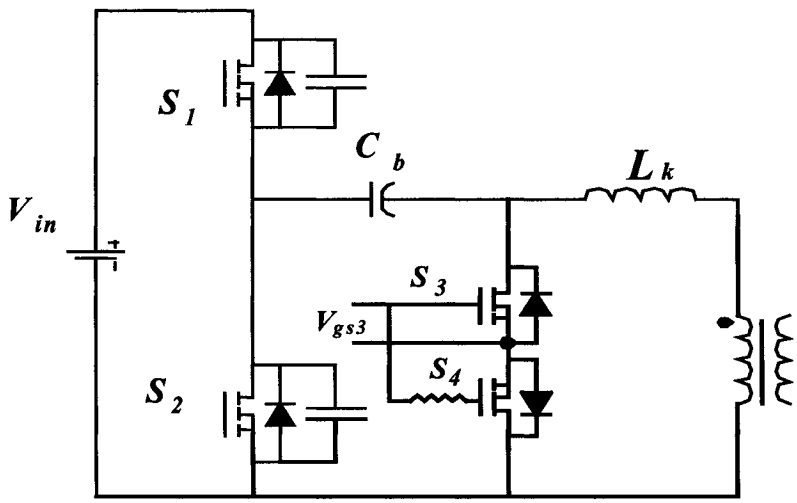



Fig. 2.42 Modified DCS HB converter with tied-gate SR

# 3. INVESTIGATION OF SNUBBER CIRCUITS FOR ISOLATED DC-DC CONVERTERS

Low output-voltage high-current converters have been broadly used to power integrated circuits. For this application, the transformer secondary winding in an isolated converter is generally only one turn. In this case, the coupling between the primary and the secondary winding will be rough, and the transformer leakage inductance will increase. The leakage inductance in isolated DC-DC converters may oscillate with parasitic capacitance leading to high frequency ringing and EMI issues. Moreover, the ringing dissipates energy and degrades the converter efficiency. In this chapter, based on the snubber topology review, an active-clamp snubber topology is proposed to clamp the leakage inductance and eliminate the related ringing, and two lossless passive snubbers are proposed to reduce reverse recovery losses in secondary synchronous rectifiers. Experimental results are presented to verify the proposed snubber circuits.

## 3.1 An Active-Clamp Snubber for Half-Bridge DC-DC Converters

In the conventional isolated half-bridge DC-DC converter, the leakage-inductance-related losses degrade converter efficiency and limit the increase of converter switching frequency. A novel active-clamp circuit is proposed to recycle the energy stored in the leakage inductance, and thus improves converter efficiency. By transferring the energy in the leakage inductance to a capacitor, the leakage inductance energy is recycled. Moreover, the proposed active-clamp circuit avoids the body diode conduction of the primary-side switches. Hence the body diode conduction and reverse-recovery losses are eliminated. The principles of operation and simulation results are presented in this

chapter. The experimental results show efficiency improvement based on a half-bridge DC-DC converter with the proposed active-clamp circuit.

### 3.1.1 Background

In isolated DC-DC converters, the transformer leakage inductance is an important factor that affects the performance of converters. Employing transformer leakage inductance, a variety of topologies and control methods are proposed to upgrade the converter performance [C1~C9]. Phase-shift full-bridge [C1] and active-clamp forward [C4] DC-DC converters are good examples to utilize the transformer leakage inductance to achieve zero-voltage switching (ZVS) and further reduce EMI noises.

For the half-bridge DC-DC converters, there are two conventional control schemes: asymmetric control [C5 ~ C7] and symmetric control. A symmetric controlled half-bridge DC-DC converter [C8 ~ C9] has simple configuration and operates with symmetric electrical stress. However, the two primary switches operate at hard-switching conditions and leakage-inductance-related ringing problems exist. To damp the ringing, dissipative snubber circuits usually are employed across switches with the result that the energy in the leakage inductance is dissipated partly or totally in the snubber circuits. Consequently, efficiency is degraded and the power level is limited.

An active current clamping method [C8~C9] is proposed to achieve ZVS of switches and to attenuate the ringing. During the off-time interval, the leakage inductance current freewheels through the auxiliary circuits. Prior to the turn-on of main switches, auxiliary switches cut off the freewheeling path, such that the energy in the leakage inductance is released to create a ZVS condition for the main switches. However, this

method has two main demerits: one is that the value of the leakage inductance should be high enough, and the other is that high circulating current exists especially at small duty cycle. That means this scheme is not suited for applications with wide-range input voltage.

In the dissertation, a new active-clamp circuit is proposed to clamp the leakage inductance current and damp the ringing during the off-time interval when both switches are off. In the proposed circuit, the energy in the transformer leakage inductance is transferred to a capacitor during the off-time interval. Hence, the ringing is extinguished, and the body diodes of switches never conduct, such that there is no body-diode reverse recovery and the ringing losses are minimized. As the current-transferring interval accounts for a small part of the period, the conduction losses during the off-time interval are also reduced significantly.

### 3.1.2 Principle of the Proposed Snubber Circuit

Fig. 3.1 shows the conventional half-bridge DC-DC converter with current doubler rectification, where $L_k$ is the transformer leakage inductance and $C_{j1}$ and $C_{j2}$ are junction capacitance of MOSFET switches $S_1$ and $S_2$. During the freewheeling period when both switches $S_1$ and $S_2$ are off, the transformer secondary is shorted by the two conducting diodes. Assuming the junction capacitance of switches is much smaller than that of capacitors $C_{b1}$ and $C_{b2}$, and neglecting other parasitic capacitance and inductance, the equivalent circuit of the freewheeling mode is shown in Fig. 3.2 (a). If two body diodes are ideal, the energy in the leakage inductance will be recycled to DC bus through the two diodes with undamped oscillation between the transformer leakage inductance and

the junction capacitance. The energy involved in the oscillation is determined by the junction capacitances and input voltage:

$$E = \frac{1}{2} C_j V_{in}^2 \tag{3-1}$$

Where, $C_j$ is the individual MOSFET junction capacitance.

As a matter of fact, the body diodes of MOSFET have undesirable reverse-recovery characteristics, especially for MOSFETs with high voltage ratings, which results in more energy involved in the oscillation. As a result, the ringing is more severe and there are more reverse-recovery and ringing losses due to the non-ideal diodes. Moreover, the ringing and reverse-recovery may lead to EMI problems.

Usually, snubber circuits are added to dampen the ringing. The R/C series snubber across a switch is the most common snubber circuit. Depending on the size of snubbers, the energy remaining in the leakage inductance may be partly recycled to the DC bus or totally dissipated in snubbers. For a small snubber, body diodes conduct to partly recycle the energy with a part of the energy dissipated in the snubber. For a large snubber, the energy in the leakage inductance may be fully dissipated in the R/C snubber without the involvement of body diodes. In this case, the power losses increase significantly with the increase of primary-side peak current and switching frequency.

A current-clamp concept is proposed in the dashed-line frame in Fig. 3.2 (b). With the clamp snubber, the energy in the leakage inductance can be recycled into the voltage source. It is important to note that the diodes in the snubber are not body diodes of MOSFETs, which means the reverse recovery characteristics of the diodes are much desirable than those of body diodes. So the ringing can be attenuated with the diodes.

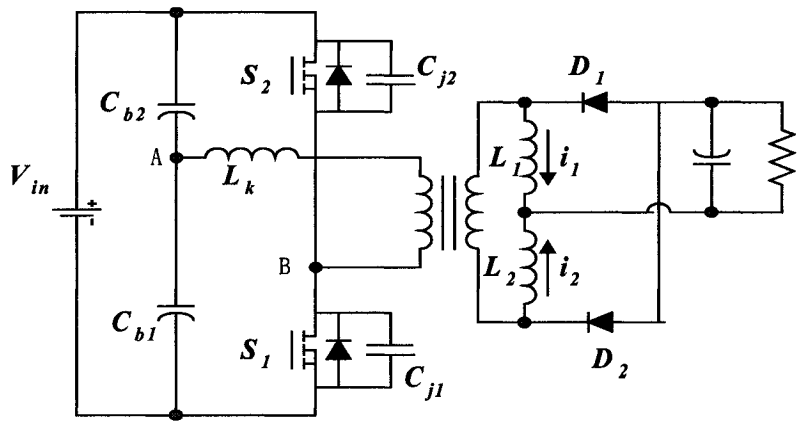



Fig. 3.1 Half-bridge isolated DC-DC converter

Employing the same clamp concept, a practical active-clamp snubber circuit is shown in Fig. 3.3, where capacitor Cs is used to absorb the energy in the leakage inductance and damp the ringing. $S_3$, $D_3$, $S_4$ and $D_4$ provide a path for the leakage inductance to transfer the remained energy into capacitor $C_s$ during the freewheeling period when both switches are off.

The key operational waveforms for the proposed topology are shown in Fig. 3.4, and the equivalent modes are shown in Fig. 3.5. To simplify the analysis of operation, components are considered ideal except as indicated otherwise. The main operation modes are described as follows:

***Mode 1*** $(t_1 < t < t_2)$: Initially, $S_1$ is conducting and $S_3$ is turned on with ZCS. At $t = t_1$, $S_1$ is turned off, causing the primary current $i_p$ to charge the junction capacitance $C_{j1}$ and discharge $C_{j2}$. When the voltage across $C_{j1}$ is charged to one-half of the input voltage $V_{in}$, the leakage inductance current flows through $D_3$, $C_s$ and $S_3$. Considering that the transformer is shorted and there is a DC voltage across $C_s$, the leakage current

continues to charge the capacitor $C_s$ until the current is reset to zero at $t_2$. Finally, all the energy in the leakage inductance is transferred into the capacitor $C_s$.

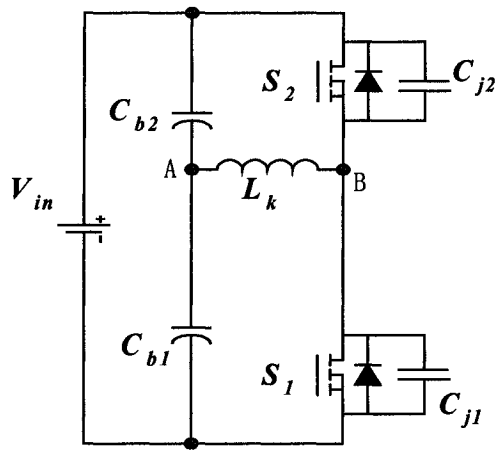



Fig. 3.2 (a) Without snubber

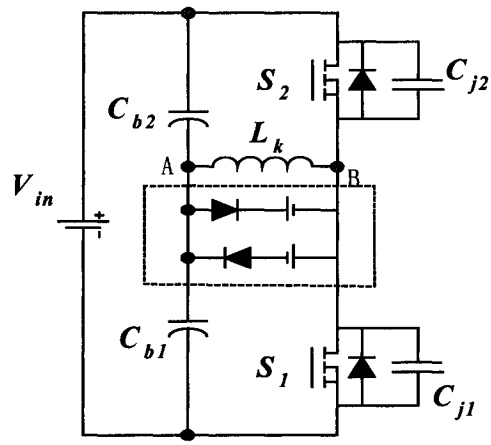



Fig. 3.2 (b) Clamp-circuit concept

Fig. 3.2 Equivalent oscillation circuits during the freewheeling period

***Mode 2*** *($t_2 < t < t_4$)*: As the diode $D_3$ blocks the potential reverse current, the reverse oscillation path through $S_3$ and $D_3$ is cut off. Considering the possibilities to use Schottky diodes as $D_3$ for many cases, the diode reverse recovery current can be eliminated. However, because the voltage $v_{AB} = 0$ is not the steady state, the voltage across $C_s$ will cause the voltage $v_{AB}$ to oscillate until $v_{AB} = V_{cs}$. Noting that the voltage across Cs is much lower than half of the input voltage, the MOSFET body diodes will not be involved in the oscillation, and thus, the ringing is so slight to be negligible. Therefore, there are no body-diodes-related losses and the ringing loss is very limited. At $t = t_3$, the switch $S_3$ is turned off with zero voltage and current.

***Mode 3*** *($t_4 < t < t_5$)*: $S_2$ is turned on at $t = t_4$, and the leakage current is charged from zero as the slope:

$$\frac{di}{dt} = \frac{0.5V_{in} + V_{cs}(t)}{L_K} \tag{3-2}$$

Where, $V_{cs}(t)$ is the voltage across the capacitor Cs. As the leakage inductance is very small, the current goes up quickly until it reaches the reflected secondary inductor current. Then the diode $D_2$ is blocked, and the converter starts to transfer energy from the primary to the secondary. The current continues to rise as the slope:

$$\frac{di}{dt} = \frac{0.5V_{in} + V_{cs}(t) - \frac{n_1}{n_2} \cdot V_o}{L_K + (\frac{n_1}{n_2})^2 \cdot L_2} \tag{3-3}$$

Where, $L_2$ is the secondary inductor, $n_1$ and $n_2$ are the transformer primary turns and secondary turns, respectively and $V_o$ is the output voltage. During this interval, the inductor current is charged, and the capacitor $C_s$ is discharged. The polarity of voltage across the capacitor $C_s$ changes during the interval. During this interval, the auxiliary switch $S_4$ is turned on with ZCS.

***Mode 4*** *($t_5 < t < t_6$)*: This mode is similar to Mode 1. $S_2$ is turned off at $t = t_5$ causing the primary current $i_p$ to charge $C_{j2}$ and discharge $C_{j1}$. When the voltage across $C_{j2}$ is charged to half of the input voltage, the leakage inductance current flows through $D_4$, $C_s$ and $S_4$. Considering that the transformer is shorted and that there is a DC voltage across $C_s$, the leakage current continues to charge the capacitor $C_s$ until the current is reset to zero at $t_6$. Finally, all the energy in the leakage inductance is transferred into capacitor $C_s$.

***Mode 5*** *($t_6 < t < t_8$)*: This mode is symmetrical with Mode 2. A slight oscillation comes to the end with:

$$V_{C_{j1}} = \frac{1}{2}V_{in} + V_{Cs}(t_6) \tag{3-4}$$

$$V_{C_{j2}} = \frac{1}{2}V_{in} - V_{Cs}(t_6) \tag{3-5}$$

Where, $V_{Cs}(t_6) > 0$. At $t = t_7$, the switch $S_3$ is turned off with zero voltage and current.

***Mode 6*** *($t_8 < t < t_{10}$)*: This mode is symmetrical with Mode 3. Switch $S_1$ is turned on, and finally the converter starts to deliver energy from the primary to the secondary. At $t = t_9$, the auxiliary switch $S_3$ is turned on with ZCS.

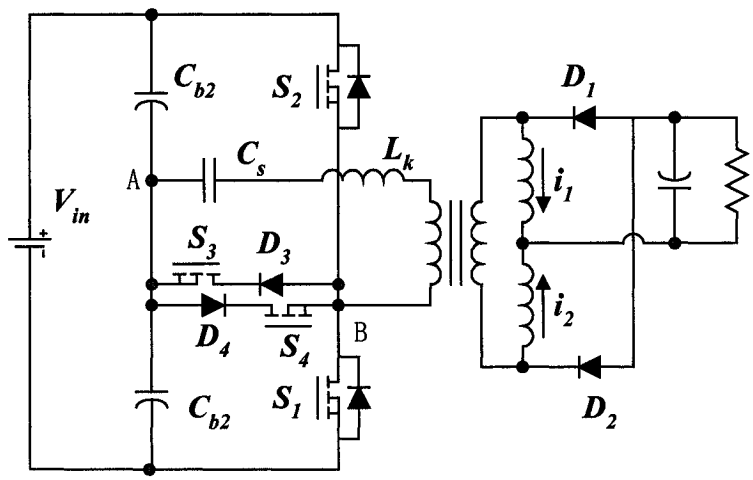



Fig. 3.3 Active-clamp half-bridge DC-DC converter

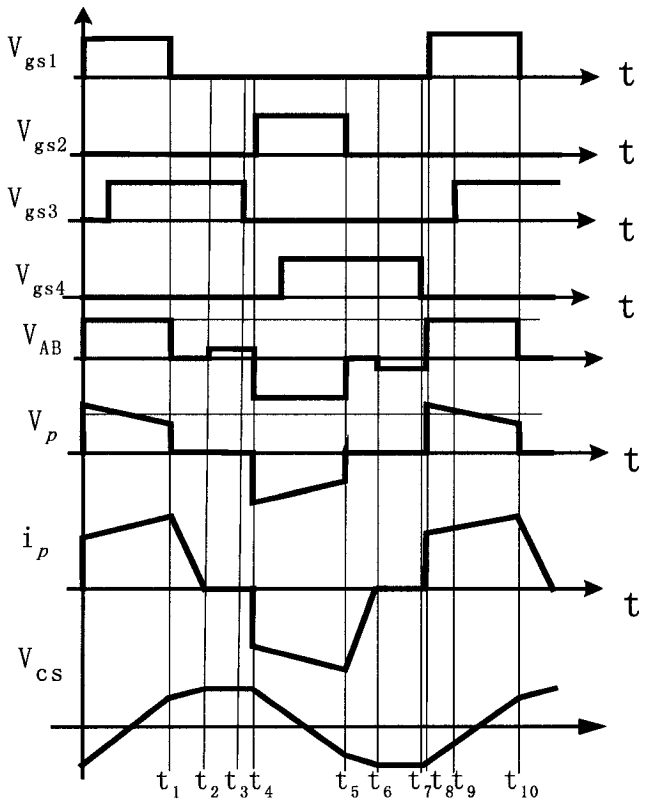



Fig. 3.4 Key waveforms of the proposed topology

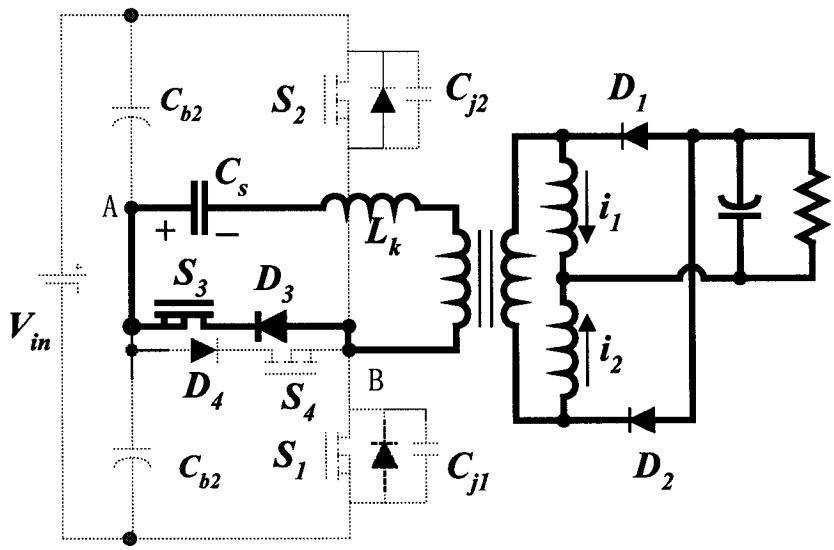



Fig. 3.5 (a) Mode 1

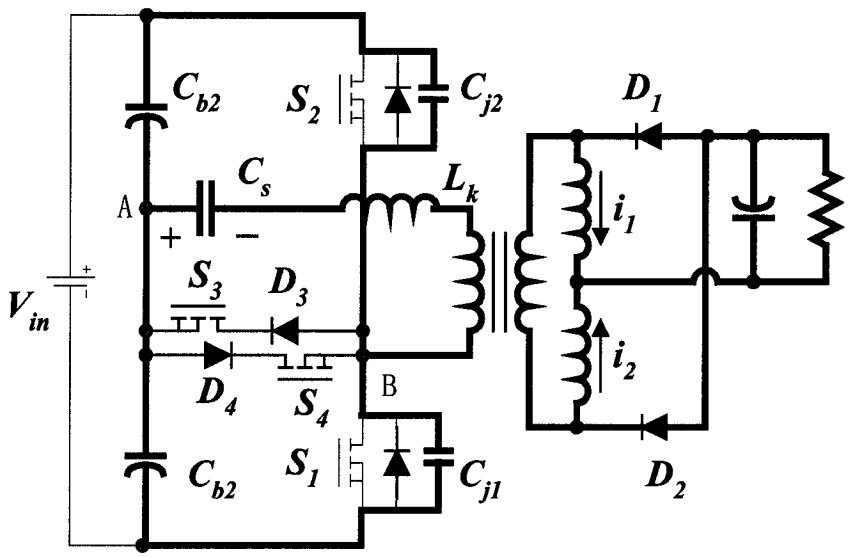



Fig. 3.5 (b) Mode 2

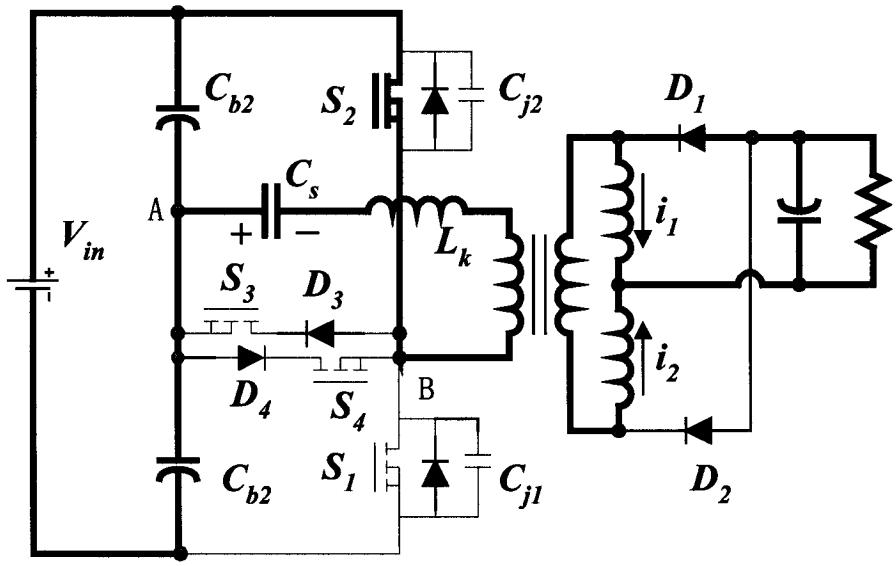



Fig. 3.5 (c) Mode 3

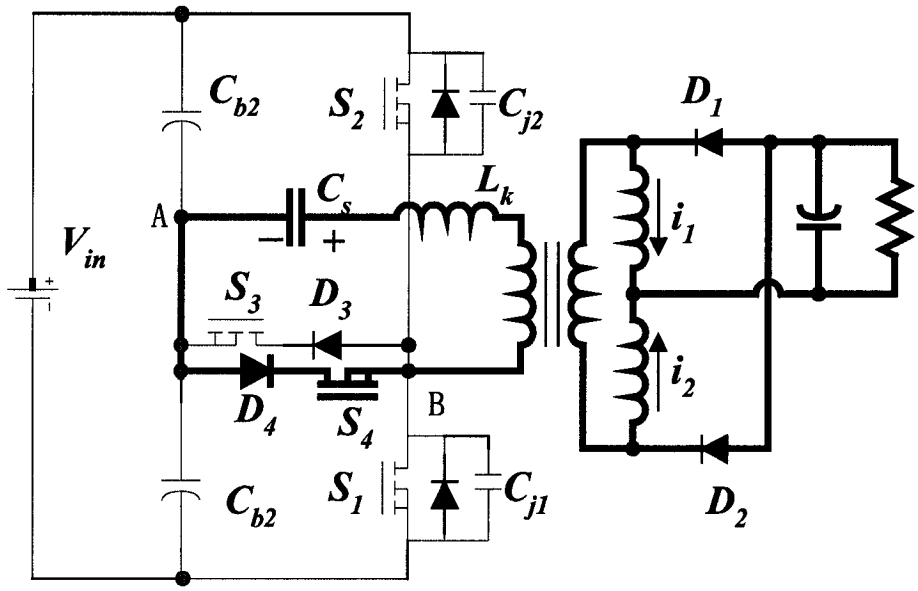



Fig. 3.5 (d) Mode 4

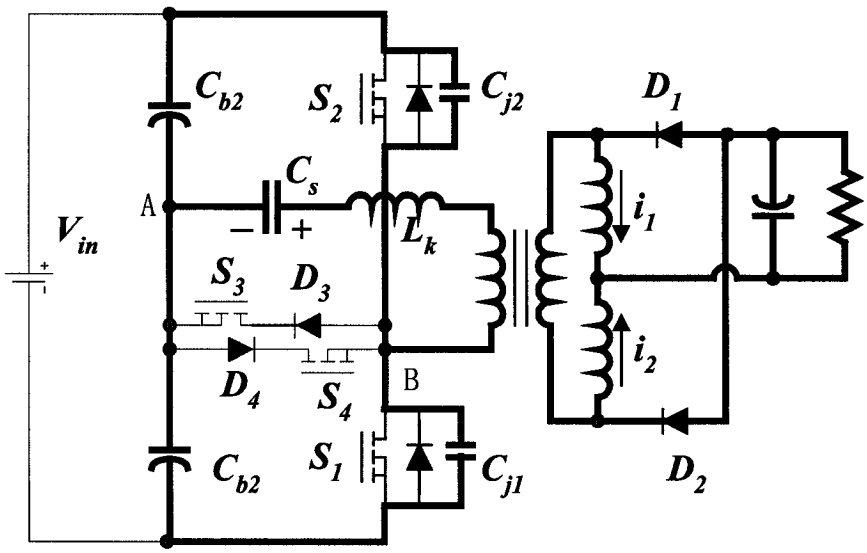



Fig. 3.5 (e) Mode 5

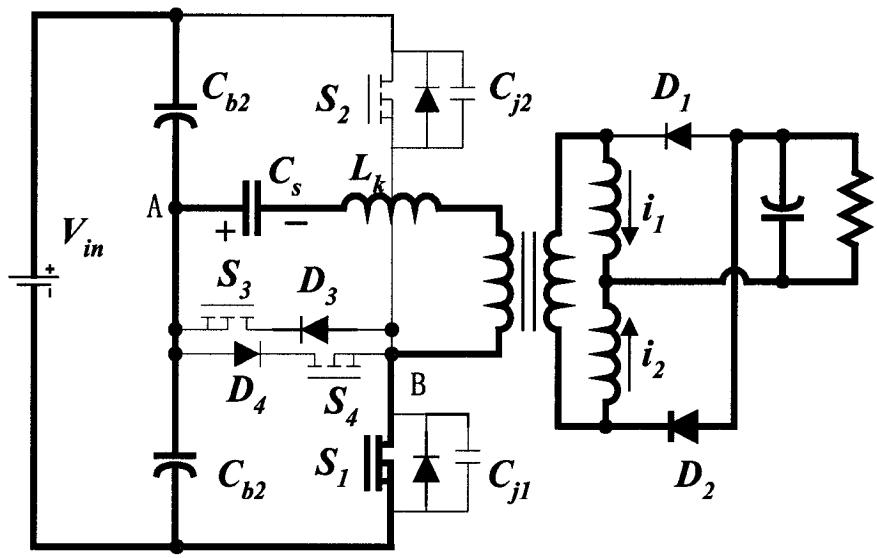



Fig. 3.5 (f) Mode 6

Fig. 3.5 Operation modes analysis

### 3.1.3 Main Features and Design Considerations

As previously discussed, with the proposed active-clamp snubber, the energy in the leakage inductance is transferred to the capacitor instead of dissipating in the dissipative snubber. Furthermore, the body diodes of the main switches are excluded from the oscillation, such that the body diodes conduction losses and reverse-recovery losses are eliminated.

The auxiliary switches $S_3$ and $S_4$ are turned on with ZCS and are turned off with ZVZCS, and thus the switching losses are minimized. Considering that the conduction intervals of auxiliary circuits only account for a very small part of the whole period, the auxiliary switches and diodes conduction losses are negligible. Therefore, total auxiliary circuits losses can be ignored. In addition, the voltage stresses in the auxiliary switches and diodes are only one-half of the input voltage. Consequently, compared with the main

switches, smaller auxiliary components with lower rated current and voltage can be used for the snubber.

When main switches are turned off, the leakage inductance current starts to reset towards zero. As shown in Fig. 3.6, $T_R$ is the reset time of leakage inductance current, $T_{on}$ and $T_{off}$ are the on-time of a main switch and off-time of the two main switches, respectively. If $T_{off} > T_R$, the operations is the same as described above, and the primary voltage and current are shown in Fig. 3.6(a). If $T_{off} < T_R$, there is not enough time for the leakage inductance to transfer the energy into capacitor $C_s$. With the turn-off of the auxiliary switches, the remaining leakage inductance energy will be used to charge/discharge the junction capacitance. In this case, the ZVS may be achieved for the main switches. Corresponding waveforms of the primary voltage and current are shown in Fig. 3.6(b). In other words, depending on the width of the duty cycle, the proposed topology has two possible operation manners, for example in the low-duty-cycle case, the converter operates with the active-clamp mode to reduce ringing problem. For the high-duty-cycle case, the active-clamp interval is reduced, such that the energy in the leakage inductance will be directly used to achieve ZVS for the main switches instead of being transferred into the capacitor $C_s$.

Therefore, this topology is suited for wide input voltage range. At high line, the converter reduces the circulation conduction losses, and at low line, the converter may reduce the switching losses. The reset time $T_R$ can be expressed as follows:

$$T_R = \frac{2C_S L_K}{DT} \tag{3-6}$$

Where, T is period and D is the duty cycle, which satisfy $T_{on} = DT$. As shown in the equation (3-6), $T_R$ is independent on the load, which provides a simple design for the capacitance of $C_s$. The peak-peak voltage ripple across capacitor $C_s$ satisfies:

$$V_{pk-pk} = \frac{DTn_2}{2C_S n_1} I_o \tag{3-7}$$

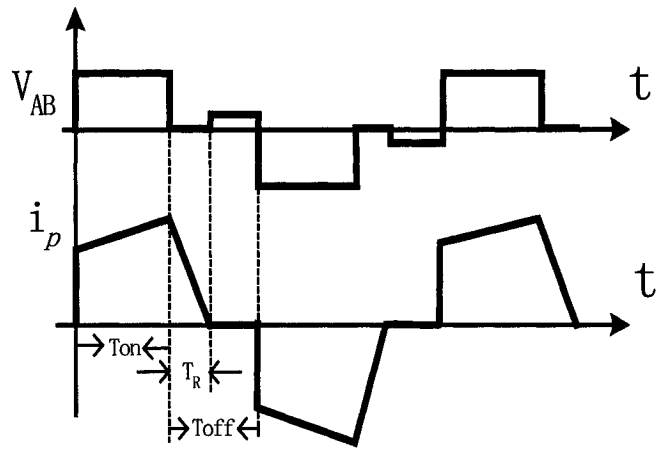



Fig. 3.6 (a) $T_{off} > T_R$

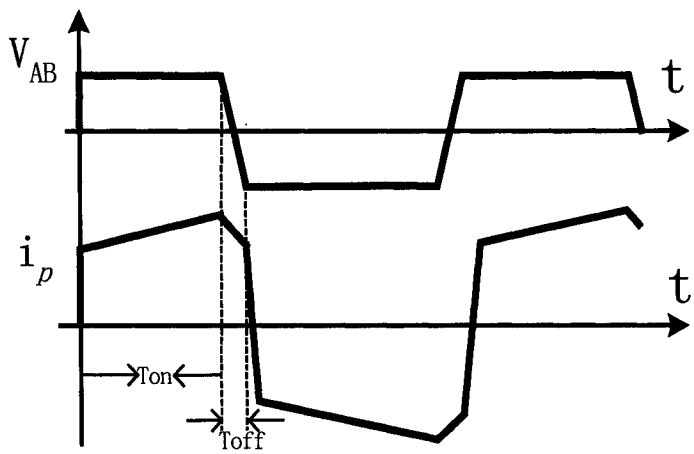



Fig. 3.6 (b) $T_{off} < T_R$

Fig. 3.6 Two operation manners for the proposed converter

Where, $I_o$ is the output current. $C_s$ value can be designed as $V_{pk-pk}$ = 10~20% $V_{in}$ at full load.

### 3.1.4 Simulation and Experimental Verification

To evaluate the proposed topology, simulation models and an experimental prototype have been built in the lab. As an example, the specification for the simulation and prototype is: $V_{in}$=36~75V, $V_{out}$=3.3V, Io=25A. The switching frequency is 200 kHz. For comparison, the conventional R/C series snubber and the proposed active-clamp snubber are simulated and tested based on the same conventional half-bridge converter simulation model and experimental prototype.

Fig. 3.7 shows the simulation waveforms of two snubbers. It can be seen that with the R/C series snubber, the half-bridge DC-DC converter suffers the damped voltage and current ringing shown in Fig 3.7(a). With the proposed active-clamp snubber, the ringing is eliminated, and clean waveforms can be observed in Fig. 3.7(b). The peak-to-peak voltage across the capacitor $C_s$ is around 5V.

For the experimental prototype, three paralleled MOSFETs (Si4420DY) are used as each synchronous rectifier. IRFS59N10D MOSFETs are used for the main switches $S_1$ and $S_2$, 30CTQ060S Schottky diodes are selected for $D_3$ and $D_4$ and Si4470EY MOSFETs are used for $S_3$ and $S_4$. The turns ratio of the planner transformer is 4:2 with 220nH leakage inductance on the primary. The capacitance value of the $C_s$ is 2uF. Driver IC HIP2100 is used to drive switches $S_1$ and $S_2$. A simple self-driving circuit based on the extra transformer windings is applied to switches $S_3$ and $S_4$.

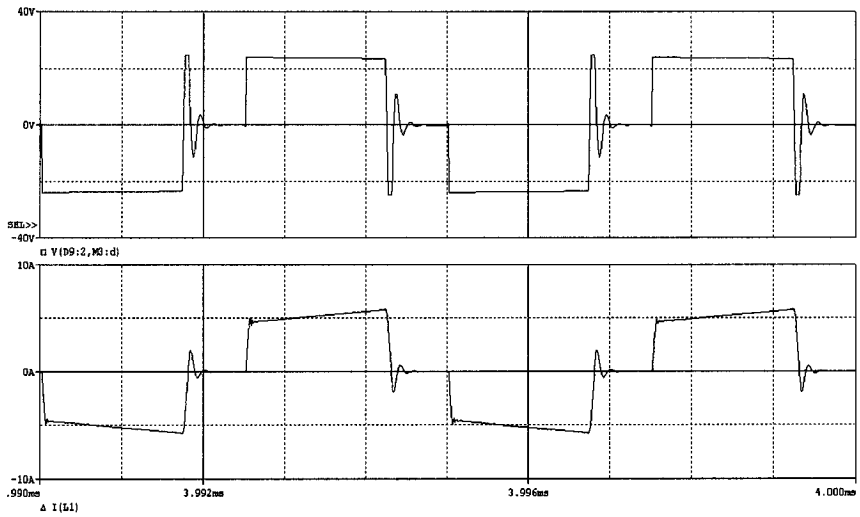



Fig. 3.7 (a) With the dissipative R/C series snubber

(Top trace: voltage $V_{AB}$; Bottom trace: primary current)

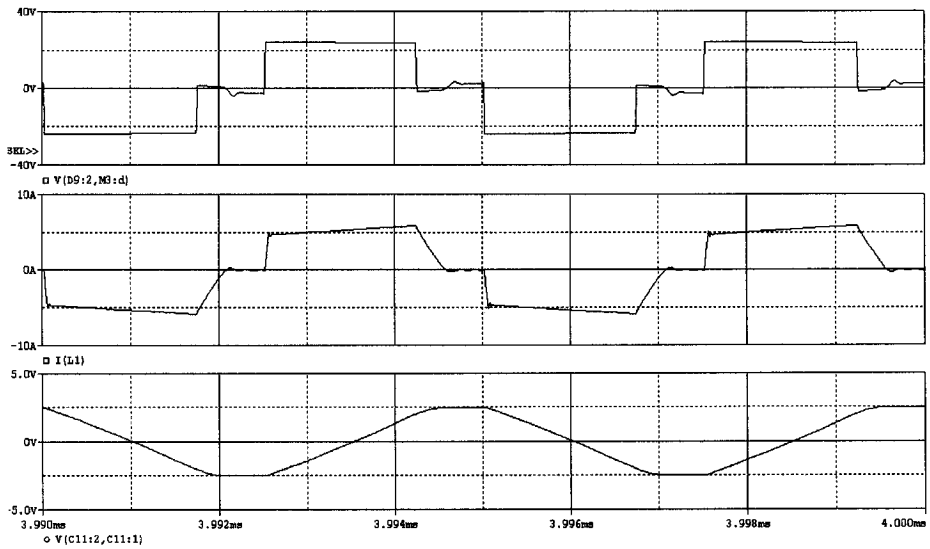



Fig. 3.7 (b) With the proposed active-clamp snubber

(Top trace: voltage $V_{AB}$; Middle trace: primary current; bottom trace: Cs voltage)

Fig. 3.7 Comparison between R/C snubber and the active-clamp snubber

The experimental waveforms at two different duty cycles are shown in Fig. 3.8 and Fig. 3.9. It can be observed that the ringing is attenuated with the help of the proposed active-clamp circuit, and the body diodes of the main switches have never been involved in any conduction or ringing.

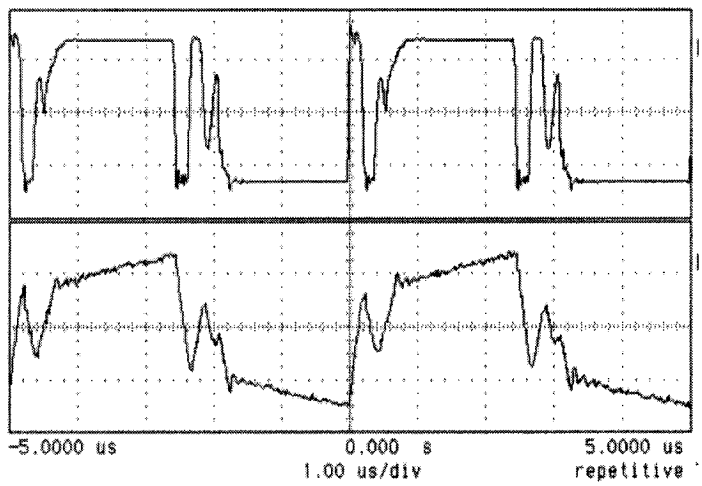



Fig. 3.8 (a) With the conventional R/C series snubber

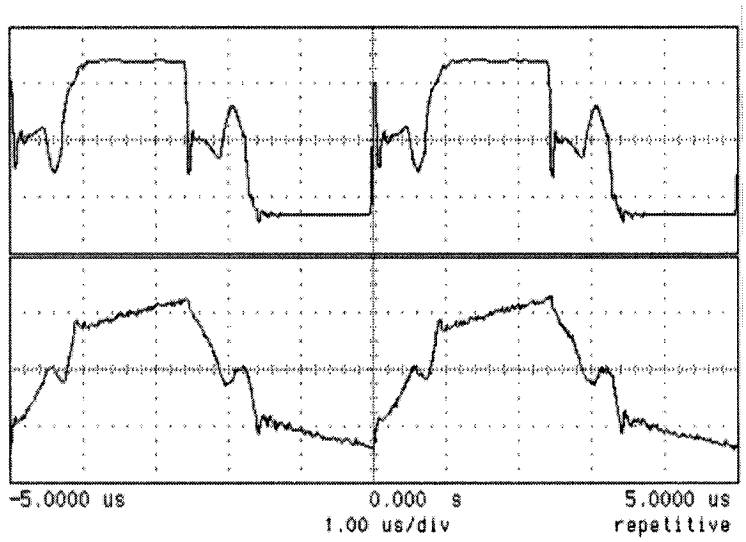



Fig. 3.8 (b) With the proposed active-clamp snubber

Fig. 3.8 Transformer voltage and current waveforms (D=0.37)
(Top trace Vab: 20V/div; Bottom trace $i_p$: 5A/div)

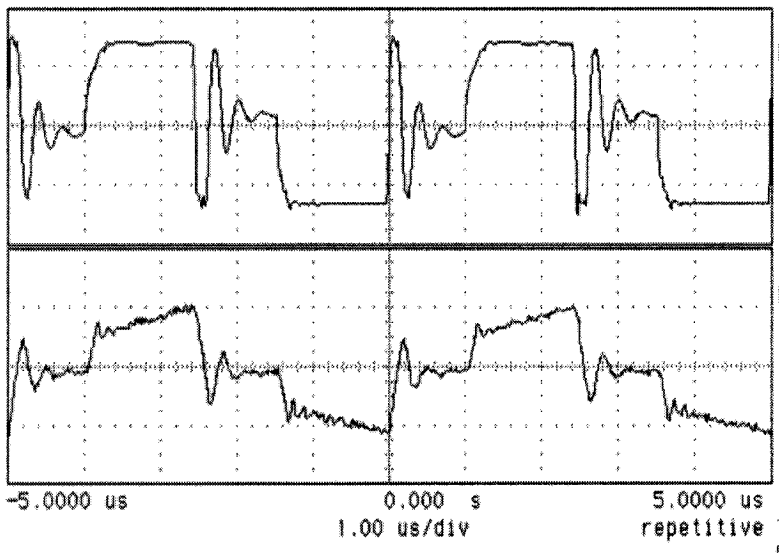



Fig. 3.9 (a) With the conventional R/C series snubber

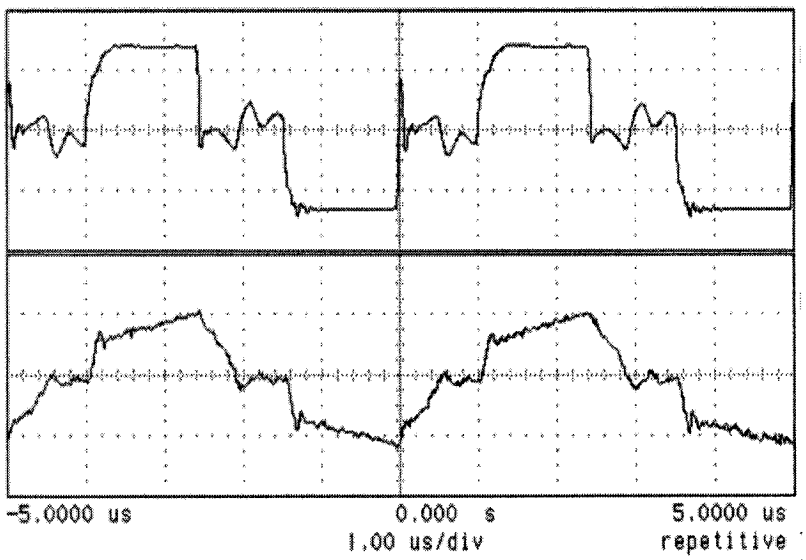



Fig. 3.9 (b) With the active-clamp snubber

Fig. 3.9 Transformer voltage and current waveforms (D=0.28)

(Top trace Vab: 20V/div; Bottom trace $i_p$: 5A/div)

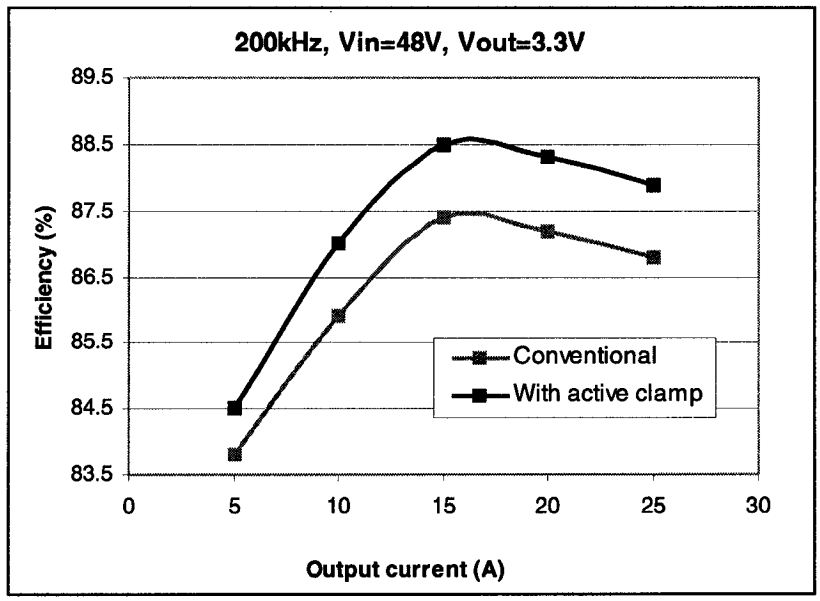



Fig. 3.10 Efficiency comparison for the two snubbers

Compared with the R/C series snubber, the body diode reverse-recovery losses and snubber losses are eliminated; hence, higher overall efficiency is expected with the proposed active-clamp converter. A comparison in efficiency is shown in Fig. 3.10, and it can be seen that one percent efficiency improvement is achieved through the active-clamp snubber compared with the conventional R/C series snubber.

### 3.1.5 Summary

A lossless active-clamp snubber circuit was proposed based on the isolated half-bridge DC-DC converter in the paper. The simulation and experimental results show that the transformer-leakage-inductance-related ringing is attenuated, and the primary-side body-diode reverse recovery is eliminated via the proposed active-clamp snubber. Also, efficiency is improved compared with a conventional R/C series snubber circuit. As a

matter of fact, this active-clamp topology has the same potential for high-input-voltage DC-DC converters.

## 3.2 Lossless Snubber Topologies for a Current Doubler Rectifier

Current doubler rectifier (CDR) is one of the best candidates for high-output-current and low-output-voltage DC-DC converters. In this subchapter, several conventional CDR snubber circuits are evaluated, and two passive lossless snubber circuits for the CDR are proposed to reduce the reverse-recovery-related losses and clamp the voltage spikes across the rectifiers. The snubber circuits are tested and verified experimentally, and higher efficiency is achieved compared with the conventional resistive snubbers.

### 3.2.1 Background

In isolated DC-DC converters, soft-switching techniques are mainly used on the primary side to reduce the switching losses [C1, C4 ~ C7]. Active-clamp forward and Phase-shift full bridge are examples that achieve Zero-Voltage-Switching (ZVS) using parasitic parameters such as transformer leakage inductance and switches junction capacitances. However, in such topologies, output rectifiers usually operate at hard switching conditions resulting in reverse-recovery-related ringing and diodes turn-off losses.

To reduce diode reverse peak currents, leakage inductance or additional inductance can be used to reduce the reverse di/dt in diodes. However, the increased inductance results in increased ringing due to the oscillation between the inductance and rectifier junction capacitances. In other words, when the diodes (including body diodes of

synchronous rectifiers) are reversed and turned off, the extra energy stored in the inductance charges the rectifier junction capacitances resulting in voltage spike and oscillation.

Resistor-Capacitor (RC) or Resistor-Capacitor-Diodes (RCD) snubber circuits are usually used to damp the ringing and limit the voltage spikes. However, the losses dissipated in such snubber circuits become more significant with the increase of the switching frequency.

Recently, an active clamp snubber was proposed to recover the energy in an oscillatory manner [C14]. The disadvantage of such snubber is that an active switch is needed with its associated driving circuitry, which increases the complexity. Compared with active snubbers, passive lossless snubbers are simpler, cost less and are more reliable since there is no need to control the active switches. Lossless snubber circuits are widely investigated in non-isolated boost and boost-derived circuits to reduce diode reverse recovery losses [C10, C11]. However, little research has been done on the snubber for the current doubler rectifiers.

The current doubler with synchronous rectification (SR) is a good candidate for low-voltage high-output-current DC-DC converters. The body diodes of MOSFETs have undesirable reverse-recovery characteristics, which significantly increase the diodes turn-off switching losses on the secondary side compared with Schottky diodes, especially at higher switching frequencies. Therefore, lossless snubbers are one of the solutions to reduce the reverse recovery losses. In this subchapter, several candidate snubbers for current doubler rectification are investigated, and two passive lossless snubber circuits are proposed to reduce the reverse-recovery losses while clamping the voltage spike.

Theoretical analysis and design considerations are presented also. Experimental results verify that the proposed snubbers improve converter efficiency and provide the converter with the potential to operate at higher switching frequencies.

### 3.2.2 Review of State-of-the-Art Snubber Techniques for Current Doubler Rectifiers

As discussed in Chapter 1, the central-tapped rectifier and current-doubler rectifier are widely used for low-voltage high-current isolation DC-DC converters. Generally, snubber circuits for central-tapped rectifiers may be used in current doubler rectifiers. The means to attenuate reverse recovery in non-isolated topologies can be employed for a current doubler rectifier.

#### 3.2.2.1 Dissipative Snubber Circuits

Due to the reverse recovery of a rectifier (body) diode, when a diode turns off, the diode suffers a reverse-recovery turn-off loss and related ringing. The ringing may degrade converter efficiency and lead to EMI issues. To damp the ringing, a dissipative snubber is most popularly employed.

RC and RCD snubber circuits are the simplest snubbers, and they are usually connected in parallel with switches or diodes. Fig. 3.11 shows two types of RC snubber circuits in current doubler rectifiers, where $D_1$ and $D_2$ are rectifier diodes, and $L_k$ is the transformer leakage inductance. As shown in Fig. 3.11(a), two RC snubbers are individually connected in parallel with two diodes in the current doubler. In fact, two RC snubbers can be combined into one as shown in Fig. 3.11(b). Several RCD snubber circuits are shown in Fig. 3.12.

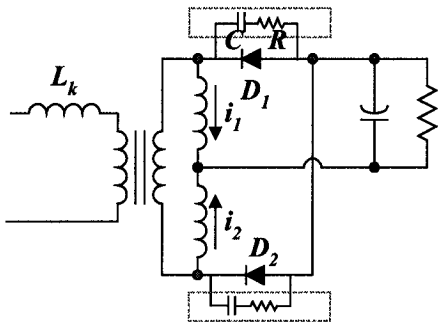



Fig. 3.11 (a) Type I

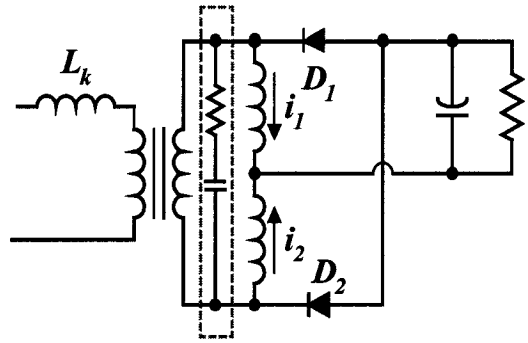



Fig. 3.11 (b) Type II

Fig. 3.11 RC snubber circuits for a current doubler rectifier

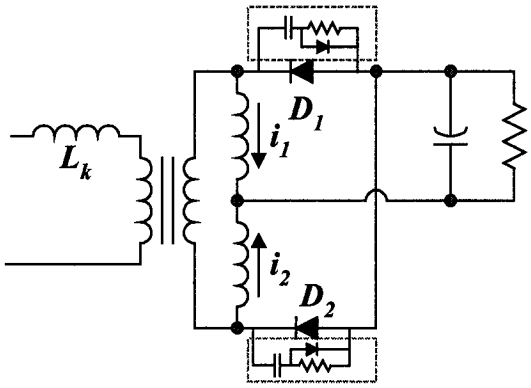



Fig. 3.12 (a) Type I

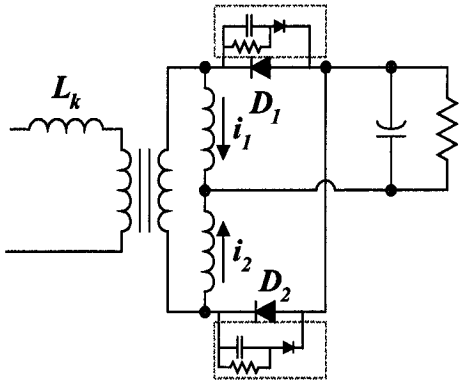



Fig. 3.12 (b) Type II

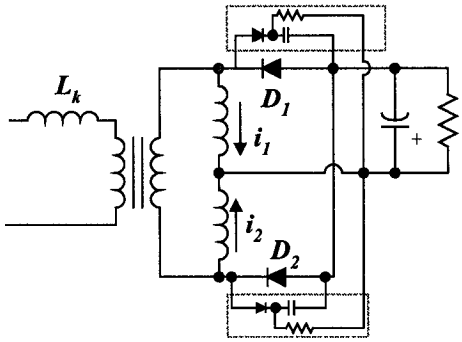
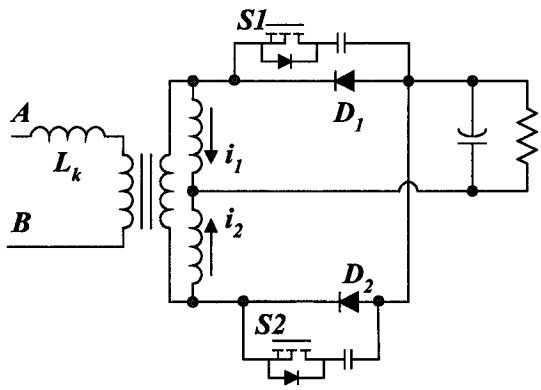



Fig. 3.12 (c) Type III

Fig. 3.12 RCD snubber circuits

3.3.2.2 Active-Clamp Snubber Circuit

As mentioned above, resistive snubber circuits extinguish the potential ringing by dissipating the redundant energy. An active snubber for full-bridge rectification was presented in [C14], where only an active switch and a capacitor are used as a snubber. In resonant manner, resonant manner, the reverse-recovery-related energy can be recycled instead of dissipated in a resistive snubber. A similar concept can be used in the current doubler rectification as shown in Fig. 3.13, where two active switches and two capacitors are used as snubbers. However, two active switches and related drive circuitry complicate the snubber.



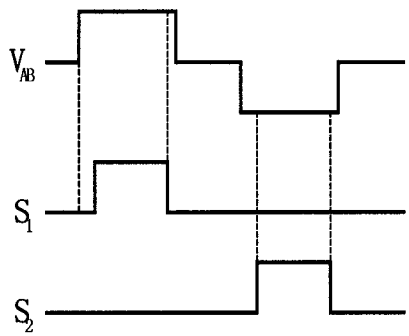




Fig. 3.13 (a) Circuits Fig. 3.13 (b) Driving waveforms of the active switches

Fig. 3.13 Active-clamp lossless snubber

3.2.2.3 Reactor Snubber Circuits

The secondary-side ringing is the result of the reverse recovery of the rectifiers. The reverse di/dt through the diodes is one of the critical factors to affect the reverse peak current. The larger reverse di/dt means the higher the reverse recovery peak current. In Fig. 3.14, it shows two kinds of reactor snubber circuits. In Fig. 3.14(a), a linear reactor is

series connected with a diode to limit the di/dt slope, thus reducing the reverse peak current.

The diodes and capacitors in snubbers are utilized to clamp the voltage spike across diodes and recycle the reverse-recovery-related energy. The snubber is theoretically lossless if the core losses in reactors and the conduction losses in snubber diodes are neglected. Unfortunately, the snubber diodes $D_{s1}$ and $D_{s2}$ carry currents before the current is shifted from $D_{s1}$, $D_{s2}$ to $D_1$. The current-shifting time is determined by the charging interval of the inductor $L_1$ via the capacitor Cs, and actually, this time interval is significantly long, such that conduction losses through diodes cannot be neglected — especially when synchronous rectifier is used in low output-voltage applications. Furthermore, linear reactors also limit the forward di/dt slope so that duty cycle loss is inevitable.

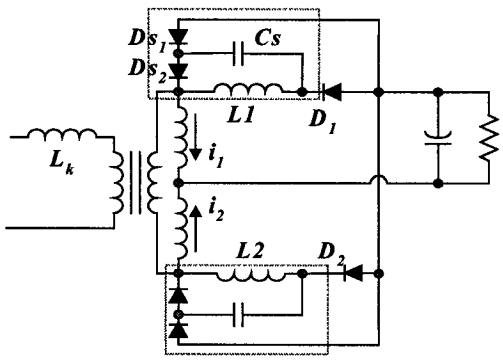



Fig. 3.14 (a) Linear reactor snubber

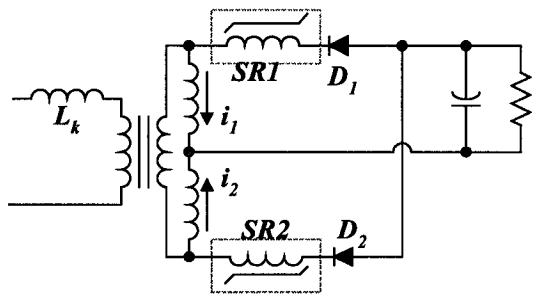



Fig. 3.14 (b) Saturable reactor snubber

Fig. 3.14 Reactor snubber circuits

To reduce the duty cycle loss, the saturable reactor snubber shown in Fig. 3.14(b) is used instead of a linear reactor snubber. Because the saturable reactor has high inductance when the current through the reactor is small, the di/dt is significantly reduced when the diode intends to reverse recover. The duty cycle loss is reduced because of the decreased inductance with the increased inductor current. The main drawback is high temperature rise in the saturable reactor, which may result in a thermal management issue.

### 3.2.3 Passive Lossless 2D-1C Snubber Topology

As discussed in the previous section, in the active snubber and reactor snubber circuits, there are no dissipative components and snubbers are theoretically lossless. Active snubbers are complicated due to the extra active switches and extra driving circuitry. Passive reactor snubbers, as shown in Fig. 3.13, have bulky inductors and an undesirable capacitor and diodes. Two passive, lossless snubbers comprised only of capacitors and diodes are proposed, one of them is named 2D-1C snubber, and the other is named 3D-2C snubber.

A two-diode, one-capacitor (2D-1C) snubber topology is proposed, as shown in Fig. 3.15, which consists of a capacitor $C_s$ and two diodes $D_{s1}$ and $D_{s2}$. Considering the symmetry of two sets of snubber topologies, only a snubber is analyzed as follows with the corresponding equivalent circuits shown in Fig. 3.16.

***Mode 1*** *($t_0<t<t_1$)*: No voltage is applied to the transformer primary side, and the inductor currents freewheel through $D_1$ and $D_2$.

***Mode 2*** *($t_1<t<t_2$)*: At $t = t_1$, a voltage is applied to the transformer's primary side, and leakage inductance is linearly charged due to the short circuit in the transformer

secondary side, and the current change slope is $V_{AB}/L_k$. At the same time, the current through $D_1$ decreases and the current through $D_2$ increases until $D_1$ current goes negative and reaches reverse peak current. During the reverse recovery interval, the primary leakage current is:

$$i_p = \frac{1}{n}(i_1 + i_{rr}) \qquad (3\text{-}8)$$

Where, $i_{rr}$ is the reverse current through the diode $D_1$, and $n$ is a transformer turns ratio.

***Mode 3 and Mode 4*** *($t_2<t<t_3$)*: At t= $t_2$, the diode $D_1$ is turned off and capacitor $C_s$ is charged as shown in Mode 3. Considering that the voltage across capacitor $C_s$ may exceed the transformer secondary voltage, capacitor $C_s$ may discharge as shown in Mode 4. Mode 3 and Mode 4 may go back and forth alternatively, and in each charging mode, some leakage inductance energy is transferred to the output. Hence, the oscillation is damped by the charging-discharging resonant behaviors as shown in Fig. 15(b).

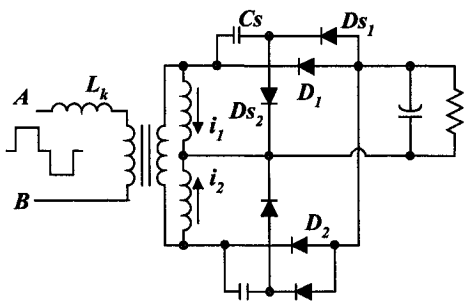



Fig. 3.15 (a)

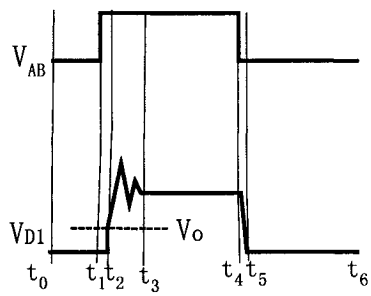



Fig. 3.15 (b)

Fig. 3.15 2D-1C snubber circuits

It should be noted that the reason for the leakage inductance energy transfer to the output by resonant behavior is because the charging and discharging paths are different. The output capacitor is not included in the discharging path, so the energy may be

pumped to output without discharging back. Actually, this is the basic concept for the two passive snubbers presented in this chapter.

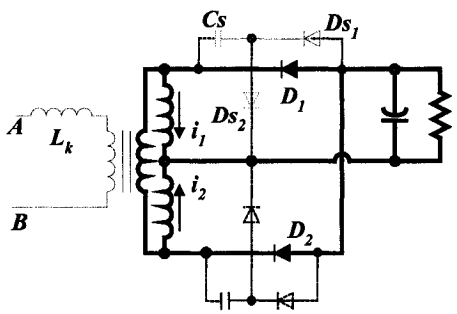



Fig. 3.16 Mode 1 ($t_0<t<t_1$)

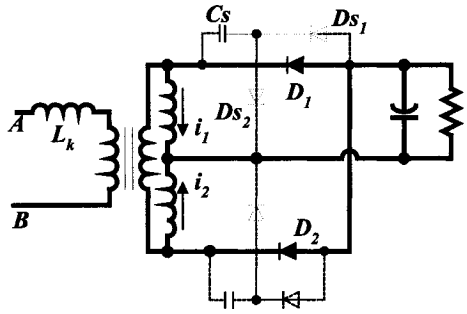



Fig. 3.16 Mode 2 ($t_1<t<t_2$)

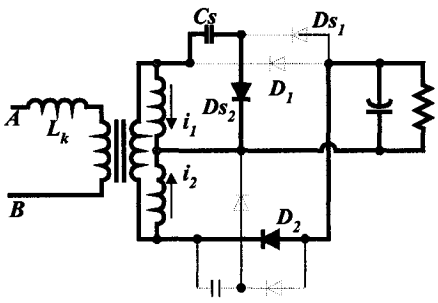



Fig. 3.16 Mode 3 ($t_2<t<t_3$)

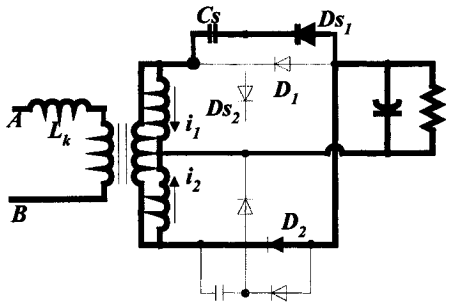



Fig. 3.16 Mode 4 ($t_2<t<t_3$)

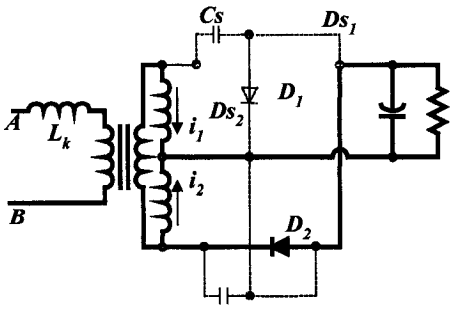



Fig. 3.16 Mode 5 ($t_3<t<t_4$)

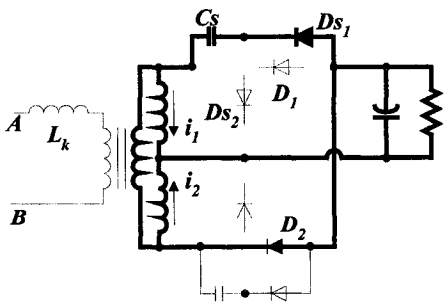



Fig. 3.16 Mode 6 ($t_4<t<t_5$)

Fig. 3.16 Operational modes of the 2D-1C snubber topology

***Mode 5*** *($t_3<t<t_4$)*: The oscillation stopped by the voltage across capacitor $C_s$ is equal to the transformer secondary-side voltage. During the interval, the diode $D_1$ is blocked and the energy is delivered from the input to the output.

***Mode 6*** *($t_4<t<t_5$)*: When the primary-side voltage $V_{AB}$ drops to zero, the primary-side current decreases, and the capacitor $C_s$ is discharged through the diode $Ds_1$ until the voltage across capacitor $C_s$ is discharged to zero. By this way, the energy in the capacitor $C_s$ is recycled to the load. Then, the circuit goes into freewheeling mode as in Model 1.

### 3.2.4 Passive Lossless 3D-2C Snubber Topology

There are two main limitations in the 2D-1C snubber circuit presented above. One limitation is that the output capacitor is involved in the charging path of the snubber capacitor, which results in extra output voltage ripple across the output capacitor. The other drawback is that when a rectifier diode is turned off, the reverse voltage across a rectifier diode rises from the value of the output voltage instead of zero. This means that rectifier diodes are turned off at hard-switching instead of soft-switching conditions.

In Fig. 3.17, a three-diode two-capacitor (3D-2C) passive snubber is proposed to solve such issues, where two capacitors in a snubber have an identical capacitance value. This snubber operates in a similar manner as the 2D-1C snubber shown in Fig. 3.15. To simplify, only the charging and discharging equivalent circuits are shown in Fig.3.18. In the charging mode shown in Fig. 3.18(a), when the rectifier diode turns off, the leakage inductance current charges capacitor $C_1$ and $C_2$ through diode $D_{s2}$, and thus, the leakage inductance energy is transferred in the two capacitors. In the discharging mode as shown

in Fig. 3.18(b), the energy stored in the capacitors $C_1$ and $C_2$ is released to output load when the current doubler rectifier starts to freewheel.

Therefore, the snubber network recovers the leakage inductance energy resulted from the reverse recoveries of rectifier diodes. Moreover, when a rectifier diode turns off, voltage across the rectifier diode rises from zero, so ZVS turn-off is achieved for the diode reverse recovery. In other words, reverse-recovery switching losses in rectifier diodes are reduced.

Considering the resistance in charging and discharging paths, when rectifier diodes turn off, the peak voltages across the rectifier diodes are smaller than twice the transformer secondary voltage. Because capacitor $C_1$ and $C_2$ have the equal value, the peak voltage across each capacitor is smaller than the transformer secondary voltage. Considering the possible discharging path shown in Fig. 3.18(b), and noting that the voltage across capacitor $C_1$ and $C_2$ is smaller than the transformer secondary voltage, no discharging behavior happens in the power-delivering mode, while the voltage $V_{AB}$ is applied to the transformer primary side. Therefore, no reverse-recovery ringing occurs when the rectifier diode turns off. The ideal voltage waveform is shown in Fig. 3.17(b). When the transformer primary-side voltage $V_{AB}$ decreases towards zero, a part of inductor current $i_1$ starts to go through the discharging path as shown in Fig. 3.18(b). Thus, the energy in the snubber capacitors is recycled to the output load.

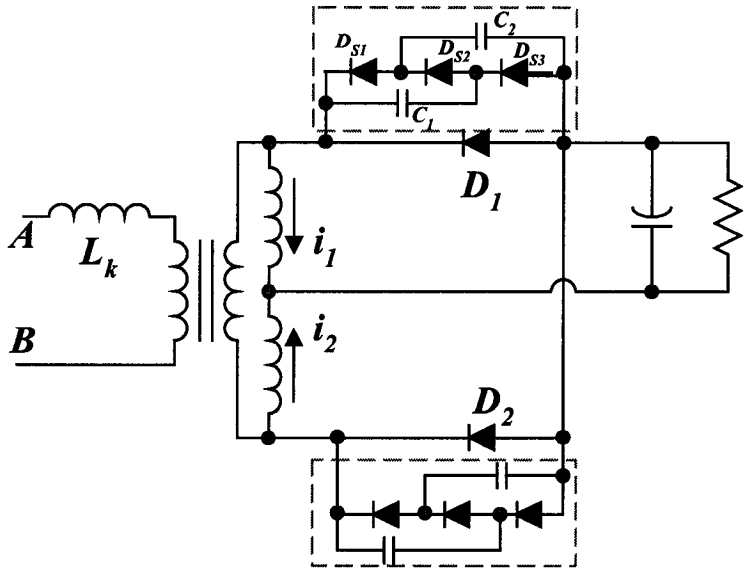



Fig. 3.17 (a)

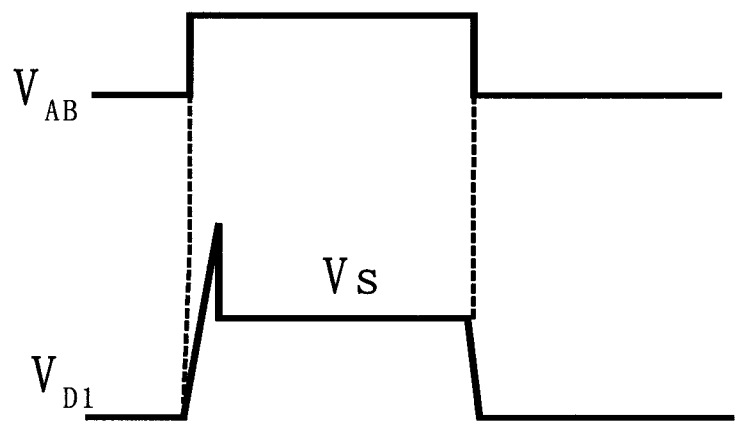



Fig. 3.17 (b)

Fig. 3.17 3D-2C snubber circuit

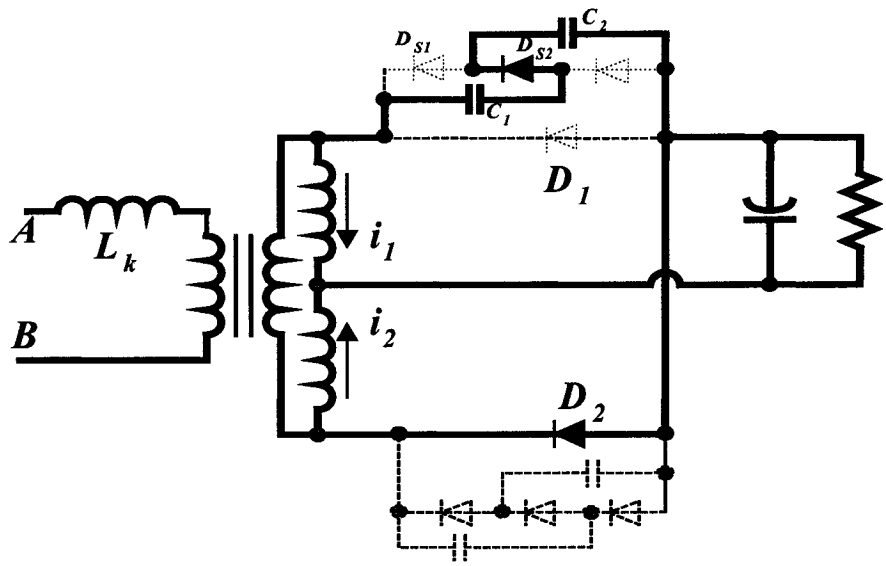



Fig. 3.18 (a) Snubber charging mode

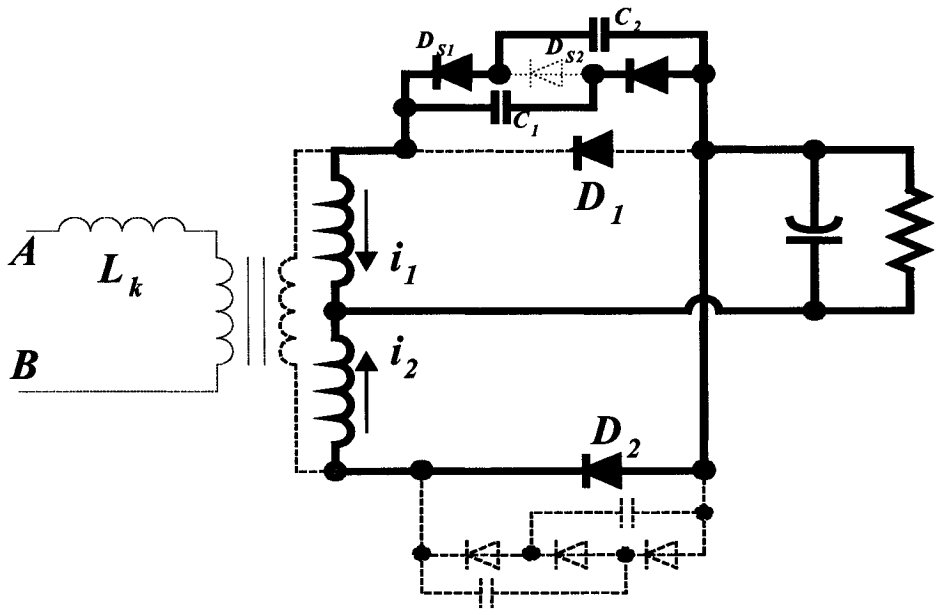



Fig. 3.18 (b) Snubber discharging mode

Fig. 3.18 Two key modes of operation

### 3.2.5 Experimental Comparison

An isolated half-bridge DC-DC converter, as shown in Fig. 3.19 is built to evaluate the two proposed lossless snubbers. The prototype specifications are: Vin=36~75V, Vout=3.3V and Iout=25A. Synchronous rectifiers are used in the secondary side instead of Schottky diodes. Conventional symmetric control is applied to primary-side switches; $SR_1$ and $SR_2$ are driven with external signals from primary side.

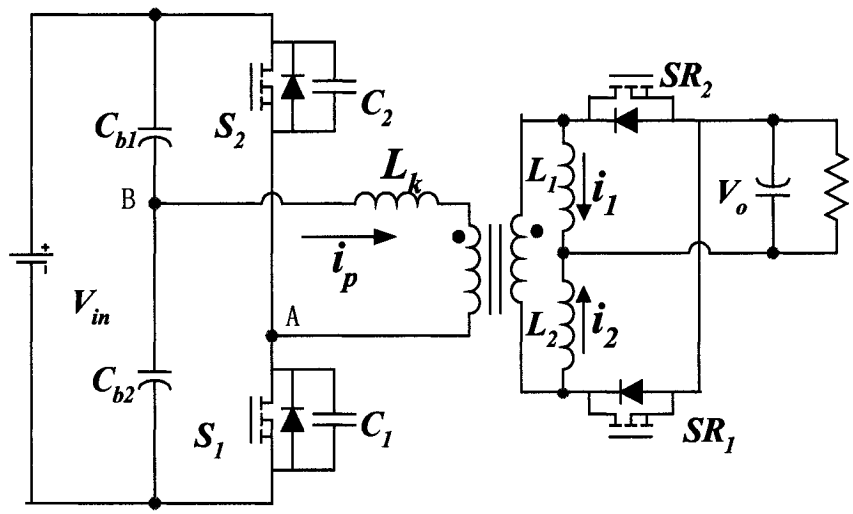



Fig. 3.19 Experimental half-bridge DC-DC converter

Fig. 3.20 shows the experimental waveforms of the drain-to-source voltage and gate voltage of a synchronous rectifier when RC and RCD snubber circuits are used. When R is infinite, which means the snubber is disconnected, the waveforms are as shown in Fig. 3.20(a). The significant ringing occurs due to the oscillation between the transformer leakage inductance and junction capacitance of the synchronous rectifier. This high frequency ringing may result in EMI issue.

Fig. 3.20(b) shows waveforms of the RC snubber at R=11ohm and C=4700pF. It can be seen that an oscillation is damped quickly and the ringing is eliminated. Fig. 3.20(c) shows the waveforms with the RCD snubbers, which are close to the RC snubbers.

Fig. 3.21 shows the waveforms using the two proposed passive lossless snubbers. From Fig. 3.21(a), we can see minor ringing that agrees with the theoretical analysis in the previous section. In Fig. 3.21(b), there is a voltage overshoot across the synchronous rectifier, but ringing is eliminated, which is close to the theoretical waveforms shown in Fig. 3.17(b). Efficiencies are measured with the different snubber circuits applied to the same power stage. Fig. 3.22 shows the measured efficiency curves. It can be observed that the RC and RCD snubbers have almost similar efficiencies, and the 2D-1C snubber has higher efficiency that is around 1.5 percent higher than the conventional RC snubber at full load. The 3D-2C snubber achieves 1 percent improvement in efficiency at full load compared with the conventional RC or RCD snubber.

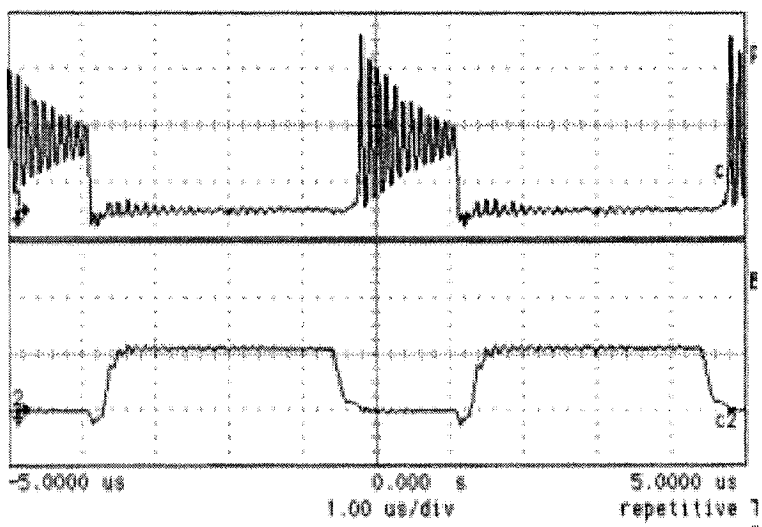



Fig. 3.20 (a) Without snubber (10V/div)

(Top trace: Vds; Bottom trace: Vgs)

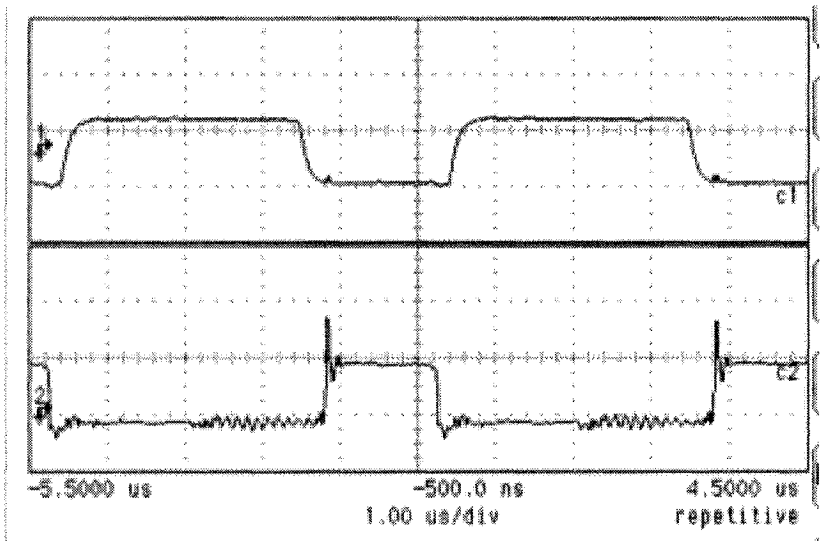



Fig. 3.20 (b) RC snubber (R=11ohm, C=4700pF)

(Top trace: Vgs; Bottom trace: Vds; 10V/div)

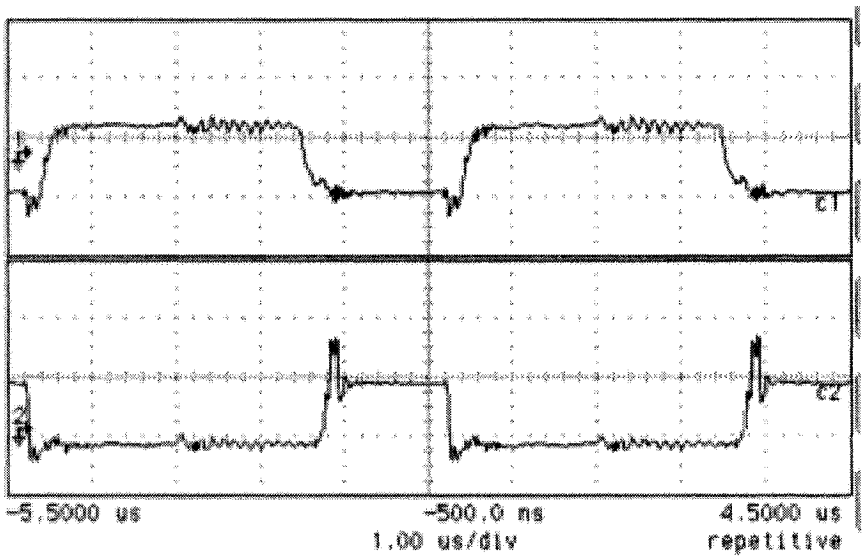



Fig. 3.20 (c) RCD snubber (R=20 ohm, C=4700pF)

(Top trace: Vgs; Bottom trace: Vds; 10V/div)

Fig. 3.20 Waveforms of the RC and RCD snubbers

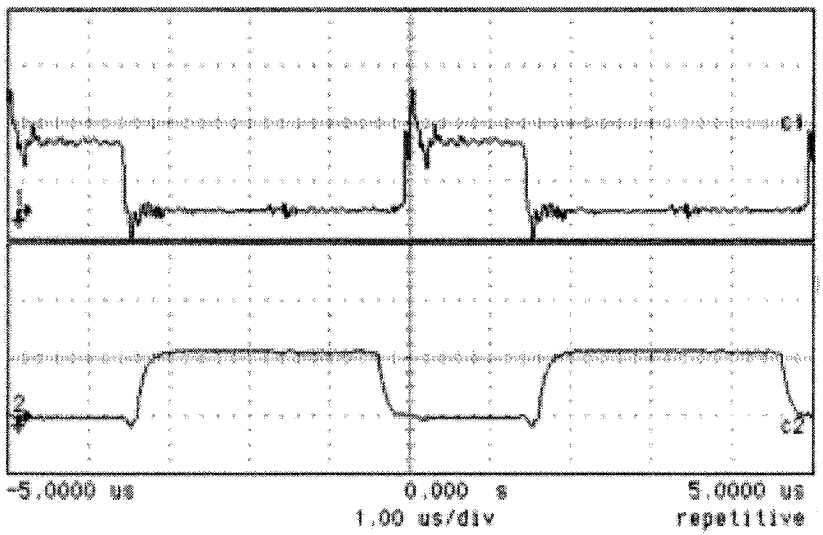



Fig. 3.21 (a) With 2D-1C snubber

(Top trace: Vds; Bottom trace: Vgs; 10V/div)

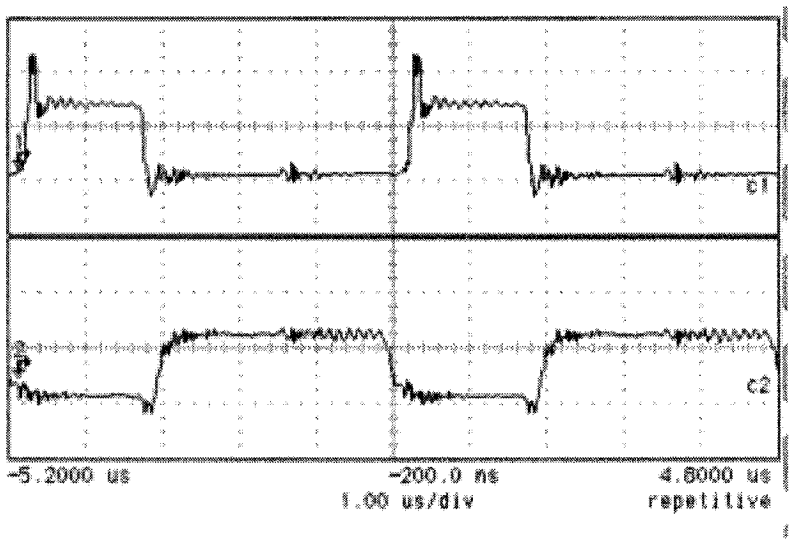
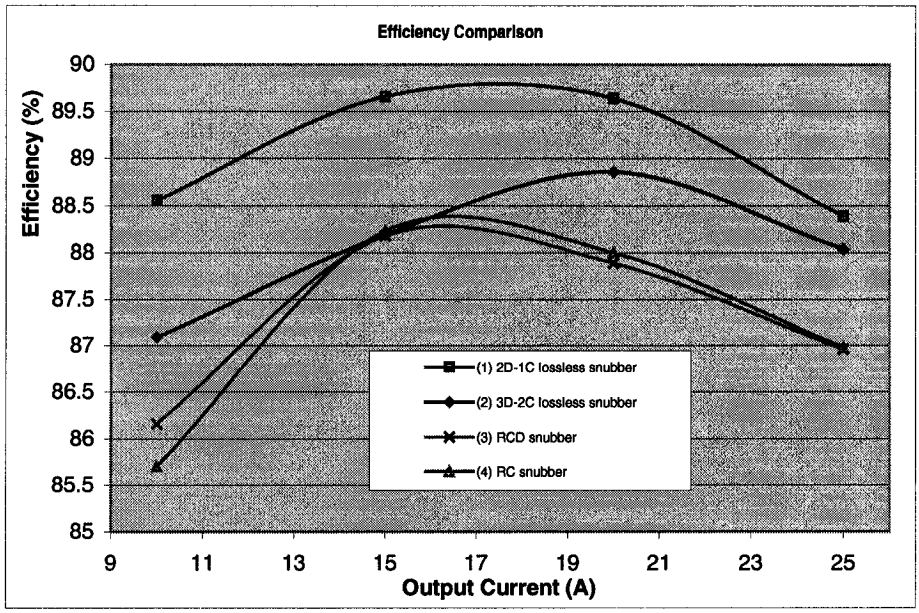



Fig. 3.21 (b) With 3D-2C snubber

(Top trace: Vds; Bottom trace: Vgs; 10V/div)

Fig.3. 21 Waveforms of the proposed snubbers




(From top to bottom: (1) (2) (3) (4) curves)

Fig. 3.22 Efficiency comparison of snubbers (fs=200kHz)

### 3.2.6 Summary

Two passive lossless snubber circuits for current doubler rectification are proposed and analyzed. It is shown that both proposed 2D-1C and 3D-2C snubber circuits attenuate the ringing and clamp voltage spikes of rectifier diodes because of their "unidirectional" architecture. Since the proposed snubbers have limited losses, higher efficiencies are achieved compared with the conventional RC or RCD snubbers.

# 4. MODELING OF ISOLATED DC-DC CONVERTERS

For low-output voltage and high-output current applications, multi-channel technology is a preponderant solution for transient response and thermal management in DC-DC converters. In these converters, the current sharing is critical, because non-uniform current distribution can lead to non-uniform thermal distribution, thus resulting in degraded converter performance. In this chapter, a unified steady-state model is built for both symmetric and asymmetric half-bridge DC-DC converters. Based on the model, current-sharing issues and transformer DC current bias issues are investigated.

Fast transient response is urgently required for the power management of microprocessors. VR (M) technologies are targeting the transient response with di/dt up to 1A/1nS to meet next-generation microprocessor powering requirements. Even though the transient response requirement for isolated DC-DC converters is not as urgent as VR, power management with fast, dynamic response is becoming one of the most important specifications for telecom customers. In this chapter, a dynamic model for isolated bridge DC-DC converters is built. Output impedance and transient response are analyzed based on the model.

## 4.1 Unified Steady-State DC Model of Half-Bridge DC-DC Converters

### 4.1.1 Introduction

For the on-board DC-DC converters, output voltage will continue to decrease with increasing output current. For isolated low-output-voltage topologies, the secondary-side

power losses are dominant, and therefore they have a major effect on conversion efficiency. To maximize conversion efficiency, it is necessary to reduce the secondary-side conduction losses. The secondary-side current-doubler rectification topology can minimize the secondary-winding *rms* current and has better thermal management for the output inductors [D1-D2]. Moreover, the current-doubler scheme minimizes the number of high-current interconnections that simplify the secondary layout and further reduce the layout-related losses [D2].

The current-doubler rectification (CDR) can be used with nearly all topologies, such as the forward, half-bridge, push-pull, and full-bridge. For the half-bridge (HB) topology, the voltage rating of switching devices is one-half of that required by push-pull and forward converters. In addition, it has efficient utilization of transformer core and copper, and the leakage inductance energy can be recycled to the input capacitors. Therefore, HB converter with CDR is suited for high-current, low-voltage applications [D9].

The dynamic modeling and analyses of symmetric and asymmetric (complementary) HB DC-DC converters are well studied [D3-D5]. However, most literature does not completely take parasitic parameters into account when deriving models of converters. Much of the available literature focuses on the half-bridge analysis with center-tapped instead of current-doubler rectification.

As a matter of fact, a current-doubler rectifier behaves like two isolated buck converters in parallel. Under ideal symmetric condition, two inductor channels should carry identical currents. However, due to the asymmetric resistive parameters of the two channels, both inductors carry uneven currents, which have a significant impact on the

thermal balance and rectifier efficiency [D7]. So far, few literature addresses this current-unbalance issue in the current-doubler rectifier. Moreover, the unwanted DC bias of the transformer magnetizing current may lead to failure of the magnetic core due to saturation [D6]. It is very important to estimate the DC bias of the magnetizing current so that the DC bias can be considered in the original transformer design. The DC bias of the magnetizing current is discussed in the asymmetric half-bridge DC-DC converter with the center-tapped rectification [D5]. Actually, for the symmetric HB DC-DC converter with current doubler rectification, the DC current bias of the transformer also exists.

A unified average state-space model is built for the half-bridge DC-DC converter with current doubler rectification while taking into consideration the parasitic parameters employing the state-space averaging concept described in [D8]. Based on the DC model, a number of important issues with current doubler rectification in both symmetric and asymmetric HB DC-DC converters, such as the current sharing of two output inductors, the DC bias of magnetizing current, related design guidelines of PCB layout, will be presented in depth in terms of numerical equations. Experimental and simulation results come to an agreement with theoretical analysis.

### 4.1.2 DC Modeling of Half-Bridge DC-DC Converters

The conventional half-bridge DC-DC converter with current doubler rectifier (CDR) is shown in Fig. 4.1, where synchronous rectifier (SR) is utilized to reduce conduction losses for low-voltage and high-current applications. The converter may operate under symmetric or asymmetric control. Neglecting the leakage inductance and transient

commutation, and considering that the converter is operating at CCM mode due to the synchronous rectifier, the converter has three typical modes as shown in Fig. 4.2 through Fig. 4.4. In these figures, the load is assumed as a constant current source since the voltage ripple can be ignored. $R_{L1}$ and $R_{L2}$ are equivalent DC resistance of inductor $L_1$ and $L_2$, respectively. $R_c$ is the ESR of output capacitors. $R_T$ is the equivalent resistance of the reflected switches on-resistance and DCR of transformer winding.

In a switching cycle, the converter can be denoted to use three linear state-space equations, respectively. The three corresponding space-state equations can be expressed as Equation (4-1): Where, $x$ is the vector of state variables and $u$ is the vector of independent sources. During the on-time of switch $S_1$, the corresponding matrices are $A_1$ and $B_1$; during the on-time of switch $S_2$, the corresponding matrices are $A_2$ and $B_2$; during the off-time of both switch $S_1$ and $S_2$, the corresponding matrices are $A_3$ and $B_3$.

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \tag{4-1}$$

where $\dot{x} \neq \frac{dx}{dt}$. For convenience, the definition is as follows:

$$\dot{x} = \begin{bmatrix} (C1+C2)\frac{dv_{C1}}{dt} \\ L1\frac{di_{L1}}{dt} \\ L2\frac{di_{L2}}{dt} \\ C\frac{dv_C}{dt} \\ L_m\frac{di_m}{dt} \end{bmatrix} \quad ; \quad x = \begin{bmatrix} v_{C1} \\ i_{L1} \\ i_{L2} \\ v_C \\ i_m \end{bmatrix} ; \quad u = \begin{bmatrix} V_{in} \\ I_o \end{bmatrix}$$

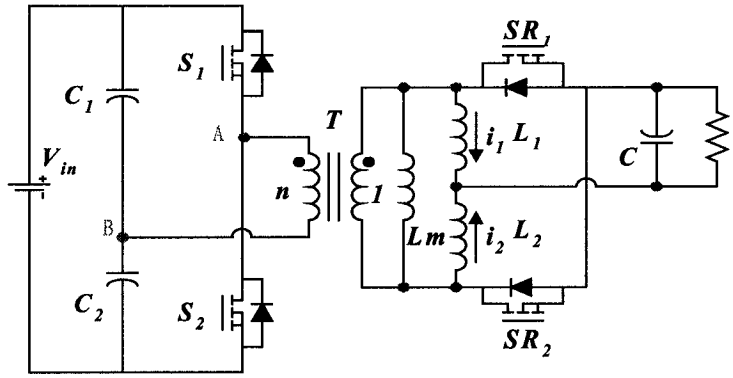



Fig. 4.1 CDR half-bridge DC-DC converter

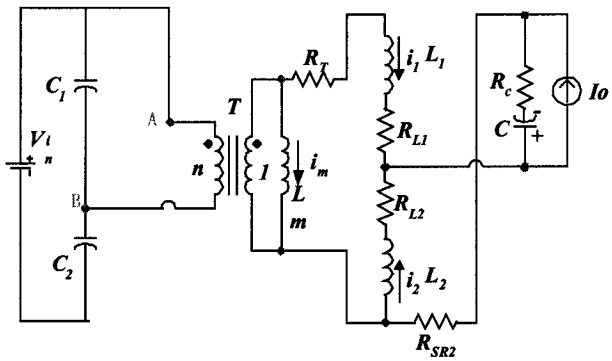



Fig. 4.2 Mode 1: S1 is on

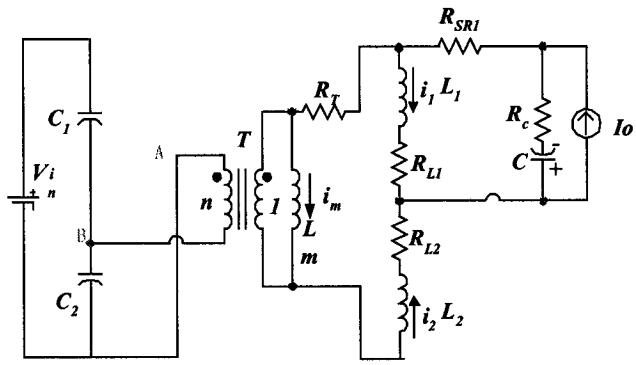



Fig. 4.3 Mode 2: S2 is on

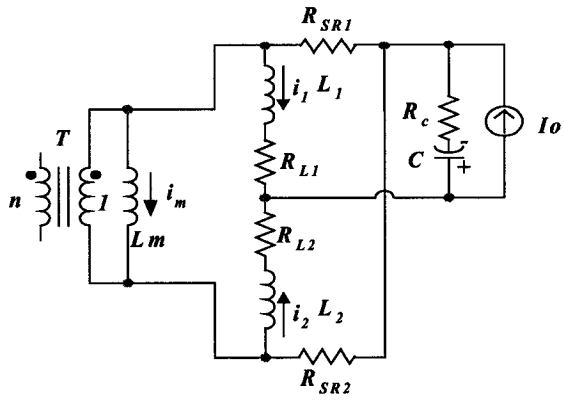



Fig. 4.4 Mode 3: Both S1 and S2 are off

During the on-time of Switch $S_1$, the corresponding matrices $A_1$ and $B_1$ are as follows:

$$A_1=\begin{bmatrix} 0 & \frac{1}{n} & 0 & 0 & \frac{1}{n} \\ \frac{1}{n} & -(R_{L1}+R_C+R_{SR2}+R_T) & -(R_C+R_{SR2}) & -1 & 0 \\ 0 & -(R_C+R_{SR2}) & -(R_{L2}+R_C+R_{SR2}) & -1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_1=\begin{bmatrix} 0 & 0 \\ 0 & R_C \\ 0 & R_C \\ 0 & -1 \\ 0 & 0 \end{bmatrix} \tag{4-2}$$

During the on-time of switch S2, the corresponding matrices $A_2$ and $B_2$ are as follows:

$$A_2=\begin{bmatrix} 0 & 0 & \frac{1}{n} & 0 & -\frac{1}{n} \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -(R_C+R_{SR1}) & -1 & 0 \\ -\frac{1}{n} & -(R_C+R_{SR1}) & -(R_{L2}+R_C+R_{SR1}+R_T) & -1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_2=\begin{bmatrix} 0 & 0 \\ 0 & R_C \\ \frac{1}{n} & R_C \\ 0 & -1 \\ -\frac{1}{n} & 0 \end{bmatrix} \tag{4-3}$$

During the off-time of both switch S1 and switch S2, the corresponding matrices $A_3$ and $B_3$ are as follows:

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -R_C & -1 & -R_{SR1} \\ 0 & -R_C & -(R_{L2}+R_C+R_{SR2}) & -1 & R_{SR2} \\ 0 & 1 & 1 & 0 & 0 \\ 0 & -R_{SR1} & R_{SR2} & 0 & -(R_{SR1}+R_{SR2}) \end{bmatrix}; \quad B_3 = \begin{bmatrix} 0 & 0 \\ 0 & R_C \\ 0 & R_C \\ 0 & -1 \\ 0 & 0 \end{bmatrix} \tag{4-4}$$

Assuming the switch $S_1$ on-time is $d_1$*T, switch $S_2$ on-time is $d_2$*T and the switching cycle is T. The key concept in state-space averaging is the replacement of the above three sets of state-space equations by a single equivalent set.

$$\dot{x} = Ax + Bu \tag{4-5}$$

Where, the equivalent matrices are defined by:

$$A = d_1A_1 + d_2A_2 + (1-d_1-d_2)A_3 \tag{4-6}$$

$$B = d_1B_1 + d_2B_2 + (1-d_1-d_2)B_3 \tag{4-7}$$

$$U = [V_{in} \quad I_o]^T \tag{4-8}$$

So far, a unified, averaging state-space model for both symmetric and asymmetric half-bridge DC-DC converter has been established.

### 4.1.3 DC Analysis of Symmetric Half-Bridge DC-DC Converter

From the average state-space matrices, the steady-state solution, with DC values indicated by capital letters, is obtained by setting $\dot{x} = 0$ in equation (4-5):

$$X = -A^{-1}BU \tag{4-9}$$

From equation (4-2) ~ (4-9), the steady-state quiescent points can be obtained. Among them, the inductor and magnetizing average currents are:

$$I_{L1} = \frac{d_2 R_T + R_{L2}}{(d_1 + d_2)R_T + R_{L1} + R_{L2}} I_o \tag{4-10}$$

$$I_{L2} = \frac{d_1 R_T + R_{L1}}{(d_1 + d_2)R_T + R_{L1} + R_{L2}} I_o \tag{4-11}$$

$$I_M = \frac{d_2 R_{L1} - d_1 R_{L2}}{(d_1 + d_2)(R_{L1} + R_{L2}) + (d1 + d2)^2 R_T} I_o \tag{4-12}$$

The equations above are general solutions for both symmetric and asymmetric half-bridge DC-DC converters. From equations above, we can conclude:

(1) Only DC resistance values and duty cycles have an effect on the DC currents' distribution in half-bridge DC-DC converters.

(2) Capacitance and inductance of a converter have no impact on the DC steady-state solutions. Actually, capacitance and inductance values only affect voltage and current ripples.

(3) Unbalanced inductor DC currents and DC bias of magnetizing current exist due to asymmetry of inductor equivalent DC resistance (DCR) and duty cycles.

(4) On-resistance of synchronous rectifiers has no effect on the DC currents distribution and averaged magnetizing current.

For the symmetric HB CDR DC-DC converter, due to the fact that peak-current-mode control cannot be applied [D9], voltage-mode control is most likely utilized. In this case, if unbalanced DC resistive parameters exist, the DC current sharing between two

inductors and two SR channels of current-doubler rectifier (CDR) cannot be achieved by control. The following conclusions are drawn from Equation (4-10) ~ (4-12):

(1) Assuming $d_1 = d_2$ *and* $R_{L1} = R_{L2}$, we obtain $I_{L1} = I_{L2}$. That means two inductors can evenly share output current $I_o$ under both symmetric duty cycles and symmetric inductor DCRs. In other words, the symmetry of inductor DCR is highly required in order to achieve good inductor and SR current sharing. In addition, effective duty cycles $d_1$ and $d_2$ of two switches should be equal in order to achieve balanced inductor currents.

(2) If $R_{L1} \neq R_{L2}$, DC currents in the two inductors become unbalanced. By adjusting the duty cycles, two inductor currents can be equal if the following equation is satisfied:

$$d_2 - d_1 = \frac{R_{L1} - R_{L2}}{R_T} \tag{4-13}$$

However, if the asymmetry of inductor DCR goes beyond the range that duty cycles can compensate, the unbalanced currents are not avoidable.

(3) If $d_2 R_{L1} \neq d_1 R_{L2}$, there is a DC bias of magnetizing current in the transformer. It means that asymmetric duty cycles or asymmetric inductor DCRs result in the DC bias of the transformer magnetizing current, which should be estimated for when designing the transformer.

### 4.1.4 DC Analysis of Asymmetric Half-Bridge DC-DC Converter

In the asymmetric HB converter, driving signals of the two primary switches are complementary, thus zero-voltage-switching (ZVS) can be achieved for both primary switches.

A steady-state matrix and DC solutions can be obtained by substituting equation $d_2 = 1 - d_1$ into equations (4-10) ~ (4-12). Among the DC solutions, the inductor currents and transformer magnetizing current are:

$$I_{L1} = \frac{R_{L2} + (1-d_1)R_T}{R_T + R_{L1} + R_{L2}} I_o \tag{4-14}$$

$$I_{L2} = \frac{R_{L1} + d_1 R_T}{R_T + R_{L1} + R_{L2}} I_o \tag{4-15}$$

$$I_M = \frac{(1-d_1)R_{L1} - d_1 R_{L2}}{R_{L1} + R_{L2} + R_T} I_o \tag{4-16}$$

From equations (4-14) ~ (4-16), we can conclude:

(1) Even if a converter has symmetric inductor DCRs, the current distribution between two inductors is uneven because of the asymmetric duty cycle. The asymmetry of currents becomes worse if the $R_T$ value is comparable to or greater than the value of inductor DCR values.

(2) Under symmetric DCRs of inductors, the transformer has DC bias of magnetizing current, which can be estimated through equation (4-16) when designing the transformer. Note that the DC bias of the magnetizing current is positively proportional to the output current, and an air gap has to be added for the transformer to avoid saturation.

(3) If the converter is designed for wide input voltage ranges, at high input voltage, the asymmetric half-bridge converter operates at severe asymmetry of duty cycle, which leads to higher DC bias of the magnetizing current and unbalanced DC current distribution between two inductors. As shown in Fig. 4.5(a), where $R_{L1}=R_{L2}=1.5$m Ohm, $R_T=2.2$m Ohm, output current Io=40A, with the increased asymmetry of duty cycle, the DC bias of magnetizing current and asymmetry of the two inductor currents become worse even with equivalent DCR of the inductors. This is one of the reasons why an asymmetric half-bridge DC-DC converter is not suitable for the wide-input voltage range that requires wide-duty cycle variation.

(4) Under asymmetric duty cycles, if the inductor DCR values are asymmetric, the DC curves shift up or down vertically while keeping the slope constant. Fig. 4.5 (b) shows the curves at $R_{L1}=2$m, $R_{L2}=1.5$m Ohm, where the curve $I_{L1}$ shifts down and curve $I_{L2}$ and $I_M$ shift up. Assuming the converter operates at the duty cycle range $0<D<0.5$, the current sharing of the two inductors is improved while the DC bias of the magnetizing current increases. If $R_{L1} < R_{L2}$, the DC bias of magnetizing decreases while the inductors current sharing become worse.

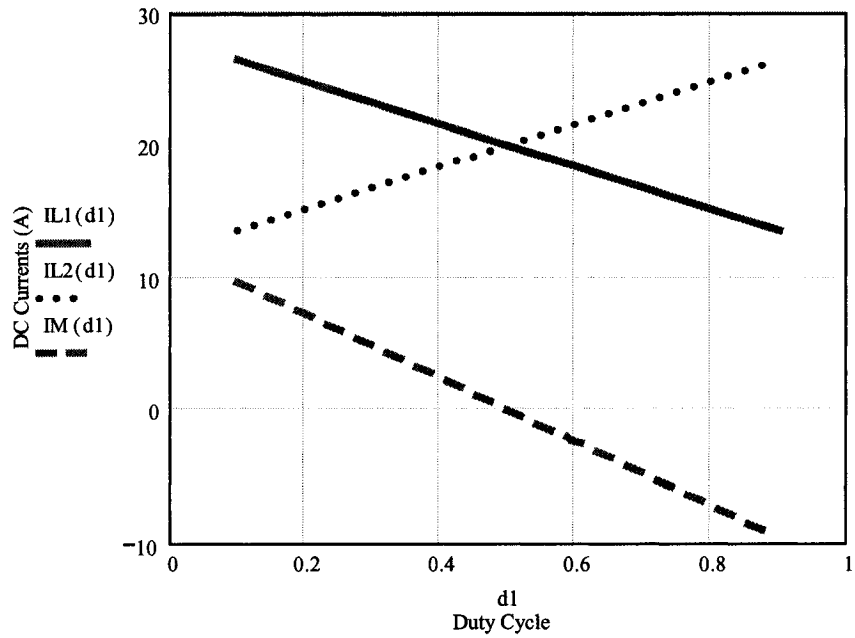



Fig. 4.5 (a) Asymmetric duty cycles and symmetric DCR values of the inductors

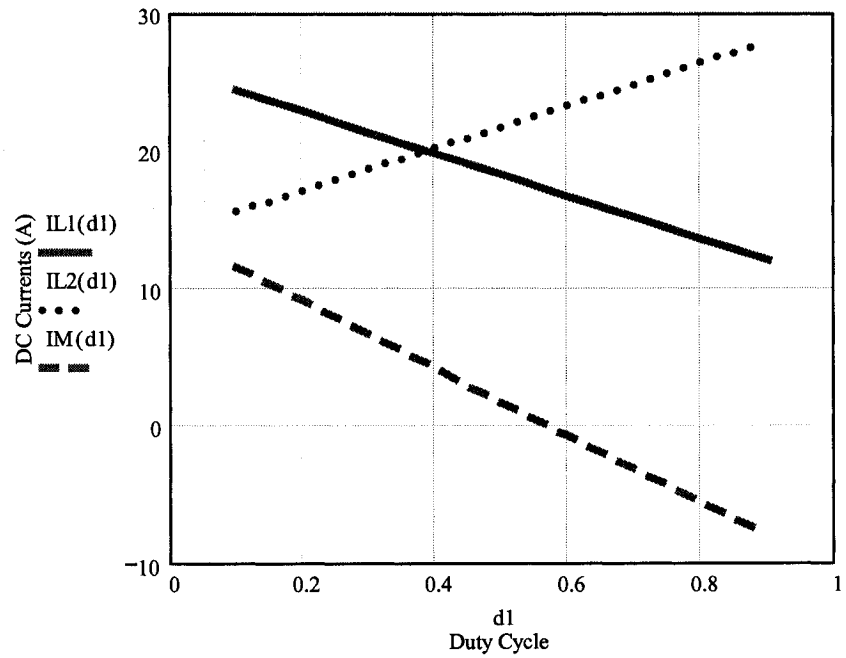



Fig. 4.5 (b) Asymmetric duty cycles and inductor DCR values

Fig. 4.5 Transformer and inductor DC currents vs. duty cycle

### 4.1.5 Experimental and Simulation Verification

The derived DC model is verified in the symmetric and asymmetric half-bridge DC-DC converters through Pspice simulation. The specifications for the symmetric HB are: Vin =36V~75V, transformer turns ratio: 4:1, output: 1.8V/40A, switching frequency: 250 kHz, Lm=$L_1$=$L_2$=2uH, primary switches: Si7856*2, synchronous rectifiers: Si7892*3*2. MOSFET Pspice models are downloaded from manufacturer's Web site.

Under symmetric duty cycles and DC parameters, duty cycle d1=d2=0.315(Vin=48V), $R_{L1}$=$R_{L2}$=1.5m Ohm, $R_T$=2.2 m Ohm, from equations (4-10) ~ (4-12), we can obtain the average magnetizing current $I_M$=0A, and the average inductor currents $I_{L1}$=$I_{L2}$=20A, which can be verified by the simulation waveforms shown in Fig. 4.6. Under asymmetric inductors DCR values: $R_{L1}$= 2m, $R_{L2}$=1.5m, and with the use of equations (4.10) ~ (4.12), we may obtain $I_M$=2.05A, $I_{L1}$=17.95A and $I_{L2}$=22.05A, which is close to the simulation results shown in Fig. 4.7 with $I_M$=1.90A, $I_{L1}$=18.45A, $I_{L2}$=21.55A. More comparisons between simulation results and theoretical computation results show that the DC model and corresponding solutions are very accurate.

Based on the same specification as the symmetric HB, the asymmetric control is applied to the converter. Under asymmetric duty cycles: d1=0.28, d2=0.70 (Vin=48V), and symmetric inductors' DCR: $R_{L1}$= $R_{L2}$=1.5m Ohm, calculated by using Equations (4-10) ~ (4-12), the following theoretical DC values are obtained: $I_M$=4.98A, $I_{L1}$=23.58A, $I_{L2}$=16.42A. Applying the same parameters to the simulation, the simulation waveforms are shown in Fig. 4.8, wherein the average values agree with the theoretical DC values. More simulation results under both asymmetric duty cycle and asymmetric inductors

DCR values are compared with the computed values, and they agree with each other very well.

A prototype of HB DC-DC converter is built with the same specification as the simulation. With symmetric duty cycles, inductor DCR values and SR channel resistance, the experimental waveforms are shown in Fig. 4.9. It can be observed that two inductors have close average currents, and thus current sharing between the two inductors is achieved under an ideally symmetric condition.

Intentionally, an external resistor of 2m Ohm is added in series with one of the SR channels to make the SR channels unbalanced. The corresponding experimental waveforms are shown in Fig. 4.10. It is noted that current sharing can still be achieved between two inductors under unbalanced SR channel resistance, which agrees with the derived equations from the steady-state model.

In the same manner, an external resistor of 1m Ohm is intentionally added in series with one of the inductors to make the inductor DCR values unbalanced. Under symmetric duty cycle and SR channel resistance, the resultant experimental waveforms are shown in Fig. 4.11. From the figure, it can be seen that two inductor average currents are unbalanced due to asymmetric inductor DCR values.

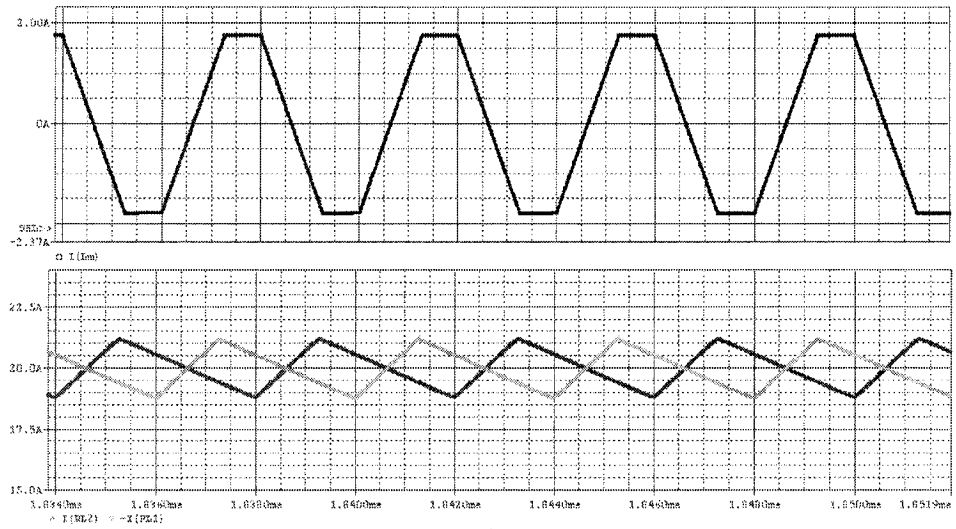


Fig. 4.6 Waveforms of the symmetric HB converter under symmetric duty cycles and inductor DCR values ($R_{L1}$=1.5m Ohm, $R_{L2}$=1.5m Ohm, $R_T$=2.2m Ohm)

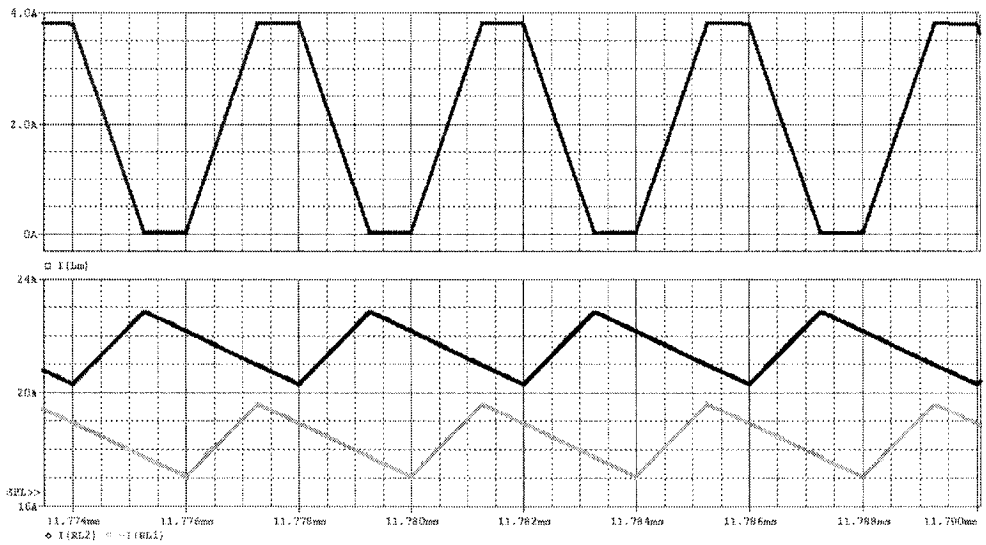


Fig. 4.7 Waveforms of a symmetric HB converter under asymmetric inductor DCR values ($R_{L1}$=2m, $R_{L2}$=1.5m, $R_T$=2.2m)

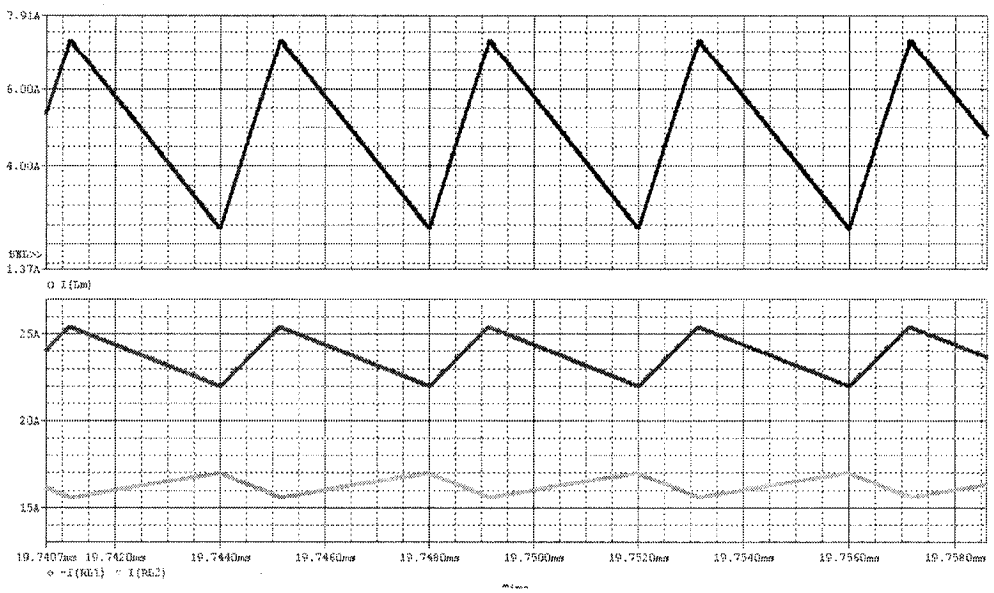


Fig. 4.8 Waveforms of an asymmetric HB converter with asymmetric duty cycles and symmetric inductors DCR (d1=0.28, d2=0.70, $R_{L1}$=$R_{L2}$=1.5m, $R_T$=2.2m)

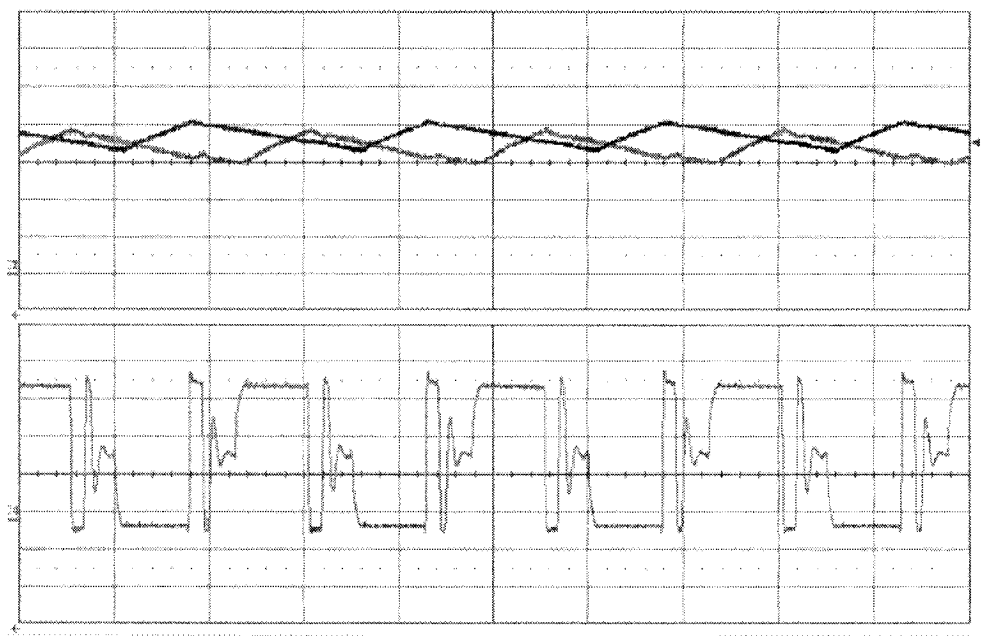


Fig. 4.9 HB DC-DC converter under symmetric conditions

(Top traces: two inductor currents (5A/div); Bottom trace: switch Vds1 (10V/div))

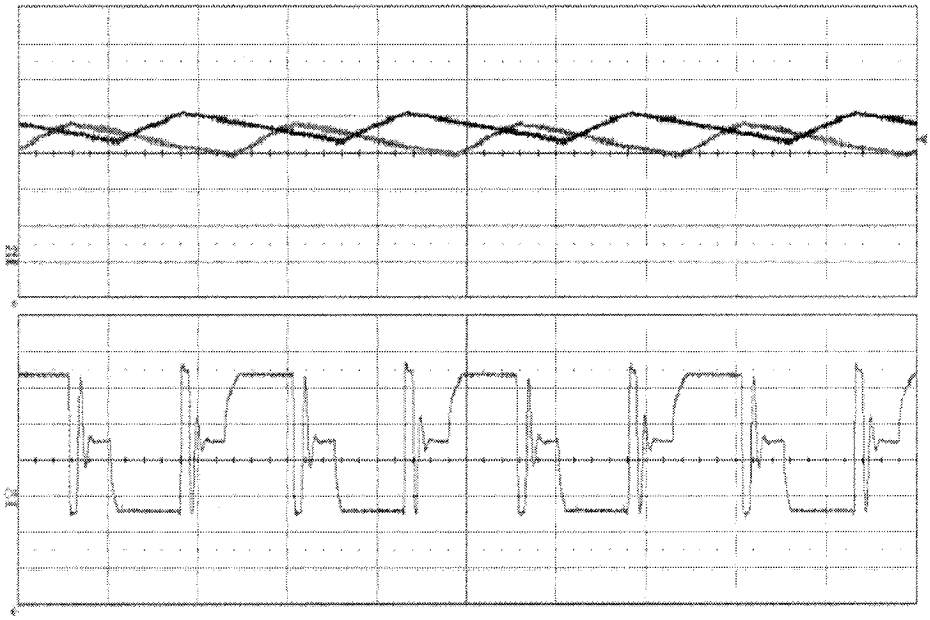


Fig. 4.10 Symmetric HB DC-DC converter under asymmetric SR channel resistance and symmetric inductor DCR values

(Top traces: two inductor currents (5A/div); Bottom trace: Switch Vds1 (10V/div))

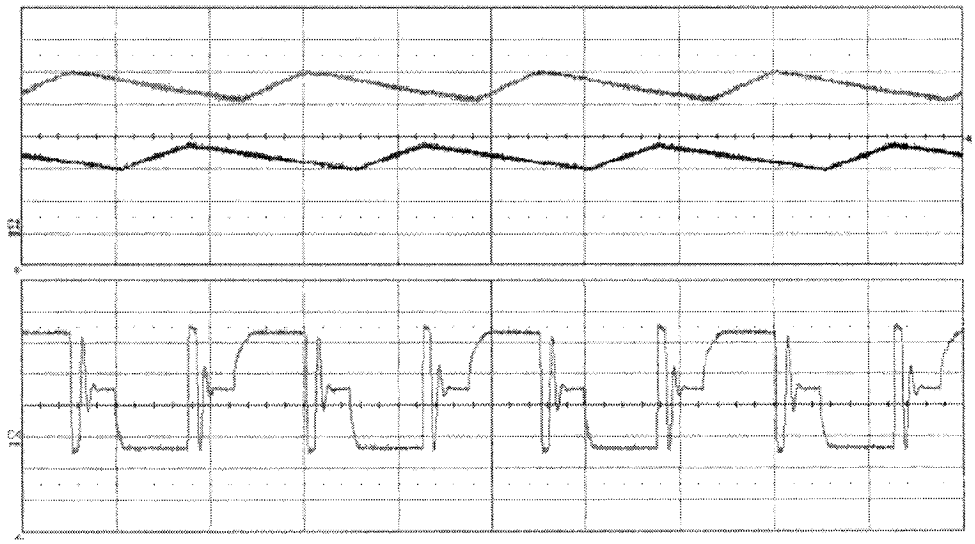


Fig. 4.11 Symmetric HB converter under asymmetric inductor DCR values and symmetric SR channel resistance

(Top traces: two inductor currents (5A/div); Bottom trace: switch Vds1 (10V/div))

### 4.1.6 Summary

A unified steady-state model was derived for both symmetric and asymmetric half-bridge current-doubler-rectifier DC-DC converters. Several conclusions and design guidelines were presented and verified by experimental and simulation results. The resistance of SR channel has no impact on the DC current distribution of a HB converter. Under symmetric duty cycles, asymmetric inductors DCR values result in imbalance inductor DC currents and DC bias in the transformer, and thus, the two inductor channels should have a well-matched layout. For the asymmetric HB DC-DC converter, the DC bias of magnetizing currents and unbalanced inductor currents exist due to the asymmetric duty cycles or unbalanced inductors DCR.

## 4.2 An Improved Half-Bridge DC-DC Converter to Achieve Current Sharing

As mentioned above, due to asymmetric DC parameters between two channels, unbalanced DC inductor currents degrade converter efficiency and thermal management. To achieve a balanced current sharing, balanced layout must be taken care of. In practice, it is hard to make equal the inductor DC resistance in the two channels.

In this subchapter, a modified HB DC-DC converter is proposed to avoid the unbalanced current sharing resulting from the unmatched layout. The topology is presented, and the DC analysis shows that the current sharing is achieved even with asymmetric inductor DC resistance.

### 4.2.1 Modified Half-Bridge DC-DC Converter

Fig. 4.12 shows the modified HB DC-DC converter, wherein an additional capacitor $C_s$ is simply added in series with the transformer secondary winding. For the half-bridge DC-DC converter, peak current control cannot be applied, because when the primary capacitor voltage goes asymmetric, a positive feedback leads to the capacitor's voltage collapsing to zero. Since the peak current control can't be used, and generally voltage mode control is used for closed-loop control, an external capacitor on the secondary side can be added without losing the control benefit in the half-bridge DC-DC converter. However, it must be noted that in a full-bridge DC-DC converter, the added capacitor will result in the peak current mode control being unusable.

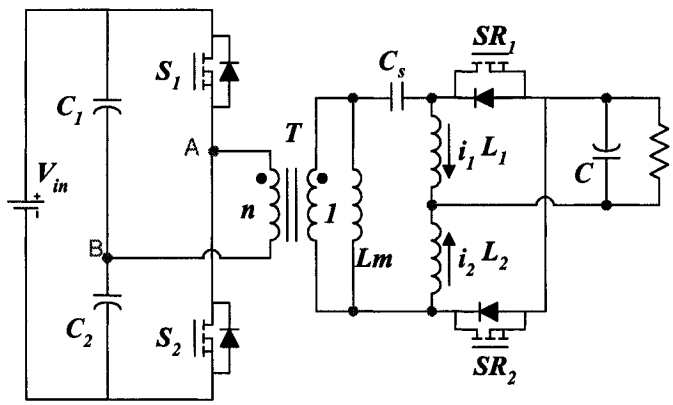



Fig. 4.12 Modified half-bridge DC-DC converter

### 4.2.2 DC Modeling of the Proposed Half-Bridge DC-DC Converter

By employing the same method as described in section 4.1, DC solution can be derived and yield the average voltages and currents in the converter.

Considering that the converter is always operating at CCM mode with the synchronous rectifiers, the topology has three typical modes as shown in Fig. 4.13 through Fig. 4.15. In a switching period, corresponding operating modes can be denoted using three linear state-space equations, respectively. State-space equations can be expressed as equation (4-17), where, $x$ is the vector of state variables and $u$ is the vector of independent sources.

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \tag{4-17}$$

For convenience, $\dot{x} \neq dx/dt$, and the definitions are as follows:

$$\dot{x} = \left[ (C1+C2)\frac{dv_{C1}}{dt} \quad L1\frac{di_{L1}}{dt} \quad L2\frac{di_{L2}}{dt} \quad C\frac{dv_C}{dt} \quad L_m\frac{di_m}{dt} \right]^T ; \; x = [v_{C1} \quad i_{L1} \quad i_{L2} \quad v_C \quad i_m]^T ; \quad u = [V_{in} \quad I_o]^T \tag{4-18}$$

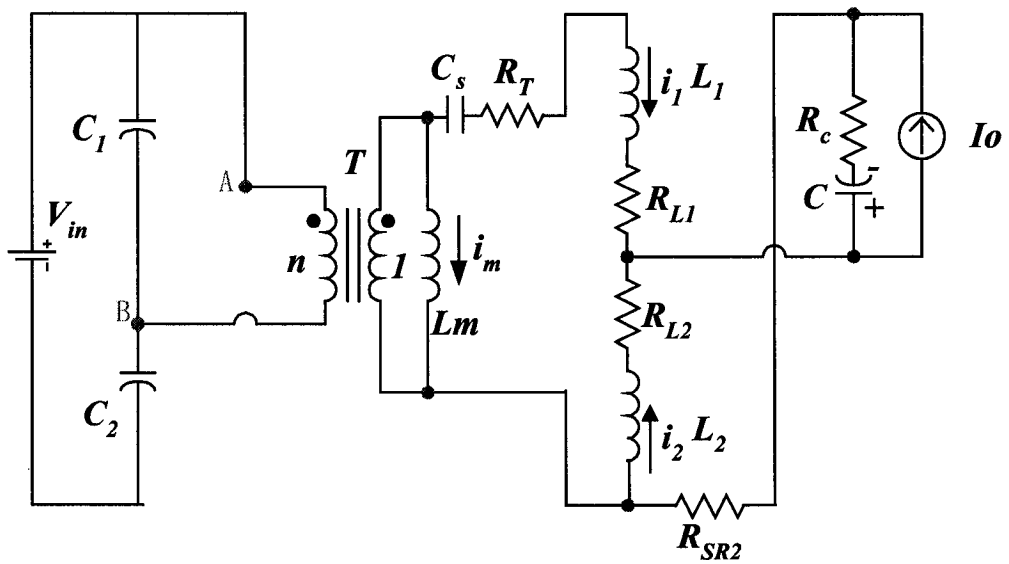



Fig. 4.13 Mode 1: $S_1$ is on

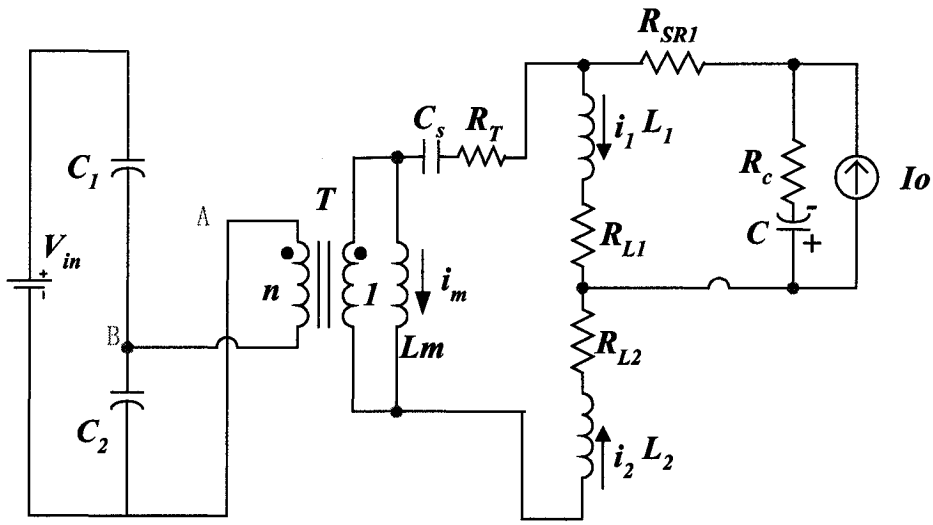



Fig. 4.14 Mode 2: $S_2$ is on

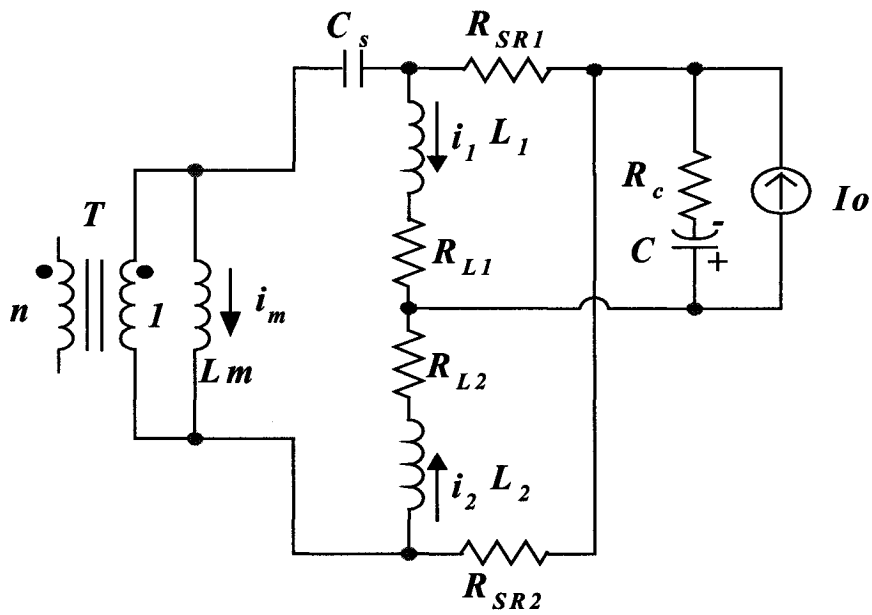



Fig. 4.15 Mode 3: Both $S_1$ and $S_2$ are off

Where, $A_1$ and $B_1$ are state-space matrices of Mode 1; $A_2$ and $B_2$ are state-space matrices of Mode 2; $A_3$ and $B_3$ are state-space matrices of Mode 3. All of these matrixes are shown as the following equations:

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{n} & 0 & 0 & -\frac{1}{n} & 0 \\ \frac{1}{n} & -(R_{L1}+R_C+R_{SR2}+R_T) & -(R_C+R_{SR2}) & -1 & 0 & -1 \\ 0 & -(R_C+R_{SR2}) & -(R_{L2}+R_C+R_{SR2}) & -1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (4\text{-}19)$$

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{1}{n} & 0 & -\frac{1}{n} & 0 \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -(R_C+R_{SR1}) & -1 & 0 & 0 \\ -\frac{1}{n} & -(R_C+R_{SR1}) & -(R_{L2}+R_C+R_{SR1}+R_T) & -1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix} \quad (4\text{-}20)$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -R_C & -1 & -R_{SR1} & 0 \\ 0 & -R_C & -(R_{L2}+R_C+R_{SR2}) & -1 & R_{SR2} & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & -R_{SR1} & R_{SR2} & 0 & -(R_{SR1}+R_{SR2}) & 1 \\ 0 & 0 & 0 & 0 & -1 & 0 \end{bmatrix} \quad (4\text{-}21)$$

$$B_1 = \begin{bmatrix} 0 & 0 \\ 0 & R_C \\ 0 & R_C \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad ; \quad B_2 = \begin{bmatrix} 0 & 0 \\ 0 & R_C \\ \frac{1}{n} & R_C \\ 0 & -1 \\ -\frac{1}{n} & 0 \\ 0 & 0 \end{bmatrix} \quad ; \quad B_3 = \begin{bmatrix} 0 & 0 \\ 0 & R_C \\ 0 & R_C \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{4-22}$$

Substitute Equations (4-19) through (4-22) into the following equations:

$$A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3 \tag{4-23}$$

$$B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3 \tag{4-24}$$

The unified averaged state-space matrix A and matrix B can be derived and denoted as follows:

$$\dot{x} = Ax + Bu \tag{4-25}$$

### 4.2.3 DC Analysis of the Proposed Half-Bridge DC-DC Converter

Setting $\dot{x} = 0$ in equation (4-25), the DC solution is obtained:

$$X = -A^{-1} B U \tag{4-26}$$

Where, $U = [V_{in} \quad I_o]^T$ (4-27)

Thus, all the DC values of state-space variables can be derived through Equation (4-26). Among those DC values, the inductor and magnetizing DC currents are:

$$I_{L1} = \frac{D_2}{D_1 + D_2} I_o \tag{4-28}$$

$$I_{L2} = \frac{D_1}{D_1 + D_2} I_o \tag{4-29}$$

$$I_M = 0 \tag{4-30}$$

From the equations above, it is clearly shown that:

(1) Inductor currents are determined only by the steady-state duty cycle and the output current Io.

(2) Averaged magnetizing current is unconditionally equal to zero, which means no air gap is needed in the transformer.

(3) Under symmetric control condition ($D_1$=$D_2$), inductor currents keep balance and there is no DC bias of the magnetizing current even under asymmetric DC resistance parameters.

(4) The modified HB DC-DC converter can achieve inductor current sharing and zero DC bias of the magnetizing current under symmetric control even if the converter has asymmetric DC resistance between channels.

(5) The added capacitor will not affect the current ripple in the transformer.

### 4.2.4 Simulation Verification

Both conventional and modified half-bridge DC-DC converters are simulated to verify the previous conclusions. Assuming duty cycle is symmetric with D1=D2=0.315 (Vin=48V), and inductor DCR values are unbalanced: $R_{L1}$= 2m, $R_{L2}$=1.5m and $R_T$=2.2m, which are the two inductor current waveforms shown in Fig.4.16 (a). It is clear that two inductors have different average currents. For the modified half-bridge DC-DC topology, current sharing is achieved between two inductors as shown in Fig. 4.16(b).

It must be noted that ceramic capacitors feature lower ESR and ESL, and therefore the added capacitor $C_s$ doesn't degrade converter performance and efficiency.

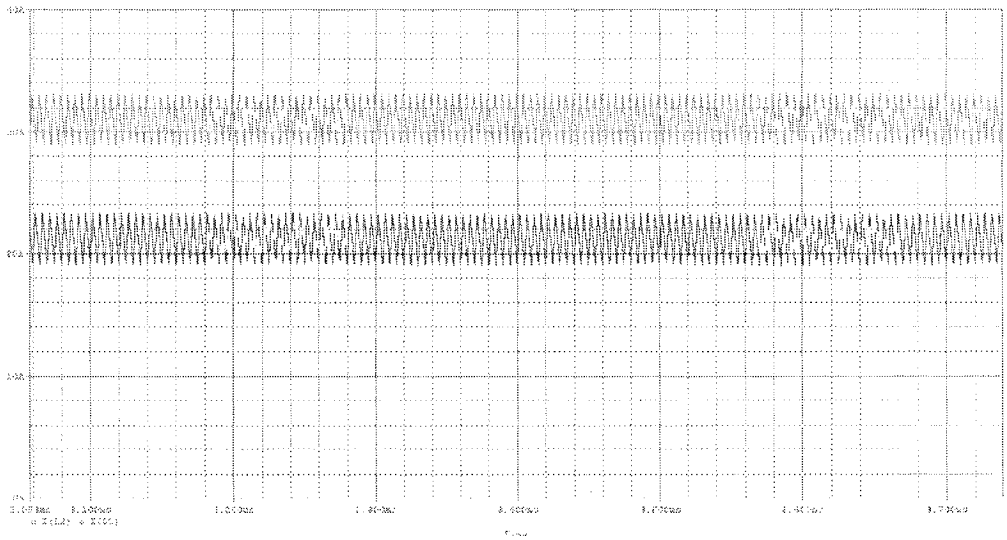


Fig. 4.16 (a) Conventional HB converter under asymmetric inductor DCR

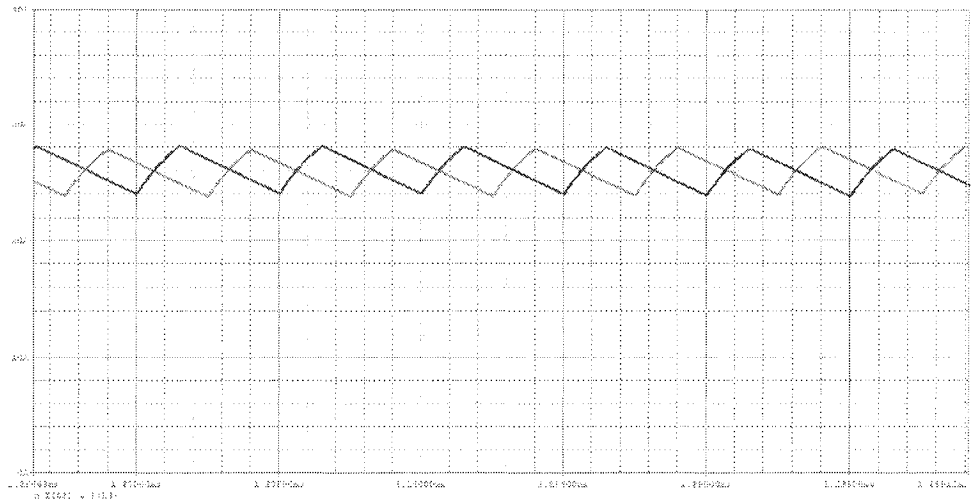


Fig. 4.16 (b) Modified half-bridge converter under asymmetric inductor DCR

Fig.4.16. Current sharing comparison between conventional and modified HB DC-DC converter ($R_{L1}$=2m, $R_{L2}$=1.5m, $R_T$=2.2m)

### 4.2.5 Summary

A modified HB DC-DC converter is proposed to solve these problems, and the converter proposed is verified via the steady-state mathematical model, simulation and experimental results. The unified steady-state mathematical model is derived for a conventional symmetric HB current-doubler-rectifier DC-DC converter. Based on the model, it is discovered that unbalanced currents through two inductors and transformer DC magnetizing current bias exist in the conventional HB DC-DC converter.

## 4.3 AC Modeling and Analysis of Isolated DC-DC Converters

### 4.3.1 Closed-Loop System Modeling

Isolated bridge converters with current doubler rectifier, can be regarded as a two-phase interleaved buck converter with transformer voltage step down. As an example of bridge converters, the small-signal model of the half-bridge DC-DC converter is studied in this section of the dissertation. As shown in Fig. 4.17, a converter has input voltage disturbance $\hat{v}_s$ and output current disturbance $\hat{i}_o$ and the disturbances are attenuated by control signal $\hat{d}$.

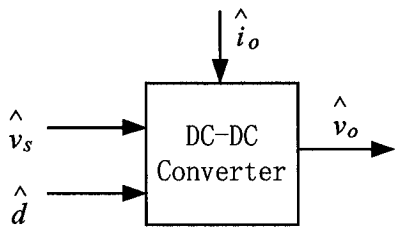



Fig. 4.17 (a)

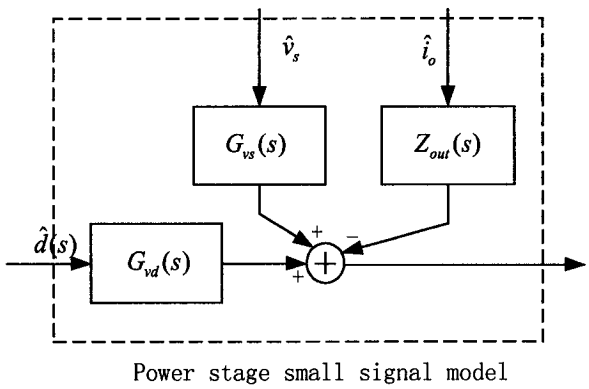



Fig. 4.17 (b)

Fig.4.17 Power stage block of DC-DC converters

A small signal model of the half-bridge DC-DC converter is shown in Fig. 4.17 (b), wherein the transfer function from input voltage to output voltage is:

$$G_{vs}(s) = \frac{D}{2n} H_e(s) \tag{4-31}$$

The transfer function from duty cycle to output voltage is:

$$G_{vd}(s)=\frac{V_s}{2n}H_e(s) \tag{4-32}$$

In Equation (4-31) and Equation (4-32),

$$H_e(s)=\frac{sC(R_c+R_L)+R_L}{s^2L_eC(R_c+R_L)+s(L_e+\mathrm{R_e}\,C(R_c+R_L)+2CR_LR_c)+R_L+\mathrm{R_e}} \tag{4-33}$$

The open-loop output impedance is:

$$Z_{out}(s)=\frac{R_LR_cCL_es^2+(R_LR_cR_eC+R_LL)s+R_LR_e}{(R_cCL_e+R_LCL_e)s^2+(R_LR_cC+R_cR_eC+R_eR_cC)s+R_LR_e} \tag{4-34}$$

The closed-loop controlled system is shown in Fig. 4.18, where the PWM modulation block is approximately expressed as:

$$G_{PWM}(s)=\frac{1}{V_m(1+\tau_m s)} \tag{4-35}$$

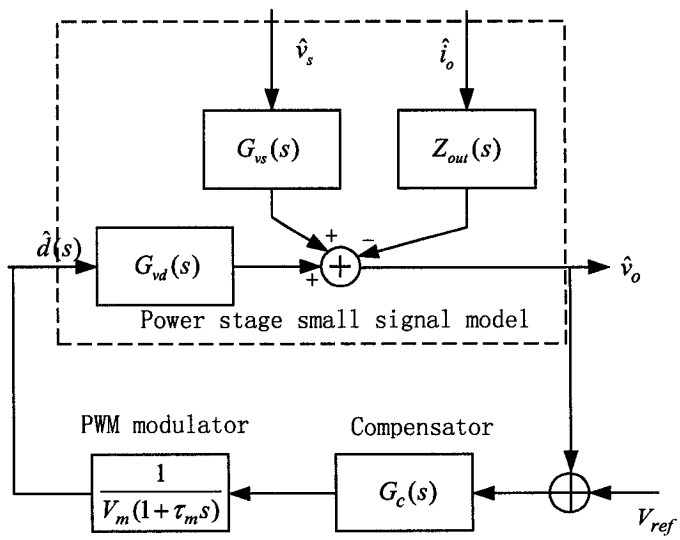



Fig. 4.18 Closed-loop controlled DC-DC converter

The loop gain is an important parameter for a closed-loop system, which is:

$$T(s) = \frac{1}{V_m(1+\tau_m s)} G_{vd}(s) G_c(s) \tag{4-36}$$

Where, $G_c(s)$ is the transfer function of the compensator.

### 4.3.2 Output Impedance Analysis

For a low-voltage, high-current DC-DC converter, the requirements of a transient response-to-load current change are becoming more and more stringent. Load current change slew rate di/dt, moving it higher and higher, which means the high-frequency components corresponding to load current slew rate increases. In frequency domain, the load current disturbance is attenuated through the closed-loop system. For a high slew rate current change to reduce the output voltage overshoot and undershoot, a small, closed-loop output impedance should be achieved within the high-frequency band.

The open loop and closed-loop output impedance are analyzed in the following. For the open-loop output impedance, the equivalent circuit is shown in Fig. 4.19. It is clear that at low-frequency band, the inductance Le is regarded as short circuit, and capacitor C is regarded as open circuit, so the resistance Re dominates the output impedance. At intermediate-frequency band, Le and C dominate. At high-frequency band, inductor Le branch is open circuit and capacitor ESR dominates.

For different filter capacitance values, the open-loop output impedance and corresponding phase angle curves are shown in Fig. 4.20, where it can be observed that:

(1) At low-frequency band, the output impedance is resistive and the phase angle is near zero. The reason is because the filter inductor has very low impedance and Re dominates the output impedance.

(2) In the front-middle-frequency band, the inductor takes effect and the impedance increases. The phase angle increase towards $90^{\circ}$.

(3) At the resonant point, the capacitor starts taking effect. The output impedance decreases, and the phase angle decreases towards $-90^{\circ}$.

(4) At high-frequency band, the output impedance decreases to the filter capacitor ESR value, and the phase angle becomes zero.

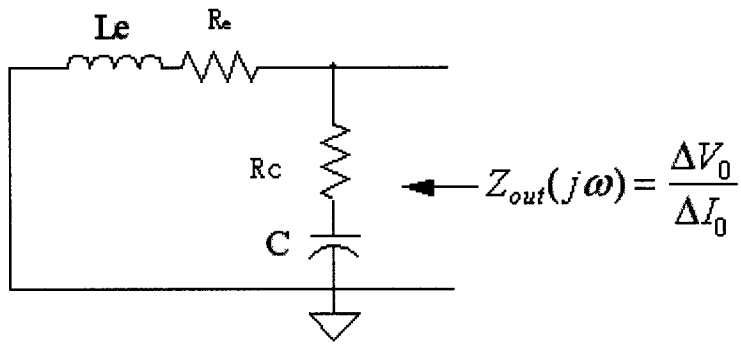



Fig. 4.19. Open-loop output impedance equivalent circuit

(5) With larger filter capacitance, the cut-off frequency decreases. It can be observed that increased capacitance decreases the output impedance values. In other words, output voltage overshoot and undershoot can be reduced by increasing output capacitance.

(6) At high-frequency band, the output impedance is dominated by capacitor ESR, because the lower ESR is preferred for a good transient response.

Fig. 4.21 shows a set of output impedance and phase angle curves with varied inductance. It is clear that lower filter inductance corresponds to higher cut-off frequency and lower output impedance. It means that faster transient response can be achieved by reducing the filter inductance. Physically, the inductor can be regarded as a roadblock on the energy transfer path from input to output. Inductance slows down the energy transfer during a transient response.

Closed-loop control can improve system transient response. The output impedance can be reduced by closed-loop control as:

$$Z_{oc}(s) = \frac{Z_{out}}{1+T(s)} \tag{4-37}$$

Where, T(s) is the system loop gain as illustrated in Equation (4-36). It must be noted that the loop gain is the function of frequency. In the frequency domain, within the bandwidth, we have T (s)>1 so that the output impedance can be reduced. However, beyond the bandwidth, closed-loop control has no impact on the output impedance. In this case, the converter performance is dominated only by the power stage. In other words, for extremely high-current load current change, the power stage works like an open-loop control until the control system kicks in.

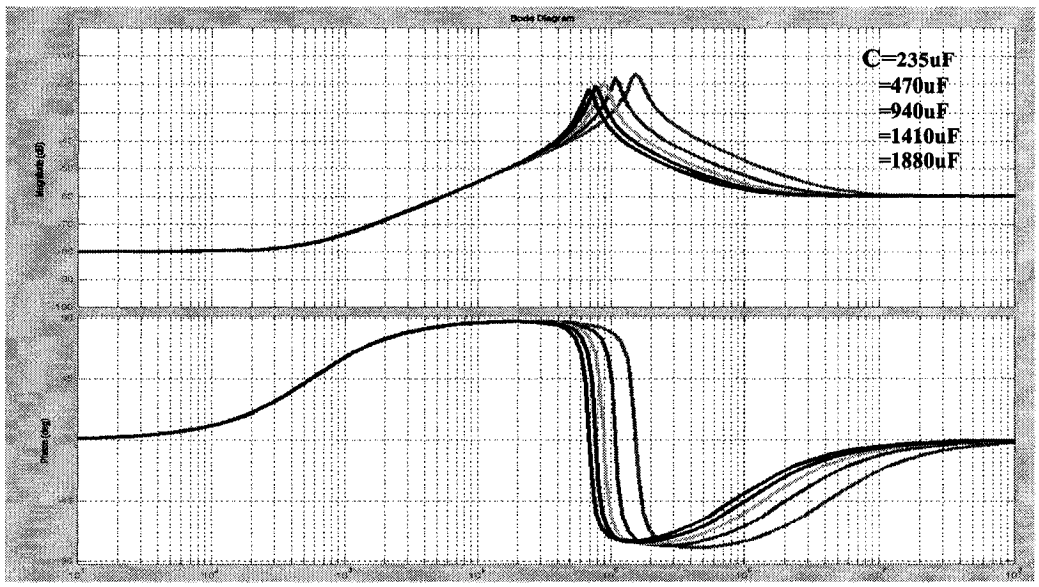



Fig. 4.20 Open-loop output impedance (dB) and phase curve

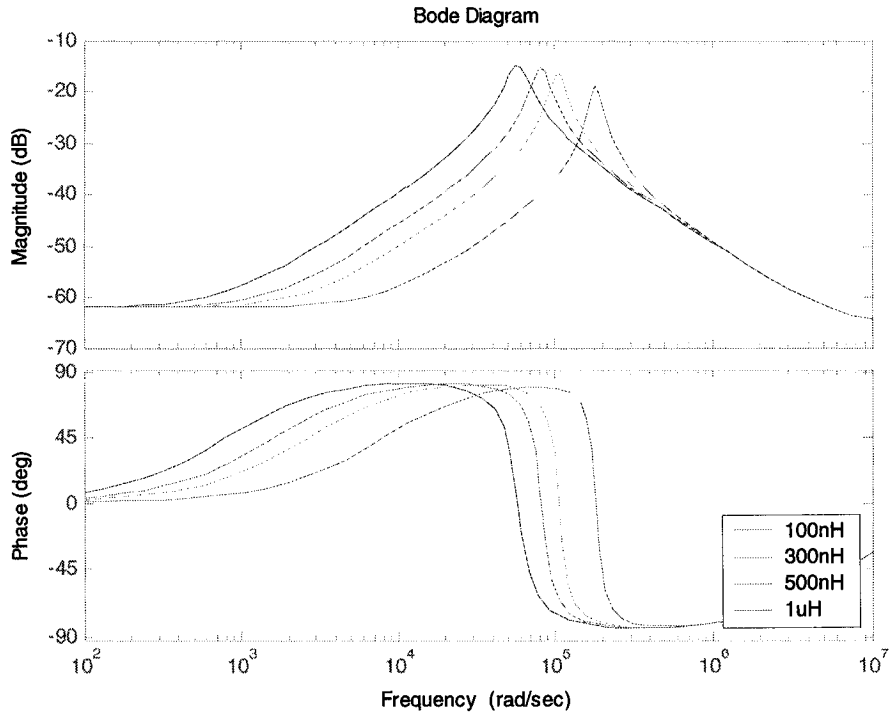



Fig. 4.21 Open-loop output impedance with a variety of filter inductance

A typical design is shown in Fig. 4.22. It is clear that the output impedance is reduced by the closed-loop control within the bandwidth. Beyond the bandwidth, the closed-loop output impedance overlaps with open-loop bandwidth.

With stringent transient response requirements, low output impedance is required with a broad frequency band. Therefore, transient response can be improved by the following means:

(1) Reducing filter parameters. To have reasonable output current and voltage ripples, the active way is to increase switching frequency.

(2) Fast control schemes to increase the system bandwidth.

(3) Soft-switching techniques, which help to push the switching frequency.

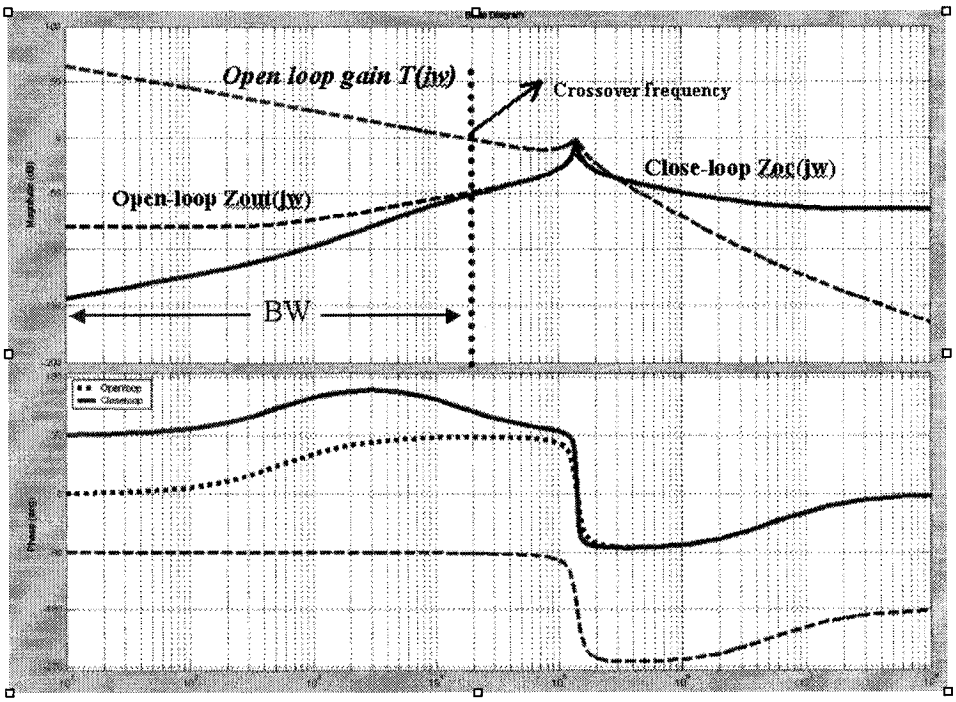



Fig. 4.22 A closed-loop design and output impedances

# 5. TWO-STAGE APPROACHES FOR DC-DC CONVERSION

With the increased power level of Point-of-Load (POL) converters, the 12V voltage bus may not be a desirable bus voltage due to the increase distribution loss and small duty cycle-related issues. 48V is a desirable voltage bus for on-board POL applications. There are two types of approaches for 48V input. One is single stage approach and the other is two-stage approach. Single stage is simple and cost effective. However, the single stage approach includes all converter functions such as safety isolation, voltage step-down, regulation to input line variation and response to load change. With the stringent transient requirement of next-generation microprocessors and DSPs, it is hard to make a trade-off within one stage, therefore, two-stage approach is a promising solution to the transient requirement. In a two-stage approach, the functions of voltage step-down and response to load change are implemented separately in different stages. For example, second stage can operate at higher switching frequencies to meet the transient response and reduce the cost of output capacitance.

## 5.1 Review of Two-Stage Architectures of Voltage Regulator

Microprocessors are becoming more and more powerful today. Meanwhile, their power consumption increases dramatically. In the past, the CPU power supply, Voltage Regulator Module (VRM), basically drew power from a 5V output of the silver box. For desktop and workstation applications today, VRM input voltage has moved to the 12V

input of the silver box to reduce the loss on the input bus. Furthermore, in the server application, a 64-bit microprocessor consumes much higher power than 32-bit microprocessors in the desktops and notebooks, therefore, 48V input voltage is used instead of 12V input.

VRM design has become a serious challenge as today's microprocessors quickly develop. In the near future, the output voltage will be less than 1V while the output current will increase up to 150A. And, the dynamic requirement is also very stringent. The current slew rate will reach 400A/us in the near future, compared with the 150A/us of today. As the output current increases, the interconnection has become a block of fast-transient response. To eliminate the interconnection effect, most of today's CPU power supplies are placed directly on the motherboard (MB). This kind power supply is called VR or VR-Down instead of VRM. However, the real estate on the MB for the VR is almost always fixed. This means the future VR should have much higher current density compared with today's VR. The only solution is high frequency to shrink the passive components and leave more room for the active components. Most of today's VRM topologies are based on the multiphase buck converter [E1~E5]. Due to the very low output voltage, the buck converter has extremely small duty cycle, which will be less than 0.1 in the near future. The small-duty cycle dramatically impacts the performance of the multiphase buck converter and the transient response and efficiency are suffer. As a result, today's solution is not suitable for the high frequency application. To deal with the problems caused by the small-duty cycle, a lot of autotransformer version buck converters are proposed [E6 ~ E9]. They improve efficiency significantly and could be

more cost-effective than the conventional multiphase buck converter. However, the leakage inductor of the transformer fundamentally limits its switching frequency because of the duty cycle loss. Usually, they cannot reach the switching frequency beyond 1.5MHz.

Conventional power management systems for desktop computers are shown in Fig. 5.1, where VR draws current from a 12V voltage bus provided by silver box. The main drawback of the architecture is that the 12V bus voltage is too high for the VR converter because the converter operates at a duty cycle of less than 0.1, which significantly degrades converter efficiency and transient response. A two-stage concept was proposed in Fig. 5.2 to breakthrough the technical bottleneck [E15]. A simple and highly efficient step-down converter is used for the first stage, which can be accomplished by the simple buck converter. An ultra-high frequency, multiphase buck is used for the second stage. The low bus voltage significantly improves the performance of the second stage. Even based on the state-of-the-art devices, 82 percent efficiency can be achieved at 2MHz switching frequency.

However, we may wonder why we don't directly use the +5V voltage bus provided by the silver box to avoid the 12V-to-5V stage. Using the silver box, the overall system should be more efficient at the expense of higher distribution loss and larger input capacitor filter across the voltage bus. In fact, the power is processed three times before arriving at the microprocessor. Therefore, it is not a good solution for a next-generation microprocessor.

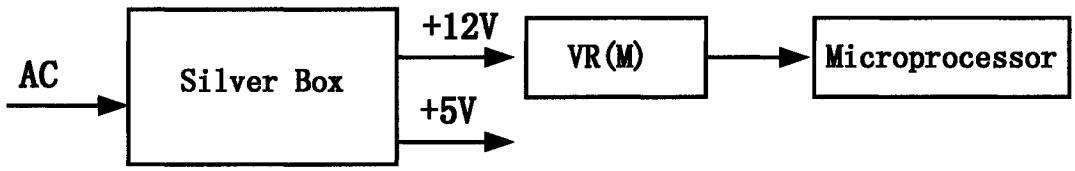



Fig. 5.1 Conventional desktop power architecture

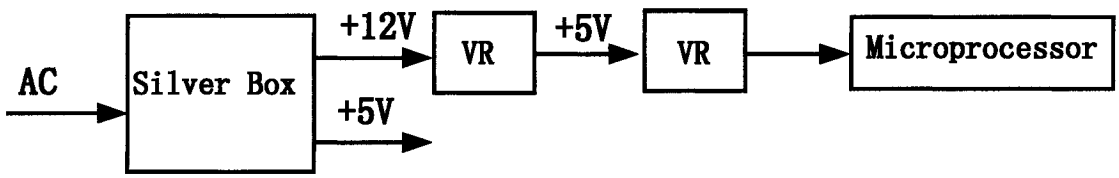



Fig. 5.2 A desktop power management architecture

In Fig. 5.3, the voltage bus is raised to 48V, which reduces the VR input filter capacitor size and distribution power loss. Two-stage concept is still used for the POL VRs. The first stage provides electrical isolation and voltage step-down just like a DC transformer. The secondary stage operates at the high switching frequency and meets the stringent transient response.

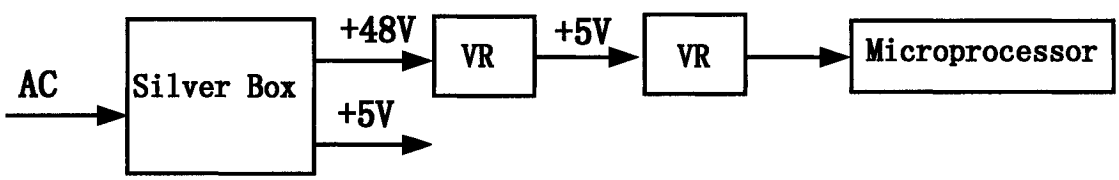



Fig. 5.3 An alternative power management architecture

A two-stage approach is more promising in the high frequency application. Because of the high frequency capability of the two-stage approach, the passive components and the cost of the VR can be significantly reduced. New power delivery architecture is also proposed associated with the high power density second stage. We can see that a two-stage approach is a very promising solution for the future VR/VRM.

## 5.2 Review of Architectures of Point-of-Load Converters

For telecom applications, isolated power modules have been standardized as shown in Fig. 5.4, with standard brick converters are used as point-of-load isolated converters. Now, let us briefly review the history of standardization of brick converters.

Early generation modular DC-DC power supplies were developed initially for the telecommunications industry. AT&T was the exclusive developer and supplier of power supplies for switching equipment used by the RBOCs (Regional Bell Operating Companies) up until the mid to late 1980s. Second-source power supplies were not available for this captive market. In 1984, AT&T signed a consent decree and was forced to divest its 22 Bell telephone companies. They were split into seven RBOCs that are more commonly known as the "Baby Bells." As part of the divestiture, Western Electric's charter was assumed by a new unit, AT&T Technologies. AT&T Technologies continued to design and use its isolated DC-DC power modules in the switching equipment it supplied the RBOCs.

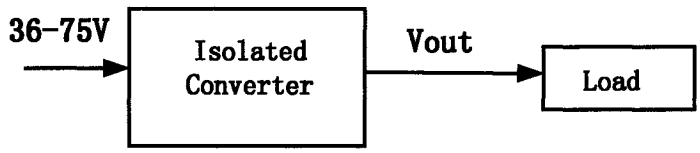



Fig. 5.4 Telecom isolated DC-DC conversion architecture

Following the breakup of AT&T, competition was established in the switching equipment marketplace. RBOCs now had the opportunity to purchase equipment from other manufacturers. These manufacturers used power modules from different suppliers in their system designs.

In 1985, Vicor Corporation was the first company to introduce a unique high-frequency zero current switching technology along with a modular form factor now commonly referred to as a "brick" (4.6" x 2.4" x 0.5"). The Vicor power module could have become the industry standard. However, the company defended its design patent to eliminate competition in the marketplace. In the course of its ongoing development program, AT&T continued to develop its own brick power modules.

The size of the merchant (non-AT&T) DC-DC power module market grew significantly during the late 1980s. Fierce competition within the telecommunications industry increased the rate of telecom technology development and powered a significant expansion of network capacity. In addition, there was growth in data communications applications, in conjunction with expanding use of distributed power.

As a result of the market's rapid growth, by the early 1990s, multiple power module manufacturers had entered the market. The power module market grew sufficiently larger

and customers started seeking second sources for isolated modules. However, the industry still had no footprint standardization. If a designer was looking for a power module for one of the emerging markets, the chance of finding functionally-equivalent modules that were also pin-for-pin compatible was extremely remote. Designers would use a discrete power supply design as a second source, or they would seek an alternative module.

Because emerging telecommunications markets held so much economic promise, many power module manufacturers sought differentiated products to gain market share. Each manufacturer strove to provide the differentiated device that it believed offered more advantages than other devices available at the time.

In February 1996, the systems and technology unit of AT&T renamed itself Lucent Technologies. The company brought the half-brick power module to market. Lucent then became a major player in the modular power market by serving the company's internal needs along with a substantial merchant presence. The success and popularity of Lucent's brick module made it the standard. Today, most power supply manufactures offer the brick form factor to insure footprint compatibility with power supplies from other manufacturers.

There are now a number of informally adopted, industry accepted "standard" sizes for brick power modules as shown in the following:

| Size | Dimensions (Inch) |
|---|---|
| • Full-brick | 4.6 x 2.4 |
| • Half-brick | 2.4 x 2.28 |
| • Quarter-brick | 2.3 x 1.45 |
| • Eighth-brick | 2.3 x 0.8 |

The outer dimension and size tolerance of the brick modules tend to vary between manufactures, but the pin position and functions are fixed. The half-brick and quarter-brick are the most common sizes. The eighth brick emerged in 2002 and is pin-compatible with the quarter-brick.

Industry standards for isolated converters have been formed as brick converters. Standardization could be the next evolutionary step in the non-isolated DC-DC power module industry [E16].

Recently, the Intermediate Bus Architecture (IBA) drew a lot of attentions [E16-E17]. IBAs that employ non-isolated modules are becoming a popular power solution for datacom and computer applications. IBA architecture is shown in Fig. 5.5, where the bus converter provides an isolated bus voltage (12V, 7.5V, 5V, 3.3V) and the POL converter steps-down the voltage to feed different loads. It is a very flexible architecture compared to the brick converter solution, because the bus converter can supply multiple loads with different voltage requirements.

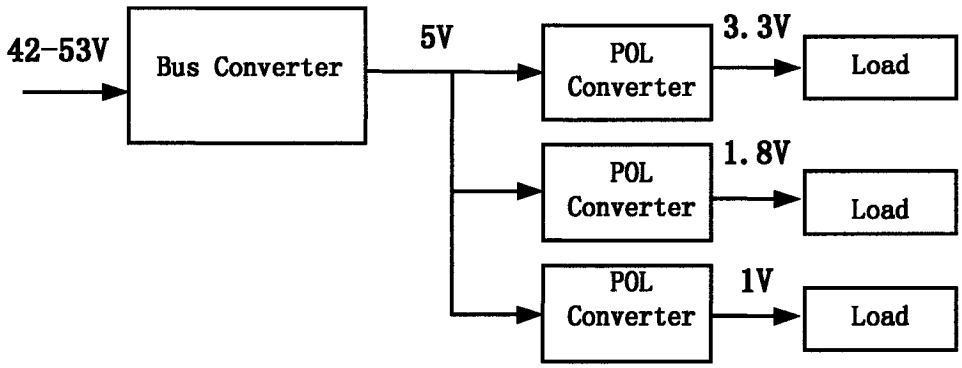



Fig. 5.5. IBA architecture

As device voltages decrease and currents rise, the need to generate voltages near the Point-of-Load (POL) becomes more pressing. This is driving the adoption of IBAs that use standard building blocks of non-isolated POL modules, which typically operate from a 3.3V, 5V or 12V input. For a given voltage and current output, the POL modules cost less than brick-style converters and usually take up less board space. Also, they enable system designers to overcome the challenges caused by the high peak current demands and low noise margins of the latest high-performance semiconductor devices by placing individual POL modules near their point of use. This minimizes losses caused by voltage drops, helps overcome noise sensitivity and EMI emission issues as well as ensures tight regulation under dynamic load conditions.

As the telecom, computer and communications industries continue their migration to IBAs, the increased use of POL modules is altering traditional business models. More and more designers are choosing standard off-the-shelf modules over discrete power

designs because of significantly lower risk, much faster time-to-market and resulting development cost savings.

## 5.3 Two-Stage Approaches of Standard Brick Converters

For datacom and computer applications, intermediate bus architecture is becoming a popular solution. Basically, the first stage is a bus converter that provides an unregulated coarse intermediate voltage, and the second stage provides regulation to load change and slight input voltage change. For telecom applications, the input voltage has a higher range of 36V ~ 75V, and the bus converter concept for datacom applications can be utilized for the brick converter. The difference is that the two stages for the brick converter are integrated into a module.

A brick-type two-stage approach is proposed in Fig. 5.6. In the architecture, the first stage has an unregulated isolated converter with a full duty cycle concept. For the forward and flyback converters, the full-duty cycle cannot be applied because the transformer resetting it has to be considered. For bridge converters, including half bridge, full bridge and push pull, the transformer magnetizing current can be reset naturally, thus full duty cycle is 50 percent. Since the duty cycle is 50 percent unregulated, the intermediate voltage is varied with the input voltage.

The secondary stage is a non-isolated converter with regulation. Since stringent transient response is required from the load, the non-isolated multi-phase buck converter is desirable for the secondary stage because:

(1) Low intermediate bus voltage reduces the switching loss of the up-side-switch and reverse recovery loss of body diode of the low-side switch, which allows the converter to operate at higher switching frequency to meet the transient response.

(2) Lower voltage rated Mosfets can be utilized for switches to reduce conduction loss and switching loss.

(3) Duty cycle can be extended for optimized efficiency.

(4) Multi-phase technology is mature to be used for high-output current and low voltage with current sharing techniques.

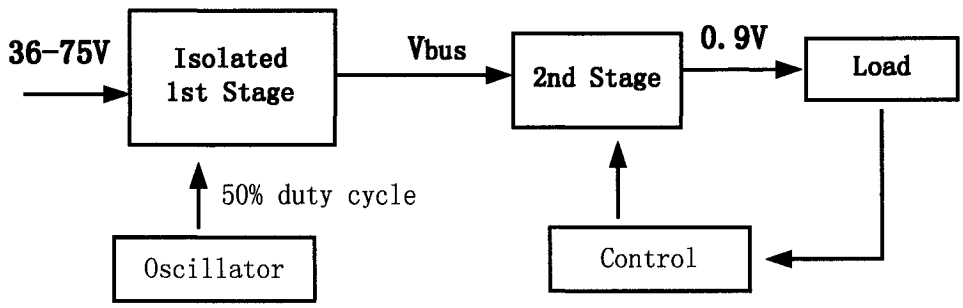



Fig. 5.6 A two-stage approach of brick converter

### 5.3.1 Buck-Type Full-Duty-Cycle Converter Approach

The first stage can be buck-driven or current-driven. Buck-driven first-stage topologies are shown in Fig. 5.7 through Fig. 5.9, and the corresponding waveforms are shown in Fig. 5.10. Since 50 percent of the duty cycle is applied to the bridge topology

with certain dead time, and at the help of leakage inductance, zero-voltage-switching can be achieved. It must be noted that because full-duty cycle is applied, theoretically the duty cycle applied to the secondary-side inductor is full, such that the filter inductance can be zero. Considering the dead time of commutation and leakage inductance, the duty cycle is not ideally full; hence, a very small inductance is employed to achieve a reasonable current ripple.

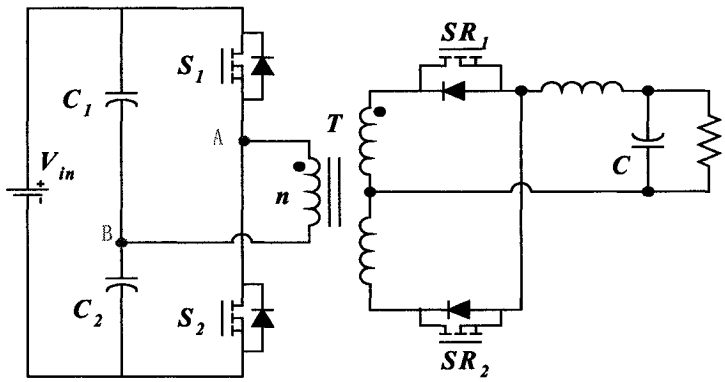



Fig. 5.7 Half-bridge DC-DC converter

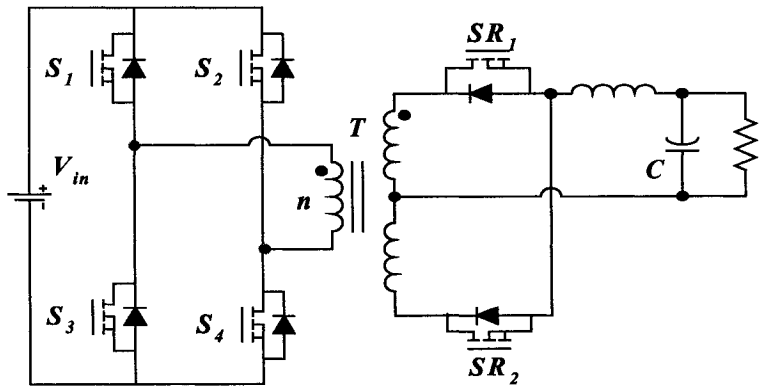



Fig. 5.8 Full-bridge DC-DC converter

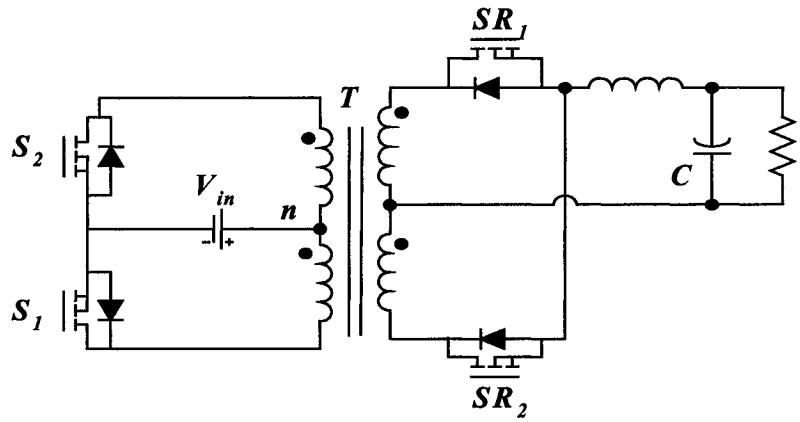



Fig. 5.9 Push-pull DC-DC converter

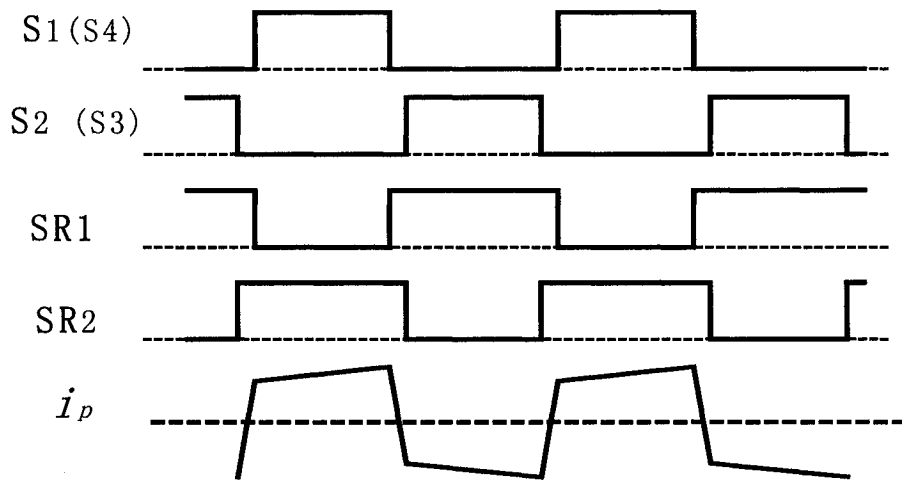



Fig. 5.10 Waveforms of full-duty cycle bridge DC-DC converters

### 5.3.2 Boost-Driven Full-Duty Cycle Converter Approach

As mentioned above, the full-duty cycle concept achieves the benefits of soft-switching and smaller filter inductance and capacitance. Likewise, full-duty-concept can

apply to a current-driven converter. Two types of current-driven topologies are shown in Fig. 5.11 and Fig. 5.12, and the corresponding waveforms are shown in Fig. 5.13. Since they are boost-type converters, the inductor is relocated to the primary side. In fact, this is a good feature for high-current output, because the primary inductor(s) carry a smaller inductor and are easy to design. Because it is a current input topology, the two primary switches cannot be off at any time, thus a short overlap interval has to be added for the two switches.

Similarly, for the push-pull converter, since the duty cycle is close to unit, the primary side inductance is very small. In Fig. 5.12, a current-divider push-pull topology is proposed and utilized on the primary side. In fact, it has a similar principal with current doubler rectifier. The benefit is that the transformer is not tapped, and the current through transformer is one-half of the converter input current, which is good for the transformer design.

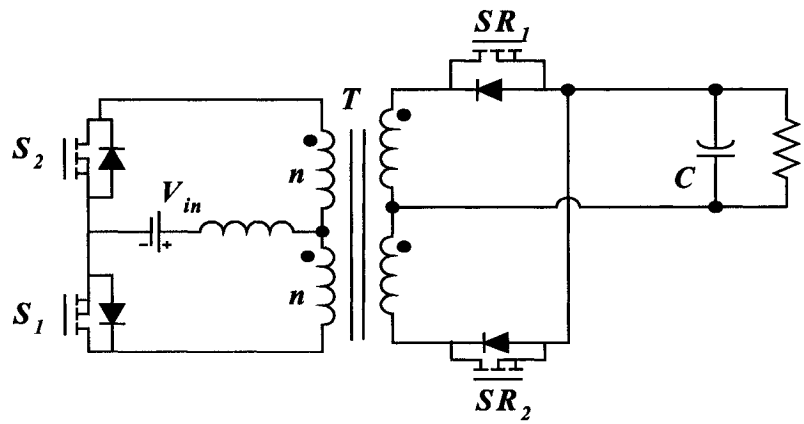



Fig. 5.11 Boost-type push-pull DC-DC converter

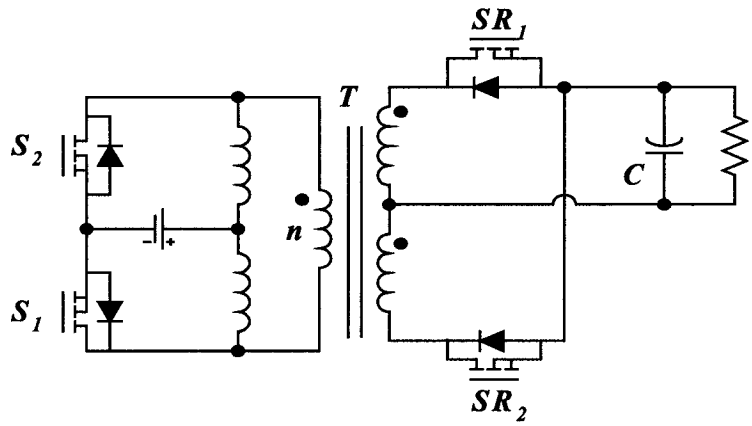



Fig. 5.12 Boost-type current-divider DC-DC converter

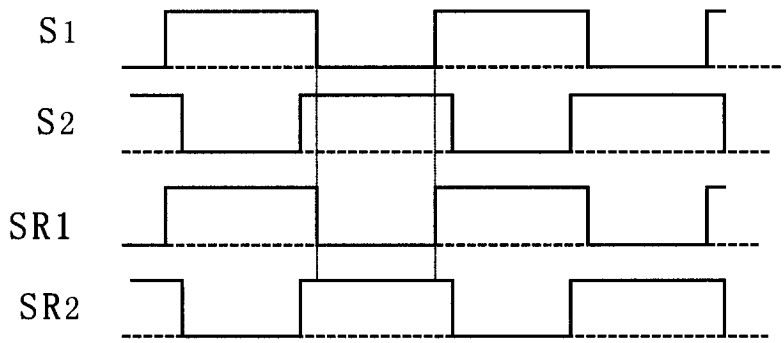



Fig. 5.13 Boost-type current-divider DC-DC converter

### 5.3.3 Transient Response Analysis of Full-Duty -Cycle Converters

From the above analysis, it is clear that filter inductance is a critical factor for transient response. In the full-duty cycle converters, the filter inductance is minimized. A set of open-loop output impedance curves is sketched in Fig. 5.14 with varied filter inductance. It is clear that the resonant impedance spike is reduced with the decreasing

inductance. When the inductance is close to zero, the LC filter becomes a first-order filter. In fact, the first-order output impedance is a desirable feature for DC-DC converters. In the voltage-mode control, zeros in the compensator can cancel one of the double poles of the LC filter. For the current-mode control, the inductor current becomes "controllable" such that the power stage is reduced from first order to second order. However, the order reduction via closed-loop controls is limited by the feedback control delay.

Full-duty cycle converters naturally reduce the power stage system order, such that desirable output impedance characteristics are achieved even for open-loop system. For this first order power stage, compensation becomes easier and fast transient response can be achieved.

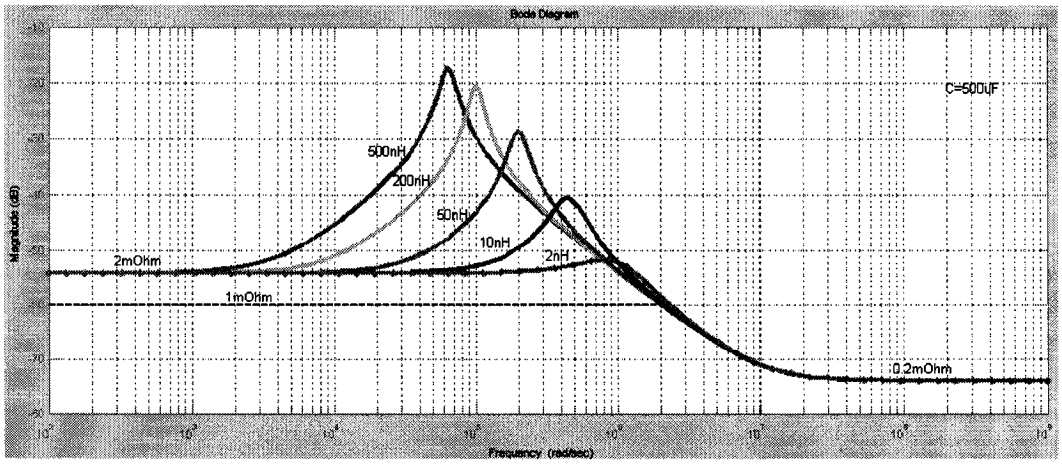



Fig. 5.14 Open-loop output impedance with varied filter inductance

For practical application, the filter inductance cannot be zero considering the switches' commutation dead time and duty cycle loss. For a designed filter inductance, varied output capacitances have an impact on the open-loop output impedance curves. In Fig. 5.15, the filter inductance is assumed equal to 2nH, $R_L$ = 2m Ohm, ESR=0.2m Ohm. With varied output capacitance of 100uF, 500uF and 1500uF, a set of output impedance curves is shown in Fig. 5.15. It can be observed that the output impedance looks more like a first-order system with the increase of output capacitance.

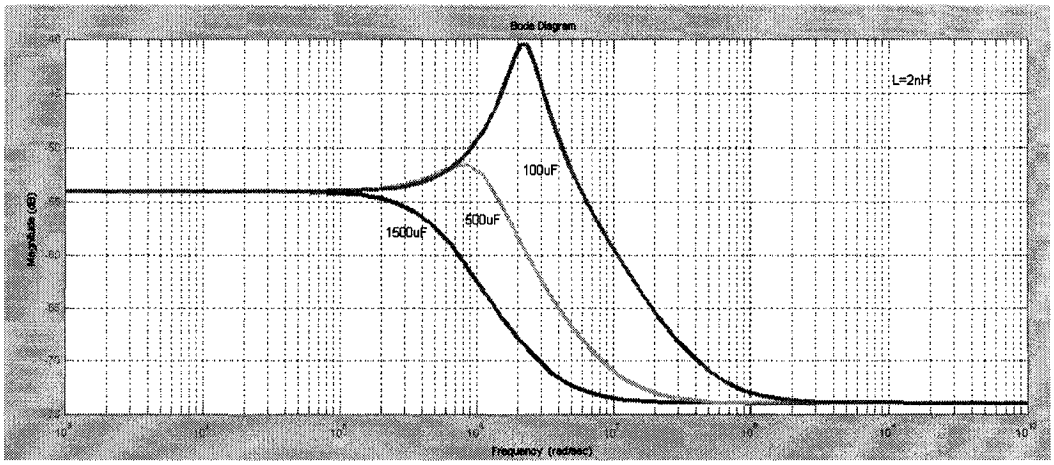



Fig. 5.15 Open-loop output impedance with varied filter capacitance

Full-duty cycle converters achieve low output impedance at a broad range of frequency, thus fast transient response is expected even at extremely high-load current change slew rate. A simulation result is shown in Fig. 5.16, showing that with the current slew rate of 1A/1nS, 70mV output voltage overshoot and undershoot are observed with a

settling time of 6uS. The full-duty cycle concept is a potential solution for the transient response of next-generation power management.

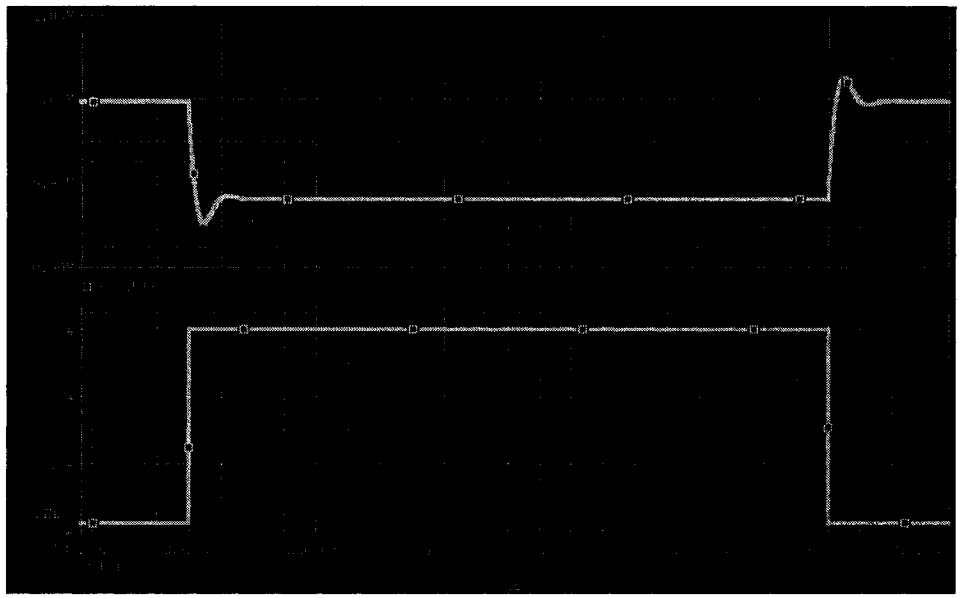


Fig. 5.16 Output voltage response to load change with 1A/1nS current slew rate

## 5.4 Resonant Converters and Two-Stage Approaches

In isolated PWM DC-DC converters, a variety of soft-switching techniques are presented to reduce the switching loss. However, most soft-switching techniques focus on the primary-side switches. For high-current low-voltage DC-DC converters, secondary-side power loss significantly accounts for the overall losses.

Considering the low-voltage output, the synchronous rectification technique should be used. For SRs, there are several kinds of losses including conduction loss, driving loss, reverse recovery loss and crossover conduction loss. Conduction loss depends on the

resistance of SR Fets and reverse recovery loss depends on reverse voltage, Fets and reverse di/dt. Driving loss is determined by the gate charge of SR Fets.

In the following part, the reverse-recovery loss and crossover conduction loss will be discussed in an example topology shown in Fig. 5.17, where the $SR_1$ and $SR_2$ are synchronous rectifiers in the half-wave rectification topology.

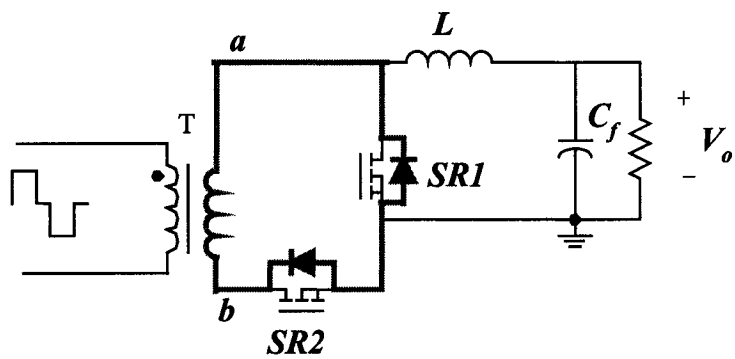



Fig. 5.17 Half-wave rectifier topology

Fig. 5.18 shows the corresponding waveforms of $SR_1$. $SR_1$ and $SR_2$ are complementarily driven, and a dead- time interval is added between them. During the deadtime, before the voltage Vab rises, the $SR_1$ is turned off, so the freewheeling current flows through the body diode of the switch $SR_1$, which leads to crossover conduction loss. It should be noted that even the time interval occupies a small portion of the switching period and the conduction loss in the body diode cannot be neglected, especially with the increased switching frequencies. The other loss related to switching frequency is reverse recovery loss. The reverse recovery waveforms of $SR_1$ are shown in

Fig. 5.18. When a positive voltage $V_{ab}$ is applied, the current through the body diode is reversed, and then the body diode is turned off, which results in a voltage rise and corresponding reverse-recovery switching loss. The higher the voltage $V_{ab}$ and freewheeling current are, the higher the reverse recovery loss.

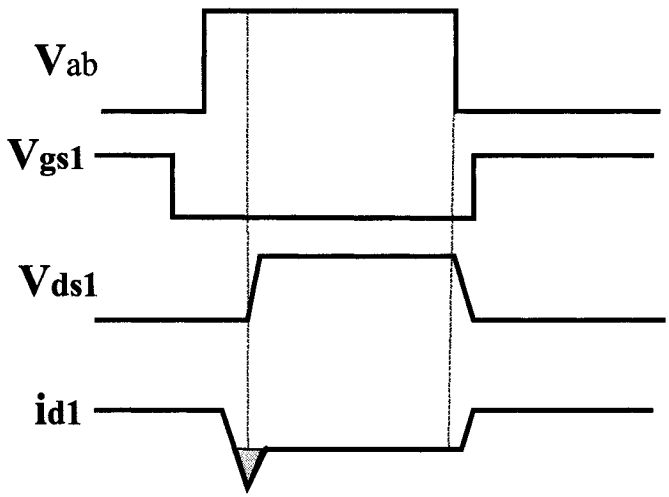



Fig. 5.18 $SR_1$ reverse-recovery waveforms

To reduce the reverse-recovery loss, we can change the wave shape of voltage $V_{ab}$ applied to the reversing body diode. If a sinusoidal voltage is applied to the transformer instead of a square voltage when a body diode turns off, the voltage rises slowly, and thus the reverse recovery loss is reduced. In fact, a zero-voltage reverse recovery is achieved as shown in Fig. 5.19.

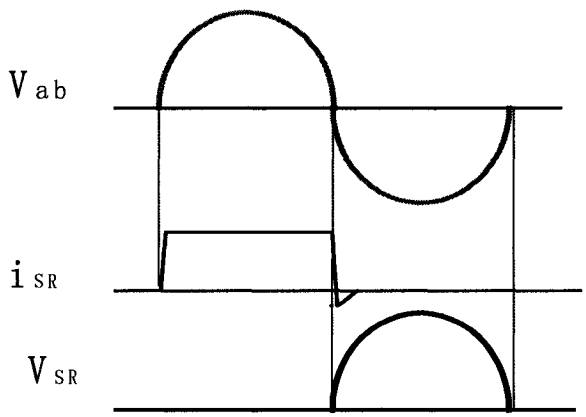



Fig. 5.19 Waveforms of the synchronous rectifier

Class-D parallel resonant converters can achieve sinusoidal voltage. Fig. 5.20 shows a Class-D half-bridge series parallel resonant converter (SPRC or LCC). With the same primary topology, there are three rectification topologies. Among them, the center-tapped rectifier is suitable for low voltage and high current output. Full-bridge and other topologies also can be used in parallel resonant converters.

To reduce the crossover body diode conduction loss, we expect a current flow through the body diode to be nearly zero during the commutation interval. The sinusoidal current can provide a current zero-crossover for two SRs to commutate. Series-resonant-type converters are good candidates to generate a sinusoidal current through the transformer. As shown in Fig. 5.21, the top current waveform is the transformer current. During the SR commiseration interval, the sinusoidal current is near zero, so the currents flowing through body diodes are so small that the body diode crossover conduction loss

is very limited. This is a very big advantage for high-frequency rectifications because with the increase of switching frequencies, the crossover body diode conduction loss increases significantly.

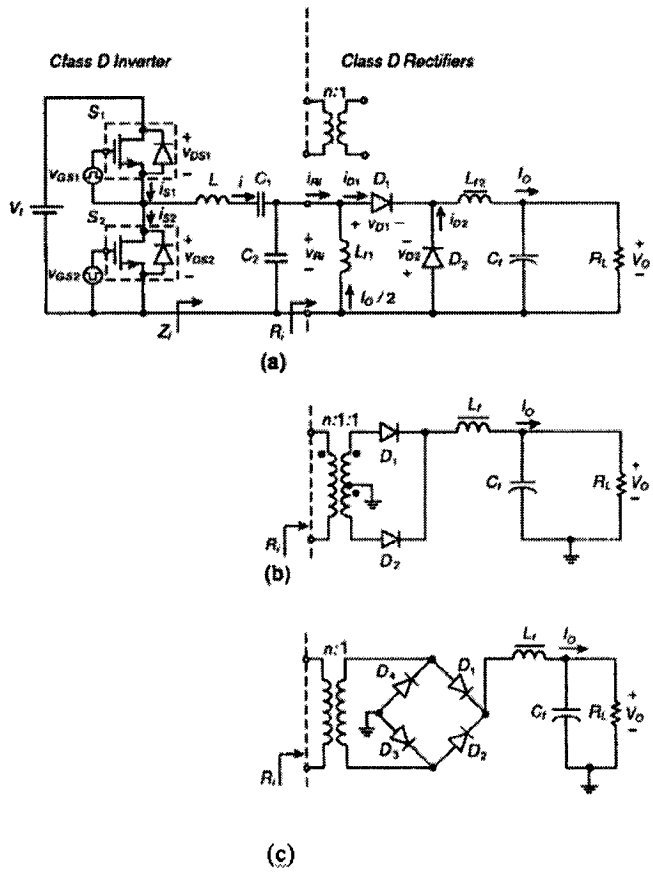



Fig. 5.20 Class-D half-bridge series parallel resonant converter (SPRC)

A series resonant converter has the capability of generating a sinusoidal current waveform feed to the transformer primary side. Since a current waveform is obtained from the transformer, only the capacitor filter is necessary in the secondary side. Fig. 5.22

through Fig. 24 shows several current-driven series resonant converters. If the transformer magnetizing inductance is large enough, compared to resonant inductance, a LLC resonant converter becomes a SRC resonant converter.

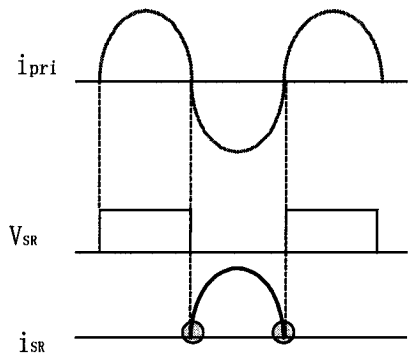



Fig. 5.21 Waveforms of the synchronous rectifier

The main drawback of the SRC converter is that the regulation is difficult at light load. This is because the voltage gain versus frequency becomes flat when the quality factor Q becomes very small at open load. To regulate the output voltage at light load, the switching frequency has to be pushed to a high-switching frequency level. The LLC converter has better voltage regulation because magnetizing inductance is comparable when contrasted with resonant inductance. The LLC converter also has the capability of regulating output voltage to load change and narrow input voltage variations.

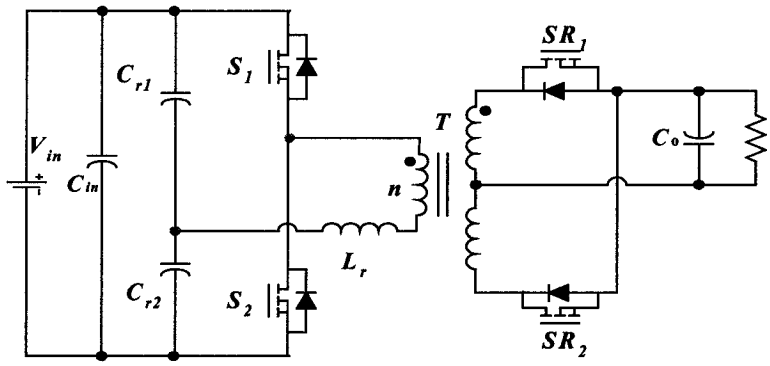



Fig. 5.22 Class-D half-bridge series resonant DC-DC converter

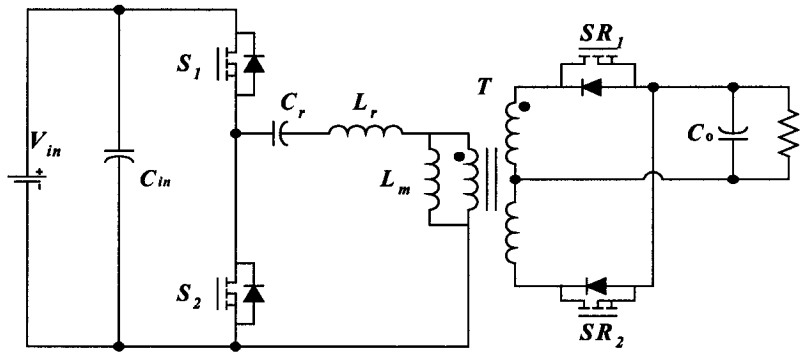



Fig. 5.23 Class-D half-bridge LLC resonant DC-DC converter

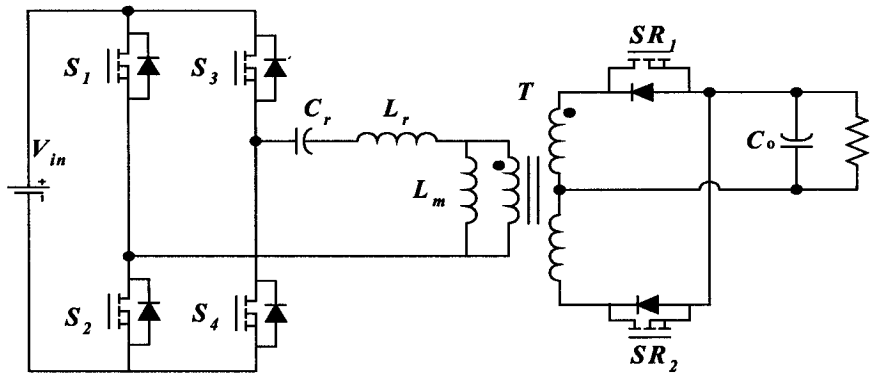



Fig. 5.24 Class-D full-bridge LLC resonant DC-DC converter

As discussed above, the series current resonant converter can achieve zero-voltage switching on the primary side and reduce secondary-side body diode conduction loss. For different resonant quality factor Q values, the DC gain characteristics are shown in Fig. 5.25, where we can observe that the curve voltage gain curves become flat with decreased Q values. Q values are defined as:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{5-1}$$

According to Equation (5-1), for certain resonant tank L and C parameters, Q value increases with the increase of the load. Output voltage regulation via switching frequency is easy to achieve at heavy load. Q value can also be changed by adjusting the resonant tank parameters. Reducing resonant capacitance value or increasing resonant inductance values can increase the Q value. However, high-Q resonance increases the voltage stress across the resonant capacitors. Even at high Q values, when the load is nearly open, Q value is still very low, and the voltage regulation is an issue.

In this part, the low Q series resonant converters (including LLC resonant converters) are proposed in two-stage approaches since the voltage regulation to input voltage variation is not a must. As shown in Fig. 5.26, the SRC or LLC converter is located in the first stage, and the voltage regulation is achieved in the second stage. The main function for the first stage is providing an isolated coarse voltage bus for the second stage, where constant a voltage DC gain is desirable at the range of load variation. Since

low Q is designed for the load range, flat voltage gain characteristic can be achieved. Therefore a relatively constant DC gain can be obtained in the first stage.

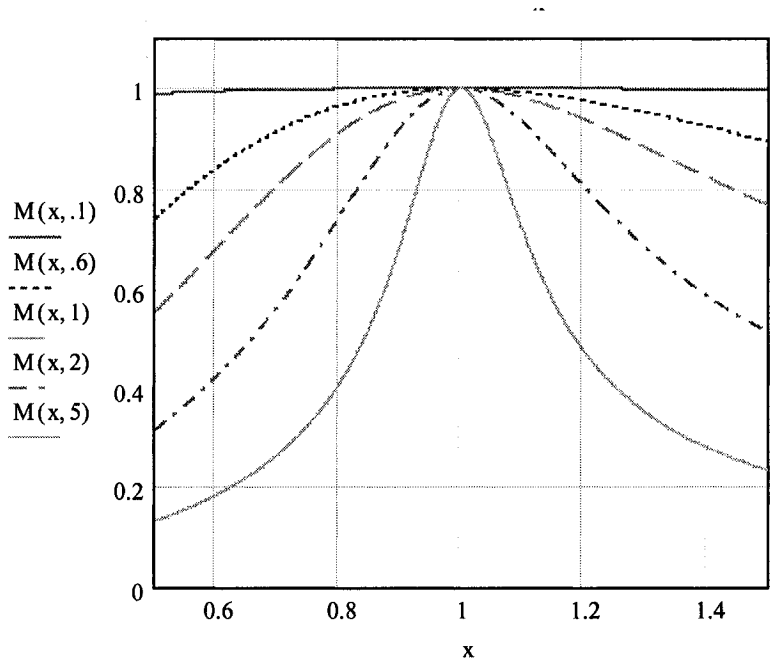



Fig. 5.25 DC voltage gain characteristics vs. normalized switching frequencies

Consequently, we may achieve such benefits in the first stage:

(1) Soft switching for the primary switches.

(2) Reduced body diode crossover conduction loss.

(3) With low Q resonance design, the transformer leakage inductance is utilized and the external resonant inductor may be eliminated.

(4) Low voltage stress across resonant capacitor.

In addition, benefits in the second stage are:

(1) Mature non-isolated POL converter technology is utilized.

(2) With low input bus voltage, switching loss is significantly reduced such that switching frequency can be increased to reduce filter inductance and capacitance.

(3) Fast transient response to load change can be achieved because there are no isolation delays in the feedback loop.

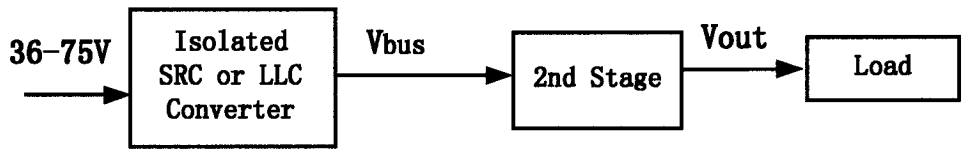



Fig. 5.26 Two-stage approach with SRC or LLC converter in the first stage

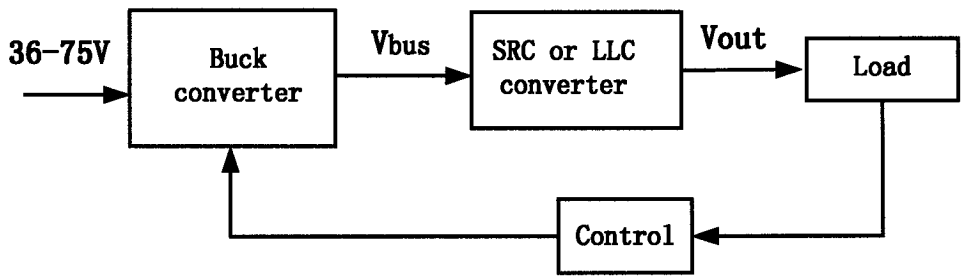



Fig. 5.27 Two-stage approach with SRC or LLC converter in the second stage

The low Q resonance concept also can be used in the second stage as shown in Fig. 5.27. The first stage is a buck converter that operates for voltage regulation. The second

stage provides voltage step down and transformer isolation. With similar benefits to the first stage, switching loss and body diode crossover loss are reduced.

It should be noted that the transient response to load change is improved by the second stage. The main reason for this is because the resonant inductance is reduced, thus the energy transfer is faster. Even before the closed loop controller is involved, the power stage can handle load current change di/dt to some degree.

With neglected inductance in the converter, the input capacitance and output capacitance can be regarded in parallel. With the transformer voltage step down, the output see more output capacitance because the input capacitance is reflected to the output and boosts the output capacitance. The architecture is simplified in Fig. 5.28, and the output capacitance is:

$$C_{eq} = C_{out} + C_{in}(n)^2 \qquad (5\text{-}2)$$

Where, n>>1. A capacitor in the primary side holds more energy because of higher capacitor voltage. This way, on the secondary side, limited-life electrolytic capacitors can be reduced or eliminated saving costs and real estate.

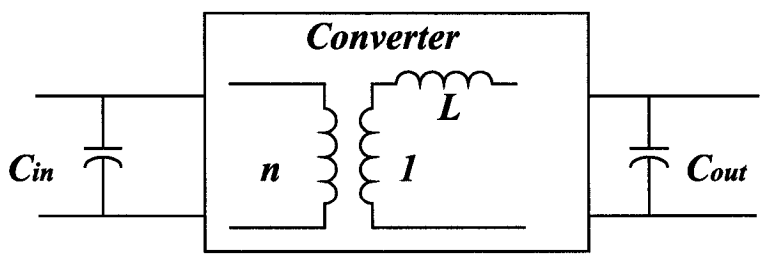



Fig. 5.28 Capacitance boost architecture

## 5.5 A Two-Stage Approach to 48V Input DC-DC Converter

### 5.5.1 Introduction

According to the Intel roadmap, microprocessors requiring 1V and 100~130A will be available in the market in the next two years [E18]. This increase of load current and reduction of its voltage is also accompanied by an increased transient current slew rate at the processor power bus. Most of today's Voltage Regulator Modules (VRMs) draw power from the 12V output of a silver box and use of non-isolated buck converters as on-board VRMs to satisfy the load power requirements [E18 ~E21]. In this case, as the required output voltage becomes lower, higher voltage step-down ratio is required, resulting in small duty cycle, low efficiency and asymmetric transient responses.

With the increase of the required power level, the 12V input bus voltage may not be able to satisfy the requirements. Thus, 48V input-voltage isolated converters are potential candidates for the next generation of low-voltage converters and VRMs [E21], especially for the "servers" and "workstations" of computer systems. In the 48V input-voltage converters, isolation transformers are utilized to step down the input voltage. As a result, the duty cycle can be optimized and better converter efficiency is expected. Moreover, the 48V voltage bus reduces the distribution conduction losses and the required input capacitance becomes smaller.

With the stringent high-current, low-voltage and fast transient requirements of the VRMs, two-stage structure is a potential candidate approach for 48V input converters. The first stage provides an isolated intermediate voltage bus, and the second stage can be

optimized to achieve faster transient response and better efficiency. Furthermore, the first stage is allowed to operate at lower frequency to keep higher overall efficiency, while the second stage is designed to operate at higher frequency to meet the transient requirements.

In two stage converters, the state-of-the-art 12V VRM techniques can be employed in the second-stage converters. However, in the interleaved multi-channel buck converters, the switches operate at hard-switching conditions. Thus, the switching losses increase with the increase of the switching frequency. In this subchapter, a two-stage soft-switching concept is proposed, which allows both first stage and second stage to operate at Zero-Voltage Switching (ZVS) condition.

Based on this concept, the half-bridge topology is employed as the first stage with the fixed 50 percent complementary duty cycles. Both switches operate at zero-voltage switching because of the small dead time between the two drive signals of switches. For the second stage, a non-isolated complementary half bridge and a Duty-Cycle-Shifted (DCS) [E22] non-isolated ZVS half bridge are proposed to achieve soft switching for the second-stage switches. Therefore, all switches in both stages operate at soft switching. Moreover, the non-isolated DCS controlled converter has a novel current sharing capability under voltage-mode control, which is suited for a low-voltage and high-current output converter. In addition, self-driven synchronous rectifiers are utilized for both stages to improve the rectification efficiency and simplify the driving circuits.

### 5.5.2 Proposed Two-Stage Approaches for 48V DC-DC Converters

For 48V nominal input voltage DC-DC converters, the electrical isolation is generally required. In two-stage converter approaches, the isolation transformer may be used in the first stage or second stage. If the transformer is used in the second stage, the first stage topology may be Buck or Boost converter, and second stage may be full bridge, half bridge, forward or push pull, wherein the first stage provides a regulated voltage bus for the second stage, and the second stage steps down the voltage and provides electrical isolation. This configuration is suitable for wide input voltage range.

On the other hand, the isolation transformer can be placed in the first stage while the second stage is non-isolated. This two-stage converter configuration is shown in Fig. 5.29, where the first stage provides step-down intermediate voltage bus and transformer isolation. If the input voltage is relatively fixed at 48V, there is no need to regulate the intermediate voltage, such that open-loop control can be used for the first stage. If the input voltage is variable, e.g. 42~52V, the non-isolated feed-forward loop control can be used to roughly regulate the intermediate bus voltage [E25], which is simpler than feedback control. At this case, the first stage functions as a "DC transformer," and topologies such as full-bridge, half-bridge, forward and push-pull can be used. The second stage is designed to tightly regulate the output voltage and meet the transient requirements, where state-of-the-art 12V multi-channel VRMs or other non-isolated buck-derived converters may be employed. It should be noted that intermediate bus voltage should be optimized according to the value of output voltage and converter power level.

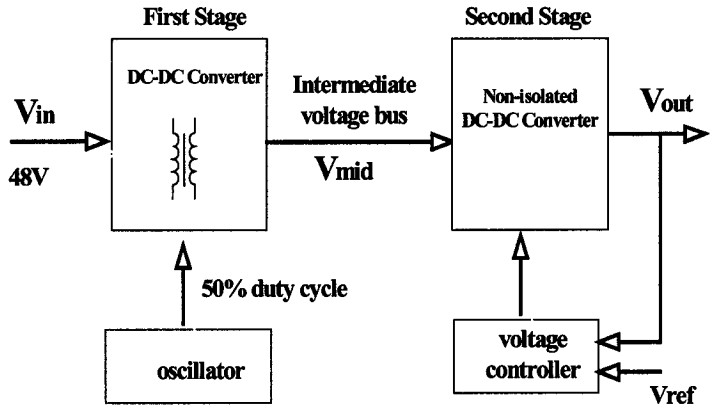



Fig. 5.29 Two-stage approach for high step-down converter

In many cases, the converter input voltage is relatively fixed at 48V, thus the first stage may operate with open-loop control offering a transformer isolation and step-down intermediate voltage bus. Thus an open-loop controlled 50 percent-duty-cycle half-bridge DC-DC converter, shown in Fig. 5.30, can be employed as the first stage. The driving signals of switches $S_1$ and $S_2$ are complementarily generated with nearly 50 percent duty cycle. There are no asymmetric penalties since the duty cycle is always symmetric, which means the voltage and current stresses in the corresponding components are symmetric. Because of the small dead time and the transformer leakage inductance, ZVS can be achieved for both switches, and the leakage-inductance-related ringing is eliminated. Moreover, on the secondary[MEJ1], synchronous rectifiers can be easily driven via extra transformer windings with minimal body diodes losses thanks to the 50 percent duty cycle. The key waveforms of the asymmetric half-bridge DC-DC converter are shown in Fig. 5.31.

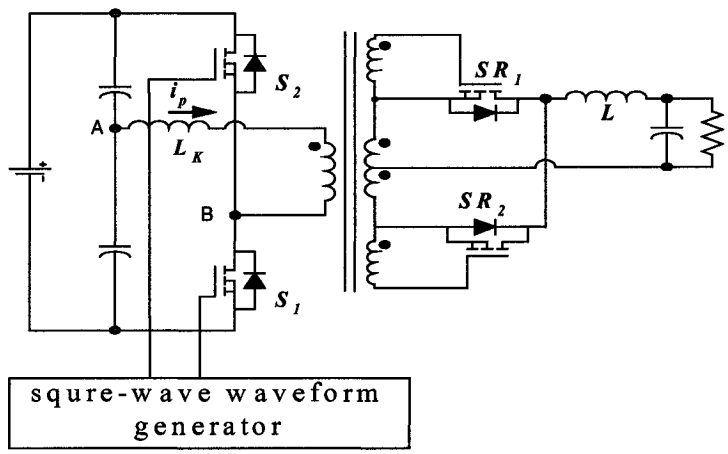



Fig. 5.30 Asymmetric HB ZVS DC-DC converter

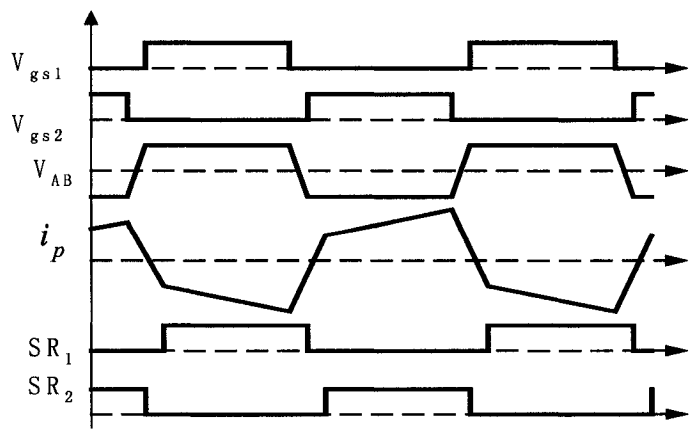



Fig. 5.31 Waveforms of asymmetric HB DC-DC converter

State-of-the-art 12V multi-channel VRMs can be directly employed in the second stage. However, all switches in the VRMs operate at hard-switching conditions, and the small duty cycle results in higher switching and conduction losses. In this section, a

family of non-isolated ZVS topologies is proposed for the second stage to reduce the switching losses, where the main difference from conventional topologies is that the isolation transformers are removed and the circuitry is simplified. A non-isolated full bridge DC-DC converter is shown in Fig. 5.32(a), where the full bridge is controlled with the phase-shift scheme to achieve ZVS for all switches. The duty cycle D (0<D<0.5) may operate at nearly 50 percent to reduce circulating losses since the intermediate voltage is fixed. The output voltage can be expressed as:

$$V_{out} = V_{bus} D \quad (0 \le D \le 0.5) \tag{5-3}$$

Where, $V_{bus}$ is the intermediate bus voltage that depends on the required output voltage, and D is the effective duty cycle. For example, if the required output voltage is 3.3V, for a duty cycle of 0.4 in the steady state, the intermediate voltage bus can be selected as 8.25V.

Inductor Lr is added as a resonant inductance to discharge switches' junction capacitance to achieve ZVS. In addition, Lr is used to limit di/dt to reduce reverse-recovery peak current through the secondary-side body diodes. In addition, schottky diodes $D_1$ and $D_2$, as shown in Fig. 5.32, are used to clamp the voltage spikes of SRs, such that the SRs voltage stresses are significantly reduced and FETs with lower voltage rating can be used as SRs to reduce the conduction loss.

Another non-isolated topology, shown in Fig. 5.32(b), is the asymmetric ZVS half-bridge with a current doubler rectifier. Lr, D1 and D2 in the converter have the same function as in the full-bridge DC-DC converter shown in Fig. 5.32 (a). As a matter of fact,

a current doubler rectifier is a kind of two-channel buck converter, and thus it has the advantages of interleaved buck converters, such as current ripple cancellation and good transient response. With asymmetric control, the topology of Fig. 5.32(b) has two major advantages over conventional two-channel interleaved buck converter: (1) ZVS can be achieved, and (2) self-driven synchronous rectifiers can be used to simplify the SR drive circuitry and reduce cost.

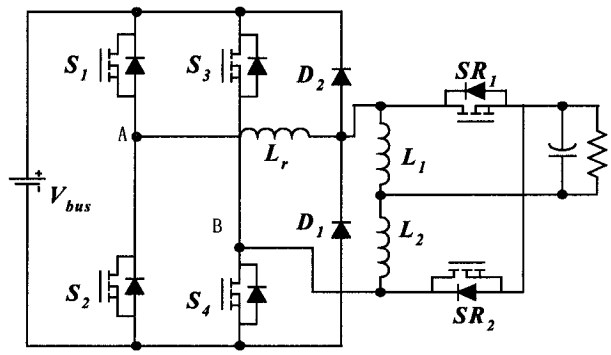



Fig. 5.32 (a) Non-isolated full bridge DC-DC'

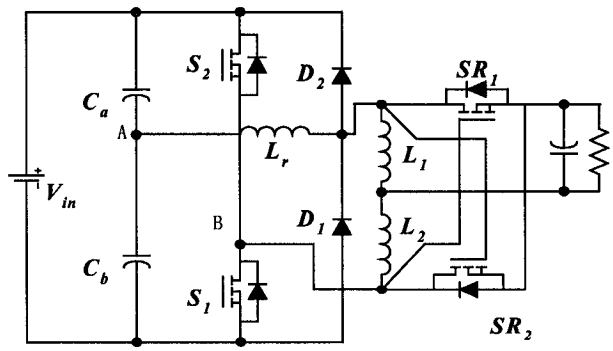



Fig. 5.32 (b) Non-isolated half-bridge DC-DC converter

Fig. 5.32 A family of non-isolated ZVS DC-DC converters

The output voltage is expressed as:

$$V_{out} = V_{bus} D(1-D) \quad (0 \le D \le 0.5) \tag{5-4}$$

It is noted that half-bridge DC-DC converter has higher step-down ratio compared to the full bridge. Thus it has lower output voltage at the same input voltage bus. Half-bridge DC-DC converter is suited for low-voltage high-current applications because of its less transformer primary turns since secondary winding is generally 1 turn for low-voltage output.

Taking into account the duty cycle losses, one may assume that the secondary-side maximum available duty cycle is 0.45. At 9V intermediate bus voltage, the output voltage is around 2V. Since higher intermediate bus voltage may reduce the conduction losses, a non-isolated coupled-current-doubler topology can be introduced to achieve higher intermediate bus voltage [E24].

However, the asymmetric non-isolated half bridge has uneven current and voltage stresses distributed in the corresponding components. The reverse voltage stresses across two synchronous rectifiers (SRs) are expressed:

$$V_{SR1} = V_{in}(1-D_1) \qquad 0 \le D \le 0.5 \tag{5-5}$$

$$V_{SR2} = V_{in} D_1 \qquad 0 \le D \le 0.5 \tag{5-6}$$

The rms currents through the two synchronous rectifiers (SRs) are expressed:

$$I_{SR1} = I_o \sqrt{1-D_1} \qquad 0 \le D \le 0.5 \tag{5-7}$$

$$I_{SR2} = I_o \sqrt{D_1} \qquad 0 \le D \le 0.5 \tag{5-8}$$

From Equations (5.5) ~ (5.8), it can be noted that the higher voltage rating SR carries higher rms current, which leads to asymmetric thermal distribution and thus degrades the rectification efficiency and reliability. Moreover, the current stresses on primary-side switches $S_1$ and $S_2$ are uneven.

As discussed above, non-isolated asymmetric half bridge can achieve ZVS for both switches. However, when the duty cycle goes asymmetric, voltage stresses and current stresses are unevenly distributed. Besides, the converter transient response depends on capacitance of the capacitors $C_a$ and $C_b$.

A Duty-Cycle-Shifted (DCS) ZVS half-bridge DC-DC converter was proposed [E22]. As a second-stage candidate topology, the non-isolated DCS ZVS half-bridge DC-DC converter is proposed as shown in Fig. 5.33, with its corresponding key waveforms shown in Fig. 5.34. In order to charge/discharge the junction capacitance, a resonant inductor Lr is added to achieve ZVS.

It should be noted that the drive signal of switch $S_2$ is shifted left and is close to the falling edge of drive signal of switch $S_1$, such that switch $S_2$ can be turned on at ZVS. During the on-time period of switch $S_2$, switch $S_3$ is turned on at Zero-Current Switching (ZCS). Thus, the energy in the resonant inductor Lr will be trapped through $D_3$ and $S_3$ when switch $S_2$ turns off. Before switch $S_1$ is turned on, switch $S_3$ is turned off to release the energy to discharge junction capacitance and create a ZVS condition for switch $S_1$. Therefore, all switches in the converter operate at soft-switching conditions. In addition, the asymmetric penalties of the asymmetric control HB converter are eliminated, thanks to the equal-duty cycle applied to the two primary-side main switches.

An interesting feature of the non-isolated DCS controlled half-bridge converter is that it has self current-sharing capability; for example, even if the inductors DCR and SRs on-resistance values are asymmetric, the average currents in the two inductors and SRs always stay identical. Therefore, no current sharing control is needed even under voltage mode control. As matter of fact, this current-balance feature can be verified with the use of the average state-space concept [E26]. By solving the average state-space equation, the average currents through the two inductors are:

$$I_{L1} = \frac{D_2}{D_1 + D_2} I_o \tag{5-9}$$

$$I_{L2} = \frac{D_1}{D_1 + D_2} I_o \tag{5-10}$$

Where, $D_1$ and $D_2$ are duty cycle of switch $S_1$ and $S_2$, respectively. Note that the inductors ESR and SRs resistance have no impact on the inductor currents. Since the duty cycles are symmetrically applied to switches, $D_1$ should be equal to $D_2$ and currents in inductors are always equal despite asymmetric inductor DCR and SRs on-resistance values. As a matter of fact, self-current-sharing is an attractive advantage especially for high-current low-voltage applications. Moreover, because the steady-state duty cycle is designed close to 50 percent, $S_3$ and $D_3$ have a very small portion of period to carry current, the conduction losses on that branch are very small.

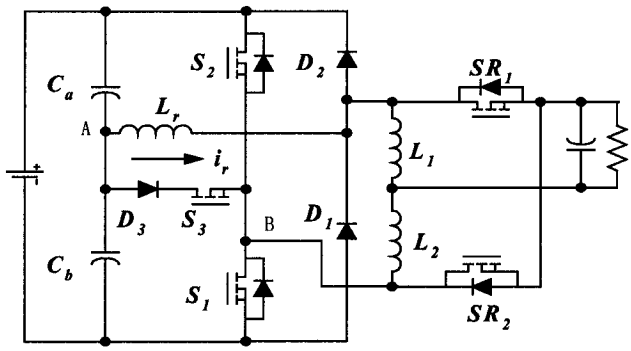



Fig. 5.33 Non-isolated DCS topology

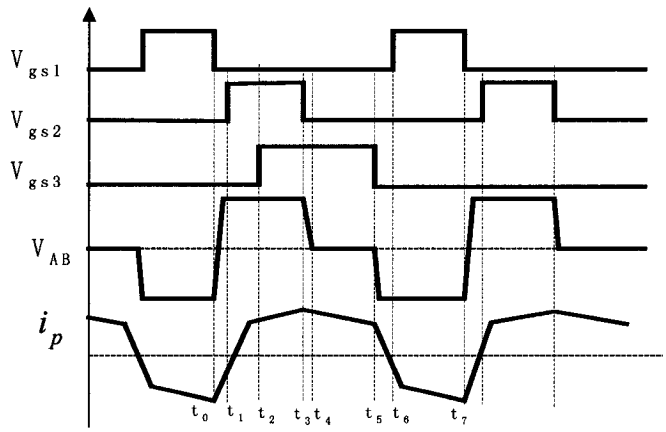



Fig. 5.34 Key waveforms

Because the duty cycle is close to 0.5, good current ripple cancellation can be achieved and the output voltage ripple can be very small. Bulky capacitor may be removed if the converter has sufficiently high bandwidth.

### 5.5.3 Experimental Results

A prototype with the topology of Fig. 5.30 and with 48V input voltage and 10V/10A output was built in the laboratory for experimental verification. Fifty percent fixed-duty-cycle signals are applied to the two main switches. Fig. 5.35(a) shows the transformer primary voltage and current waveforms. It can be observed that the current waveform is very clean. ZVS turn-on behavior of switch $S_1$ is clearly shown in Fig. 5.35(b).

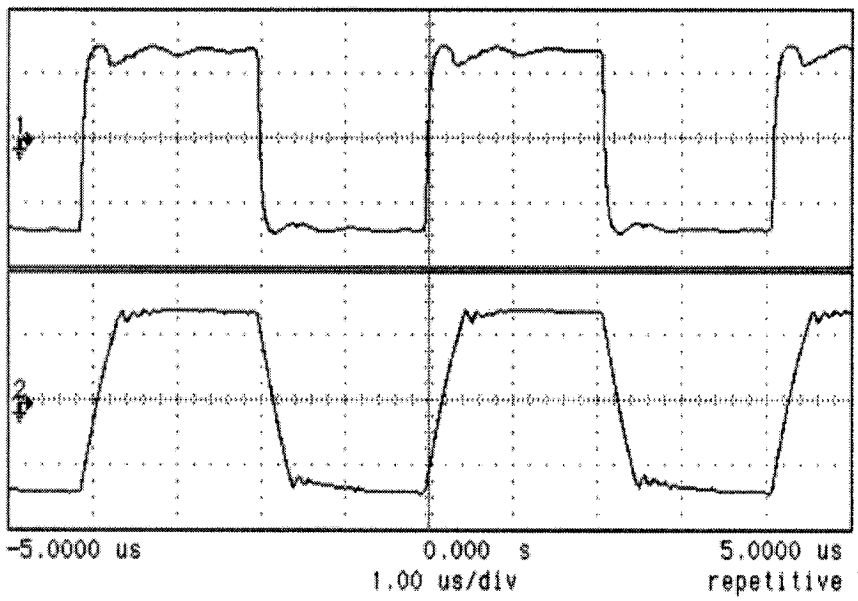



Fig. 5.35 (a) Transformer primary-side voltage and current

(Top trace: 20V/div; Bottom trace: 5A/div)

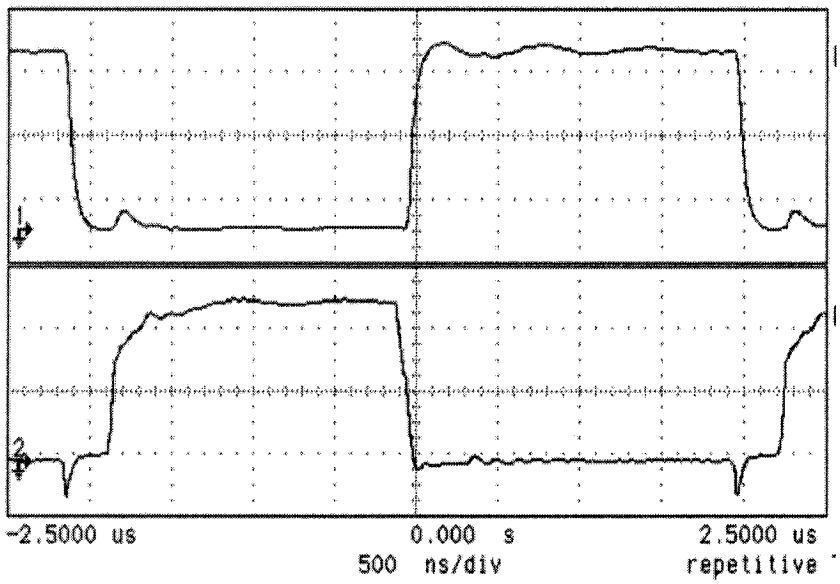



Fig. 5.35 (b) ZVS waveforms of the switch $S_1$

(Top trace Vds 20V/div; Bottom trace Vgs: 5v/div)

Fig. 5.35 Experimental results of the first-stage converter

The second-stage converter shown in Fig. 5.33 is separately built with 10V input and 1.8V/30A output. Fig. 5.36 shows corresponding experimental results. Fig. 5.36(a) shows the gate signals of switches $S_1$, $S_2$ and $S_3$, while Fig. 5.36(b) shows waveforms of $S_1$ drain-to-source voltage and current through resonant inductor Lr. Fig. 5.36(c) shows the ZVS waveforms of switch $S_1$. Note that ZVS range of switch $S_2$ is wider than $S_1$, because the energy in the output inductor current can be utilized to achieve ZVS for switch $S_2$ while energy in the resonant inductor Lr is utilized for ZVS of switch $S_1$.

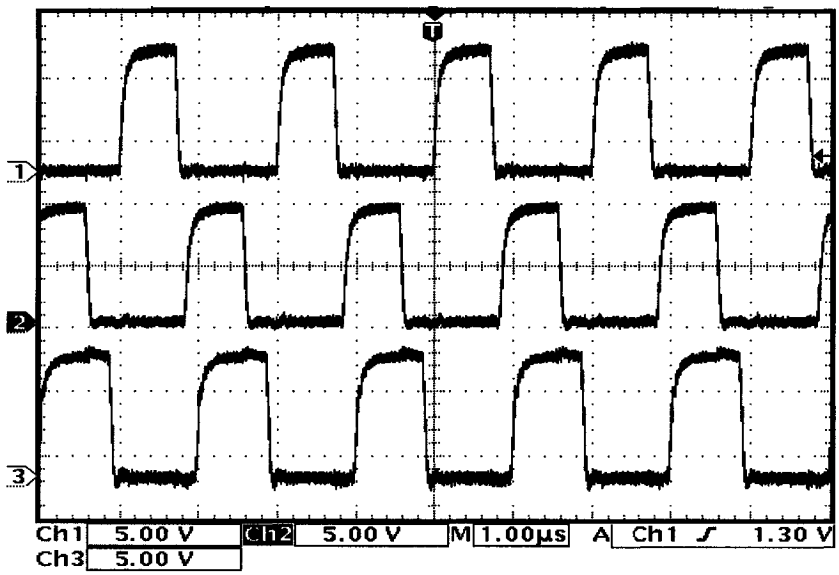



Fig. 5.36 (a) Gate signals

(From top to bottom $S_1 \sim S_3$: 5V/div)

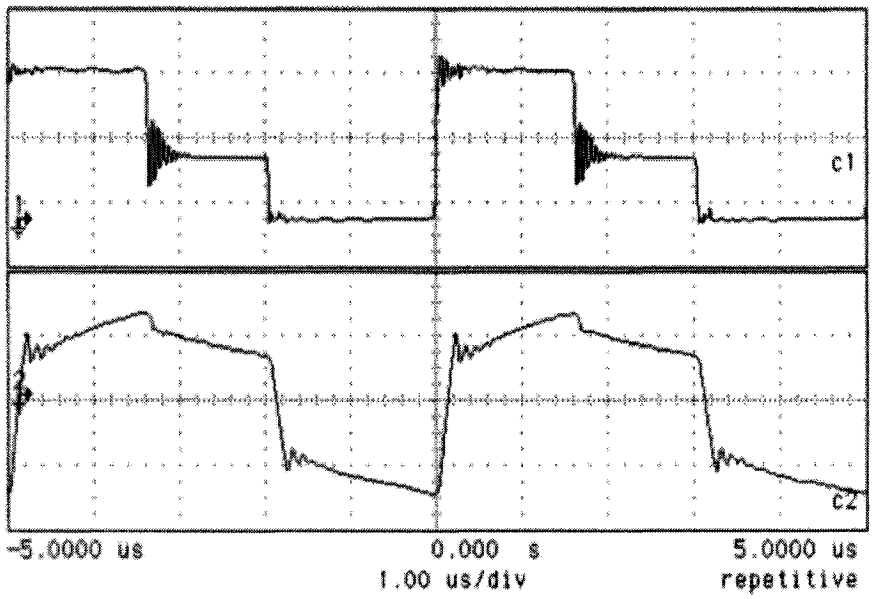



Fig. 5.36 (b) Vds1 voltage and inductor Lr current $i_r$

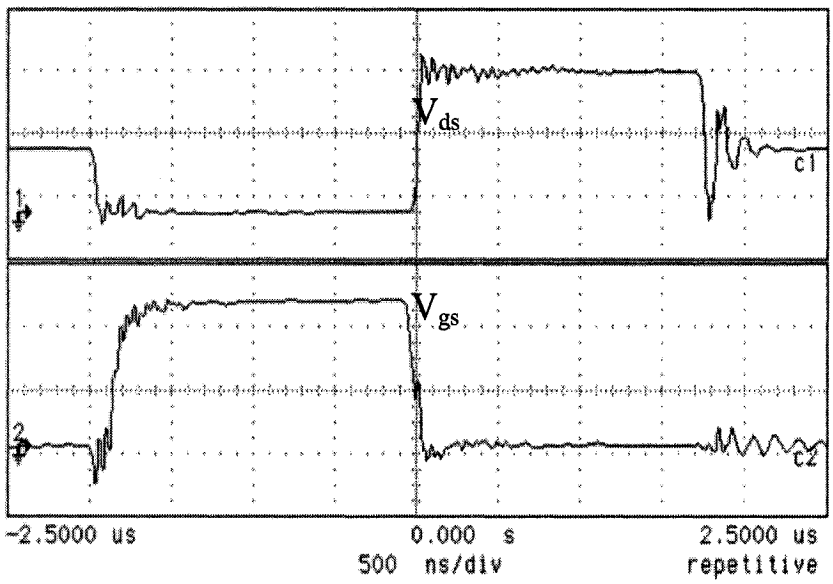



Fig. 5.36 (c) $S_1$ ZVS waveforms

Fig. 5.36 Experimental results of the non-isolated DCS ZVS HB DC-DC converters

### 5.5.4 Summary

A two-stage approach for 48V DC-DC conversion was proposed, where an open-loop-controlled ZVS isolated half-bridge DC-DC converter is used as the first stage, and a non-isolated DCS-controlled ZVS HB DC-DC converter and a non-isolated asymmetric ZVS HB DC-DC converter are proposed for the second stage. In this two-stage scheme, both stages operate at ZVS conditions, which provide the potential for converters to operate at higher switching frequencies to meet the high-density and fast-transient requirements of next generation microprocessors. Initial experimental results verified the two-stage DC-DC converter concept.

# 6. CONCLUSION

This dissertation investigates topology and control techniques in low-voltage high-current on-board DC-DC converters, with the objective of achieving improvements in efficiency and transient response. Major conclusions achieved are summarized as follows:

The half-bridge DC-DC converter is a suitable topology for low-voltage high-current applications, with simpler architecture and smaller transformer turns ratio as compared to other topologies. Current doubler rectifier has a number of advantages over other rectifiers for high-current low-voltage applications. Therefore, half-bridge DC-DC converter with current doubler rectifier is a desirable topology for low-voltage high-current applications with isolation required. This dissertation mainly focuses on half-bridge-derived DC-DC converter topologies and corresponding control, modeling and analysis.

There are two control schemes for half-bridge DC-DC converters: one is symmetric control, and the other is asymmetric control. Symmetric half bridge operates at hard switching conditions, and asymmetric half bridge suffers a penalty of asymmetric current and voltage stresses. A DCS concept is proposed for half-bridge DC-DC converters. Since the on-time of the two switches is equal, the penalty in asymmetric half bridge is avoided. Simply applying DCS control concept to a half-bride bridge DC-DC converter, Zero-Voltage-Switching (ZVS) can be achieved for one of the two main switches.

The DCS concept is improved in a proposed ZVS half-bridge DC-DC converter topology, where an auxiliary branch consisting of an active switch and a diode is added across transformer primary terminals, such that the energy stored in the transformer leakage inductance can be trapped during freewheeling intervals. This energy is utilized to achieve ZVS for the other main switch, and the potential ringing is clamped without dissipative resistive snubbers.

Considering that the active switch in the auxiliary branch mentioned above is floating to the ground, the switch driving circuitry is complex. A modified ZVS half-bridge topology is proposed to have a grounded auxiliary switch. In addition, SR technique is used for the auxiliary branch to reduce conduction loss especially at low duty cycle.

Detailed analysis and a number of experimental results verify the DCS concept and the concept-based ZVS topologies. The concept is successfully demonstrated on a industry demo prototype and high efficiencies are achieved.

At high-line input, the duty cycle becomes small and the freewheeling time becomes significantly long, and the above-mentioned ZVS half-bridge DC-DC converter suffers freewheeling conduction loss. In a conventional half-bridge DC-DC converter, leakage inductance ringing results in loss that is usually dissipated in RC snubbers. An active-clamp topology is proposed in the dissertation, and by recycling the leakage inductance energy to a capacitor, the potential ringing is reduced and higher efficiency is achieved.

For most of the soft-switching techniques, efforts are mainly put on the primary side of the transformer instead of on the synchronous rectifiers. With the increasing switching

frequencies, body diode reverse recovery loss increases proportionally, which decreases conversion efficiency. Two passive lossless snubber circuit topologies are proposed to soften the reverse recovery and attenuate the related-ringing in the current-doubler rectifier. By recycling the leakage inductance energy to the passive snubber when a body diode is turned off, converter efficiency is improved. For the proposed 3D-2C snubber, the body diodes of SRs achieve Zero-Voltage reverse recovery, and the reverse switching loss is reduced.

A half-bridge DC-DC converter with a current-doubler rectifier is physically a two-channel isolated buck converter. The voltage balance and current sharing between two channels are issues, though, since the peak-current-mode control cannot be directly applied to the half-bridge DC-DC converter. A unified DC model is built for symmetric, asymmetric and DCS half-bridge DC-DC converters. Based on the model, DC analysis is conducted and important conclusions are drawn for a variety of half-bridge converters.

According to the DC analysis and experimental results, symmetric half bridge suffers a current unbalance when the inductor DCRs in the current-doubler rectifier is unmatched. To achieve balanced currents, a PCB layout must be carefully carried out. A simple modified current-doubler rectifier topology is proposed to achieve current sharing between two channels even if the inductor DCRs is unmatched.

Output impedance is an important parameter to determine the output voltage transient response to the load current change. Open-loop and closed-loop output impedance characteristics are analyzed based on the AC modeling. It is concluded that filter inductance value is very critical to the transient response.

With the stringent transient response powering requirements, a one-stage DC-DC conversion approach may not achieve very fast transient response. Two-stage approaches may make a trade-off between conversion efficiency and transient response. In the dissertation, a few two-stage approaches are proposed based on the Full-Duty-Concept and resonant converters.

It is found that open-loop controlled Full-Duty-Cycle converters may achieve as desirable output impedance as a closed-loop controlled conventional PWM converter. Full-duty-cycle converters are potential topologies in two-stage approaches.

Class-D resonant converters are investigated and recognized as potential topologies to reduce switching loss and SR conduction loss. Considering the limited regulation capability of class-D resonant converters, low-Q SRC and LLC resonant converters are proposed as candidate topologies in the two-stage approaches. More experimental work needs to be conducted for two-stage approaches.

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