Digital Pulse Width Modulator Techniques For Dc - Dc Converters

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DIGITAL PULSE WIDTH MODULATOR TECHNIQUES FOR DC–DC CONVERTERS

by

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ABSTRACT

Recent research activities focused on improving the steady–state as well as the dynamic behavior of DC–DC converters for proper system performance, by proposing different design methods and control approaches with growing tendency to using digital implementation over analog practices. Because of the rapid advancement in semiconductors and microprocessor industry, digital control grew in popularity among PWM converters and is taking over analog techniques due to availability of fast speed microprocessors, flexibility and immunity to noise and environmental variations. Furthermore, increased interest in Field Programmable Gate Arrays (FPGA) makes it a convenient design platform for digitally controlled converters.

The objective of this research is to propose new digital control schemes, aiming to improve the steady–state and transient responses of a high switching frequency FPGA–based digitally controlled DC–DC converters. The target is to achieve enhanced performance in terms of tight regulation with minimum power consumption and high efficiency at steady–state, as well as shorter settling time with optimal over– and undershoots during transients. The main task is to develop new and innovative digital PWM techniques in order to achieve:

1. Tight regulation at steady–state: by proposing high resolution DPWM architecture, based on Digital Clock Management (DCM) resources available on FPGA boards. The proposed architecture *Window–Masked Segmented Digital Clock Manager–FPGA based Digital Pulse Width Modulator Technique*, is designed to achieve high resolution operating at high switching frequencies with minimum power consumption.

2. Enhanced dynamic response: by applying a shift to the basic saw–tooth DPWM signal, in order to benefit from the best linearity and simplest architecture offered by the

conventional counter–comparator DPWM. This proposed control scheme will help the compensator reach the steady–state value faster. *Dynamically Shifted Ramp Digital Control Technique for Improved Transient Response in DC–DC Converters,* is projected to enhance the transient response by dynamically controlling the ramp signal of the DPWM unit.

Dedication

To my beloved parents Ghazi and Maha Batarseh

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Majd Ghazi Batarseh

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CHAPTER 1:
INTRODUCTION

1.1 Background

The development path in semiconductor technology did not fail to follow the famous prediction of Moore's Law, stating that the number of transistors on a chip doubles about every two years [1]. A clear impact of Moore's law can be noticed on the continuous increase of the number of transistors on processors and microprocessors throughout the years [2, 3]. Figure 1.1 illustrates the roadmap of microprocessors by Intel and predicts that the number of transistors is expected to reach one billion in 2010 [2].

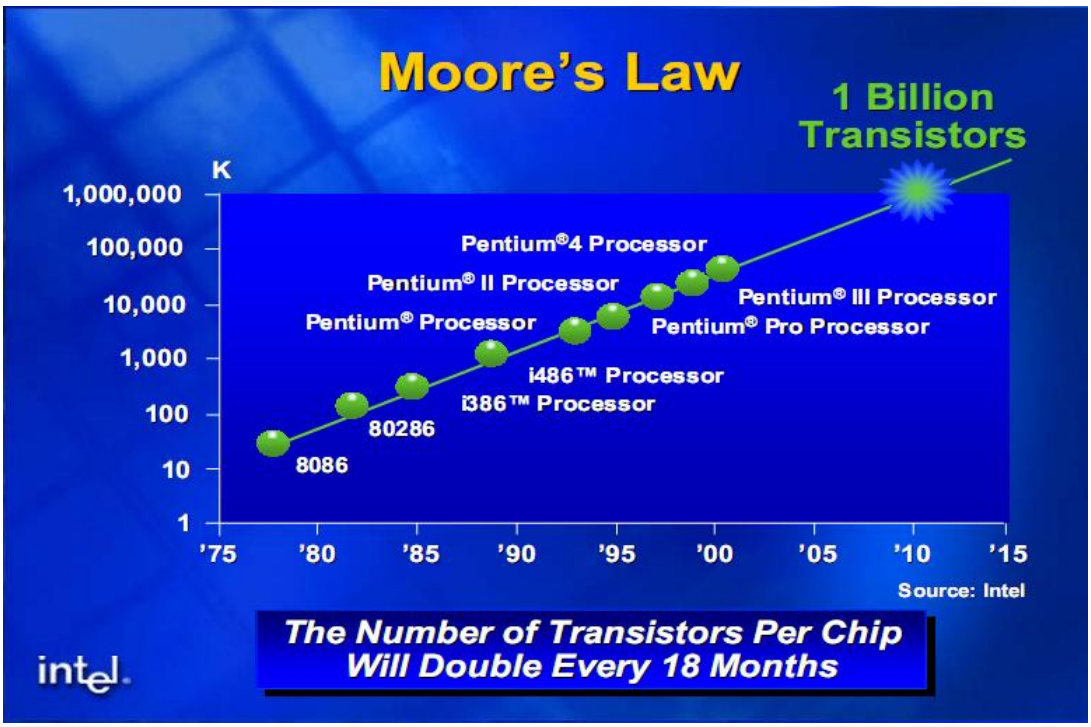


Figure 1.1 Impact of Moore's Law on Intel Microprocessors (Source [2])

Equally, Moore's law affected the whole IC industry in terms of cost, speed, functionality, overall efficiency and reliability. Nowadays, fast and highly sophisticated IC's can be purchased with relatively low cost. Intel Corporation has already launched sophisticated microprocessors with diverse functions and high capabilities running in the GHz range (the latest Pentium IV microprocessor by Intel runs at 3 GHz). Furthermore, Intel is currently working on increasing the speed to tens of GHz in the near future [2]. The growth in IC industry prompted the unprecedented advancement in the technology of digital signal processing which lead to many commercial as well as residential applications and devices based solely on fast multi–functional digital microprocessors.

The benefits reaped out from applying Moore's law, specifically speaking on microprocessors, did not come free of remuneration; many design and control challenges paralleled the advantages discussed above. Figure 1.2 explains the consequential downfalls faced by design engineers as a counterpart to the advantages of Moore's law.

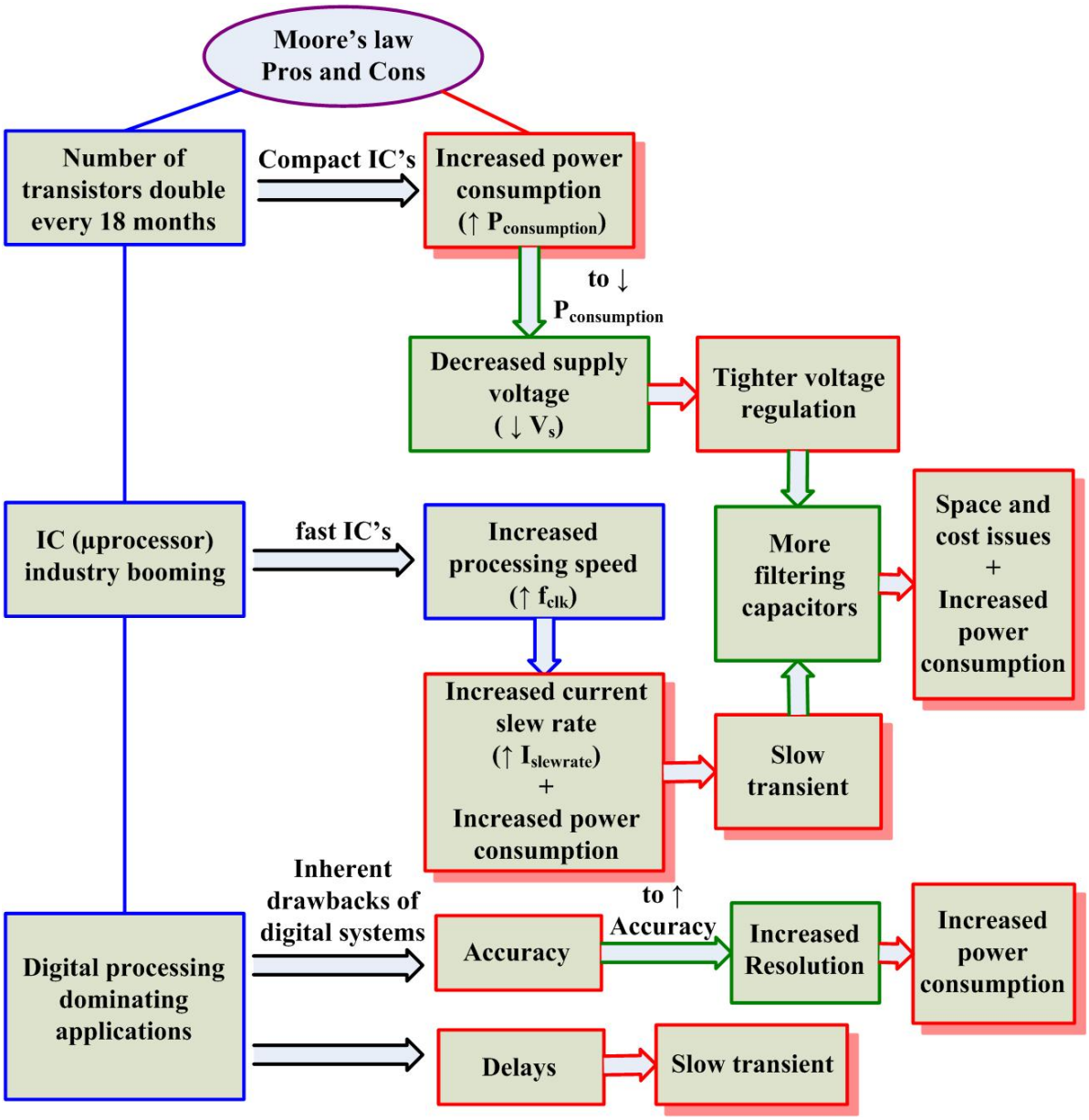


Figure 1.2 Moore's Law: More and Beyond

The consequences of Moore's law on microprocessors industry, exemplified in Figure 1.2, can be summarized in four points:

1. The resultant compact IC design due to increased number of transistors lead to increased power consumption whereas the requirements for fast clocking processor

had caused abrupt load changes (high current slew rates) [2]. For microprocessors to operate at high speeds, the clocking frequency is increased which furthermore results in additional power dissipation as expressed in Equation (1.1), which calculates the electrical power consumed by the processor [4]:

$$P = \alpha \, f_{clk} \, C_{in} \, V^2 \qquad (1.1)$$

Where,

α : is the probability of activation

f_{clk} : clocking frequency

C_{in} : input capacitance

V : is the processor's core voltage

High speed microprocessors are desirable for their performance. Nevertheless, they suffer from high power consumption which makes them unsuitable for low power applications. This in turn opens new research areas in packaging technologies, thermal management and heat dissipation techniques [4, 5]. Given that it is not in the scope of this work, a good summary of some of the power saving techniques implemented on microprocessors is listed in [4]. Moreover, high performance processors, which handle data in high speed, are susceptible to sudden load changes: In the case of microprocessors and CPUs, the amount of data handled by the processor varies with the number of programs being run, and this comprises the processor load. This load may not merely vary but may also change from no load to full load with a very high slew rate reaching up to 120A/μs [6], which eventually leads to deteriorated dynamic response of the system [4].

2. Since power is proportional to the core voltage of the processor as given by Equation (1.1), therefore, to compensate for power dissipation the voltage is decreased [4]. However, in order to maintain the same power level, the load current is increased in accordance with the International Technology Roadmap for Semiconductors (ITRS) as shown in Figure 1.3, where the continuous drop in the voltage with the accompanied increase in load current is noted [2]. Starting in the year 2006, the voltage became lower than 1Volt and expected in 5 years time to reach 75mV in the year 2011, as highlighted in Figure 1.3. Whereas, the load current is anticipated to reach 300A. The decreased load voltage and increased slew rates in turn placed stringent voltage regulation and load control design requirements [2].

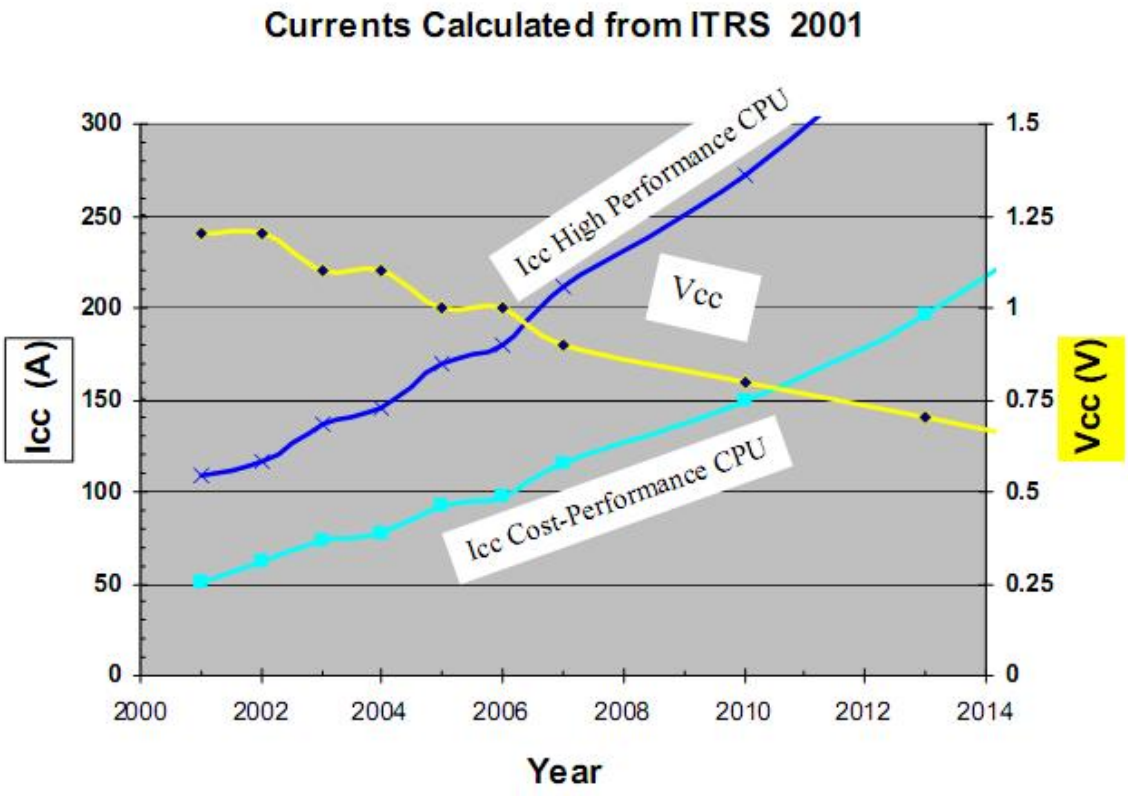


Figure 1.3 Currents Calculated from ITRS (Source [2])

3. More filtering capacitors were added at the load side in order to maintain a well regulated output voltage, taking into consideration the resultant tight regulation due to decreased load voltage as well as the undesired output spikes resulting from the high slew rates at transient conditions. The additional capacitors caused further power consumption as given by Equation (1.1) and illustrated in Figure 1.2, which also adds to the critical motherboard space and cost issues to be carefully handled. Different types and kinds of filtering capacitors play an essential part on transient behavior and output voltage spikes suppression. A study and comparison of how different capacitors affect the transient is given in [4, 7].

4. The development in microprocessors and digital signal processing, initially triggered by Moore's law, had indirectly but predictably paved the way into switching to digital control, as opposed to the conventional analog control techniques. The shift in control domains was due to the following reasons: 1- the development in both the IC industry from one end, as a core and hardware environment and 2- the information technology from another end, as a tool and software platform. Nevertheless, the inevitable and well–known consequences of the digital realm, which are *limited accuracy* and added *sampling and computation delays*, geared the research into focusing on new fields of interest and analytical studies. Hence, many efforts have been put into designing a high–resolution, low–power digital path for a high performance, fast and efficient microprocessor [8 – 129].

1.2 Research Objective and Proposed Techniques

It is the objective of this dissertation to tackle some of the challenges outlined in Figure 1.2 and highlighted above.

Much effort has been dedicated into including both high speed and high resolution in a digital microprocessor and yet maintaining minimum power consumption and utmost dynamic behavior (in terms of transient spikes and settling time). This work is an attempt to harness the benefits of digital control and designing a high resolution DPWM architecture that works at high switching frequency without deteriorating the power consumption as well as achieving both high static and dynamic efficiencies.

The work in this research proposes DPWM architectures addressing the topics of high resolution at high switching frequency converters with optimal power reduction as well as improved transient response. Following is a brief summary of the proposed architectures and control techniques that recap the work of this research:

I. Window–Masked Segmented Digital Clock Manager–FPGA based Digital Pulse Width Modulator Technique

This research presents a new Digital Pulse Width Modulator (DPWM) architecture for Field Programmable Gate Array (FPGA) based systems. The design of the proposed DPWM architecture is based on fully utilizing the Digital Clock Manager (DCM) resources available on new FPGA boards. DCM is a clock management system that enables the following features: input clock frequency duplication, multiplication and division in addition to generating four different phase shifting clock versions: 0°, 90°, 180° and 270°. The phase shifted versions of the input clock have the corrected duty cycle, (corrected duty cycle means a duty cycle locked at 50% with 0.5/0.5 ON–time/OFF–time relationship).

Through analysis and examination of the DCM operation it can be determined that, in order to take full advantage of the DCM modules, the same phase shifts are better utilized if generated with different ON–time/OFF–time relationship other than the 50% corrected default duty cycle.

Another attractive feature of DCM blocks is the ability to cascade them; one DCM module feeds the next to further increase the resolution while using available power–optimized FPGA resources. The design of the proposed DPWM is basically a segmentation of the available power optimized DCM blocks to increase the effective resolution of the system.

Furthermore, this architecture will also add a window–mask signal which limits the DCM operation to only a portion of the switching period in order to further decrease power dissipation. This proposed digital modulator technique allows for higher DPWM resolution with lower power consumption which was the primary barrier to high switching frequency operation.

The presented technique relies on power–optimized resources already existing on new FPGAs, and benefits from the inherit phase shifting properties of the DCM blocks which help in simplifying the duty cycle generation.

The architecture can be applied to achieve different numbers of bits for the DPWM resolution designed for different DC–DC applications, by determining how many DCM modules will be cascaded in the design.

II. Dynamic Ramp Shift Digital Control Technique for Improved Transient Response

A new digital control scheme aiming to improve the transient response and efficiency of an FPGA–based digitally controlled DC–DC converters in terms of shorter settling time with optimal over–and undershoots is also presented in this document. The proposed approach enhances the dynamic response by dynamically controlling the ramp of the Digital Pulse Width Modulator (DPWM) unit through applying a linear and nonlinear shift to the conventional ramp–based DPWM. This will help the compensator reach the steady–state value faster. The dynamic ramp shift design method presented in this research utilizes existing system digital controller, and does not require any additional circuitry.

During transients, the system diverges away from the desired steady–state range, and thus the power stage relies on the compensator to minimize the deviation and return to the wanted steady–state. The longer it takes for the compensator to reach the steady–state, the worse the transient response becomes. The idea of adjusting the offset value of the DPWM ramp was investigated in an attempt to achieve a better dynamics response through reducing the time required by the compensator to reach back to the steady–state during a transient condition. The PWM shifting will only occur during transients for the reason that the error (which basically compromises the shift value) is almost zero during steady–state. While during transients, the positive or negative value of the error will shift the ramp downwards or upwards.

The proposed architecture shifts the ramp signal by a value which is a proportional function of the error signal to compensate for the difference, (deviation of output voltage from the desired reference value) and help the system reach the steady–state faster than the case where the compensator works alone.

1.3 Dissertation Outline

An overview about digital control techniques is given in Chapter 2, the advantages and challenges of digital control in terms of *accuracy* and *delays* are presented. Furthermore, two of the most common voltage mode digital control design methods; *design by emulation* and the *direct design approach*, are presented. Some of the frequently faced digital design issues are also discussed in addition to reviewing several current state–of–the–art DPWM architectures found in literature.

Chapter 3 discusses in details the proposed DPWM architecture; window–masked segmented digital clock manager–FPGA based DPWM technique. First the FPGA resources of Digital Clock Manager (DCM) circuits are presented highlighting the main characteristics of the DCM on–board circuits. In addition to illustrating the new derived features to achieve the desired functionality. Moreover, a comparison between the Delay Locked Loops (DLL) and the DCM based DPWM architecture is clarified in details. The operation of the proposed high resolution segmented DCM based DPWM at high switching frequency is then discussed. Simulation results and experimental verification with power estimation are also given.

Chapter 4 proposes the dynamic ramp–shift digital control technique for improved transient response. The research will first investigate and present this new design method that utilizes existing system digital control. The dynamic linear and non linear ramp–shift is presented to improve the transient response of DC–DC converters by dynamically controlling the ramp of the digital pulse width modulation DPWM unit. Throughout the research, detailed and rigorous analysis and simulations were performed and presented in Chapter 4 to solidly verify the proposed concept followed by experimental results.

In the final chapter, both a summary of the dissertation work, and an outline for a new concept; dynamic clock–adjusted digital ramp control technique for high switching frequency DC–DC converters, are given.

CHAPTER 2:
LITERATURE REVIEW

2.1 Introduction

The transition from the analog control techniques, conventionally applied in power converters, to the recently renewed and deeply investigated digital control was foreseeable due to the many advantages digital control offers [14 – 39] including:

Flexibility: The control law is digitally implemented by writing a software code which makes it easily modified and promptly reprogrammed without requiring hardware modification. This is unlike the on–board discrete components (resistors and capacitors) needed to implement the control law via analog techniques.

Reliability: Digital control realm is a component–free environment with the exception of a power–efficient, compactly integrated, fast and highly reliable microprocessor. This is in sharp contrast to the many analog components (resistors and capacitors) and power amplifiers required to implement the control law in the analog field. Fewer components with tighter integration means failure probabilities are reduced, which makes it nearly immune to aging, temperature, and environmental variations, increasing the reliability of digital controlled systems.

Expandability: Digital control techniques can be easily expanded to include sophisticated in addition to nonlinear control algorithms by simply expressing the architecture in software code rather than building the circuit using hardware components. These complicated control techniques are difficult to be implemented in the analog PWM switch mode power supplies. However, non–linear control techniques, which are easily expressed in digital control, was

proven to achieve enhanced steady–state regulation as well as dynamic behavior of DC–DC converters.

On the other hand, digital control falls short compared to the *infinite–resolution* and *sampling–free* analog control. One of the setbacks of digital control is the resolution of the two main building blocks of the digital loop: the Analog to Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM). While, the conventional analog control is ideally assumed to have infinite resolution, the resolution of the two digital blocks decides the accuracy by which the duty cycle is determined.

Thus, the advantages of digital control listed above should be weighed against the drawbacks naturally inherent in discrete systems and which can be summarized in two main points:

1- Reduced *accuracy* due to limited resolution: only finite set of discrete values can be used to represent any analog signal. Analog control excels over its digital counterpart by its ideally infinite resolution.

2- Added *delays* due to sampling and processing times: Round off and truncations errors resulting from the quantization effect can become noise sources where some kind of filter structure is needed to alleviate the quantization effect [76 – 77, 79]. Quantization also adds to the delay time of the system [76, 40].

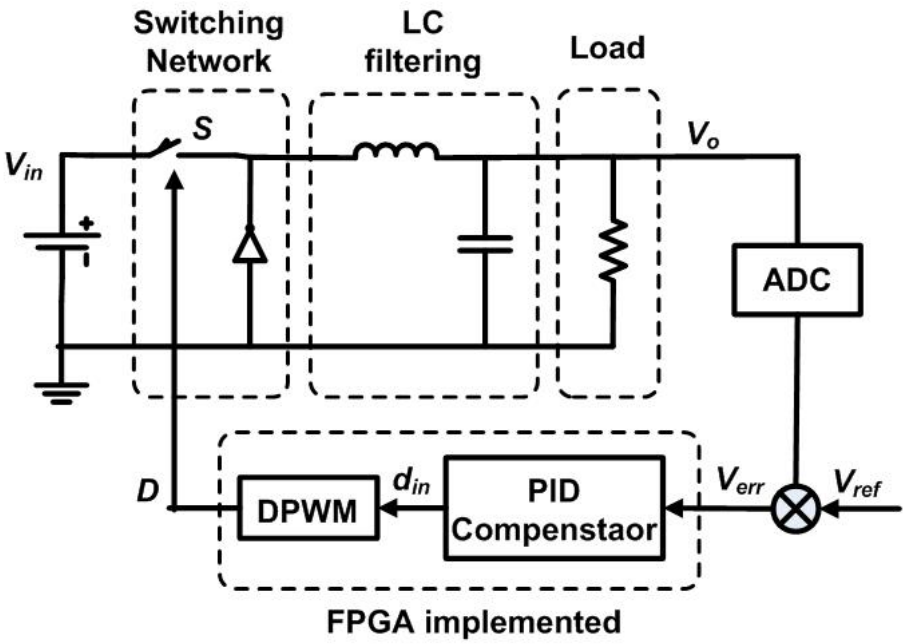


Figure 2.1 Digitally Controlled DC–DC Buck Converter

Figure 2.1 shows a circuit schematic for a digitally controlled DC–DC buck converter. The digital loop starts at the Analog to Digital Converter (ADC) where the sensed output voltage is first digitized and is next compared to the desired reference value, V_{ref}, the resulting error signal, V_{err}, is subsequently minimized through the action of the PID compensator which generates a duty cycle command (d_{in}), trying to maintain a near zero error signal and enhance the dynamic performance of the overall system. The output of the compensator is a digital representation of the duty cycle, (d_{in}) represented in discrete format from the Most to Least Significant Bit (MSB to LSB) as $d[MSB, \cdots, LSB]$. The compensator is followed by the DPWM which translates the discrete duty cycle command of the compensator into an analog Pulse Width Modulated driving signal (D), controlling the ON–time of the main switch S. Consequently, a well designed PID compensator and high resolution DPWM architecture are essential to achieve a tightly regulated converter output.

The least significant bit (LSB) of the DPWM determines the minimum change in the duty cycle. Thus the resolution of the DPWM is very critical in deciding the accuracy and the overall performance of the converter. Consequently, a well designed PID compensator and high resolution DPWM architecture are essential to achieve a tightly regulated converter output.

Thus, research has been dedicated into increasing the accuracy of the system by increasing the DPWM resolution without increasing power loss and deteriorating efficiency specifically at high switching frequencies.

In other words, a more accurate performance entails high resolution DPWM. High resolution DPWM is required for the following reasons to mention a few:

1- Avoiding limit cycling which will be explained in the following section.

2- DPWM resolution is proportional to the switching frequency; the higher the resolution, the higher the cost and the higher the sampling frequency required which can prove to be impractical in terms of needed oscillator, particularly at high switching frequency.

2.1.1 ADC Resolution

In order to fully leverage the advantages of digital control, the two previously mentioned well–known and thoroughly–studied challenges; *accuracy* and *delay* should be addressed. Research has focused on decreasing the delay and increasing the accuracy of both the ADC

and DPWM. Significant effort has been devoted to analyzing the ADC resolution requirements [27, 41, 76 – 77].

Stated concisely; the system specifications for the minimum output voltage quantization, ΔV_o, and the desired output voltage, V_o, determine the minimum required resolution of the ADC in order to meet the desired design specifications with respect to output voltage regulation [27, 41, 76 – 77], as shown in Figure 2.2.

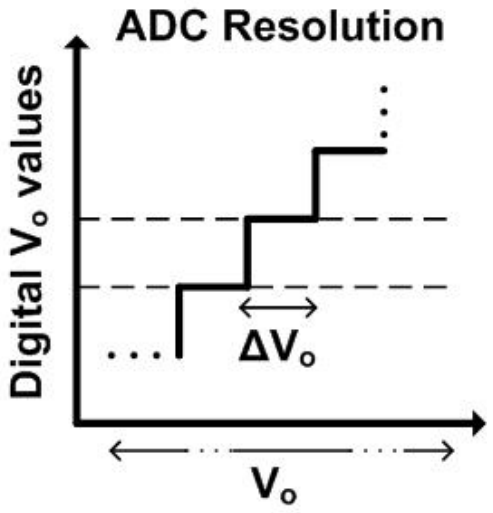


Figure 2.2 Output Voltage Quantization and ADC Resolution

Another important parameter to be assigned to the ADC is the sampling frequency. Sampling at the switching frequency results in 180° phase delay, Nyquist theorem sets the sampling frequency threshold to be, at its least, twice the switching frequency in order to correctly reconstruct the signal and avoid any aliasing effect [14 – 16, 23]. On one hand, higher switching frequency helps minimize magnetic size and enhance the dynamic performance. But on the other hand, higher switching frequencies place the sampling

frequency to be in the MHz range which can be impractical and extremely costly. Taking into consideration that sampling at twice the switching frequency will result in 90° phase delay which can still impair the performance of the converter. Some designers sample at frequencies around ten times higher than the switching frequencies to minimize the phase delay and avoid reconstruction problems.

The sampling action of the ADC, the propagation and computational time and the DAC process of the DPWM cause a delay between the instant the output voltage is sensed and the time the duty cycle is accordingly generated, this delay deteriorates the efficiency of the overall performance of the converter and degrades the dynamic response.

Research focused on increasing the accuracy of the ADC and DPWM as well as decreasing the delay time in order to take full advantage of applying digital control laws to PWM converters.

2.1.2 Limit Cycle Oscillation

Due to the limited resolution of any digital system, only limited discrete values of the duty cycle are obtained, which consequently means that only discrete values of the output voltage can be achieved at the load side. If the desired output voltage, which guarantees a zero error signal, is not mapped to exactly one of the available discrete values, then the feedback loop will continually alternate between at least two available values of the duty cycle. This kind of fluctuation is referred to as limit cycle oscillation [76 – 77].

The main guideline to avoid the undesired limit cycle oscillations is to guarantee the mapping between minimum variations of the output voltage to a discrete duty cycle value that maintains a zero error signal. This condition can be realized by a DPWM resolution higher than that of the ADC as illustrated in Figure 2.3.

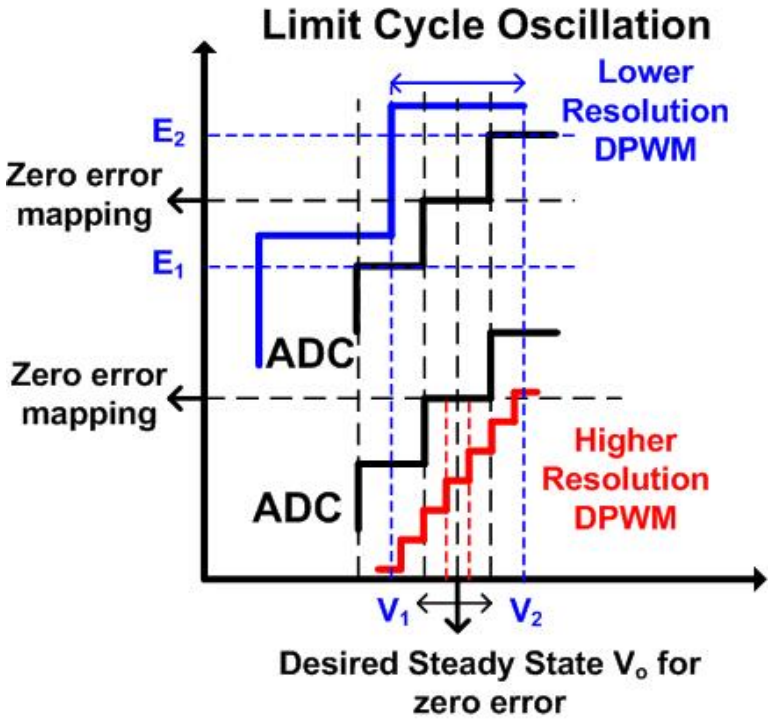


Figure 2.3 Limit Cycle Resolved

Figure 2.3 illustrates two cases; the first is a DPWM with lower resolution than that of the ADC; it can be noted that the output voltage is alternating between V_1 and V_2 values trying, unsuccessfully, to map and achieve the desired output voltage. However, since the DPWM cannot generate the required duty cycle value that produces the desired output voltage, due to low resolution, therefore the system will not reach zero error signal and effectively, creates

undesired limit cycle oscillation superimposed on the load voltage. The second case is a DPWM with higher resolution than the ADC, and as depicted in Figure 2.3 with a DPWM resolution exceeding the ADC, multiple duty cycle commands can possibly be mapped to the desired output voltage which means that the zero error quantization level can be certainly reached.

Therefore, selecting the ADC resolution is of great importance for the overall system given that it places a threshold for the minimum DPWM resolution required to avoid any unwanted limit cycle oscillations [76 – 77, 79].

2.2 Voltage Mode Digital Design Methods for DC–DC Converters

Many efforts have been dedicated to review and compare the various digital control design approaches for DC–DC converters [14 – 39]. Basically, there are two main methods to design a digital compensator discussed below:

2.2.1 Digital Redesign Approach (Design by Emulation)

Where, first, the delays due to sampling is modeled as delay element and added to the system then an analog controller is designed using the well known control knowledge of Bode plots in the continuous s–domain. Afterwards one of the several available discretization methods is applied to digitize the derived analog controller [9, 14, 17].

The Redesign Approach makes use of the well known analog control design procedure, on the other hand, ignoring the sampling and hold effect leads to inaccurate dynamic

performance [14, 17]. Backward Euler, Bilinear transformation, the step invariant method and the Pole/Zero match transformation are some discretization methods used in the redesign method. Each of those digitization methods offers an advantage and a trade–off disadvantage as listed in [14, 17].

2.2.2 Direct Digital Design Approach

As the name states, this approach first digitizes the converter and treats the system in the digital z–domain directly. The ADC is represented by an ideal sampler with T_s sampling frequency. Despite the fact that, a Zero Order Hold device $\left(ZOH(s)\right)$ is what is typically used in literature to represent both the ADC and the DPWM. First and second order sample and hold devices may also be applied [23, 26].

The zero order hold can be expressed in the s domain as shown in Equation (2.1) [23, 26]

$$ZOH(s) = \frac{1 - e^{-s\,T_s}}{s} \qquad (2.1)$$

The effect of sampling and hold introduces 180° phase delay when the sampling is done at the switching frequency. To get 18° phase delay, the sampling frequency should be roughly ten times higher than the switching frequency which dictates a very fast DSP.

The work in [9] compared the effect of varying the ADC delay, the more the ADC delay, the less the phase and gain margins which leads into driving the system to instability.

Direct Design method results in a better transient response; since the effect of the sample and hold is taken into account prior to the compensator design which in turn leads to better phase margin and bandwidth. The frequency response method, the graphical root locus method and the deadbeat control are some z domain controller design approaches. Efforts have been put into trying to benefit from the advantages each technique offers and compensating their setbacks by utilizing two of the above control methods [9, 14, 17, 23].

2.3 Digital Control Implementation Platforms

Digital control deals with two areas; control law design and power management capabilities [14–39]. While, the control law is applied to maintain a well regulated output by controlling the ON time of the switches, power management on the other hand helps protect the system and provides communication means between the device and its environment [14–39].

Power management relies on available protocols; IPMI (Intelligent Platform Management Interface) and PMBus which is gaining popularity among power supply and semiconductor manufacturers. Data transportation is carried out using I^2C or SMBus [29].

Digital control can be implemented using one of the following implementation techniques [15, 29, 40]:

1. Digital Signal Processing (DSP)

2. Field Programming Gate Array (FPGA)
3. Custom Hardware
4. Some combination form of software and custom hardware

The flexibility the DSP chip offers, via reprogramming and the capability of addressing multiple tasks is offset by the cost and speed of the DSP [29].

FPGAs are faster than DSP chips but they are of higher cost. They are attracting more attention and dedicated effort in modeling, simulation and design verification fields [15, 29].

Dedicated custom ICs need to be designed, layout and manufactured, nevertheless, they are cheaper than DSPs and FPGAs and provide better performance [29].

Researchers are trying to combine custom hardware with processor based power management in an attempt to get easily implemented system with optimized cost and performance [29].

2.4 DPWM State of the Art Architectures

As the push for higher power densities and high integration, DC–DC converters are expected to operate at switching frequencies exceeding tens of MHz, resulting in a new set of challenges that create new research opportunities in DPWMs [40 – 62]. Many DPWM

architectures are presented in the open literature including: counter comparator [44], delay line [17–18, 44], hybrid DPWM [43], segmented delay line [45], dithering [17, 28], etc. to name a few. Each of the existing DPWM architectures has some advantages and disadvantages depending on the application as discussed below.

Counter comparator based DPWM: The simplest DPWM architecture is a direct emulation of the PWM ramp, offering the best linearity. It is basically a digital form of the conventional analog duty cycle generation where a digital saw–tooth signal with a frequency equals to the switching frequency of the converter, f_{sw}, is compared to the duty cycle value coming from the compensator, d_{in} as clarified in Figure 2.4. The duty cycle is set high every time the counter of the ramp signal resets to zero. On the other hand, the comparator resets the duty cycle by triggering the instance at which the commanded duty cycle d_{in} exceeds the ramp signal, as shown in Figure 2.4. Nevertheless, the resolution of the DPWM and the switching frequency determine the clock frequency of the counter. Hence, with high switching frequencies and high DPWM resolution, the required clock frequency may be impractically large, particularly in terms of power consumption [44].

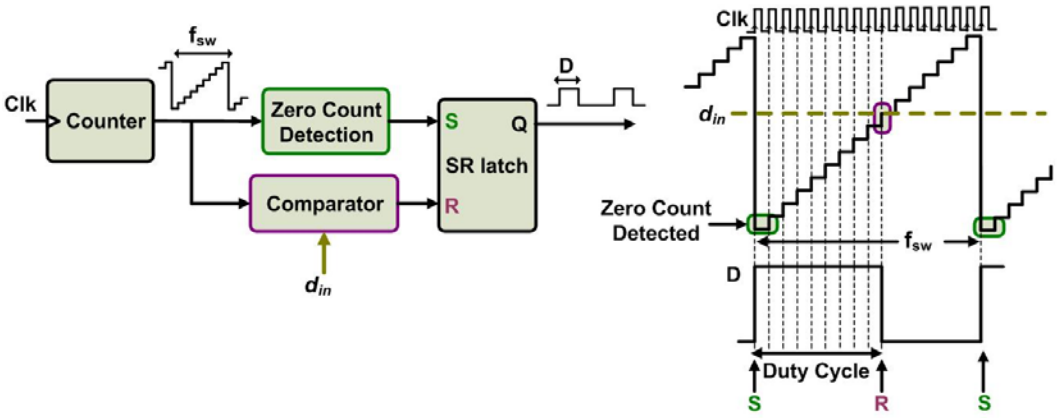


Figure 2.4 Counter–Comparator DPWM architecture

Delay line architecture: This technique, shown in Figure 2.5, uses the switching frequency as a clock frequency; which helps in decreasing the power consumption at the expense of large area in terms of increased gate count with more delays [17–18, 44]. The DPWM output is set high at a clock pulse signal which will propagate down the delay line till it reaches the output set value [44]. $2^{N_{DPWM}}$ Delay elements and a $2^{N_{DPWM}} \times 1$ multiplexer comprise the delay line based–DWPM, where N_{DPWM} is the DPWM resolution in bits. This architecture helps eliminate the high clock frequency needed by the counter comparator approach as an advantage, but the large area needed for the $2^{N_{DPWM}}$ delay elements and the multiplexer makes it unsuitable for high resolution DPWM. Device matching is another issue with such high number of delay elements which may also affect the linearity of the digital control, even though digital control tolerates a certain amount of non linearity compared to the analog control realm [17–18, 44].

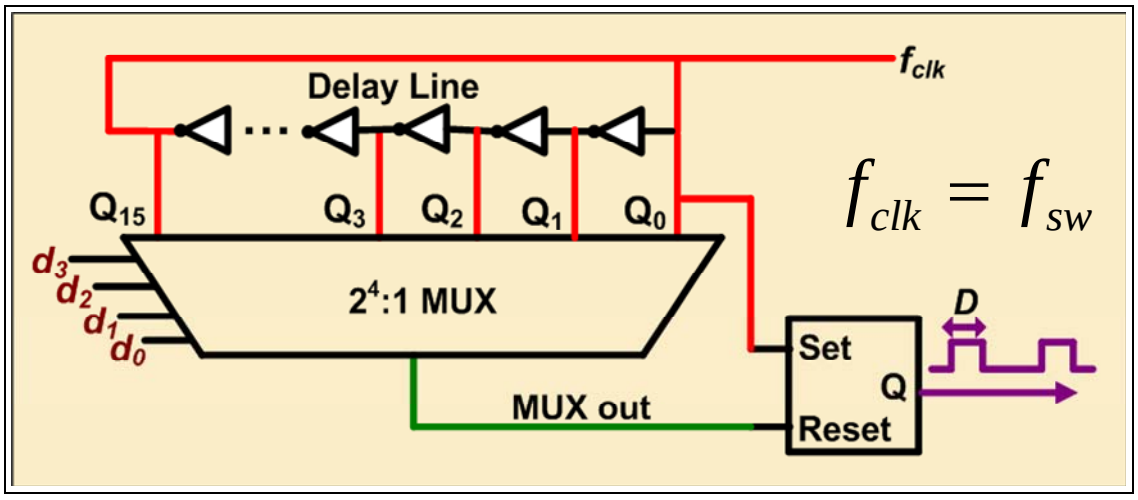


Figure 2.5 Delay Line DPWM Structure (Source [44])

Hybrid approach: A combined strategy which uses both the counter comparator and the delay line as a compromise between the power consumption and the area. The delay line is configured as a ring oscillator which feeds the clock of the counter, thus the delays should be adjusted so that the total delay time provides for both the system switching frequency and the clock frequency [43].

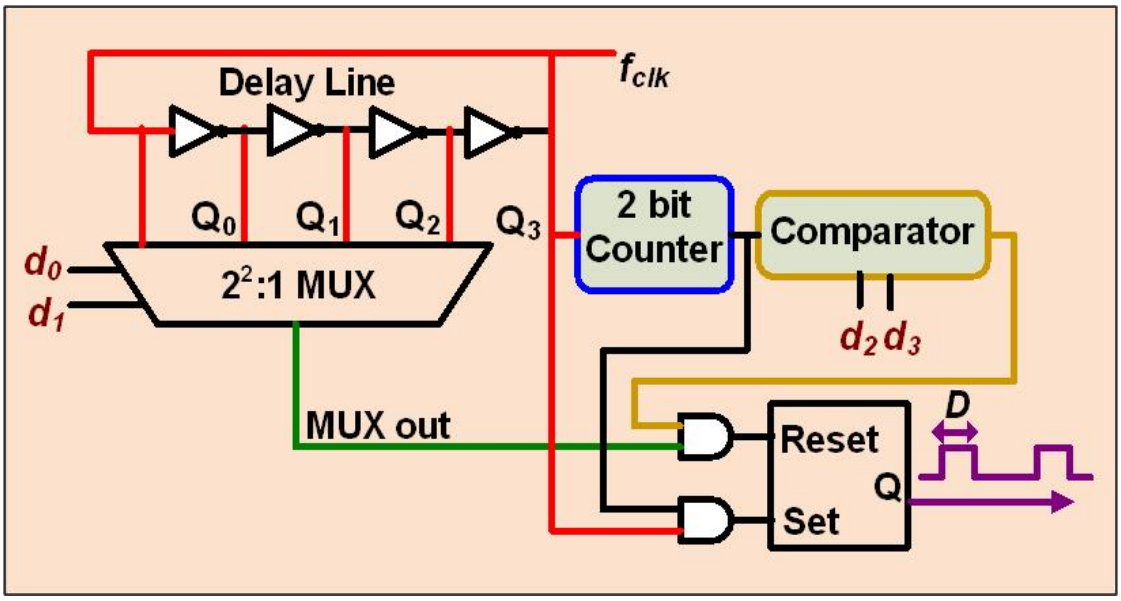


Figure 2.6 Hybrid DPWM Structure with 4 bit Resolution (Source [43])

Segmented delay line architecture: This technique is a fragmented version of the delay line which, ultimately, will result in a smaller area compared to the delay line–based DPWM [45]. Unlike the delay line architecture where the DPWM resolution (N_{DPWM}) requires $2^{N_{DPWM}}$ delay elements forming one line and one $2^{N_{DPWM}} \times 1$ multiplexer; the N_{DPWM} bits can be segmented into groups of smaller delay lines (N_{DPWM_seg}) with a smaller multiplexer for each line instead of one big multiplexer. 6 bit DPWM ($N_{DPWM} = 6$)can be segmented to three 2

bit delay lines $\left(N_{DPWM\_seg} = 2\right)$, each has 4 delay elements $(2^{N_{DPWM\_seg}} = 2^2 = 4)$ and a 4x1 multiplexer as shown in Figure 2.6, which will result is a smaller area compared to the delay line based DPWM which will need $(2^{N_{DPWM}} = 2^6 = 64)$ delay elements and one 64x1 multiplexer [45].

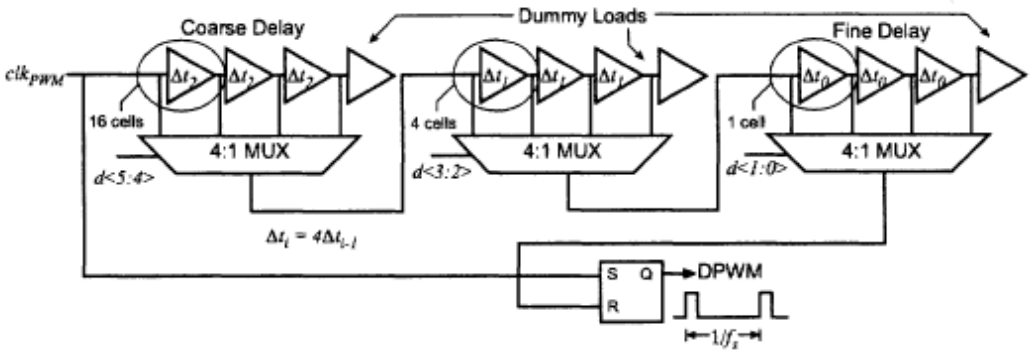


Figure 2.7 A Segmented 6 bit DPWM (Source [45]).

Dithering is another method for increasing the resolution of the DPWM via implementing a lower resolution but effectively getting a higher resolution. This technique can be is accomplished by alternates the duty cycle between two values and the average is taken which can increase the resolution without increasing the clock frequency. Nevertheless, it is subject to EMI due to the occurrence of sub harmonics at frequencies lower than the switching frequency [17, 28].

Sigma Delta Modulation: shown in Figure 2.7, was previously introduced in the analog world replacing the analog PWM, which is a natural source of EMI, by a single bit sigma delta modulator. The inherent noise in the PWM disturbs the DPWM values and may cause

the duty cycle values to be mismatched to any of the DPWM levels, shaping the noise by reducing the low frequency noise and increasing the high frequency noise which will eventually be filtered out by the system's LC filter help match all duty cycle values to DPWM levels without additional quantization. The work in [47] show an effective increase in the DPWM resolution via preprocessing the duty cycle values prior to DPWM application through a unity magnitude and delay free multi bit digital sigma delta modulator, in order to decrease the quantization noise and shift them from low frequency levels into high frequency levels which will then be filtered out by the converter's filter and consequently increase the DPWM resolution without destabilizing the system since the transfer function of a sigma delta pre modulator will not affect pole placement for it has a magnitude of one and no delay.

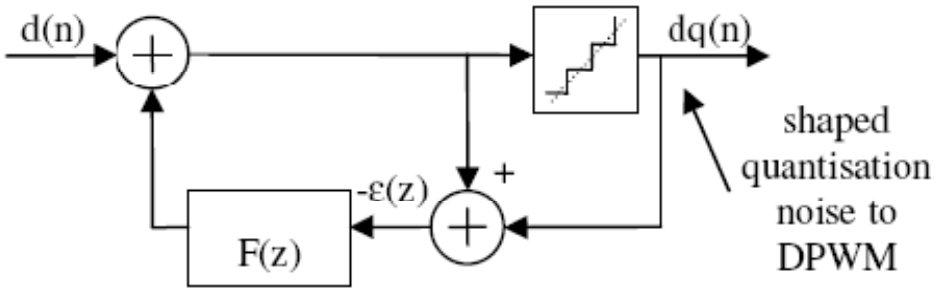


Figure 2.8 Sigma Delta Modulator Block Diagram (Source [47]).

Delay Locked Loop (DLL): Another attractive architecture used particularly for low switching frequencies is the DLL–DPWM. It is a hybrid architecture where the synchronous part is a counter–based DPWM while the asynchronous part comes from the FPGA internal resources with a trade–off between the resolution and linearity. Recent work utilizes the

available DLL blocks on the FPGA, however, the high number of bits used to implement the counter component in this architecture, makes it unsuitable for high switching frequency operation [46, 118].

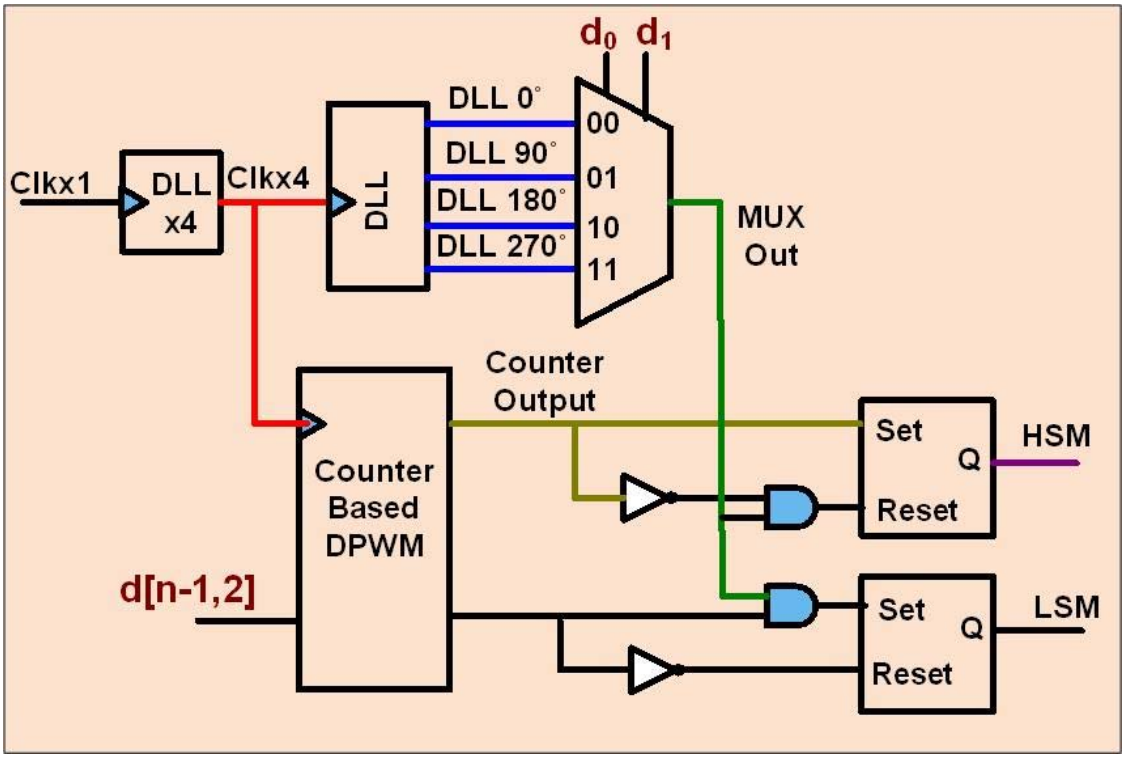


Figure 2.9 DLL DPWM Architecture (Source [118]).

CHAPTER 3:
WINDOW–MASKED SEGMENTED DIGITAL CLOCK MANAGER–FPGA BASED DPWM TECHNIQUE

3.1 Introduction

This chapter presents a new Digital Pulse Width Modulator (DPWM) architecture for Field Programmable Gate Array (FPGA) based systems. The design of the proposed DPWM architecture is based on fully utilizing the Digital Clock Manager (DCM) resources available on new FPGA boards. Furthermore, this architecture also applies a window–mask to limit the DCM operation to only a portion of the switching period in order to decrease power dissipation. This proposed digital modulator technique allows for higher DPWM resolution with lower power consumption, the primary barrier to high switching frequency operation. The presented technique relies on power–optimized resources already existing on new FPGAs, and benefits from the inherit phase shifting properties of the DCM blocks which help in simplifying the duty cycle generation. The architecture can be applied to achieve different numbers of bits for high or low DPWM resolution designed for different DC–DC applications. The suggested architecture is first simulated, implemented, and experimentally verified on a Virtex–4 FPGA board.

3.2 Digital Implementation Platforms: Why FPGA?

In order to obtain high power density and high dynamic performance, some present converters are pushed to higher switching frequencies beyond MHz range, which needs high resolution DPWM and high computation throughput. The commercialized DSPs and ASICs

cannot meet all these demands. However, FPGAs with re–configurability and hardware parallelism offer the potential solution to control these kinds of converters. Meanwhile, the control hardware configured in FPGA using Hardware Description Language (HDL) can be easily integrated into DSPs or ASICs with support of foundry.

3.2.1 DSP versus FPGA

The two most common programmable platforms used to implement digital controllers are: digital signal processors (DSP) and FPGAs [8 – 13, 117 – 129]. DSPs, which are special form of microcontrollers, have been used to implement sophisticated control laws such as fuzzy control [73] and renewable energy control schemes [73].

Recently, the use of FPGAs which are a structure of highly configurable type of hardware, have been growing faster and more popular than DSPs primarily due to three main reasons:

1. The FPGA processor capabilities measured in Million Instructions per Second (MIPS) surpass DSPs, which entails faster program execution time and decreased processing delays, elevating one of the drawbacks of DSPs based digital systems [73, 117].
2. Enhanced hardware reliability and maintainability of FPGAs when compared to DSPs, discussed thoroughly in [117].
3. FPGA boards have evolved in system resources in terms of clock frequencies and memory capabilities as compared to DSPs [29].

3.2.2 ASIC versus FPGA

Compared to ASICs, FPGAs are more popular due to the following:

1. Faster time–to–market since no layout or manufacturing steps are required compared to the full design, verification and manufacturing processes needed for full custom ASICs [110]
2. Free from NRE (Non Recurring Expenses) which are ASICs related issues making them design costly [110].
3. Simpler design process eliminating complicated as well as time consuming design flow steps required in ASICs such as floor–planning, equivalency checking and circuit verification [110].
4. The most important advantage of FPGA over ASICs is their field reprogram–ability which can also be done remotely [110].

ASICs are the best platform for a full custom design, unlike the FPGA which operates more unneeded circuitries. Nevertheless, this is time consuming and cost justified for high volume production.

It was taken that FPGAs were selected for low speed designs compared to the fast clock ASICs, however currently FPGAs are available with high internal speed clocking [110].

Literature has reported the use of FPGAs in digital converters operating in low switching frequencies and high power levels [29, 117 – 129]. Other efforts investigated the suitability of FPGAs for higher frequencies with moderate power levels [73] and some research efforts have shown the use of FPGA in low power converters without pushing frequency into higher ranges [117 – 129]. This work aims at using the full capabilities and resources of FPGA boards to implement digital controllers for low–power, high–frequency converters.

The DPWM architectures presented in this work propose novel structures aiming to improve the resolution by cascading DCM blocks available on almost all FPGA boards in order to generate high–resolution pulses. Since the DCMs are commonly available in most of today's FPGAs, the proposed structure without introducing any pure delay in PWM update is more universal for FPGAs compared to [122] in which a DPWM architecture is presented to adopt a fine phase shift technique which can shift the input clock in steps of 1/256th of the clock period to generate the output clock by using delay taps, a unique feature is solely offered in the family of Spartan–3 from Xilinx. With this technique, very high resolution DPWM can be obtained. However during transient state, the duty cycle would change greatly. But the proposed structure in [122] has a at least 80–input clock delay to update the new PWM through variable phase shifter controller, which will deteriorate the dynamic performance by introducing a pure delay unit, especially in converters with high switching frequency.

This chapter proposes a new DPWM technique, which utilizes the Digital Clock Manager (DCM) capabilities supported by the FPGA resources. It is a hybrid approach, combining the

linear counter–comparator and the FPGA on–board DCM resources, offering reduced external clock frequency and thus, allowing high switching frequency operation.

3.3 FPGA resources: Digital Clock Manager Circuit

3.3.1 DCM Capabilities, Features and Charactarestics

FPGA boards continue to grow in terms of size and capabilities, such capabilities include the Digital Clock Manager (DCM) resources [111]. DCM is a clock management system that enables input clock frequency duplication, multiplication and division in addition to generating four different phase shifting clock versions: 0°, 90°, 180° and 270°. Xilinx–Virtex–4 devices provide many on chip DCM circuits which offer zero propagation delay, lower jitter and better phase–shifting resolution [111].

The generated phase shifted clock versions from the DCM can be viewed as delayed duplicates of the input clock maintaining the same 0.5/0.5 duty cycle ON–time/OFF–time relationship of the input clock (in other words, phase shifts have an ON–time interval equals to the OFF–time and both are half the clocking period of the input clock) as shown in Figure 3.1.

In Figure 3.1, **Clk in** represents the input clock to the DCM block where it is processed to produce four different versions of clock phase shifts or delays designated: **Clk_shifted 0°**, **Clk_shifted 90°, Clk_shifted 180°** and **Clk_shifted 270°**. Additionally, the DCM block

provides clocking signals of double and four times the input clock, assigned **Clk2x** and **Clk4x**, along with their inverted signals, labeled **Clk2x_180°** and **Clk4x_180°,** respectively.

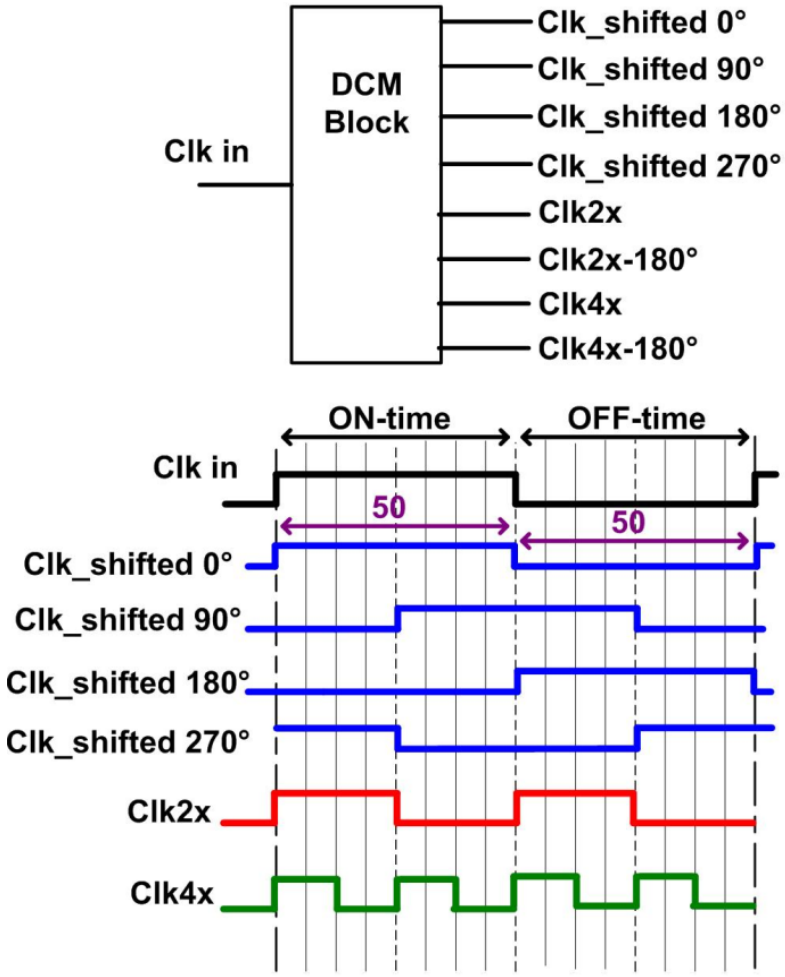


Figure 3.1 Possible outputs by the Digital Clock Manager

As illustrated by Figure 3.1, the phase shifted versions of the input clock have the corrected duty cycle, (corrected duty cycle in this context refers to a duty cycle locked at 50% with 0.5/0.5 ON–time/OFF–time). Through analysis and examination of the DCM operation it can be determined that, in order to take full advantage of the DCM modules, the same phase

shifts are necessary to be generated with different ON–time/OFF–time relationship other than the corrected 50% duty cycle. It will be shown that two DCM blocks, designated in this work as DCM_¼ and DCM_½ blocks, can be used to meet the desired functionality as shown in Figure 3.2, where the outputs of DCM_¼ will be locked at (1/4) x 0.5 = 0.125 duty cycle. In other words, DCM_¼ will generate ON–time/OFF–time relationship with 0.125/0.875 duty ratio. In the same way, the outputs from DCM_½ will be locked at (1/2) x 0.5 = 0.25 duty cycle, with ON–time/OFF–time relationship of 0.25/0.75 duty ratio. Now, in order for the delayed waveform generated from both DCM_¼ and DCM_½ to be at the same phase shifts locations of delays 0°, 90°, 180° and 270° as the original DCM shown in Figure 3.1, the delayed waveforms must go through a bank of AND gates that uses both the true and the inverted forms of **Clk2x** and **Clk4x** previously generated from the original DCM block as shown in Figure 3.2.

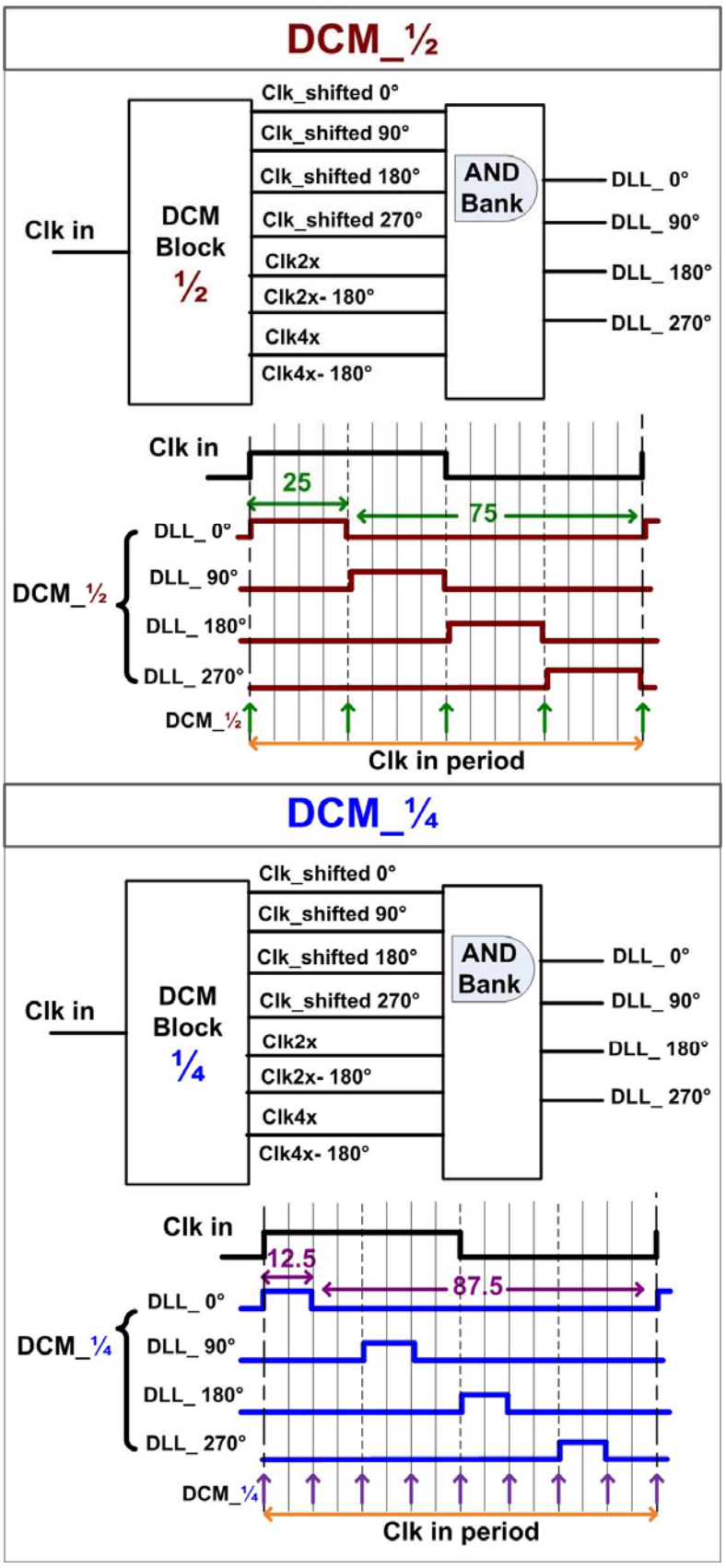


Figure 3.2 DCM_½ and DCM_¼ Block Signals

As stated previously, one of the limitations of digital control is its finite resolution, which implies that not all duty cycle values can be generated but only limited discrete values ranging from 0 to 1 are possible. It has been the objective of research to increase the resolution of DPWM in order to enhance the steady–state performance of any digital system.

The resolution can be measured as either the number of bits expressing the duty cycle value in binary representation (base 2) or it can be defined as the minimum increment in ON–time step between two successive duty cycle values as depicted in Figure 3.3.

Note that (base 2) is written as xb' where x corresponds to the number of bits represented in binary b', for example, 3 in decimal is written in 2 bit binary value as $2b'11$.

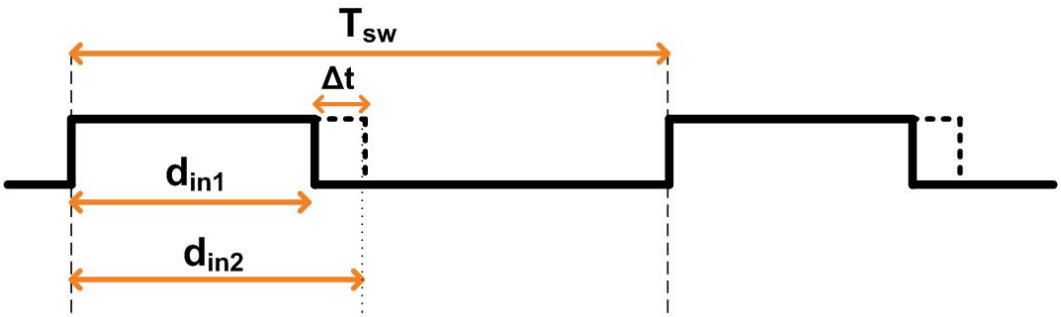


Figure 3.3 DPWM Resolution illustrated

From Figure 3.3, it is shown that the resolution can be calculated using two successive duty cycle values ($d_{in1}\ and\ d_{in2}$) and the minimum increment in ON–time step (Δt) in one switching period denoted by T_{sw}, as expressed in Equation (3.1)

$$\Delta d = d_{in2} - d_{in1} = \frac{t_{on2}}{T_{sw}} - \frac{t_{on1}}{T_{sw}} = \frac{t_{on2} - t_{on1}}{T_{sw}} = \frac{\Delta t}{T_{sw}} \qquad (3.1)$$

Where smaller Δt between two successive duty cycle values ($d_{in1}\ and\ d_{in2}$) means higher resolution and thus enhanced performance.

Now back to DCM blocks and Figure 3.2, it can be noted that different instances can be accessed within one **Clk in** period. This will enable a reduced Δt (increasing the resolution by four times) when DCM_½ is used compared to the original DCM block. In other words, DCM_½ generates only four digital values for the duty cycle in one **Clk in** period whereas, DCM_¼ covers one **Clk in** period in eight values of the duty cycle between 0 and 1 as illustrated in Figure 3.4.

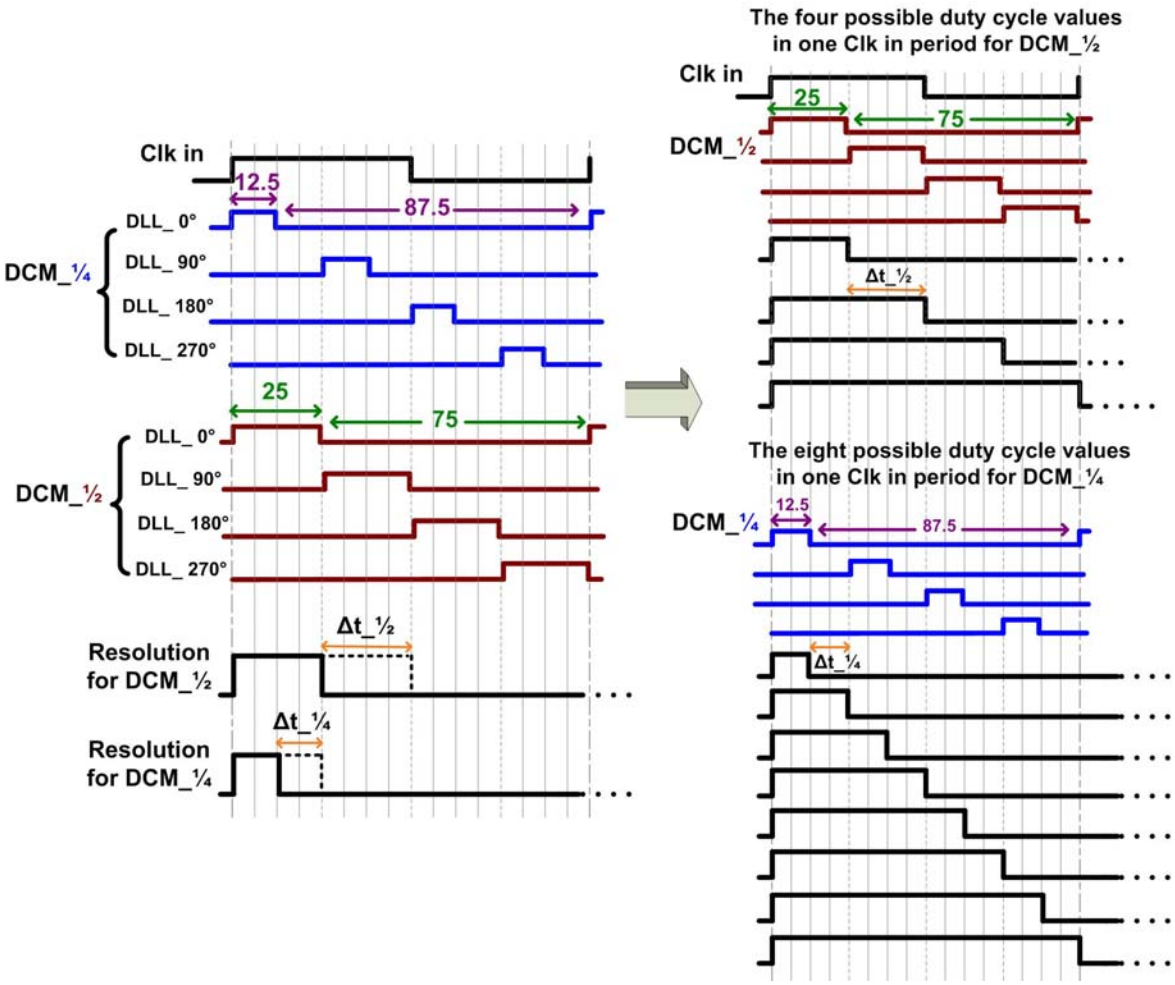


Figure 3.4 Resolution increase achieved from DCM_½ and DCM_¼

Figure 3.4, shows that $\Delta t\_{}^{1}/_{4}$ is less than $\Delta t\_{}^{1}/_{2}$ which means that the resolution using DCM_¼ is higher than that when DCM_½ is used. Moreover, higher resolution guarantees better performance since it allows for more duty cycle values in one clocking period as illustrated in Figure 3.4. Where there is only four possible duty cycle values using DCM_½ compared to eight duty cycle values obtained when DCM_¼ is used. This DCM characteristic offers increased resolution and yet maintaining the same input clock without the need for a higher clock frequency, the main cause of deteriorated power consumption from which previous DPWM architectures suffer.

Another attractive feature of DCM blocks is the ability to cascade them. As shown in Figure 3.5; one DCM module feeds the next to further increase the resolution while using available power–optimized FPGA resources.

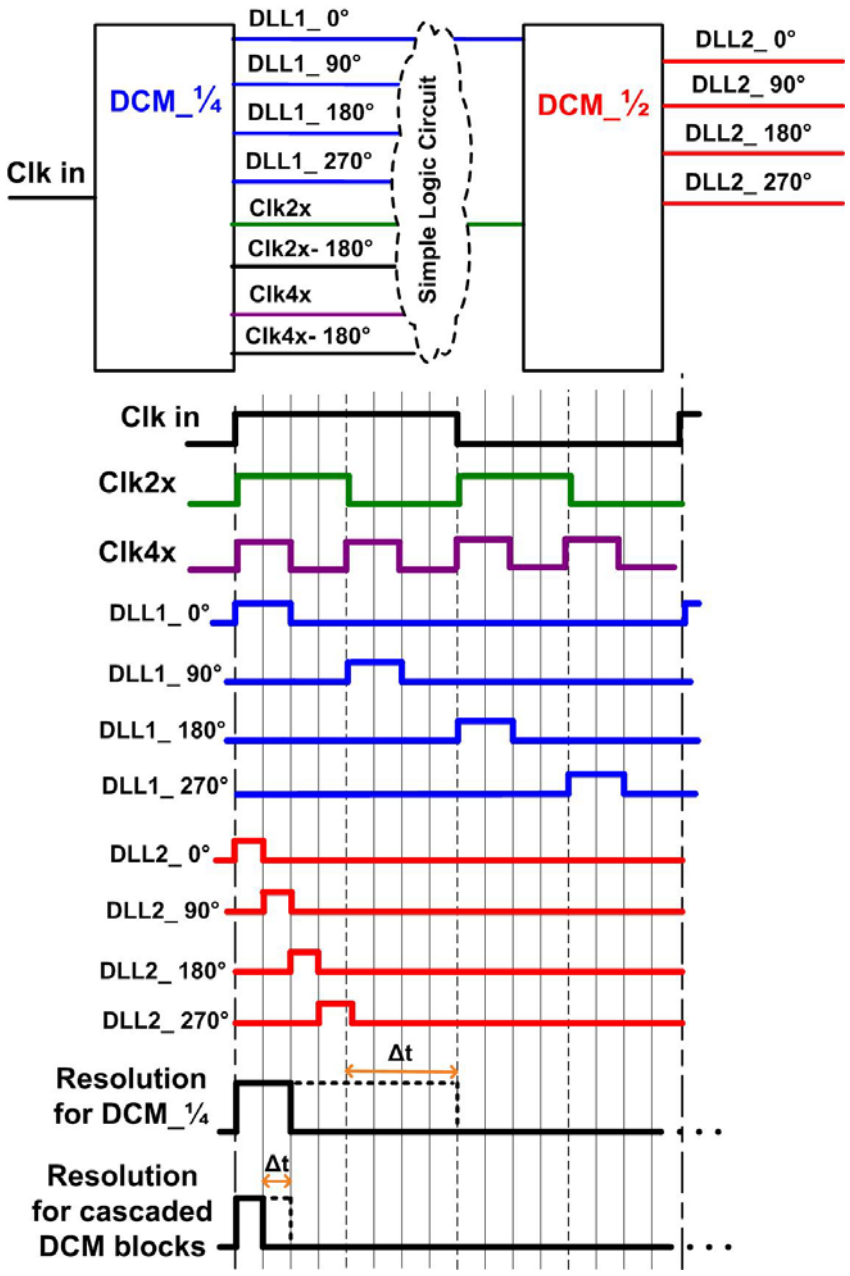


Figure 3.5 Cascading DCM blocks ½ and ¼

Figure 3.5 illustrates the operation of two DCM blocks in series, the input clock labeled **Clk in**, propagates in zero delay through DCM_½, and the output of the first DCM block corresponds to the first set of phase shift versions (DLL1_0°, DLL1_90°, DLL1_180° and DLL1_270°) together with double the input frequency, **Clkx2**, at which the second DCM block (DCM_¼) is operated, where further phase shifted signals of the clock are produced, DLL2_0°, DLL2_90°, DLL2_180° and DLL2_270°. As observed from Figure 3.5, the resolution is now increased by 16 times without the need of operating the whole system at clocking frequency 16 times higher than the original **Clk in**. It has been thus far shown that one DCM block can be used to increase the resolution by either four times (DCM_½) or eight times (DCM_¼) in addition to using two DCM blocks in series increases the resolution by 16 times. Therefore, the feature of cascading DCM blocks with different duty cycle ratios of the phase shifted clocks will increase the resolution without operating the whole system at higher clocking ranges. This will ultimately enhance the resolution, minimize the power dissipation, and pave the way to generating PWM signals with higher switching frequencies. The design of the proposed DPWM is basically a segmentation of the available power optimized DCM blocks to increase the effective resolution of the system.

3.3.2 DLL versus DCM

The Segmented DCM architecture proposed in this chapter relies on the DCM blocks available on FPGA boards as presented in the previous discussion. This new proposed approach is a hybrid technique, similar in concept to the Hybrid DPWM presented in [46] and the DLL based DPWM in [118], where the overall resolution of the DPWM is divided among two blocks: a linear counter–comparator part which employs the most significant bits (MSB)

of the DPWM resolution while the second block realizes the least significant bits (LSB) through a delay line implementation. The main difference between:

(1) The Hybrid DPWM of [46], (2) The DLL based DPWM in [118] and, (3) The DCM proposed architecture, is the means by which the second block is implemented.

Although the delay cell in [46] can achieve high resolution using custom design gate delay instead of utilizing any FPGA internal resources, this implementation technique introduces delays and deteriorates linearity due to device matching issues which makes it difficult to transplant the design from one FPGA family to another FPGA or ASICs due to different delay features in each chip, in addition to requiring many gates which increases the design area as well as power consumption making it unsuitable for high switching operation.

In comparison, both the DLL in [118] and the proposed DCM architecture benefit from FPGA on board resources (DLL and DCM circuits respectively) to implement the delay line.

Unlike the design presented in [118] where the synchronous block counter–comparator component of the DPWM uses the most significant bits (MSB) of the duty cycle, $d[n-1,2]$, and only the two least significant bits (LSB), $d[1,0]$, are used to select among one of four phase shifted clock versions generated by the FPGA's DLL. Where $d[n]$ represents the duty cycle command coming from the compensator and n corresponds to the number of bits comprising the resolution by which the duty cycle is expressed. ($d[n-1,2]$, is a notation used throughout this text to refer to the resolution of the DPWM, where n is the number of bits and the square parenthesis indicate bit selection. For example a 6–bit DPWM entails that $n=6$ and the total resolution can be expressed as $d[5,0]$ from the sixth bit $d[5]$ representing

the most significant bit to the first bit $d[0]$ as the least significant bit in the 6–bit string expressed as $6b'000000$ the DLL DPWM is implemented with a counter–comparator using the 4 most significant bits $d[n-1,2] = d[5,2]$, counting from $0 \Rightarrow 4b'0000$ up to $2^4 - 1 = 15 \Rightarrow 4b'1111$ whereas, the two least significant bits $d[1,0]$ are used as MUX select as detailed later in this chapter).

Referring to the DLL DPWM architecture presented in [118], for a given switching frequency, f_{sw}, and a targeted DPWM resolution, N_{DPWM}, the clock frequency, f_{clk}, can be as high as calculated from Equation (3.2), where N_{clk} is the number of bits implementing the counter block. In the case of the DLL architecture presented in [118], the clock resolution needed is $N_{clk} = N_{DPWM} - 2$, which dramatically increases the power consumption of a high resolution DPWM [44 – 45] not to mention driving unrealistic requirements on the magnitude of the clock frequency.

$$f_{clk} = 2^{N_{clk}} \times f_{sw} \qquad (3.2)$$

The proposed Segmented DCM is an enhanced version of the conventional DLL DPWM, where most of the DPWM resolution bits are achieved by the DCM blocks and the remaining bits are used to implement the counter–comparator technique. As an example, for $N_{DPWM} = 6$, the DPWM is implemented by the conventional DLL approach presented in [118] as a 4–bit counter and a 2–bit DCM Digital PWM, resulting in a required clock frequency 16 times higher than the switching frequency as calculated using Equation (3.2) where $N_{clk} = N_{DPWM} - 2 = 6 - 2 = 4$. Compared to the new Segmented DCM proposed in this work;

where the same 6–bit DPWM resolution would be implemented as a 2–bit counter and a 4–bit DCM using two cascaded DCM blocks, as shown in Figure 3.6.

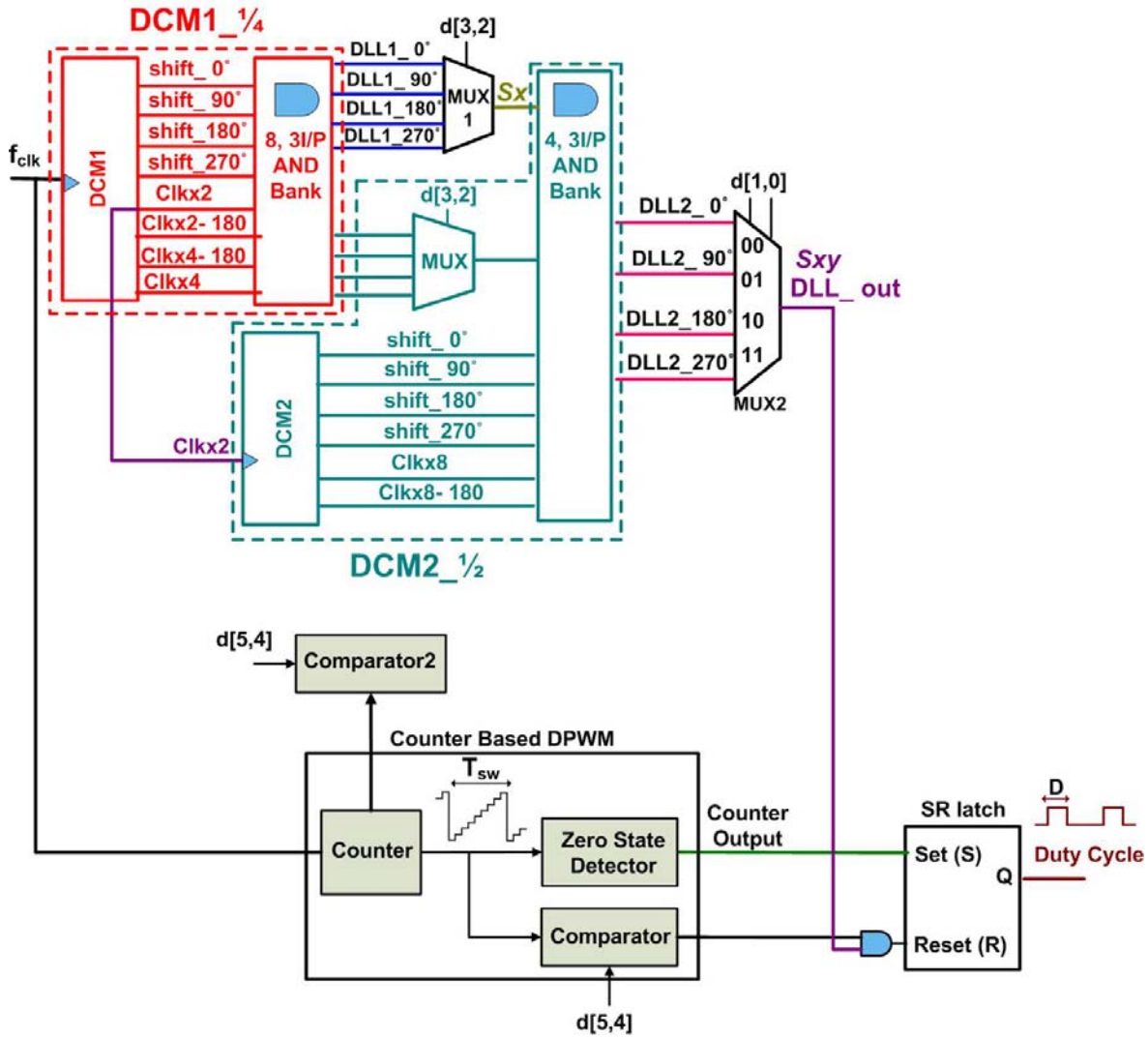


Figure 3.6 6–bit Segmented DCM DPWM implemented as a 2–bit counter & 4–bit DCM

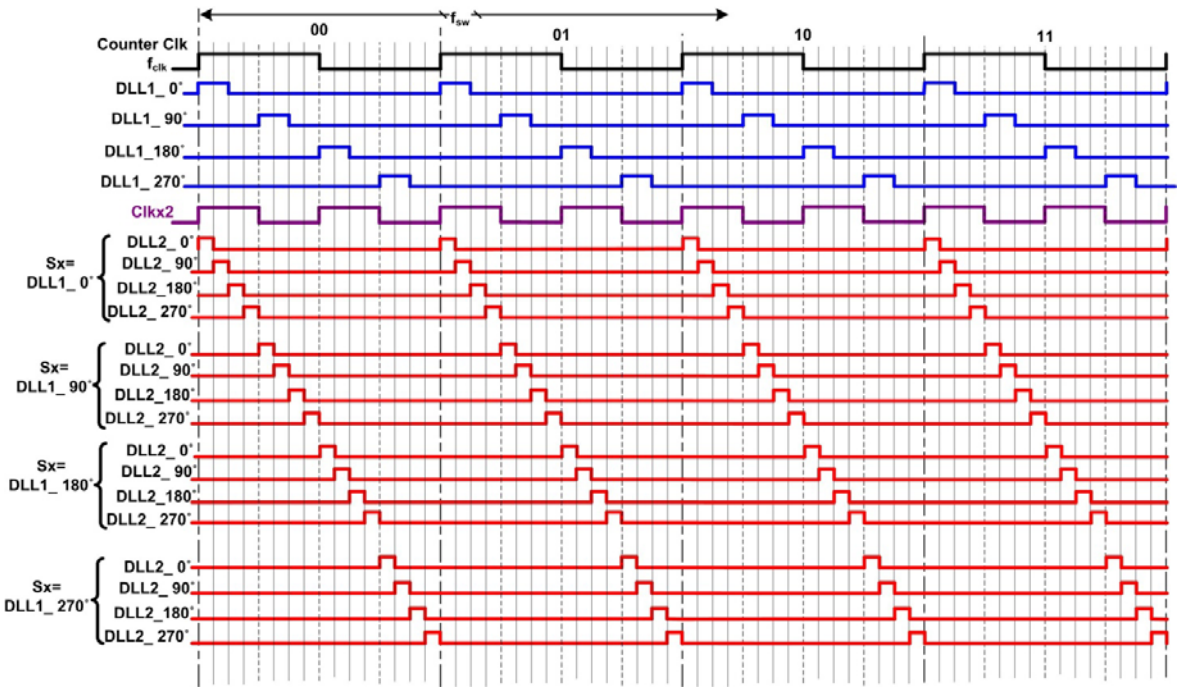


Figure 3.7 Operational Waveforms of 6–bit Segmented DCM–based DPWM

Since this Segmented DCM architecture uses 2 bits for the counter then the required clock frequency, f_{clk}, as calculated using Equation (3.2) with $N_{clk} = 2$ is only 4 times the switching frequency compared to 16 times needed by the conventional DLL DPWM, presented in [118]. The savings in the oscillator clock frequency is more clearly noticeable and appreciated when higher DPWM resolution is required. For example, a 12–bit DPWM system, $N_{DPWM} = 12$, operating at few hundreds of kHz switching frequency is not practically realizable using the DLL approach discussed in [118]. This is due to the impractically high clock frequency needed; reaching 1024 times the switching frequency where the clock frequency needed can be calculated using Equation (3.2) to be:

$$f_{clk} = 2^{N_{clk}} \times f_{sw} = 2^{N_{DPWM}-2} \times f_{sw} = 2^{10} \times f_{sw} = 1024 \times f_{sw} \qquad (3.3)$$

Equation (3.3) states that the needed clock to operate a 12–bit DPWM is 1024 times higher than the desired switching frequency. Which means a clock frequency of 102.4MHz is required to achieve a 12 bit DPWM operating at 100 kHz switching frequency. Whereas, the same 100 kHz and 12–bit DPWM system can be realized with a 25.6 MHz clock frequency using the proposed concept of Segmented DCM architecture and two DCM blocks since in this case $N_{clk} = 8$,. The savings in clock frequency achieved via segmented DCM is reflected to less power dissipation.

FPGA boards provide many DCM blocks and it will be shown that more DCM blocks can be cascaded in the Segmented DCM architecture to further decrease the clocking requirements, as discussed in the experimental verification in Section 3.3 below. Thus, the reduced clock requirements attained using the new Segmented DCM DPWM proposed in this work helps in minimizing the power consumption, as tabulated in Section 3.4, and paves the way to switching at higher frequencies with reduced clock oscillators frequency and higher DWPM resolution, hence better system performance.

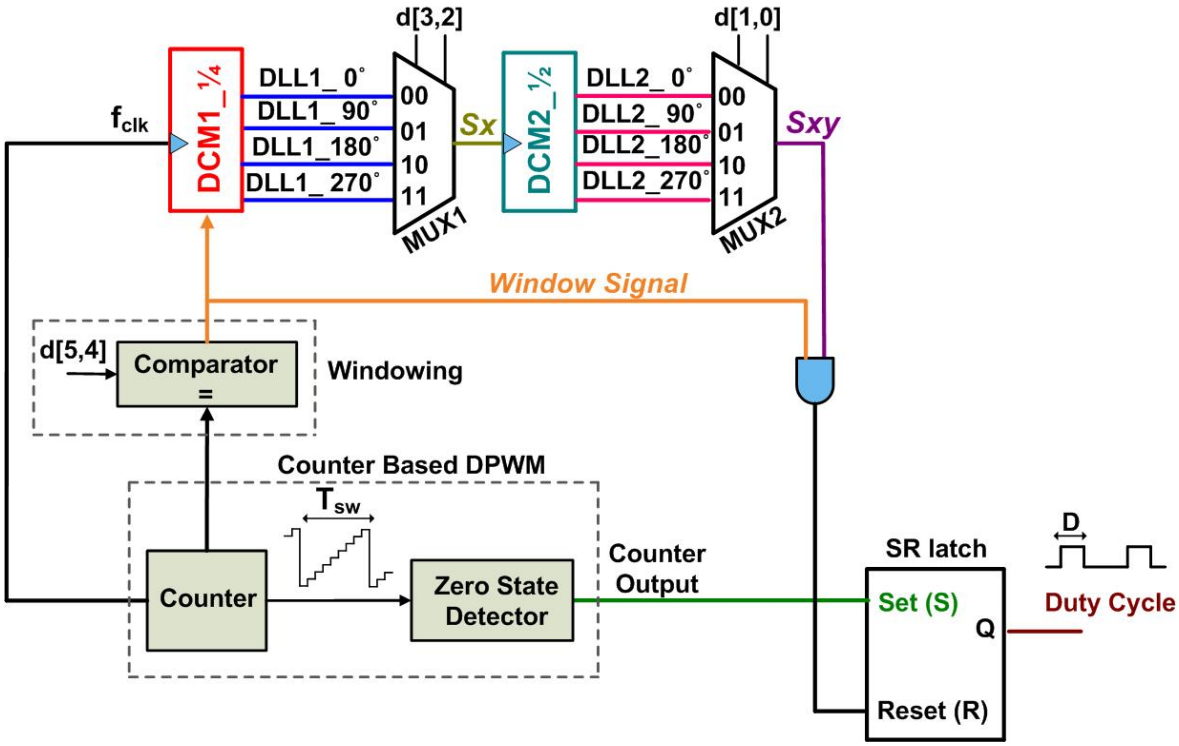
3.3.3 Segmented DCM based–DPWM Operation

To illustrate the operation of the Segmented DCM–based DPWM, the 6–bit DPWM, $d[5,4,3,2,1,0]$ discussed above, will be redesigned using a 2–bit counter and 4–bit coming from two cascaded DCM blocks as shown in Figure 3.5.

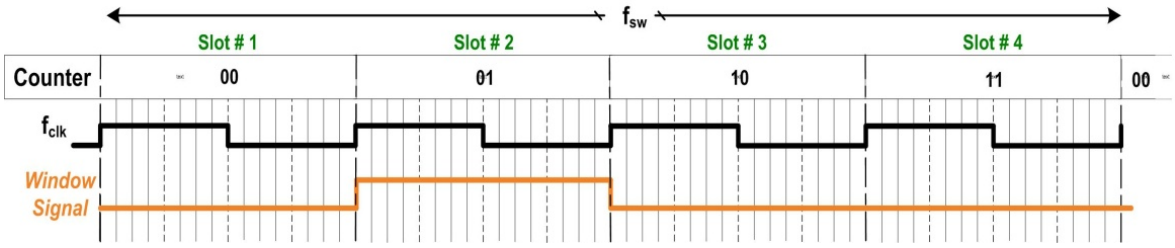
The duty cycle value generated by the compensator will vary from a minimum value of 0, corresponding to the DPWM binary code of $6b'000000$, incrementing in 64 steps, reaching

a maximum of $2^6 - 1 = 63$, matching $6b'111111$. For example, 49% Duty cycle is translated into $63 \times 49/100 = 30.87 \cong 31$, which is equivalent to the DPWM binary value of $d[5,4,3,2,1,0] = 6b'011111$. This 6–bit binary representation of the duty cycle is generated by the compensator and goes into the DPWM block, where, the comparator will be set when the counter matches the 2–bit: $d[5,4] = 2b'01$, and the output of the DCM blocks will be decided by the 4–bits: $d[3,2] = 2b'11$ and $d[1,0] = 2b'11$, as shown in Figure 3.6. The operation of the circuit shown in Figure 3.6 is as follows; the clock frequency from the oscillator f_{clk} goes through DCM1_¼ block. The output of DCM1_¼ is one of four different phase shifted versions of the input clock; DLL1_0°, DLL1_90°, DLL1_180° and DLL1_270° with 0.125/0.875 ON–time/OFF–time relationship, as shown in Figure 3.7. The value of the MUX1 select comes from the compensator duty cycle command, $d[3,2]$ which selects among DCM1_¼ output versions and the output of MUX1, ***Sx***, is then further phase shifted by DCM2_½ block, as depicted in Figure 3.7.

The system block diagram of Figure 3.6 can be simplified as illustrated in Figure 3.8(a), where DCM1 block and the bank of eight 3–input AND gates are grouped in one block labeled DCM1_¼ and similarly, DCM2 with a 4x1 Multiplexer (MUX) and the bank of 3–input AND gates are assembled in one block labeled DCM2_½ as shown in Figure 3.8(a). A new windowing feature is added to the circuit previously shown in Figure 3.6 for the purpose of eliminating the propagation of the generated phase shifts through the whole switching cycle as shown in Figure 3.7 and limits it to a moving window set by the comparator.



(a)



(b)

Figure 3.8 (a) Simplified circuit of 6–bit Window–Segmented DCM Digital PWM, (b) Windowing Signal

The operation of the proposed Window–Segmented DCM–based DPWM architecture of Figure 3.8(a) is as follows: First, the counter ramps up from zero till it reaches $2^{N_{clk}} - 1$ at every rising edge of the clock f_{clk}, making one counting cycle (the counting cycle is the time

required for the counter to count up starting from zero, at the beginning of the cycle, to $2^{N_{clk}} - 1$ at the end of the cycle, i.e. one counting cycle for the counter makes up one switching period for the converter, $T_{sw} = \frac{1}{f_{sw}}$. In this case, the counter cycle starts the sequence from 0 till $2^{N_{clk}} - 1 = 2^2 - 1 = 3$) as illustrated in Figure 3.8(b). In other words, one switching period is composed of $2^{N_{clk}}$ slots. As Figure 3.8(b) shows, a 2 bit counter divides one switching cycle f_{sw} into four slots.

The comparator compares between the counter value and the duty cycle command coming from the compensator $d[5,4]$. The output of the comparator sets the Window Signal high when the count value matches the duty cycle $d[5,4]$. The generated window signal goes through DCM1_¼ block. The output of DCM1_¼ is one of four different window phase shifted versions of the input clock; DLL1_0°, DLL1_90°, DLL1_180° and DLL1_270° with 0.125/0.875 ON–time/OFF–time relationship, as shown in Figure 3.9. The value of MUX1 select coming from the compensator duty cycle command, $d[3,2]$, selects among these DCM1_¼ output versions and the output of MUX1, $\boldsymbol{Sx}$, is then further phase shifted by DCM2_½ block. . The windowing feature added to this proposed architecture confines the operation of all high frequency DCM blocks to only one slot of the switching period according to the value of the comparator bits as illustrated in Figures 3.8(a) and 3.8(b) .

Therefore, with two cascaded DCM blocks, the maximal clock frequency from DCM2_½ is twice that from DLL presented in [118]. However, this high frequency clock is only confined to only one slot ($1/\ 2^{N_{clk}}$) of the switching period for DCM2_½ and the four 3I/P AND Bank which eventually contribute to the power efficiency compared to almost all other FPGA

based DPWM architectures. Taking into consideration that when using the same system input clock for [118] and the proposed architecture, it is noted that no clock multiplication is required for neither the counter comparator nor the first DCM in the proposed architecture and only twice the input clock operates the second DCM block which is also confined to a fraction of the switching period. Whereas, the DLL block and the counter comparator part in [118] operate at a frequency 4 times higher than the input clock.

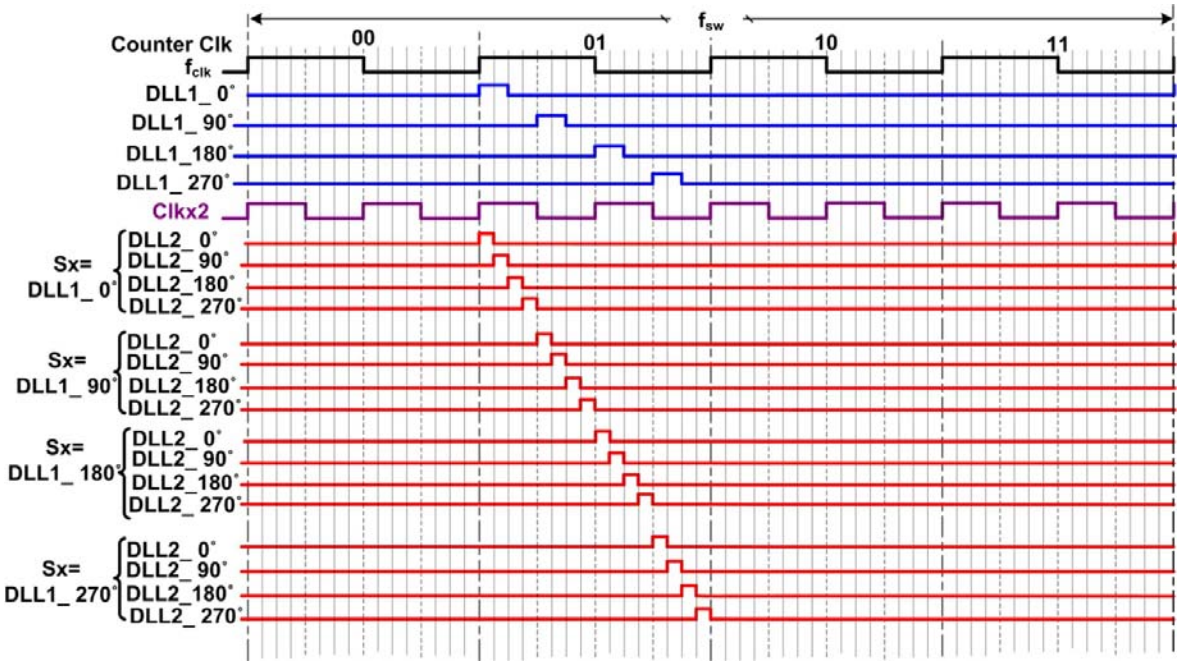


Figure 3.9 Operational Waveforms of 6–bit Window Segmented DCM–based DPWM for $d[5,4] = 2b'01$

Without further ado, another important distinction between the proposed architecture and the DLL based DPWM in [118] is the fact that the counter comparator part and the DCM blocks are operated at the same clocking source which means that the SR Latch is Set and Reset using the same clock at the same rising edge of the clock which eliminates any non

linearity aroused in [118] due to using different clocking. In addition, the proposed architecture benefits from the high resolution and high precision phase shifting capabilities of the DCM blocks rather than DLL circuits which determine the linearity of the duty cycle. Therefore, a highly linear duty cycle generation is guaranteed using the accurate DCM circuits which offer zero propagation delay, lower jitter and better phase–shifting resolution within the operating VCO frequency [111], an issue that needed to be addressed in hybrid as well as DLL based DPWM architectures and does not exist in the proposed architecture.

A numerical example will best illustrate the operation of the circuit shown in Figure 3.8(a) as follows; if the duty cycle value coming from the compensator is 42.8% corresponding to $^{27}/_{63}$, which is translated from the compensator output as a duty cycle command $6b'011011$, where, $d[5,4] = 2b'01,\ d[3,2] = 2b'10\ and\ d[1,0] = 2b'11$.

First the counter will count from zero ($2b'00$ in base 2 representation) up to $2^{N_{clk}} - 1 = 2^2 - 1 = 3$ ($2b'11$ in base2 representation) and resumes at every rising edge of f_{clk}. The comparator will then generate a Window Signal each time the counter reaches the value of the duty cycle $d[5,4] = 2b'01$. DCM1_¼ is operated at the f_{clk} frequency and together with the Window Signal will generate the window phase shifts, DLL1_0°, DLL1_90°, DLL1_180° and DLL1_270° as shown in Figure 3.10.

The value of the select is $d[3,2] = 2b'10$ and therefore, MUX1 output (***Sx***) is a 180° phase shifted clock output of DCM1_¼, designated DLL1_180° illustrated in Figure 3.10.

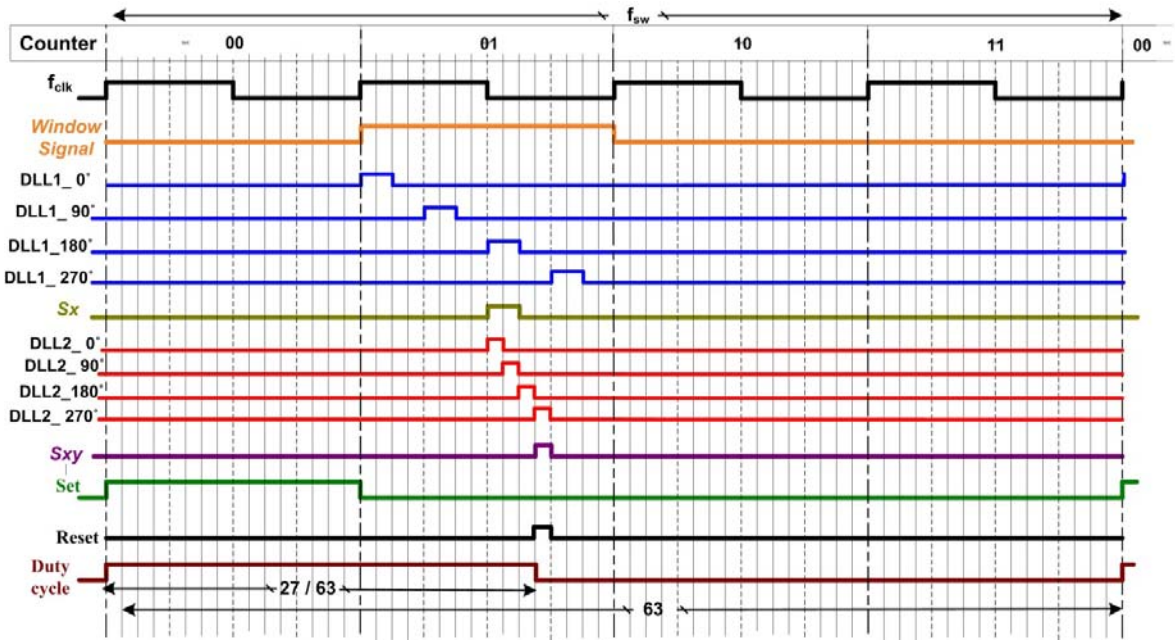


Figure 3.10 Numerical example for a 6–bit Window–Segmented DCM–based DPWM

Sx, will then be further phase shifted using DCM2_½ resulting in DLL2_0°, DLL2_90°, DLL2_180° and DLL2_270°. And MUX2 output (***Sxy***) is a DLL2_270° phase shifted clock output of DCM2_½, since the select is $d[1,0] = 2b'11$, as shown in Figures 3.7 through 3.9.

The SR latch is set high at the beginning of each counting cycle (Zero State detect corresponding to a count value 00 in base 2 representation). On the other hand, the SR latch is reset when both the comparator detects that the counter reaches the value of $d[5,4]$ and the clock is shifted by DCM1_¼ block and further phase shifted by DCM2_½ block. Resetting the SR flip–flop determines the converter duty cycle value, D as verified in Figure 3.10 demonstrating the 42.8% Duty Cycle corresponding to $^{27}/_{63}$. . The whole system is verified via simulation and the results are given in Section 3.3. Whereas Section 3.4 presents the experimental results implementing a 12 bit DPWM using DLL, 2 DCM and 3 DCM blocks.

Figure 3.11 shows the complete and simplified DCM part for a 3DCM based DPWM with the synchronous part of the counter comparator is basically the same as shown in the full and simplified circuit in Figures 3.6 and 3.8(a) respectively.

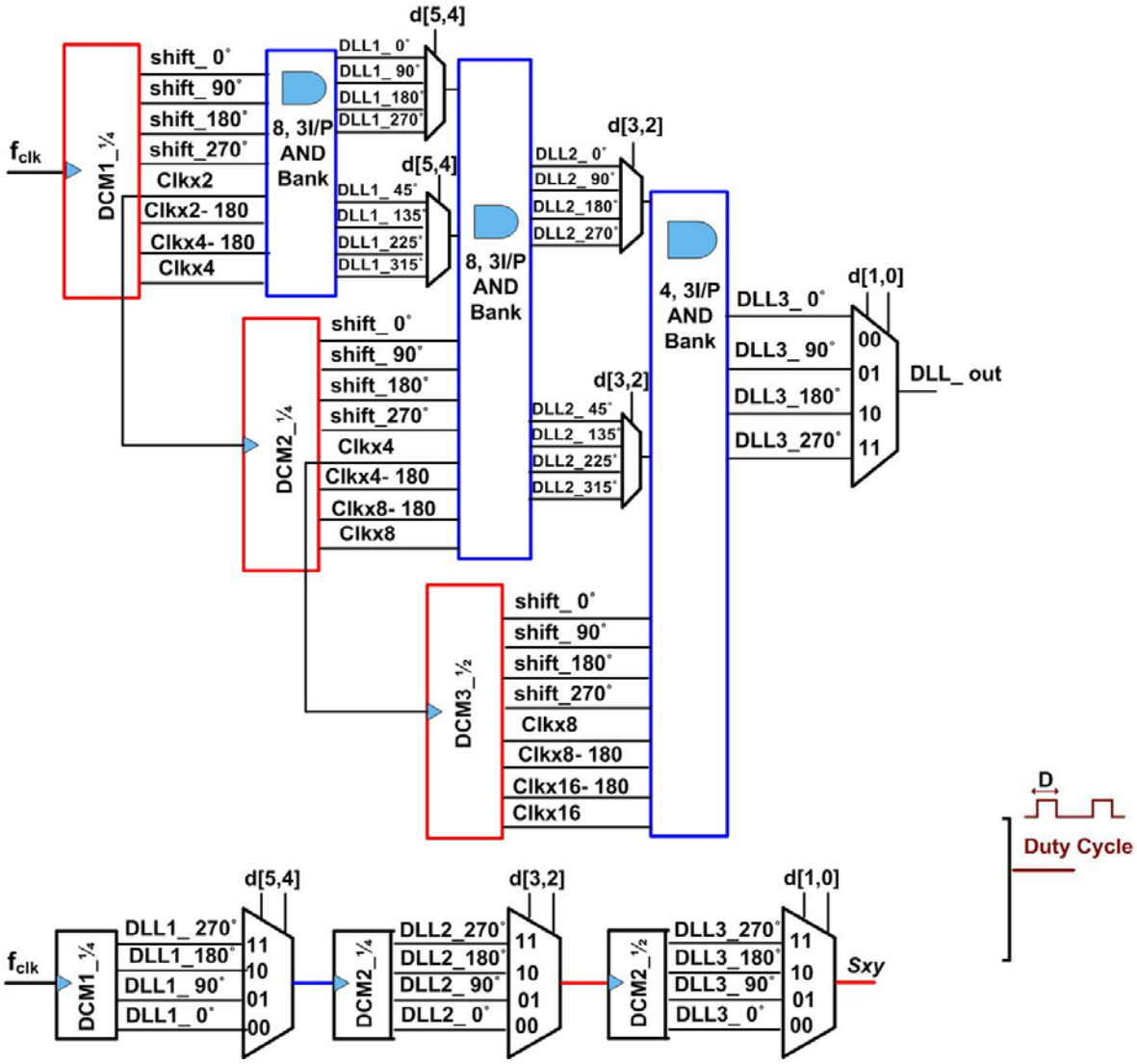


Figure 3.11 The DCM Part of a Window–Segmented DCM– based DPWM implementing 3 DCM blocks

3.3 Simulation Results

To verify the proposed segmented architecture, a behavioral simulation of the proposed Window–Segmented DCM–based DPWM was carried out using Xilinx ISE software prior to hardware implementation. A Verilog code describing the circuit is simulated using a Xilinx simulator environment design tool ISE WebPack 9.2i [112] and various DPWM resolution architectures are tested. Moreover, the Digital Clock Manager Circuit is also validated for design before using it to implement the proposed architecture. First, the DCM block introduced in Figure 3.1 is verified using the available FPGA templates. The simulation results are as shown in Figure 3.12.

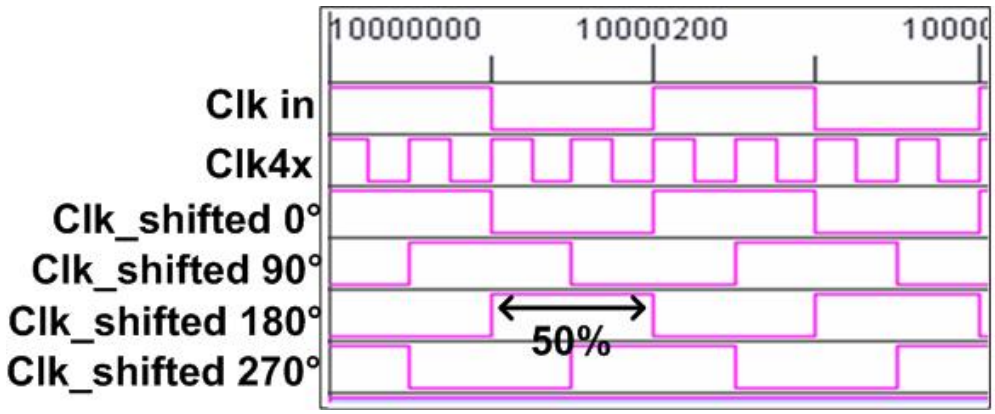


Figure 3.12 DCM Circuit Simulation Results

Figure 3.12 illustrates the operation of the DCM block, where the input clock, **Clk in**, propagates in zero delay [111] to produce the four phase shifted clock signals, **Clk_shifted 0°**, **Clk_shifted 90°, Clk_shifted 180°** and **Clk_shifted 270°** each with 0.5/0.5 corrected duty cycle.

As stated in Section 3.2, a bank of AND gates was added in order to vary the ON–time/OFF–time relationship of the phase shifted clock versions which are produced by the DCM block. Figure 3.13 illustrates the simulation results of the DCM_¼ shown previously in Figure 3.2, where the phase shifted versions of the clock, **DLL_0°**, **DLL_90°, DLL_180°** and **DLL_270°**, are generated with 0.125/0.875 ON–time/ OFF–time durations.

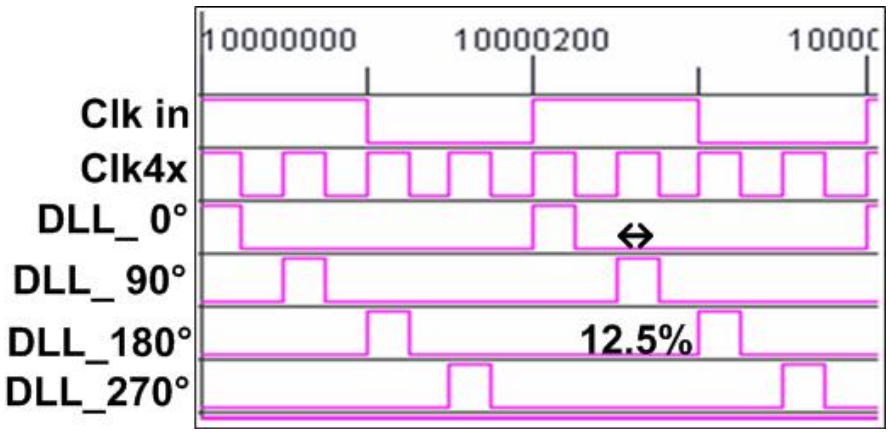


Figure 3.13 DCM_¼ Circuit Simulation Results

Finally, the complete circuit of the 6–bit DWPM of Figure 3.8(a) is simulated for verification and the results of a 50% duty cycle are given in Figure 3.14.

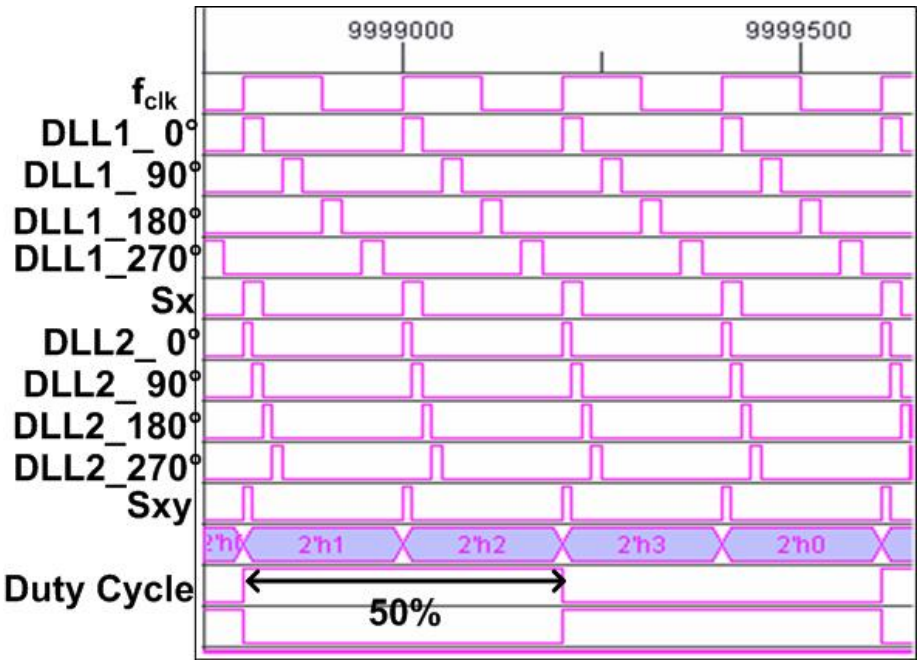


Figure 3.14 6–bit DPWM, 50% Duty Cycle Generation Simulation Results

3.4 Experimental Verification

The simulation results were verified on a Xilinx environment platform and carried out on a Virtex4–board with XC4VSX35 device and FF668 Package. Virtex–4 boards provide up to eight DCM blocks, i.e cascading more DCM blocks is available for a reconfigurable design and further savings in the clocking requirements. In other words, a 12–bit DCM based DPWM architecture can be implemented using one of the combinations for resolution–partitioning as shown in TABLE 3.1.

TABLE 3.1
RESOLUTION PARTITIONING FOR SEGMENTED DCM

Resolution Partitioning for 12 bit DPWM	Counter bits (MSB) = N_{clk}	DCM select bits (LSB)
1DCM–2bits (DLL)	10	2
2DCMs–4bit	8	4
3DCMs–6bit	6	6

Moreover, the duty cycle generation and the corresponding estimated power analysis are also given in this section.

The Xilinx–Virtex 4 board is operated by a 100MHz internal system clock which serves as the oscillator clock for the counter block of the DCM–based DPWM architecture presented here.

For a clock frequency of 100MHz and a 12–bit DPWM resolution, a maximum switching frequency of 24.41 kHz can be achieved by the conventional Counter–Comparator DPWM architecture with utmost linearity. If the same 12–bit DPWM, operating at a 100MHz oscillator, is implemented using the DLL architecture presented in [118], then the maximum possible switching frequency is 97.65 kHz as calculated from Equation (3.2) using the 10 MSB to implement a 10–bits counter resolution and the 2 LSB as the select bits of the MUX in the DLL architecture. Whereas, the same design can be implemented using the proposed Window Segmented DCM DPWM to achieve different switching frequencies according to different reconfigurations as listed in TABLE 3.1. For example, switching frequencies of 390

kHz, 781.25 kHz and 1.56 MHz, can be accomplished by implementing the 12 bit DPWM as: (8–bit counter with 4–bit DCM using 2 DCM blocks) or (7–bit counter with 5–bit DCM using 2 DCM blocks with one extra bit) or (6–bit counter with 6–bit DCM using 3 DCM blocks) as resolution partitioning combinations, respectively.

Figures 3.15 through 3.18 show different resolution partitioning for the 12–bit DPWM discussed earlier. This results in higher switching frequencies with different duty cycle values for demonstration purposes.

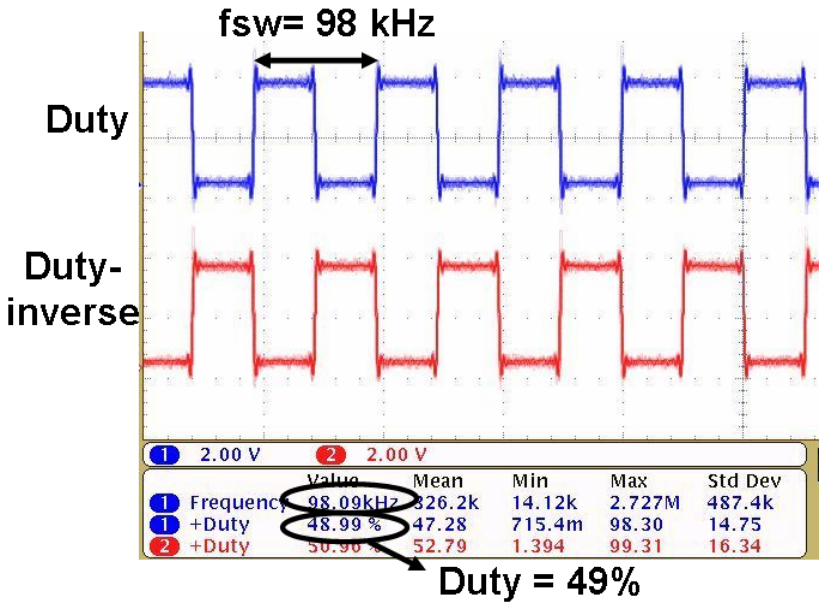


Figure 3.15 12–bit DPWM implemented with 10–bit counter and 2–bit DLL using one DCM block demonstrating 49% duty cycle

Figure 3.15 illustrates the case with 10–bit counter and 2–bit DLL using one DCM block achieving around 98 kHz.

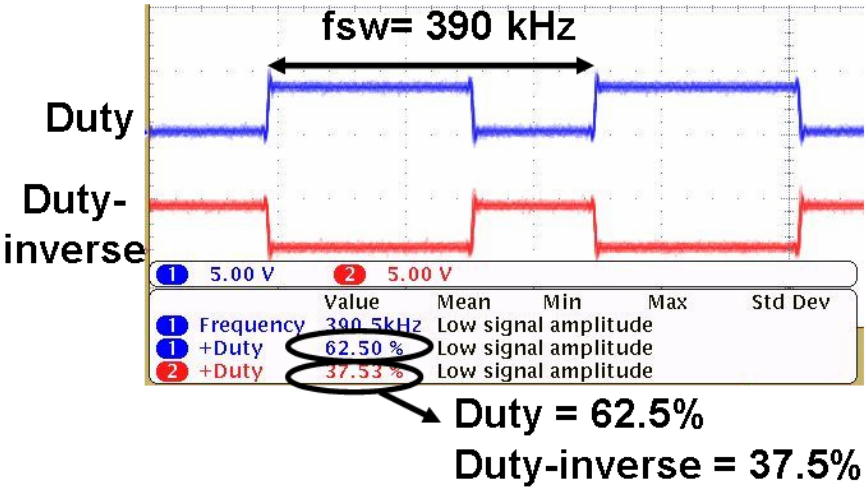


Figure 3.16 12–bit DPWM implemented as 8–bit counter with 4–bit DCM using two DCM blocks demonstrating 62.5% duty cycle

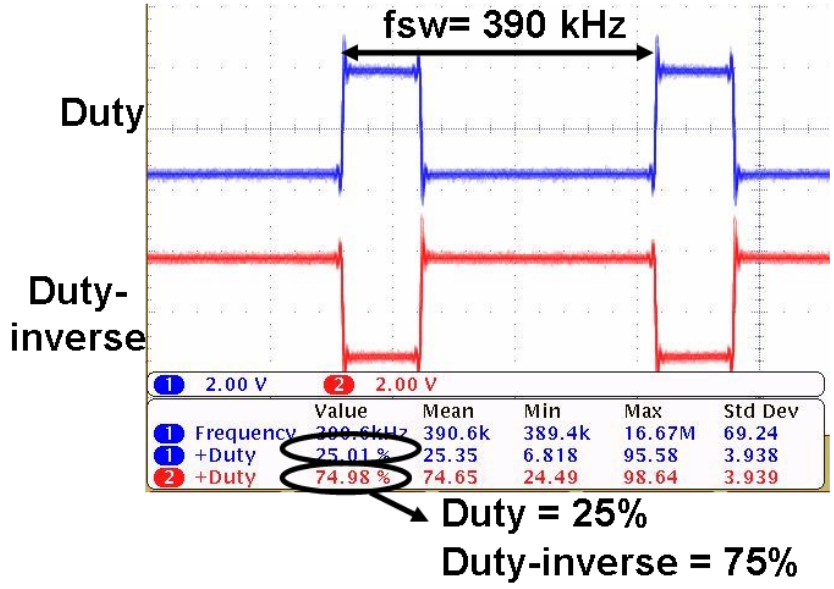


Figure 3.17 12–bit DPWM implemented with 8–bit counter and 4–bit DCM using two DCM blocks demonstrating 25% duty cycle

Figures 3.16 and 3.17 illustrate the 8–bit counter & 4–bit DCM using 2 DCM blocks cascaded as illustrated earlier in Section 3.2. Arbitrary values of the duty cycle (62.5% and 25% duty cycle, respectively) are chosen for illustration and verification purposes.

A higher switching frequency of 1.56 MHz is obtainable as shown in Figure 3.18 with 17.5% duty cycle.

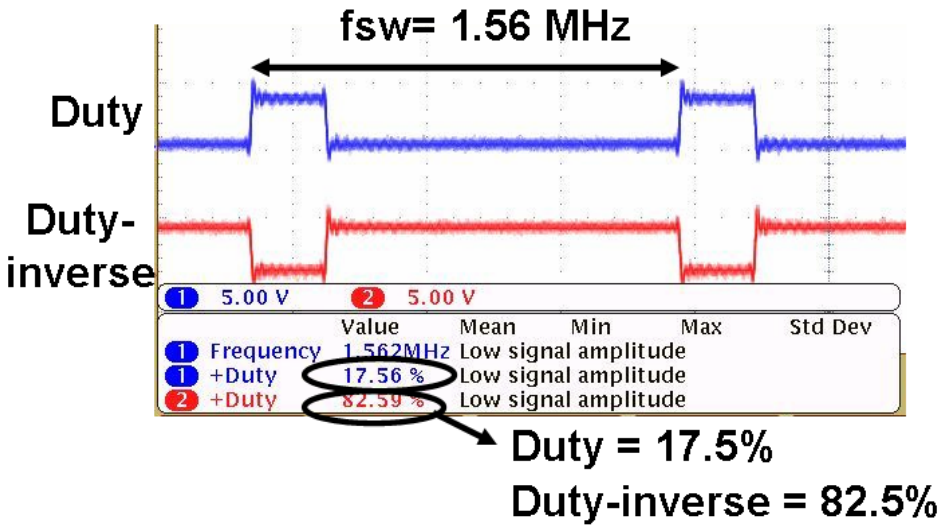


Figure 3.18 12–bit DPWM implemented with 6–bit counter and 6–bit DCM using 3 DCM blocks demonstrating 17.5% duty cycle

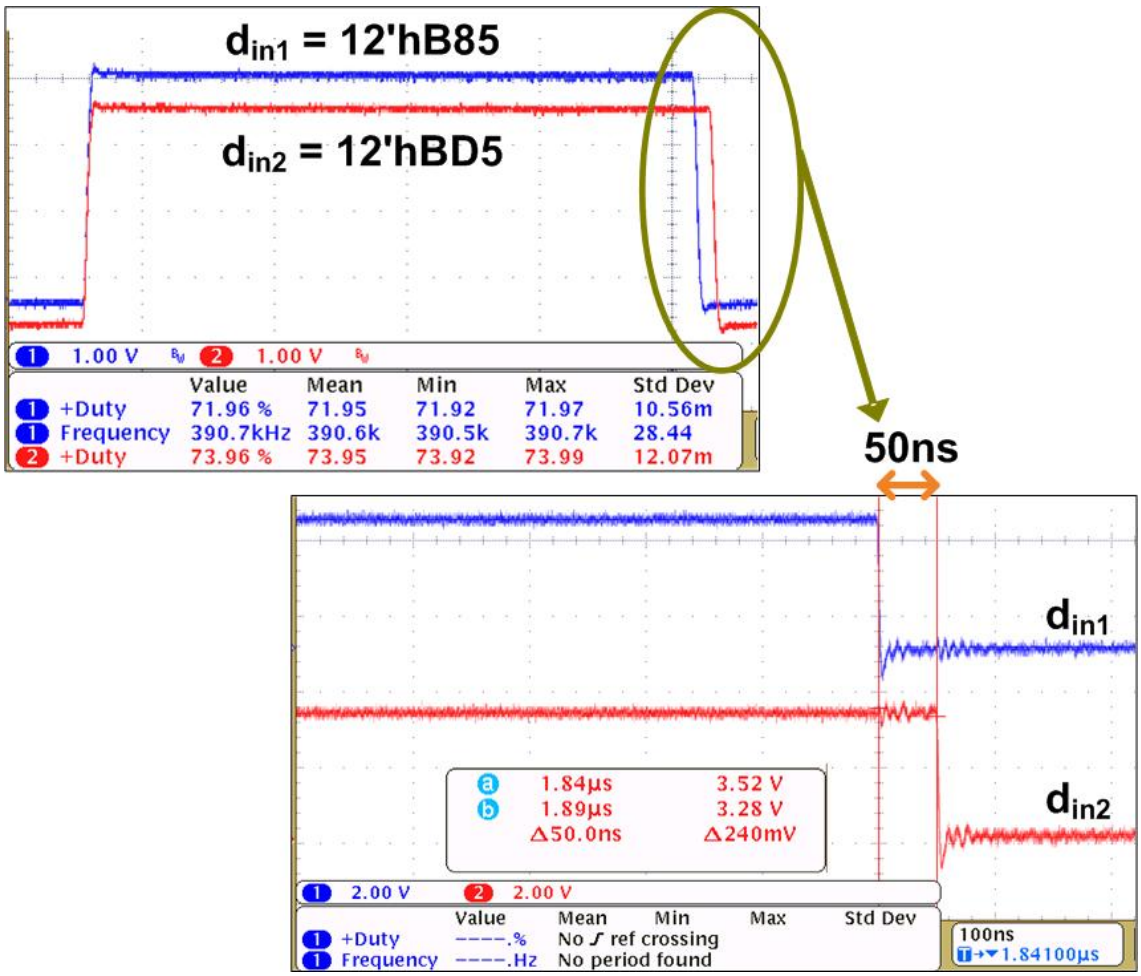


Figure 3.19 12–bit DPWM implemented with 8–bit counter and 4–bit DCM using two DCM blocks showing 0.6ns time resolution

For additional demonstration of the fine resolution achieved using the proposed Window Segmented DCM based DPWM, Figure 3.19 verifies the high resolution achieved by showing the increment in the duty cycle for 80 bit value difference due to hardware limitations in the oscilloscope to show finer steps of 1 bit.. In other words, d_{in1} was the first duty cycle value coming from the compensator corresponding to a value expressed in hexadecimal representation as $d_{in1} = 12'hB85$, a value translated to 2949 in decimal or expressed in percentage as:

$^{2949}/_{2^{12}} = {}^{2949}/_{4096} = 71.99\%$. Whereas, $d_{in2} = d_{in1} + 80bits\ value = 12'hBD5$ which can be expressed in decimal representation as $d_{in2} = 2949 + 80 = 3029$ or written in a percentage notation as $^{3029}/_{2^{12}} = {}^{3029}/_{4096} = 73.95\%$ duty cycle as verified in Figure 3.19.

For the achieved switching frequency of 390 kHz ($T_{sw} = 2.56\mu sec$), the resolution per LSB increment can be demonstrated by Equation (3.4):

$$\Delta t|_{1bit} = \frac{T_{sw}}{2^{N_{DPWM}}} = \frac{2.56\mu sec}{4096} = 0.6nsec \qquad (3.4)$$

For the case of 80 bit value increment, the time resolution is $0.6n \times 80 = 50nsec$ as verified in the experimental waveform shown in Figure 3.19.

The experimental results presented in this section verified the operation of the proposed Window Segmented DCM based DPWM architecture. It can be noted that the DPWM resolution is reconfigurable and the counter resolution can be decreased with added DCM blocks operating at a fixed oscillator frequency which results in increased switching frequency.

For a targeted 1MHz switching frequency and 12–bit DPWM, the required oscillator clock frequency, f_{clk} is shown in TABLE 3.2. It can be noted from the table that the proposed DCM–based DPWM can lower the clocking frequency requirements to achieve higher

switching frequencies operating at improved resolution. TABLE 3.3 lists the maximum switching frequency achieved if a fixed 100MHz oscillator clock, f_{clk} is used.

TABLE 3.2
f_{clk} REQUIREMENTS FOR 1MHZ SWITCHING FREQUENCY

Resolution Partitioning	N_{clk}	f_{clk}
Counter–Comparator	12	4 GHz
DLL	10	1 GHz
2DCMs–4bit	8	256 MHz
3DCMs–6bit	6	64 MHz

TABLE 3.3
MAXIMUM f_{sw}RESULTING FROM 100 MHZ OSCILLATOR

Resolution Partitioning	N_{clk}	f_{sw}
Counter–Comparator	12	24.41 kHz
DLL	10	97.65 kHz
2DCMs–4bit	8	390.625 kHz
3DCMs–6bit	6	1.56 MHz

Another beneficial tool Xilinx provides is the pre–design Xilinx Power Estimator tool (XPE) available on the web [116] which helps estimate worst case power and design cooling systems if needed [115]. XPE is a spreadsheet that works with Microsoft Excel supporting almost all devices and platforms [113, 114]. The XPE spreadsheet consists of many tabs and considers the design resource usages and several other design parameters entered by the user

in the power estimation process. Thus, the accuracy of the results and measurements derived from using XPE depends on the input data entered into the spreadsheet by the end user and the characterization of the device already modeled into the tool and summarized in the Release tab as part of the tool. Therefore, the best utilization of XPE is to report the worst case power estimation which gives a good look at the optimum operation and best application of the design [114, 115].

For more accurate and closer to realistic power calculations, the XPE allows for importing the Map reports (.mrp) that summarizes the design in terms of actual resource utilization. The (.mrp) files are generated from Xilinx ISE Webpack software used for simulation and bitstream loading and can be imported to the XPE sheet in the first tab (Summary tab) by clicking the “Import from ISE” button as shown in Figure 3.20. Furthermore, the Summary tab allows for device description specifying the part, package and grade of the chip for further accuracy.

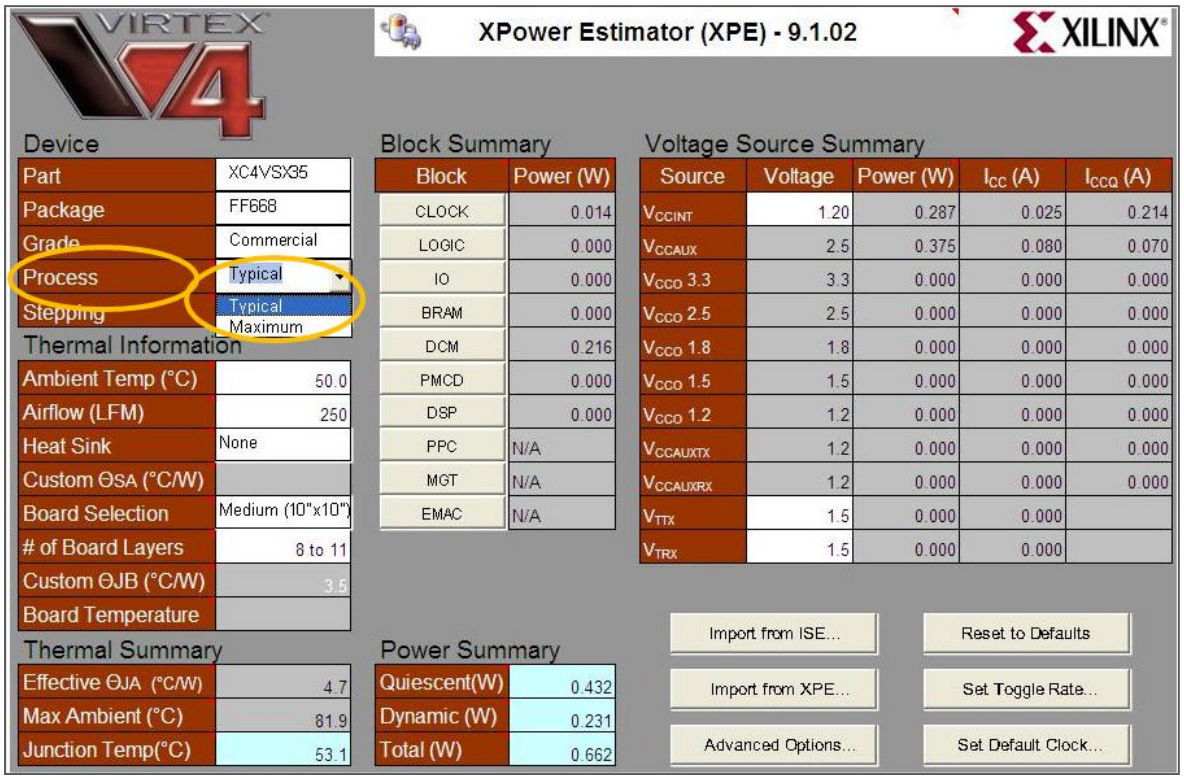


Figure 3.20 XPE for Virtex–4 FPGAs

Power numbers show both the static (quiescent) which merely depends on the FPGA board being used and entered in the Summary tab as mentioned above and the dynamic power consumption to which the clocking frequency contribute the most along with the load capacitance [114, 115]. Another important factor in calculating power is the logic power consumed by the total number of gates being used in the design and resource utilization of the board which add a large share in the overall power that is consumed by the architecture. The ISE tool provide the necessary information about the total number of Configurable Logic Blocks (CLBs) which is the building block of FPGAs, Look–Up tables (LUTs) and flip flops count needed to obtain the logic power which can also be imported from the ISE to the XPE via the (.mrp) file.

TABLE 3.4 shows both the estimated nominal (for typical processing entered in the design information Summary tab as shown in Figure 3.20) and worst case power (for maximum process setting) in Watts (W) for 12bit DPWM in case of using conventional DLL and two configurations of DCM block combinations with 100MHz clocking frequency.

TABLE 3.4
XPOWER ESTIMATED RESULTS

Resolution partitioning with $f_{clk} = 100MHz$	N_{clk}	f_{sw}	Nominal total power (W)	Worst case total power (W)
DLL	10	97.65 kHz	0.521	0.781
2DCMs–4bit	8	390.625kHz	0.662	0.952
3DCMs–6bit	6	1.56 MHz	0.914	1.181

TABLE 3.5
XPOWER ESTIMATED RESULTS FOR $F_{SW} = 390$ KHZ

Resolution partitioning for $f_{sw} = 390kHz$	N_{clk}	f_{clk}	Nominal total power (W)	Worst case total power (W)
DLL	10	400 MHz	0.727	0.991
2DCMs–4bit	8	100 MHz	0.662	0.952

As apparent from TABLE 3.4, the 12bit DPWM configured as a conventional DLL operating at 100MHz clocking can only achieve a maximum of 97.65 kHz switching frequency consuming around 0.8W of estimated power loss in the worst case scenario. While the reconfigurable DCM architecture achieves higher switching frequency ranges using the

same 100 MHz oscillator clock with a slight increase in the power consumption compared to using DLL. However, for the same targeted switching frequency of 390 kHz as an example, a lower clocking will be needed for DCM based architecture and consequently less power consumed compared to DLL based DPWM design as listed in TABLE 3.5.

It is worth the mention here that the XPower Estimator tool from Xilinx used to generate Table V does not capture in its calculations the windowing feature. i.e the numbers in Table V are the worst calculated power consumption which do not include the window signal assuming that the DCM blocks operate at high frequency during the whole switching period. This is not the case in the proposed architecture where the high frequency DCM blocks are operated only during a small fraction of the switching period ($1/2^{N_{clk}}$ of the switching period) which will result in much lower power consumption in real application than the numbers shown in Table V.

3.5 Conclusions

A new Digital Clock Manager (DCM) based DPWM architecture is proposed in this chapter. It consists of two components: a linear counter comparator and the DCM based component. The main advantage of the proposed architecture is the full utilization of the DCM resources already existing on FPGA boards at a reduced clock frequency when compared to the conventional DLL. Consequently, lower power consumption can be achieved and thus, allowing for higher switching frequencies. The proposed architecture is verified in this paper using Xilinx Virtex4 board – XC4VSX35 FFG668 device, however, since the proposed DPWM structure uses DCM blocks and few other hardware resources

such AND gates, Flip–flops and counters, it can be easily transplanted into other small–scale FPGAs or smaller devices of the same family with lower quiescent power for lower power consumption, giving more application–oriented design flexibility. Moreover, this architecture can be reconfigured to achieve different desired DPWM resolutions.

CHAPTER 4:
LINEAR AND NONLINEAR DYNAMICALLY SHIFTED RAMP DIGITAL CONTROL TECHNIQUE FOR IMPROVED TRANSIENT RESPONSE IN DC–DC CONVERTERS

4.1 Introduction

Improving the steady–state and dynamic behaviors of DC–DC converters is a quest that has not ceased to be the focus of design engineers and researchers whether in the analog [84 – 96, 98, 100, 101, 103, 108] or the digital control [83, 97, 99, 102, 104 – 107] domains. Robust closed–loop compensator design readily achieves a well regulated performance at a fixed operating point but unexpected and fast load changes occur causing the whole system to deviate into a transient mode away from the desired steady–state condition.

Under load changes, the difference in the energy balance must be handled, and since the power stage cannot catch up with the fast load change effectively due to the large filter inductance required to decrease the output current ripple, the energy imbalance will be accounted for by the bulk filtering capacitors until the power stage is capable of delivering the energy needed at the load side [95]. The time it takes the power stage to establish a steady–state energy balance during the transient can result in out–of–tolerance output voltage which can lead to thermal stresses as well as system failure and degraded reliability. Thus, major research efforts have been devoted to increasing the transient response of the regulator and help the power stage respond faster to any input and load change [83 – 109].

Moreover, since during load transients the output voltage suffers unwanted spikes, this requires huge filtering capacitors at the load side to clean out the signal. These filtering capacitors are expensive in terms of cost and space utilization. Consequently, numerous techniques have been dedicated into treating transient conditions as discussed in the following section.

4.2 Past Practices

Literature covers two main techniques in handling transients and suppressing the undesired voltage spikes: linear and non–linear control techniques [83 – 109]:

4.2.1 Linear Techniques

Linear techniques include:

Passive methods The first attempt into improving the dynamic response was centered at suppressing the high voltage spikes which occur during transients by means of passive techniques.

Passive methods include two approaches into solving the transients and enhancing the dynamic response of converters:

More filtering capacitors: The straight and direct method is by adding more filtering capacitors to clean out the voltage and reduce the spikes. And as listed in literature, different capacitors have different parasitic values; mainly the equivalent series resistance, ESR, and the equivalent series inductance, ESL. Thus, different kinds of capacitors have different effect on voltage spikes during transients. Paralleling more capacitors aim at reducing the parasitic ESR and ESL which help alleviate and reduce the voltage spikes. This method is

effective in enhancing the transient and decreasing the voltage spikes; however, the improvement is limited by the parasitic resistance and inductance values of the trace, in addition to the drawback of increased cost and size which make this method unsuitable to meet the increasing requirements of smaller DC–DC converters in terms of size and cost.

Higher switching frequencies: Another passive method investigated in research was increasing the switching frequency of the system. This entails smaller magnetics which includes smaller inductance value, which in turn lead to improved transient response. However, this technique deteriorates the efficiency due to the accompanying increase in the switching losses.

Active Approach: The second approach is an active control oriented method, focusing on decreasing the delays and improving the bandwidth. It includes, but not limited to, current and voltage compensation techniques:

Current Compensators: The conventional current compensation was an attractive method of injecting high slew rate current in step–up load and absorbing the voltage overshoot in step down load, the injection can be made in either a linear or a switching mode. The drawback is the large current stress that results in high conduction losses in linear mode and high switching losses in the switching mode.

Voltage Compensators: Active Transient Voltage Compensator (ATVC) is a voltage injection method. The power loss is reduced due to the transformer that is being introduced as

a vital element in the circuit of the ATVC. It relies on injecting high slew rate current during step–up load and energy recovery in step down load [95].

ATVC is only activated during transients with several MHz operating frequency whereas the main VR remains at relatively lower frequency range to maintain better efficiency. The extra circuitry introduces new losses in addition to control complications.

Controller Design Approach: Large delay times inherited in the controller, compensation network and the LC filter deteriorated the voltage spikes even more. Hence, the recent attention drawn to control design development as a direction to improve the dynamic response instead of circuit topologies. Literatures covers many control techniques to alleviate the load spikes during transients, below is a review of some control practices:

Duty Cycle Saturation: This control technique senses the load variations, and when transients occur, the controller saturates the duty cycle. In other words, at step–up load the controller will push the duty cycle to 100% in order to supply the extra needed current as quickly as possible to the load in less switching cycles with minimum dependency on the filtering capacitors to deliver that current to the load. And hence, alleviate the spikes and decrease the settling time and faster retain the output voltage to the desired value. In an analogous scenario, at step down load, the controller shuts off the duty cycle to the minimum to allow fast absorption of the extra current at the load with reduced spikes. This method proves efficient only in case of extreme transients but may cause overcompensation.

Compensator gain: Some design engineers varied the compensator gain during transients to minimize the required error signal which ultimately enhances the transient response. The loop

gain is varied to compensate for any error between the output voltage and the desired value. At transients, the gain of the compensator is controlled to modulate the bandwidth of the loop and minimize the required change in the error signal and eventually enhance the dynamic response of the system. This method is limited due to system instability issues that might occur through varying the loop gain of the converter.

Dynamic PWM ramp signal: This control technique dynamically modulates the peak value of the PWM ramp waveform, which will then vary the modulator gain, and during transients will minimize the required change in the error signal. This will help the compensator reach the steady–state value faster enhancing the transient response of the converter. Nevertheless, varying the peak of the ramp signal effectively varies the slope of the signal which means that a big change in the peak will be needed to compensate for big transients. Furthermore, an extra analog oscillator is needed to control the ramp. This topology is not optimal in digital implementation since for higher peak values, faster oscillators will be needed which dramatically affect the efficiency due to increased power consumption [97].

4.2.2 Non Linear methods

Many non–linear control techniques, mainly implemented digitally for various advantages discussed in Chapter 2, have been extensively applied to improve dynamic behavior of DC–DC converters.

A new digital control scheme aiming to improve the transient response and efficiency of an FPGA–based digitally controlled DC–DC converters in terms of shorter settling time with optimal over–and undershoots is presented in this Chapter. The proposed approach enhances the dynamic response by dynamically controlling the ramp of the digital PWM unit through applying a positive or negative shift value moving the PWM ramp waveform upwards or downwards respectively depending on the sign of the error signal or in other words, the direction of transient. This will help the compensator reach the steady–state value faster.

The dynamic Ramp Shift design method presented in this work can be a linear DC shift or can be extended to include higher order nonlinear terms. Moreover, it utilizes existing system digital controller, and does not require any additional circuitry.

4.3 Proposed Control Technique – Principal of Operation

Figure 4.1 shows a block diagram of a digitally controlled switching converter, where the ADC digitizes the output voltage which is next compared to the desired reference value V_{ref}. The resultant error signal V_{err} is subsequently minimized through the action of a compensator that generates a duty cycle command d_{in}. The compensator is designed to maintain a near zero error signal during steady–state and to enhance the dynamic performance during transients. The DPWM unit translates the duty cycle command of the compensator d_{in}, to an analog driving signal D, controlling the ON–time of the switching Converter. Consequently, a well designed PID compensator and high resolution DPWM architecture are essential to achieve a tightly regulated converter.

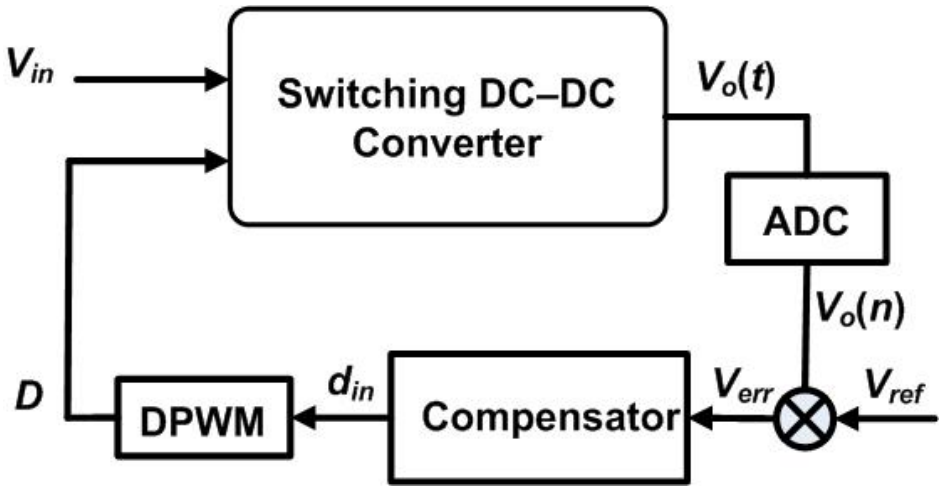


Figure 4.1 Block diagram of a digitally controlled DC–DC converter

Moving around the closed loop, the first block encountered in the digital loop is the Analog to Digital Converter (ADC) whose function is to sample and convert the analog sensed output voltage, $V_o(t)$, into digital data, $V_o(n)$. System requirements for minimum output voltage ripple ΔV_o and desired output voltage V_{ref} decide the resolution of the ADC.

Next, the compensator processes the error voltage, V_{err}, and generates a duty cycle command d_{in}.A third order PID compensator is used in many systems. Different compensation methods were introduced to optimize the poles and zeros of the compensator to enhance the transient response of the system, while this research focuses on utilizing the DPWM unit to achieve better dynamics.

The final block in the digital loop is the Digital Pulse Width Modulator (DPWM) which translates the digital output of the compensator into an analog pulse train. Many circuits and architectures are presented in the literature on the implementation of the DPWM unit. The first reported and simplest architecture, offering the best linearity is the direct emulation of the analog ramp signal, shown in Figure 4.2, known as the counter–comparator DPWM [44]. It is basically a digital form of the conventional analog duty cycle generation where a digital saw–tooth signal with a frequency equals to the switching frequency of the converter is compared to the duty cycle value coming from the compensator d_{in} as shown in Figure 4.2.

The duty cycle is set high every time the counter of the ramp signal resets to zero and the comparator resets the duty cycle by triggering the instance at which the commanded duty cycle d_{in} exceeds the ramp signal, as shown in Figures 4.2 and 4.3.

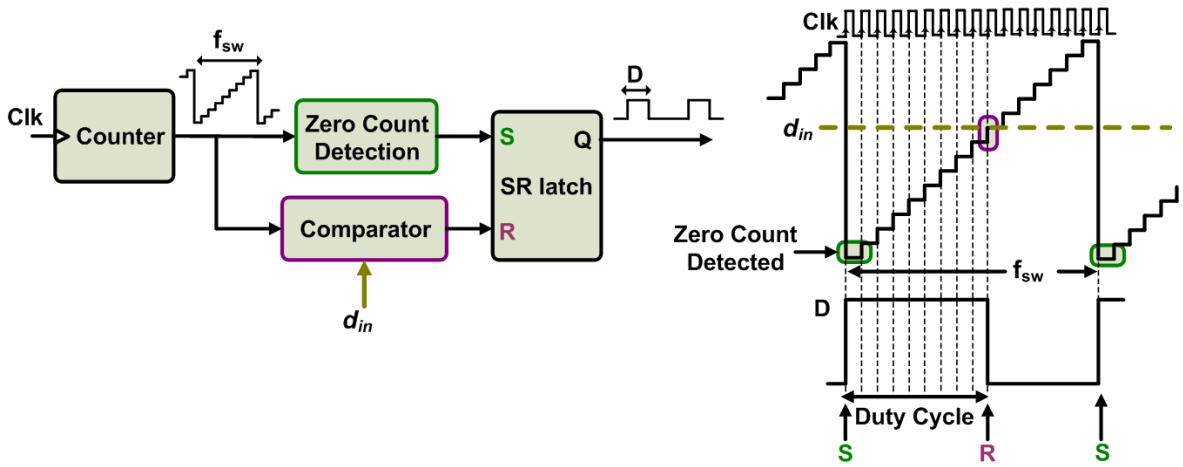


Figure 4.2 Counter–Comparator DPWM architecture

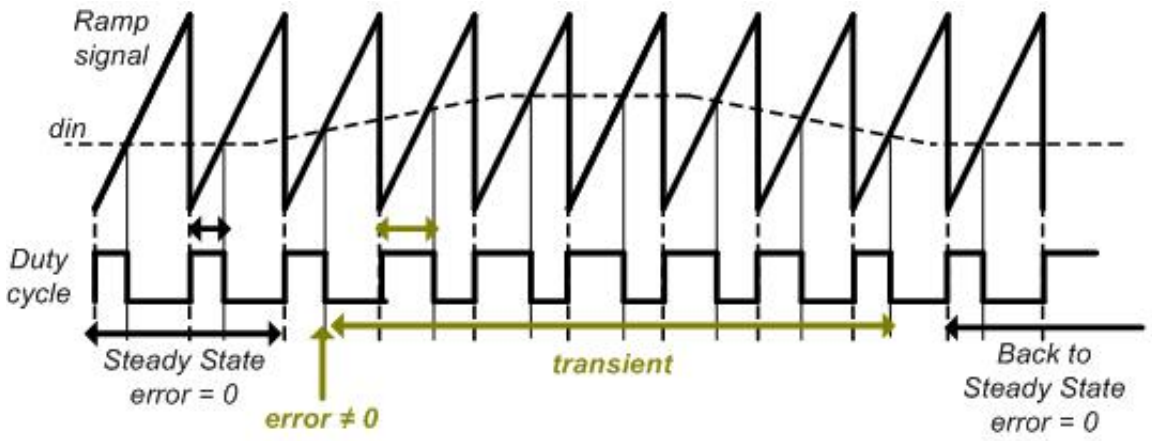


Figure 4.3 A Ramp PWM operation

The operation shown in Figure 4.2 generates the steady–state duty cycle by which the switches are operated and achieve the desired output voltage. After a load increase, the sensed output voltage is less than the desired reference voltage and, a positive error signal will occur. Consequently, the compensator will produce a discrete duty cycle value larger than the steady–state duty cycle d_{in} which will cause the comparator to reset the duty cycle at a later instance, hence increasing the effective ON–time of the main switch. This helps raise the output voltage back to the desired steady–state value, as shown in Figure 4.3.

In summary, the duty cycle command coming from the compensator is compared against a ramp signal and the duty cycle D is accordingly generated.

During transients the system diverges away from the desired steady–state region, and thus, the power stage relies on the compensator to minimize the deviation and return to the designed steady–state. The longer it takes for the compensator to reach the steady–state, the

worse the transient response becomes. In an attempt to reduce the time required by the compensator and consequently achieve better dynamics, the idea of adjusting the offset shift value of the ramp PWM was investigated.

In this research in Chapter 4, the proposed architecture shifts the ramp signal by a DC value which is a proportional function of the error signal in order to compensate for the difference and help the system reach the steady–state faster than the case where the compensator works alone discussed as follows:

For a step–up load change, a positive error will occur according to Equation (4.1)

$$V_{err} = V_{ref} - V_o \qquad (4.1)$$

Consequently, the compensator produces a duty cycle command larger than the duty cycle value at the steady–state (zero error) and the PWM generates a larger duty cycle to compensate for the error and increase the output voltage to the desired reference again. This process takes the compensator many switching cycles as shown in Figure 4.3, which deteriorates the dynamic performance of the system.

Figure 4.4 illustrates the proposed concept of Ramp–Shifting, where the ramp signal is shifted by a value proportional to the error signal $f(e)$; at steady–state, the error signal is near zero and the ramp is not altered, whereas, a positive error will shift the ramp down by a value set by the $f(e)$ block.

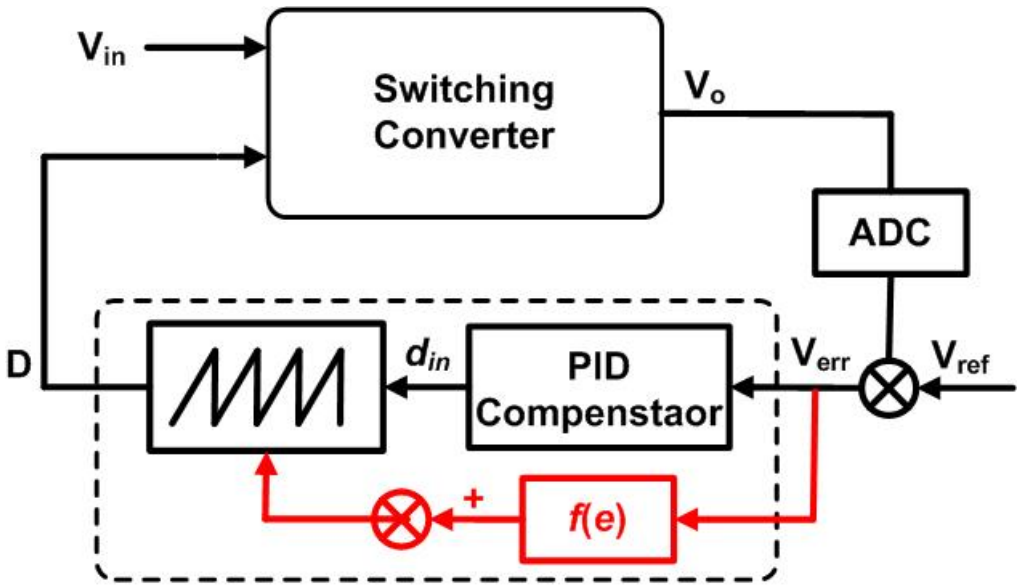


Figure 4.4 Proposed DC–Ramp–Shift architecture

The shifted ramp will help the compensator reach back the steady–state faster; in less switching cycles and shorter time as shown conceptually in Figures 4.5(a) and(b).

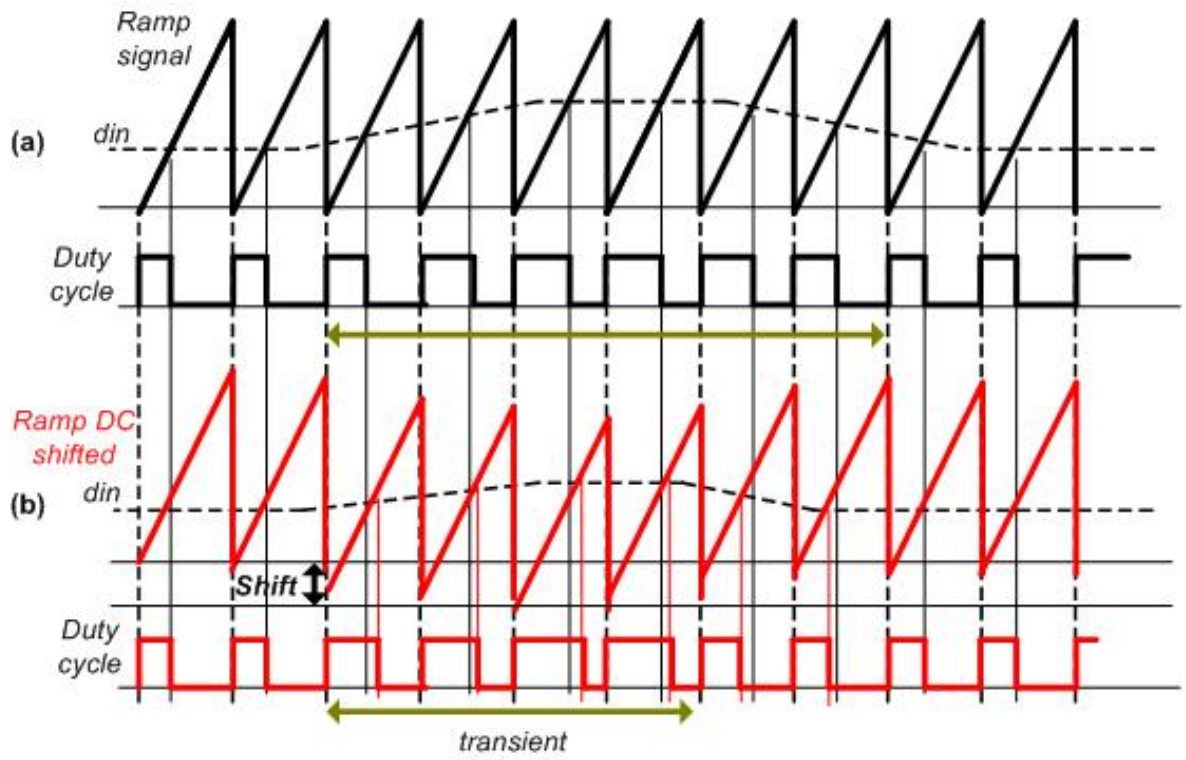


Figure 4.5 Ramp and PWM signals: (a) conventional PWM without dc ramp–shift, (b) PWM with the proposed dc ramp–shift architecture

Therefore, based on the error signal, the ramp signal is dynamically moved up and down in order to lower the output voltage deviation and as a result enhance the performance.

At the instance the transient occurs until the system is back to the steady–state, the compensator tries to minimize the error by controlling the duty cycle. Therefore, the error is continually varied and gradually reaches a near–to–zero value at steady–state. And as a result, the shift factor $f(e)$ is dynamically varied with the value of the error signal.

Figures 4.5(a) and (b) compare the conventional and the proposed ramp architecture for the same transient, the proposed dc ramp–shift architecture treats the output voltage deviation with more duty cycle variation than the conventional ramp. The PWM shift will only occur during transient in order to shift the ramp downwards or upwards as illustrated in Figures 4.6(a) and (b).

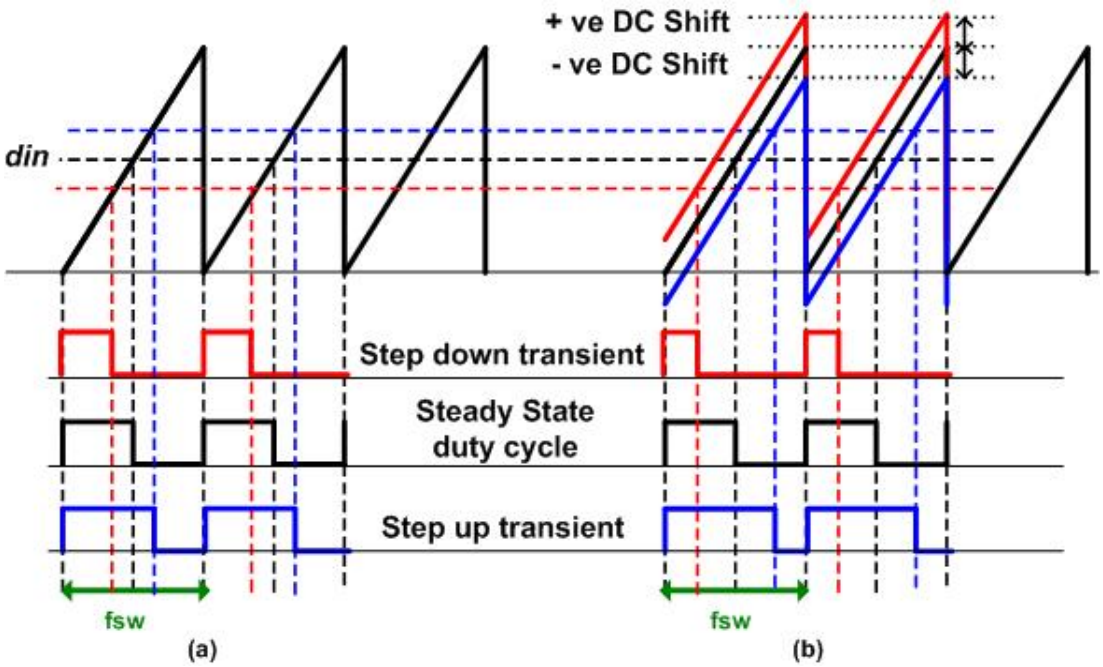


Figure 4.6 The Effect of dc–ramp–shift during transients: (a) conventional ramp architecture with no dc ramp–shift (b) with dc ramp–shift

Figure 4.6(a) shows the conventional ramp during steady–state and transient conditions. A step–up in the load current produces positive error which is processed through the compensator and a switching signal with larger duty cycle is thus generated. This longer ON–time of the switching network will help generate the desired current and increase the output voltage back to the steady–state value over a number of switching periods.

On the other hand, the same step–up load transient treated using the proposed DC–Ramp–Shift shown in Figure 4.6(b) will produce a larger duty cycle which will reduce the number of switching periods required by the conventional architecture illustrated in Figure 4.6 (a), thus enhanced transient response.

Since the DC shift depends on the error signal and only occur during transients, there will be no delay in detecting the transients, given that the error signal carries in its value the occurrence of any transient. Meaning, a near zero error means steady–state condition, whereas a step–up and step down load entail a positive and negative error respectively. In other words, the shifting will only occur during transient for the reason that the error (shift value) is almost zero during steady–state, while during transient, the positive or negative value of the error will shift the ramp downwards or upwards.

4.4 Numerical Analysis:Verification of Concept

4.4.1 Verification of Concept

Closed–loops are designed to drive the system into operation around a desired steady–state at near zero error signal (V_{err_ss}) by generating a duty cycle command (d_{in_ss}) corresponding to the desired steady–state operating point $(D_{ss} = V_{ref}/V_{in})$ as illustrated in Figure 4.7 and expressed in Equation (4.2).

$$D_{ss} = \frac{x}{y} = \frac{V_{err\_ss}}{V_p} \qquad (4.2)$$

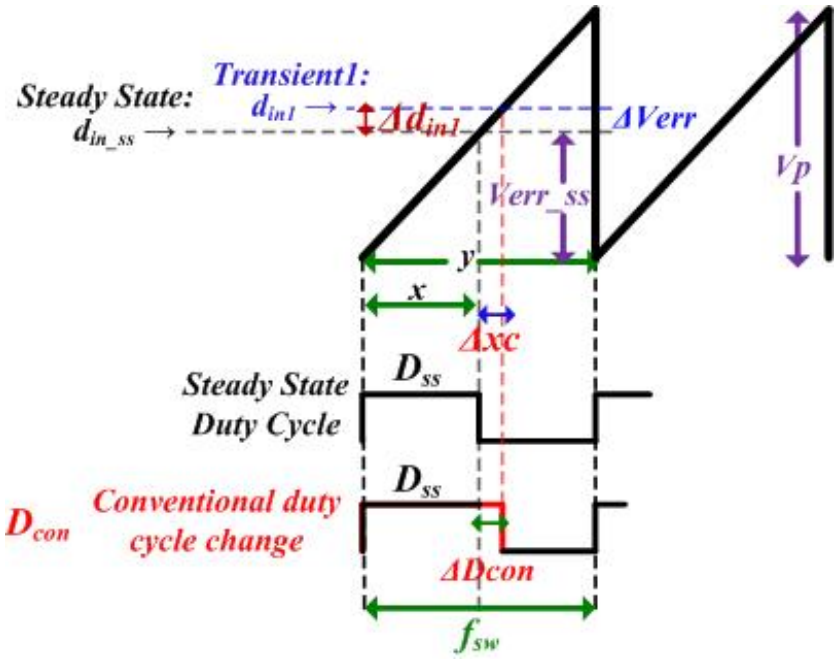


Figure 4.7 Conventional static ramp control

At load change, the output voltage deviates from the reference value resulting in a change in the error signal $(\pm\Delta V_{err})$ superimposed on the steady–state value (V_{err_ss}), the function of the compensator is to minimize $|\ \Delta V_{err}\ |$ by producing a change in the duty cycle command $(\pm\Delta d_{in})$ added/subtracted to/from the steady–state, depending on the sign of the transient.

For demonstration purposes, a step–up load is discussed when *Transient1* occurs as depicted in Figure 4.7. Accordingly, the compensator generates a duty cycle command larger than the steady–state value $(d_{in1} > d_{in\_ss})$ which when compared against the ramp signal is translated by the DPWM into a longer duty cycle to compensate for the difference in current and the decrease in the output voltage.

The new duty cycle command d_{in1} can be denoted as an increment added (Δd_{in1}) to the steady–state command which results in a proportional increment (ΔD_{con}) added by the DPWM to the steady–state duty cycle value as put in Equation (4.3).

$$d_{in1} = d_{in\_ss} + \Delta d_{in1} \implies D_{con} = D_{ss} + \Delta D_{con} \tag{4.3}$$

Where ΔD_{con} refers to the change in duty cycle for conventional ramp.

The generated duty cycle value (D_{con}) corresponding to the increase in the load current can be derived from Figure 4.7 as expressed in Equation (4.4)

$$D_{con} = D_{ss} + \Delta D_{con} = \frac{x + \Delta x_c}{y} = \frac{V_{err\_ss} + \Delta V_{err}}{V_p} \tag{4.4}$$

Thus, the dynamic response of the system is highly dependent on the output of the compensator (change in duty cycle command, Δd_{in}) and the mechanism by which (ΔV_{err}) is processed which eventually results in the duty cycle change from the DPWM (ΔD) in order to restore the steady–state operation. Typically, compensators designed in the small–signal model do not efficiently handle large signal swings created during transients. As a result, many switching cycles are required before the system is back to steady–state.

The purpose of the proposed control scheme is to help the compensator process the change in the error (ΔV_{err}) more effectively, faster and with minimum over– and under–shoots. A

look into the conventional static ramp control–based systems will help highlight the benefits of the proposed approach.

Equation (4.4) can be rearranged as in Equation (4.5) to extract the change in the duty cycle generated by the compensator as the result of step–up *Transient1* shown in Figure 4.7 using a conventional ramp.

$$D_{ss} + \Delta D_{con} = \frac{V_{err\_ss} + \Delta V_{err}}{V_p}$$

$$D_{ss} + \Delta D_{con} = D_{ss} + \frac{\Delta V_{err}}{V_p}$$

$$\Delta D_{con} = \frac{\Delta V_{err}}{V_p} \qquad (4.5)$$

Equation (4.5) relates the change in the duty cycle value to the change in error (transient) which is a highly linear relationship.

Whereas, the proposed control scheme shifts the ramp signal by a DC value proportional to the error function $f(e)$. A step–up load results in a positive error change and accordingly the ramp will be reversely shifted downwards to compensate faster for the error as shown in Figure 4.8. In this case, the change in the duty cycle corresponding to the same *Transient1* of Figure 4.7 is derived as follows and stated in Equation (4.6)

$$D_{shift} = D_{ss} + \Delta D_{shift} = \frac{x + \Delta x}{y} = \frac{V_{err\_ss} + \Delta V_{err} + f(e)}{V_p}$$

$$D_{ss} + \Delta D_{shift} = \frac{V_{err}}{V_p} + \frac{\Delta V_{err\_ss}}{V_p} + \frac{f(e)}{V_p}$$

$$\Delta D_{shift} = \frac{\Delta V_{err}}{V_p} + \frac{f(e)}{V_p} \tag{4.6}$$

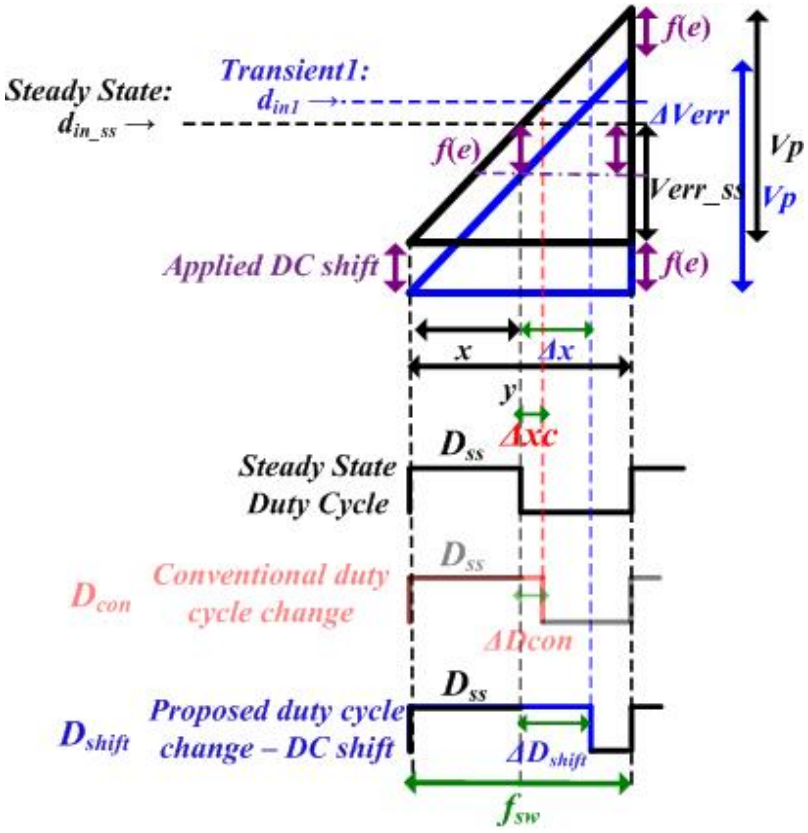


Figure 4.8 Proposed DC–ramp–shift control

Comparing Equations (4.5) and (4.6), it is noted that $\Delta D_{shift} > \Delta D_{con}$, by a value proportional to the DC shift function, $f(e)$ which means the change in the duty cycle value using the proposed approach is larger than that for the same transient compared to the conventional control. It will be shown later that this adjusted duty cycle will result in faster dynamics and less output deviation.

4.4.2 Control Loop Implementation

It is worth mentioning at this point that the effect of the proposed DC shift can be viewed as equivalent to adding an extra command to the output of the compensator before applying the DPWM, as shown in Figure 4.9

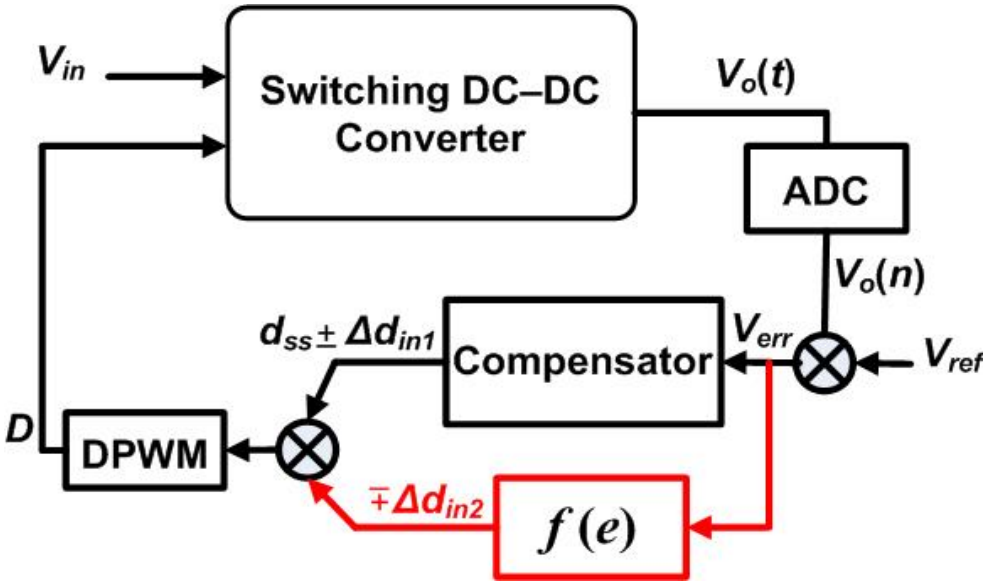


Figure 4.9 Conceptual effect of DC–ramp–shift

From Figure 4.9, it is noted that the compensator will operate as designed and will produce a duty cycle command of $(d_{ss} + \Delta d_{in1})$.

In parallel, the proposed $f(e)$ representing the DC shift of the ramp, processes the error and generates another duty cycle command (Δd_{in2}) added to the output of the compensator. The result (d_{in}) is then compared to the ramp to generate the duty cycle value with

additional processing of the error via applying $f(e)$ rather than the compensator alone which guarantees an improved dynamic behavior.

Figure 4.10 is a geometrical translation of Figure 4.9.

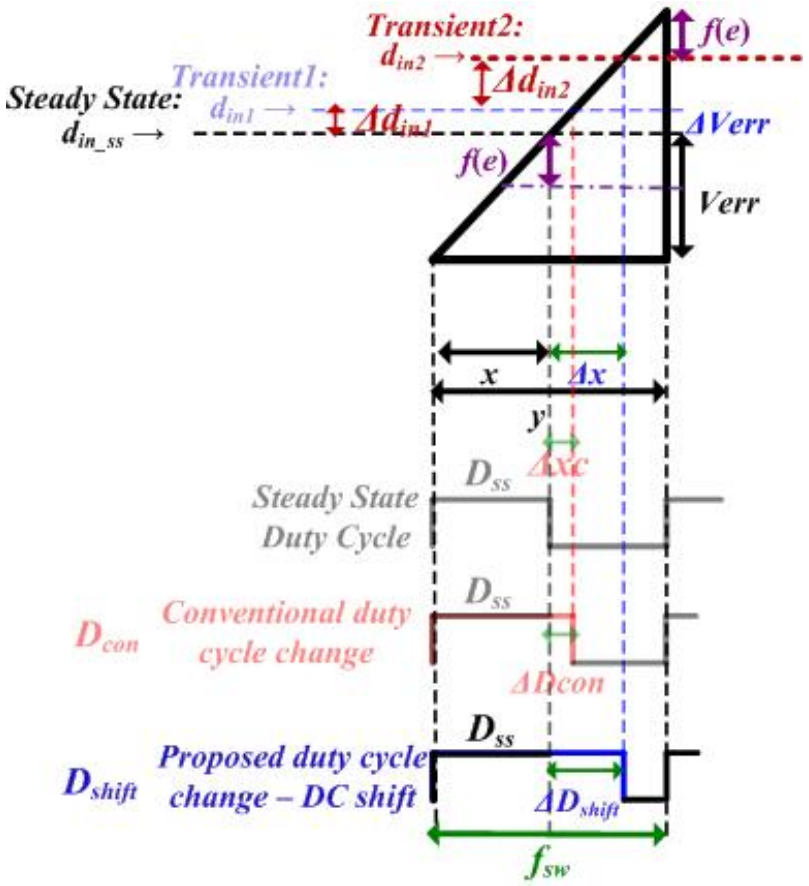


Figure 4.10 Geometrical realization of Figure 4.9

Thus, the proposed approach treats *Transient1* by a duty cycle command equal to that generated to treat *Transient2*, as highlighted by Figure 4.10, which projects an improved dynamics.

The next section focuses on the means of deriving the DC value by which the ramp is shifted.

4.4.3 Shift function Derivation

The main objective of applying the shift function $f(e)$ at transient conditions is to help the compensator achieve better dynamics by reducing the error signal. Therefore, the derivation of the best possible $f(e)$ requires studying the error signal which comprises the cost function to be reduced, a concept on which the derivation of the shift value is based and is thoroughly detailed later in this section.

Since the shift concept proposed in this work is a function of the error signal, $f(e)$, it can be a function of any order varying from a simple constant value of a linear gain $f(e) = \alpha$ to a complex time varying function $f(e) = \sum_{i=1}^{n} \left(\alpha_i \times e^{\mathrm{i}-1}\right)$ where e is the error signal and α_i are the coefficients to be determined. A general technique for deriving the coefficients of the shift function will be first generated for the simple linear gain, and subsequently expanded to include more complex nonlinear higher order terms, $f(e) = \alpha_1 + \alpha_2\, e + \alpha_3\, e^2 + \cdots + \alpha_n\, e^{\mathrm{n}-1}$:

4.4.3.1 DC Linear Shift

Due to the complexity of non–linear system analysis and the use of a digital platform which transforms systems into difference equations, a numerical approach is a better alternative to be adopted into determining the value of $f(e)$ that guarantees optimal dynamic response.

Furthermore, since the proposed PWM shift technique is specific for a certain controller and is intended to help the pre–designed compensator reach the steady–state faster, then the converter is first mathematically represented in difference equations, in terms of the inductor current and capacitor voltage.

Next an iterative technique is applied on the generated error sweeping the whole range of valid coefficient values and narrowing down the result to a set of optimal coefficients depending on the order of the shift function. A detailed numerical simulation of a digital DC–DC buck converter will best illustrate the derivation of the shift function, through a system with the following design specifications will be used for illustration purposes:

$$V_{in} = 10V, \qquad V_o = 3.3V, \qquad I_o = 1A,$$

$$f_{sw} = 100kHz, \quad \Delta V_o = 3mV, \qquad R_o = V_o/I_o$$

$$C = 1.03mF, \qquad L = 20.2\mu H, \quad r_L = 30m\Omega$$

Where r_L is the series resistance of the filtering inductance.

A complete diagram of the system in closed loop is shown in Figure 4.11(a), while the shifting circuit is given in Figure 4.11(b)

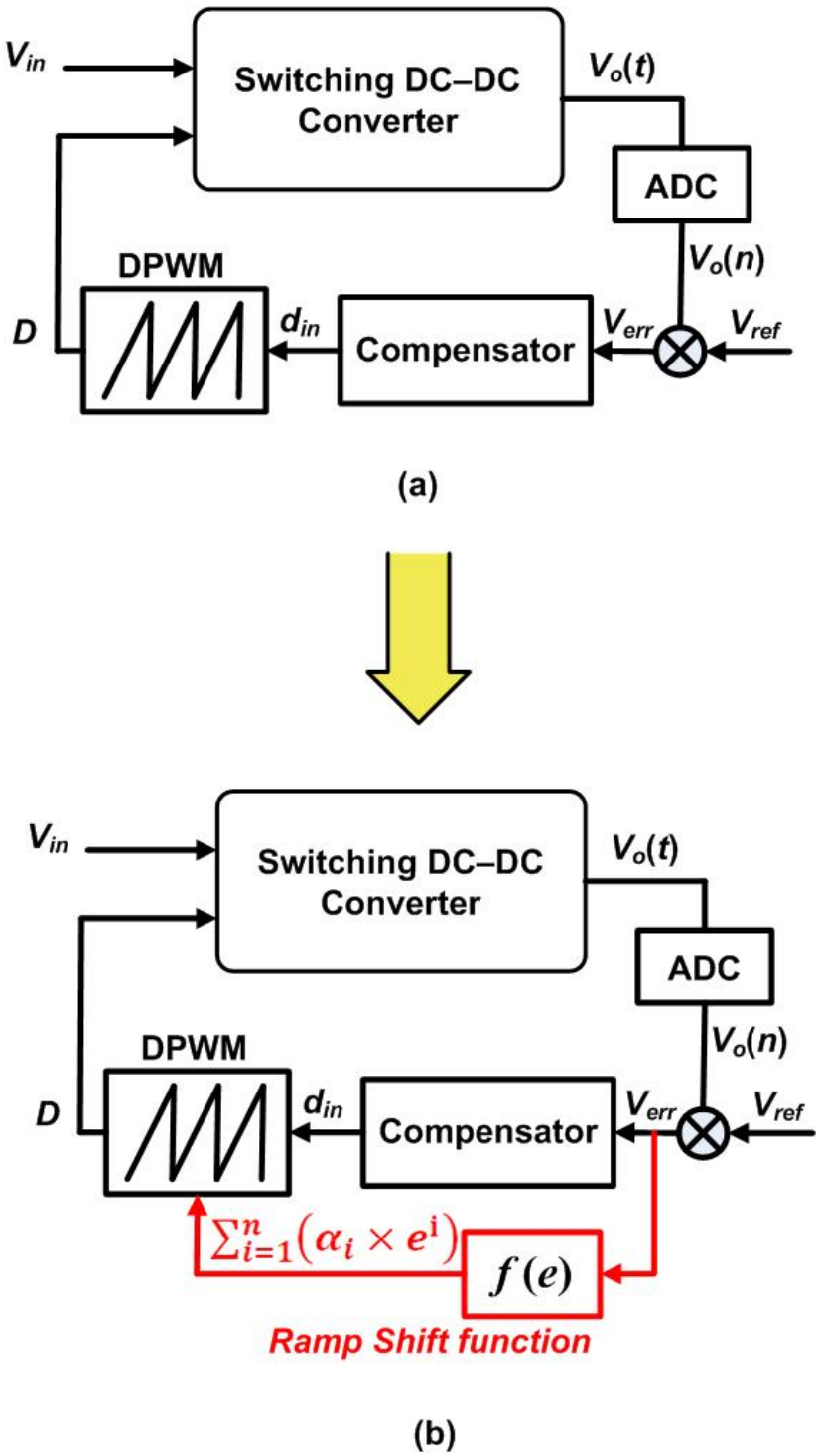


Figure 4.11 Simplified Block Diagram of a DC–DC converter with (a) Conventional (b) Shifted, Counter–Comparator DPWM architecture

A well regulated steady–state behavior is governed by designing a PID compensator in the small signal model of the converter in order to operate around the desired static point. The compensator was designed using the redesign digital approach and abiding to the stability criteria of control theory with gain margin around 24dB, phase margin of 69° and cutoff frequency of 7.5 kHz. Applying the bi–linear transformation, the digital compensator of Equation (4.7) was designed.

$$G(z) = \frac{\Delta d_{in}(z)}{V_{err}(z)} = \frac{8.631\,z^3 - 7.955\,z^2 - 8.619\,z + 7.968}{z^3 - 0.3333\,z^2 - 0.5556\,z - 0.1111} \quad (4.7)$$

Equation (4.7) can be expressed as a difference equation for updating the duty cycle change, $\Delta d_{in}[n+1]$ using previous, current and updated error signal values as in Equation (4.8).

$$\begin{aligned}\Delta d_{in}[n+1] = {} & 0.1111\,\Delta d_{in}[n-2] + 0.5556\,\Delta d_{in}[n-1] + 0.3333\,\Delta d_{in}[n] \\ & + 7.968\,\Delta V_{err}[n-2] - 8.619\,\Delta V_{err}[n-1] - 7.955\,\Delta V_{err}[n] \\ & + 8.631\,\Delta V_{err}[n+1] \qquad (4.8)\end{aligned}$$

As stated earlier, the PWM shift technique is a function of the error signal as shown in Figure 4.11(b). This means the shifting does not occur at steady–state when the error is almost zero. However, the error deviates from the steady–state range during transients; a step–up load will generate a positive error which shifts the PWM down by a value corresponding to $e\ f(e)$. And similarly, a step–down load generates a negative error shifting the PWM up. The proposed shifting mechanism helps the compensator alleviate the error deviation faster and ultimately results in an enhanced dynamic response. Nevertheless,

adding the shift loop to the overall feedback system affects the closed loop gain and may result in instability for certain values of the coefficients of $f(e)$.

Before moving any further, a preliminary simulation for the above mentioned system is run to verify the effect of the proposed PWM shift on the transient response using a linear gain DC shift function and the response plots are shown in Figure 4.12. Where $f(e)$ for $\alpha = 0$ corresponds to the conventional static PWM ramp with no DC shift shown previously in Figure 4.11(a).

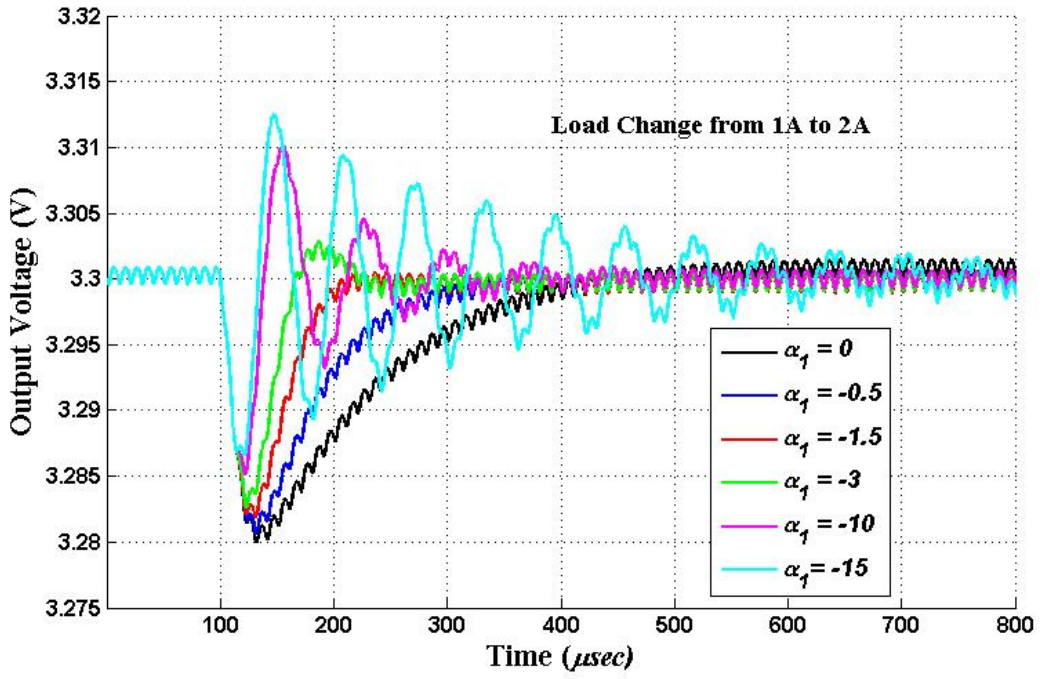


Figure 4.12 Output response under sudden load change with different DC shift values

Figure 4.12 illustrates the transient response of the system under step–up load change based on the converter specifications given earlier.

In order to maintain a constant power at the load side, the sudden increase in the load current drops the voltage instantly which results in a large positive error and, consequently a large overshoot occurs that is not easily–controlled and is highly dependent on the output filtering capacitors. Then, the closed loop compensator corresponds to the produced error and accordingly generates duty cycle commands over a number of switching cycles in order to minimize the error and retrieve the system back to the desired steady–state.

The shift technique alters the closed–loop during transient and impact the dynamic response, thus different shift values produce different dynamic responses as noted from Figure 4.12. Theoretically speaking, the bigger the DC shift value, the faster the system settles back to the steady–state, hence, $\alpha = -1.5$ produces a better response than $\alpha = 0$ and $\alpha = -0.5$ in terms of settling time. However, there is a limit beyond which over–compensation occurs and may result in an undesired overshoot as demonstrated by the plot for $\alpha = -3$ in Figure 4.12. Shift values that exceed a certain limit may eventually settle to steady–state but after experiencing undesired oscillations as shown in Figure 4.12 for the case of $\alpha = -10$.

Moreover, increasing the gain value may affect the overall gain of the feedback loop and cause instability which causes error signal to exceed the stable tolerance as shown for $\alpha = -15$. Therefore, there exists a range of values for $f(e)$ coefficients beyond which the system

goes either unstable or eventually reaches stability yet undergo undesired oscillatory response before reaching steady–state. Such oscillations may become completely unstable, hence, those values causing either instability or oscillatory response must be eliminated and a constrained stability region with minimum oscillation should be first found. Furthermore, within that stability range there exists an optimal value of $f(e)$ which guarantees an improved transient performance in terms of overshoots and settling time compared to the static PWM ramp (trace with $\alpha = 0$) as depicted in Figure 4.12. A proposed numerical algorithm for deriving the optimal shift value is discussed next.

In order to find the desired optimal shift value, first the system is expressed in numerical equations and the shift function is applied as an added value to the output of the compensator as discussed above Control Loop Implementation section and shown in Figure 4.13

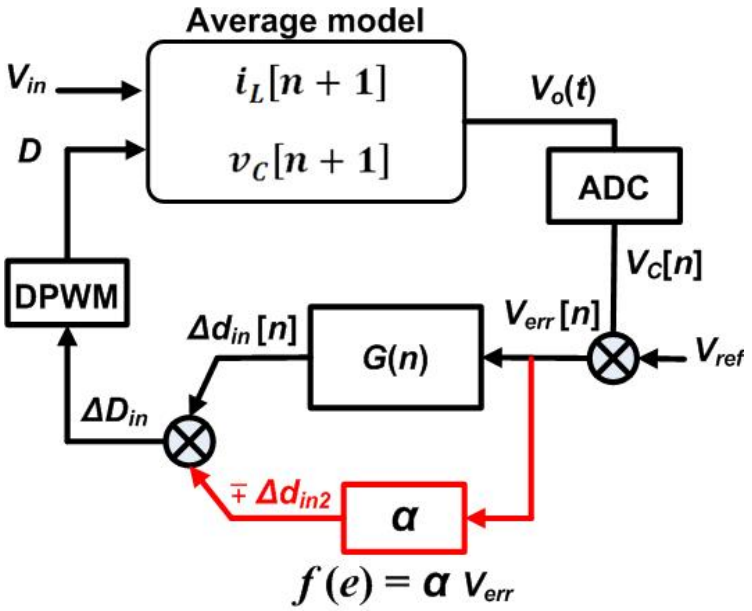


Figure 4.13 System representation in discrete domain

The average model is expressed using the set of difference equations representing the inductor current $i_L[n+1]$ and the output voltage $v_C[n+1]$ in Equation (4.9) in terms of: load R_o, filtering parameters: inductor, L, and output Capacitor, C, and maximum inductor current, I_{Lmax}, and maximum capacitor voltage, V_{Cmax}.

$$i_L[n+1] = I_{Lmax} - \frac{V_{Cmax}\,(1 - \Delta d_{in}[n]\,)\,T_s}{L} \qquad (4.9)$$

$$v_C[n+1] = V_{Cmax} + \frac{(I_{Lmax} - V_{Cmax}/R_o)\,(1 - \Delta d_{in}[n]\,)\,T_s}{C}$$

Whereas, the error signal is written in Equation (4.10)

$$V_{err}[n+1] = V_{ref} - v_C[n+1] \qquad (4.10)$$

where I_{Lmax} and V_{Cmax}. may be expressed by the following difference equations:

$$I_{Lmax} = i_L[n] + \frac{(V_{in} - v_C[n])\,\Delta d_{in}[n]\;T_s}{L}$$

$$V_{Cmax} = v_C[n] + \frac{(i_L[n] - v_C[n]/R_o)\,\Delta d_{in}[n]\;T_s}{C}$$

The total digital duty cycle command d_{in} which controls the closed loop behavior by generating an analog duty cycle signal through the DAC action of the DPWM is expressed in Equation (4.11)

$$d_{in} = d_{in\_comp} + \Delta d_{in2} \qquad (4.11)$$

Where d_{in_comp} is given by the compensator difference equation derived in Equation (4.8) whereas, Δd_{in2} is the result of the shifting function as in Equation (4.12) and only applied at transients

$$\Delta d_{in2} = e\ f(e) = e\ \sum_{i=1}^{n} \left(\alpha_i\ e^{\mathrm{i}-1}\right) = \sum_{i=1}^{n} \left(\alpha_i\ e^{\mathrm{i}}\right) \qquad (4.12)$$

The algorithm for obtaining the optimal shift function $f(e)$ begins with a first order linear gain, $n = 1$ which makes $f(e) = \alpha_1$ and $\Delta d_{in2} = \alpha_1\ e$. The numerical simulation starts by computing and determining the optimal value for the first coefficient α_1 . Once the optimal α_1 is obtained the algorithm updates the order $n = 2$ making $f(e) = \alpha_1 + \alpha_2\ e$ and $\Delta d_{in2} = \alpha_1\, e + \alpha_2\, e^2$, then α_2 is optimized around the previously best selected α_1 value. The system continues iterating to find best α_i value using all previous optimal values from α_1 to α_{i-1} .

Before proceeding to find the optimal value of the shift, it is first necessary to discard all values that diverges the system into oscillatory response or complete instability. Therefore, the range of the coefficient values that retains the system within its stability region is found in order to confine the algorithm to a bounded limit. Figure 4.14 shows the flowchart outlining the general procedure of limiting coefficient values to a bounded range that guarantees a stable response during transient, a linear first order function is primarily run, optimized then one higher order coefficient is added and accordingly tested.

The essence of the PWM shift function is the error signal in the sense of realizing that the purpose of shifting the PWM ramp is to minimize the error generated at transients by a value that depends on the error signal. This is the exact definition of a cost function needed for optimization practices; therefore, the optimal value is when the area under the error signal is minimal and the magnitude of the error signal decides whether the system is stable or not. Thus, both the availability and the magnitude of the error signal are crucial in all coming numerical calculations; the use of digital control makes the error signal easily obtained as in Equation (4.10). And the application of numerical simulation adopted in this work enables complex calculations.

Figure 4.14 first searches for the lower limit of the stability region then moves up to determine the upper limit; starting with a zero DC shift with $\alpha_1 = 0$. If the magnitude of the error signal is within the stability tolerance threshold, the DC shift value is decremented and the system is run under the new updated value, then the error generated is compared to the tolerance again and the value is incremented or decremented accordingly. The algorithm repeats until it reaches a lower limit for stability beyond which the magnitude of error exceeds threshold, then the search for upper limit is similarly achieved starting from $\alpha_1 = 0$ and incrementing until the whole stability range is determined and within which the search for optimal shift value is confined.

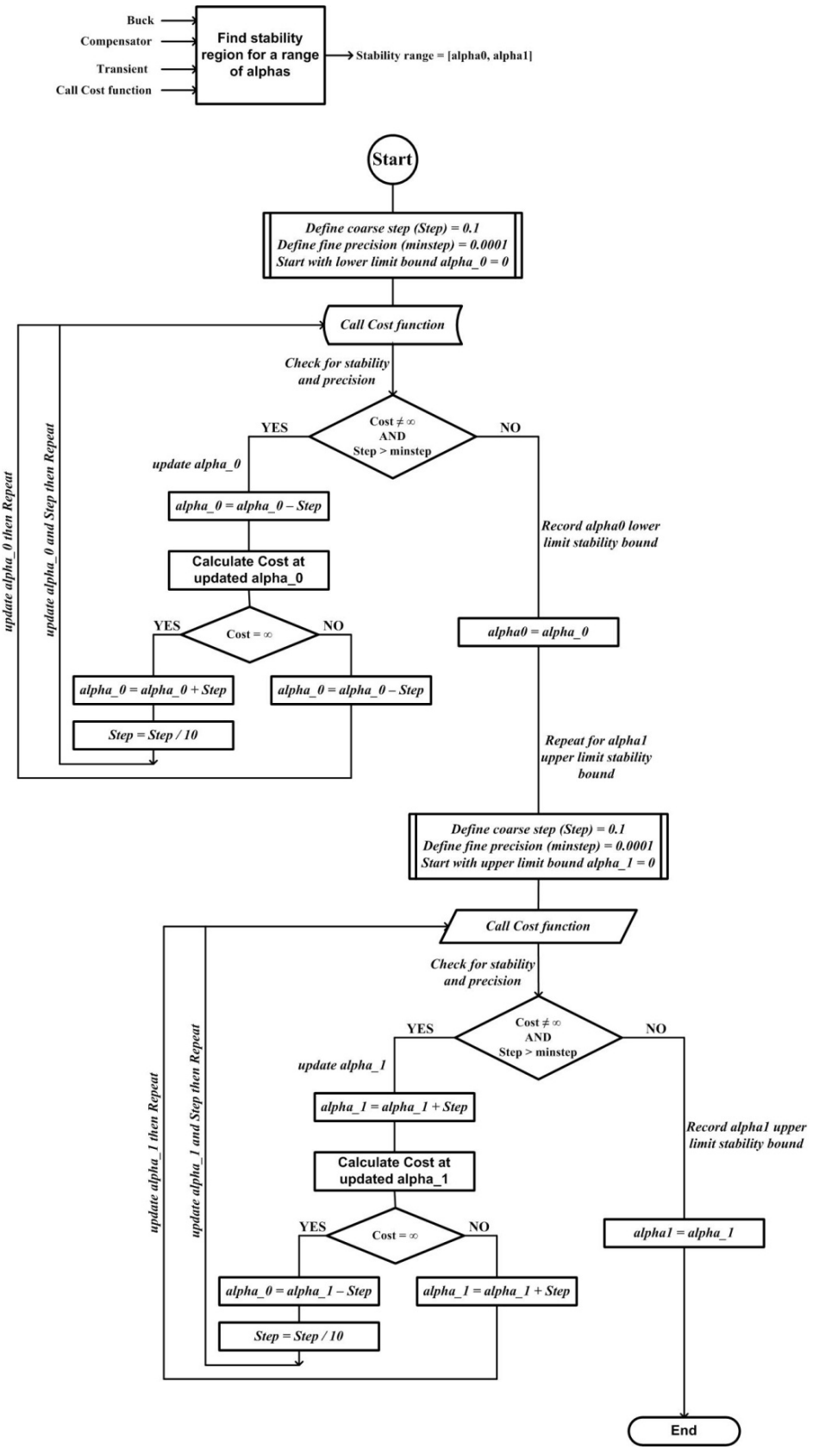


Figure 4.14 Flowchart to find lower and upper limit bound for alpha

Figure 4.14 gives an interval of DC shift values for first coefficient α_1 that satisfies system stability but still does not reject shift values which result in oscillatory response.

The Cost function called within the flowchart is shown in Figure 4.15.

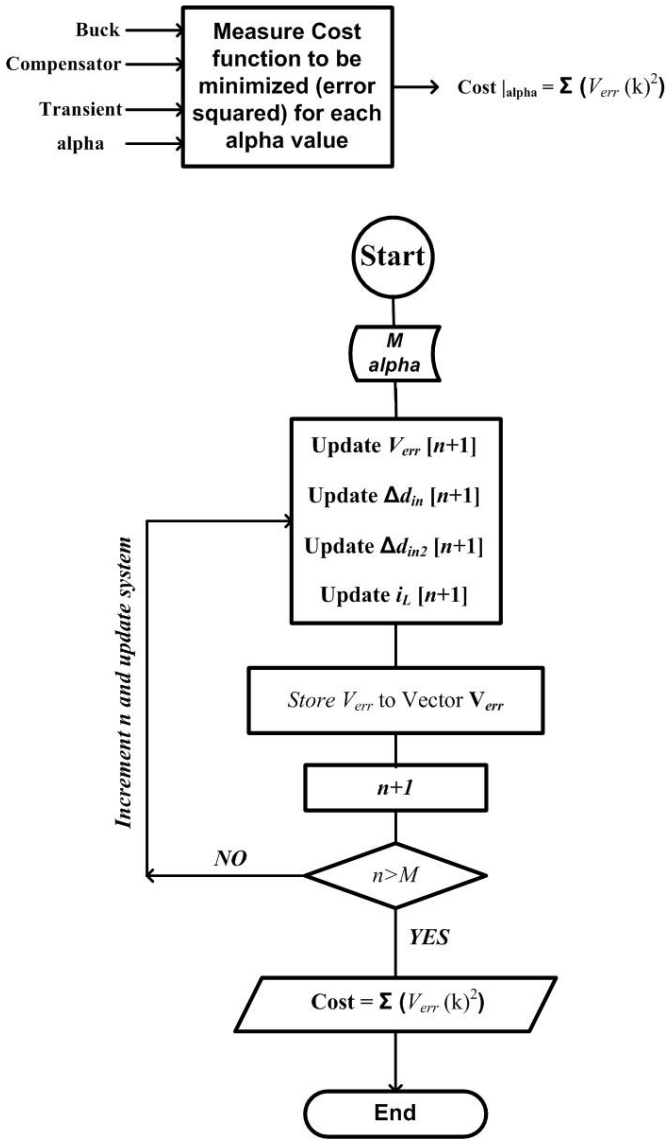


Figure 4.15 Flowchart of calculating Cost function for one or a range of shift values

Referring to the above design example illustration, running the stability region algorithm for a step–up load from the nominal 1A to 2A gives the range of α_1 equals to $[-12.057 \quad 0.825]$ for stable range of shift values.

Figure 4.16 plots the cost function versus shift values for all values of α_1. It is noted from the figure that the error magnitude goes to large values indicating instability for shift values less than $\alpha_1 = -12.057$ and larger than $\alpha_1 = 0.825$.

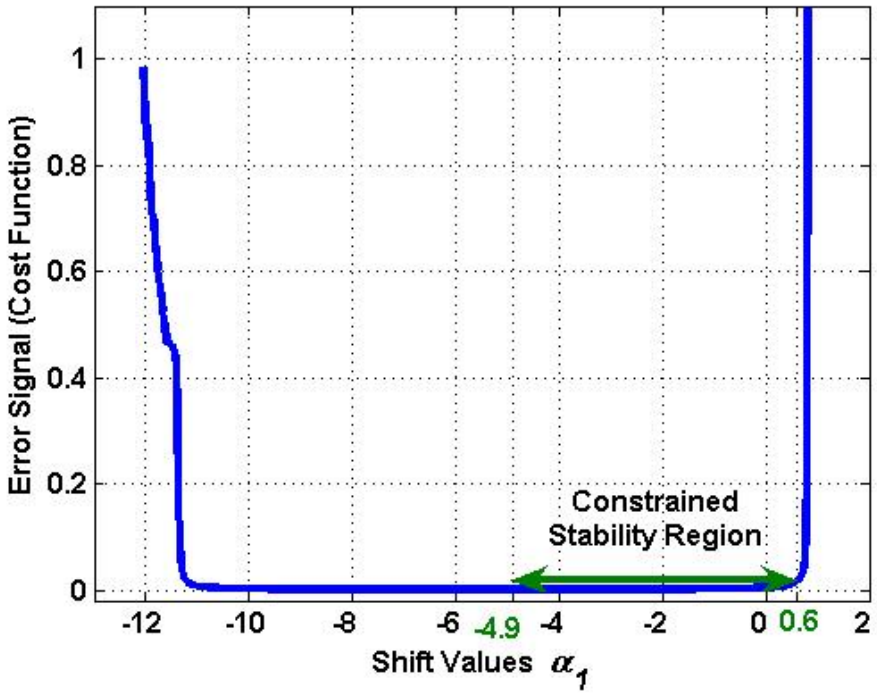


Figure 4.16 Stable values of α_1 for linear shift function versus error signal

Next, this region of stable α_1 $[-12.057 \quad 0.825]$ will be further refined to end up with a smaller range of shift values that guarantee complete stability which is within

$[-4.9 \quad 0.6]$ as indicated in Figure 4.16. Figure 4.17 gives the cost function for the complete stable region of α_1 $[-4.9 \quad 0.6]$.

From Figure 4.17 it is clear that the error signal, for the shift values beyond the upper confined stability limit $\alpha_1 = 0.6$, is not large enough to cause instability, it merely states that shift values greater than 0.6 and less than -4.9 yield a dynamic behavior with undesired oscillations before it dies out to steady–state.

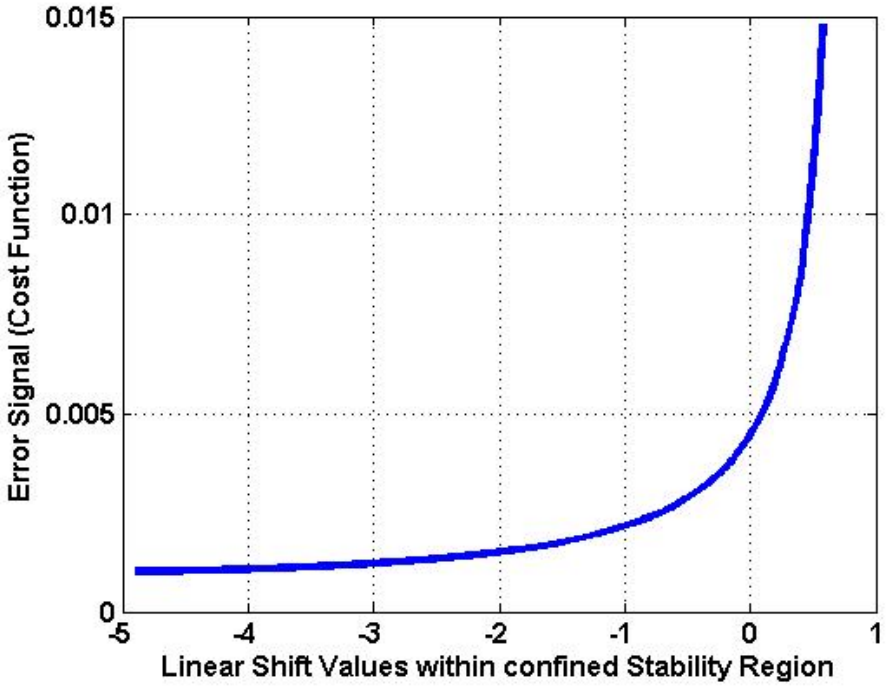


Figure 4.17 Confined stable values for shift function versus error signal.

At this point, the search for the optimal shift value that produces the best transient response which maps to the minimum cost function (minimum area under error curve) begins. Since

the parameters of interest are; settling time and overshoot, a desired transient behavior may vary depending on the application. In other words, a transient response with minimum overshoot which settles to a certain percentage of the reference value over many switching cycles might be considered a better response than one with less settling time and more overshoot. As a result, for a more useful approach the methodology of searching for the optimal shift value in the stability range depends on a user defined criteria for the two transient parameters of performance; settling time and overshoot.

Moreover, the fact that the first fast voltage undershoot due to sudden change in the load is highly dependent on the ESR of the filtering capacitors and is very hard to minimize, the attention in this work is focused on the second overshoot that is not exclusively circuit parameter dependent.

A numerical function is generated to sweep the confined stability range and for every shift value in that range the algorithm calculates both the settling time and the second overshoot using the flowchart in Figure 4.18.

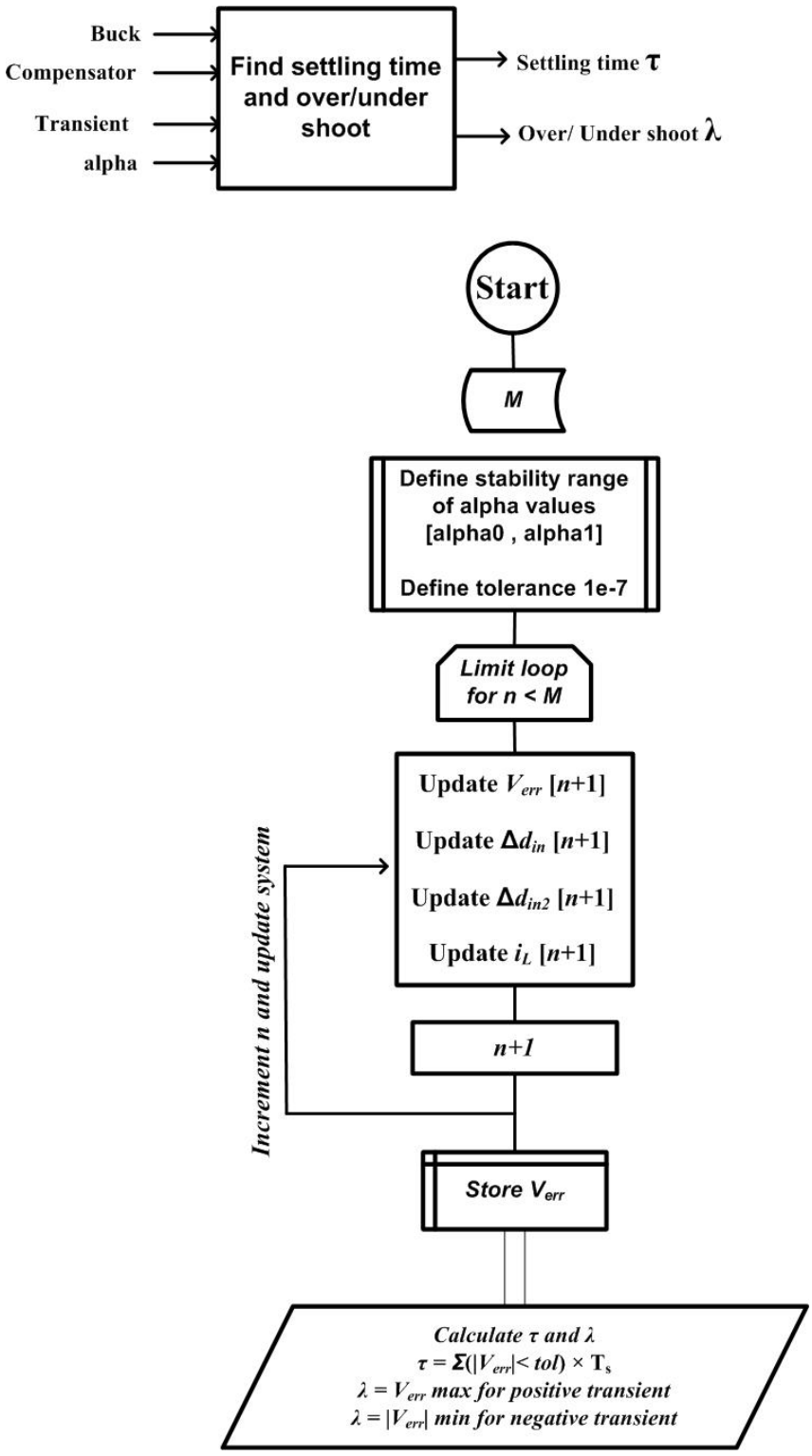


Figure 4.18 Flowchart of Calculating settling time and overshoot

Figure 4.18 outlines the steps to calculate and record the settling time with the overshoot along with the shift values.

Back to the system discussed above and for the same step–up load from 1A to 2 A, Figure 4.19 shows the settling times for all shift values within the confined stability range, whereas, Figure 4.20 plots the second overshoot for the same confined stability range.

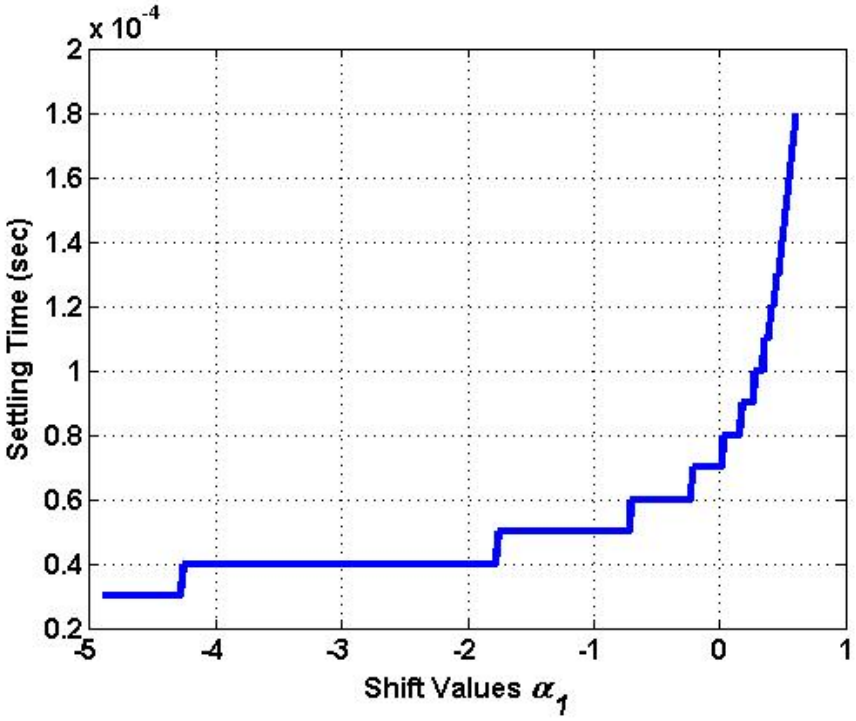


Figure 4.19 Settling time versus DC shift values within the confined stability range

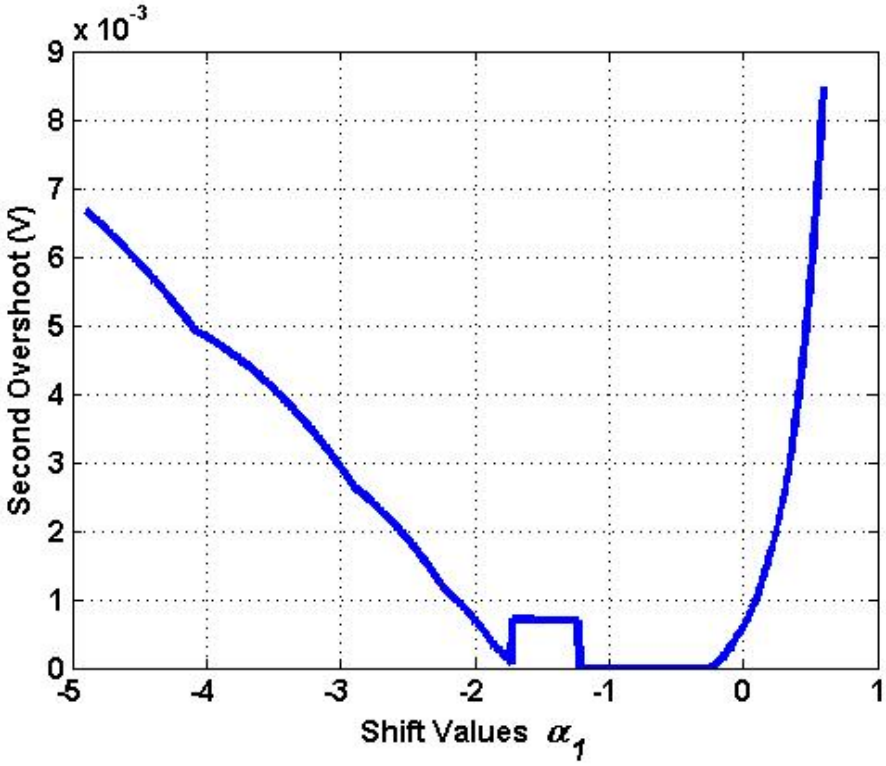
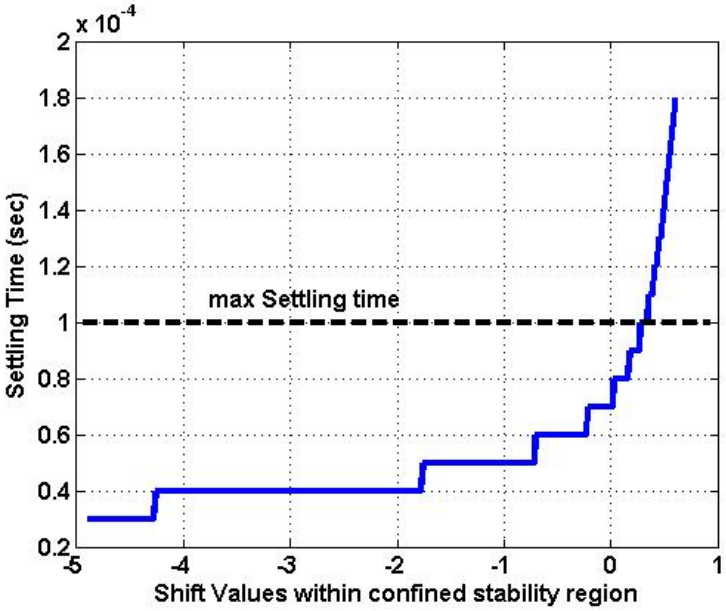


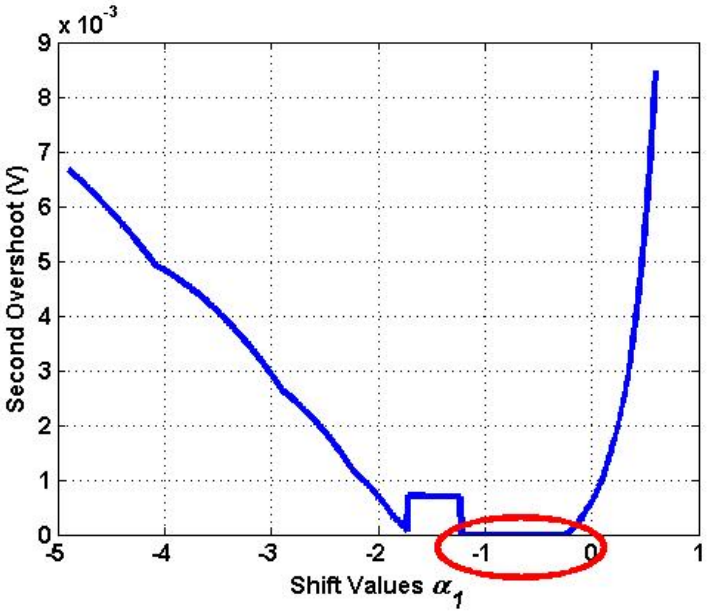
Figure 4.20 Overshoot versus DC shift values within the confined stability range

As can be noted from Figures 4.19 and 4.20, shift values that guarantee minimum settling time might not necessarily optimize overshoot as well. Therefore, it is very helpful to instead derive the optimal shift value in terms of not only minimum error but also a shift value that customize the transient behavior and guarantees a response with a maximum settling time and a maximum second overshoot set by the designer and depending on the application.

As a numerical example, the shift values that give a transient response with a maximum $100\mu sec$ settling time are in the range between $[-4.9 \quad 0.3433]$, and a minimum of no second overshoot $(10\mu V)$ are in the range between $[-1.2333 \quad -0.2433]$ as depicted in Figures 4.21(a) and (b), respectively.



(a)



(b)

Figure 4.21 Bounded limits set by the designer for (a) maximum settling time (a) maximum overshoot

Figure 4.22 plots the two parameters (settling time and second overshoot) together which makes it is easier now to identify the common range of $[-1.2333 \quad -0.2433]$ as the range of shift values which ensure a stable transient response with a desired settling time of no longer than $100\mu sec$ and with the minimal possible second overshoot of $(10\mu V)$.

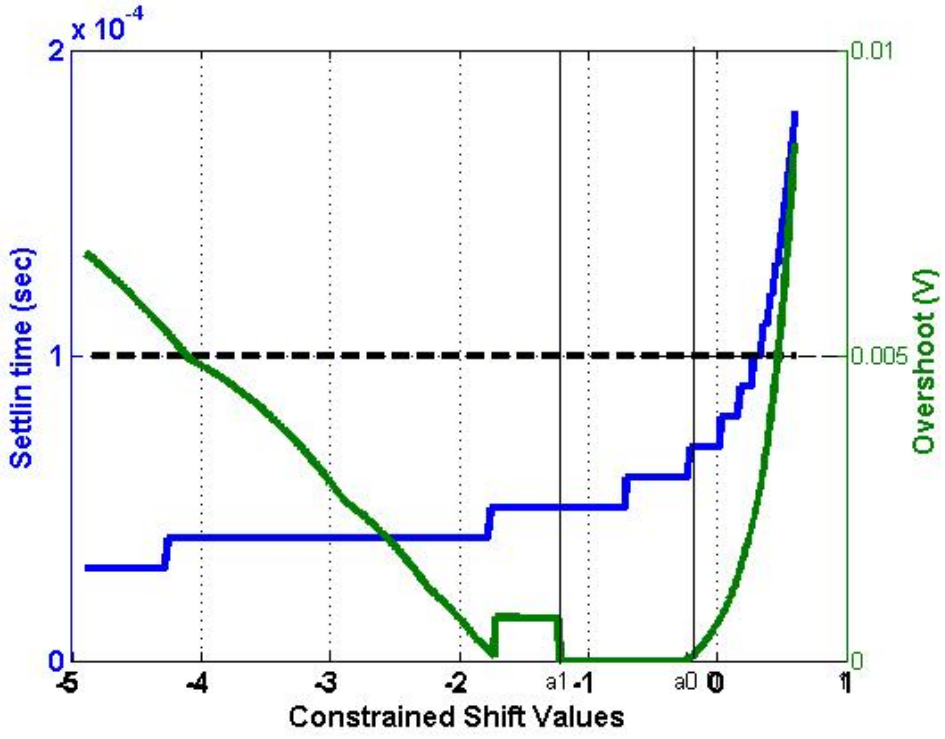


Figure 4.22 Settling time and second overshoot versus shift values

At this point, the search for the optimal shift value seems sensible since it is limited to the filtered–out refined stability range $[-1.2333 \quad -0.2433]$. A shift value once added to the feedback loop will ultimately result in a minimum cost function, as shown in Figure 4.22, in addition to a controlled dynamic behavior for given desired maximum settling time and second overshoot.

Applying the algorithm in Figure 4.15 within the range $[-1.2333 \quad -0.2433]$ gives $\alpha_{1\_optimzed} = -1.2333$ to be the optimal linear shift value for that specific designed compensator that guarantees a dynamic response with a minimum cost function (area under error signal) as confirmed through Figure 4.23.

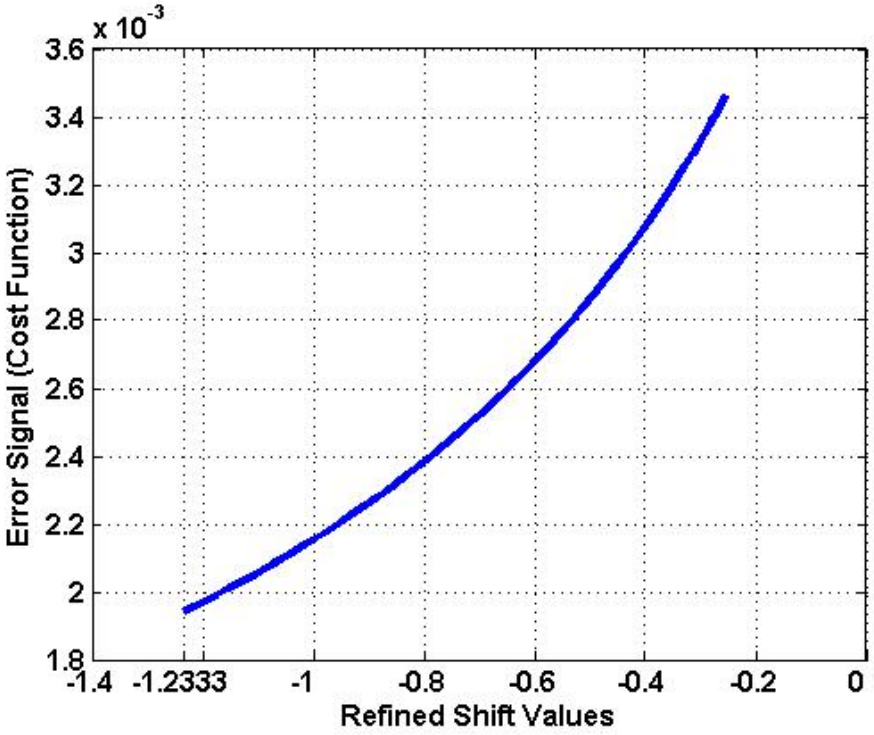


Figure 4.23 Cost function for refined shift values

Figure 4.23 verifies that the derived shift value $\alpha_{1\_optimzed} = -1.2333$ gives the minimum cost function and yields the desired dynamic response, which is furthered verified in simulation as shown in Figure 4.27 in Section 4.5 entitled "Simulation Results".

Next, is to consider expanding the shifting concept to include higher order non–linear PWM shift terms.

4.4.3.2 Non–Linear Higher Oder Shift

Considering that the linear PWM shift satisfies a desired transient response as shown above, the question would be why to move to higher order non–linear shift. Therefore, before moving any further, the effect of adding nonlinear terms into the shift function is first examined.

Figure 4.24 shows two plots for the cost function: one for a linear shift $f(e) = \alpha_1$ making $\Delta d_{in2} = \alpha_1 \, e$ and the second for one higher order term added $f(e) = \alpha_1 + \alpha_2 \, e$ making $\Delta d_{in2} = \alpha_1 \, e + \alpha_2 \, e^2$.

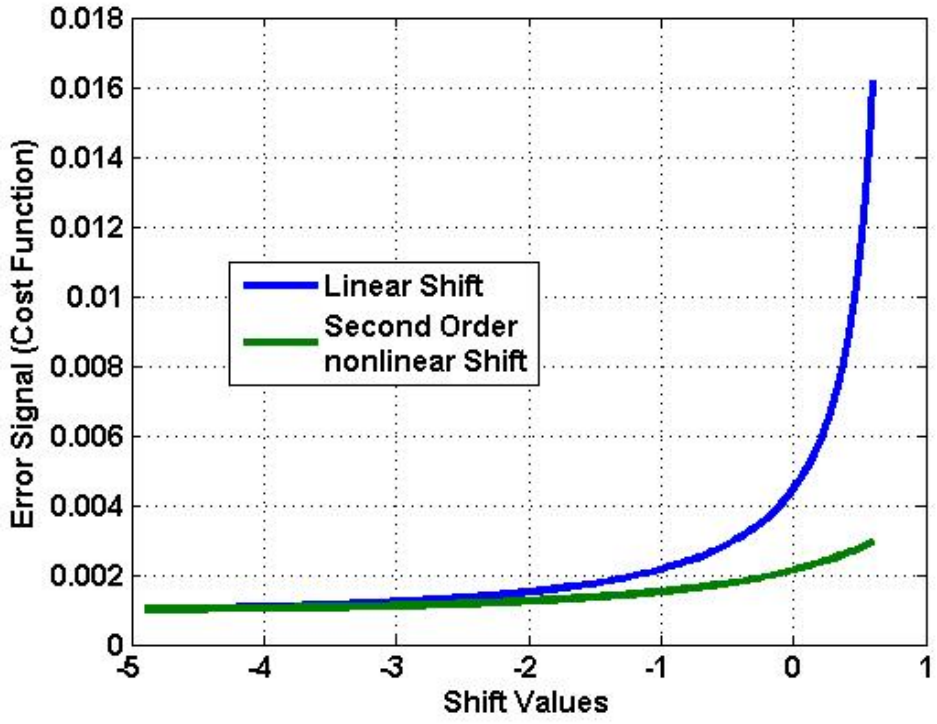


Figure 4.24 Cost function versus Order of shift function

Please note that the values for α_1 and α_2 are randomly chosen just to verify the advantage of using a nonlinear PWM shift which can be notably realized from Figure 4.24, where the cost function within the stability range is less for the second (non–linear) order than the first (linear) case. The search for the gain values of the nonlinear shift is discussed next.

4.4.3.3 Deriving the gain values for high order shift function

As described above, the finding of the optimal gain values for any shift function starts first with a linear optimization for α_1 in the linear shift function $f(e) = \alpha_1$ as detailed earlier. Afterwards, the order of the shift function is increased, with two gain values, $\alpha_{1\_optimzed}$ and α_2 as in $f(e) = \alpha_{1\_optimzed} + \alpha_2\, e$ and the optimization for α_2 is done around $\alpha_{1\_optimzed}$ following the same steps presented above for α_1, and so on with higher orders, $f(e) = \alpha_{1\_optimzed} + \alpha_{2\_optimzed}\, e + \alpha_3\, e^2$.

As previously derived in the design example, the confined stable region for the linear shift is $[-0.6 \quad 4.9]$, within which the filtered out range between $[-1.2333 \quad -0.3433]$ satisfies the designer's set criteria of a $100\mu sec$ settling time and with minimum second overshoot and the gain $\alpha_{1\_optimzed} = -1.2333$ was found to be the value with minimum cost. From this result, α_2 was added and accordingly, the confined stable region for α_2 with is $\alpha_{1\_optimzed}$ is now a wider range of $[-296.4 \quad 98.5]$. Among which the value $\alpha_{2\_optimzed} = -53.93$ gives minimum cost for the same desired transient response with $100\mu sec$ and no second overshoot $(10\mu V)$ as illustrated in Figure 4.25. Where the system

runs with the $\alpha_{1\_optimzed} = -1.2333$ and for different values of α_2, the error signal is plotted over α_2 values lying within stable range $[-296.4 \quad 98.5]$ derived from flowchart in Figure 4.15.

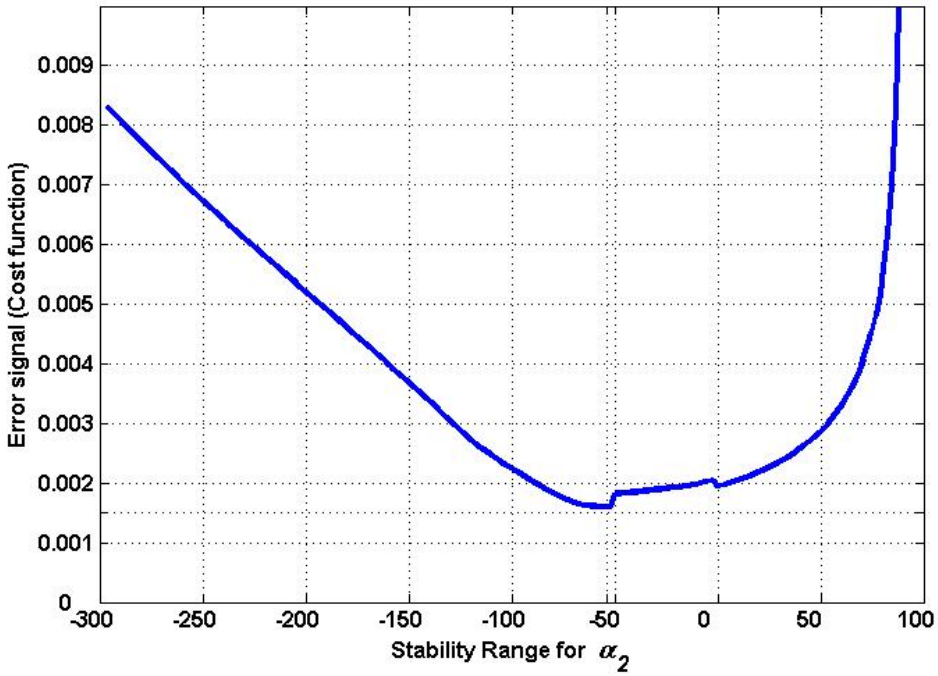


Figure 4.25 Cost function for $\alpha_{1\_optimzed}$ versus Second term of shift function

It can be noted from Figure 4.25 that the value for the second nonlinear term in the shift function α_2 using the optimized linear shift $\alpha_{1\_optimzed}$, which yields the minimum error corresponding to better dynamic behavior is at $\alpha_{2\_optimzed} = -53.93$ as supported below by Figure 4.26.

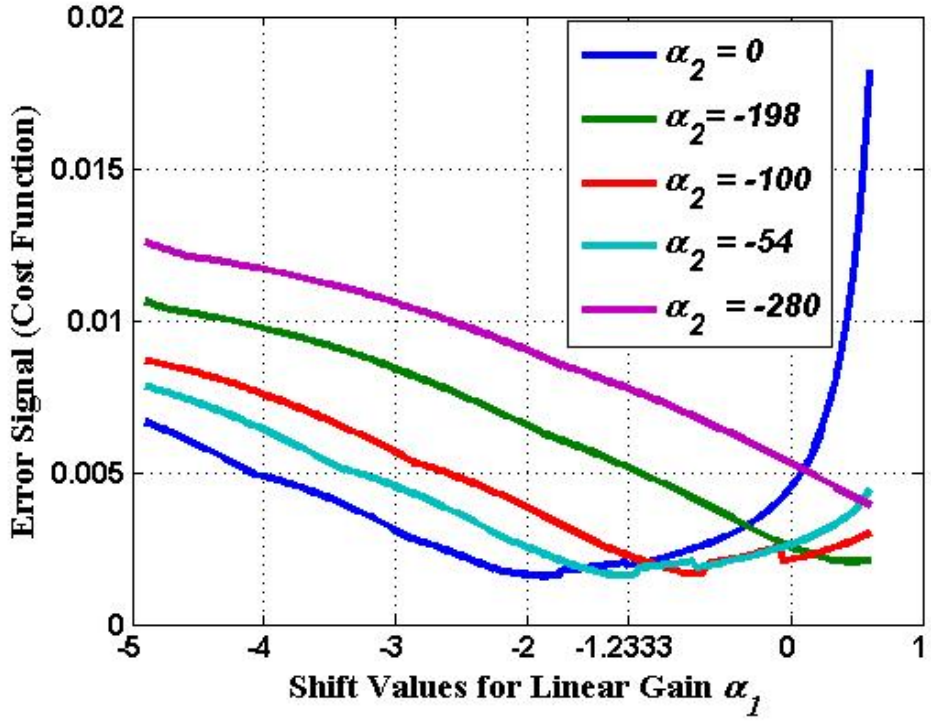


Figure 4.26 Cost function versus linear shift values α_1 for different α_2

Figure 4.26 plots the cost function versus the shift values for the linear term within the confined stability range for different values of α_2 . It is clearly noted from Figure 4.26 that the minimum error for $\alpha_{1\_optimzed} = -1.2333$ is for the derived $\alpha_{2\_optimzed} = -53.93$

Results are also confirmed with linear findings through simulation as discussed in the follow section.

4.5 Simulation Results

The numerical results derived in the previous section are verified through simulation using the average model of the power stage for the same design specifications and under the same transient used in numerical analysis. Results are shown in Figures 4.27 and 4.28 for the linear and second order non– linear shift function respectively.

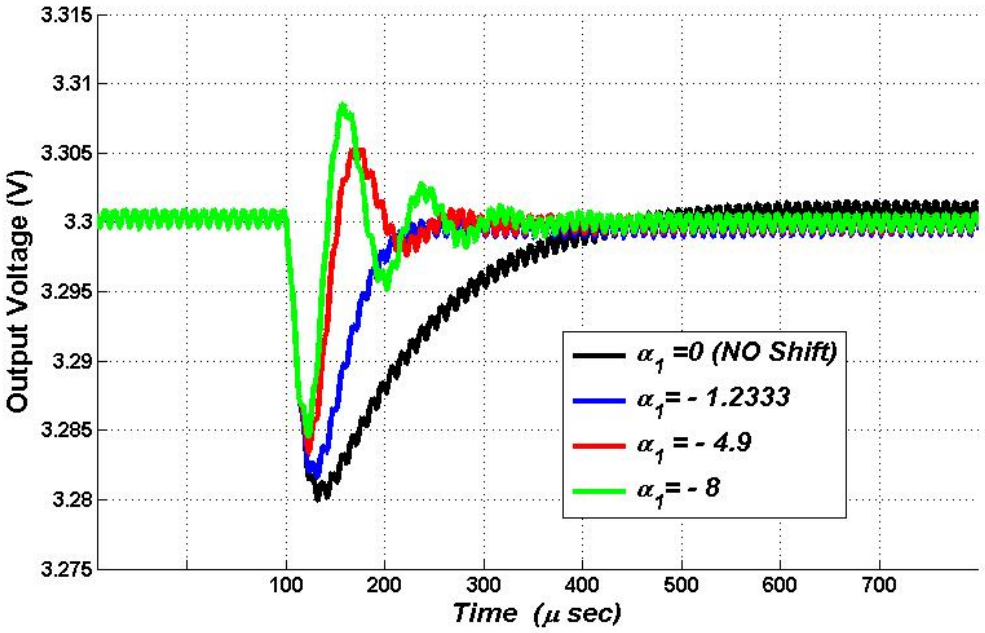


Figure 4.27 Output Voltage under 1A step–up with a linear shift

Figure 4.27 shows first, the improvement using the PWM shift technique during transients compared to the conventional closed loop (trace with alpha1=0). And second, that the desired transient response with the shift function is within the designer's specifications using the optimal gain with a linear PWM shift. Therefore, Figure 4.27 concludes the following:

1. The proposed PWM shift technique does improve the dynamic behavior at transient conditions as detailed previously.
2. The adopted numerical approach for finding optimal shift gain with pre–set transient behavior criteria proves accurate results.

Figures 4.28 and 4.29 demonstrates the results with a second order PWM shift.

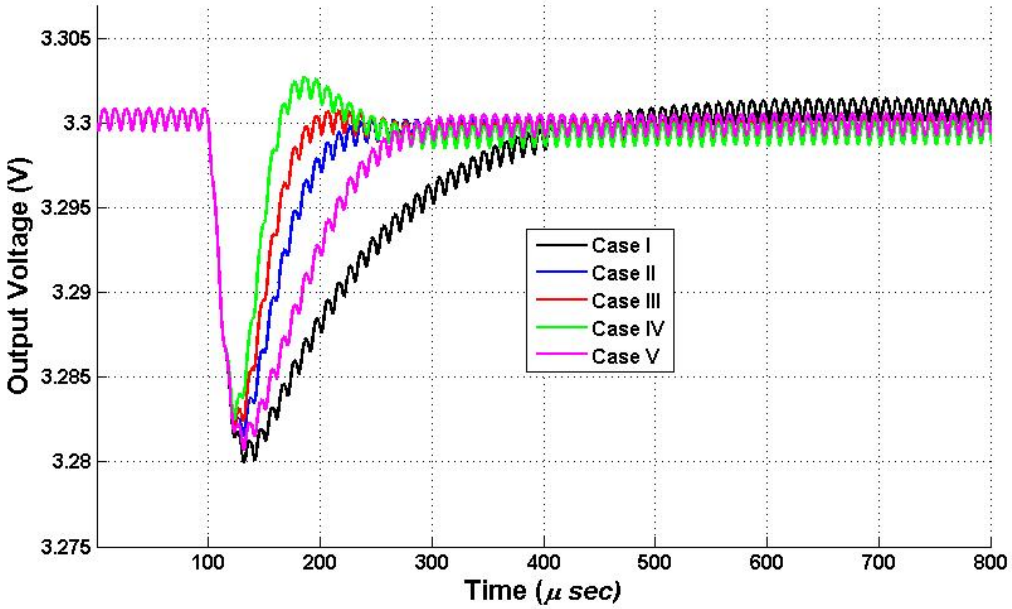


Figure 4.28 Output Voltage under 1A step–up for different gain values,

Figure 4.28 shows five traces, equivalent to the following five cases:

1. $\alpha_1 = 0$ and $\alpha_2 = 0$ corresponding to the conventional non shifting PWM.

2. $\alpha_1 = -1.2333$ and $\alpha_2 = 0$ corresponding to the linear DC shift with optimized α_1
3. $\alpha_1 = -1.2333$ and $\alpha_2 = -53.93$ corresponding to optimized second order non linear shift
4. $\alpha_1 = -1.2333$ and $\alpha_2 = -150$ corresponding to non optimized second order non linear shift for the second gain α_2
5. $\alpha_1 = -1.2333$ and $\alpha_2 = 50$ corresponding to non optimized second order non linear shift for the second gain α_2

Figure 4.28 confirms the improvement on the transient response by using the shifting technique over the conventional static PWM through comparing first trace, matching Case I– conventional no shift, with the other cases. Moreover, the derivation of the optimal shifting values proves correct where the trace corresponding to Case III ($\alpha_1 = -1.2333$ and $\alpha_2 = -53.93$) demonstrates best dynamic behavior.

TABLE 4.1 highlights the improvement of the transient behavior around optimized non linear shift values, in terms of shorter settling time and overshoot as shown in Figure 4.28 plus minimal cost as listed in TABLE 4.1.

TABLE 4.1
COST FUNCTION FOR DIFFERENT SHIFT GAIN VALUES

Case	α_1	α_2	Cost (10^{-3})
I	0	0	4.5
II	−0.5	0	2.9
III	−1.2333	0	1.9
IV	−4.9	0	6.6
V	−1.2333	−150	3.7
VI	−1.2333	−53.93	1.6
VII	−1.2333	50	2.9

In TABLE 4.1, Case I denotes the conventional static PWM and gives large error signal indicating a deteriorated dynamic behavior. Case III represents the optimized DC Linear shift with a less cost value compared to other linear shift of Cases II and IV signifying an enhanced transient response. Similarly, Case VI outperforms both the non linear shift with gain values other than the optimized shift value listed in Cases V and VII and also the linear shifting.

Figure 4.29 represents a clear improvement on the transient response moving from the conventional static PWM to the proposed DC linear shifting in addition to the superior dynamic behavior under the higher order non linear PWM.

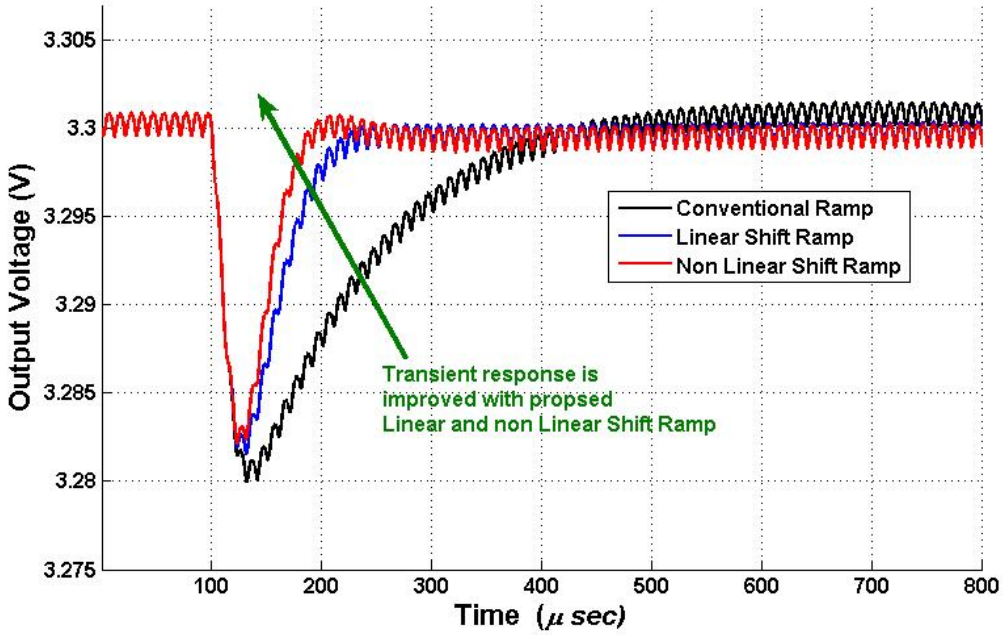


Figure 4.29 Simulation results for output voltage response comparing conventional ramp (Case I) with optimized linear (Case III) and optimized nonlinear shift (Case VI).

Therefore, the above results and findings confirm numerical analysis and simulation for the DC linear as well as higher order non linear PWM shift.

Finally, it is important to point out the distinction between the compensator–gain–variation and the proposed dc shifting techniques for improved dynamics. During transients, the dc shifting results in changing only one gain value outside of the poles and zeros of the already designed closed–loop compensator. Whereas, the traditional compensator–gain–control technique involves altering three gain values, i.e the coefficients of the zeros for a PID compensator. Hence, this requires more memory space and adds computational complexity when compared to the dc shifting technique. Stability is thus more likely maintained in the

linear shifting technique rather than varying three coefficients on which stability is directly measured by their location on the unity circle.

4.6 Experimental Verification

The simulation results were verified on a Xilinx FPGA environment platform and carried out on a Virtex4– board with XC4VSX35 device and FF668 Package. The power stage is designed based on the specifications presented earlier with the output is digitized using an ADC from TI ADS7881. Figure 4.30 shows the hardware setup.

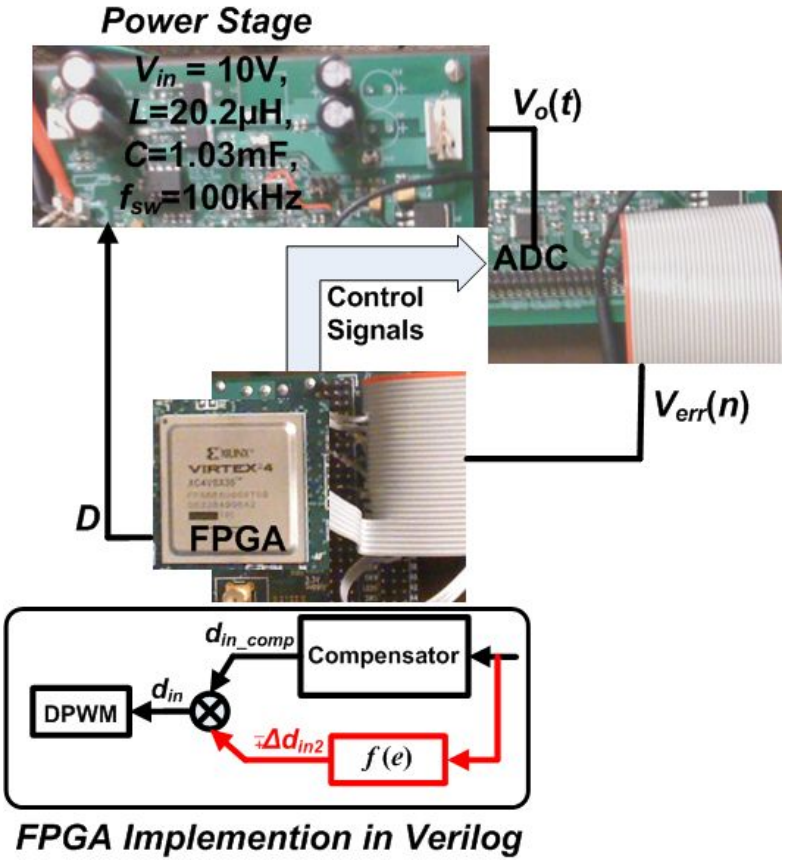


Figure 4.30 Experimental Setup

First we verified the linear shift by applying a 1A step–up sudden load change with $f(e) = \alpha_1$, using different values for α_1.The results are given in Figures 4.32 through 4.36, whereas Figure 4.31 demonstrates the response of a conventionally controlled converter with no shifting $\alpha_1 = 0$ for reasons of comparison.

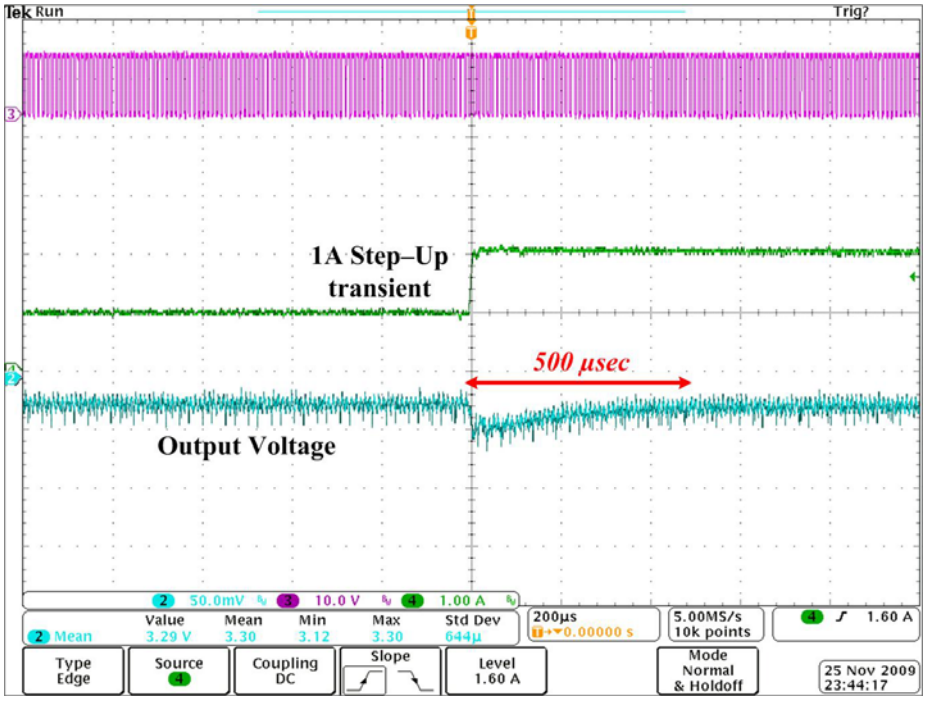


Figure 4.31 Output Voltage Response with no dc shift

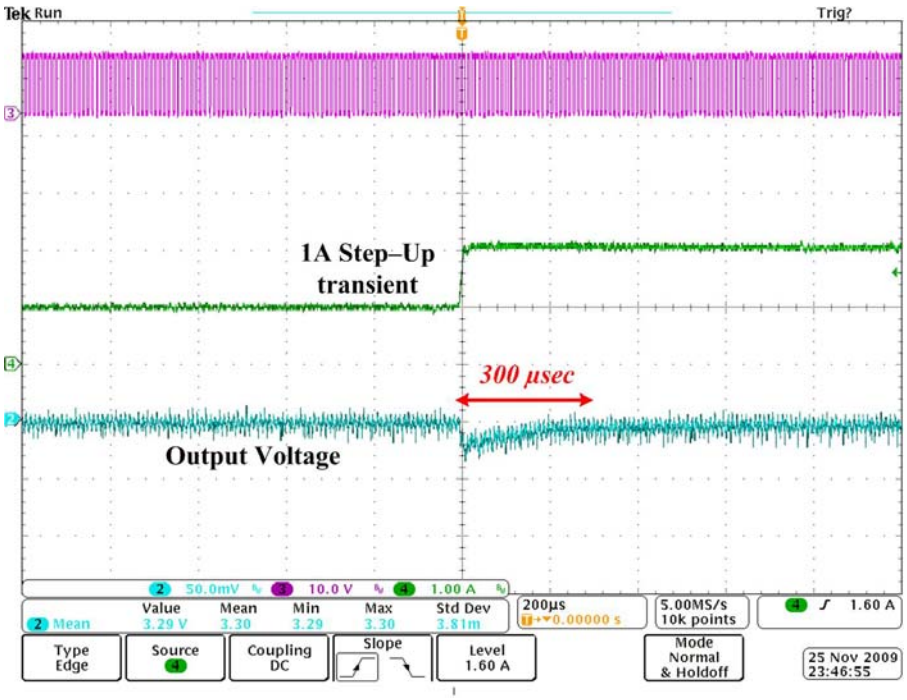


Figure 4.32 Output Voltage Response with linear shift of gain $\alpha_1 = -0.5$

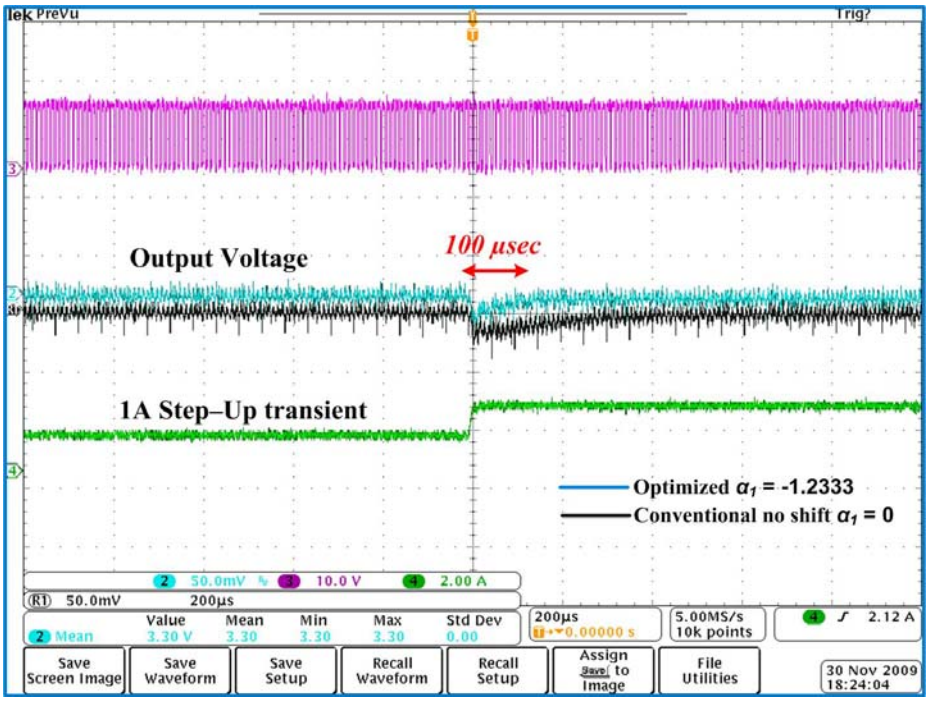


Figure 4.33 Output Voltage Response with optimized linear shift of gain $\alpha_1 = -1.2333$

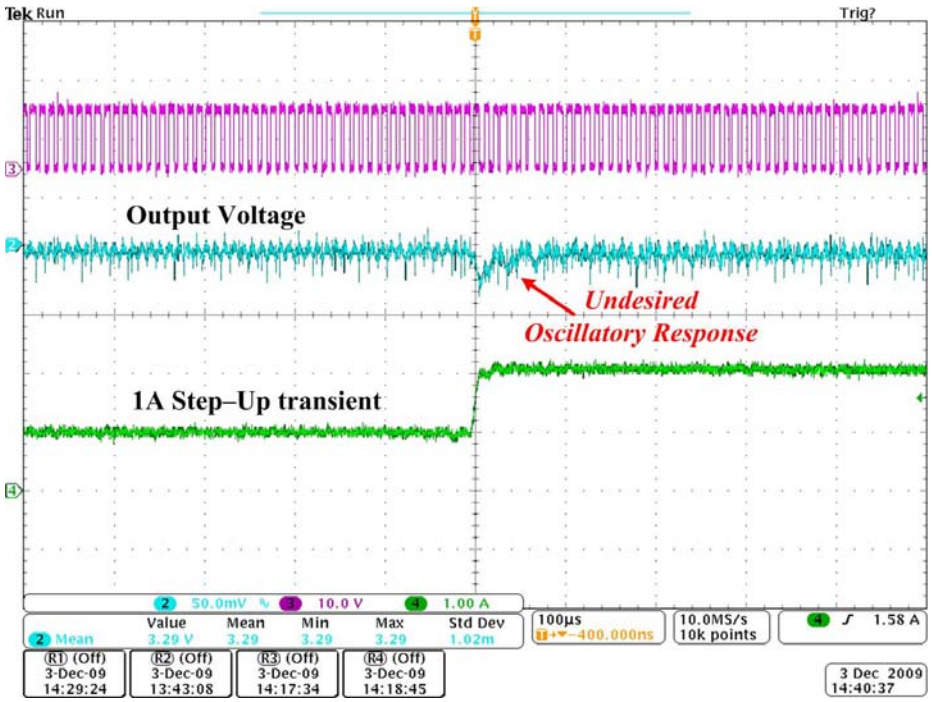


Figure 4.34 Output Voltage Response with linear shift of gain $\alpha_1 = -4.9$

TABLE 4.2 shows the best dynamic behavior in terms of settling time and minimum error is achieved using the optimized linear shift.

TABLE 4.2
DIFFERENT LINEAR SHIFT GAIN VALUES

Linear Shift Gain Value	**Experimental Settling time (µsec)**	**Cost (10^{-3})**
$\alpha_1 = 0$	500	4.5
$\alpha_1 = -0.5$	300	2.9
$\alpha_1 = -1.2333$	100	1.9
$\alpha_1 = -4.9$	150	6.6

Figures 4.35 and 4.36 show the experimental waveforms for the output voltage responses when compared to the conventional ramp with optimized linear and nonlinear shift cases.

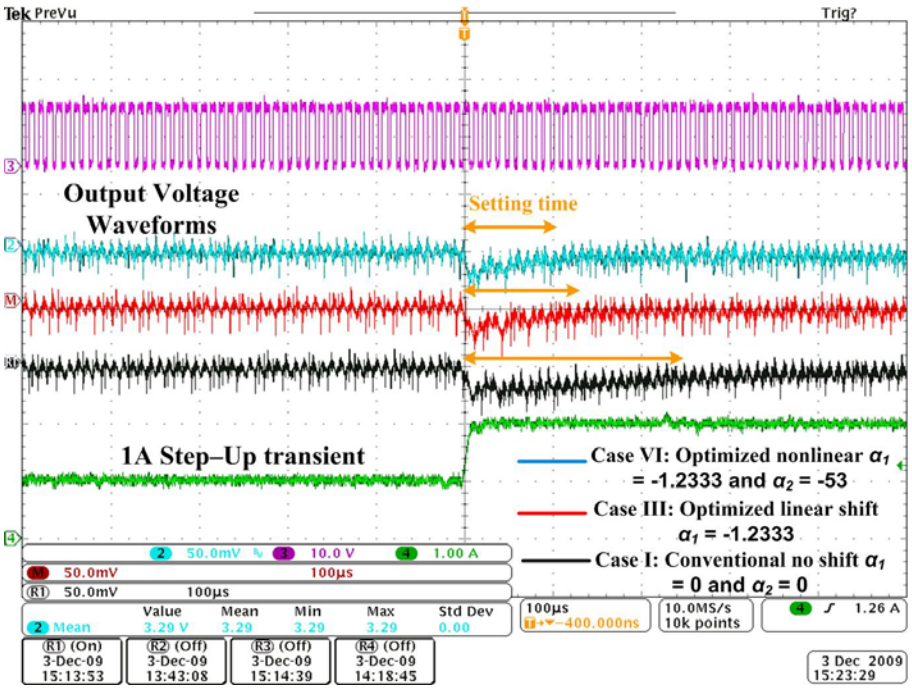


Figure 4.35 Output Voltage Response comparing conventional ramp (Case I) with optimized linear (Case III) and optimized nonlinear shift (Case VI).

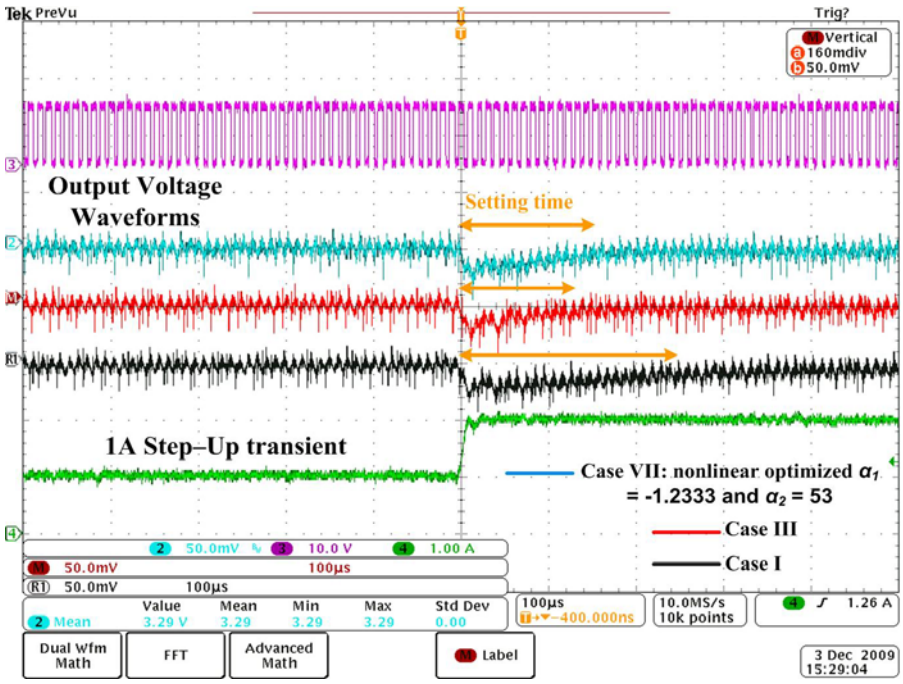


Figure 4.36 Output Voltage Response comparing conventional ramp (Case I) with optimized linear (Case III) and non–optimized nonlinear shift (Case VII).

The nonlinear shifting is summarized in TABLE 4.3 for several values of α_1

TABLE 4.3
DIFFERENT NON–LINEAR SHIFT GAIN VALUES

Linear Shift Gain Value	Non–Linear Shift Gain Value	Experimental Settling time (µsec)	Cost (10^{-3})
$\alpha_1 = 0$	$\alpha_2 = 0$	500	4.5
$\alpha_1 = -1.233$	$\alpha_2 = 0$	100	1.9
$\alpha_1 = -1.2333$	$\alpha_2 = -53.93$	80	1.6
$\alpha_1 = -1.2333$	$\alpha_2 = 53.93$	160	3.0

Again, significant improvement in settling time is obtained using non–linear PWM shift with optimized gain values under sudden load change from 1A to 2A. Similarly, Figures 4.37 and 4.38 illustrate the enhancement of the transient behavior with a higher load step of 4A. Figures 4.37 and 4.38 clearly illustrate the effect of both the linear and non linear dc shifting over the conventional static ramp for a larger load increase. It is noted as well that the optimized value for the linear gain is almost constant and is load independent whereas the value of the second term non linear gain is smaller for a larger increase.

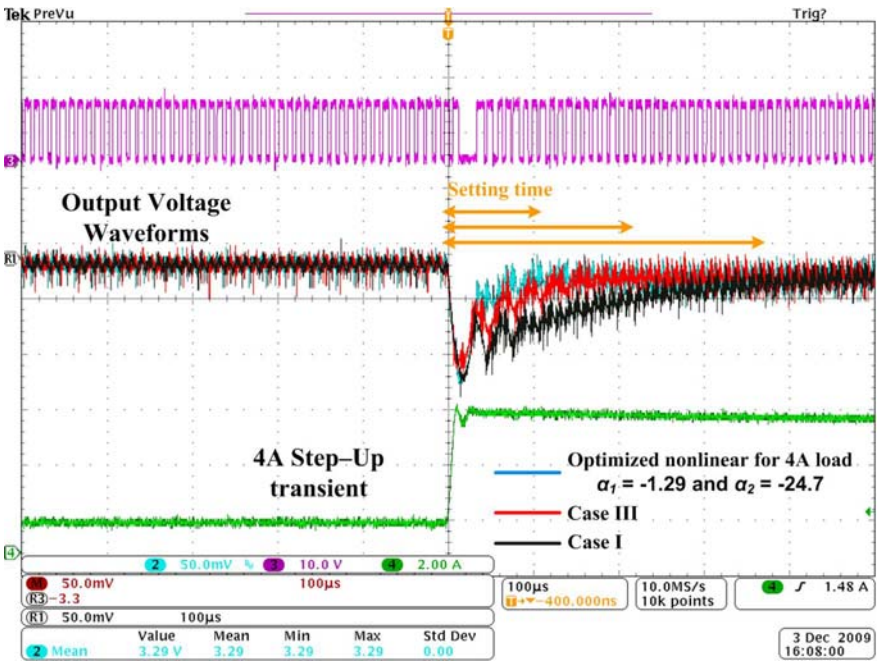


Figure 4.37 Output Voltage Response comparing conventional ramp (Case I) with optimized linear (Case III) and optimized nonlinear shift (Case VI) for 4A load increase.

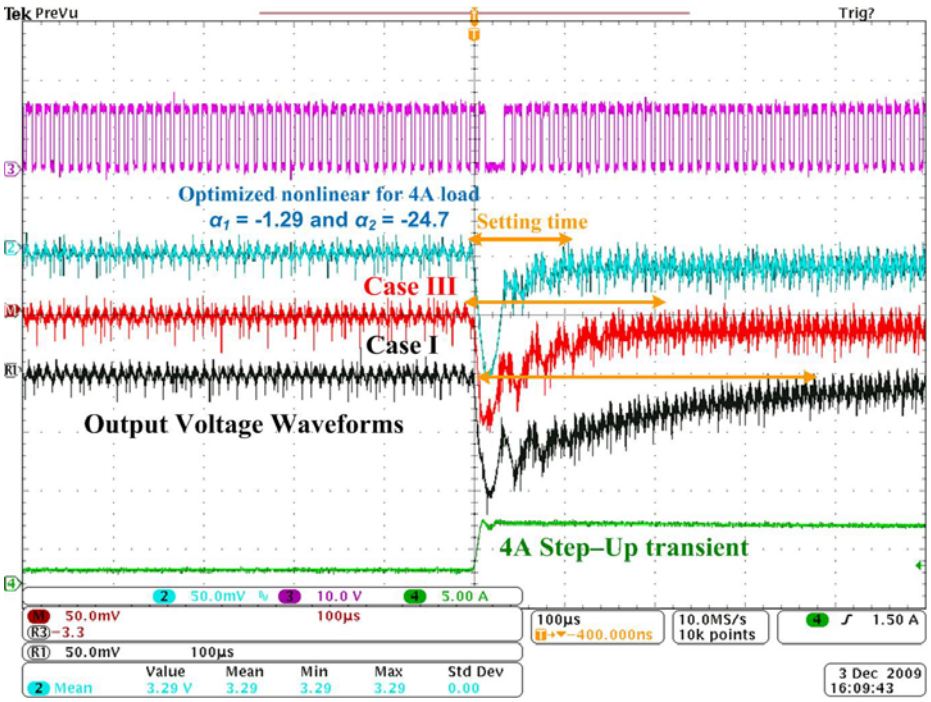


Figure 4.38 Improvement of non linear shift for 4A load increase.

It is clear that the experimental work confirms numerical finding to a great degree and verifies the proposed concept showing improvement of the dynamic response using optimal derived gain values for linear and non–linear PWM shifting. Moreover, the above experimental findings clearly match simulation results with slight differences due to the following reasons:

1. Numerical simulation is based on average model while experimental run a switch mode power converter
2. No dead–time in numerical simulation while there is $8\,nsec$ dead–time in experimental

3. Parasitics effects in resistance, capacitance and inductance in components, ICs and traces are not accounted for in theoretical and simulation analysis except for the series resistance of the inductance of $30\ m\Omega$.
4. Numerical simulation utilizes difference equations with no ADC or quantization effects.
5. A small delay between ADC and FPGA output.
6. Measurement noise from probes and use of long wires which add to voltage drops.

4.7 Conclusions

A new digital control technique for improved dynamics is proposed in this chapter. The control scheme dynamically shifts the ramp DPWM by a value depending on the error signal. The main advantage of the proposed architecture is helping the compensator reach steady–state faster by dynamically adjusting error deviation during transient while optimizing the system overshoot. This architecture utilizes existing system digital controller, and does not require any additional circuitry. The proposed design is verified using Xilinx Virtex4 board–XC4VSX35 FFG668 device. This control technique can be simplified using a linear shift or expanded to higher order non linear PWM shifting.

CHAPTER 5:
SUMMARY AND FUTURE RESEARCH WORK

5.1 Dissertation Summary

DC–DC control domain has notably moved from analog to digital for the advances the latter offers. Nevertheless, inherit characteristics of digital domain which analog techniques are free from, should be addressed for the full benefit of digital control. Limited resolution and sampling delays are of great interest to resolve specially at high frequency operation.

Furthermore, the ease and convenience of FPGAs facilitated their employment as implementation platforms. As a result, the many powerful resources on FPGA boards became also available to utilize and benefit from.

The work presented in this document exploits FPGA capabilities in order to achieve the following:

1- Increase the effective resolution of the DPWM unit for high frequency converters with maintaining low power consumption:

A novel FPGA Digital Clock Manager (DCM) based DPWM architecture was proposed in Chapter 3. It consists of two components: a linear counter–comparator and the DCM based component. The main advantage of the proposed architecture is the full utilization of the DCM resources already existing on FPGA boards at a reduced clock frequency when compared to the conventional DLL. Consequently, lower power consumption can be

achieved and thus, allowing for higher switching frequencies. The proposed architecture was verified using Xilinx Virtex4 board – XC4VSX35 FFG668 device, however, since the proposed DPWM structure uses DCM blocks and few other hardware resources such AND gates, Flip–flops and counters, it can be easily transplanted into other small–scale FPGAs or smaller devices of the same family with lower quiescent power for lower power consumption, giving more application–oriented design flexibility. Moreover, this architecture can be reconfigured to achieve different desired DPWM resolutions.

2- Enhance the dynamic response of DC–DC converters in terms of settling time and overshoot:

A new digital control technique for improved dynamics of digitally controlled DC–DC converters in terms of improved settling time and overshoot was proposed in Chapter 4. The proposed approach enhances the transient response by dynamically controlling the ramp of the Digital Pulse Width Modulator (DPWM) unit by adjusting the offset value of the conventional ramp–based PWM during load change. The shifting value can be a simple linear gain or can be expanded to include high order non linear terms; a complicated feature made effortless through the use of FPGA based controllers compared to analog implementation. The control scheme dynamically shifts the ramp DPWM by a value depending on the error signal. The main advantages of the proposed architecture include; enhanced dynamic response and fast transient behavior using fast FPGA implementation, helping the compensator reach steady–state faster by minimizing error deviation. This architecture also benefits from the advantages of the simplest counter–comparator DPWM which demonstrates best linearity among DPWM architectures. This technique utilizes existing system digital

controller, and does not require any additional circuitry. The presented control scheme was thoroughly analyzed, simulated and finally experimentally verified using Xilinx Virtex4 board–XC4VSX35 FFG668 device.

5.2 Future Work

In this section, a new concept is presented that is based on dynamically adjusting the system clock in DPWM to help improve efficiency while achieving high switching frequency in DC–DC Converters.

5.2.1 Introduction

Today, DC–DC converters are operating at switching frequencies exceeding tens of MHz, resulting in a new set of challenges that open new research fields in Digital Pulse Width Modulator unit (DPWM) [40 – 62, 117 – 129].

Many DPWM architectures are presented in literature including: counter–comparator, delay line, hybrid DPWM, segmented delay line, dithering, etc. to name a few [17 – 18, 28, 43 – 45]. Each of the existing DPWM architectures has some advantages and disadvantages depending on the application as previously detailed in Chapter 2.

A look into the power consumption of the existing DPWM architectures is of great benefit in order to come up with DPWM architectures suitable for MHz switching frequencies and minimized power consumption.

The high linearity offered by the counter–comparator based DPWM is counter–parted by its high power consumption at higher switching frequency.

The Delay Line technique helped decrease the power loss at the expense of large area while the Hybrid approach combines the Counter based and Delay Line as a compromise between the power loss and the area.

The losses are calculated according to Equation (5.1):

$$P = \sum_{i=1}^{N} \alpha_i \, C_{in} \, V_{dd}^2 \, f_{clk} + \alpha_i \, I_{sc} \, V_{dd} + I_{Leakage} \, V_{dd} \qquad (5.1)$$

where,

α: The probability the gate is active.

C_{in}: The input capacitance of the gate

V_{dd}: The gate drive voltage

I_{sc}: The short circuit current

$I_{Leakage}$: The leakage current

The higher the switching frequency and the gate drive voltage the higher the power consumption numbers are, which negatively affects the efficiency.

Research efforts have been directed into investigating MHz switching frequencies for buck converters, along with, emerge new design challenges.

In order to achieve high efficiency at high switching operating converters, the DPWM unit requires in depth studies.

The action of the DPWM can be viewed as a Digital to Analog Converter (DAC), converting the output of the compensator to duty cycle values and operate the switching network of the DC–DC converter. The least significant bit of the DPWM determines the minimum change in the duty cycle. Thus the resolution of the DPWM is very critical in deciding the accuracy and the overall performance of the converter.

In other words, the DPWM resolution is an important factor in deciding the steady–state as well as the dynamic responses of the system. A more accurate performance entails high resolution DPWM. The higher the resolution, the higher the cost and the higher the sampling frequency required which can prove to be impractical, particularly at high switching frequency. Thus, research has been dedicated into increasing the accuracy of the system without exaggerating in the resolution of the DPWM unit.

5.2.2 Proposed Control Technique

The resolution of the ADC and the DPWM blocks decide to a great extent the efficiency of the overall system. For a high resolution DPWM, a fast oscillator clock is required which

increases the power consumption. The hypothesis is the following: fast clock and thus high resolution is only needed in the steady–state range, whereas outside that range, the clock and the resolution can be saved at low values with no effect on the performance of the system, as shown in Figure 5.1.

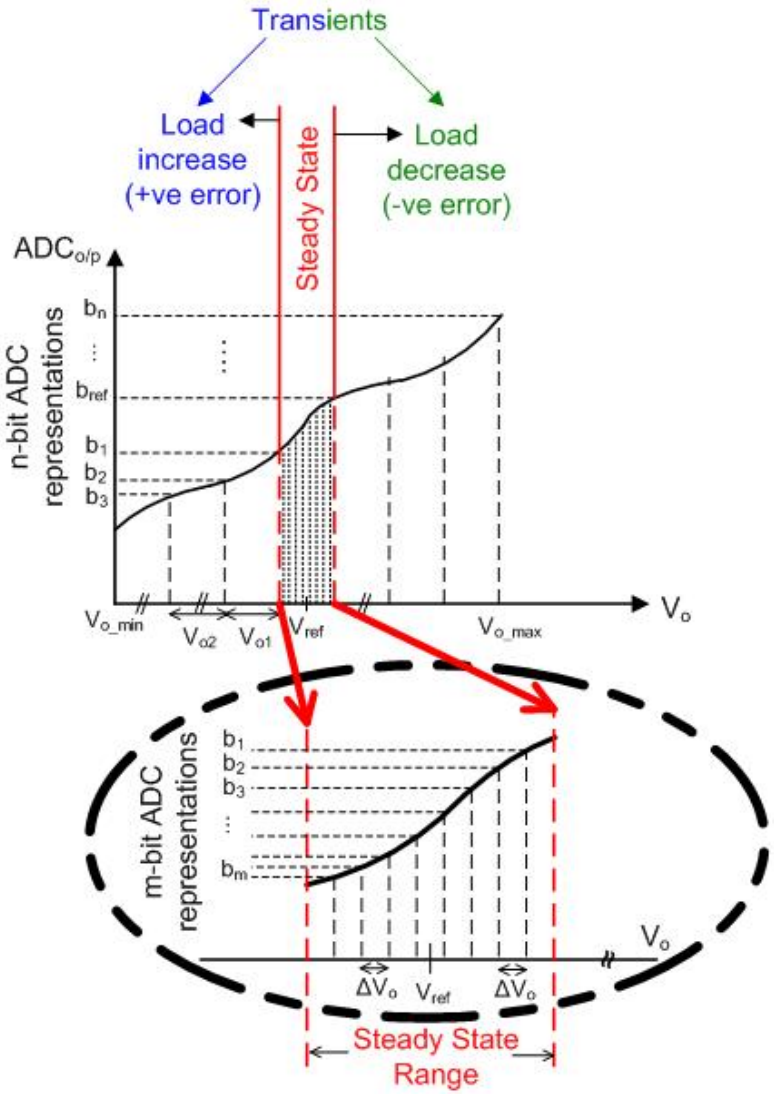


Figure 5.1 Irregular Resolution Concept

Figure 5.1 illustrates the concept of irregular resolution, the output of the ADC $\left(ADC_{o/p} \right)$, is a fixed set of values, $n - bit,\ \ b_n$ depending on the resolution of the ADC and the range of the output voltage sensed.

As noticed from Figure 5.1, the resolution of the ADC during steady–state $ADC_{ss-step}$ $(m - bit)$ is dictated by the minimum resolution of the output voltage determined by system requirements, with $m > n$ and is calculated using Equation (5.2);

$$ADC_{ss-step} = \frac{V_{ADC\ max}}{2^{m\ ADC}} < \Delta V_o \qquad (5.2)$$

$ADC_{ss-step}$: is the maximum voltage at the input of the ADC $(V_{ADC\ max})$ divided by the number of output voltage representations $(2^{m\ ADC})$ and this should be smaller than the minimum resolution required at the output voltage (ΔV_o).

Using Equation (5.2), the $m - bit$ ADC resolution during steady–state can be calculated and the resolution of the DPWM should be higher to avoid limit cycle problems.

Again, during transients the resolution of the ADC can be lowered to $n - bit$ since the output voltage needs to be quickly relocated to the steady–state range. Either the ADC resolution or the sampling frequency can be lowered during transients. In the latter case, the resolution of the ADC can be maintained unchanged in both the steady–state and transient modes.

The full range of the output voltage is drawn versus $n-bit$ ADC as shown in Figure 5.1. Where, V_{o_min} (minimum output voltage) corresponds to the resultant load voltage at maximum load variation and V_{o_max} (maximum output voltage) matches the load voltage at minimum load during step up and step down transients respectively. Also, the reference voltage V_{ref} is a fixed number that can be represented as a discrete value of b_{ref}.

The proposed control technique first distinguishes the mode of operation, steady–state or transient, and treats each case separately: if the value of the sensed output voltage lies outside the steady–state range $(V_{o\_ss}\, range)$ then, a transient condition is detected and the coarse resolution ADC $(n-bit)$, which requires a slow clock, is applied during the transient to drive the output voltage back to the steady–state range as quickly as possible to alleviate the spikes that result at the load due to the transients.

Figure 5.1 also illustrates the two techniques of sampling the output voltage and assigning discrete values for each sample, i.e., if the sampled value of the output voltage lies in the V_{o1} range, which is outside the steady–state range, an $n-bit$ ADC assigns to it a digitized value of b_1. The error signal resulting from the difference $e_1 = b_{ref} - b_1$ is thus calculated.

Similarly, if the sampled value of the output voltage lies in the V_{o2} range, a discrete representation of b_2 is assigned to it and an error signal e_2 is produced.

The function of the compensator is to process the errors and generate a duty cycle value such that the difference between the sensed output voltage and the reference value is zero. And accordingly a digital value of the required duty cycle is sent from the compensator to the DPWM, it is then compared to a ramp waveform and an analog duty cycle is generated that sets the output voltage equal to the reference.

Since a coarse resolution is applied during transients, the variation in duty cycle will be larger compared to the conventional regular resolution ADC.

As explained above, first; the mode of operation is to be checked. A decision needs to be taken according to the $n - bit$ representations of the sensed value of the output voltage; if the output voltage is outside the steady–state range, a slow clock and low resolution DPWM is applied to quickly and roughly retrieve the output voltage and take it back to the steady–state range where then a fine tuning algorithm using a finer $m - bit$ ADC with an accurately designed compensator based control loop sets the output voltage precisely at the reference value. Thus, the low resolution during transients should be able to more or less re–place the output voltage in the region of the steady–state range which is then directly followed by the steady–state fine tuning algorithm as shown in Figure 5.1.

At a zero error signal, the output voltage is equal to the desired reference value and the steady–state duty cycle at the output of the DPWM is set to a value D_{ref} equal to D.

The proposed counter–comparator DPWM is as shown in Figure 5.2.

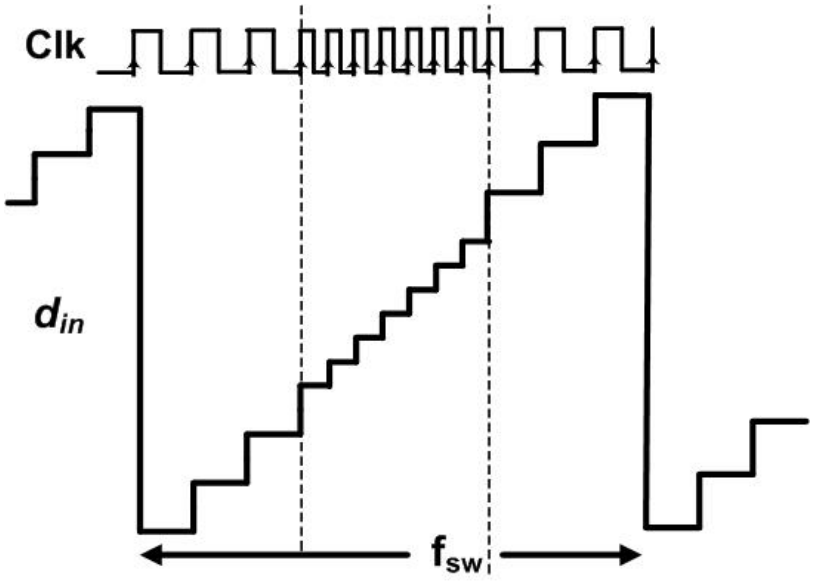


Figure 5.2 Dynamically Clock–Adjusted DPWM

A fast clock and thus a high resolution DPWM is only needed during the steady–state region, whereas a slow clock and coarse resolution is sufficient outside the steady–state region. As a result, the savings in clock and consequently power loss outside the steady–state region in the proposed dynamic clock–adjusted digital ramp architecture makes it possible for converters to operate at high switching frequency with high DPWM resolution and yet improved efficiency.

The anticipated advantages reaped out of this control structure are the following:

1. During transients, a coarse sampling of the output voltage will be adequate in order to generate a duty cycle that takes the deviated output voltage back to the steady–state range.

2. Enhanced dynamic response due to the fast recovery from load transients via the use of the coarse resolution DPWM and followed by fine tuning.

3. Reduced power consumption due to reduced clock requirement and thus a promising solution for a high switching converter.

This section is intended to present the proposed concept of dynamic clock–adjusted digital ramp architecture. This control technique is primarily addressing clocking requirements and power consumption at steady–state in addition to the dynamic response of digital converters during transients.

5.2.3 Suggested work for proposed concept

1- Detailed analysis for the whole system with the adjusted clock within the steady–state and dynamic regions. The projected analysis should include power calculations estimating the losses as well as savings. In addition to balancing the benefits with emerging control complications.

2- Targeted simulation of the proposed control scheme with various clock adjustments inside steady–state region and outside with exposing the system to various degrees of transient conditions.

3- Experimental validation of the proposed concept.

5.2.4 Conclusions

This chapter proposes a new DPWM architecture designed to operate at high switching frequencies. The dynamic clock–adjusted digital ramp is presented as an improved version of the counter–comparator, it benefits from the best linearity and simplest architecture offered by the conventional counter–comparator DPWM, nevertheless it adjusts the clock and thus the resolution in order to lower power consumption which was originally the barrier to high switching operation. It is a direct emulation of the conventional ramp PWM signal except for the constant resolution; the proposed dynamic clock–adjusted digital ramp utilizes fast clock and thus high resolution in the steady–state region and a slower clock with lower resolution outside that region. The anticipated savings in the power consumption due to slower clock oscillator will make the use of the simple architecture counter–comparator DPWM suitable for high switching operations. In addition to improved dynamic response due to using a slower ADC outside the steady–state region.

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