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FRONT-END CONVERTER DESIGN AND SYSTEM INTEGRATION TECHNIQUES IN DISTRIBUTED POWER SYSTEMS

by

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A dissertation submitted in partial fulfillment of the requirements
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Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
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Summer Term
2001

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ABSTRACT

Power conversion system design issues are becoming increasingly important in state-of-the-art electronic systems, especially in computing and information system applications. These issues include not only improving power conversion efficiency, but also increased concerns regarding the cost and complexity of the power converters and systems utilized to satisfy the host system's total performance requirements. Further, system integration techniques, which can be used in "building blocks" to implement a wide range of power electronic circuits and systems, will be taking a critical role to innovate conventional designs and also bring profound effects into practical applications.

This dissertation explores front-end converter design and system integration techniques in distributed power systems (DPS), with the objective of achieving improvements in converter topology, system performance, system configuration and cost-effectiveness over conventional approaches. Key issues of single-stage (S^2) power-factor-correction (PFC) converters are addressed and the solutions to these issues are investigated. An optimization design procedure of a family of S^2 converters, which is based on the averaging circuit model and MathCAD tool, is developed and verified by both simulation and experiment. A new PFC cell is presented with the direct-power-transfer (DPT) concept, and a new family of S^2 converters is derived and experimentally verified, which has excellent characteristics that help push S^2 converters into medium power applications. A comparison study of high power down converters is conducted, and in particular, experimental comparison of high power level for secondary-side

topologies is completed in this dissertation, which demonstrates that the current doubler rectification topology is a viable choice for high-efficiency converters. The dissertation also investigates system level techniques such as interleaving, paralleling and configuration simplification. New interleaving method for high power converters is presented and simulated results demonstrate its potentials in decreasing filter size and increasing power density. New paralleling methods for power converters have been obtained based on the comprehensive classification and evaluation of paralleling approaches of power supply modules. The dissertation also describes the operation principle, design considerations, and experimental results of an AC-DPS with multiple PWM-wave buses. Finally, a redundant AC-DPS with trapezoidal waveform bus is proposed.

To my grandparents and parents

ACKNOWLEDGMENTS

My four year stay in the U.S. has created an important literary piece of not only my research life but also my ideological reformation shaped through experiencing unnumbered horrific nights, but fantastic years, also through hardships and triumphs of study and research.

I sincerely thank my advisor, Dr. Issa Batarseh, for giving me the opportunity and confidence to work towards my Ph.D. degree at UCF, and providing me with a pleasant and productive research environment. In particular, his warm personality and friendship made my experience at this university one of the most cherished experiences of my life. Although my graduate study at UCF had experienced the hardest years and unexpected developments, his strong encouragement and wholehearted support have become my original power and pushed me to achieve my dream. Without his great help and supervision, this dissertation would never be born.

I wish to express my sincere appreciation to Dr. Fred C. Lee, who gave me the opportunity to enter the states, working as a visiting professor in Center of Power Electronics Systems (CPES, former VPEC) at Virginia Tech., from middle 1997 to end 1998, with which I had chance to know so many power electronics folks. I also thank the following CPES peers, Profs. Dan Y. Chen and Alex Huang, Drs. Hengchun Mao, Xuening Li, Xiaogang Feng, Zhihong Ye, Wei Chen, Lizhi Zhu, Liang Wang, Xunwei Zhou, and Mr. Xinsheng Zhou, Bo Zhang, Mr. Heping Dai, Dayu Qu, Yuhui Chen, Yongxuan Hu, Qun Zhao and Jianwen Shao for their constant care and friendship.

I also wish to take this opportunity to thank my former advisor, Prof. Zhencheng Hou, for bringing me into the wonderful field of power electronics.

I would like to express my gratitude to my research buddies Drs. Huai Wei Guangyong Zhu, and Chris Iannello, for sharing with me for many of valuable technical discussions, and unforgettable time we spent together.

I would also like to express my particular appreciation to Mr. Weihong Qiu, Mr. Lei Hua and Dr. Peter Kernetzky, who provided the help needed in implementing experimental verifications. Special thanks are also expanded to my close study fellow Dr. Wei Gu, as well as my old colleagues Drs. Zhixiang Liang and Jun Chen for beneficial technical arguments.

I gratefully thank FloridaPEC's faculty member, Dr. Thomas X. Wu, who gave me much encouragement toward my Ph. D. degree. To my other advisory committee members, Dr. Xin Li, Dr. Wasfy B Mikhael and Dr. Louis C. Chow, thanks for the patient, the passion, and their feedbacks.

Thanks are due to the many UCF staff who made the program and work possible, particularly for Ms. Mickey Gravois.

I am indebted to all my fellow students at UCF. Their friendship has made my stay in study & research program enjoyable. Especially, I thank FloridaPEC's members, Dr. Wenkai Wu, Jabber A. Abu Qahouq, Manasi Soundalgekar, Jia Luo, Yaomin Yang, Enrique Tenicela, Abdelhalim M. Alsharqawi, Khalid Rustom and Shailesh Anthony and Joy Mazumdar, for the valuable technical discussions.

Above all, I would like to express my deepest gratitude to my wife and son, Huaiying and Maozhe, who have been standing by me with their honest follow and also with their determined courage together sharing the life stress and struggling fruits.

This work was supported by NASA, NSF and the University of Central Florida.

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1. INTRODUCTION

1.1 Background and Motivations

Power conversion system design issues are becoming increasingly important in state-of-the-art electronics systems, especially in computing and information system applications. However, the basic power architecture in current electronic systems remains the same as it was decades ago [1,3]. Many of current power architectures are no longer effective in terms of performance and/or cost. For example, current stand-alone "silver box" designs in computers are unable to meet transient voltage regulation requirements for future computer systems. As a result, post-regulators (known as voltage regulator modules or "VRM") are being developed. The power processing combination of the silver box and VRM is used to meet the future microcomputer's stringent power quality requirement, as shown in Fig. 1-1. However, VRM performance (e.g., efficiency and transient response) is constrained to the limitations imposed by the silver box outputs. A power processing structure where there are several conversion steps in series will lead to an inefficient overall power system design, accompanying a relatively larger size and weight [4,5]. A target area for reducing the power system cost is to eliminate and/or simplify as many conversion steps as possible. This is especially true in light of the more stringent power system performance objectives that lie in the future computer system design [2-7].

Also, it is very difficult to optimize the VRM design to further improve efficiency. The size is also difficult to reduced. It utilizes a large amount of input and output capacitors that contribute to the most part of the volume of VRM. In addition, another drawback to the power system architecture shown in Fig. 1-1 is its inflexibility. As a particularly important issue for high-availability/fault-tolerant computing systems (e.g., workstations and servers), this inflexibility causes the following profound impacts [8-11]:

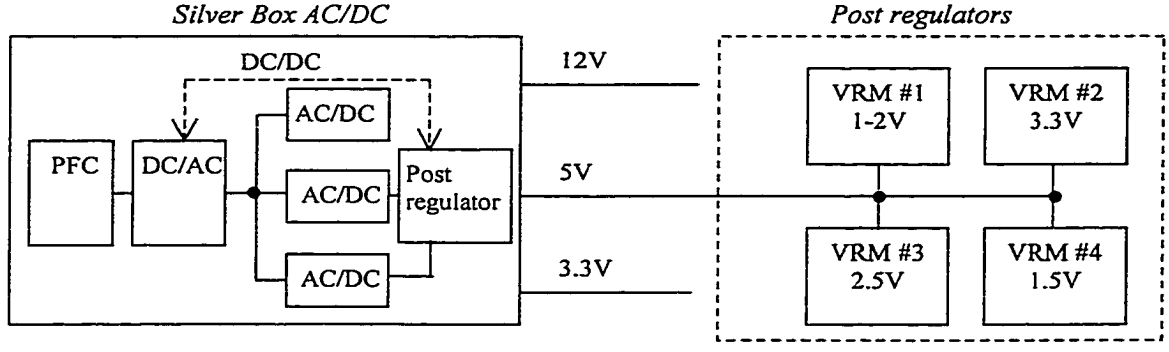


Fig. 1-1. Power processing combination scheme using silver box and VRMs for future generation of computers.

1) As system power level increases, the distribution of multiple low-output voltages becomes impractical and the silver box efficiency suffers.

2) Non-isolated VRMs may lead to potential difficulties with ground loops, load-fault isolation, and system noise levels.

3) The power backup function at the output side of the silver box in the power system is complicated, primarily because there is no common output bus.

4) A fault-tolerant system design requires a redundant silver box, and this implies high system cost and complicated power architecture.

Solutions to the above problems can be found in distributed power system (DPS) structure [1,2,7-17]. Today's power system in electronic equipment is actually a hybrid system. As we see it, the trend toward distributed power and away from centralized power is being forced upon the industry because of the use of ICs with lower voltages and higher clock rates. The next decade projection from the Semiconductor Industry Association points out the need for efficient supplies with less than one volt output that can handle the load of processors with giga-hertz clock rates. Distributed power can meet this need because it provides better point-of-load voltage regulation than centralized power for high-speed, low-voltage microprocessor. However, the jury is still out on deciding exactly what distributed power system design approach should be followed [1-5].

Broadly speaking, there are two possible distributed power approaches: AC-bus or DC-bus. The DC approach employs an intermediate DC voltage, say 48V, which is distributed to multiple DC-DC converters in system. In the AC approach, an intermediate high frequency AC voltage (might be 48V) is distributed to each AC-DC power supply in the system. The DC outputs of load converters may range from 1V to 12V for computer system applications.

A typical DPS architecture with 48 Vdc bus is shown in Fig. 1-2. Generally, four to five power conversion steps are required to obtain ideal electrical specifications to meet load need from an AC line input. One way to reduce the power system cost is to eliminate and/or simplify as many conversion steps as possible. It is expected that this will be the trend in future power supply system design. Compared to the above power processing approach-combination of the silver box and VRM, with a 48 Vdc bus, VRM

efficiency can be improved by as much as 3% [4,5]. Not only is the VRM efficiency improved; but also the accompanying I^2R loss is decreased in distributing power to the VRMs from silver box.

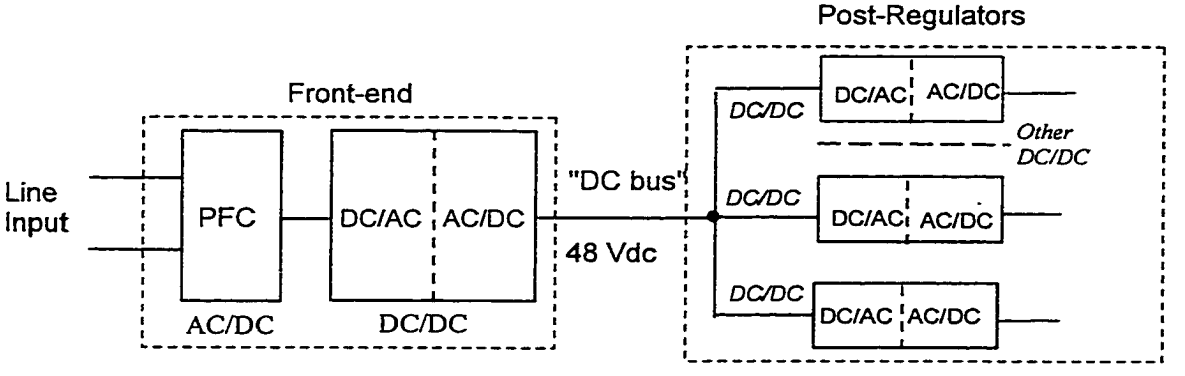


Fig. 1-2. A typical architecture of DC distributed power system.

In fact, the DC-DPS is not a new concept, as it has been used extensively in mainframe computer systems, communication systems, aircraft, fighting jets, warships, phased-radar arrays, and space vehicles, and lately been used in the construction of the international space station [7-12]. In the system of Fig. 1-2, although the front-end design is now simplified, the power architecture in the system still requires five conversion steps (an inner AC/DC or DC/AC as a step) to process power from the AC line to the system loads. Three of these conversion steps reside within the front-end converter. Therefore, it becomes a natural target for further simplification [18-24].

DC-DPS system has been an improvement over supply system of Fig. 1-1. However, the complexity of the DC-DPS shown of Fig. 1-2 can be further simplified by using high frequency AC-DPS structure. As shown in Fig. 1-3, AC/DC conversion step in front-ended DC/DC stage and DC/AC conversion step in post-regulator of Fig. 1-2 are

eliminated, i.e., two out of five power conversion steps that may be removed. The resultant AC-DPS structure, if successful, can be expected to have less components and higher efficiency [31-45].

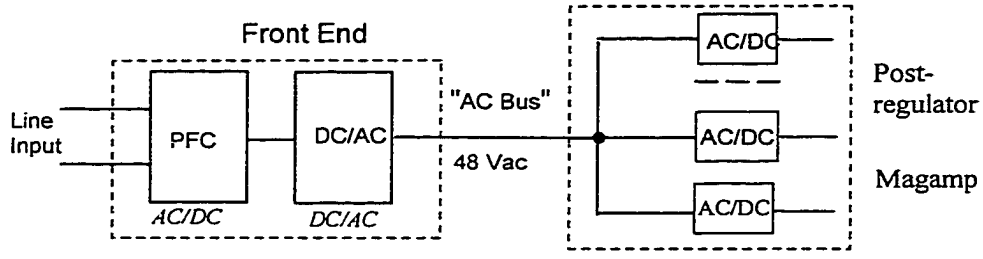


Fig. 1-3. A typical architecture of AC distributed power system.

From a structural complexity viewpoint, we believe that the proposed AC-DPS shown in Fig. 1-3 is a significant improvement over the DC-DPS counterpart system shown in Fig. 1-2. These two systems have a common feature that the front-end converters in DPS with AC or DC bus are implemented with two-stage schemes to meet stringent power factor and harmonics regulations. In this two-stage scheme, an active power-factor correction stage (usually boost converter) is adopted as first stage to force the line current track the line voltage. The second stage is a DC/DC converter in a DC-DPS and a DC/AC inverter in an AC-DPS, which provides the both isolation and the tightly regulated output voltage to meet bus requirements. This two-stage scheme suffers from some drawbacks such as an increased number of components, and a complicated power train and controller. This is why such schemes are not ideal for a cost-effective and efficient structure. We need to make sure if it is possible to further simplify power conversion steps in front-ended through applying advanced power conversion techniques.

This is just one of the major motivations of this dissertation work, namely, how to design front-end converters with simplified system configuration, high efficiency, and low cost.

The above motivation drives us to incorporate advanced power conversion techniques into the systems of Figs. 1-2 and 1-3 in order to obtain further simplification of the overall DPS structure. An alternative solution to realize the goal is to integrate the active PFC stage with the isolated high quality output DC/DC or DC/AC stage into one stage, which is known as single stage (S^2) converter with PFC or S^2 inverter with PFC. The S^2 converter or S^2 inverter has the least number of components and uses only one controller in the front-end power stage of DC or AC-DPS.

The underlying strategy of S^2 converter is to design the circuit in such a way that it allows its PFC circuit and voltage regulation circuit to share the same power stage. It is the S^2 converter that has least components and simplest controller. Therefore, by applying S^2 converter to implement all the functions of a front-end converter in a DC-DPS, we will obtain the simplest DC-DPS, as shown in Fig. 1-4.

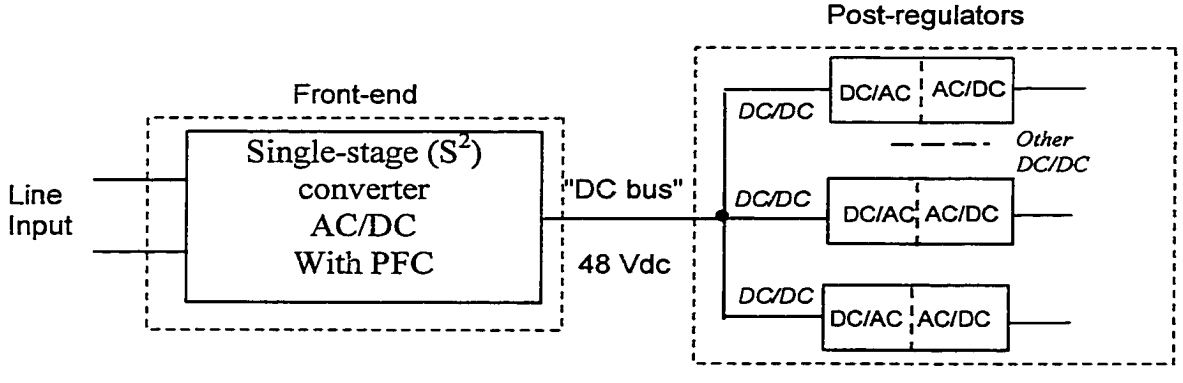


Fig. 1-4. Simplified DC distributed power system.

Correspondingly, by applying the S^2 inverter as a front-end stage in AC-DPS, we will obtain the simplest system structure of the AC-DPS, as shown in Fig.1-5. So far there is no significant research efforts in the proposed system structure as there is no published work in the open literature.

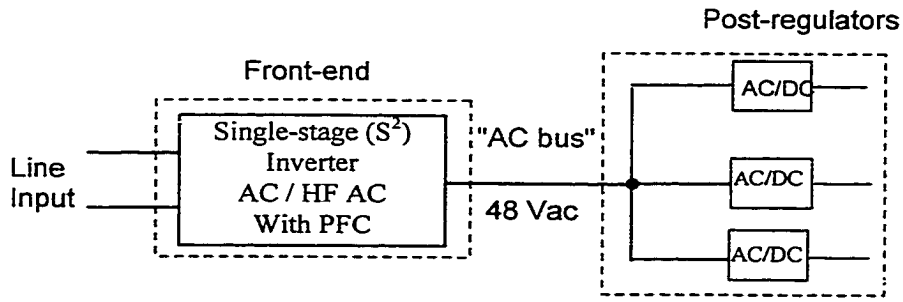


Fig. 1-5. Simplified AC distributed power system.

Although a certain number of S^2 converters have been reported in [17-23], all of those S^2 converters are not for application to front-end converters in DC-DPS. So those S^2 converter generally have low power rating and/or low efficiency. In order to use S^2 converter into a DPS, its power level must be first pushed to/over medium power level. Currently this is one of the most challenge issues to useful application of S^2 converters into DPS. Other issues include high bus capacitor voltage-stress, wide DC bus voltage range, difficult design for power train, and low efficiency at relatively high power output. Thus, the target of this work also aims at the above issues and present new approaches to innovate conventional power conversion techniques.

Today's electronic systems become more and more sophisticated. In many of advanced application cases, it is difficult for a single power converter or power supply to meet all system performance requirements. In particular, for a high power, high reliability power system, system integration technology employing multiple power stages or

multiple converters have gained rapid acceptance in recent years [47, 48].

In fact, system integration techniques cover very extensive multiple branch research areas, such as interleaving techniques, paralleling, system simplifying, stocking, device integration, control integration and packaging integration etc. System integration techniques can be used in "building blocks" to implement a wide range of power electronics circuit and systems

For almost all practical DPSs, another common feature is that multiple power stages or converters are simultaneously used in a DPS. So another study subject of this dissertaion work is placed in system integration techniques, that is to say, how to achieve good system performance by integrating multiple power stages or multiple converters into a DPS.

Theoretically, changing the "DC" power distribution to "AC" power distribution can substantially mitigate the cost and complexity of DC-DPS. Then the question arised here is why such a concept has not been extensively adopted in today's power systems. This is because there are still some of the existing technical challenges with respect to the development of an applicable AC-DPS. Furthermore, unlike the DC-DPS structure with a considerable amount of available design documents, the open literature shows that the research of AC-DPS is still in conceptual stage. Significant work remains to be done ahead.

1.2 Dissertation Outline and Major Results

The dissertation is organized into three parts and divided into nine chapters, including the conclusion chapter. Part I consists of Chapters 1 and 2 and reviews current techniques of distributed power systems. Part II consists of Chapters 3, 4 and 5 that

focuses the study on front-end converters to be used in DPS. Part III consists of Chapters 6, 7 and 8 and brings investigations into system level technology, namely, system interleaving, paralleling and simplifying. Please see framework description about this dissertation coverage, as shown in Fig. 1-6.

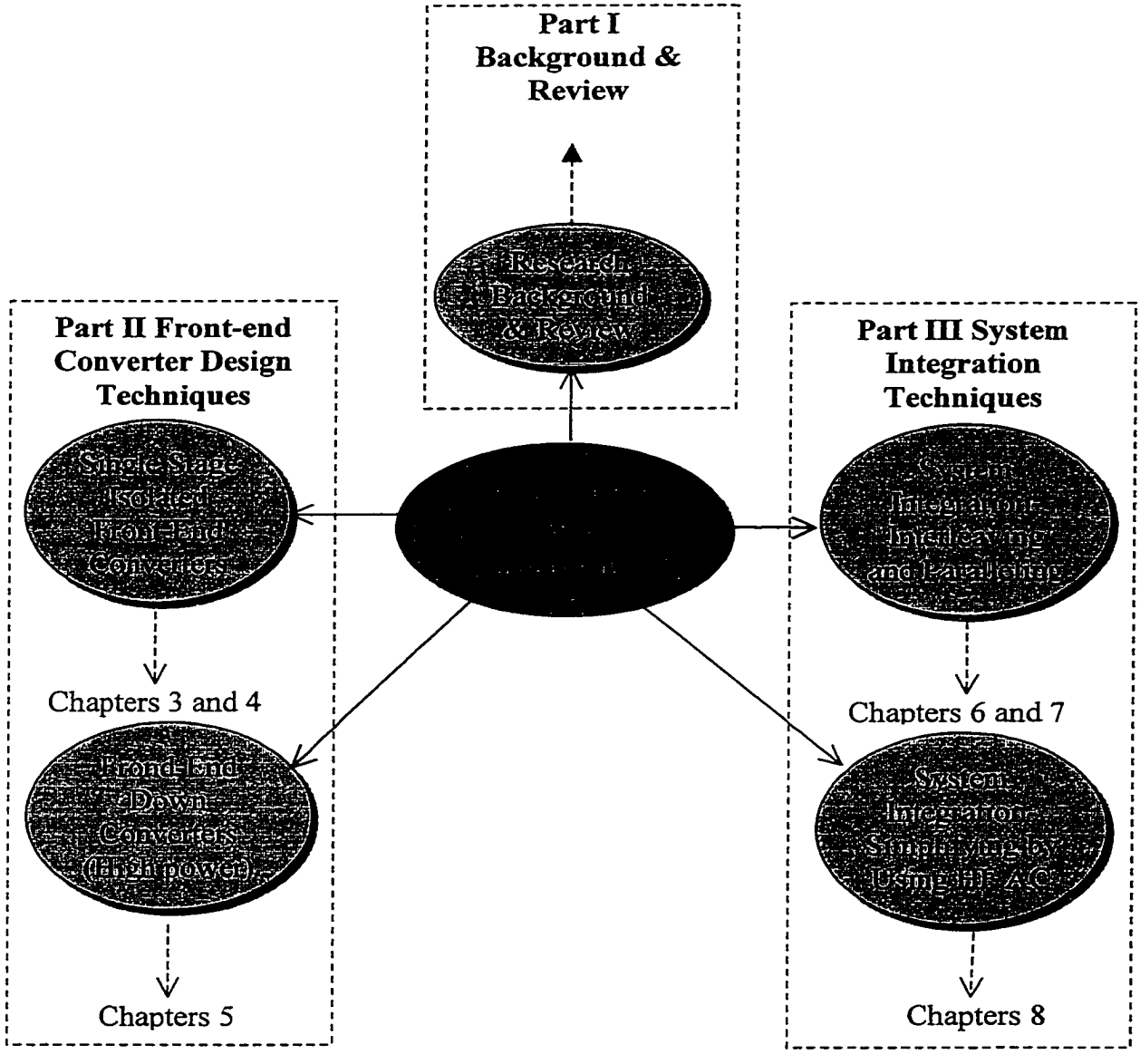


Fig. 1-6. Framework description of dissertation coverage.

Chapter 1 presents background and motivations of this work, and provides a baseline assessment of distributed power systems.

Chapter 2 offers a review for current techniques in distributed power systems, and identifies what the issues and challenges are in this research direction. These issues include not only improving efficiency, but also increased concerns regarding the cost and complexity of power supplying system. Major potential advantages using AC bus into DPS include simplified system configuration, low cost, high efficiency, and ease of voltage and current transformation. However, several practical issues still exist, including high EMI level, difficulty to back up power, non-redundant system structure and limited post-regulation approaches, etc.

Chapter 3 addresses key issues of S^2 converters, and possible solutions are explored. The high bus capacitor voltage-stress generally makes most of existing S^2 converters impractical. The inherent reason of high DC bus voltage is in power unbalance between the input and the output. Another challenging issue in designing S^2 converters is wide DC bus voltage range, which makes the design of a high efficiency converter to very difficult. An optimization methodology, which is applicable to most of S^2 converters, has been presented and verified through both simulation and experiments on the basis of a 150 W prototype at 28 V output. From the research on target S^2 converters, it can be generalized that higher the turns ratio, lower DC bus voltage, wider DC bus voltage range, larger boost inductor and wider duty cycle at nominal condition result in higher efficiency at the same operation mode.

Chapter 4 first introduces a new direct power transfer (DPT) concept to implement high efficiency S^2 PFC converters. Then a new PFC cell with DPT feature,

called "flyboost", is presented. It combines functions of flyback transformer and boost inductor. By having the flyboost cell operating in DCM, only a simple control will be required to achieve high power factor (greater than 0.97). The flyboost cell also significantly helps improve the efficiency above 5% over converters without using flyboost. Another important characteristic of the flyboost cell is that it will also automatically limit the DC bus voltage through a properly designed flyboost transformer and power train, which means that the converters using flyboost PFC cell can operate either DCM+DCM mode or DCM+CCM mode. As a result, the proposed converters are especially suitable for universal voltage applications with higher power handling capability than other known S^2 converters. By combining the flyboost cell and any family of other DC/DC conversion cell, we can obtain new family of S^2 PFC converters.

Chapter 5 presents a comparison study of high-power down-converters to be used in front-end converters of DC-DPS. In primary-side topologies for medium input voltage level such as 400Vdc, ZVT-PS-FB topology is the best choice. In primary-side topologies for high input voltage such as 800Vdc bus, generally, the topologies based on multilevel cell combination have relatively simple structure and low switch number. The topologies based on association of converters have higher magnetic volume than the structures based on multilevel cell association. For the secondary-side topologies, though the current-doubler rectifier has higher efficiency, the center-tap counterpart may have somewhat benefits in terms of cost and power density. In summary, regardless of primary-side or secondary-side topologies, the desirable approach would vary depending on which criteria is deemed most critical, such as cost, size, or efficiency. It also varies depending on specific application.

Chapter 6 investigates system integration technique using interleaving to be suited for high power topologies. According to frequency relationship between switching frequency and output ripple frequency, topologies are reclassified into secondary-side, same-frequency rectification topologies and secondary-side, double-frequency rectification topologies. It was found that the conventional interleaving techniques are actually suited only for the secondary-side same-frequency rectification topologies. For secondary-side double-frequency rectification topologies, phase-shift quantity among module control signals for N interleaved modules should be reduced to π/N. Typically, for the two-power stage case, a special quarter-cycle phase-shift between two control signals is required, not the previous half-cycle (180 degree) phase-shift. The characteristics achieved from the new interleaving method are as the same as those by conventional one, such as increased output ripple frequency, automatic ripple cancellation, and less EMI level, etc.

Chapter 7 details investigations into system integration technique using paralleling. Based on the classification of paralleing approaches of power modules, some new active current-sharing schemes can be obtained by proper combination of the sharing control structures and the current-programming methods. For instance, a combination of the inner regulation sharing control structure and current-programming scheme of an automatic master can be expected to achieve some special advantages. This chapter also gives a comprehensive evaluation of paralleling schemes for power supply modules. In summary, each paralleling scheme has its own merits and limitations, and each application has different criteria. The author's opinion is that there is no single best scheme suitable to all paralleling systems at the present time.

Chapter 8 explores another system integration technique-simplifying by using HF AC bus. A new DPS with multiple HF PWM buses is proposed and experimental prototype was built with a total of 210W output power for three independent outputs, i.e, 3.3V@30A, 5V@10A, and 12V@5.1A. The experimental results demonstrate that the proposed system works fine and a comparable efficiency around 80% can be obtained by this simple DPS system. In order to realize system redundancy, a new AC-DPS with trapezoidal waveform bus is presented and a conducting scheme is proposed. The scheme is expected to combine major advantages and eliminates main disadvantages coming from both of conventional sine-wave and square-wave buses.

Chapter 9 summarizes the conclusions of this work and contains suggestions for future work in related research areas.

2. REVIEW OF DISTRIBUTED POWER SYSTEMS (DPS)

2.1 Introduction

Basically, there are three different types of "power supply" architectures, i.e., centralized power system, modular power system and distributed power system (DPS), as shown in Fig. 2-1.

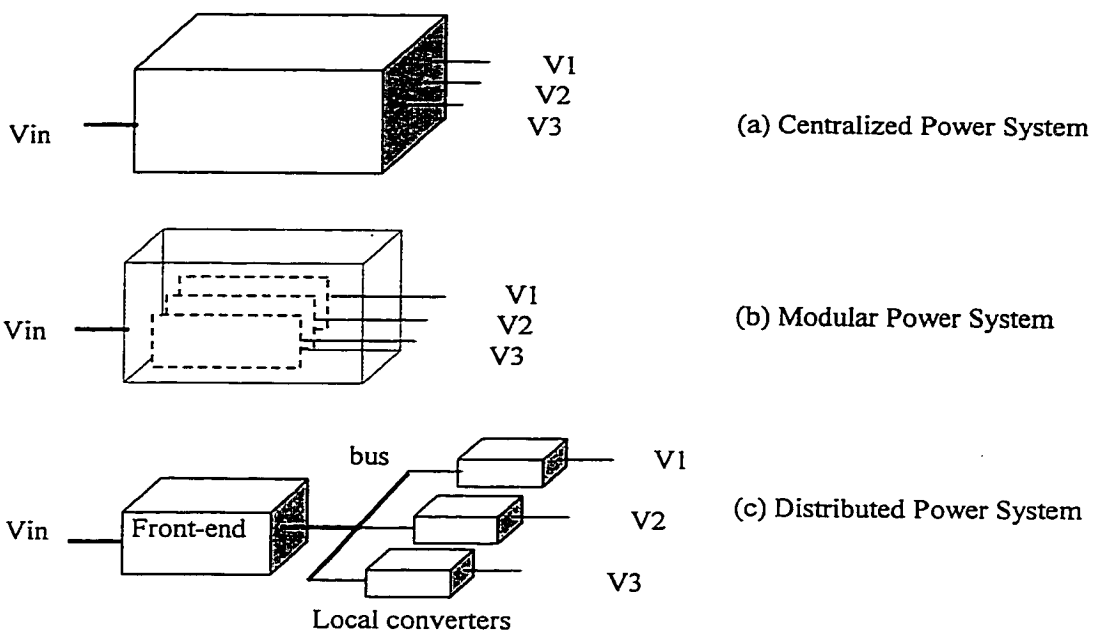


Fig. 2-1. Three types of "power supply" architectures.

The features of centralized power systems are:

1) One power conversion stage is located in one physical location in the system.

2) Multiple outputs are generated and bussed to the load.

The advantages of centralized power systems include concentrating all the power processing technology-including thermal management into a single box that can be designed, subcontracted, or purchased as a stand-alone item. However, this system often fails to provide adequate performance for new generations of electronic equipment.

Comparatively, modular power systems include features:

1) Multiple power conversion stages or converters are located in one location in the system, usually far away from the load.

2) Voltages and current can be combined to meet load requirements.

Modular power system is particularly suited for high power design. High power is achieved by paralleling multiple small power stages in a single package, producing the physical equivalent of a single large device. This way, power modules are easily standardized and traditional low power converter design techniques can be used. System's potentials for improved functional performance depend on both the individual power cells and their aggregation.

Distributed power systems, usually employing the modular design technique, incorporate the advantages of modular power system. But all outputs of the front-end converters will go to the intermediate bus by paralleling technology. Its basic characteristics are:

1) Multiple power conversion stages and/or converters can be allocated in different locations.

2) Intermediate voltage is bussed around the system; and

3) Multiple DC/DC converters located at the point-of-use are used to provided the local voltage.

While the ultimate extension of this concept is the "on-board" regulator or power supply, many other solutions for distributing power processing tasks are common. Before going to deep discussion for various issues, it is helpful to understand the motivation for considering distributed power.

2.2 Characteristics of Distributed Power Systems

DPS approach is gaining increased acceptance in many of advanced electronics systems due to its various attractive characteristics over traditional "power supply" architectures. The features listed below are summary of recent research work in references [7-17]. While not all of the following list potential advantages are common to all distributed power configurations, it is still a list worthy of consideration during any power system definition phase.

1) *Thermal Management and Packaging:* Modularization is a major characteristic in a modern DPS. Cellular power processing system can take advantage of a heat sink area much more effectively than can a single power module, and so lower cost thermal manipulating (air-cooling) rather than expensive liquid cooling technologies can be employed. Obviously, thermal design becomes simplified. By distributing the sources of heat generation, thermal management can often rely on conducted and radiated cooling, sometimes eliminating the need for air moving equipment, compact package can be achieved.

2) *Module Size Reduction:* Modular design in DPS may provide increased power density because lower power modules can operate at higher switching frequencies with reduced filter component size. Interleaving (phase-shifting of clock signals) of parallel

modules increases the ripple frequency, leading to reduction of the overall filter size. In addition, the small devices with less parasitic elements have considerable advantage as the switching frequency is increased.

3) *Less EMI and Harmonics:* By using interleaving technology for front-end and load converters, ripple frequency can be increased and the phases of the stages can be shifted to be beneficial to cancel ripples each other. Therefore, ripples are more easily manipulated than in a higher power, single power converter. Furthermore, aggregated outputs of parallel modules produce a low energy density spectrum with stochastically reduced harmonic components. The effects of aggregation considerably reduce both acoustic noise and EMI.

4) *Modularity and Standardized Designs:* DPS's layout is very suitable for modular system design. A centralized power supply almost by definition must be designed specifically for each new set of requirements. A goal of a modular design is the availability of standardized off-the-shelf modules or designs which could be combined in a variety of ways to meet a specific application. This has various benefits in development time and engineering costs as well as the confidence gained from using pre-qualified power components.

5) *Redundancy and Reliability:* An important characteristic of a DPS is the possibility of configuring a redundancy system using more modules than the minimum required by the load. Usually $(m+r)$ modules are used, where m is the minimum number of modules required delivering the load power and r is the number of redundant units (usually 1), which gives the system the ability to tolerate r failures without impact. Redundancy is desirable in many high reliability applications. Moreover, the paralleling

in DPS reduces electrical and thermal stress on semiconductor devices. In addition, the higher switching frequency of parallel converters results in a higher control bandwidth, and so a parallel system can respond more quickly to abnormal and damaging system conditions, such as short circuits and overloads. These simple arguments indicate that though the number of components in a parallel structure may go up, the reliability of overall system is still increased.

6) *Availability and Maintainability:* Availability is defined as the fraction of time the converter is expected to be operational. When using a Mean Time Between Failure (MTBF) and a Mean Time To Repair (MTTR) as specifications, we will find that the availability of parallel system is much higher than in a single, high-power supply, since repairing a paralleling system involves only replacing a single standard cell [47]. In addition, a properly designed parallel configuration allows the on-line replacement (hot-swapping) of defective modules. This provides the means for non-interrupting maintenance and repair.

7) *Point-of-Load Regulation:* DPS configuration facilitates placement of a power supply in close vicinity to the load for improved voltage regulation and dynamic response. If the load converter can be fabricated with sufficiently high power density, it can be placed directly on a logic board next to the load (so called "on-board application"). This characteristic is expected to use to meet challenging requirements for new generation of processors.

8) *Flexible System Structure and Layout:* Unlike centralized power system with only one power converter, DPS can realize very complicated power "supply" architecture to meet different load requirements in an electronic system. For instance, hot-plug

redundant system can be obtained by power module paralleling; by using cascading connection, the point-of-load regulation can be obtained and wide input voltage can be easily accommodated. In addition, based on the consideration of reliability, you can use multiple resources to supply power to the bus, such as utility resource, generator, and battery, etc. Also, loads could be split to obtain distributed load regulation and reduced noise coupling.

2.3 Basic Distributed Structures

Although distributed power architectures can get quite complex and specialized, most are either derived from or combinations of five basic configurations that are shown in Fig. 2-2, including parallel, series, split source, split load and stacked modules. It should be recognized that in addition to different interconnections, each of these approaches represents a solution to a different set of objectives. A description of these architectures and their characteristics is given below:

1) *Paralleling:* Paralleling power modules infers a common source and load. This usually means retaining a central location where a single high power supply is replaced with a grouping of paralleled lower power modules. While power processing is distributed, it may not be distributed very far. Parallel connections are often generated by the need for standardization and redundancy rather than reducing distribution losses. With higher reliability as an objective, equalizing stress by insuring load sharing between modules is usually required. Configuring power converters for current sharing when paralleled is not a trivial problem but IC's for that purpose as well as the use of current-

mode control methods provide ready solutions. In some of literature, such a configuration is often referred to as a modular power supply system.

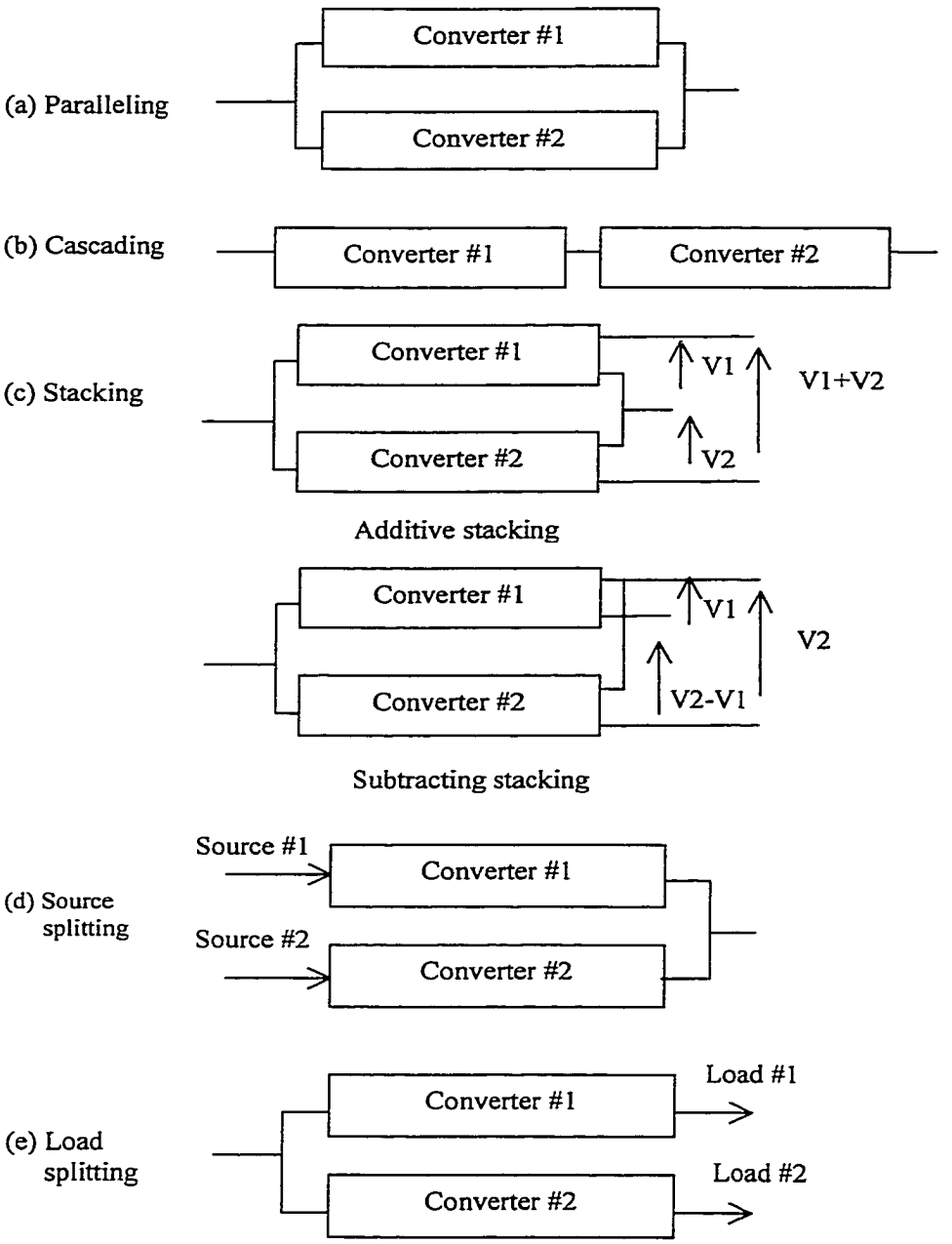


Fig. 2-2 Basic distribution structures (a) paralleling, (b) cascading, (c) stacking, (d) source splitting, and (e) load splitting.

2) Cascading: With a cascaded power system, an intermediate bus voltage is developed with each interconnection as shown in Fig. 2-2 (b). A typical cascaded system would be to follow a power factor correction pre-regulator with a down converter. Since each block handles the same current, it would not seem prudent to process the power twice, however there are offsetting benefits, specially in the example of two stage front-end converter, the PFC stage, in addition to removing distortion in the input line current waveform, accommodates a wide range of input line voltage variation and provides a roughly regulated intermediate voltage of 380 Vdc. Using this voltage on the bulk storage capacitor provides a very efficient means of accommodating long hold-up requirements.

The down converter then reduces the 380 Vdc to a more manageable bus voltage but, with minimum input variation, this converter can be designed very efficiently with large duty cycle and have a fast control loop for good dynamic load regulation. Additionally, with this structure, point-of-load regulation is easily obtained.

3) Stacking: Stacking of converters (usually DC/DC converters) allows combining the outputs of individual converters to obtain voltage different than the nominal voltage of each individual converter. This technique can be used to obtain non-standard output voltages using standardized converter modules. Taking high voltage application for instance, the additive stocking configuration of Fig. 2-2(c) provides output voltage equal to the sum of the nominal voltages of stocked converters. For low voltage applications, the subtractive stacking configuration provides output voltage equal to the difference between the voltages of the individual converters, thus providing an improved overall efficiency in some applications.

4) Source Splitting: Splitting structure shown in Fig. 2-2(d) allows the use of separate power sources to supply a common load. The typical applications are:

a) Battery Backup: Many systems require uninterrupted power supply operation. Battery backup is the technology most commonly used to provide a temporary power supply in the case of a primary power failure;

b) Separate Phase: Another form of power source redundancy can be achieved by supplying power to the equipment from separate utility phases. In such a case, redundancy is achieved by using separate power processing unit for each phase;

c) Multiple Buses: An additional level of system redundancy can be achieved by using multiple power distribution buses and using a separate load converter for each bus.

5) Load Splitting: Load splitting is a configuration where separate load converters are used to supply different loads, as shown in Fig. 2-2(e). The most common understanding of distributed power assumes split loads where different portions of the system are each powered by their own power-processing unit. Load splitting is used based on the following considerations:

a) Distribution power: in many large-scale systems (spacecraft, mainframe computer, etc), loads are physically distributed over substantial distances, also multiple voltage levels are required;

b) Regulation: in systems with distributed loads, centralized power supply often cannot provide adequate regulation at the point-of-load due to the bus impedance. This problem is eliminated by using a DPS with the separate load converters located in close proximity to each load.

c) Noise decoupling: when several loads are connected to a common power distribution bus, noise interference may occur between the loads. Load splitting technique minimizes this problem by introducing more load converters with the individual filters. An additional advantage is the possibility of isolating noise-generating loads from the rest of the system.

2.4 DC Distributed Power Systems

DC-DPS structures have been gaining increased popularity and are becoming mature technologies due to numerous attractions to industry. The application range from small several hundreds of watts personal computers, through 1 kW military electronic systems, to 100 kW commercial mainframe computers as well as telecom industry.

Figure 2-3 shows the mostly common implementation of a distributed power systems being used in many industry sectors such as communication system, computer system and advanced electronics equipment. The first block in foreword power path be designed for either single or three phase inputs to provide the line conditioning, power factor correction, EMI filtering, line pre-regulation, and energy storage at a high bulk voltage capacitors.

The second block in the forward path is typically a forward down converter operating with tight voltage regulation for maximum dynamic response to load variations. A transformer is included for isolation and efficient step-down to the bus voltage.

The load converters are connected between the bus and loads either in single or in parallel to handle high load currents and insure reliability. The front-end converters and load converters all can operate in parallel to provide the required power and *n+1*

system redundancy. Also, DC battery backup and AC generator backup are provided to system. Therefore, the system is completely protected from any single-point failure and shut down from utility system. When utility power is shut down, the power from battery will supply DC bus, with time the backup generator will be started up while the bus voltage drop down to some preset level.

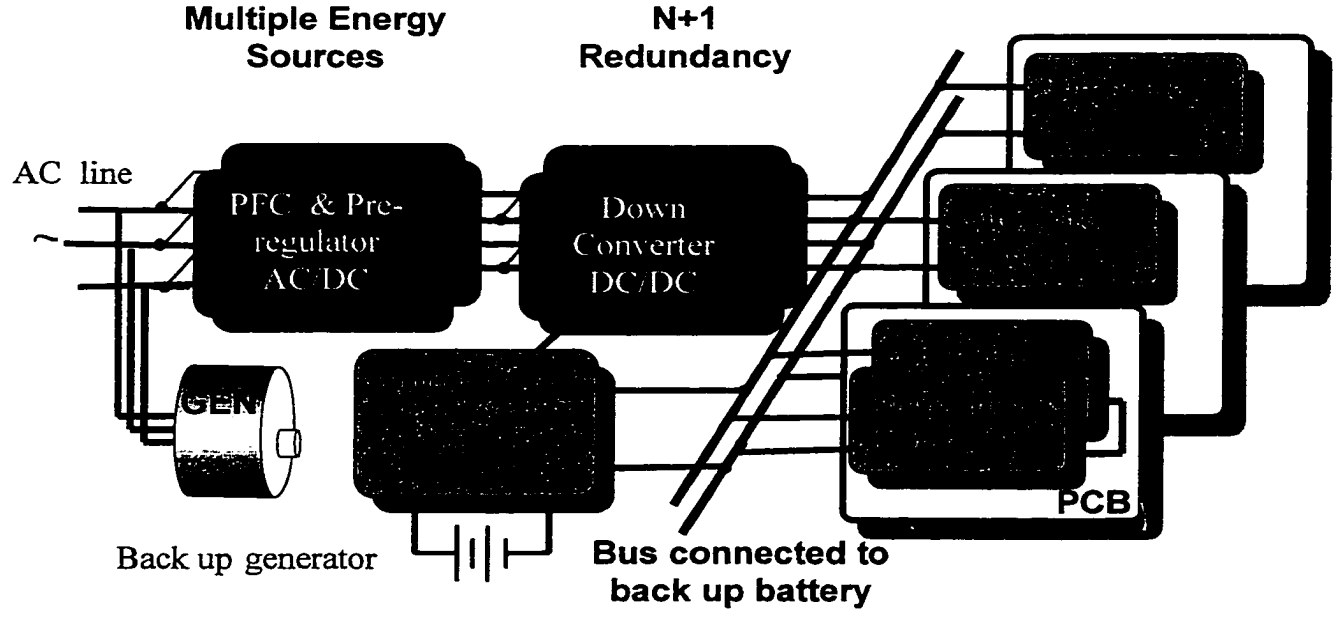


Fig. 2-3. A typical example for distributed power system.

2.4.1 System Design Considerations

Design of a DC bus DPS involves a number of trade-offs and choices related to the selection of distribution bus voltage, optimization of the front-end and load converters, and integration of the system. They are discussed as follows:

1) Bus Voltage Selection

Selection of the bus characteristics is an important step in DPS design since it affects all power system components. The level of bus voltage and degree of bus voltage

regulation are the main characteristics of the DC bus. The major considerations in the selection of the DC-bus voltage are [7-11]:

a) *Power level*: To minimize distribution losses, bus voltage must be sufficiently high to reduce distribution currents to acceptable levels. This implies higher bus voltages for higher power systems.

b) *Power losses*: With the recognition that losses in the distribution network are usually determined by I^2R, higher bus voltage levels with correspondingly lower currents make for a more efficient system.

c) *Safety considerations*: If safety is an important consideration, the bus voltage must be within safety-defined levels. In most cases this means a bus voltage below 60 V DC. To avoid possibility of a sustained arc, a bus voltage below 32 V must be selected [8, 10]. An equally troublesome feature is that this voltage (actually any DC voltage much over 32V) may sustain an arc which makes every switch and connector a significant problem.

d) *System simplification and dynamics*: An interesting counterpoint to a high voltage bus is the use of a very low voltage DC for distribution. The decision here is to accept some I^2R losses in the distribution bus in return for very simple, low cost point-of-use regulators. While this demands good regulation of the bus voltage, say around 5V and a well-engineered network, the gain is that the local on-card 5V regulators can be simple, low-drop linear types. These provide excellent dynamic load regulation at a very low cost.

e) *Isolation consideration*: While the transmission losses are low with high voltage, each point-of-use will require a relatively sophisticated DC/DC converter which must include a transformer (albeit at high frequency) for voltage step-down to load levels.

f) *Battery backup requirement*: In many systems with a battery backup, the bus voltage

must be compatible with the battery voltage to eliminate the battery discharger unit. In some applications *(e.g.,* telecom) this single item determines the bus voltage level.

2) Regulation of Bus Voltage Range

The regulation of bus voltage has a serious impact on the power system components. A tightly regulated bus allows the optimization of the load converters for maximum efficiency. To provide a tightly regulated bus voltage, however, the front-end section must include a regulating stage, typically a DC/DC converter. As a result, the efficiency of the front-end section is reduced. Hence the bus voltage regulation must be specified based on the overall system performance after careful consideration of the involved trade-offs.

3) System Hold-up Time

Typically, most power systems have a requirement to maintain some intelligence for a specified period of time after removal of the input supply. Without a backup power source, this means energy storage somewhere in the power path. If only a small and defined portion of the load has the holdup requirement, it might well be provided with capacitor storage at the point of use; but more often the location of hold-up energy will be on or before the distribution bus. So it might be another important criteria that is used to define the bus voltage level.

Since energy stored in a capacitor is proportioned to the square of the voltage, it is clear that the higher the voltage, the less capacitance is required for the same energy storage.

To derive a general formula, if we assume a constant load power, P_L, and require a T_{hold} millisecond as a hold-up time during which the bus voltage is allowed to drop

from V_1 to V_2 by no more than 20%, the value of the required storage capacitance, C, is given by Eq. (2.1):

$$C = \frac{2P_L T_{hold}}{V_1^2 - V_2^2} \tag{2.1}$$

4) System Cost

It should be clear that there are some additional system level factors to consider such as cost. While many cost-saving components, materials, and manufacturing techniques have been developed, the fact remains that one is unlikely to be able to build two converters as inexpensively as one. So it would seem that when compared just on the basis of hardware costs, a distributed power system will most likely more expensive to procure centralized power supply. Obviously, there are many other factors which enter into the equation and the growing popularity of distributed approaches can only attest to the many offsetting benefits.

5) System Integration and Interactions

One of the primary concerns associated with the application of DPSs is the system integration and interactions between the components of the DPS. This issue has been often ignored in the development stage. The potential sources of the dynamic interactions in a DPS are related to paralleling and cascading of converter modules. In most applications, an EMI filter is necessary for each DC/DC converter in the DPS that drastically increases system complexity and potential for interactions among the system components [12-15]. In some cases, instabilities can occur when individual power processing units are stable and connected together. A few but certainly not all of these characteristics are discussed below:

a) Parallel Converters:

In the paralleling power units to deliver shared current to a common load, the location of the output capacitor can have an effect. While it might be easy to assume that a large capacitor located as close to the load as possible would give the best dynamic performance, stability then becomes a function of the number of modules. Paralleling multiple modules lowers the total output impedance, which can boost the crossover frequency of the overall system closed loop. The preferable approach is to incorporate the output capacitor into the modules where the loop bandwidth will remain constant, regardless of the number of paralleled units [12].

b) Cascaded Converters:

Since a DC/DC converter is designed to deliver constant power to its load, its input impedance is a negative resistance. A front-end converter optimized for a resistive load can often become unstable when connected to this negative resistance. If the driving converter is a buck-derived topology, this problem can often be addressed by raising the crossover frequency of that unit; however, that solution may not be practical with a boost or other topology, which contains a right half-plane zero. Under these conditions, substantial reductions in bandwidth may be required. Another way of assuring stability of cascaded converters is to design them so that the magnitude of the source impedance of the driving unit is smaller that of the input impedance of the following converter. The stability would be assured if this criteria could be met over the entire operating bandwidth, however this is often difficult to achieve and overly restrictive [12, 13].

A typical example is shown in Fig 2-4 where two cascaded converters are considered, the transfer function for the combined system can be described as:

$$F = \frac{V_{2B}}{V_{1A}} = \frac{G \times H}{1 + T_M} \tag{2.2}$$

where $T_M = \frac{Z_o}{Z_{in}}$

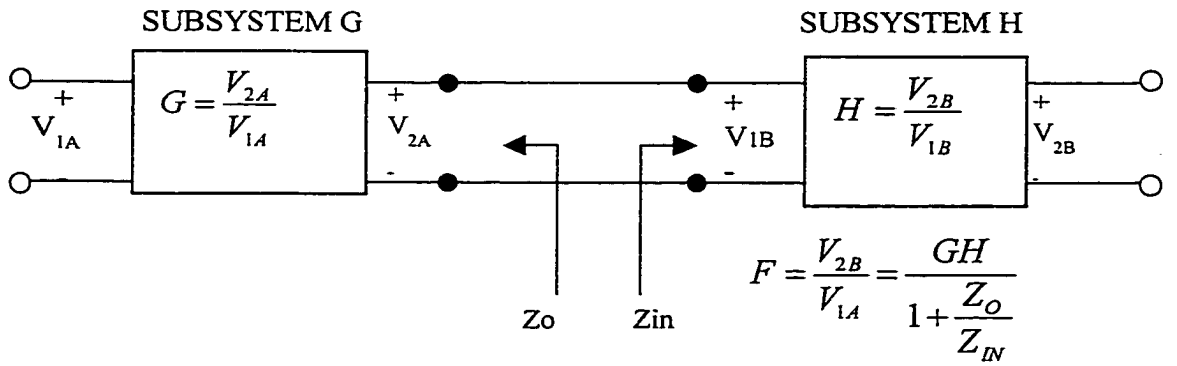


Fig. 2-4. Prediction of stability for cascaded impedances.

If Z_o is larger than Z_{in}, there is a loading effect that can be analyzed using the Nyquist criterion to determine the stability. Drawing a polar plot of the loop gain T_M will help define the phase margins at the points of overlap. With knowledge of the phase of the source output impedance, a phase band for the input impedance of the following stage can be defined which will ensure both stability and minimal performance degradation. For additional details of this method, see Reference [13-15].

c) EMI Filter Interaction:

Most switching converters need some form of input EMI filters for noise suppression. Paralleling multiple converters, particularly when driven from a pre-regulation processor that has its own input EMI filter, can cause undesirable interactions. A possible action to alleviate this problem is to use a two-stage filter between cascaded stages, as shown in Figure 2-5. The first stage would be common to all modules while the second stage is built into each module independently. The separate secondary filters will

reduce the ripple current on the distribution bus but, even then, some damping may be required to eliminate undesirable effects.

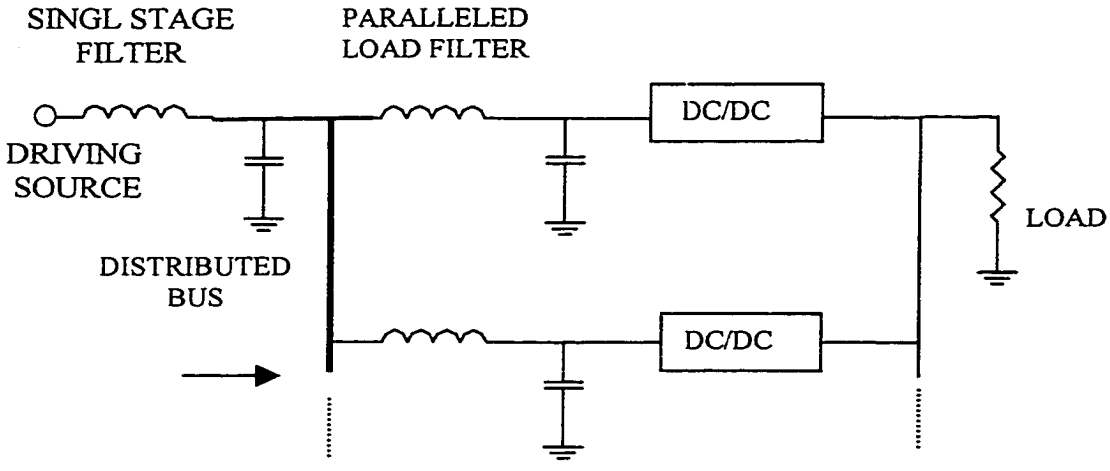


Fig. 2-5. Stability enhanced with single source filter driving paralleled input filters.

d) Switching Frequency Interactions:

It seems prudent, although perhaps not always necessary, to synchronize the switching frequency of all the power modulators within a system. This can sometimes be difficult, as, for example, when isolation boundaries must be crossed, or where one unit is designed with a switching frequency significantly higher or lower than others within the system. Bruce Carsten [16] recommends a phase-lock loop system, which, in addition to a frequency lock, can be set up with phase-shifts to prevent simultaneous switching.

6) General Analysis Procedure of DPS

In a DC-DPS structure, stability analysis and controller design are currently based on reduced order system modeling method and impedance match analysis method [12-15]. The following is a general procedure:

a) Modeling of each power stage as a subsystem;

b) Large and small-signal simulation of individual subsystems;

c) Integration of subsystems to form the complete system;

d) Worst-case performance analysis;

e) Fault simulation and solutions;

f) Compatibility analysis between the power stages;

g) Large-signal stability analysis of the entire system; and

h) Experimental verification of theoretical design and simulation of DPS.

2.4.2 Investigation of Current Techniques

1) Bus Voltage Level

As for the bus voltage, between 6V and 360V there is obviously a lot of room to maneuver. Many industrial controls use 24Vdc while the military and aerospace have a long history of standardizing on 28Vdc. Often the choice of bus voltage is defined by the output level of some difficult-to-change source, for example, the voltage provided by the backup battery.

The –48V batteries, which have been in use by telecommunication companies for years, fall into this category. With the backup battery defined, it was easy for the telecommunication industry to select 48Vdc as their bus voltage of choice. This voltage level received added emphasis with the European Telecom Standards EN41003 and UL1950 that designate 60Vdc the maximum SELV (Safety Extra Low Voltage) limit. With agreement on 60V as the maximum voltage which will not create a hazard, a nominal bus voltage of 48 V has become a widely accepted as the best compromise *between* 1GW distribution losses and safety. As such trend, if there were anyone voltage level which could be considered a standard for distributed power, it would be 48V.

One such standard has been defined in the future bus backplane distribution specification for computer applications, designated IEEE 896.2 —1991. In addition to several low-voltage bus levels, this specification defines a 48 volt level with a tolerance of 3~ to 54 volts. An additional requirement of this standard is that this 48V bus must be a fully isolated power source. That gives the user the opportunity to make it a ±48V, ± 24V, or any other combination. This means that the most versatile load modules will in turn be isolated so that the load and not the source will define the ground.

Another fact is that Intel Corporation specifies 48V as bus in sever DPS, this would also be the trend for future generation of computers that will use DPS [46].

2) Front-end Converters

A front-end converter, including a PFC pre-regulation converter and a followed down converter, is sometimes referred to as a line conditioner or a prime power converter that perform one or all of the following functions:

a) Line rectification and filtering;

b) Power factor correction and input line current harmonic reduction;

c) Down DC/DC conversion; and

d) Energy' storage for hold-up time.

In the simplest DPS, the input filter and diode rectifier are the only parts of the front-end power processing (FEPP). The bus voltage is unregulated, and the load converters must be designed to accept a relatively wide input voltage range. If a PFC is required, additional circuit will be added to FEPP, and the circuit is referred as to PFC pre-regulation converter.

Generally, there are three types of front-end converters to implement AC/DC conversion with PFC and DC voltage regulation, namely, passive PFC converter, active

two-stage PFC converter and active single-stage PFC converter, as shown in Fig. 2-6 (a), (b) and (c). The major performance comparison for three alternative methods is listed in Table 2-1.

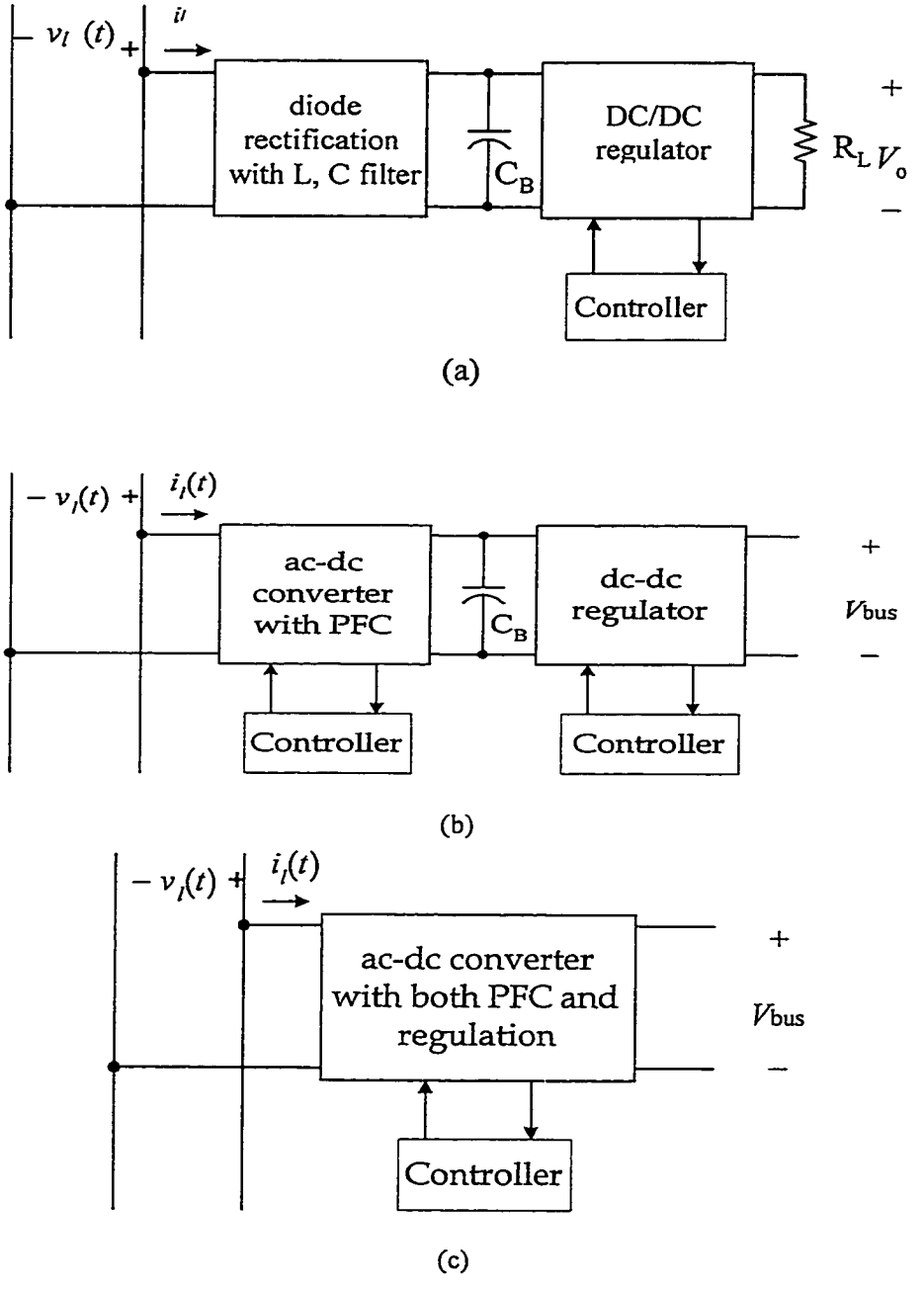


Fig. 2-6. Three PFC approaches: (a) passive PFC converter, (b) active two-stage PFC converter, and (c) active single-stage (S^2) PFC converter.

Table 2-1 Performance comparison of three front-end converters

Performance Review	Passive PFC	Active Two-stage	Active Single-Stage
THD	High	Low	Medium
Power Factor	Low	High	Medium
Efficiency	High	Medium	Low
Size	Large	Large	Small
Bulk Cap Voltage	Variation	Constant	Variation
Control	Simple	Complex	Medium
Component Count	Least	Most	Medium
Power Range	< 300 W	Any	< 300 W
Design Difficulty	Low	Medium	High

At present, the two-stage PFC converter scheme is a mainstream in industry. In the two-stage scheme, an active PFC stage (usually boost converter) is adopted as the first stage to force the line current track the line voltage. Its power handling capabilities can range from a few hundred watts to several thousands. This stage utilizes a 50-150 kHz switching frequency, and with reasonable effort, achieving a conversion efficiency around 95%. The boost topology provides a non-isolated, high voltage DC output [17-23].

The second stage is a DC/DC conversion stage, which provide the isolation and the tightly regulated output voltage to meet the DC bus requirements. With a roughly regulated input voltage and a tightly regulated output of bus voltage level, this converter can usually achieve near 92% efficiency under hard switching operation and 94%

efficiency under soft switching condition even with switching frequencies above 100 kHz. The circuit topology can be single-ended for power levels in the range of a few hundred watts, but above a kilowatt, a full bridge topology is usually needed [23-26].

The two-stage scheme suffers from some drawbacks such as the increased number of components, complicated topology and complicated controller. This is why such schemes are not ideal for a cost-effectiveness design.

An alternative solution is to integrate the active PFC stage with the isolated high quality output DC/DC stage into one stage, forming the so-called single-stage (S^2) converter, as shown in Fig. 2-6 (c). The underlying strategy of this scheme is to design the circuit in such a way that it allows its PFC circuit and voltage regulation circuit to share the same power stage. It is the S^2 converter that has the least components and the simplest controller. By applying S^2 to implement all functions of a front-end converter, we will obtain the simplest DPS. Although these have some limitations that have prevented widespread use, they may be applicable in the specialized applications, particularly for the cases from low power to medium power systems [17-23]. Several favorable topologies are active clamp flyback [17] and other single-stage power factor correctors with a boost type input [19-23].

The major issues in a S^2 PFC converter have been identified in Table 2-1. It is because these practical issues that are blocking this technique to extensive industry applications.

Another relatively new consideration for a circuit topology applicable to the frond-end converters is soft switching techniques such as zero-voltage-switching (ZVS) or/and zero-current-switching (ZCS), zreo-voltage-transition (ZVT) phase-shifted control for a bridge power stage etc [24,25,26]. Even with switching frequencies approaching 1MHz. This soft switching will provide very efficient power conversion in a high power

density configuration. In addition, new control techniques such as peak current control, average current control, hysteretic control, etc. have been used in front-end converters.

In high-reliability systems it is necessary to use the parallel front-end DC/DC converter modules. To provide the optimum performance, current sharing between the modules must be assured. Most current-sharing techniques use a current-sharing bus to provide a common voltage to control the current supplied by each module. "Democratic" current-sharing techniques are preferred to the single sharing bus " automatic master-slave" configuration [46-48].

To reduce the system noise, modules can be operated with the fixed phase-shift (interleaving, phase staggering). This technique, however, is difficult to use in an expandable system, where the number of modules is not predetermined, and no control circuitry outside the modules is allowed. A desirable synchronization scheme would be included inside identical modules, and would automatically change the phase-shift according to the number of operational modules connected to the bus [47].

3) Load Regulators

The success of the DPS concept depends largely on the availability of small, efficient, low-noise, and low cost load converters. Substantial research efforts have been devoted recently to the development of new circuit techniques suitable for high-density load converter modules. Clearly, the choices will be made on the basis of each specific requirement where performance and efficiency can be weighed against cost and simplicity with power level being an additional variable. For the non-isolated applications, some possible choices that might be preferred are: simple buck and synchronous buck converters. For the isolated applications, the choices may be active-

clamped forward converter, push-pull converter, symmetrical and asymmetrical half-bridge converters, and PS-FB converters as well as their modified version converters.

Several state-of-the-art designs have been developed for the on-board converter applications, including a HF soft switching converters [26,27], multiple-phase interleaved converters [28,29], load converter with the integrated magnetics [30,31]. All mentioned circuits could typically achieve power density in a range of 50~200W/in^3 and around 90% efficiency, mainly depending on the output voltage levels.

Current research efforts suggest that the major improvements are necessary in the power semiconductor devices and magnetic materials to achieve the desirable density and high efficiency. In particular, the low-voltage MOSFETs designed specifically for synchronous rectifier applications could dramatically improve the efficiency of the low-voltage load converters [28-30]. Commercial applications are pushing the power density and the efficiency of on-board power converters higher.

In order to meet the demands for faster and more efficient data processing, modern microprocessors and digital circuits are being designed with lower voltage implementations. New high-performance microprocessors may require from 40 to 80 watts of power for the CPU alone. Load current must be supplied with up to 30A/μs slew rate while keeping the output voltage within tight regulation and response time tolerances [2-4].

Based on the challenge requirements for new generation data processing loads, high-input-voltage and high-performance DC/DC will replace most of today's voltage regulator modules that use synchronous rectifier buck topology that needs large input capacitor and has asymmetrical transient response. Advanced topologies that are being

used or developed are: quasi-square-wave (QSW) buck, synchronous buck converters modules for non-isolated use; forward, push-pull, symmetrical and asymmetrical half-bridge converters for isolated use. All of these topologies can be implemented by interleaving technique, current doublers technique as well as control techniques such as PWM voltage control, PWM current control, variable frequency current control and hysteretic control.

2.4.3 Issues and Challenges

In view of the numerous advantages of DPS, there is no doubt that DPS will eventually replace centralized architectures in most high, many medium, and some low power supply systems, particularly for new generation of computer and electronic systems. To make DPS more viable in practical applications, however, many issues still need to be addressed. Also the following challenges can be currently identified.

1) Simplification and Cost of System

In the great majority of cases, the success of a practical DPS in the marketplace will depend on economics. Manufacturing costs for a distributed power modules are currently higher than those for centralized power supplies. One of the important reasons is that multiple power conversion steps are needed from input to anyone output. In some of cases, many independent converters exist in the system to replace the centralized power supply. Some circuit components, such as power devices and drivers, snubber circuits input and output filters for each converter in the system are inevitably replicated. As more and more cells are used, the replicated component costs become a higher fraction of the total.

Another reason is the complexity of control circuits. Some circuit components, such as sensing and control circuits, are not distributed among converters, but are replicated. Moreover, introduction of a current-sharing control circuit or interleaving circuit will further increase costs. Therefore, the simplification of a control system is also important for reducing cost, especially for low power applications.

High manufacturing costs (measured in dollars per watt) may cause an economical barrier in some applications where DPS architecture is desired, but economical considerations are an overriding factor. To make DPS approach attractive for these applications, the manufacturing costs must be reduced. This can be achieved by extensive standardization of the DPS subsystems and the full utilization of the surface-mount technology.

2) Analysis and Design Techniques

The design of the overall control system is a crucial issue, since it heavily impacts the cost, the reliability and other performances of a distributed power system. But it is very difficult to conduct feasible trade-offs for a practical DPS. Some conflicts and problems inevitably occur, e.g., conflicts between modularity, cost and regulation performances, power stage simplification and conversion efficiency, ... etc, are all needed to be taken into a consideration of control design.

Although much has been done to explain dynamic interactions at the system level in a DPS system, too many premises exist in the previous analyses, and so the study, particularly for complete DPS, still needs to be continued. A design methodology based on the modeling techniques is expected to be developed in the near future. The

corresponding computer-aided tools and higher-level simulation models must be also developed to provide systematic design techniques to shorten development times.

3) System Interactions

As discussed above, an important issue in a DPS is interactions between power units, e.g., cascaded converter interactions, EMI filter interactions and switching frequency interactions. In some cases, even though each power unit is stable, the instability still can occur when individual power processing modules are connected altogether. It is also interactions that cause design difficulty in system level.

4) Efficiency

The high efficiency is required for the whole DPS system, particularly for new generation of data processing type of loads with low voltage high current. It presents new challenge for the load converters or VRMs to minimize power dissipation on the board containing the load. Presently, the on-board DC/DC converters or VRMs can only achieve efficiency around 90%. Improvements must be made to increase the efficiency to over 95%. Also, compact size for point-of-load converters is still required. New converter technologies should be explored to combine low switching losses with low device voltage and current stresses. The semiconductor and magnetic devices should be improved to meet the challenges of high-frequency, high-density, on-board converters.

2.5 High Frequency (HF) AC Distributed Power Systems

In recent years, the DC-DPS has been used extensively in mainframe computer systems, communication systems, aircraft, fighting jets, warships, phased-radar arrays and space vehicles, and lately been used in the construction of the international space

station. However, in many of today's applications, theoretical design issues and philosophies of the power conversion systems are finding their way to practical design. These issues include not only improving efficiency, but also increased concerns regarding the cost and complexity of power supplying system used to satisfy the electronic system's total performance requirements [7,32,33].

Theoretically, changing the "DC" power distribution to an "AC" power distribution can substantially mitigate the cost and complexity of DC-DPS. Other potential advantages of AC bus DPS include: simplified system configuration, high efficiency, ease of voltage and current transformation, effective ground noise isolation, and the possibility of connector-less distribution via a distributed transformer. However, ac-bus DPSs have not been widely accepted in power supply applications due to several potential problems such as EMI noise, high frequency losses, and bus distortion, etc.

2.5.1 System Design Considerations

In an AC-DPS, except the similar system design considerations in a DC-DPS (see Section 2.4.1), there are two additional principal aspects that impact the system design: 1) bus frequency, and 2) bus waveform shapes. The selection of bus frequency will have a major impact on the size of reactive components used in the system. However, a choice of too high a frequency places an increased burden on the circuit design with the diminished advantage with respect to component size reduction. In addition, core losses in the magnetics, AC bus losses and voltage drop across interconnect inductance and transformer leakage inductance increase with frequency. Thus the AC bus frequency is an important tradeoff parameter. If an AC-DPS performance is comparable to a DC-DPS, it

seems to be reasonable to set the bus frequency range from about 50 kHz to around 500 kHz based on the current available power conversion technologies and power devices.

On the other hand, the special bus cabling increases the cost and the complexity of a DPS. In addition, the skin-effect increases the bus resistance at high-frequencies. To keep the bus losses down, the practical maximum bus frequency seems to be limited to a range of 20-250 kHz range. As a result, filtering of the rectified bus voltage requires relatively large filters.

Basically, there are two waveform shapes to be used as AC bus waveform, namely, sine wave and square wave/PWM waveforms. Sine wave HF regulated AC bus has some advantages and can be generated at a fixed frequency with good efficiency for distribution to line transformers with rectifier/filters for "point-of-load" voltage. Noise level coupled into system depends on circuit impedance. The EMI problems can be improved with a low impedance coaxial bus design. It is natural to reason that the less distortion the bus waveform, the less the potential noise effects. From this perspective, sine wave bus is optimum. However, while keeping bus voltage and current waveofrm as sinusoidal, to regulate load voltage, complex issues with regards to inverter and load converter circuit designs will be introduced [34-43]. This is particularly true if wide load ranges are required and bus waveform's harmonic distortion must be minimized. In addition, a low power factor load converter will bring high harmonics and adds stress on the source generator size and efficiency, as well as adds losses and EMI noise on the system.

The prominent disadvantage of implementing a square wave/regulated PWM voltage waveform for the bus is the resultant wide spectrum noise content (compared to a

sine wave) [33,43-45]. Therefore, most of the previous research on the proposed AC-DPS has concentrated on the use of a sine wave voltage bus under the assumption that this is the preferred power distribution waveform shape from the perspective of system noise propagation [35-38]. The major advantages of square wave bus are that simpler/cheaper frond-end and load converters are available, most of the mature PWM converter techniques including frond-end converters and load converters, e. g., the post-regulator-magamps, can be transplanted by the proper modification in this system. The wide range load regulation is relatively easier to be solved. Thus we can conclude that the bus waveform shape depends heavily on the load features such as required regulation range, noise sensitivity and distribution distance, etc. Some new ideas, such as using trapezoidal waveform bus and the stacked structure frond-end inverters have been presented in Florida Power Electronics Laboratory. Expected outcomes are that good trade-off between major performance specifications will be obtained, particularly for the system EMI/EMC, efficiency, system reliability and complexity. Further research will be reported for investigation of bus structure and waveform shapes in future.

2.5.2 Investigation of Current Techniques

1) Frond-end Inverters Topologies

Generally, bus waveform shapes determine which family of topologies should be suitable as the frond-end inverters in an AC-DPS system. Figure 2-7 shows a popular front-end inverter topology, using a LCC resonant inverter as a frond-end inverter with sine wave AC bus. Its major features are:

a) constant frequency, clamped-mode LCC inverter;

b) possible ZCS/ZVS operation with reduced circulating energy; and

c) low THD for both bus voltage and current.

Figure 2-8 shows a half-bridge inverter as a frond-end inverter with square wave AC bus. Its major features are [35,37]:

a) constant duty cycle control;

b) ZVS can be realized for both bridge; and

c) bus voltage can be regulated indirectly through PFC pre-regulator.

The front-end inverters in Figs. 2-7 and 2-8 are implemented with the two-stage schemes to meet stringent power factor and harmonics regulations. In this two-stage scheme, an active power-factor correction stage (also being called as pre-regulator, usually using boost converter) is adopted as the first stage to force the line current track the line voltage. The second stage is a DC/AC inverter, which provide the isolation and the tightly regulated output voltage to meet DC bus requirements. This scheme suffers from some drawbacks such as increased number of components, complicated topology and complicated controller. This is why such schemes are not ideal for cost-effective systems. An alternative solution is to integrate the active PFC stage with the isolated high quality output DC/AC stage into one stage, as shown in Fig. 2-9.

2) Post-Regulator Topology

The rectification of the AC voltage in the load converters may cause serious problem due to the harmonic currents injected in the bus. To avoid this problem, each load converter should be designed with high power factor and low harmonic distortion of the input current.

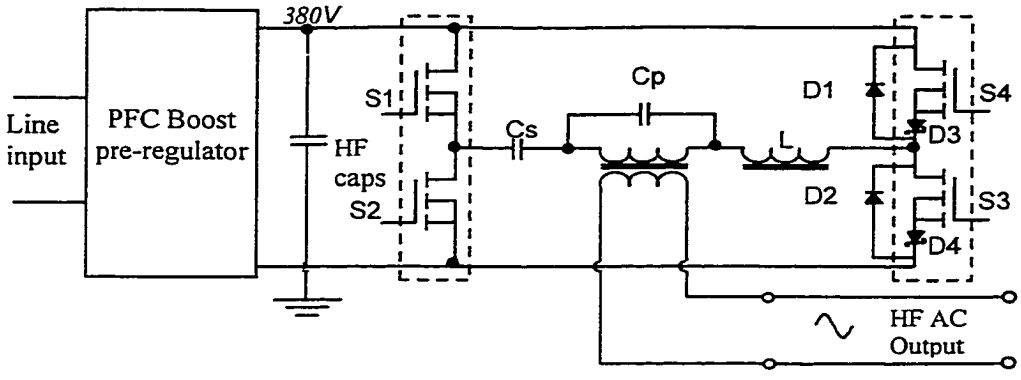


Fig. 2-7. An example of front-end inverter with sine wave bus.

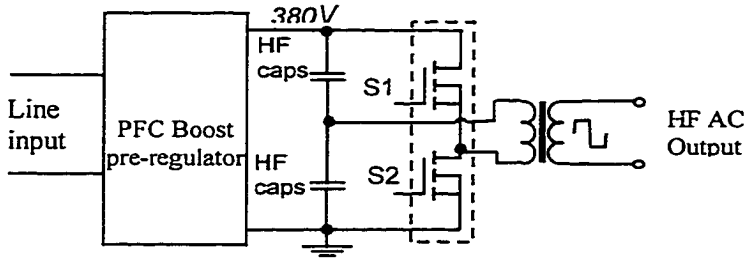


Fig. 2-8. An example of front-end inverter with square wave bus.

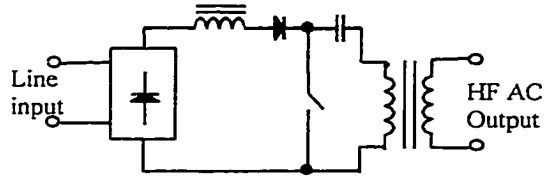


Fig. 2-9. An example of single stage front-end inverter.

Similarly, the selection of post-regulator topologies depends also on the bus wave shape. Fig. 2-10 gives the dominant class of topologies as the post regulators with sine wave bus, i.e., series resonant rectifiers (SRR). Its output voltage regulation can be realized through three approaches [10]:

e) by variable capacitor control;

f) by varying the resonant inductance; and

g) by phase-angle control.

The other evolved schemes can be found in [11-13]. Fig. 2-11 shows the dominant type of post regulators with square wave bus, namely, magamps. In fact, the magamps can be developed based on the conventional PWM DC/DC converters.

2.5.3 Issues and Challenges

As stated above, in this cutting-edge technology area there are still several technical challenges to traditionally block the development of an AC-DPS into practical industry applications. It is not too early to be thinking about answers to these issues because authors strongly feel that the High-frequency AC bus DPS is perhaps an idea whose time has come up. Through extensive survey, the major issues and challenges are summarized as follows:

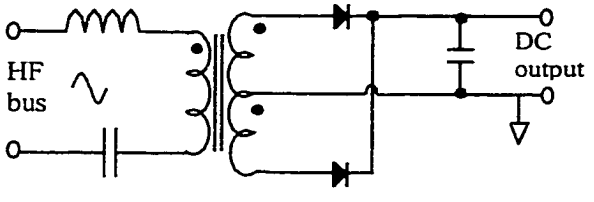


Fig. 2-10. A post-regulator using SRR with sine wave bus.

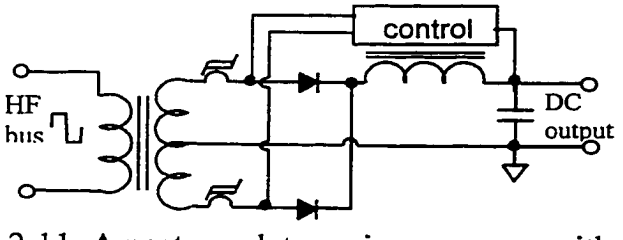


Fig. 2-11. A post-regulator using magamp with square wave bus.

1) Modeling, Analysis and Design of HF AC DPS

a) At converter level, available models need to be developed for emerging new converters such as single stage inverters, sine wave and square wave post regulators with specific controls.

b) At system level, it might be very complicated and challenging to characterize behavior for both small-signal and large-signal transient response, especially in case of considering various parasitic parameters. So far there is no report at system level modeling in this area in current available literature.

2) Front-end Inverter

Tight regulation and high efficiency are still difficult to realize, particularly for the inverters working under the distorted input condition of post-regulators. Ideal goal might be to use single stage single switch implementation to integrate the inverter function with the PFC function. However, the following issues will be encountered:

a) A critical issue for most of topologies is in that it has very high bulk capacitor voltage stress at high line and light load. A high capacitor voltage stress means a high component rating, high cost and low efficiency.

b) The second challenging issue is that the wide capacitor voltage range of the single-stage PFC converters will require the larger component ratings compared to the two-stage PFC converters

c) The another drawback is that although the simplification can be obtained in a single-stage scheme, the converter regulation capabilities will be largely limited because one stage simultaneously performs PFC, and load regulation and line regulations

d) It is usually difficult to push single stage converter to medium or higher power levels.

3) Bus Structure

The characterization of EMI (induced system noise), different waveforms [sine or square], line structures and PCB layouts need to be further addressed regarding the system performance.

4) Post-Regulator

The performance challenges of conventional post regulators (in particular, VRMs) are the same as that of the AC-DPS post-regulators have, including the following:

a) Can the synchronous rectification and integrated magnetic techniques be applied to AC-DPS post-regulators;

b) Fault-protection and current limiting, since there is no switch directly in series with the AC distribution input to the post-regulator;

c) Hot-swapping or hot-plug-in are unique issues as well because paralleling is more difficult than in case of DC-DPS;

d) Large-signal transient response performance needs exploration;

e) Various methods to achieve closed-loop post-regulation, in addition to magamp control should be investigated; and

f) So far, paralleling of converter modules in the AC bus environment may be rather difficult due to the requirement of precise synchronization and impedance matching.

5) Overall System

a) Battery-backup of distribution bus becomes an issue when the power distribution method is a high-frequency AC type, as discussed above;

b) System stability will also be an issue due to interactions between front-end and post-regulators.

2.6 Summary

The present state of development of distributed power systems is systematically reviewed in this section. Basic distributed structures and their characteristics are described. Various DC-bus and AC-bus distributed power system architectures are discussed. The system design considerations are discussed. The characteristics and challenges of both DC-bus and AC-bus distributed power systems in potential applications are summarized.

Most of DPSs can be constructed by combining five basic distributed structures. The bus voltage can be either DC or AC and thus two fundamentally different DPS architectures can be identified — DC-bus and AC-bus. The selection of the DC-bus or AC-bus architecture has a profound impact on the entire DPS design and performance.

In the traditional DC-bus DPS, the front-end converters include the first stage AC/DC with PFC and the second stage DC/DC conversion. Together with load converter, there are totally two inversions and three rectifications must be performed. Since each conversion step introduces power losses, the overall efficiency is not optimal.

The AC-bus DPS is potentially more efficient than the DC-bus DPS, since the conversion is achieved using only one inversion and two rectification. Similar to the DC distribution scheme, some means of regulation is usually required for the AC DPS to compensate for line and load variations. As well known, the low-frequency (50 or 60 Hz) AC power distribution has been used for decades in utility systems where the efficiency is critical. The high-frequency AC power distribution has been investigated just in recent years. Moreover, its research stays in only conceptual stage and primarily for avionic and

space application considerations at present. The reason why AC-bus DPSs have not been widely accepted in industry applications is due to several practical problems such as high EMI level, difficult to back up power, limited post-regulation approaches etc. Therefore, we believe, there is a lot of work to be done before the AC-DPS is put into industrial applications.

This work was supported by the grant from NSF.

3 KEY ISSUES AND SOLUTIONS FOR SINGLE STAGE (S^2) CONVERTERS

3.1 Introduction

Declining power quality in many power electronic systems has become an important problem as illustrated by many recent surveys [18-23]. Power factor correction (PFC) techniques have become attractive since several regulations have been effected recently. Many PFC AC/DC converters have been presented in recent years. For active PFC techniques, classified by the system configurations, these techniques can be categorized into two-stage and single-stage (S^2) schemes, or the two-stage approach and the single-stage approach. The two-stage approach is currently the most commonly used approach. As shown in Table 2-1 of Chapter 2, two-stage approach has good electrical characteristics of high power factor and fast output voltage regulation. Furthermore, since the two power stages are controlled separately, optimization of both power stages is made easier. The main drawbacks of this scheme are its higher cost and larger size resulted from its increased component number and complicated control circuits.

A S^2 scheme combines the PFC circuit and DC/DC power conversion circuit into one stage. Due to its simplified power stage and control circuit, this scheme has some potential attractions. A number of S^2 PFC circuits have been reported in recent years [18-23]. These circuits are especially attractive in low cost, and low power applications.

The underlining strategy of the S^2 PFC scheme is to design the circuit in a certain way that allows its PFC circuit and power conversion circuit to share the same power

stage. The PFC inductor is still necessary while saving an active switch and a PFC controller. The remaining controller is to perform tight output voltage regulation. Therefore, the switch duty-cycle is almost constant during one line cycle in steady state, which means that input PFC would be performed automatically when the output is regulated tightly. PFC is usually obtained by operating the PFC stage in the discontinuous current mode (DCM).

Main drawbacks for S^2 PFC converter have been highlighted in Table 2-1. Herein it is necessary that we further state the issues before going into depth.

The instantaneous ac input power always varies at twice the line frequency, even if the output power is kept relatively constant. As a result, a bulky capacitor is needed to handle the instantaneous power difference between the input and output, such that the output voltage is regulated tightly and free of line ripple. This is a major drawback since S^2 converters have limited capability to process unbalance power with single active switch and limited capacitance of capacitor. Therefore, the high bus capacitor voltage-stress generally exists for most of S^2 PFC converters, which makes most of existing S^2 converters be impractical for universal input application. This issue is more severe under the high line voltage and light load current case [20]. A high bus voltage means high component rating, high cost and low efficiency.

The accompanying issue with the resulted wide capacitor voltage range of the S^2 PFC converters will require larger component ratings compared to the two-stage PFC converters. To make situation worse is that the intermediate bus voltage generally has wide range and is determined by many factors such as boost inductance, transformer turns ratio and input voltage, etc. This results in big difficulty in system de-coupling

before designing, which is often necessary to derive design formulas. Therefore, how to characterize bus voltage and optimally design power stage will be further research efforts.

The other issue is that one power stage and DCM operation make S^2 converters only attractive for low power applications and result in a low efficiency while used in medium power level. This limits the application of the S^2 PFC converters into DPS in certain degree. Therefore, how to push the power rating higher and integrate individual S^2 converters into DPS application will be next research step.

In this chapter, the above three highlighted issues are addressed and possible solutions are explored.

3.2 Intermediate Bus Voltage Stress and Solutions

3.2.1 Reason for High Bus Voltage Stress

Figure 3-1 shows a general block diagram of S^2 PFC converters, which use only one active switch and one controller. In order to generalize the concept of bus voltage stress, it is desirable to use two functional blocks, PFC block and DC/DC block, to represent the S^2 PFC AC/DC converter, as shown in Fig. 3-2. The first block is a PFC stage to achieve high power factor function, which is usually a boost-like converter; the second functional block is a DC/DC converter to obtain tight regulation with output isolation. There is a bulky capacitor between the two functional blocks to withstand the fluctuating input power and rectified line ripple. Both PFC block and DC/DC block can operate either in DCM or in CCM. Therefore, there are four possible combinations to implement S^2 PFC converters, i.e., DCM PFC + CCM DC/DC, DCM PFC + DCM

DC/DC, CCM PFC + CCM DC/DC and CCM PFC +DCM DC/DC. However, these combinations present different forms of power balance relationship. For example, the DCM PFC + CCM DC/DC combination generates a DC bus voltage that could be as high as over 1000 V at high line and light load conditions for universal line applications [56]. Selection of switches and capacitors in this case would be limited and very costly.

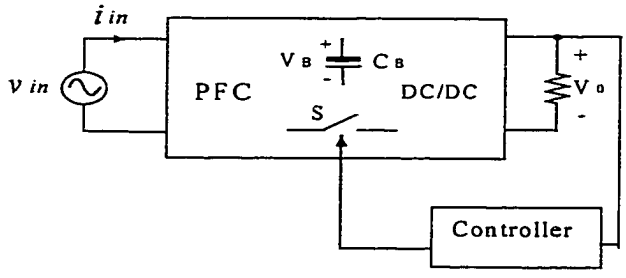


Fig. 3-1. General block diagram of S^2 PFC converters.

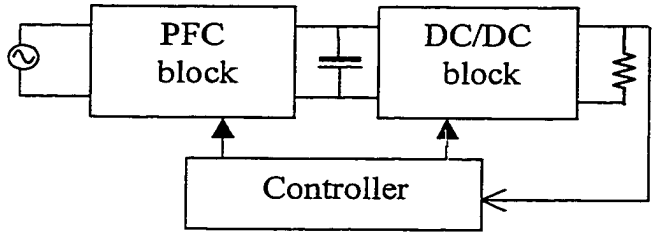


Fig. 3-2. Functional block diagram of S^2 PFC converters.

Usually, it is required that the PFC block has an inherent PFC property, while using the controller regulates the output voltage of DC/DC block. On the other hand, the CCM operation for DC/DC block is preferred to reduce power losses. Therefore, the operating mode, the DCM PFC + CCM DC/DC is deemed to be ideal in low to medium

power level. However, critical bus voltage stress occurs in this combination. Figure 3-3 shows the relationship between the input power and the duty cycle in the PFC block, and between the output power and the duty cycle in the DC/DC block [20]. The figure explains well the reason why the unbalance power exists. We can obtain understanding to high bus voltage stress by analyzing the relationship between duty-cycle and converter power processing capacity.

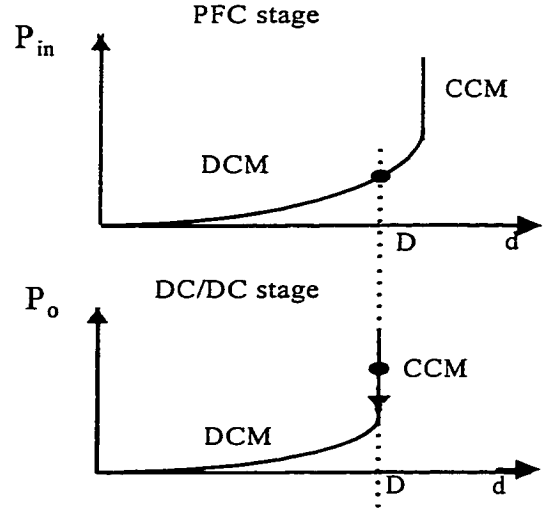


Fig. 3-3. Relationship between the input power, output power, and duty-cycle.

Since the DC/DC stage operates in CCM, the duty cycle does not change with the load variation according to Fig. 3-3. The duty cycle doesn't change immediately when the output power decreases, because of the CCM operation in the DC/DC block. Thus, the input power remains the same as under heavy load. There exists an unbalanced power between the input and the output. This unbalanced power has to be stored in the bulk capacitor C_B, causing the DC bus voltage to increase. As a result, the output voltage will increase too. To compensate for the output voltage increase due to the increase of the bus voltage, the voltage feedback loop is operated to regulate the output voltage as a constant.

So the duty ratio has to decrease, and the input power also decreases correspondingly. This dynamic process will not stop until the input power equals the output power, and new power equilibrium is reached. In summary, power unbalance in different operating mode combination is the inherent reason for causing high bus voltage. The detailed analysis and explanation of power balance relationship for the other combination modes have been presented in [20].

3.2.2 Schemes to Alleviate Bus Voltage

From the above analysis, perceptively, the bus voltage could be controlled within proper range so as to make a S^2 PFC converter be practical. The analysis also provides some possible approaches to resolve the bus voltage stress problem of S^2 AC/DC converter at light load high line. If the power delivered by both blocks of the converter is either duty cycle dependent or independent simultaneously, the converter should have less bus voltage stress under the proper design. Some S^2 PFC implementation circuits with proper bus voltage have been presented in [19,20,21,23,56]. This section classifies these circuits into the following four schemes to suppress high bus voltage stress:

1) DCM + CCM combination with variable frequency control
2) Both functional blocks operate under same mode
3) Series-charging, parallel-discharging capacitors scheme
4) Bus voltage feedback

The following sections investigate each of the four categories.

1) DCM + CCM Combination with Variable Frequency Control

This scheme was proposed in [56]. Since the gain of the CCM DC/DC stage depends only on the duty-cycle, and the gain of the DCM boost input block depends on the frequency but not duty-cycle. It is possible, for the DCM boost input block to regulate the capacitor voltage (without affecting the output) by a variable-frequency control. That is to say, the input power of PFC block is inversely proportional to the switching frequency at DCM with constant duty ratio, the unbalance power between the input and output decreases with the increasing of switching frequency. This scheme is proven effective to resolve the bus voltage stress problem. The drawback of this approach is that large load variation range results in large range of variation in switching frequency. For a load change from full to 10% of the rated load, the switching frequency has to be as 10 time as that of the full load to remain the same bus voltage. Such wide switching frequency variation makes it difficult to optimize the inductive components of the converter. In practical circuits, the frequency range is smaller than the theoretically calculated one because 100% efficiency is assumed in theoretical analysis.

2) Both Functional Blocks Operate under Same Mode

As discussed in the last section, power unbalance in the combination DCM + CCM will cause high voltage stress on inter-mediate DC bus. However, there is no DC bus voltage stress problem in combinations of same operating mode, either in DCM or in CCM for the two functional blocks, i.e., DCM + DCM and CCM + CCM. Taking DCM + DCM for example, the duty-cycles of the two blocks in Fig. 3-1 will simultaneously decrease with the load becoming light. As a result, the input power also decreases with output power because of decreased duty-cycle. There is no unbalanced power between the input and the output. Power balance relationship is similar in CCM + CCM

combination. Thus, it is concluded that there is no DC bus voltage issue for both functional blocks operate under the same mode with proper circuit design. This statement will be verified through the next theoretical analysis of an example circuit.

Figure 3-4 shows an integrated S^2 PFC converter consisted of two flyback converters [20]. The PFC block is composed of a bridge rectifier, an EMI filter, transformer T_1, main switch S, diode D_1 and bulk capacitor C_B. The DC/DC block is formed by the main switch S, diodes D_2 and D_3, transformer T_2 and output capacitor C_f. The bus voltage V_B can be calculated from the input-output power balance in half line cycle.

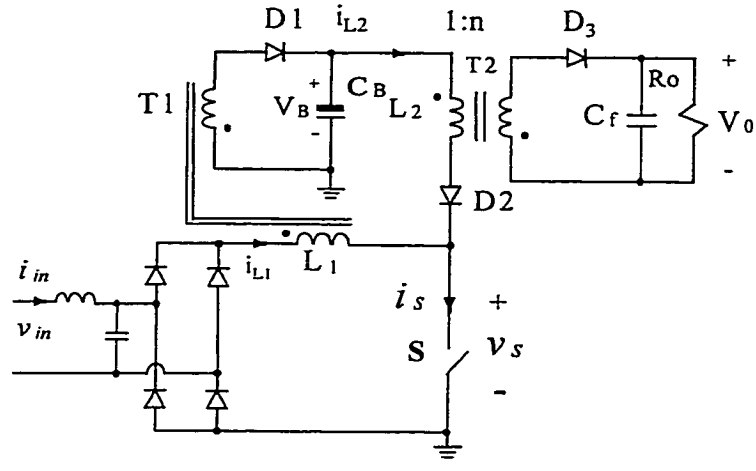


Fig. 3-4. S^2 converter consisting of two flyback converters.

a) (DCM + DCM) Operation Mode

To simplify analysis, C_B and C_f are considered to be large enough and ripple on the DC voltages can be omitted. Assuming all components being ideal (100% efficiency), it follows that,

$$P_{in} = P_{PFC} = P_{DC} = P_o \tag{3.1}$$

where P_{in} is average ac input power over half line cycle, P_{PFC} represents the delivered average power by PFC stage, P_{DC} is the delivered power by DC/DC stage and P_o is the output power on the load with rated voltage V_o and current I_o.

Taking quasi-static approach, i.e., the rectified line input voltage is assumed constant in one switching cycle, the average inductor current $i_{L1,ave}(t)$, during a switching cycle, is given by:

$$i_{L1,ave}(t)=\frac{v_{in}(t)D^2}{2L_1 f_s}=\frac{D^2 V_{in}}{2L_1 f_s}\sin\omega t \tag{3.2}$$

where D and f_s are the duty ratio and switching frequency, respectively, and the ac input voltage is given by $v_{in}(t)=V_{in}\sin\omega t$. So the $i_{L1,ave}(t)$ could be deemed to represent a moving average over switching cycle, T_s, during the line period, T_L.

The instantaneous input power over a switching period can be obtained as follows:

$$p_{in}(t)=i_{L1,ave}(t)v_{in}(t)=\frac{v_{in}^2(t)D^2}{2L_1 f_s}=\frac{D^2 V_{in}}{2L_1 f_s}\sin^2\omega t \tag{3.3}$$

The average ac input power P_{in} is averaging of P_{in} (t) over a half line cycle, it yields:

$$P_{in}=P_{PFC}=\frac{2}{T_L}\int_0^{T_L/2}p_{in}(t)dt=\frac{V_{in}^2 D^2}{4L_1 f_s} \tag{3.4}$$

According to the operation mechanism of the flyback converter under DCM, the average output voltage is given by:

$$V_o = V_B D \sqrt{\frac{R_o}{2L_2 f_s}} \tag{3.5}$$

where R_o represents the load resistance, and L_2 is the magnetizing inductor of T_2.

The average output power can be achieved:

$$P_{DC} = P_o = V_o I_o = \frac{V_o^2}{R_o} = \frac{V_B^2 D^2}{2L_2 f_s} \tag{3.6}$$

By equating Eqs. (3.4) and (3.6), the DC bus voltage on the capacitor is expressed by:

$$V_B = V_{in} \sqrt{\frac{L_2}{2L_1}} \tag{3.7}$$

From Eq. (3.7), the bus voltage is independent of the load condition, and is dependent only on the ratio of two magnetizing inductors and ac input peak voltage. Therefore, high bus voltage stress can be overcome by properly designing the ratio of two inductors.

b) (DCM + CCM) Operation Mode

For this operating mode, Eq. (3.4) holds true. For DC/DC block under CCM mode, we have:

$$V_o = nV_B \frac{D}{1-D} \tag{3.8}$$

where n is turns ratio of the transformer T_2, as shown in Fig. 3-4.

To guarantee balance between input and output powers, it follows:

$$P_{in} = P_o = V_o I_o \tag{3.9}$$

Substituting Eqs (3.4) and (3.8) into (3.9), we obtain:

$$V_B = \frac{1}{n}\left(V_{in}\sqrt{\frac{V_o}{4 f_s L_1 I_o}} - V_o \right) = \frac{1}{n}\left(V_{in}\sqrt{\frac{R_o}{4 f_s L_1}} - V_o \right) \tag{3.10}$$

It can be seen that V_B depends on, not only turns ratio and line voltage, but also load variation. A critical situation is that V_B will be infinite at no load condition. It is almost impossible to handle this issue in practical application.

Figure 3-5 shows bus voltage stress comparison under two different combinations. As is shown, the bus voltage is significantly dependent upon the load level under DCM + CCM mode. The bus voltage exceeds 2000V at light load and no device is available in this case. For DCM + DCM mode, bus voltage can keeps constant for variation load. This feature is pretty suitable for low power application.

3) Series-Charging, Parallel Discharging Capacitors Scheme (SCPDC)

A S^2 PFC converter with low capacitor bus voltage is proposed in [21]. Actually, it is a combination of a boost circuit and a forward circuit. There are two primary windings connected with separate bulk capacitors in series in isolated transformer of the

DC/DC stage. It is because of this unique structure, which makes the converter capacitors implement series-charging, parallel discharging capacitors scheme (SCPDC). The SCPDC means that the two energy-storage capacitors are charged in series when the switch is off and discharged in parallel when the switch is on. Thus, effectively, a two-to-one voltage division is introduced into the original single bulk capacitor, as far as most S^2 PFC converters hold, e.g., BIFRED and BIBRED converters. A similar structure converter, called as Russian circuit, is also described in [18,19]

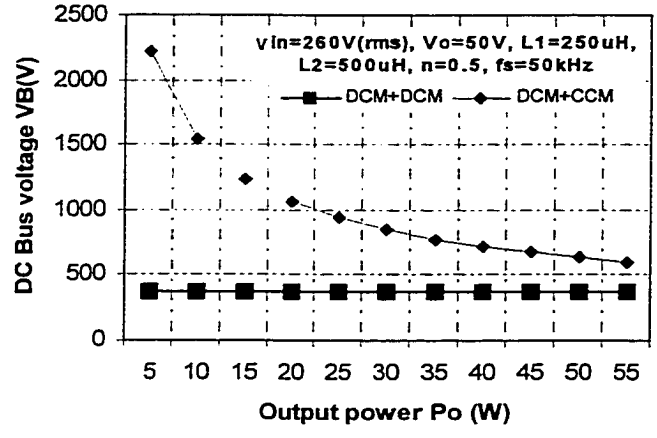


Fig. 3-5. Bus voltage stress comparison under two combinations.

In Fig. 3-6 converter, the two primary windings of the forward transformer are designed with the same turn ratio referring to the secondary winding (1:1:*n*). Inductances L_1 and L_2 ($L_1 = L_2$) are the leakage inductances of the forward transformer. From circuit steady-state analysis (assuming the components are ideal) [21], the bus voltages can be calculated by:

$$V_{CB1}=V_{CB2}=\frac{1}{2}V_o\left[\frac{1}{n}+\frac{kn\tau_n}{2D^2}+\sqrt{\left(\frac{1}{n}+\frac{kn\tau_n}{2D^2}\right)^2+\frac{2k\tau_n}{D^2}}\right] \tag{3.11}$$

where k and τ_n are defined as follows:

$k=\frac{L1}{L}=\frac{L_2}{L}$ — inductor ratio

$\tau_n=\frac{L}{R_o}f_s$ — normalized load time constant

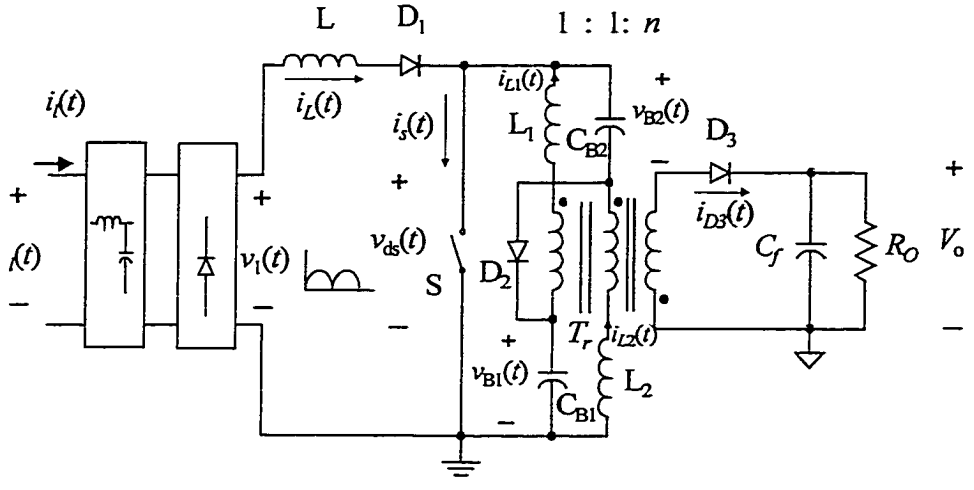


Fig. 3-6. A S^2 converter with low capacitor voltage.

To help in the closed-loop design of the above converter, a large signal modeling has been developed in [55] which makes it possible to simulate the close-loop schematic of the S^2 converter in a relatively short time. Figures 3-7 and 3-8 show the DC bus voltage as a function of the line voltage and output power, respectively. Figure 3-7 shows that the capacitor voltage can be controlled within 250 V, resulting in low rating

capacitors can be used as the bulky capacitors. The low DC bus voltage enables the converter to be applicable to universal input. Figure 3-8 shows that capacitor voltages are almost independent of the load condition, it is beneficial to optimize design of the DC/DC stage transformer and employ low rated voltage components.

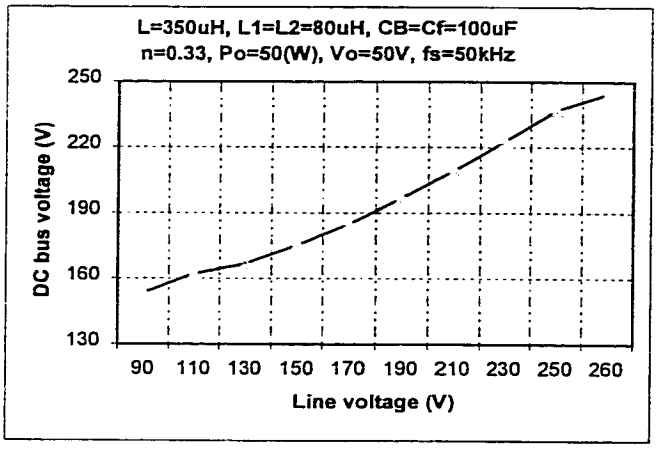


Fig. 3-7. Bus voltage stress at line voltage for the converter in Fig. 3-6.

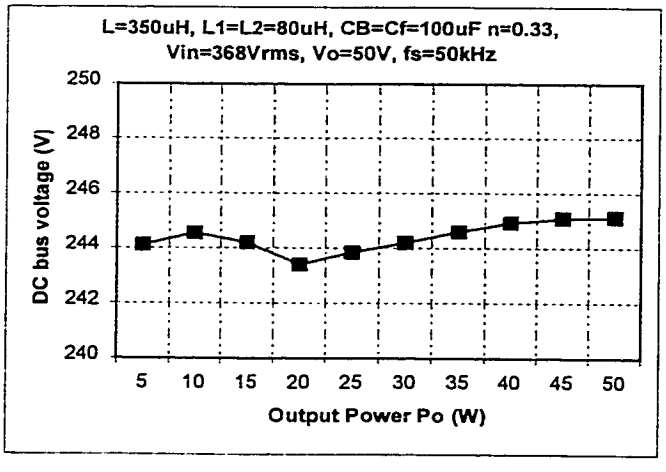


Fig. 3-8. Bus voltage at output power for the converter in Fig. 3-6.

To derive new topologies, it is helpful to generalize the SCPDC concept where N capacitors are charged in series and discharged in parallel. In fact, the concept had been used in "transformer-less DC/DC converters with large conversion ratios" [57]. Recently, employing the SCPDC idea, an AC/DC PFC converter with 3.3Vdc output was developed in [58], as shown in Figure 3-9.

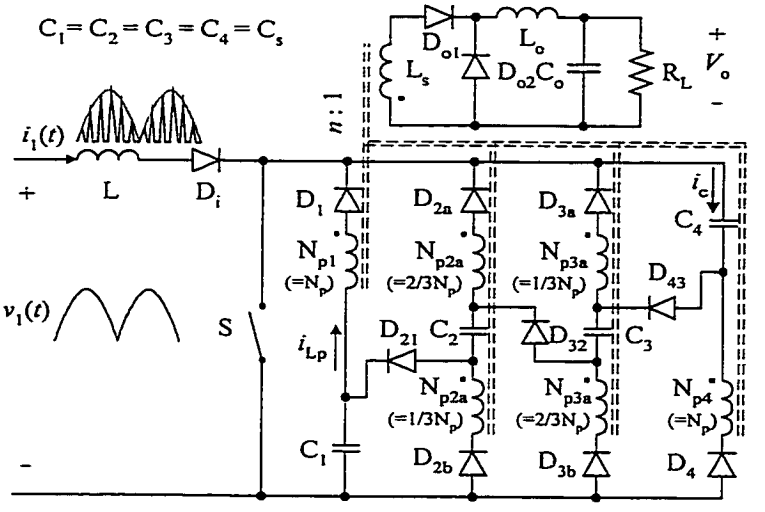


Fig. 3-9. A S^2 AC/DC converter implementing 3.3Vdc output.

4) Bus Voltage Feedback

Figures 3-10 and 3-11 show the basic BIFRED converter and the modified BIFRED converter with the bus voltage feedback. The basic BIFRED converter is actually a combination of a DCM boost converter and a DC/DC flyback converter. This converter is not practical due to high DC bus voltage caused by unbalance power between two functional blocks of PFC and DC/DC. Figure 3-12 shows simulated bus voltage variation with output power under high line voltage. The bus voltage exceeds 650 V

when load reaches 50 W, and the peak voltage of the switch exceeds 1000 V, resulting in impractical devices.

In the modified scheme, an additional transformer winding n_3 is added on the boost inductor branch in series. The winding can feedback the bus capacitor voltage when the boost inductor is charged, and the feedback strength depends on DC bus voltage level. The feedback depth will increase when the bus voltage has an increasing trend. Thus, the input power can be automatically reduced and the balance between input and output power can be guaranteed. As a result, the DC bus voltage is limited within a specified range. Furthermore, the feedback winding can provide a direct energy transfer from the input to the DC output. This brings an additional bonus of reduced component rating and increased efficiency. However, the penalty is while obtaining low bus voltage that input current waveform is deteriorated because of inductor current dead region caused by the feedback winding. Figure 3-13 shows simulated DC bus voltage variation under output power changing. The capacitor voltage is effectively suppressed within 450 V, and so a 450 V rated capacitor can be used.

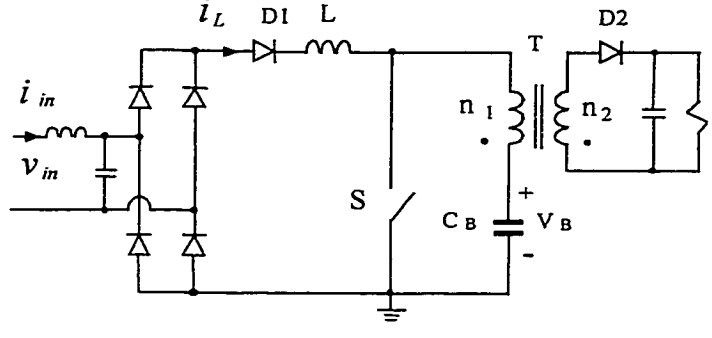


Fig. 3-10. Basic BIFRED converter.

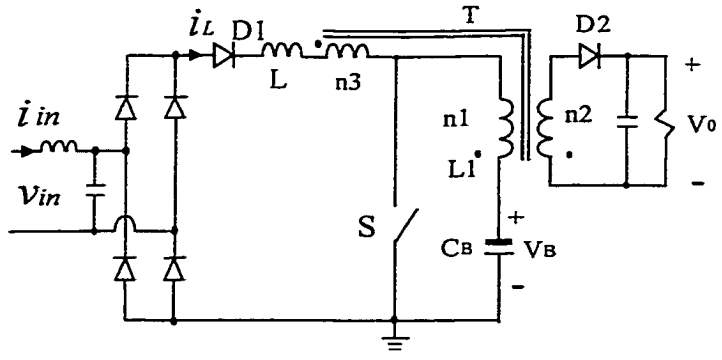


Fig. 3-11. BIFRED converter with DC voltage feedback.

Based on the concept of using bus voltage feedback, some of new topologies can be derived. In fact, this concept can be extended to any S^2 PFC converter, as long as the PFC function is based on the DCM boost converter. Several derived example circuits are demonstrated in [20].

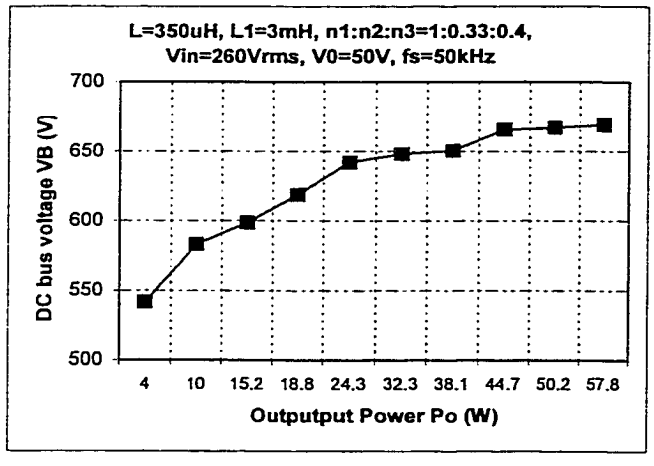


Fig. 3-12. DC bus voltage variation without bus voltage feedback.

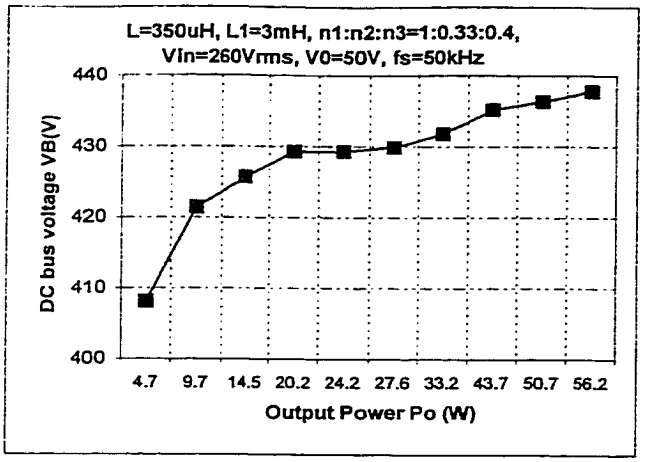


Fig. 3-13. DC bus voltage variation with bus voltage feedback.

3.2.3 Comparative Conclusions

In S^2 PFC converters, the DC bus voltage stress is one of the most important issues. The inherent reason of high DC bus voltage is in power unbalance between the input and the output. Through seeking for approaches to suppress bus voltage stress, it is helpful to derive and develop new topologies in the integrated S^2 PFC families. Four possible schemes to remove high bus voltage stress are analyzed in this section.

For method 1, DCM PFC + CCM DC/DC combination with variable frequency control, it is difficult to optimally design inductive components such as transformer and inductors for a wide range switching frequency control involved. For method 2, both functional blocks operate under same mode, i.e., (DCM PFC+ DCM DC/DC) and (CCM PFC + CCM DC/DC) combinations are practical. However, the former method takes a low efficiency because of high conduction loss; the latter, generally speaking, has relatively low power factor and high distortion in input current. For method 3, series-charging, parallel-discharging capacitors scheme is useful, it is a good scheme except that

additional bulk capacitor and fast diode are required. For method 4, DC bus voltage feedback, it is effective to suppress bus voltage while with a penalty of decreased THD. However, it is possible that to suppress the DC bus voltage as low as possible while keeping the input current harmonics below IEC standards. In summary, both the series-charging, parallel-discharging capacitors and the bus-voltage-feedback schemes are deemed to be more viable than the other two methods.

3.3 Optimization Design of Single Stage (S^2) Converters

The configuration of S^2 converters is relatively simpler than that of the conventional two stage counterparts, but each power stage of two stage converters can be optimized with individual controller. Whereas, optimized design of S^2 converters is very difficult because single power stage and controller has to complete double tasks as two-stage does. In this section, a procedure for optimizing converter design by limiting the bulk capacitor voltage stress and output current peak while obtain high efficiency and power factor is introduced. A 150 W universal input, 28V/5.4A full load power supply was built, and the theoretical prediction of key features has been verified experimentally. Original research objective was funded by STTR-NASA's project "Single-Stage Power Factor Correction Circuits".

3.3.1 Operation Principle of Example Converter

The proposed AC/DC converter is shown in Fig. 3-14. The input circuit is a boost circuit (formed by choke inductor L, diode D_1 and switch S). The switched-capacitor network consists of capacitors C_{s1} and C_{s2} and diode D_2, serving as a load to the input

circuit, and as a source to the output forward circuit (formed by transformer T_r and diode D_3). The two primary windings of the forward transformer is designed with the same turn ratio referring to the secondary winding (1:1:n). Inductances L_1 and L_2 ($L_1 = L_2$) are the leakage inductances of the forward transformer. It can be shown that, in steady-state, the proposed converter has four switching periods during one switching cycle. Table 3-1 shows the four operation periods and conducting devices during their corresponding time intervals. The equivalent circuits of the four operation periods are shown in Fig. 3-15 and key operation waveforms are depicted in Fig. 3-16.

In order to simplify analysis of the above time-variant circuit, we will employ "quasi-static" analysis method. That is to say, in one switching cycle the line voltage could be considered as a relatively constant voltage, represented by V_g in the equivalent circuits. Capacitors C_{s1} and C_{s2} are designed to be large enough and equal. Hence, in the steady-state analysis, each capacitor voltage is approximated by a dc source $V_{Cs1} = V_{Cs2} = V_{Cs}$.

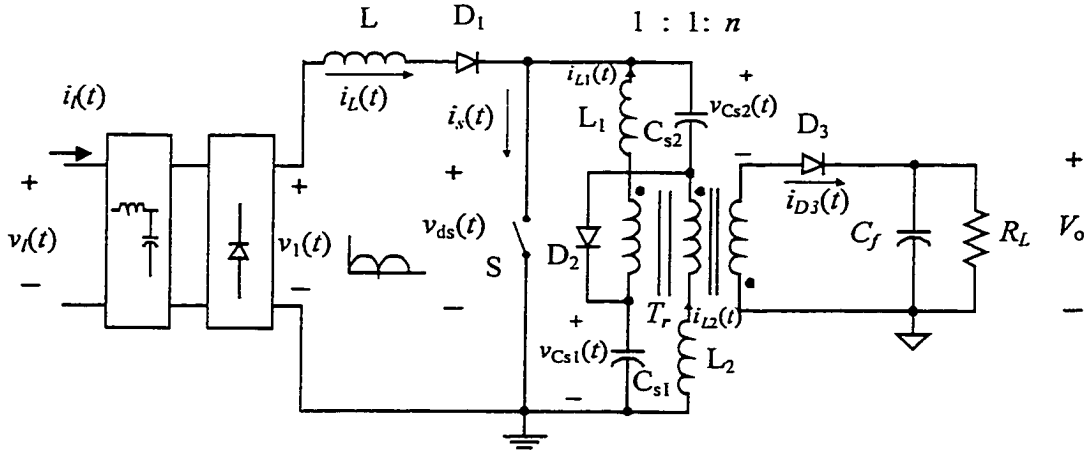


Fig. 3-14. Basic circuit schematic of the proposed two-storage capacitor converter.

Table 3-1 Four operation periods

Period	Time interval	Conducting device			
		S	D_1	D_2	D_3
P1	$t_0 \le t < t_1$	×	×		×
P2	$t_1 \le t < t_2$		×	×	×
P3	$t_2 \le t < t_3$		×	×	
P4	$t_3 \le t < t_0 + T_s$				

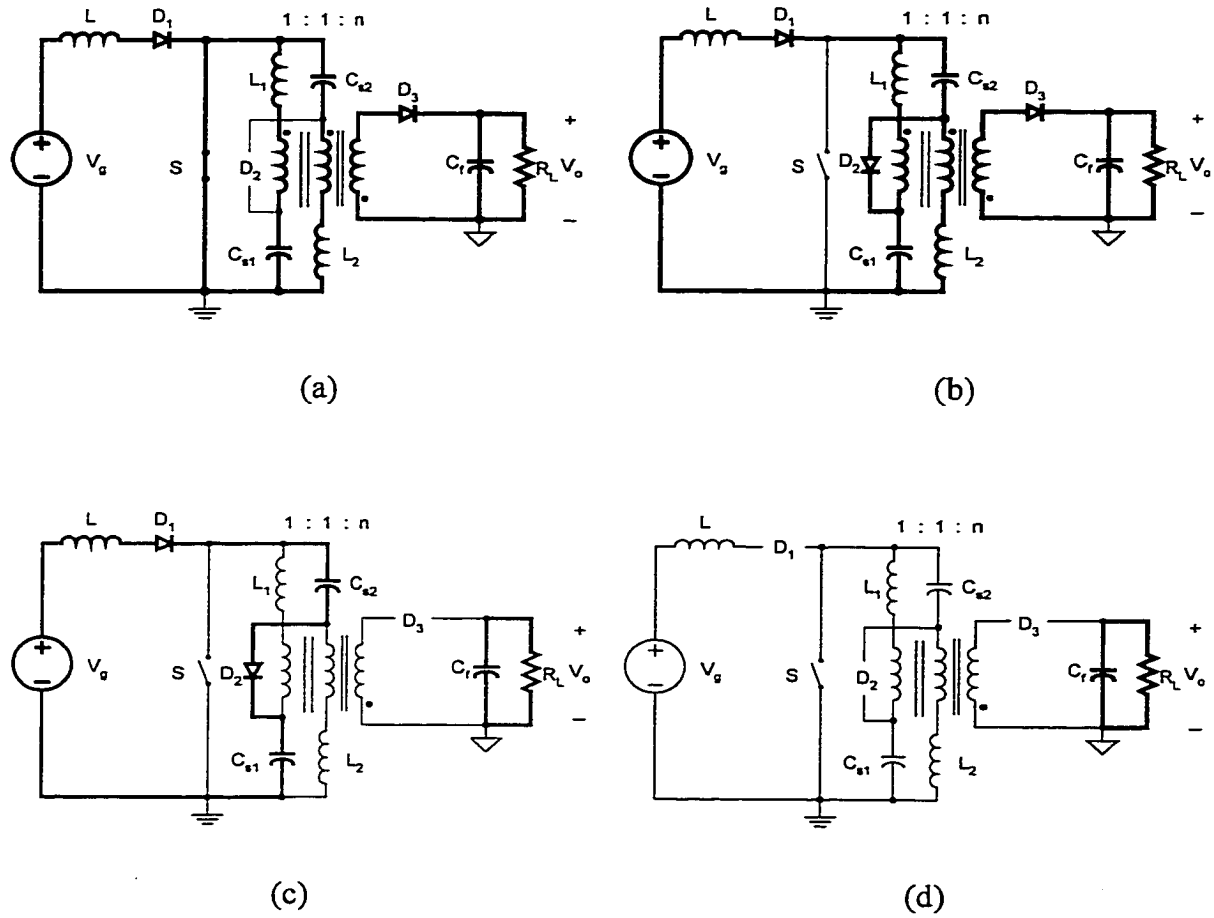


Fig. 3-15. Equivalent topologies for the four switching periods: (a) $P_1(t_0 \le t < t_1)$, (b) $P_2(t_1 \le t < t_2)$, (c) $P_3(t_2 \le t < t_3)$, and (d) $P_4(t_3 \le t < t_0 + T_s)$.

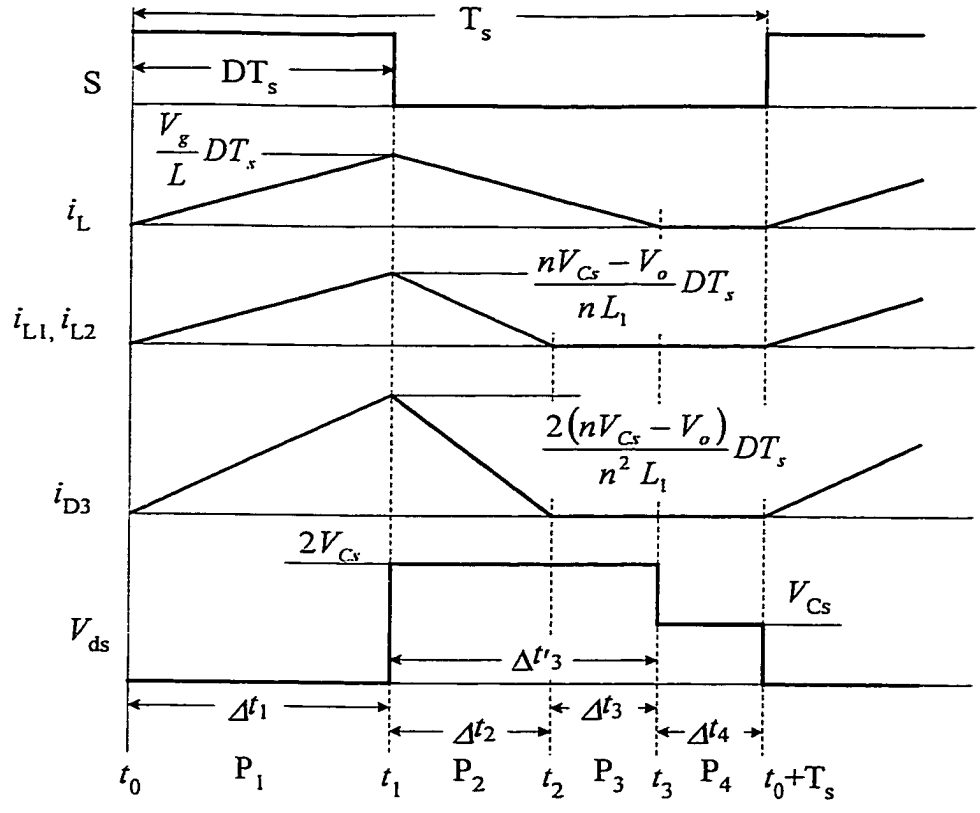


Fig. 3-16. Theoretical key waveforms of the proposed converter.

3.3.2 Circuit Equations and Averaging Model

The following section gives circuit equations corresponding to four switching periods discussed above:

3.3.2.1 Circuit Equations

Operation Period 1: During operation period 1, energy stored in bulk capacitors C_{s1} and C_{s2} are transferred to output side by forward mode. Meanwhile, boost inductor is being charged from ac input. By analyzing equivalent circuit Fig. 3-15 (a) we have:

$$i_L(t)=\frac{V_g}{L}t \tag{3.12}$$

$$i_{L1}(t)= i_{L2}(t)=\frac{nV_{Cs}-V_o}{nL_1}t \tag{3.13}$$

$$i_{D3}(t)=\frac{2(nV_{Cs}-V_o)}{n^2L_1}t \tag{3.14}$$

$$v_{ds}(t)=0 \tag{3.15}$$

where $V_g = V_{in}\sin\omega kT_s$, k represents kth switching cycles over half line cycle, and V_g could be regarded as a relatively static voltage during a switching cycle because T_s is very small as for line cycle T_L.

The duration of this period is:

$$\Delta t_1 = D_1 T_s. \tag{3.16}$$

where, $D_1=\frac{t_1-t_0}{T_s}=\frac{\Delta t_1}{T_s}=D$ is the regulated duty cycle by the controller.

Operation Period 2: During this period, boost inductor is discharging its energy into bulk capacitors C_{s1} and C_{s2}. At the same time, the forward transformer is being demagnetized. Its leakage inductor and magnetizing energy is fed back to capacitors C_{s1} and C_{s2} and also transfer to secondary-side. This period doesn't end until leakage inductor energy is completely discharged. By analyzing equivalent circuit Fig. 3-15 (b) we have:

$$i_L(t)=\frac{V_g}{L}DT_s-\frac{2V_{Cs}-V_g}{L}(t-DT_s) \tag{3.17}$$

$$i_{L1}(t)=i_{L2}(t)=\frac{nV_{Cs}-V_o}{nL_1}DT_s-\frac{nV_{Cs}+V_o}{nL_1}(t-DT_s) \tag{3.18}$$

$$i_{D3}(t)=\frac{2}{n}i_{L1}(t) \tag{3.19}$$

$$v_{ds}(t)=2V_{Cs} \tag{3.20}$$

The time interval Δt_2 is given by:

$$\Delta t_2 = t_2 - t_1 = \frac{nV_{Cs} - V_o}{nV_{Cs} + V_o} DT_s . \tag{3.21}$$

Operation Period 3: In circuit period 3, the choke inductor current, I_L, continues to decrease linearly, discharging its energy to capacitors. This period ends when the choke inductor current reaches zero. The key voltages and currents in this duration can be described as followed.

$$i_L(t) = \frac{V_g}{L} DT_s - \frac{2V_{Cs} - V_g}{L}(t - DT_s) \tag{3.22}$$

$$i_{L1}(t) = i_{L2}(t) = i_{D3}(t) = 0 \tag{3.23}$$

$$v_{ds}(t) = 2V_{Cs} \tag{3.24}$$

The time intervals are:

$$\Delta t_3 = \Delta t_3' - \Delta t_2 \tag{3.25}$$

where,

$$\Delta t_3' = \frac{V_g}{2V_{Cs} - V_g} DT_s . \tag{3.26}$$

Operation Period 4: The period 4 between t_3 and t_0+T_s is known as a free-wheeling stage, which is used to guarantee boost inductor operating in DCM in order to get high power factor. During this period, we have:

$$i_L(t) = i_{L1}(t) = i_{L2}(t) = i_{D3}(t) = 0 \tag{3.27}$$

$$v_{ds}(t) = V_{Cs} \tag{3.28}$$

The time interval is given by:

$$\Delta t_4 = T_s - DT_s - \Delta t_2 - \Delta t_3 . \tag{3.29}$$

3.3.2.2 Averaging Model

Any of the known ac line power factor correction converters is inherently a nonlinear time-varying system. Especially for proposed S^2 converter, two operation frequencies exist in the converter, i.e., low line frequency, f_L (50Hz or 60Hz) and high switching frequency, f_s. The input of the power stage is with a rectified sinusoidal waveform. These unique characteristics determine that 1) strict dynamic small signal model does not exist because the input is a sinusoidal large signal; 2) it is also impossible to obtain accurate DC model because the input is an ac signal. But we should pay attention to a fact that real-time duty-cycle varies only a little bit around a fixed duty-cycle during a sinusoidal input period, this is because duty-cycle mainly depends on the intermediate DC voltage of bulk storage capacitors (here V_{Cs1} and V_{Cs2}). Furthermore, DC voltage of bulk storage capacitors is kept almost constant during a line period due to a bulk capacitor capacitance. Therefore, to simplify the analysis, *the proposed converter can be approximated by replacing the dc input voltage and duty ratio in its equivalent dc/dc converter by using an rms input voltage and average duty ratio, respectively.* An approximate approach also exists for ac analysis. Assume that the ac line variations are much slower than the converter dynamics, so that the rectifier always operates near equilibrium. The quiescent operating point changes slowly along the input sinusoid, and we can find the slowly- varying "equilibrium" duty ratio. The converter small-signal transfer functions derived based on the quasi-static assumptions. The poles, zeroes, and gains vary slowly as the operating point varies, and thus a compensator can be designed. In the open literature, several authors have reported success using this method [53,55,59].

In the steady state analysis of the proposed converter and modeling derivation, specified unless otherwise, the following notations are defined:

V_{in}: rms value input voltage;

V_o: Output voltage;

V_{cs}: Average voltage across individual storage capacitor;

$T_s=1/f_s$: Switching period;

T_L: Line period

n: Transformer turns ratio (secondary to primary);

$D_1=\frac{t_1-t_0}{T_s}=\frac{\Delta t_1}{T_s}$: Duty ratio of period 1, drive control;

$D_2=\frac{t_2-t_1}{T_s}=\frac{\Delta t_2}{T_s}$: Duty ratio of period 2;

$D_3=\frac{t_3-t_2}{T_s}=\frac{\Delta t_3}{T_s}$: Duty ratio of period 3;

$D_4=\frac{t_4-t_3}{T_s}=\frac{\Delta t_4}{T_s}$: Duty ratio of period 4

D_{max}: Maximum duty ratio;

$\tau=L/R_L$: Time constant of the load;

$\tau_n=\tau/T_s$: Normalized load time constant;

$M=V_o/V_{in,rms}$: Ratio of dc output voltage to nominal ac input voltage;

$k=L_1/L=L_2/L$: Leakage inductor to boost inductor ratio;

$M_1=V_{cs}/V_o$: Intermediate dc bus voltage to output voltage ratio.

It should be indicated that the conversion ratio defined here by M is approximately equal to the one derived by using "DC substitution method" of quasi-static

method. Using state space averaging method for instantaneous Eqs. (3.12)-(3.29), we can obtain the following equations that describe relationship among duty-cycle, parameters and voltage regulation ratio (53):

$$M_1 = \frac{1}{8M^2 n}(n^2 k + 2Mn + 4M^2 + \sqrt{n^4 k^2 + 4n^3 kM + 24n^2 kM^2 + 4M^2 n^2 - 16M^3 n + 16M^4}) \tag{3.30}$$

$$D_1 = \frac{1}{2\sqrt{M_1}(M_1 n - 1)}\sqrt{2k\tau_n n(M_1^2 n^2 - 1)} \tag{3.31}$$

Based on the instantaneous equations corresponding to four operation modes, average equations to describe averaging circuit behavior can be derived as follows [53, 60]:

$$V_{in} - \left[2 \cdot V_{cs} \cdot (D_3 + D_2) + V_{in} \cdot D_4\right] = 0 \tag{3.32}$$

$$\frac{V_o}{R} = \frac{1}{2} \cdot (D_1 + D_2) \cdot \frac{(n \cdot V_{cs} - V_o)}{n^2 \cdot \frac{L_1}{2}} \cdot D_1 \cdot T_s \tag{3.33}$$

$$D_1 + D_2 + D_3 = \frac{I_{Lavg} \cdot 2}{\frac{V_{in}}{L} \cdot D_1 \cdot T_s} \tag{3.34}$$

$$0 = \frac{T_s}{2} \cdot \left[\frac{\left(V_{cs} - \frac{V_o}{n}\right)}{L_1} \cdot D_1 \cdot (D_2 - D_1) + \frac{V_{in} - 2 \cdot V_{cs}}{L} \cdot D_2 \cdot (D_2 + D_3) + \frac{V_{in}}{L} \cdot D_1 \cdot (2 \cdot D_2 + D_3) \right] \tag{3.35}$$

$$D_4 = 1 - (D_1 + D_2 + D_3) \tag{3.36}$$

$$0 = V_{cs} \cdot (D_1 - D_2) - \frac{V_o}{n} \cdot (D_1 + D_2) \tag{3.37}$$

The above equations describe function relationship among input and output voltages, intermediate dc voltage, circuit parameters and duty ratios corresponding to various operation periods.

3.3.3 Optimization Design Methodology

For a conventional two stage AC/DC converter, the first stage can be optimized in terms of low total harmonic distortion (THD) and low switch loss as well as diode loss. Usually, an average current method is used in PFC stage and thus boost inductor current operates in continuous current mode (CCM). The second stage can be optimized being considered approximately constant input dc voltage such that transformer turns ratio and switch duty ratio can be designed as large as possible. Larger turns ratio and duty-ratio, lower rms current and power loss will be resulted in primary and secondary sides of the isolated transformer in DC/DC down converter. However, it is a tough challenge to optimally design a S^2 converter, especially when operating under universal input voltage range (85~265V) is required. This may be the reason why so far no paper methodologically discusses optimization design procedure of S^2 converters.

In fact, two key operating parameters, intermediate DC bus voltage V_{cs} and duty ratio D_1, have an implied function relationship with the most critical design parameters, namely, transformer turns ratio n, boost inductor L and transformer leakage inductor to boost inductor ratio L_l/L. The function relationship has been included in the Eqs. (3.32)-(3.37). In this section, an optimization design methodology is presented for an example S^2 converter described above. The key point to implement optimization is to seek for the best trade-off in terms of small bulk capacitor voltage (dc bus voltage) range and high

duty ratio that means low rms and peak currents as well as low power loss. As a result, two important circuit parameters, turns ratio n and leakage inductor to boost inductor ratio L_l/L, will be obtained from this optimization design method. A universal input, 150 W output prototype at 28V@5.4A, designed by following the optimization procedure, was built. Also, theoretical predication and simulation are verified experimentally.

MathCAD will be used to implement calculation to search optimum parameter values. Through appropriately applying MathCAD's nonlinear solver to the averaging model Eqs. (3.32)-(3.37), circuit operation parameters can be solved. An example of MathCAD implementation of the valid solution set for the given converter parameters and initial values is demonstrated below:

The following initial parameter values are obtained from other MathCAD design document that is set up by circuit operation equations and regular design procedure of power converters.

Initial iterative parameters are given (in MathCAD expression):

$$L := 64 \cdot 10^{-6}\ \text{uH} \quad R := 5.227\ \text{ohm} \quad n := .25 \quad F_s := 100 \cdot 10^{3}\ \text{Hz}$$

$$V_{in} := 110\ \text{Vrms} \quad L_l := 10 \cdot 10^{-6}\ \text{uH} \quad D_1 := 0.3 \quad T_s := \frac{1}{F_s}$$

Solving process using MathCAD is demonstrated as follows:

Given (MathCAD code)

$$V_{in} - \left[2 \cdot V_{cs} \cdot (D_3 + D_2) + V_{in} \cdot D_4\right] = 0$$

$$\frac{V_o}{R} = \frac{1}{2} \cdot (D_1 + D_2) \cdot \frac{(n \cdot V_{cs} - V_o)}{n^2 \cdot \frac{L_1}{2}} \cdot D_1 \cdot T_s$$

$$D_1 + D_2 + D_3 = \frac{I_{Lavg} \cdot 2}{\frac{V_{in}}{L} \cdot D_1 \cdot T_s}$$

$$0 = \frac{T_s}{2} \cdot \left[\frac{\left(V_{cs} - \frac{V_o}{n}\right)}{L_1} \cdot D_1 \cdot (D_2 - D_1) + \frac{V_{in} - 2 \cdot V_{cs}}{L} \cdot D_2 \cdot (D_2 + D_3) + \frac{V_{in}}{L} \cdot D_1 \cdot (2 \cdot D_2 + D_3) \right]$$

$$D_4 = 1 - (D_1 + D_2 + D_3)$$

$$0 = V_{cs} \cdot (D_1 - D_2) - \frac{V_o}{n} \cdot (D_1 + D_2)$$

Now the circuit operation parameters can be solved below: Find (X) is a MathCAD code

$$\text{Find}(V_o, V_{cs}, D_2, D_3, D_4, I_{Lavg}) \text{ float}, 3 \rightarrow \begin{pmatrix} 1.89 & -235. & -15.8 & 28.1 \\ -.447 & 55.4 & -71.3 & 126. \\ -.338 & -.338 & 1.77 \cdot 10^{-2} & 1.77 \cdot 10^{-2} \\ 4.01 \cdot 10^{-2} & 37.2 & -.148 & .214 \\ .998 & -36.2 & .831 & .469 \\ 6.24 \cdot 10^{-3} & 95.9 & .437 & 1.37 \end{pmatrix} \tag{3.38}$$

MathCAD puts forward four potential solutions in Eq. (3.38). It should be noted that the fourth solution is the only physically possible choice. Therefore, the fourth solution should be considered the operating point regarding given parameter values. Actually, this solution also corresponds to the one arrived at by conventional analysis

techniques through comparing with simulated and experimental results and therefore the averaging model and calculation method have been verified.

To make the design procedure simple, the following assumptions are made:

1) Input boost inductor L is operated in DCM in the range of whole input and load;
2) Maximum duty ratio must be less than 0.5 in order to meet demagnetizing requirement (flux reset constraint);
3) A practical converter could be taken into consideration as an ideal converter with 100% efficiency when the converter is regarded as higher power output converter including loss. For instance, practical efficiency of a converter is 80% at nominal input and full load 150W. This converter could be approximately regarded as a converter that is processing the load of 187 W (equivalent 4.2Ω) with 100% efficiency.

The proposed optimization design procedure is as follows:

Step 1 — Preliminary design: For a set of given specifications, select roughly factor k and turns ratio n, then calculate basic circuit parameters such as L, L_1, $C_{s...}$, etc, and solve a set of initial values of operation variables D_1, D_2, D_3, D_4, I_{Lavg} and V_{cs} in Eqs. (3.32)-(3.37).

Step 2 — Optimize turns ratio n: For a given output power, find the optimum transformer turns ratio n (n_2/n_1) with which the bulk capacitor's voltages are acceptable and theirs swing ranges are as low as possible. Also must make capacitors and MOSFETs be commercially available from standpoints of cost and practical design considerations. The comparison study shows that the wide bus voltage range of the S^2 PFC converter will

require larger component ratings compared to the two-stage PFC converters. This is why the value of n dominates performance of the S^2 converter.

Step 3 — Optimize inductor ratio L_l/L: According to other circuit parameters obtained by steps 1 and 2, to select appropriate inductor parameters L and L_l so as to make duty cycle as large as possible under nominal line and full load condition, while meeting magnetic reset constraint at low line. This is because, for given basic circuit parameters, larger duty cycle generally results in lower ac rms current, higher efficiency and lower component stress.

Step 4 — Verification of optimized parameters with the worst case analysis: Generally speaking, the worst case usually appears either at the lowest input voltage or at the highest input voltage. Therefore, it is necessary to analyze the range of duty ratio and dc bus voltage under the highest and the lowest input voltages. This will be implemented by applying MathCAD's nonlinear solver to the averaging model Eqs. (3.32) - (3.37). The whole optimization process will be conducted by repeating steps 2, 3 and 4.

3.3.4 Design Example of A 150W S^2 Converter

3.3.4.1 Power Stage Design

Let us consider the following parameters for a specific example:

$V_{nom} := 110$ V_{rms} $V_{max} := 260$ V_{rms} $V_{min} := 85$ V_{rms} $V_{out} := 28$ V_{dc}

$P_{out} := 150$ W $f_s := 100 \cdot 10^3$ Hz $T_{line} := \frac{1}{60}$ S $\Delta V_{out} := \frac{1 \cdot V_{out}}{100}$

Equivalent load resistor $R := 4.2$ Ω considering 80% efficiency

Setting initial values $k := 0.2$ $n := 0.15$

Step 1 —preliminary design: Calculation process of major parameters is listed below:

From notation's definition and Eq. (3.30), we can calculate,

$M = 0.255 \qquad M_1 = 6.982$

Setting D_{max}=0.48, the duty cycle at nominal input voltage could be roughly selected by the empirical formula, and its final value will be determined by optimization design formulation,

$$D_1 = 0.1 + 0.6(D_{max} - 0.1) \tag{3.39}$$

This results in D_1=0.334. From Eq. (3.31), we can calculate inductances of L_1 and L_2 by MathCAD nonlinear solver. For given,

$$D_1 = \frac{1}{2\sqrt{M_1}(M_1 n - 1)}\sqrt{2k\tau_n n(M_1^2 n^2 - 1)} = 0.334 \tag{3.40}$$

solving for τ_n, we have,

$$\tau_n = 1.198$$

From notation's definition, the other parameters are obtained as follows:

$L := \tau_n \cdot R_L \cdot T_s \quad , \quad L = 5.032 \times 10^{-5}$

$L_1 := k \cdot L \quad , \quad L_1 = 1.006 \times 10^{-5}$

$\tau := \frac{L}{R_L} \quad , \quad \tau = 1.198 \times 10^{-5}$

Setting holding up time factor K_c=0.2 (this means 20% voltage drop during one cycle is permitted), we can determine storage capacitor's capacitances by equation,

$$C_{holding,up} = \frac{T_{line}}{K_c\left(1 - \frac{K_c}{2}\right)R_L M_1^2} \tag{3.41}$$

In the proposed converter, the holding up capacitance value should be the sum of capacitance values for two capacitors. It is calculated out $2C_s = 420uF$, so we can choose 220uF for each bulk capacitor.

Finally, a minimum capacitor of output filter can be selected by equation:

$$C_f = \frac{M_1\left(2DM_1 n - 2D - n^2 k\tau_n\right)^2 V_{out}}{\left(2nL_1 f_s^2\right)\left(M_1^2 n^2 - 1\right)\Delta V_{out}} \tag{3.42}$$

The capacitance is calculated as $C_f = 167uF$, also considering ESR limit required by output voltage ripples, probably two 220uF capacitors are suited for this use.

Based on the above designed parameters, a set of initial values of operation variables D_1, D_2, D_3, D_4, I_{Lavg} and V_{cs} in Eqs. (3.32)-(3.37) can be solved as follows:

Given and initially designed parameters are:

$L := 50 \cdot 10^{-6}$ uH $R := 4.2$ Ω $n := .15$ $f_s := 100$ kHz

$V_{in} := 110$ Vrms $L_1 := 10 \cdot 10^{-6}$ H $D_1 := .334$ $T_s := \frac{1}{f_s}$

Solved parameters is given by equation (MathCAD expression):

$$\text{Find}\left(V_o, V_{cs}, D_2, D_3, D_4, I_{Lavg}\right) \text{float}, 3 \rightarrow \begin{pmatrix} 1.57 & -361. & -20.2 & 28.1 \\ -.240 & 55.2 & -141. & 196. \\ -.350 & -.350 & 7.66 \cdot 10^{-3} & 7.66 \cdot 10^{-3} \\ 1.71 \cdot 10^{-2} & 76.9 & -.101 & .123 \\ .999 & -75.9 & .760 & .536 \\ 5.33 \cdot 10^{-3} & 283. & .883 & 1.71 \end{pmatrix} \tag{3.43}$$

Step 2 — Optimize turns ratio n: Based on the Eqs. (3.32)-(3.37), the following MathCAD function could be defined and the curves against between any two variables can be plotted in the equations from MathCAD expressions.

$$A(V_{in}, n) := \text{Find}(D_1, V_{cs}, D_2, D_3, D_4, I_{Lavg})$$

$$n := 0.1, 0.11 .. 0.5 \quad , \quad V_{cs}(V_{in}, n) := A(V_{in}, n)_1 \tag{3.44}$$

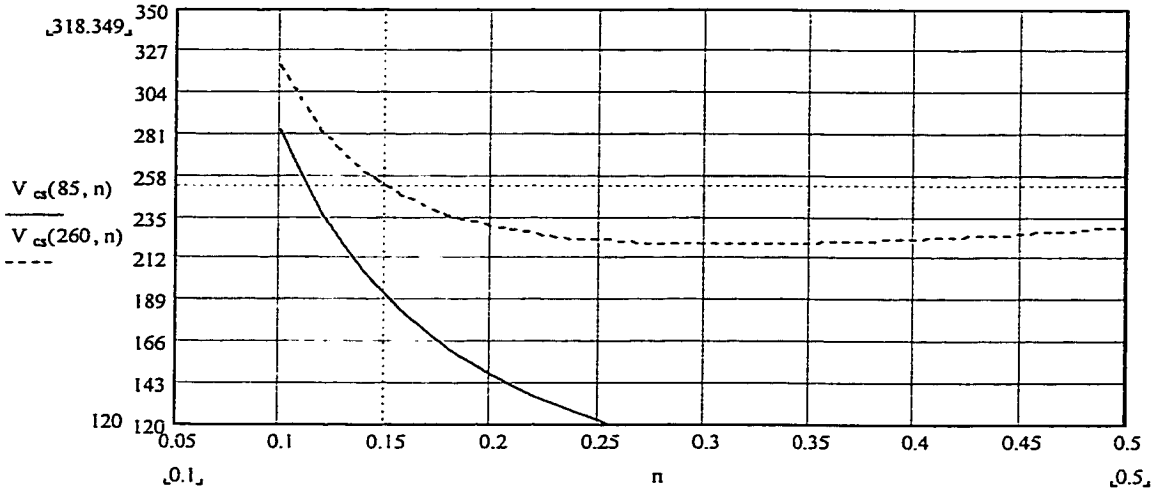


Fig. 3-17. Storage capacitor's voltage vs. turns ratio under high line and low line at full load (specs: V_o=28, L=50uH, R=4.2ohm, f_s=100kHz, L_1=10uH, steady-state nominal D_1=0.334).

Figure 3.17 shows storage capacitor's voltage V_s as a function of the turns ratio under high line and low line input at full load output. Through plotting of several curves under different output loads, it is shown that V_{cs} is independent of the load. According to optimization criteria of transformer turns ratio *n* (n_2/n_1) from the above optimization methodology. Figure 3-17 indicates that proper turns ratio could be in the range of 0.13 - 0.16. V_{Cs} varies from 220V to 270V if *n* is selected as 0.13 and V_{cs} varies from 190V to 250V if *n* is selected as 0.15. However, V_{Cs} should be lower than 250V such that a 600V MOSFET is applicable as an active switch. Its trade-off between dc bus voltage range

and MOSFET voltage stress ($2V_{cs}$), it seems that a 0.15 turns ratio is preferable. Figure 3-18 shows storage capacitor's voltage varying with input voltage under different *n* at full load, it verifies that the selected *n* can make the converter operating under universal input.

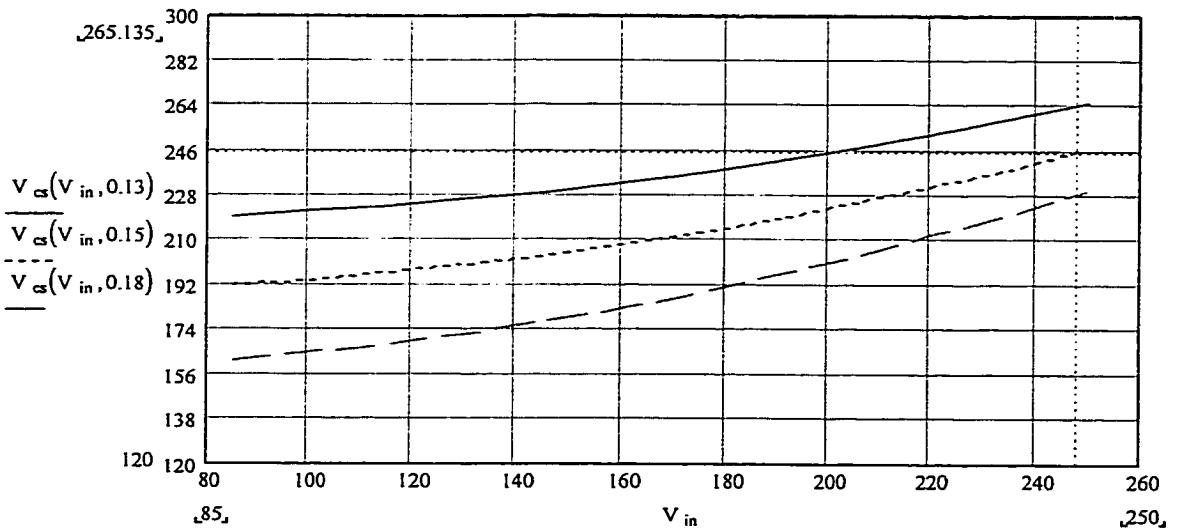


Fig. 3-18. Storage capacitor's voltage vs. input voltage under different turns ratio *n* at full load (specs: V_0=28, L=50uH, R=4.2ohm, f_s=100kHz, L_1=10uH, n=0.15, C_s=220uF, steady-state nominal D_1=0.334).

Step 3 — Optimize inductor ratio L_1/L: Recall that the criteria of this step is to select appropriate L and L_1 to make D_{max} safely lower than one required by magnetic constraint-demagnetizing. Figure 3-19 shows that under typical turns ratio n, duty cycle curves vary with inductance of the choke inductor. Figure3-20 shows duty cycle curves varying with inductance of the choke inductor under typical input voltages. It is found that the higher the inductance, the higher is the duty cycle. But too high duty cycle will degrade the regulation capability of the converter, for instance, a rated output voltage can't be achieved at low line input condition. Thus an L of 60 uH and an L_1 (L_2) of 10 uH

selection may be reasonable, which corresponds a near 0.36 duty cycle at nominal input voltage, this will be further identified by step 4. On the other hand, it is observed that we have chance to design larger turns ratio *n* if the L is selected relatively larger.

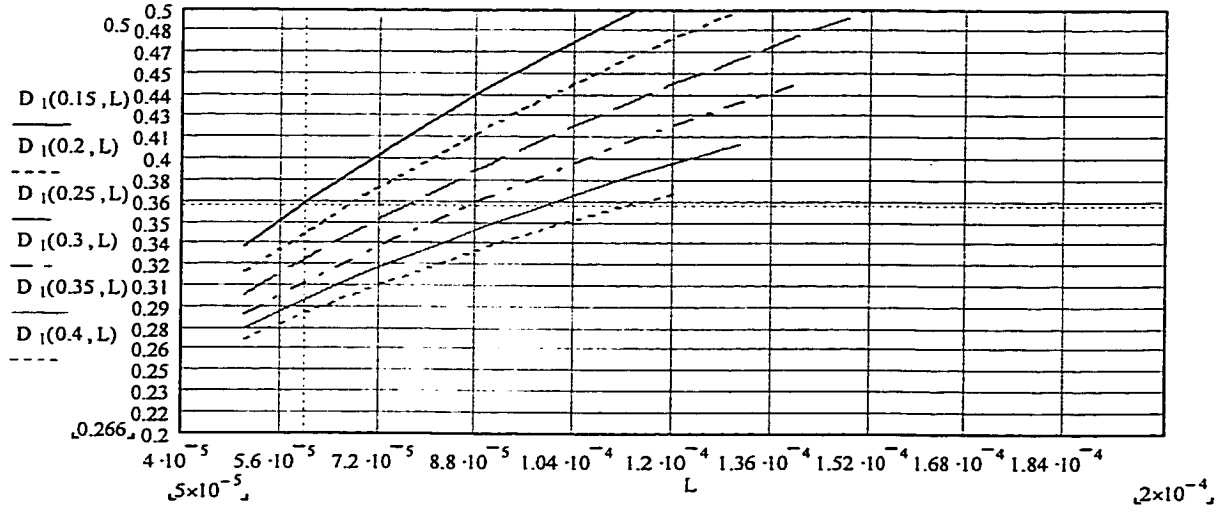


Fig. 3-19. Duty cycle curves vs. inductance of the choke inductor under typical turns ratio *n* (specs: V_o=28, R=4.2ohm, f_s=100kHz, L_1=10uH, V_{in} =110 V_{rms}, C_s=220uF).

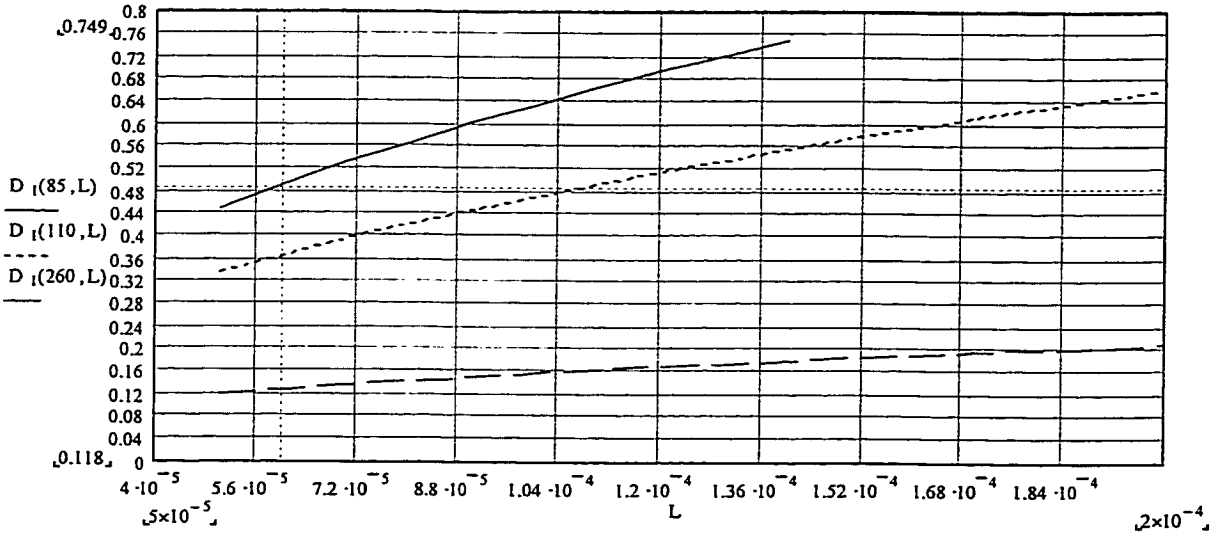


Fig. 3-20. Duty cycle curves vs. inductance of the choke inductor under typical input voltages (specs: V_o=28Vdc, R=4.2ohm, f_s=100kHz, L_1=10uH, n=0.15, C_s=220uF).

Step 4 — Verification of optimum parameters with the worst-case analysis: Based on the above design parameters, two key operation parameters, i.e., duty-cycle and dc bus voltage under typical inputs, including worst input cases, while keeping same circuit parameters, can be calculated as follows:

1) Input voltage 85V and full load, D_1=0.491 and V_{cs}=192Vdc.
2) Input voltage 110V and full load, D_1=0.365 and V_{cs}=195Vdc.
3) Input voltage 265V and full load, D_1=0.127 and V_{cs}=252Vdc.
4) Input voltage 265V and 10% load, D_1=0.0.04 and V_{cs}=252Vdc.

The above results show that maximum duty ratio D1=0.491, less than 0.5, meeting flux reset constraint, and dc bus voltage is controlled within 260Vdc and thus 600V MOSFET is applicable.

Similarly, from MathCAD, we obtain Figs. 3-21 and 3-22 that verify the two important converter performance, namely, line and load regulation capability. From these two drawings a less than 0.5 duty cycles can always be got at full range of input voltage and from (1/10) to full load range.

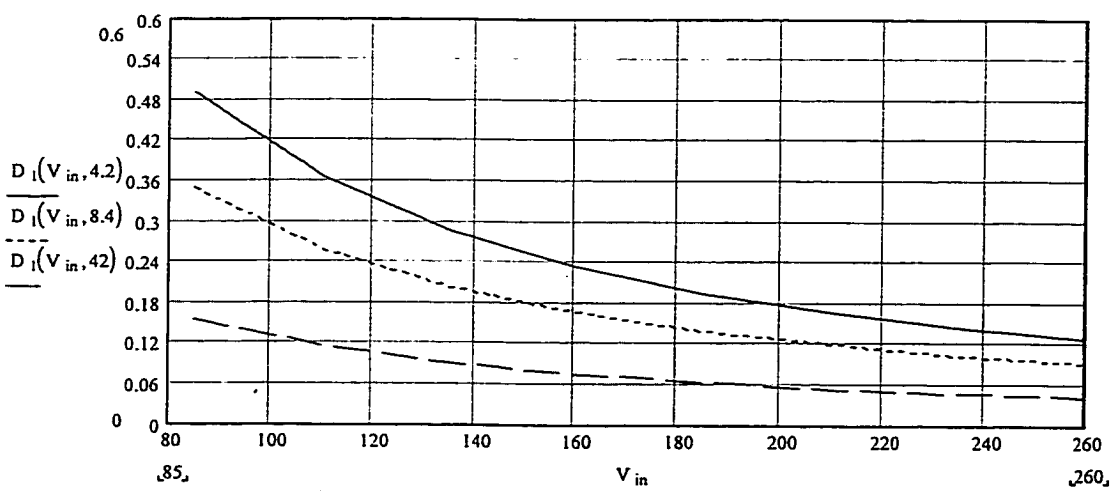


Fig. 3-21. Duty cycle curves vs. input voltage.

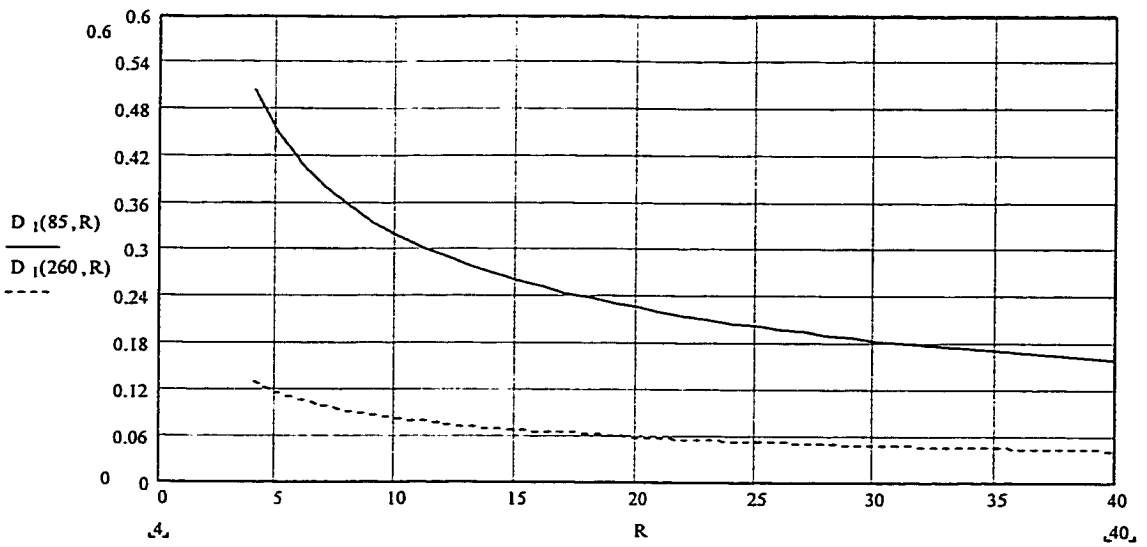


Fig. 3-22. Duty cycle curves varying with load under high line and low line input voltages.

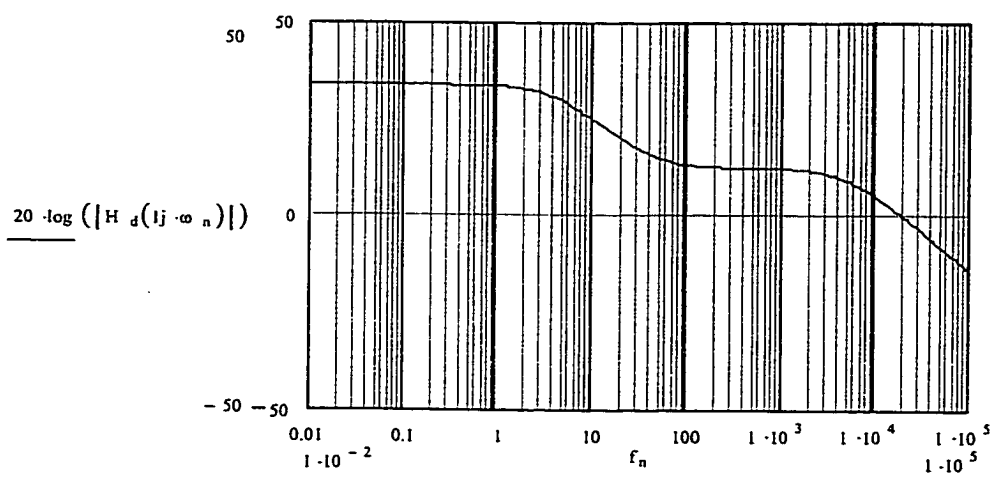
3.3.4.2 Controller Design

The control of S^2 converter is also essential to obtain maximum performance based on the optimized power stage circuitry. Basically, converter use closed loop feedback to achieve design objectives for line and load regulation and dynamic response. Fortunately, the control-loop systems used in the power converters are usually not very complex, permitting the use of simple analytic techniques to achieve loop stabilization. A simplified version of the Nyquist stability criteria can be used because unity gain crossover occurs only once in the gain vs. frequency characteristic [59,60]. Bode plots provide a simple and powerful method of displaying and calculating the loop gain parameters. Controller design completed in this work is just based on the investigation of Bode plots after and before adding control loop compensator. An averaging model

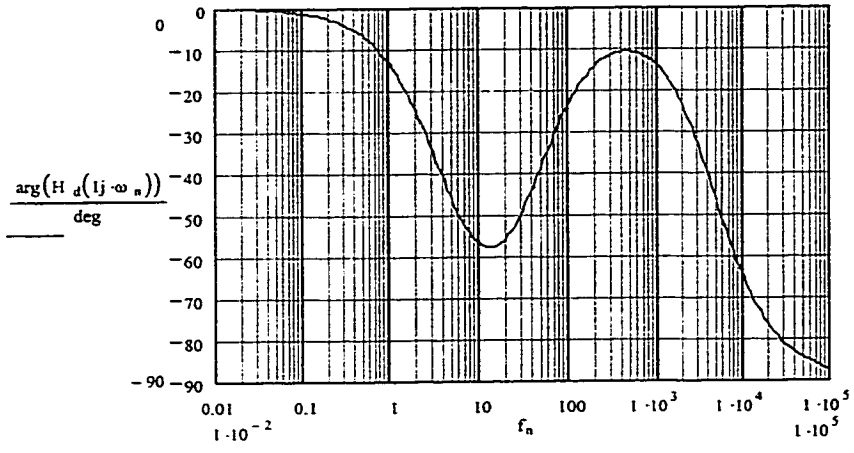
derived in [53] is used to set up original transfer function with MathCAD tools and simulation platform. An example is taken to show whole design process. In fact, this design procedure is also suited for other similar converter applications.

Equation (3.44) expresses an open loop transfer function derived from averaging model of an example converter. Figure 3-23 shows Bode plot of the open loop transfer function, $H_d(s)$, with the designed parameters: output power 165W, R=4.75Ω, n=0.16, L=100uH, L_1=L_2=16uH, C_s=200uF, V_{in}=110V_{rms}, V_{out}=28V_{dc} and f_s=100kHz.

$$H_d(s) := \frac{\left(1.19\cdot10^{3}\cdot s + 3.35\cdot10^{5}\right)}{\left(9.74\cdot10^{-3}\cdot s^{2} + 288.\cdot s + 6.82\cdot10^{3}\right)} \tag{3.44}$$



(a) Gain



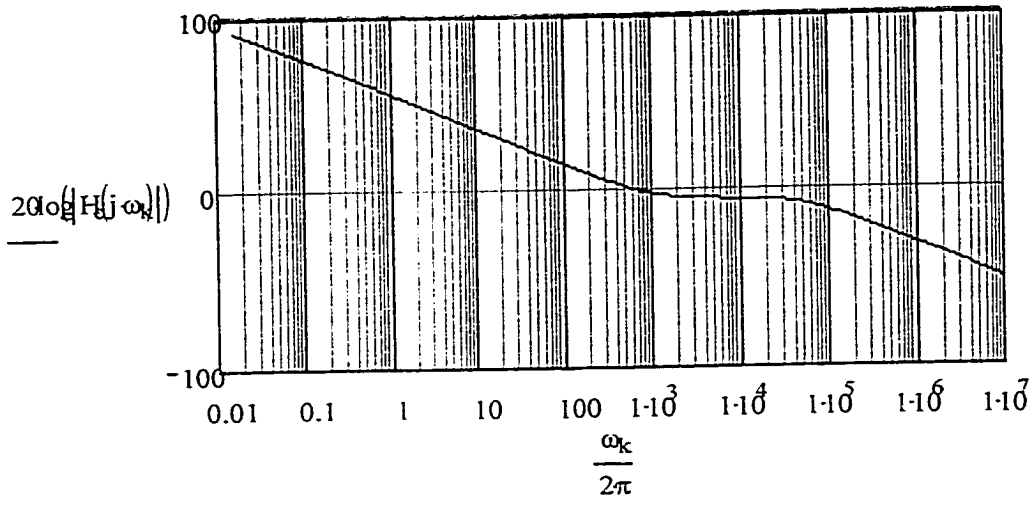
(b) Phase

Fig. 3-23. Bode plot of open loop transfer function of power stage: (a) gain, and (b) phase.

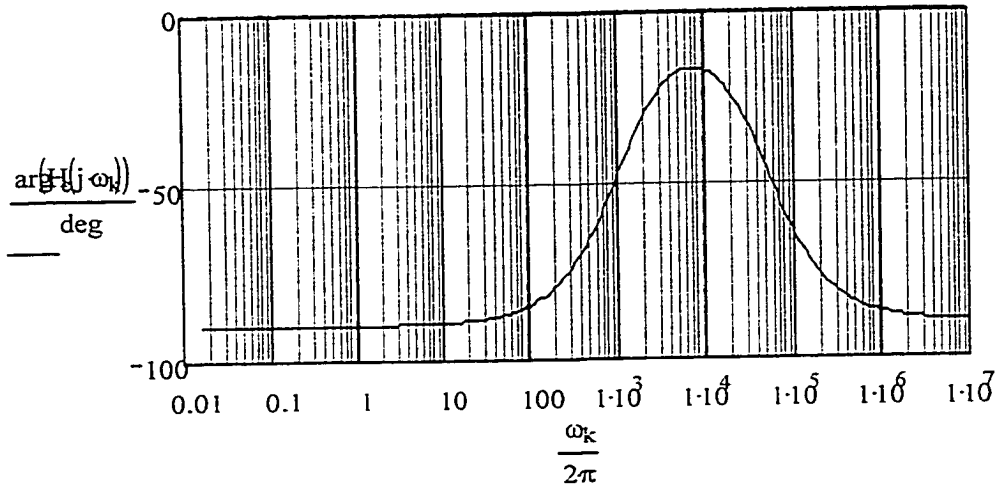
A one-pole not at the origin, and one-zero compensator will be employed to achieve desirable loop crossover frequency 10kHz (here 1/10 switching frequency) and enough phase margin, which is required by system stability. Equation (3.45) is the transfer function of compensator, and Fig. 3-24 shows the Bode plot of the Eq. (3.45). Note minus sign is canceled by minus sign on summer in the control loop.

$$H_c(s) := G_0 \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{s \cdot \left(\frac{s}{\omega_{p1}} + 1\right)} \tag{3.45}$$

where G_0 is the dc gain and W_{z1} and W_{p1} are respectively the zero and pole of the transfer function.



(a) gain

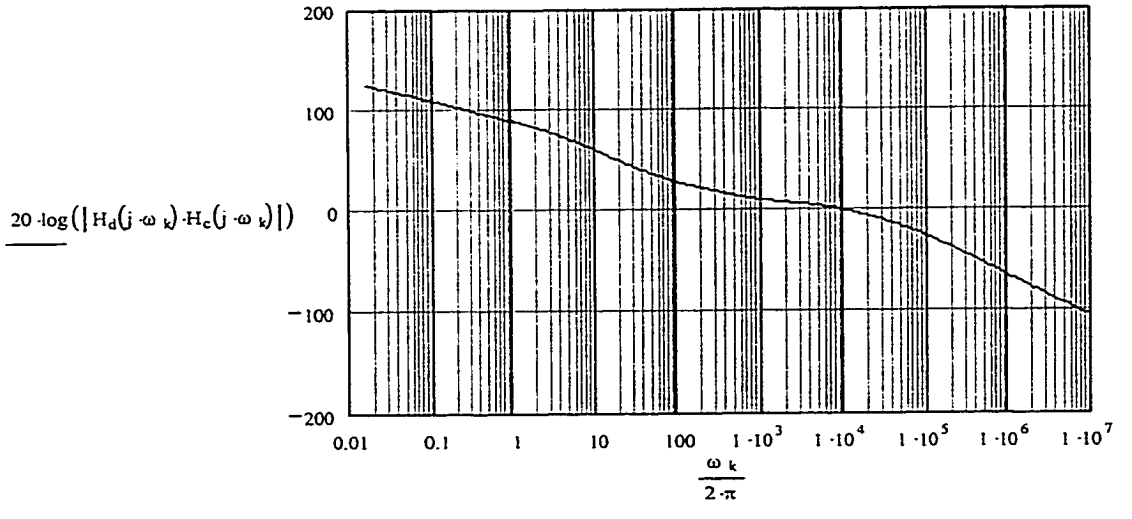


(b) phase

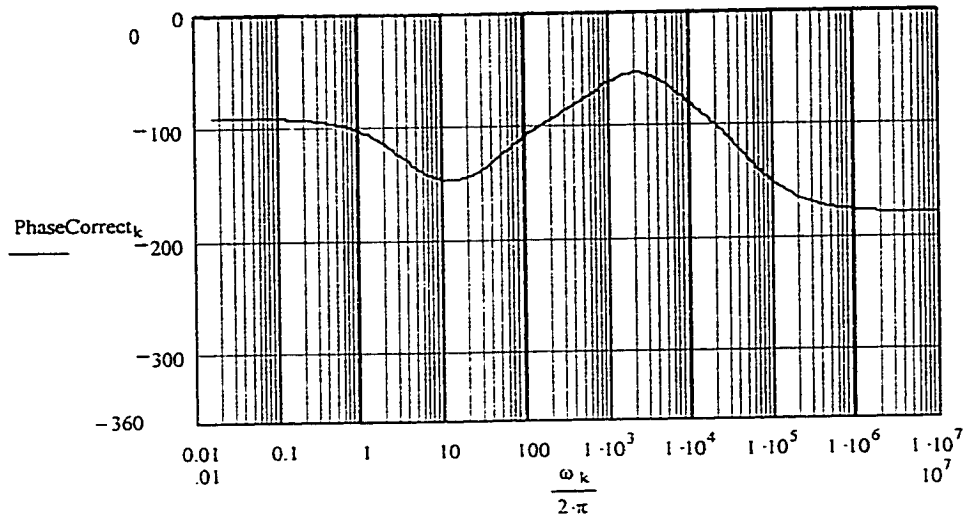
Fig. 3-24. Bode plot of compensator transfer function: (a) gain, and (b) phase.

Closed-loop loop gain is verified by the investigation for Bode plot of closed loop control, as shown in Fig. 3-25. We found design outcomes with crossover-frequency 10kHz and phase margin larger than 65° usually required by system stability.

Finally, it should be emphasized that most of designers misunderstand a fact that *S^2 converter control design should follow a rule, i.e., closed-loop gain should be designed with enough low crossover frequency, say 25Hz, far lower than ½ of the second order harmonic (120Hz) that is drawn through utility 60Hz ac input source [55].* Indeed, the rule is applicable for other PFC Boost front-end rectifiers where averaging current mode (two loops) is used and outer loop voltage feedback signal will substantially carry the second order harmonic (120Hz) component. The second order harmonic component will further affect the output of compensator and thus it probably make the output of the PFC stage unstable and contain the same order harmonics. *However, for most of S^2 converters, DCM operation mode is picked up and thus high power factor will be automatically achieved.* In this way, the controller can be designed in charging of only DC/DC regulation. Therefore, we can conclude that the S^2 controllers can be designed like those of regular DC/DC converters.



(a) gain



(b) phase

Fig. 3-25. Bode plot of closed loop transfer function: (a) gain, and (b) phase.

3.3.5 Simulated and Experimental Results

3.3.5.1 Simulated results

By using the above designed circuit parameters of the proposed S^2 converter, the closed-loop PSPICE large signal and small signal simulations have been carried out. Figure 3-26 shows simulated schematics for transient in time domain. Simulated results, using the compensator with loop crossover frequency at about 1kHz, are shown in Fig. 3-27. Note that it would take much-much time (about 8hrs on computer of 500MHz CPU) to complete simulation if the crossover frequency were designed at very low, say 25kHz. This is because system response is too slow, particularly for the case at large signal ac input. Figure 3-28 shows the simulated results with the compensator that make loop gain crossover frequency at about 14kHz (1/7 switching frequency). Obviously we found that higher crossover frequency, faster transient response. The former has settling time about

15ms, and the latter has settling time only 2ms and overshoots only 0.5 V. Figure 3-29 shows simulated schematics to conduct small signal analysis through using averaging circuit model. Note that a quasi-static method has been used in the simulation schematics, that is to say, a 110Vdc voltage source is used to substitute ac source with 110Vrms value. In the schematics, V_{10} represents injection signal (varying duty cycle) including steady state duty cycle, here DC component 0.362, and small signal ac component with magnitude of one. The closed-loop is cut at the limiter cascaded after the compensator. Therefore, loop gain can be directly obtained by measuring the voltage on the R_{21}. Figure 3-30 shows a simulated Bode plot based on the Fig. 3-29.

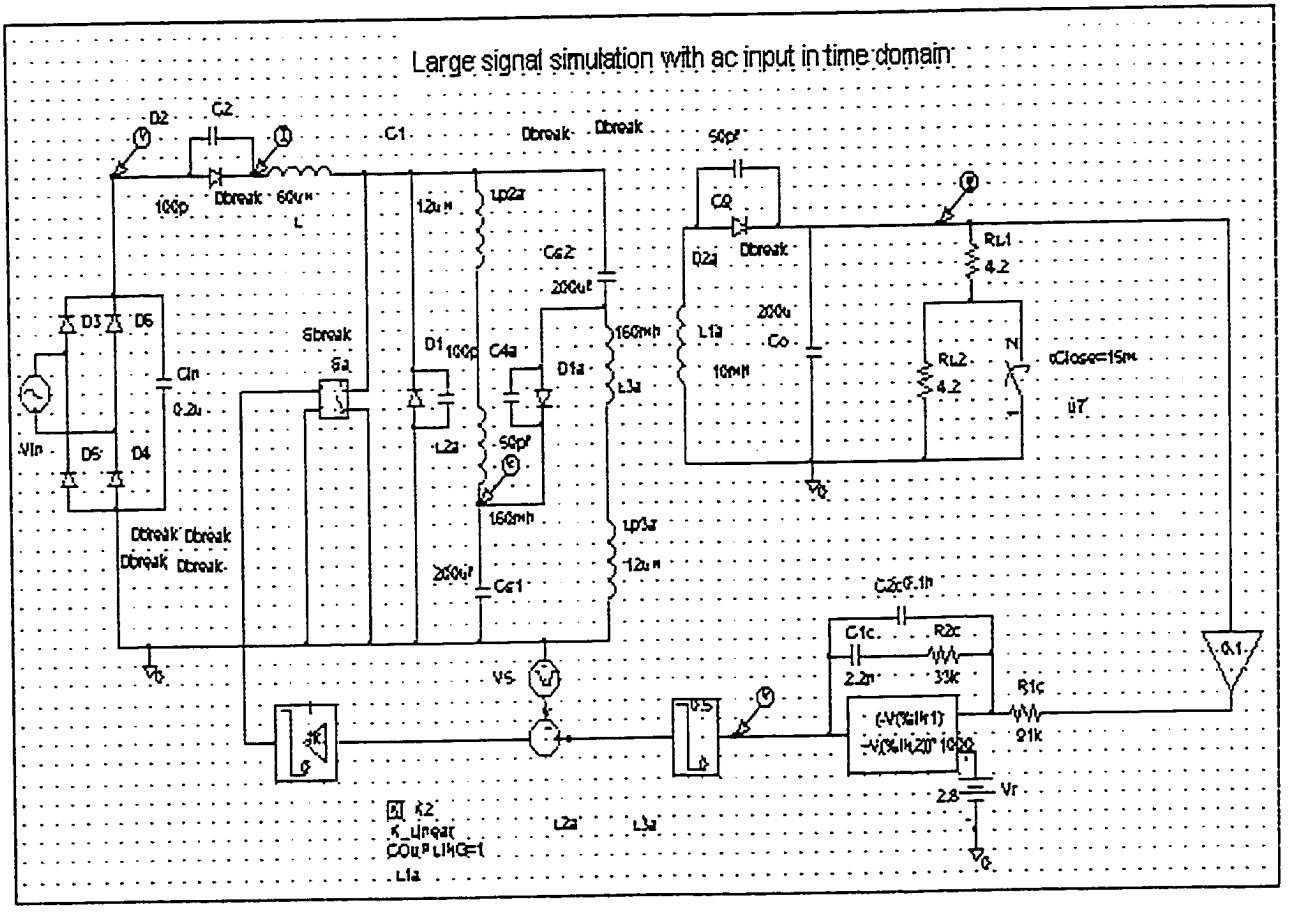


Fig. 3-26. Simulated schematics for transient in time domain.

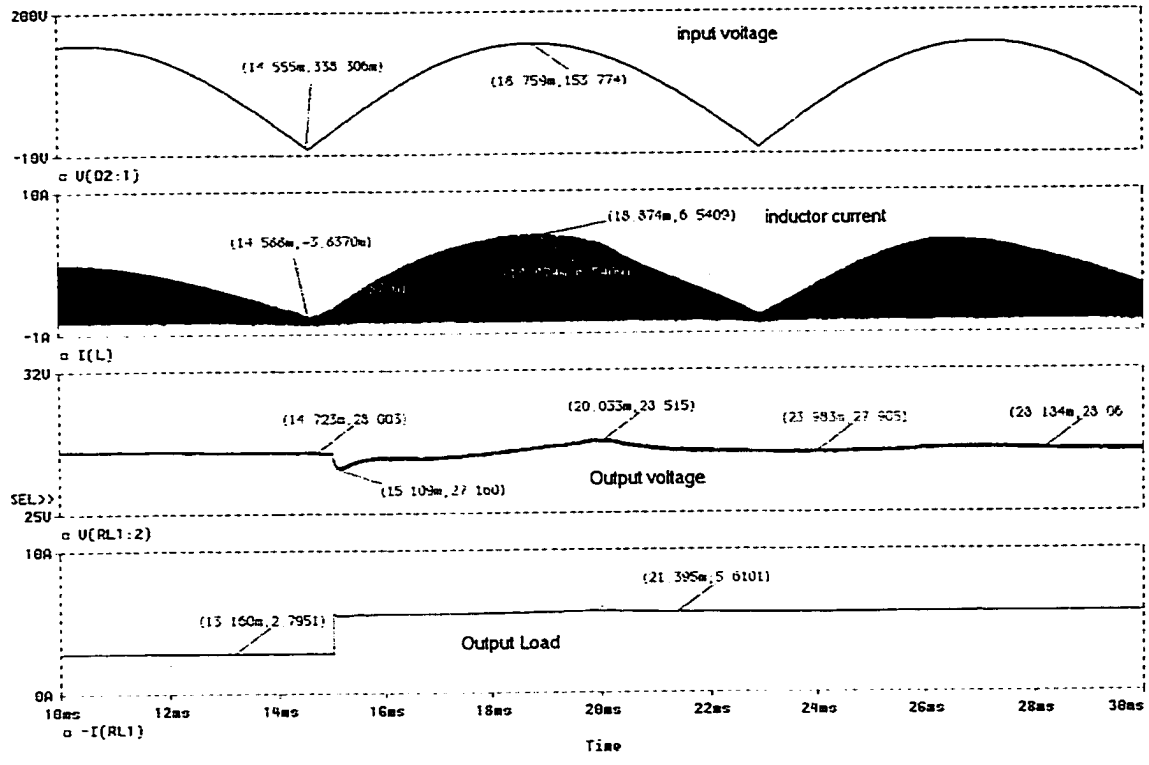


Fig. 3-27. 50% step up response with loop crossover frequency at about 1 kHz.

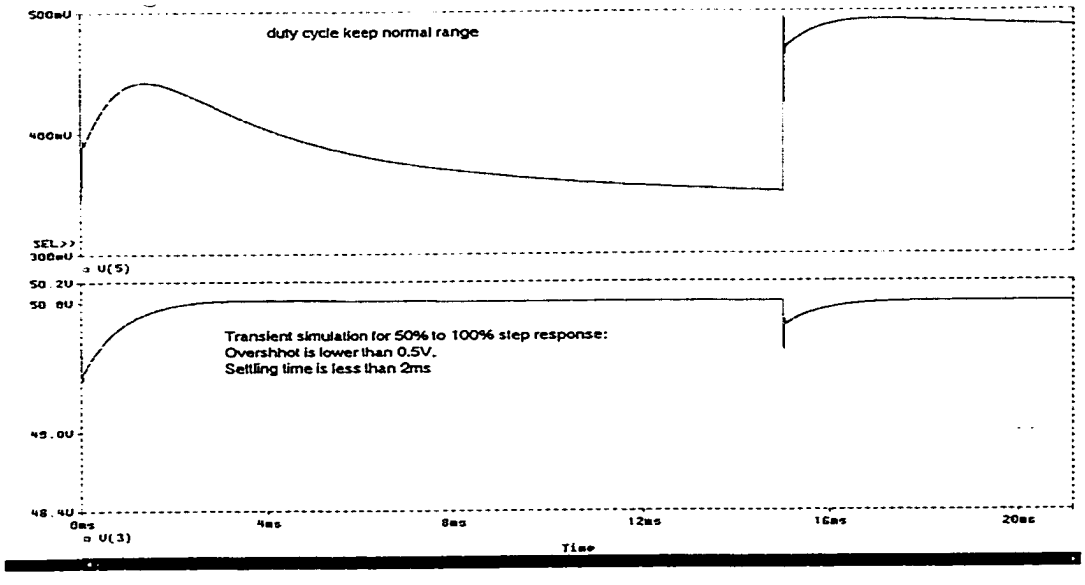


Fig. 3-28. 50% step up response with loop crossover frequency at about 14 kHz.

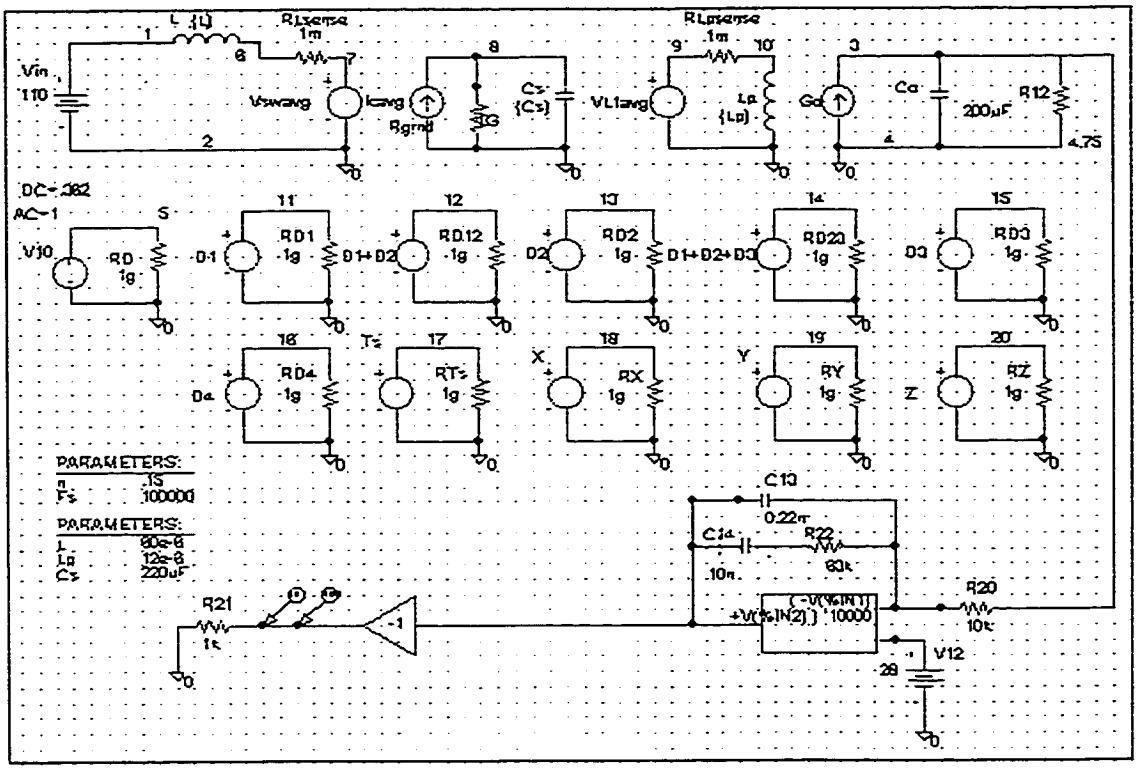


Fig. 3-29. Simulated schematics of small signal analysis with averaging model.

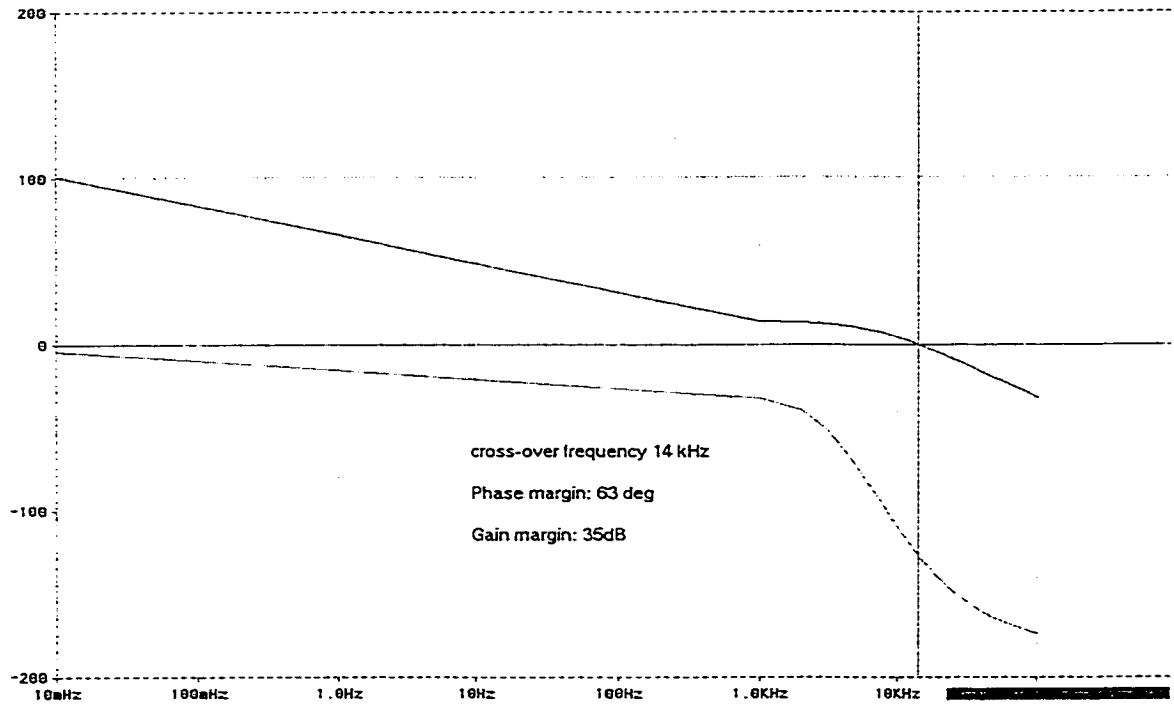


Fig. 3-30. Simulated Bode plot based on the Fig. 3-29.

3.3.5.2 Experimental results

An experimental testbed prototype of the converter has been built in the laboratory, as shown in Fig. 3-31. We called prototype as testbed is because it is built with design considerations to make component replacement convenient. The forward transformer was created with a Philips ETD-PST39 core. To obtain the designed transformer ratios n and proper leakage inductance, the primary windings and secondary winding were built with different structure, variation inductances and coupling way, respectively. Pulse-width-modulation control chip UC3825 was used to achieve closed-loop control. The experimental waveforms of filtered line current, and voltage and current at the switch, shown in Fig. 3-32, were recorded by using hp54542A oscilloscope. Both the simulated and the experimental waveforms agree well and show that the waveforms of the line current is almost sinusoidal one, proving that a good power factor can be achieved by this converter topology.

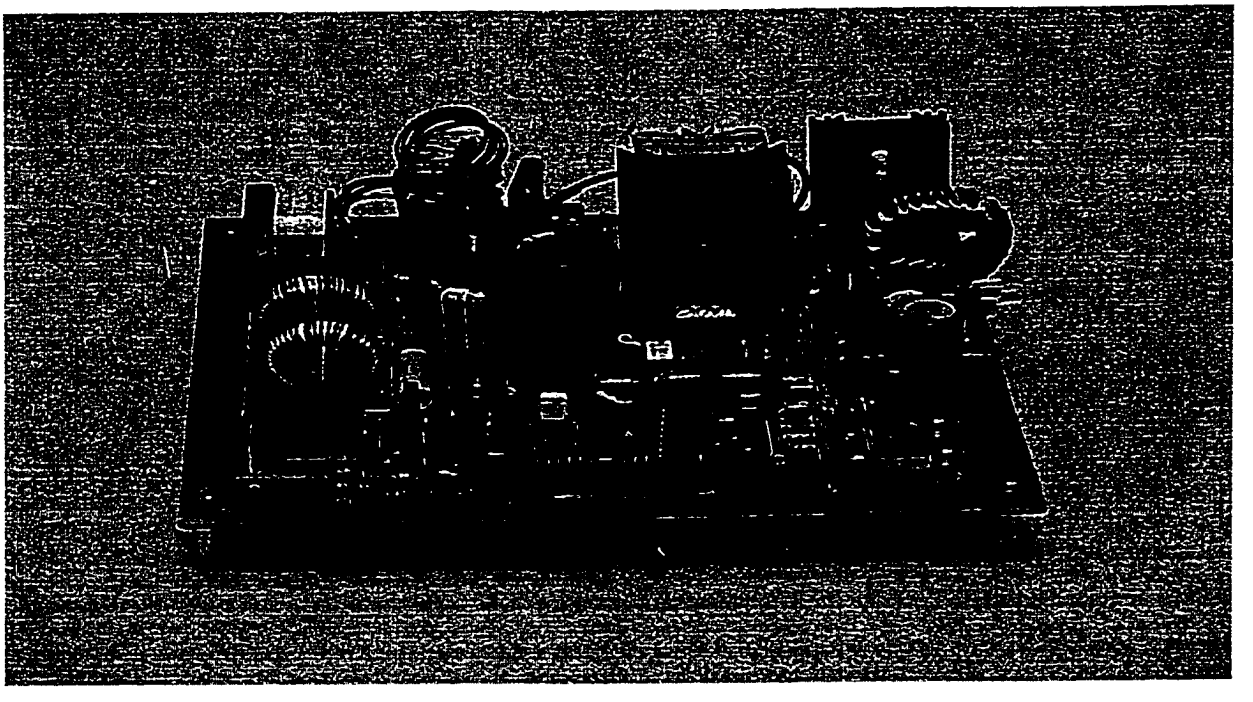
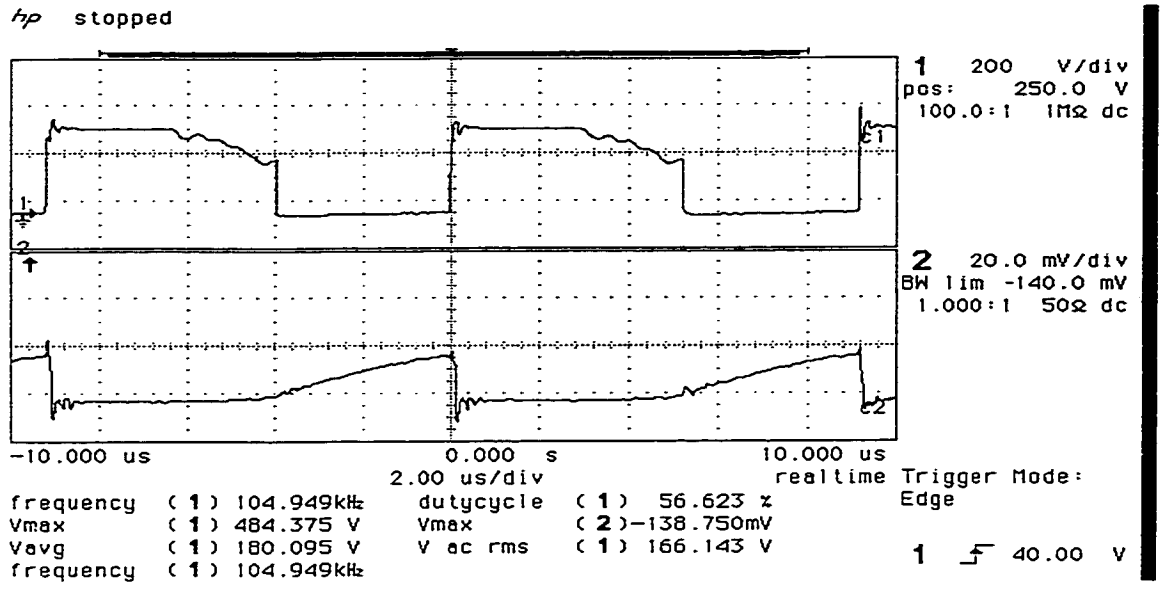
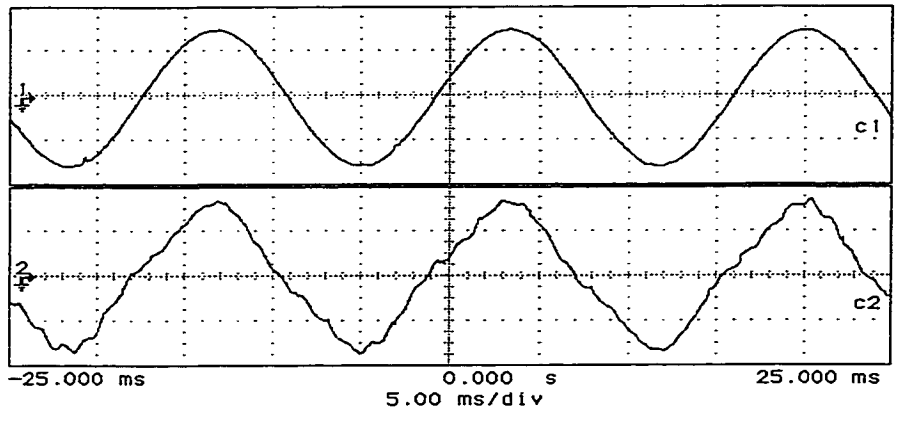


Fig. 3-31 Experimental testbed prototype.



(a)



(b)

Fig. 3-32. Experimental waveforms of the proposed converter: (a) voltage (upper) and current (lower) on the switch, and (b) line voltage and filtered input current of the converter.

Power factor is measured with hp6841A harmonic/flicker test system. Measured power factor under universal input is shown in Fig. 3-33. It can be seen that the proposed converter can maintain above 93% power factor under universal input. Figure 3-34 shows experimental efficiency comparison with different boost inductor under n=0.16 and full

load 160W output. Note all losses have been included while calculating the efficiency. It can be seen that higher inductor L means the higher duty cycle D1, and a higher efficiency can be achieved. However, excessive L will kill the line regulation capability, for instance, using 100 uH boost inductor at n=0.15, it will result in under-voltage output about only 23V. Figure 3-35 shows experimental dc bus voltage comparison with different turns ratio n at L=60uH and full load. It is manifest that higher the turns ratio n, the higher the dc bus voltage produced. The above results agree well with theoretical analysis shown in Figs. 3-17 and 3-18, which verify that optimization methodology proposed for S^2 converters. Figure 3-36 shows experimental efficiency comparison at half load and at full load. The efficiency at full load is 3% lower than that at half load. Therefore, it implies that the proposed converter is good only for low power applications (under 100W). This is because a lower than 75% efficiency at nominal conditions could not be accepted in practical applications compared to counterpart converters using two-stage topology, with which a above 80% efficiency should be got at nominal.

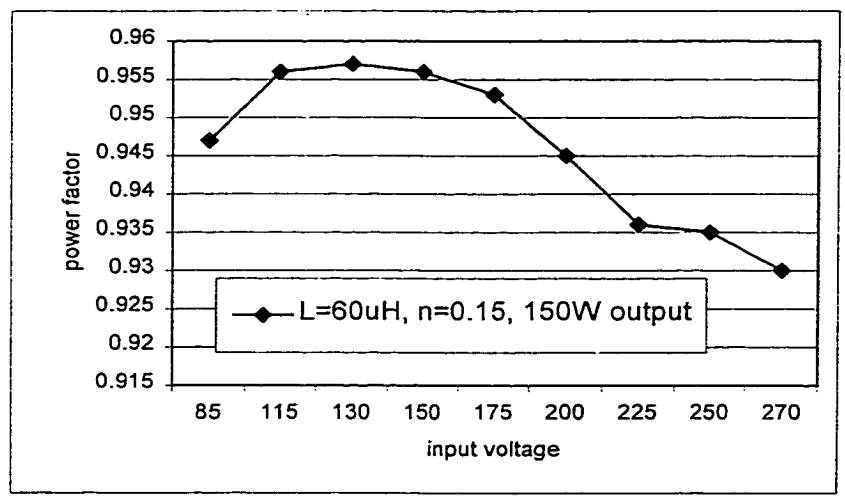


Fig. 3-33. Experimental input power factor.

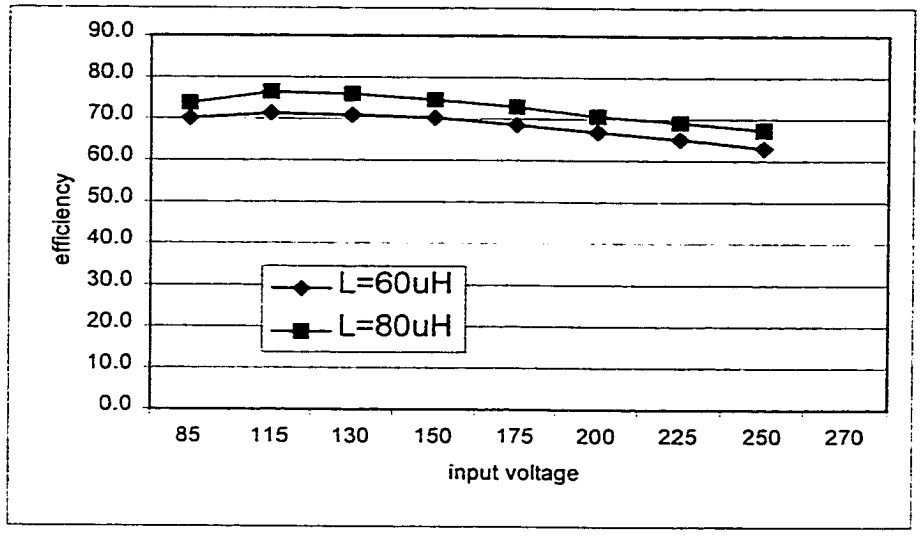


Fig 3-34. Experimental efficiency comparison under different boost inductors at n=0.16 and full load 160W output.

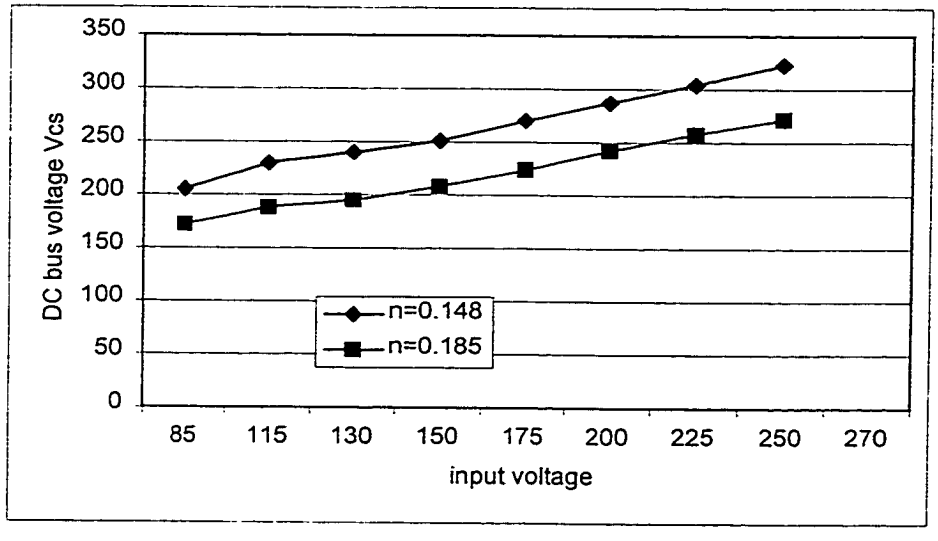


Fig. 3-35. Experimental dc bus voltage comparison under different turns ratio *n* at L=60uH and full load.

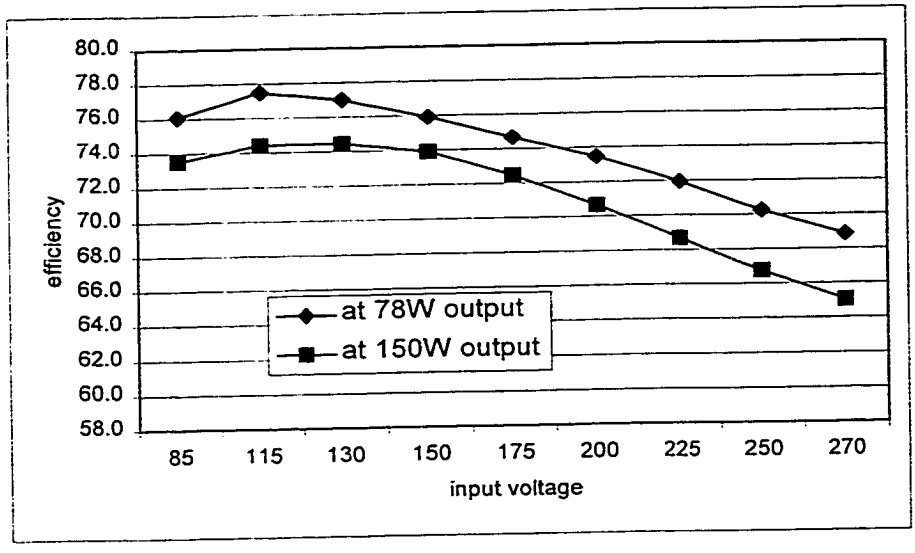


Fig. 3-36. Experimental efficiency comparison under half load and full load.

3.4 Summary

In this chapter, key issues for S^2 converters are addressed and possible solutions are explored. The high bus capacitor voltage-stress normally exists for most of S^2 PFC converters, which makes most of existing S^2 converters be impractical for universal input applications. Four general approaches, to lower dc bus voltage, are proposed and simplified theoretical analysis and simulation are completed to identify the methods, which show that both the series-charging, parallel-discharging capacitors and the bus-voltage-feedback schemes are deemed to be more viable than the other two methods.

Another challenge issue is wide dc bus voltage (bulk capacitor's voltage) range, which make designing a high efficiency converter be very difficult, particularly for universal input applications. Therefore, how to optimize design of S^2 converters is a tough challenge for design engineers. An optimization methodology, which is applicable to most of S^2 converters, has been presented in this Chapter. A popular mathematical tool "MathCAD" is employed to conduct optimization process. Simulation and

experiments are carried out to verify theoretical analysis. From the above analysis and experimental results, we can conclude that

1) Based on the proposed S^2 converter, a high power factor over 0.93, at universal input (85V~265V) and full load, can be achieved.

2) Crossover frequency of the controller can be designed far higher than that of conventional boost front-end converters employing averaging current control. With reasonable crossover frequency design about (1/10~1/6) switching frequency, a desired transient response lower than 0.5V overshoot and 2 ms settling time could be achieved.

3) Optimization procedure for a specific S^2 converter results in the conclusion that higher turns ratio, lower dc bus voltage, wider bus voltage range, larger boost inductor and duty cycle will result in higher efficiency at same operation mode. This optimization methodology is applicable to other S^2 converters if only similar circuit equations and math model could be obtained.

4) Due to operation mechanism of discontinued current mode (DCM), the proposed converter is good only for low power applications, say under 100W. The efficiency of 80% is just comparable at low power applications compared to two-stage converter counterparts.

This work was supported by the grant from NASA.

4 A FAMILY OF S^2 ISOLATED FRONT-END CONVERTERS

4.1 Introduction

The remarkable advantages achieved by the converter topology proposed in Section 3.3 are its relatively simple circuit configuration, high input power factor and low storage capacitor voltage. Particularly, it has some benefits for low power applications, as shown in [21], an above 80% efficiency can be obtained from the same topology while operating at low power (50W output). However, when considered as a front-end converter, the following drawbacks still exist:

1) Due to the DCM operation mechanism, the proposed converter is suited for only low power applications. Higher power operation will significantly reduce the efficiency due to high I^2R loss, distributed loss and switching loss in the circuitry. However, future computers and electronics equipment will consume more power. It seems that a 200W power rating might be the minimum requirement for a single front-end converter used in the DPS structure.

2) Although a trial optimization design methodology is developed in Chapter 3, its efficiency improvement seems to be very limited due to inherent characteristics: the wide dc bus voltage range, the influence of wide input voltage range on power factor, and the strong dependence of efficiency on load power and input voltage.

3) Peak currents on the switch and diode strongly depend on transformer leakage inductance due to lack of secondary filtering inductor. The higher peak current will cause larger component stresses on the switch and diodes, which will also cause increased cost

due to larger power rating components. In fact, it is not easy to control transformer leakage inductance in the practical manufacturing process.

4) As stated in Section 3.2, CCM+CCM operation is desired for S^2 converters to obtain the highest efficiency for the same topology. From circuitry design consideration and operation mechanism analysis, it is very difficult to push the proposed converter to double CCM operation. Like other S^2 converters introduced in [56, 61, 62], it is also very critical to meet the stringent harmonic standard IEC-1000-3-2, even if S^2 converters can be forced to run in double CCM with a complicated control scheme.

In this chapter, a new concept to improve converter efficiency, entitled "direct-power-transfer" (DPT), is established. Further, a new PFC cell called "*flyboost*" is presented for the first time, and also a new family of S^2 converters with improved efficiency is proposed, which are intended for use in medium power systems such as front-end converters in most of computers and some of workstations.

4.2 Direct Power Transfer Concept for High Efficiency Converters

In recent years, many S^2 circuits have been presented and implemented. However, many issues still exist before they can be put into practical applications, as discussed in Chapter 3. In all kinds of S^2 converters, the most popular class of topologies should belong to the combination of a boost PFC cell (or called boost PFC functional block) and a member of any family of r DC/DC conversion cells, as described in [19, 23]. This popular combination can be expressed into a general functional block diagram, as shown in Fig. 4-1. The power factor of a S^2 converter is guaranteed by the boost cell (DCM in

most cases) and the tight output regulation is completed by DC/DC cell. Figure 4-2 expresses a functional block diagram for a general two-stage structure counterpart.

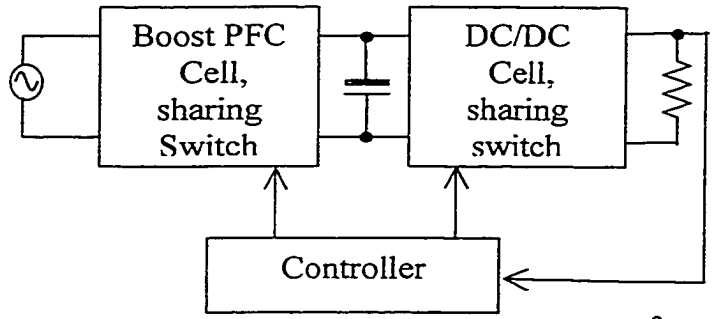


Fig. 4-1. Functional block diagram of a general S^2 PFC converter.

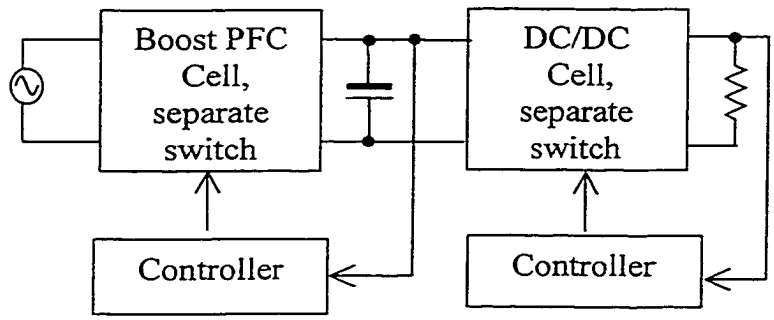


Fig. 4-2. Functional block diagram of a general two-stage PFC converter.

In order to understand the operation mechanism of S^2 converters, let us investigate power (energy) flow in a converter. From the above analysis, no matter whether it is a S^2 or a two-stage configuration front-end converter, we can see a common characteristic. AC input power is first transferred into somewhat pulsating dc power stored on intermediate bulk capacitors, this process is completed by PFC functional block, and the power stored on the capacitors will then be processed again to reach final output. This power flow process is actually more obvious in a two-stage frond-end converter. Therefore, a "*tenet*" is recognized in the front-end converters with PFC, as

stated in many references such as in [20, 56, 65], that is *input power must be processed twice to finally reach the output stage in a front-end converter*, as shown in the Fig. 4-3. Though the percentage numbers in the figure are available for S^2 converter implemented at 150W using the circuit in Fig. 3-14, the Fig. 4-3 shows a general power transfer relationship between the input and output. The percentage inside a square block shows local cell conversion efficiency, and the percentage inside an elliptical block shows power quantity ratio that reaches the power stage after passing someone cell in power flow. The research in Section 3.3 shows that the converter has near 75% efficiency at nominal input. It could be roughly estimated for a total of 150W output that PFC cell has about 90% efficiency and DC/DC cell has near 85% efficiency when both cells operate in DCM. So the circle representing power in the figure will become smaller and smaller.

From the above analysis, we can see that the double power processing means low conversion efficiency since it is the product of the efficiency of each power conversion. So far, there has been little effort reported on improving the efficiency by changing the power stage configuration or topology. Therefore, the most likely approach to achieve high efficiency is to innovate our thinking and explore a new power processing (energy-transfer) roadmap.

A new concept is to allow major input power to be processed only once, let minor input power to be processed twice, while still achieving both high power factor and tight output regulation. This concept provides a new approach to achieve more efficient and higher power rating S^2 converters than conventional approaches. For this kind of power-transfer-approach, with which power is processed only once, it is referred to as *direct power transfer (DPT)* in this dissertation. A generalized DPT concept of power

processing with improved efficiency is expressed in Fig. 4-4. Compared to the existing converter shown in Fig. 3-14 [21], obviously, converters with DPT would attain higher efficiency. Although both DPT and DC/DC cells simultaneously transfer power from high voltage side to low voltage side (28V) while operating in DCM, it may be a reasonable to assume that the DC/DC conversion cell should has relatively high efficiency because it transfers minor power and the DPT cell should hold relatively low efficiency because it is supposed to transfer major power. In Fig. 4-4 (a), the percentage numbers are only estimated values for a DCM operation S^2 converter, with which we can get a direct numerical comparison with that of Fig. 4-3. Supposing that the DPT cell has the same efficiency as the DC/DC cell, Fig. 4-14 (b) gives a generalized conceptual comparison, which clarifies why the converter with DPT generally has higher efficiency than its counterpart, simply because the converter with DPT concept follows an inequality $k\eta_1\eta_2+(1-k)\,\eta_2>\eta_1\eta_2$.

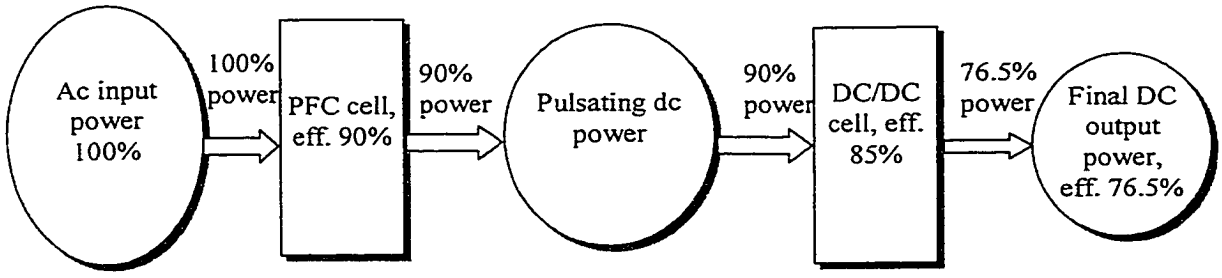


Fig. 4-3. An example of power flow implemented at 150 W in Fig. 3-14.

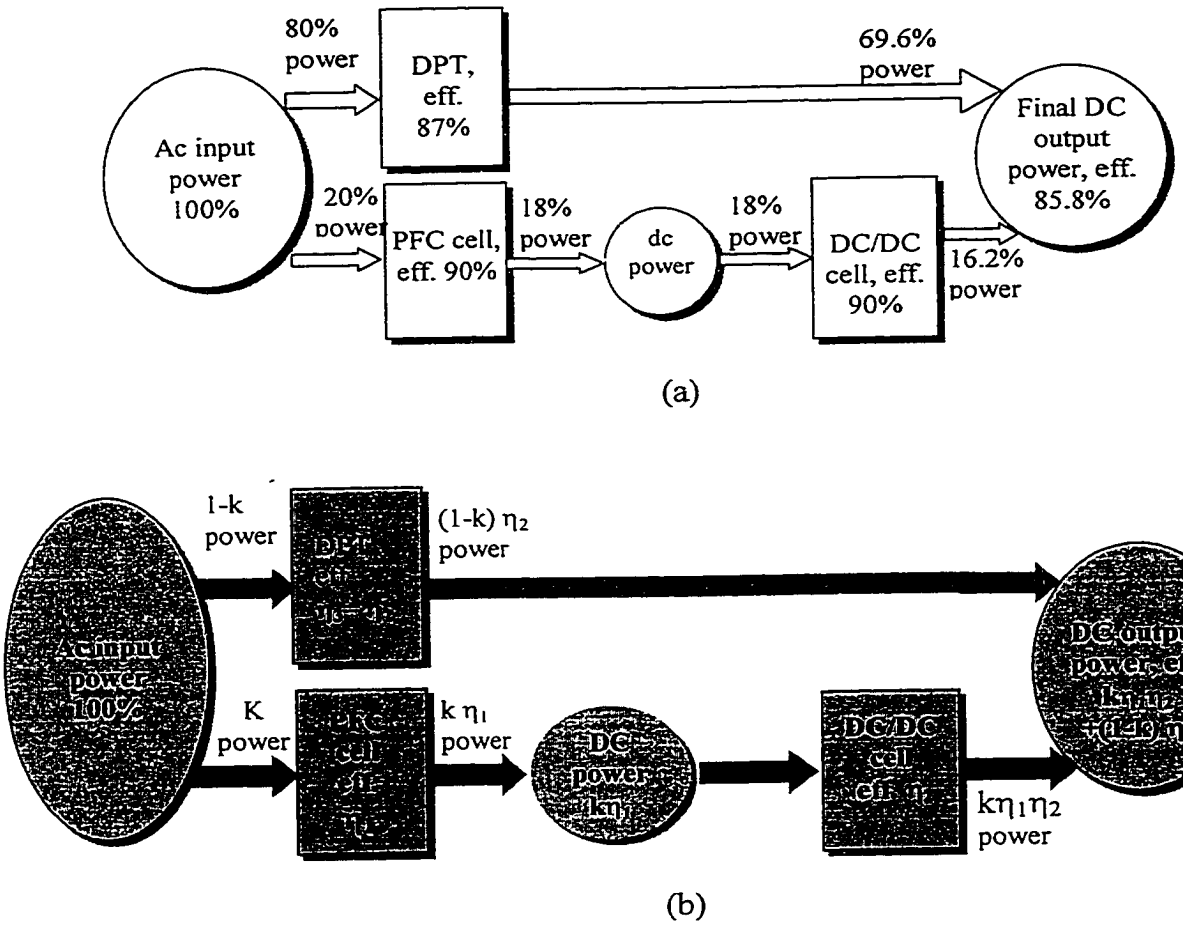


Fig. 4-4. A new roadmap of power process: (a) predicted efficiency with DPT concept based on the Fig.3-14, and (b) generalized conceptual comparison.

Naturally, we would think that a simple flyback converter could realize the above idea. It is true and reported that a above 85% efficiency can be obtained through using simple flyback converter as font-end PFC converter [64]. However, the following arguments exist:

1) Large low-frequency ripple at the output, particularly for the ripple with double utility line frequency, a very large size output filter is needed, in which the capacitor could be actually understood as an equivalent part of bulk storage capacitor in

other S^2 converters. Usually, a bulk capacitor is necessary to handle low-frequency power unbalance between input power and output power within a half-line cycle;

2) Low utilization of the power transformer due to the transition of pulsating power and large energy stored in the leakage inductance;

3) Slow regulation of the output voltage due to the big output filter and the low loop crossover frequency;

4) Hold-up time could not be guaranteed due to lack of bulk storage capacitor in the high voltage primary side. A complicated circuit for hold-up time has been designed to solve this issue [64], however, it is not a cost-effective solution.

4.3 Development of Topologies

4.3.1 "Flyboost" PFC Cell

Recall that when the topology in Fig.3-14 is applied for high power output, a large peak current will show up in the secondary side and it causes increased switch peak current. As a result, unexpected additional loss will be produced. It is necessary to replace the secondary side rectification circuit using formal dc/dc forward secondary circuit. A modified topology is shown in Fig. 4-5(a). The two primary-side leakage inductors are merged into output filtering inductor L_o, adding D3 and D4 is a practical consideration for the start-up process and light load operation. D6 is a freewheeling diode being used like in other forward converters. The fixed topology is called the Russian's circuit (topology) in [18]. The reason that the topology is introduced herein is because of

its similarity to the prototyped topology in Section 3.3. We will also compare its features with new topologies proposed in this chapter.

Now the topic is how to implement the above idea using a simple structure, a simple circuit and simple control. A parallel power factor correction (PPFC) concept has been proposed in [65, 66], which allows partial input power to be processed by the DPT approach. However, the word "parallel" inherently implies that multiple power stages must be used. In fact, as described in [65, 66], PPFC circuit implementations are very complicated, which cause practical issues such as complicated structure, sophisticated operation mechanism, complicated control, and thus difficult design and poor reliability. It is clear that applications may be limited to high power rather than medium power. On the other hand, the simple flyback PFC circuit can do DPT, but it also has its own inherent defects as argued above.

It is well known that the flyback converter can automatically produce near unity power factor with constant duty ratio under DCM operation [63, 64], as does the boost [14]. Therefore, it is desirable to still keep the input cell with flyback or/and boost features. The second desirable feature is to let the input cell implement DPT, allowing major input power to be processed once. But at the same time, we have to keep the dc/dc stage function to obtain tight output regulation. Further, in order to achieve simple control while obtaining both high power factor and tight output regulation, it is desirable to keep the input cell operating under DCM. The second DC/DC cell can operate either in DCM or in CCM depending on dc bus voltage and power level.

Based on the DPT concept, the Russian's topology depicted in Fig. 4-5 (a) can be further modified into a new topology shown in Fig. 4-5 (b), which basically consists of a

PFC cell and a series/parallel forward converter cell. Comparing with Fig. 4-5 (a), physically, the added part is only diode D_1, and then we put one more winding (a few turns) on the same core of the previous boost inductor which change the original boost inductor into a special transformer to implement partial DPT.

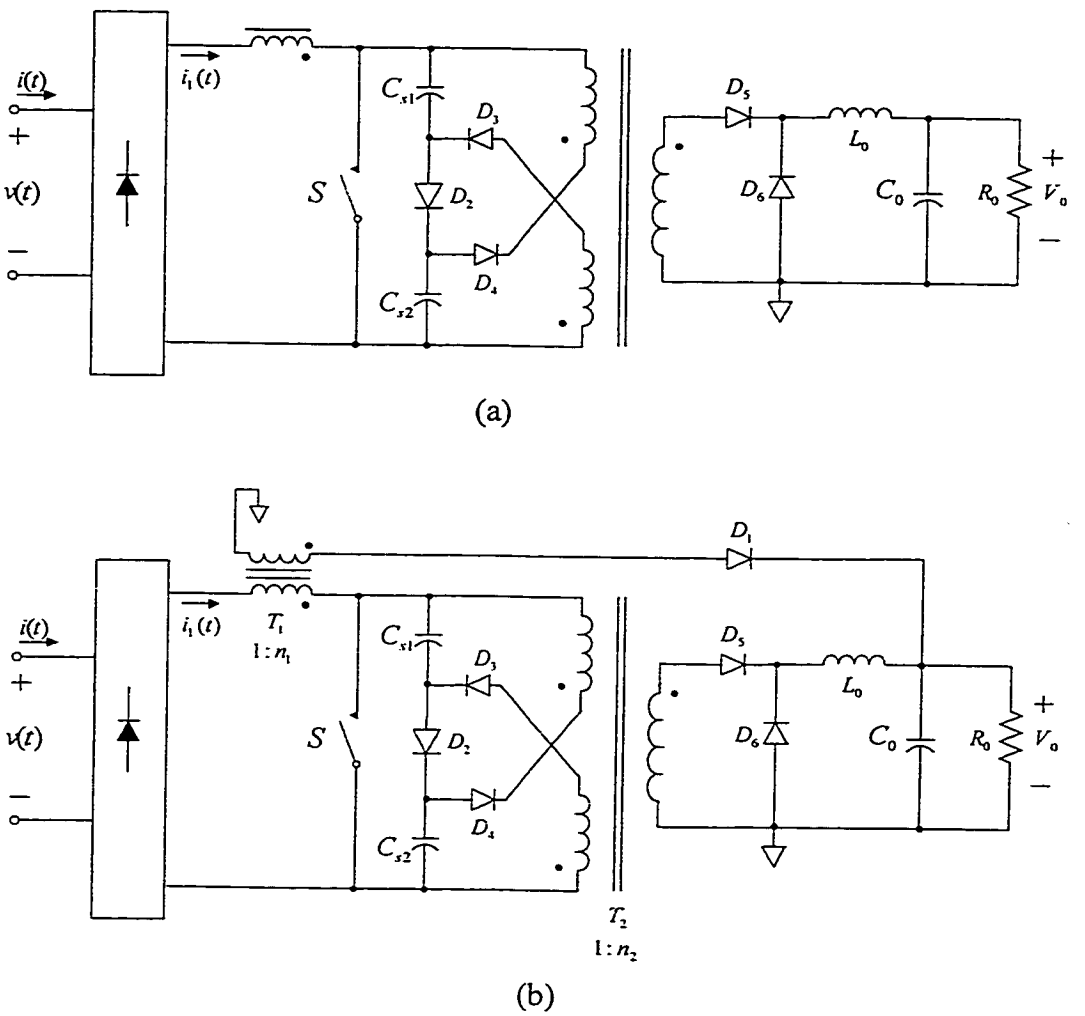


Fig. 4-5. Improved S^2 topologies: (a) Russian topology based on Fig. 3-14 topology, and (b) new topology with DPT concept based on Russian topology.

In the topology shown in Fig. 4-5(b), the conventional boost inductor has been modified, which results in a new PFC cell (or functional block). Unlike any existing

front-end converters, the modified boost inductor is not the former boost inductor, and it is not a flyback transformer either. By this modification, we simultaneously implements two types of power transfer, namely, flyback power transfer and boost power transfer. In this dissertation the modified boost inductor is named the *flyboost* transformer because the combined word *flyback-boost* exactly expresses its new functionality. Therefore, the corresponding PFC cell consisting of a switch, a capacitor and a flyboost secondary diode, is referred to as *flyboost PFC cell*, which could be expressed as a general structure shown in Fig. 4-6. Compared to currently known PFC cells such as boost, SEPIC, buck-boost, Cuk and buck, etc, although only small differences physically, its operation mechanism is very different from the following analysis.

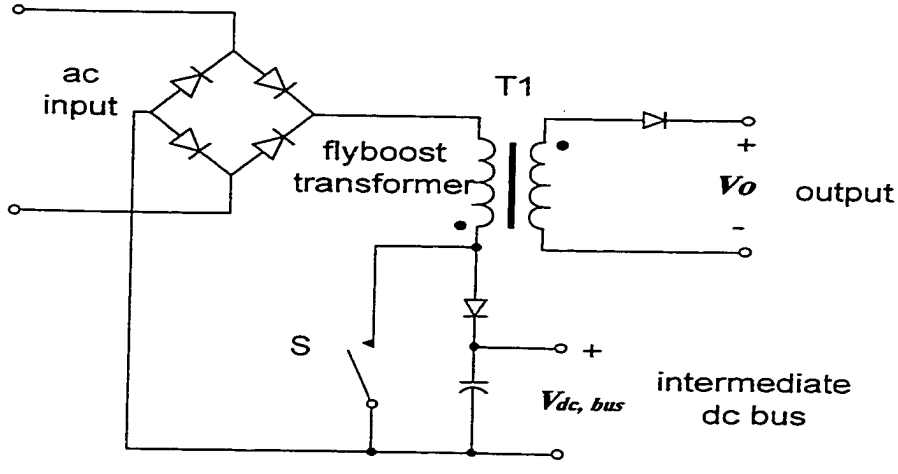


Fig. 4-6. Flyboost PFC cell as a general PFC cell.

4.3.2 A Family of S^2 Topologies Based on the Flyboost PFC Cell

Compared to the other known S^2 converters, the proposed converter in Fig.4-5(b) has the following potential merits:

1) High power factor due to inherent characteristics resulting from both the flyback and boost converters;

2) High efficiency due to the major input power to be processed only once;

3) Intermediate DC bus voltages on capacitors C_1 and C_2 could be kept within a desirable range by properly designing the turns ratio of the transformer T_1;

4) Relatively low voltage stress power MOSFETs and bulk capacitors can be used in the converters because of controllable DC bus voltage;

5) Input inrush and surge current protection because of heritage for characteristics of flyback and boost converters;

6) Still simplified circuit structure due to the use of only one power switch and one controller and keeping the same number of magnetic components;

7) Higher power processing capability due to two modes of power-transfer, the flyback and forward in the converter;

8) Decreased output current ripple due to interleaving of currents i_1 and i_2 out of phase;

9) Unlike other S^2 converters using the flyback circuit structure, hold-up time in the proposed converter can be guaranteed by stored energy on the bulk capacitors C_1 and C_2;

10) Better magnetic utilization due to multiple channel power transfer modes; and

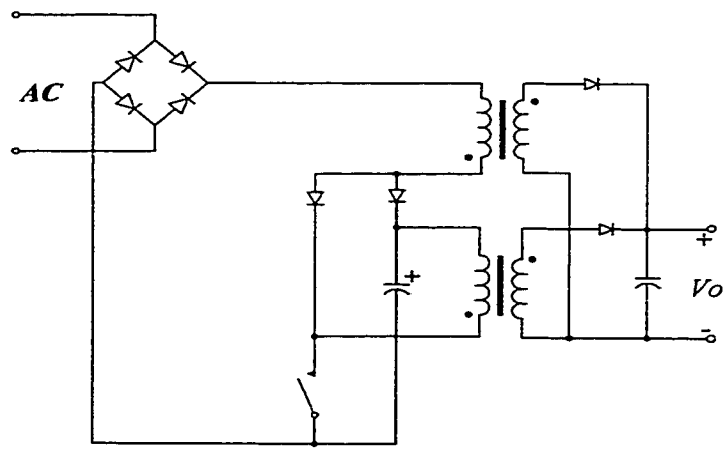
11) More flexibility for power supply design engineers, depending on your care for efficiency, DC bus voltage and ripple.

Like other PFC cells such as boost, SEPIC, buck-boost and Cuk [19], the flyboost cell in Fig. 4-6 can be used to replace any PFC cell in existing S^2 topologies and thus a

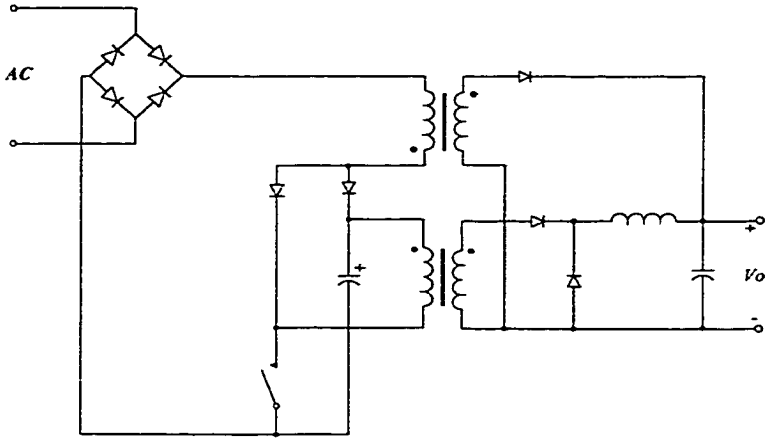
new family of topology can be derived from the general functional structure shown in Fig. 4-1. Note that in most of S^2 converters, active switch is shared after both PFC cell and dc/dc cell are combined. If both cells operate in DCM, a simple control circuitry can be employed.

Figure 4-7 gives several sample topologies obtained through modifying existing S^2 topologies; some of them are patented circuits in the past. In all figures, for clarity and simplicity, we do not depict the input EMI filter, the reset and clamp circuits of the single-switch flyback and forward converter cells.

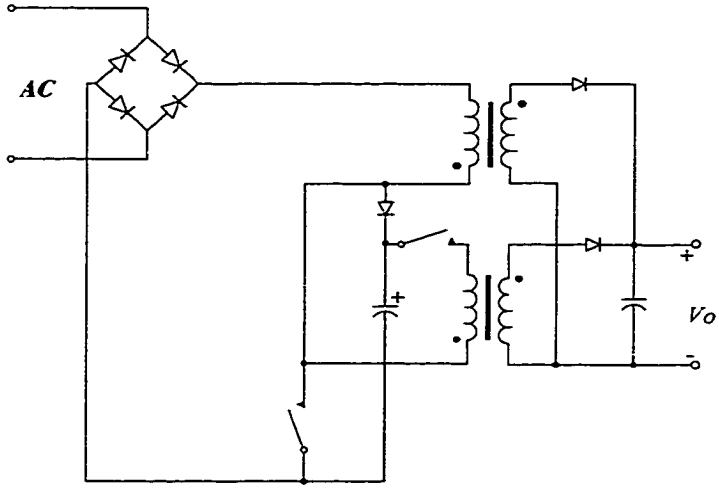
It is obvious that a similar derivation using the flyboost cell can be applied into any existing two-stage topologies, and new family of two-stage topologies can also be achieved through a general structure diagram shown in Fig. 4-2. The research here is concentrated on only S^2 converters.



(a)



(b)



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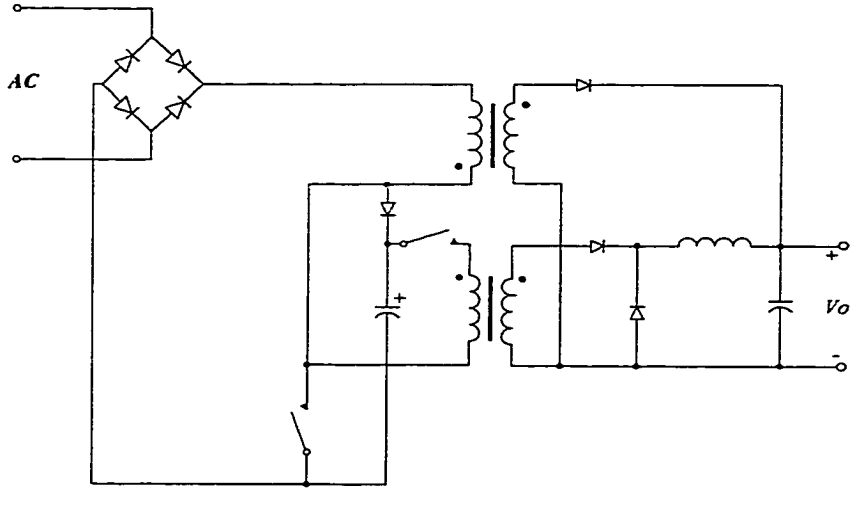

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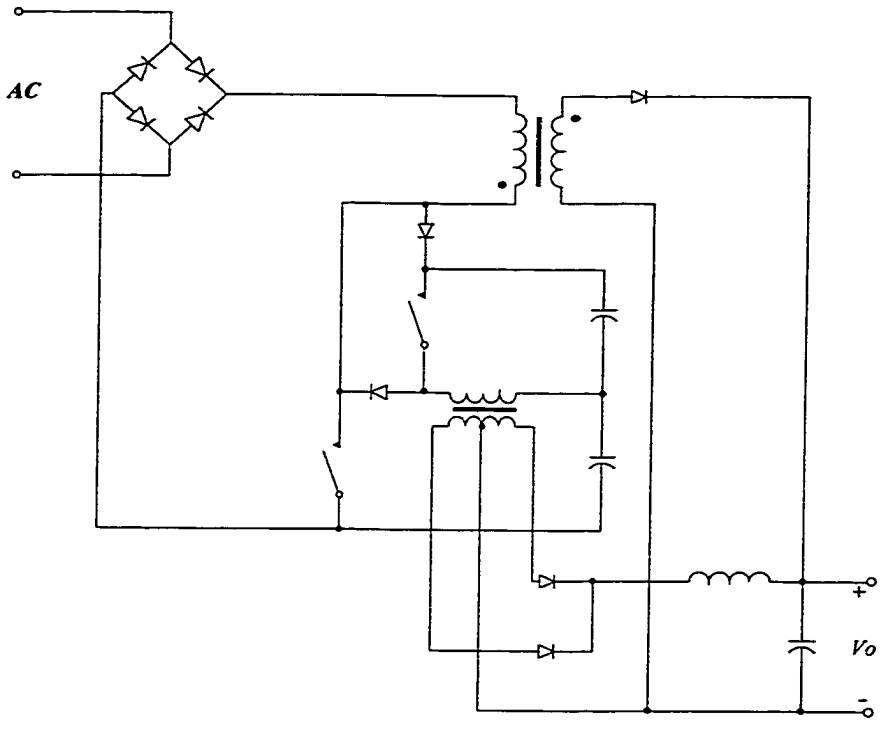

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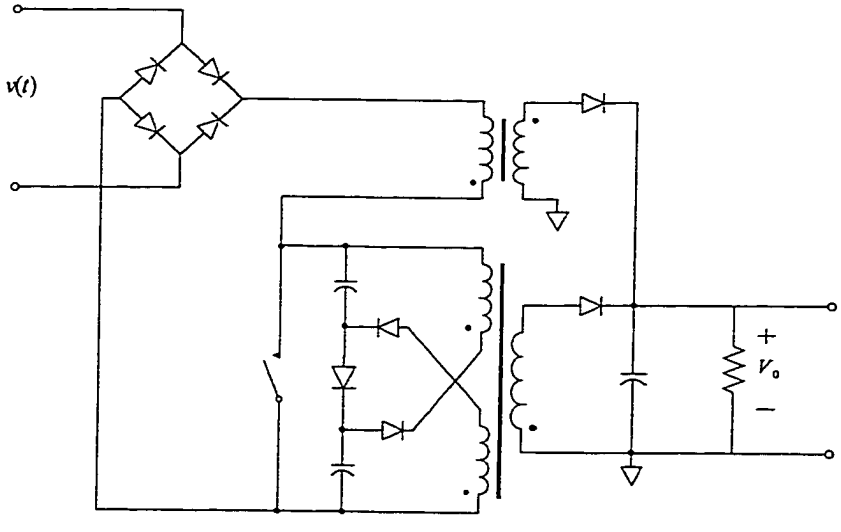

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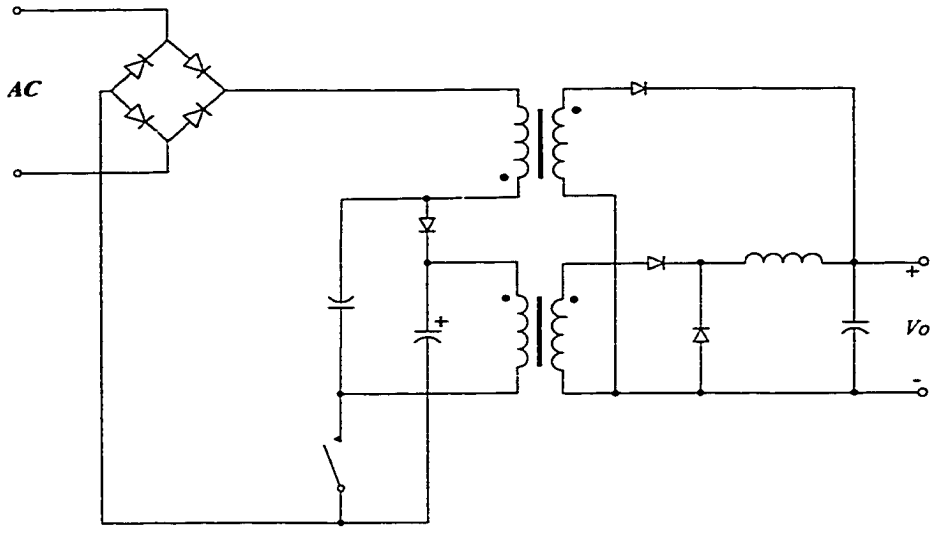


(g)

Fig. 4-7. Derived new family of topologies based on the flyboost PFC cell and typical dc/dc cells: (a) flyboost PFC + flyback dc/dc (b) flyboost PFC + forward dc/dc, (c) flyboost PFC + two switch flyback DC/DC, (d) flyboost PFC + two switch forward dc/dc, (e) flyboost PFC + half-bridge DC/DC, (f) flyboost PFC + series/parallel flyback, and (g) flyboost PFC + forward DC/DC, but both cells operating in CCM.

4.3.3 Extended Topologies

Except DPT approach, the following considerations are also beneficial to push power and efficiency higher:

1) For the same topology, higher duty cycle design, especially larger than 0.5, do help lower rms and peak currents and thus reduce conduction loss;
2) CCM operation in order to reduce peak current and rms current on the components. In order to achieve good power factor while using CCM operation, charge control (one-cycle) with double loops might be a candidate option;
3) Multiple channel power transfer also help decrease peak and rms currents.

Based on the above considerations, a new class of topologies might be constructed. Figure 4-8 gives a combined example. The topology consists of flyboost PFC cell and series/parallel forward DC/DC with center-tapped secondary-side configuration. From his topology, we may get bi-directional power transfer by the center-tapped and a specially designed transformer in the forward cell. It seems to be the only way that we can obtain bi-directional power transfer in the single-ended converter is to change our design idea. It is well known that there are two basic power transfer transformers in the single-ended isolated converters, namely, the forward and the flyback transformers. Now the question why not design a mixed functional transformer is coming? We hope that the mixed transformer behaves with half to half forward and flyback characteristics. As a result, a bi-directional power transfer could be obtained. Expected benefits are 1) increased magnetic utilization; 2) double frequency output ripple; 3) higher efficiency due to smaller peak current on the components; 4) smaller size output filters; 5) possibly easier for CCM operation.

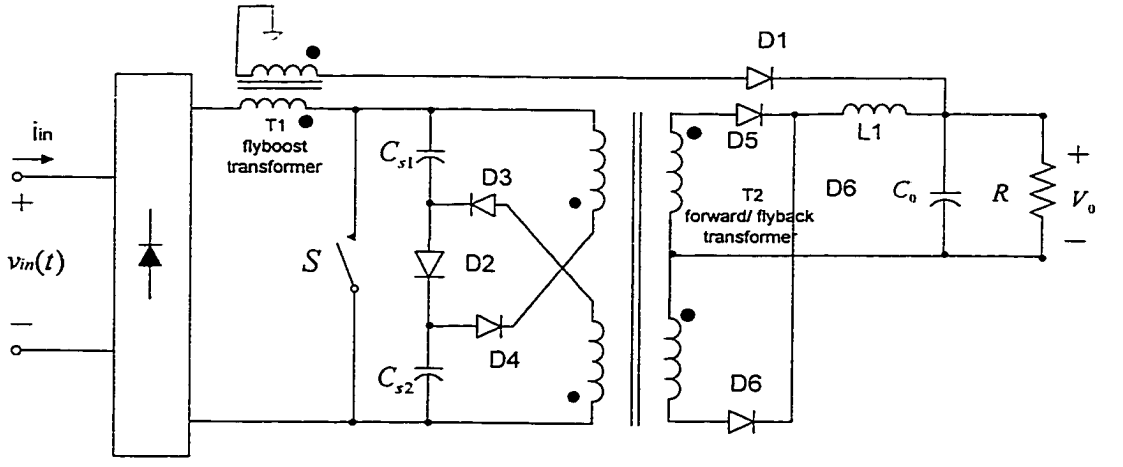


Fig. 4-8. Topology with flyboost PFC cell and series/parallel forward cell with center-tapped secondary side rectification.

In the converters using flyboost PFC cell, a relatively larger low frequency ripple may be introduced to the output due to DPT through using the flyboost cell. A possible approach to reduce low-frequency ripple at the output side is to introduce a voltage feedback into the secondary flyback branch through an additional winding on transformer 2, as shown in Fig. 4-9. The ripple cancellation mechanism is to utilize a feature that in a half-line cycle, the feedback voltage is proportional to Vcs. Therefore, during low input voltage in half-cycle we can allow more current (power) to reach the output; during high input voltage a larger feedback voltage will tend to block current to the output through flyboost secondary-side.

The ideas to improve topologies shown in Figs. 4-9 can be employed to improve other topologies of the new family in Fig. 4-7 and thus other new category of topologies may be obtained.

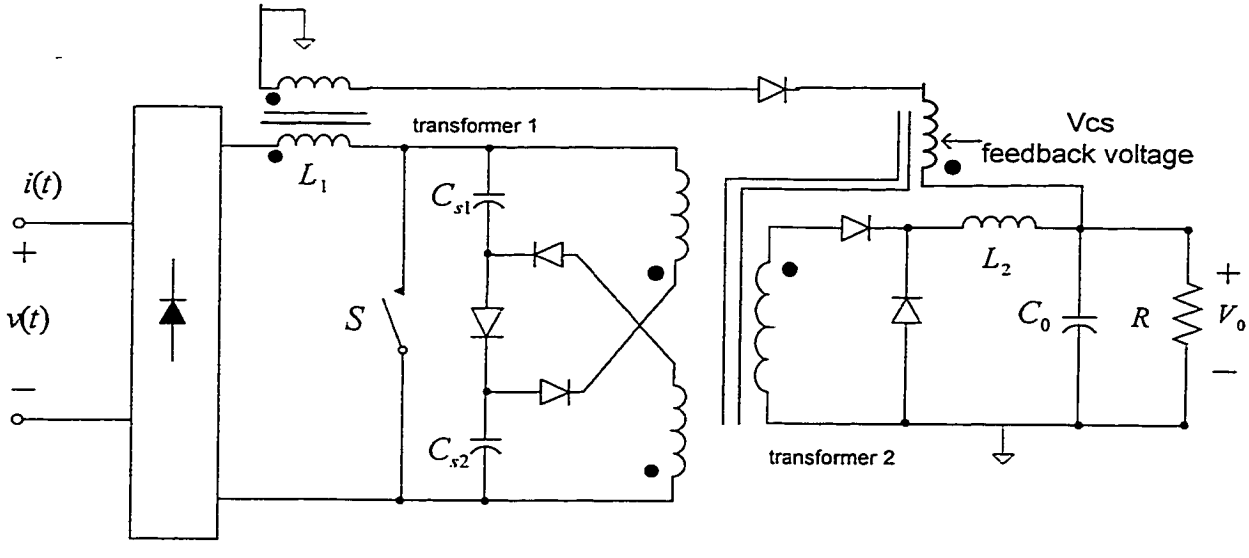


Fig. 4-9. Topology with reduced low-frequency ripple.

4.4 Example Circuit Operation and Basic Design Considerations

4.4.1 Circuit operation

For the sake of comparing topology characteristics in Figs. 3-14 and 4-5 (b), all of the following analyses and discussion are concentrated on the modified topology that is redrawn in Fig. 4-10. From the general concept introduced above, the topology is actually comprised of a flyboost PFC cell and a series/parallel forward cell. From a practical standpoint, it might be necessary to place a high-frequency diode, D_{boost}, in series with flyboost primary side, because the rectifier diodes in the bridge rectifier are turned off with the rather high di/dt.

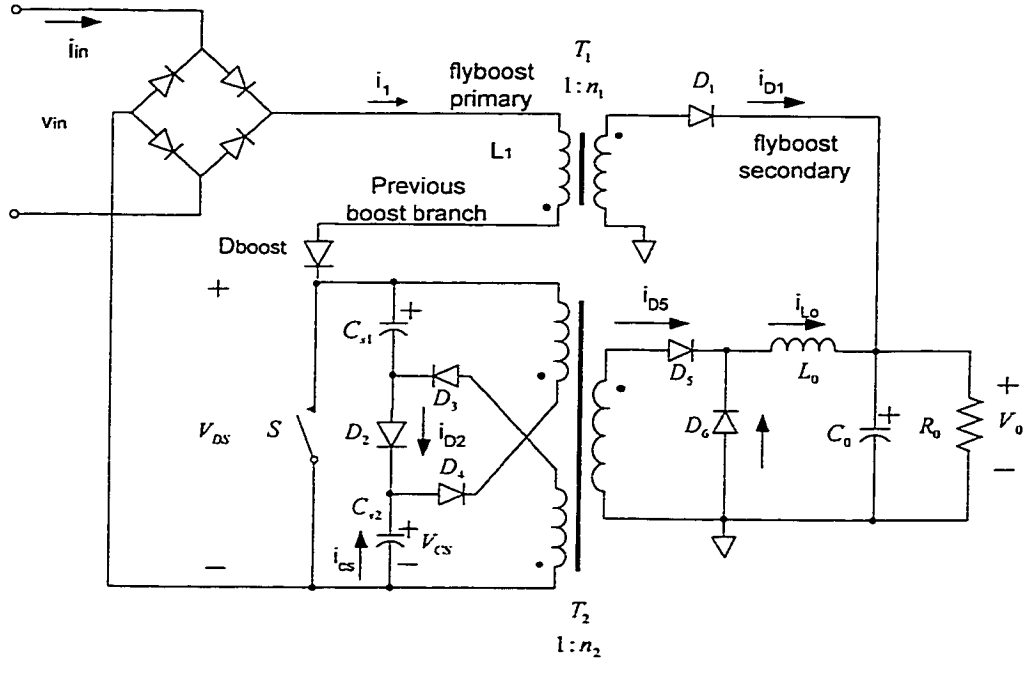


Fig. 4-10. Combined topology with flyboost PFC cell and series/parallel forward cell.

For most of the existing S^2 topologies, optimally, both the PFC section and the DC/DC converter section operate in DCM, otherwise, it is almost impossible satisfy

trade-offs of design. This is because the intermediate DC bus voltage variation range is load-dependent and unacceptable if DCM+CCM operation is employed, and also low power factor with complicated control is inevitably encountered if CCM+CCM operation is used. However, in the topology shown in Fig. 4-10, an important trait is that the intermediate DC bus voltage is controllable if only magnetic components for both flyboost PFC and forward DC/DC cells are properly designed. DC bus voltage can be clamped to a desired range. This means that the proposed topology can operate either DCM+DCM or DCM+CCM while still keeping simple controller. The first DCM means that by the end of the switching cycle the flyboost delivers all of its stored energy to either the next stage or the output. The second DCM means that output-filtering inductor current for the DC/DC forward cell is discontinuous on a cycle by cycle basis. However, CCM+CCM operation is not yet favorable to the overall performance because of relatively low power factor and a slow regulation with low crossover frequency. In addition, it is difficult to meet power factor and harmonics requirements while the PFC cell is operating in CCM. In fact, the penalty to pay for the first DCM operation is only a slight increase in the conduction losses. However, the switching losses associated with hard turn-off of the rectifier diodes are eliminated.

Though there is only one active switch and one controller in target converter presented in Fig. 4-10, like other S^2 converter, the proposed topology has only one inductive energy-storage component for each conversion cell. However, its operation mechanism is very different due to the traits of the flyboost PFC cell. In fact, there are three power transfer modes simultaneously existing in the converter, i.e., flyback, boost and forward modes. Therefore, analysis for circuit operation can be carried out by

considering the circuit as three sections with the connection shown in Fig. 11(a). For circuit operation modes of other S^2 converters, the two sections are essentially decoupled by the large energy-storage-capacitor, as shown in Fig. 11(b). So the circuit operation is combination of two relatively independent sections. However, for circuit operation modes of the proposed converter, mutual interactions among three circuit sections are obvious. The main reason is that flyboost PFC cell has more than one operation modes.

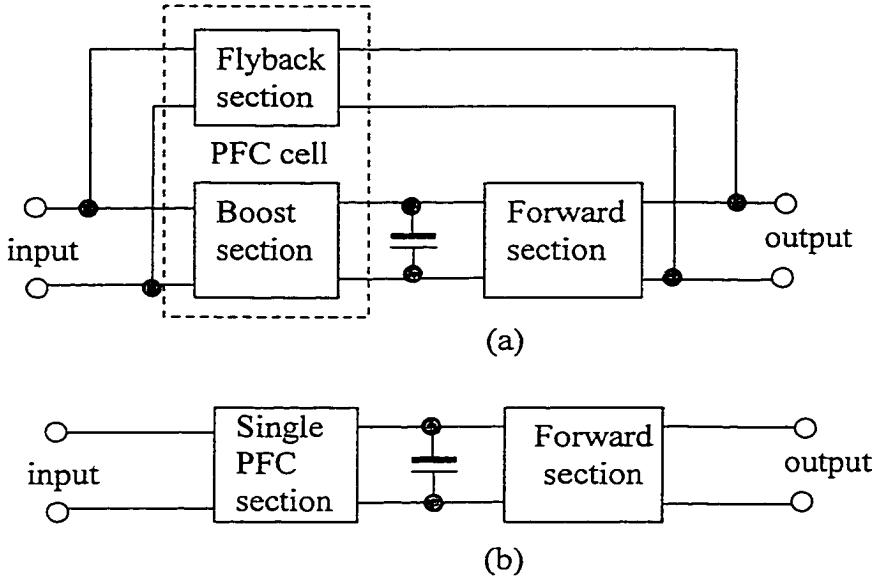


Fig. 4-11. Sections of circuit operation: (a) proposed S^2 converters, and (b) other S^2 converter.

In this dissertation, a quasi-decoupling method has been used to simplify the analysis of circuit operation modes. As for PFC cell, there are three possible operation modes, namely, pure flyback mode, pure boost mode and mixed mode (combination of former two modes). For forward cell, we need to consider that the circuit is operating in the DCM or CCM.

Ideally, assuming that the capacitance of intermediate bulk capacitor is infinitely large such that it could be regarded as an ideal voltage source, as most papers assumed in the past. There are only two operation modes for flyboost cell, as shown in Fig. 4-12. When $|V_{in}(t)| < (2V_{cs} - V_o/n_1)$ for $t<t_x$, flyboost works like a flyback circuit and all input power is directly transferred to the load. Assume for instant t_x to $(T/2 - t_x)$, the instantaneous line voltage is higher than $(2V_{cs}-V_o/n_1)$, and flyboost transformer works in a boost fashion and all input power is stored in storage capacitors C_{s1} and C_{s2}. The forward section continues to transfer power from intermediate dc bus to output, regardless of which circuit operation way the flyboost cell takes. Meanwhile, it should be pointed out that circuit operation way is still sensitive to all magnetics component design even if C_{s1} and C_{s2} are selected as several times large than those of the regular design.

In practical applications, however, infinitely large capacitance is impractical. Consequently, mixed mode dominates circuit operation. Table 4-1 gives conduction status of power components under DCM+CCM), corresponding to typical four periods of circuit operation in one switching cycle in Fig.4-10. Figure 4-13 shows key waveforms corresponding to Table 4-1.

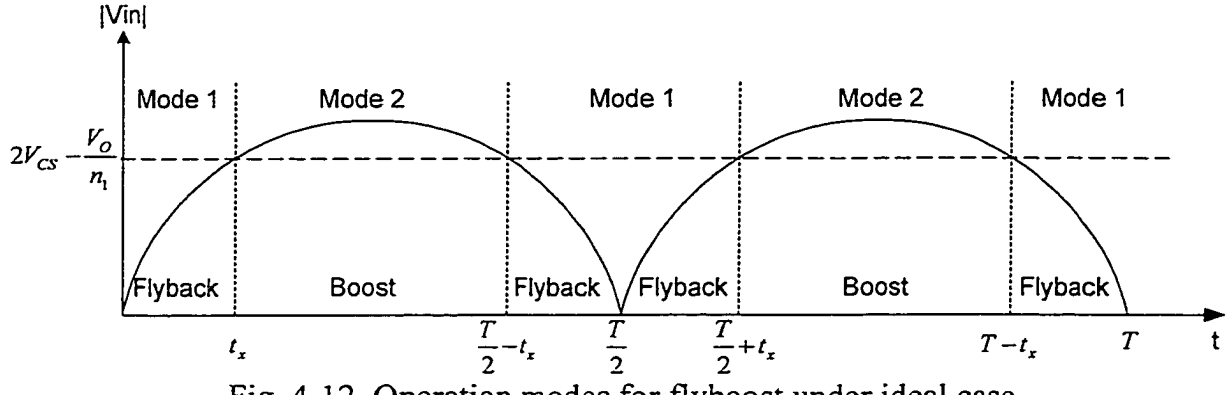


Fig. 4-12. Operation modes for flyboost under ideal case.

Table 4-1 Conduction statuses of power components

Device	Period			
	P_1	P_2	P_3	P_4
S	X			
D_{boost}	X	X		
D_1		X	X	
D_2		X		
D_3/D_4	X	x*		
D_5	X			
D_6		X	X	X

*Components switch off if magnetizing inductance of T_2 is relaxed

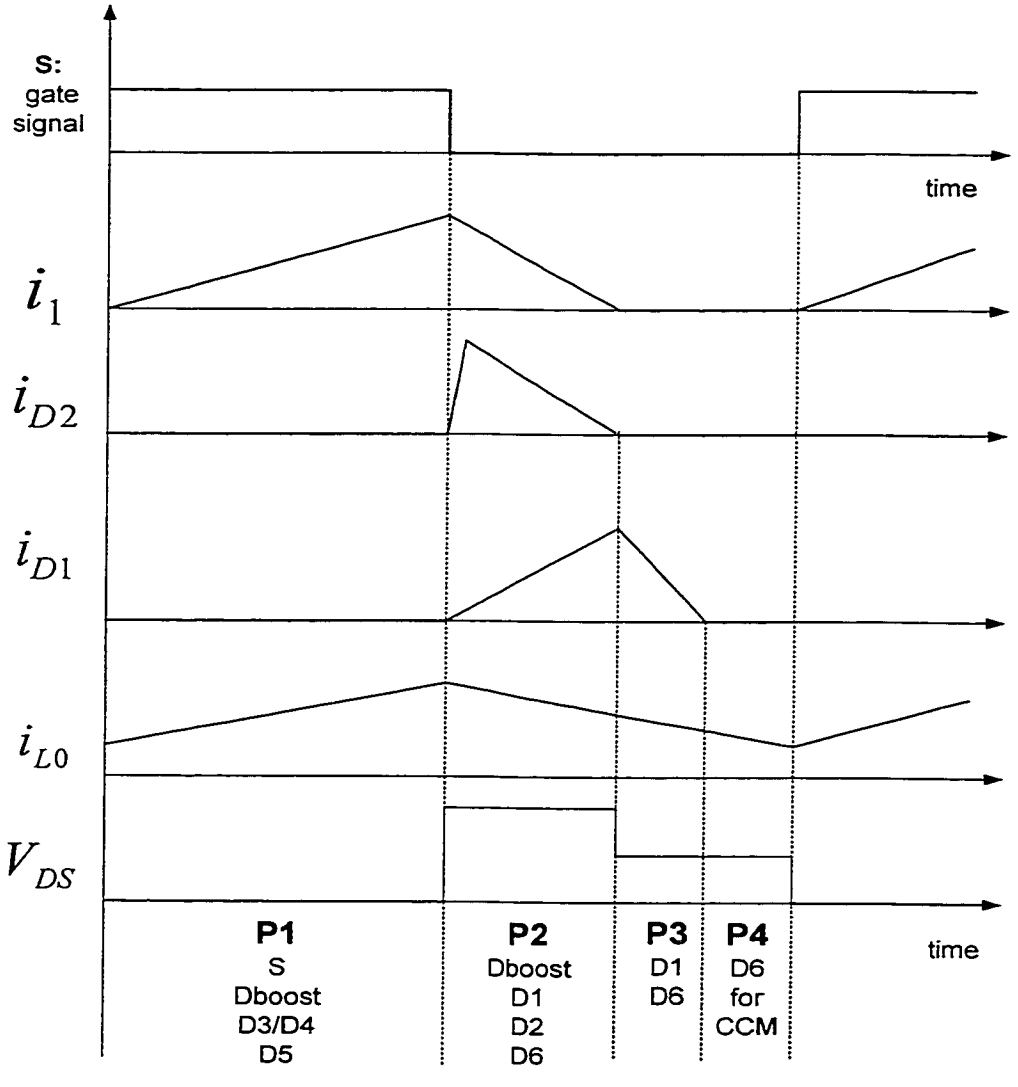


Fig. 4-13. Key waveforms corresponding to Table 4-1.

4.4.2 Basic Design Considerations

In designed prototype, a simple voltage mode control strategy is used for DCM+DCM operation. According to the characteristics of the proposed topology, the related design considerations are discussed below:

1) Control

Like other regular DC/DC converter, a single fast voltage control loop can be employed, which keeps the output voltage constant by monitoring output voltage and correcting it as needed. Of course, current-mode controls (either constant-frequency or variable-frequency) are also applicable. But this family of topologies complicates the control strategy of current mode, because the inner current-controlling loop must be based on the current flowing in the DC/DC cell and current-flowing in secondary of flyboost cell. In fact, both currents are substantially contributing to the load. It could not be acceptable to sense only the current of the switch that carries the currents not directly related to output. Due to pulsating flyboost secondary current, average switch current-mode (ASCM) control might fit this applications [59, 67]. It is intuitive that the benefits of the current mode control are decreased low-frequency ripple at the output and increased dynamic response.

2) Component Stresses

Since maximum intermediate dc bus voltage is clamped at $(V_{in,max}(\omega t)+V_o/n_1)$, component voltage stress in primary side might be considered with certain safety coefficient (say 1.2 ~1.5) based on this maximum dc bus voltage $V_{cs,max}$. This feature is very important for cost-effective and high efficiency design, because low component stress means low cost and low switching as well as conducting losses.

3) Simplified Magnetic Design for Forward Cell

Demagnetizing voltage for DC/DC forward transformer is clamped at V_{cs}, it means that magnetic constraints requires that maximum duty cycle must be lower than 0.5.

Other design considerations should follow regular forward transformer design procedure. We must be aware that the load that will be taken into design account is not the whole load that the converter is powering, it is only part of output load, herein called as forward load and referred to as $R_{forward}$. The remaining load, which is powered by flyboost cell through DPT way, may be called as flyback load and referred to as $R_{flyback}$. The sum of both loads $R_{forward}$ and $R_{flyback}$ is whole load, R. The quantities for $R_{forward}$ and $R_{flyback}$ depend mainly on design trade-off that you want how much proportion load transferred through DPT and how much power is processed twice to guarantee tight regulation for the output.

Taking CCM operation mode above certain load (say half load), the following constraints should be applied. The filtering inductor and maximum duty ratio should respectively meet:

$$L > \frac{R_{forward}(1 - D_{forward})T_S}{2} \tag{4.1}$$

and,

$$D_{\max} = \frac{V_o}{n_2 V_{cs,\min}} \tag{4.2}$$

where $D_{forward}$ represents the duty ratio under certain conditions such as load $R_{forward}$, dc bus voltage V_{cs}, etc, and $V_{cs,min}$ is minimum dc bus voltage.

Turns number of transformer at primary and secondary sides can be determined by:

$$N_P = \frac{V_{cs,\min} T_s D_{\max}}{B_{\max} \times A_e} \tag{4.3}$$

and

$$N_s = \frac{V_o N_p}{V_{cs,\min} D_{\max}} \tag{4.4}$$

where B_{max} is maximum flux density designated, generally, taking $\frac{2}{3}(B_S)$, and A_e is magnetic core across-section area.

4) Simplified Magnetic Design for Flyboost Cell

In specific topology, the most challenging design is for the flyboost transformer. In fact, the transformer performs two types of power transfer, namely, flyback and boost. Ideally, major power is transferred by flyback mode with DPT. Therefore, we could consider that conventional flyback operation dominates the behavior of flyboost cell. For the sake of simplicity, we could regard that an equivalent flyback transformer is transferring all power from the input, including transferred power that boost operation mode does. The following are the simplified design procedure:

a) First, for a DCM operating flyback transformer (inductor), to protect from flux walking, magnetic reset must be taken into account, volt-second balance must be followed by:

$$\frac{V_o(1-D_{\max})}{D_{\max} \times \sqrt{2} V_{in,\min}} \le n_1 \tag{4.5}$$

where V_o represents output voltage, n_1 expresses turns ratio of the flyboost transformer, D_{max} is designed maximum duty cycle (less than 0.5), which is decided by DC/DC forward controller, corresponding to minimum ac input voltage $V_{in,min}$.

b) Considering power balance between input and output and also employing quasi-static principle that ac input voltage resource is replaced by an equivalent dc voltage resource with the same value as ac rms, peak current at primary-side of flyboost could be approximately determined by:

$$I_{pk} = \frac{2P_o}{V_{in,\min} D_{\max} \eta} \tag{4.6}$$

where η is the converter efficiency from input to output, and P_o is the average output power.

c) Equivalent inductance at primary side could be roughly determined below:

$$L_p = \frac{V_{in,\min} D_{\max} T_s}{I_{pk}} \tag{4.7}$$

5) Capacitor and Inductor

Output capacitor in primary side is determined by output ripple requirement and output inductor is determined by output ripple and also considered if it is considered operating in CCM or DCM. The two bulk capacitors are design to meet hold-up time requirement (please see Section 3.3).

6) High Efficiency Design Consideration

In order to achieve high efficiency while meeting hold-up time and tight regulation, allow more input power to reach the output through flyboost with DPT method. At the same time, duty-cycle should be designed as large as possible.

7) Operation over A Wide Line-Voltage Range

The voltage across the storage capacitor is a proportional function of the line voltage. Several simulation results show that although maximum dc bus voltage is controllable, the voltage still varies over two times when the line voltage varies between 85 and 265 V_{rms}. It is difficult to design the power supply to accommodate that variation so as to keep high efficiency in the whole input voltage range. So optimum point has to be considered at 110 V_{rms} line voltage. The simplest way to handle this issue may be by using variable inductor that is: connecting the two winding in series at 230Vrms line and in parallel at 110Vrms line. As a result, a relatively high duty-cycle operation can be kept so that high efficiency could be obtained.

4.5 Simulation and Experimental Verification

4.5.1. Simulation Verification for Circuit Operation

Figure 4-14 shows simulated schematics based on the simulation platform OrCAD–capture 9.2. Figure 4-15 shows interested simulation waveforms of proposed topology, in terms of line cycle, working in different operation modes under DCM +CCM operation for flyboost and forward cells. Main circuit parameters are: V_{in}=110 V_{rms}, L_1=60uH, L_o=90uH, n_1=0.25, n_2=0.67, f_s=100kHz, C_{s1}=C_{s2}=330uF, $L_{flyboost}$=0.5uH (leakage inductance). From Fig. 4-15(a), we can understand power flow in the proposed converter, it is seen that average i_{in} is a sinusoidal shape with high power factor and it represents input line current, and the sum of i_{D4} and $n_1 i_{Leak}$ express total current (power) transferred by flyboost cell. The total current must also be sinusoidal shape if a high power factor will be obtained and i_{D2} current transferred to bulk capacitors as boost mode and i_{D1} current directly transferred to load as flyback mode. Fig. 4-15(b) shows mixed operation mode in terms of switching cycle, and (c) flyback mode and (d) boost mode.

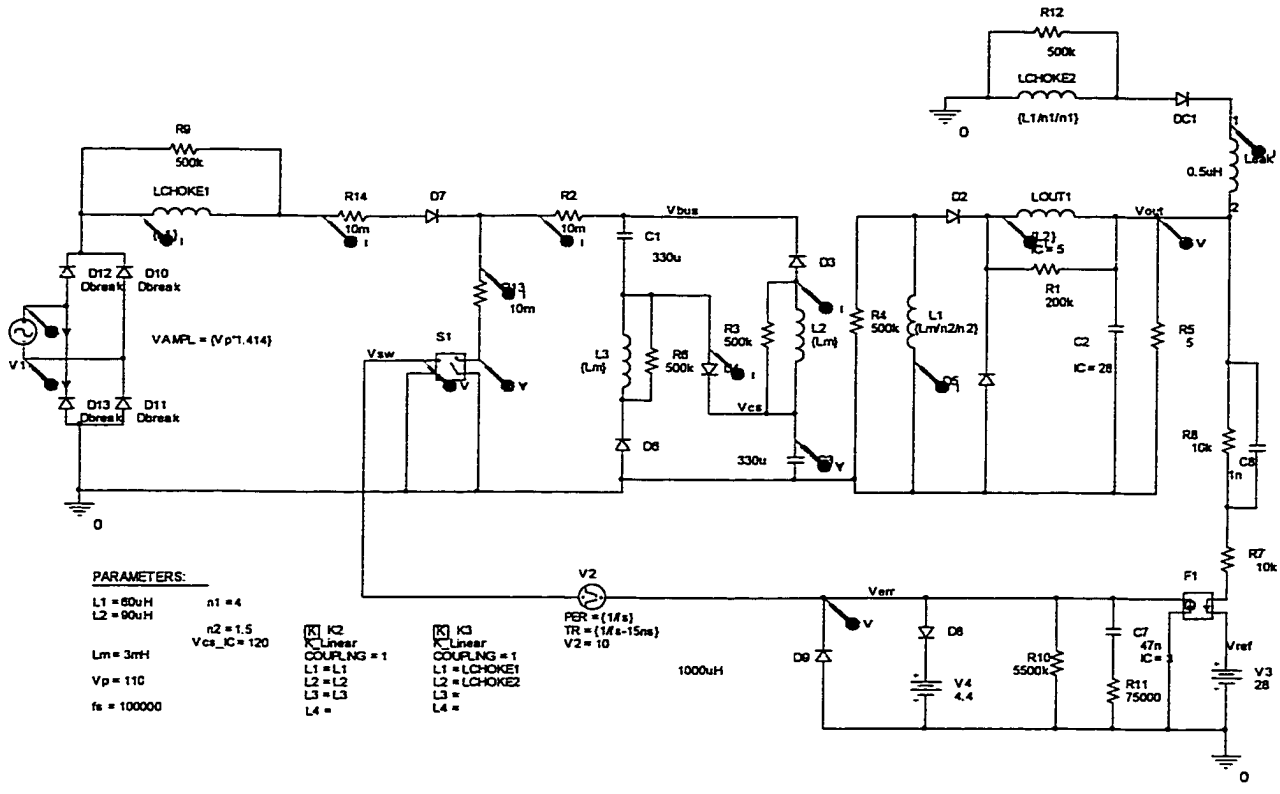
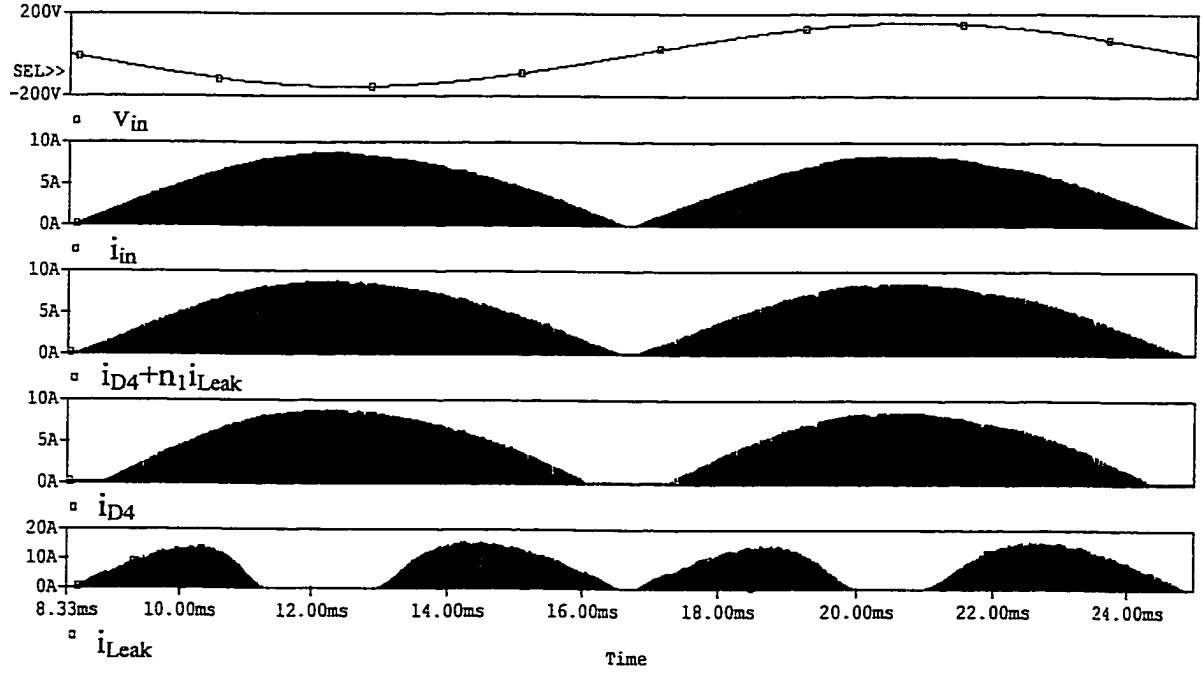
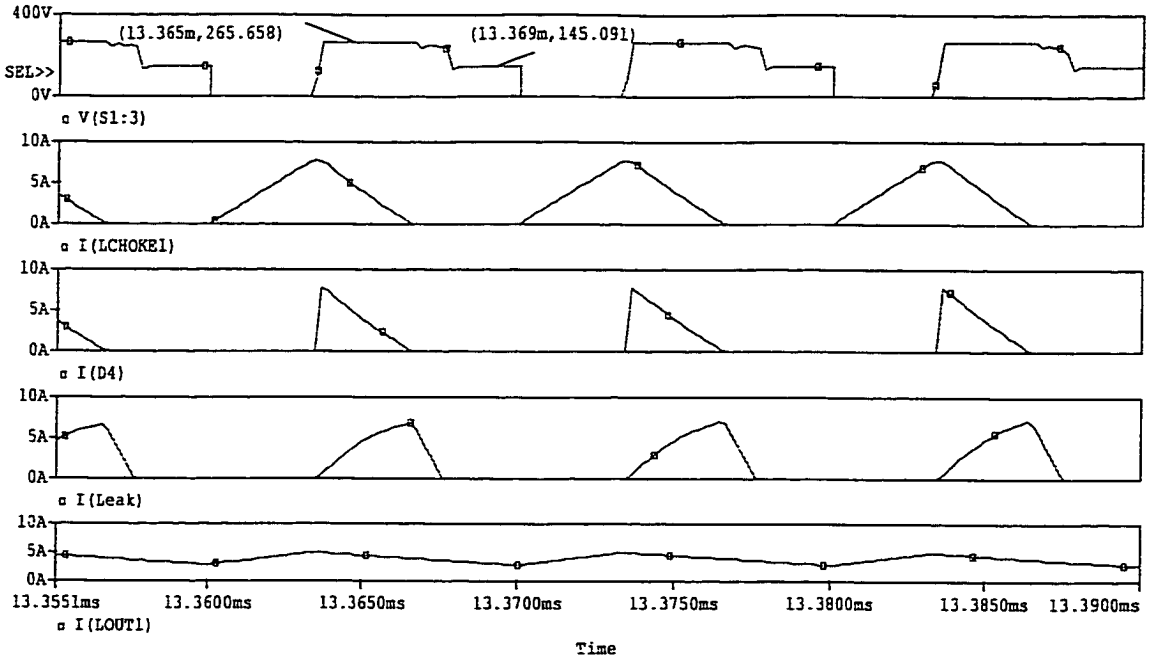


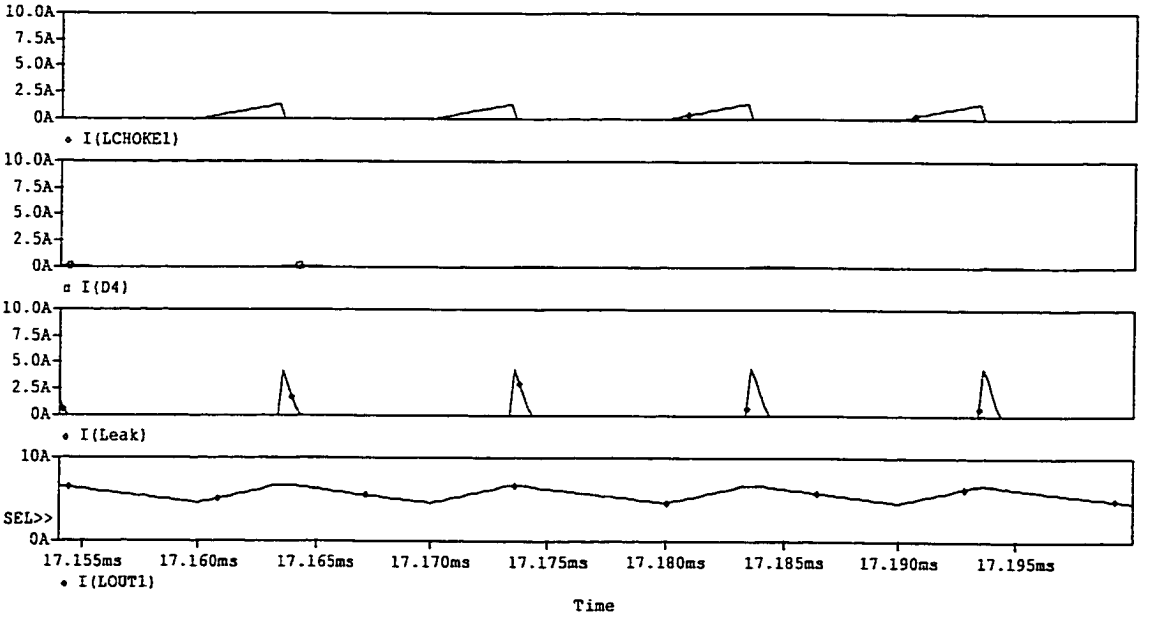
Fig. 4-14. Simulated Schematics based on the OrCAD 9.2.



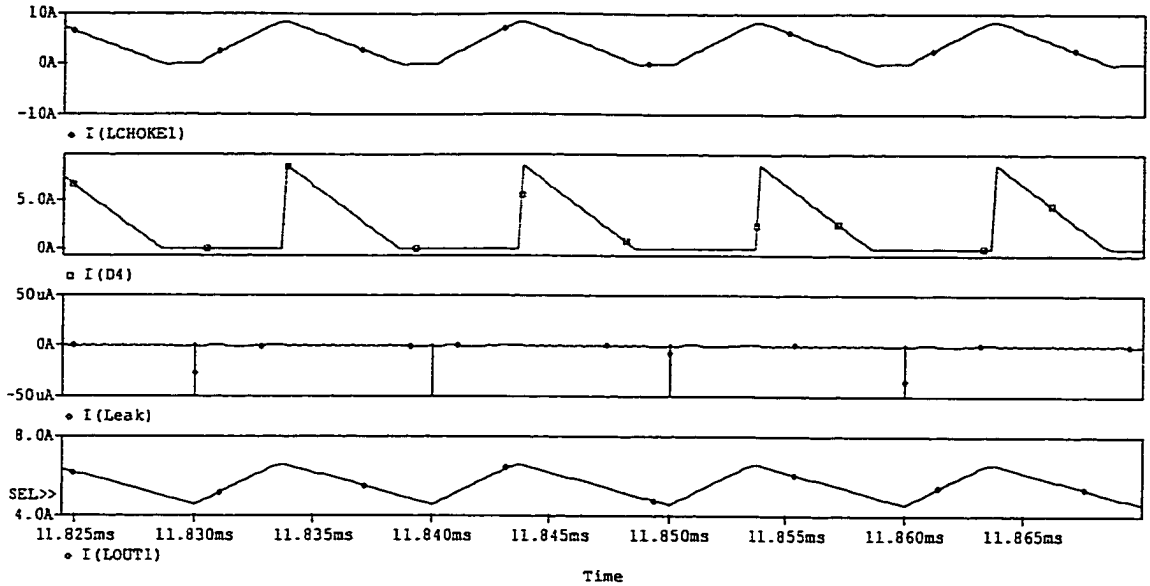
(a)



(b)



(c)



(d)

Fig. 4-15. Interested simulation waveforms of proposed topology for different operation modes under DCM +CCM operation: (a) power flow in terms of line cycle, (b) mixed mode in terms of switching cycle, (c) flyback mode, and (d) boost mode.

4.5.2. Verification for DCM+CCM Operation

This is to verify that the proposed converter has capability to run in (DCM+CCM) mode; at this point it is very different from other regular S^2 converters. The mainly designed circuit parameters are f_s=100kHz, L_1=56.7uH, L_o=100uH, n_1=0.34, n_2=0.67, C_{s1}=C_{s2}=220uF. Target specifications are:

- Universal line voltage: 85 – 265 V_{rms};
- Nominal line voltage: 110VAC;
- Output voltage: 28VDC;
- Output power: 150W;
- Hold up time:0.17ms;

- Switching frequency: 100kHz;
- Ripple limit 200 mV p-p;
- Power factor higher than 0.95;
- Regulation 1%.

An experimental verification is completed based on the same testbed prototype in Fig. 3.31. The following measurement equipment was used:

1) AC Source and PFC measurement: HP4861A;
2) DC Voltage measurements: HP34401;
3) Waveforms were recorded using HP54542A oscilloscope;
4) Dynamic measurements: DSO Le Croy PS374 system with Diff. Amplifier DA1855A/DXC100A and current probe CP015; and
5) Load: Agilent N3300A.

Figure 4-16 shows experimental waveforms of input line voltage and input line at nominal line voltage, and a near unity power factor 0.994 is measured and it dawn a nice sinusoidal shape from input. Figure 4-17 shows simulated and experimental waveforms of drain-source voltage and drain current of the main switch (MOSFET). Figure 4-18 shows experimental power factor, efficiency and storage capacitor voltage varying with input line voltage. It can be seen that the curves of power factor and efficiency take only a little bit change under universal input from 85 to 270V, and dc bus voltage Vcs varies only from 110V to $265V_{ac}$, which make 600V stress power devices commercially available.

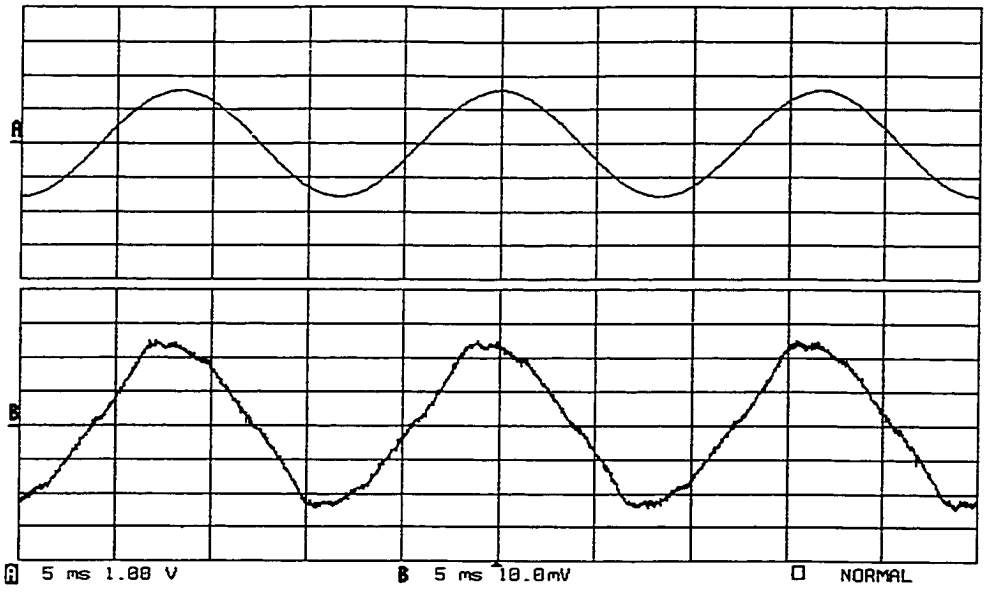
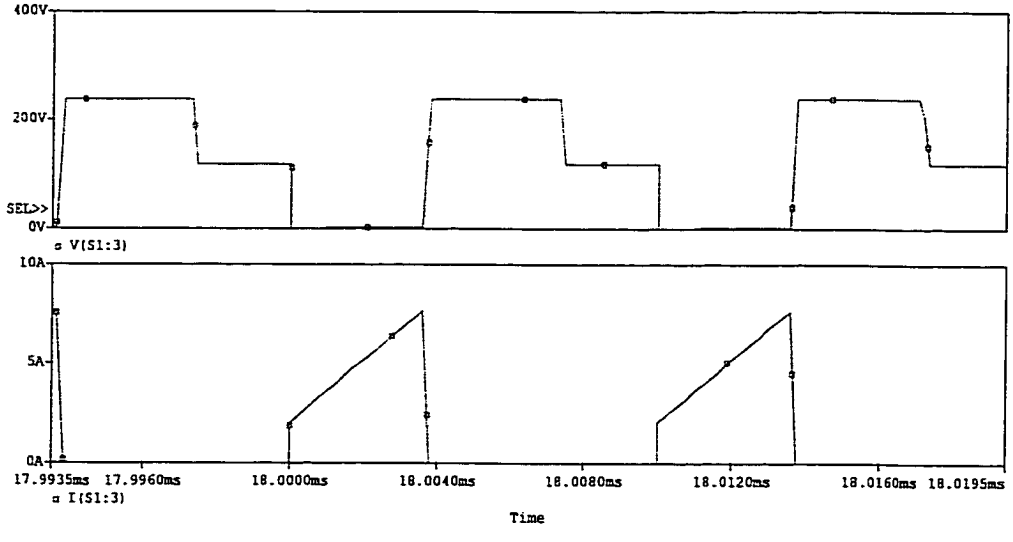
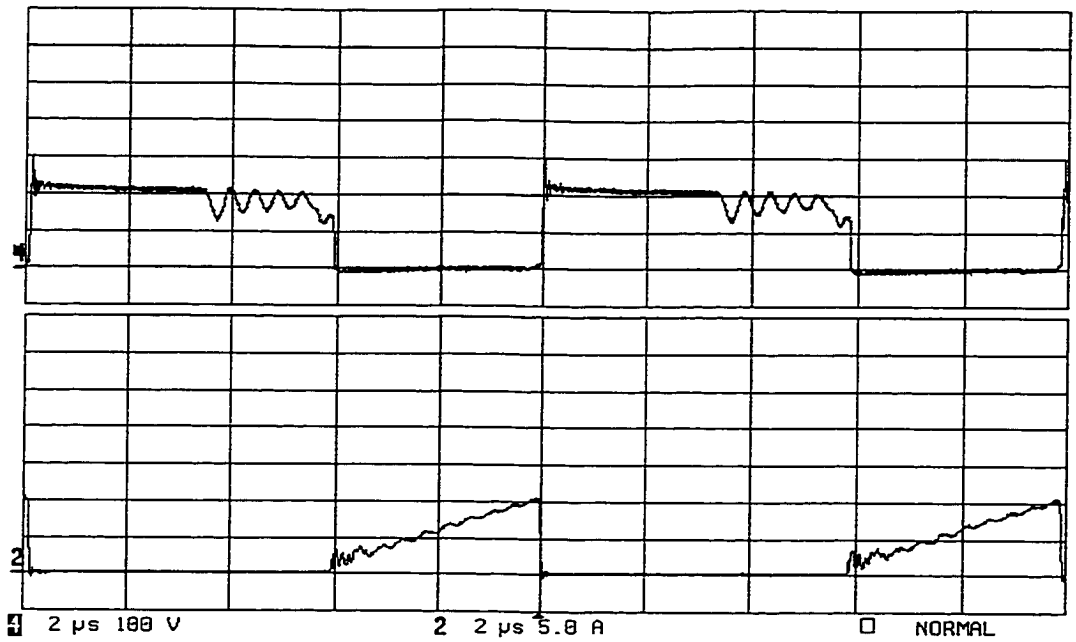


Fig. 4-16. Experimental line voltage and line current at nominal voltage=110Vrms: trace A, line voltage (100V/div, 5ms/div); trace B, line current (measured after auxiliary line filter;1A/div; 5ms/div), and the measured power factor is 99.4%.

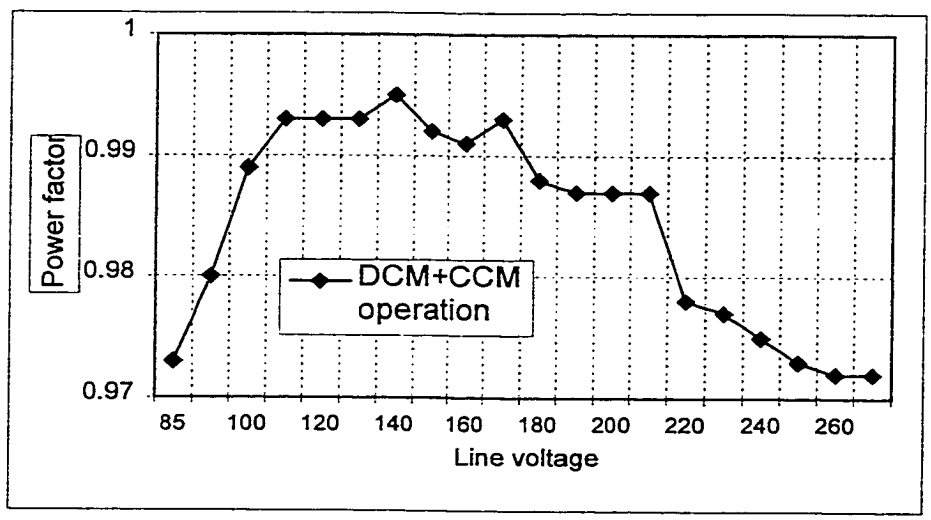


(a)

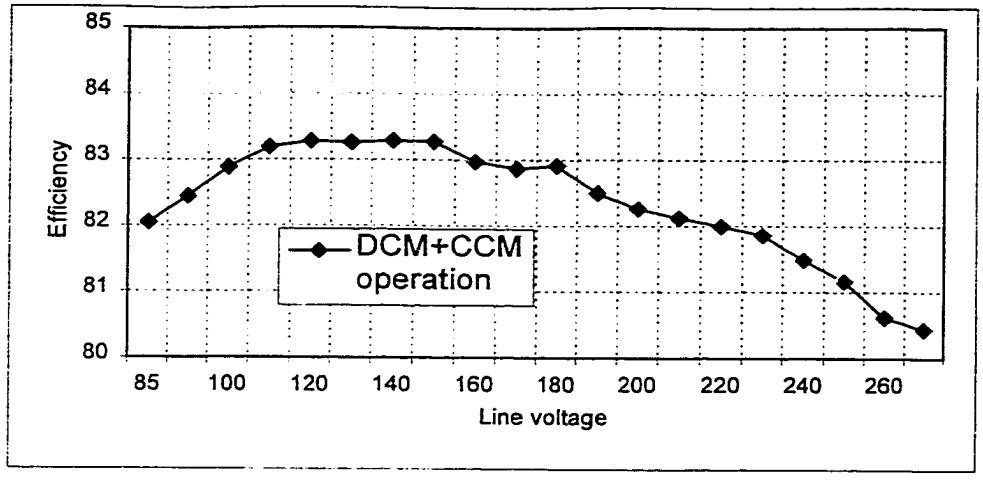


(b)

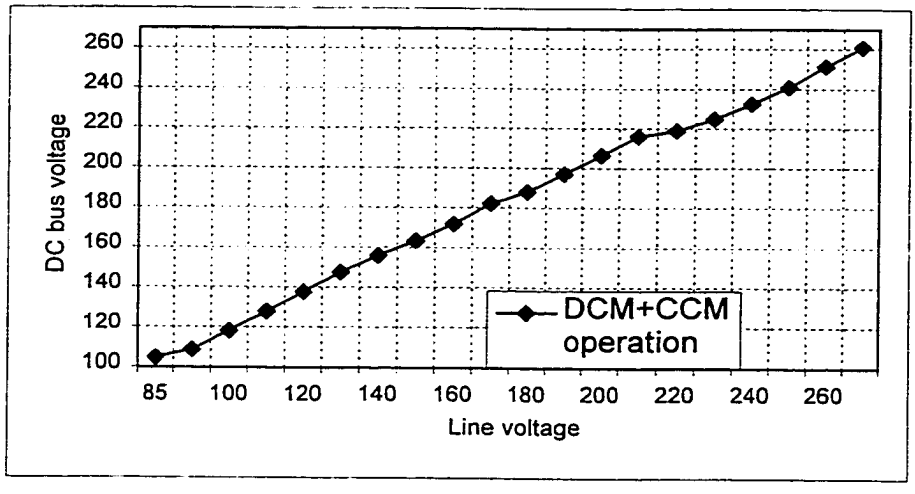
Fig. 4-17. Simulated and experimental waveforms of drain-source voltage and drain current of the main switch.



(a)



(b)



(c)

Fig 4-18.Experimental results: (a) power factor, (b) efficiency, and (c) storage capacitor voltage varying with input line voltage.

4.5.3. Verification and Comparison for DCM+DCM Operation

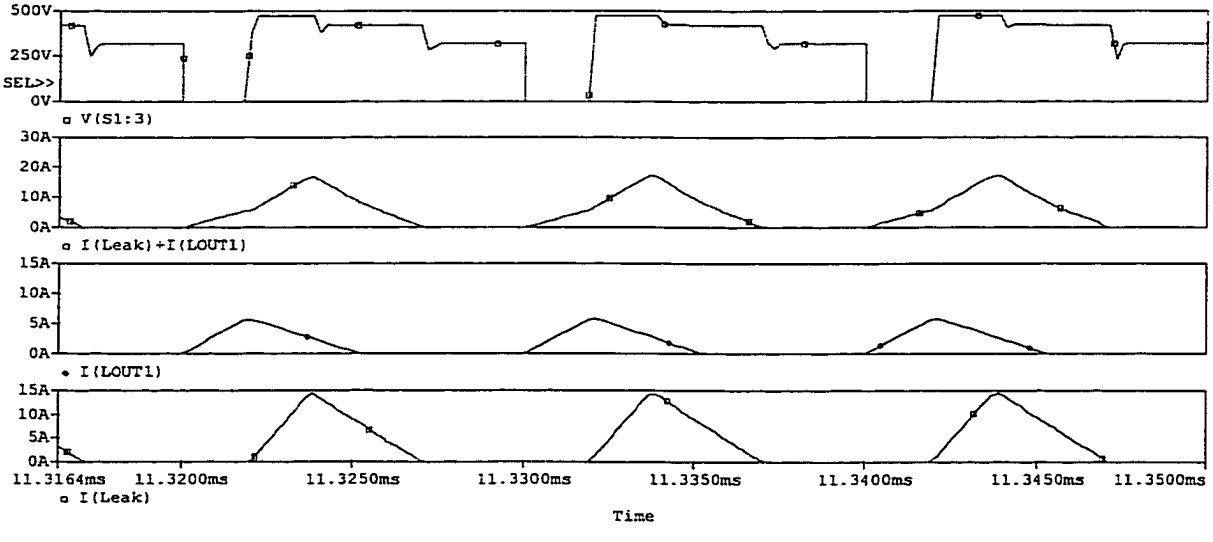
An experimental verification is completed based on the testbed prototype modified from Fig. 3.31. A popular reference and control chip TL431 is used to achieve closed-loop control. Except the above experimental condition, the following experimental conditions are applied:

1) The mainly designed circuit parameters are f_s=100kHz, L_1=90uH, L_o=15uH, n_1=0.242, n_2=0.333, C_{s1}=C_{s2}=220uF.

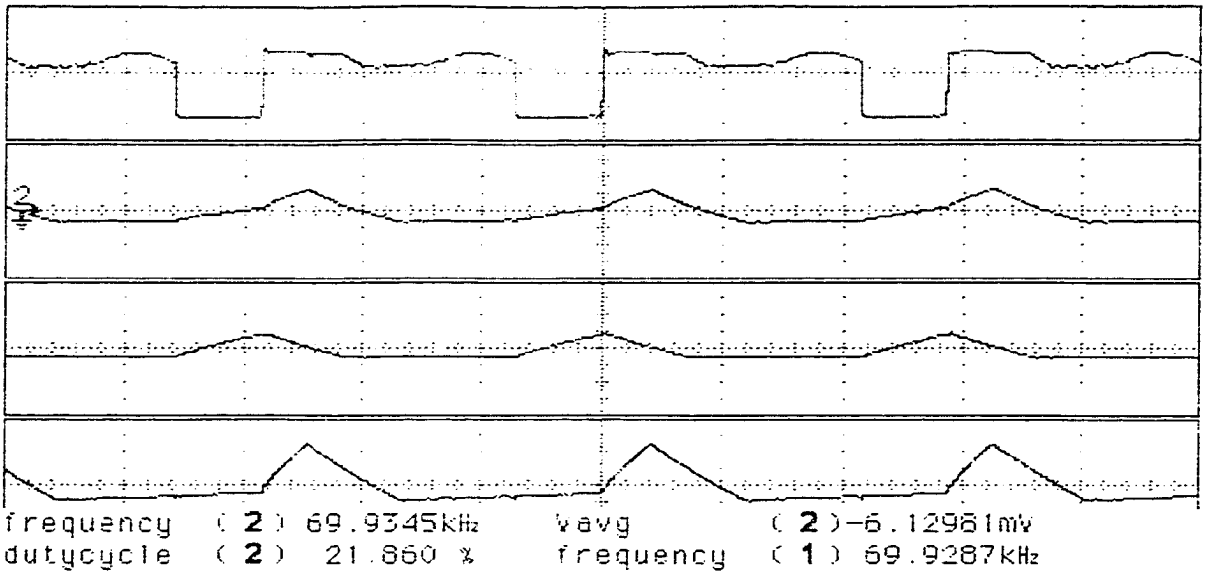
2) All losses are included while calculating efficiency.

3) For the convenience of comparison, the measurement is completed at full load 150W output power. In addition, we have obtained comparative efficiency and power factor while running the same prototype over 200W output power even if under DCM+DCM combination.

Figure 4-19 shows the simulated and experimental waveforms of V_{ds} on the switch, interleaved secondary side output current, forward and flyboost DC/DC secondary side currents. The waveforms show important characteristics of the proposed topology, that is to say, interleaved output current and multiple channel power transfer, which are obtained by only a power switch and one controller. Figure 4-20 shows simulated and experimental waveforms on the active switch. MOSFET drain-source voltage and current waveforms are almost spike-free and thus a low voltage stress MOSFET can be used.

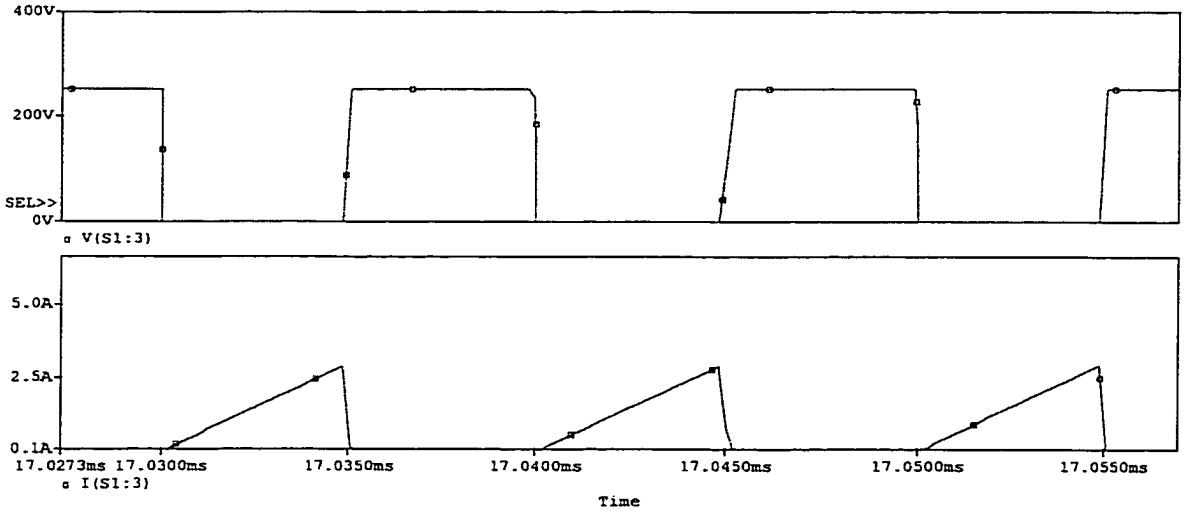


(a)



(b)

Fig. 4-19. Simulated and experimental waveforms of showing interleaving at high line, from upper to lower lines, V_{ds}, interleaved secondary side output current, forward and flyboost secondary side currents: (a) simulated results, (b) experimental results.



(a)

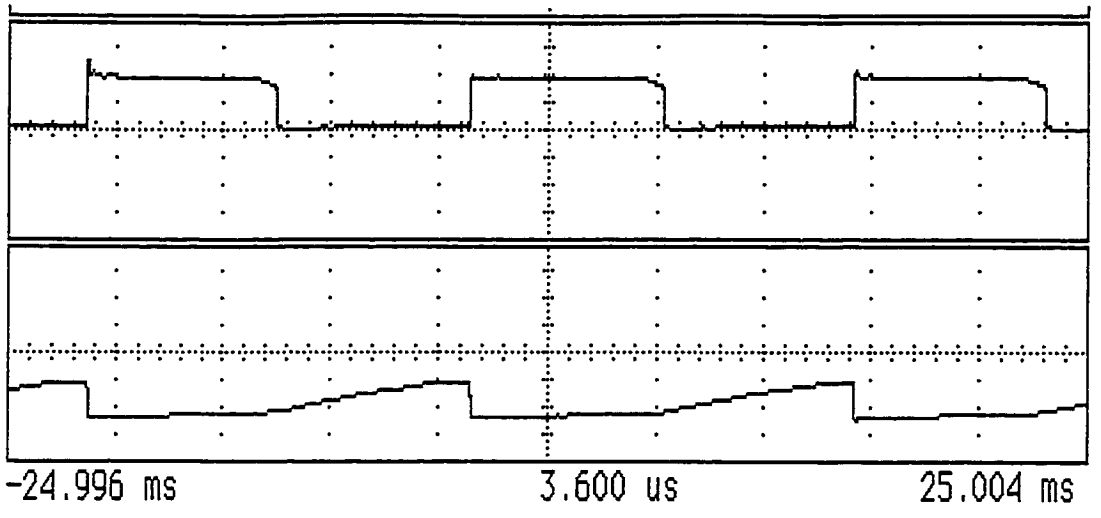


Fig. 4-20. Simulated and experimental waveforms for the active switch at low line: (a) simulated waveforms, and (b) experimental waveforms.

Measured power factor under universal input is shown in Fig 4-21. Compared to Fig. 3.33, it can be seen that the proposed converter significantly improves power factor and an above 0.97 power factor can be achieved under universal input. For Russian's topology, although high power factor is obtained, it cannot operate under universal input. Figure 4-22 shows experimental efficiency comparison with different topologies at full load 150W output. Note that all losses have been included while calculating the efficiency. It can be seen that the topology with flyboost PFC cell has the highest efficiency, the second Russia's topology. Figure 4-23 shows experimental dc bus voltage comparison with several similar topologies at full load. It is manifest that the topology in Fig. 3-14 has the lowest dc bus voltage, but its variation range is comparable to topology with flyboost PFC cell, about 130V. Russia's topology has excessive bus voltage when input exceeds 150V, and it makes the topology be impractical for universal input applications.

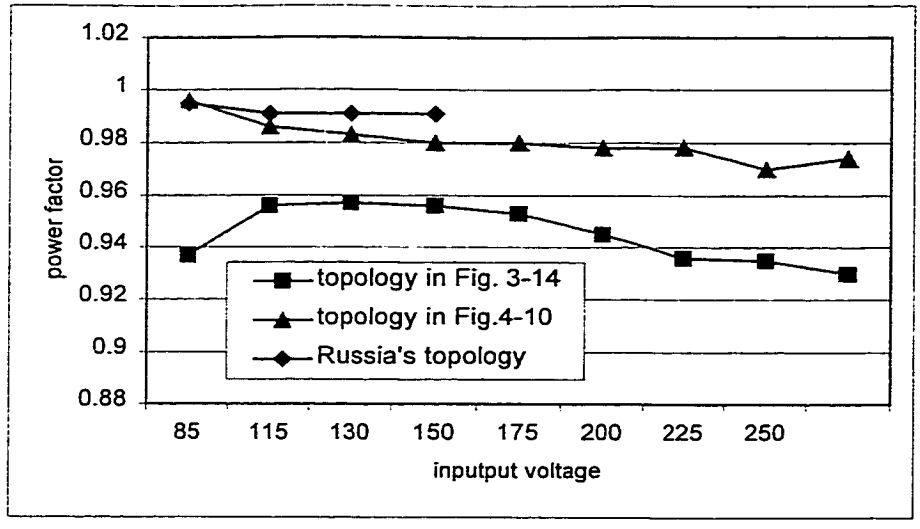


Fig. 4-21. Experimental power factor comparison for a 150W S^2 converter using several similar topologies.

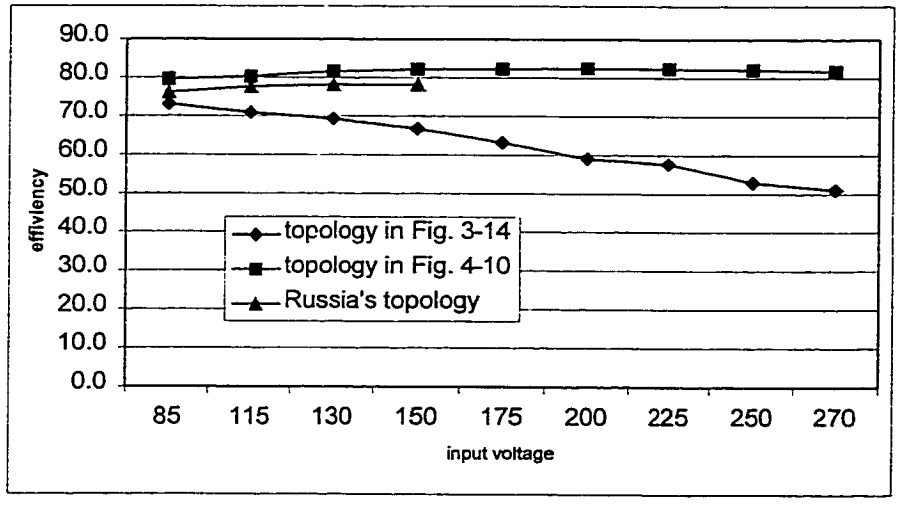


Fig. 4-22. Experimental efficiency comparison with several similar topologies.

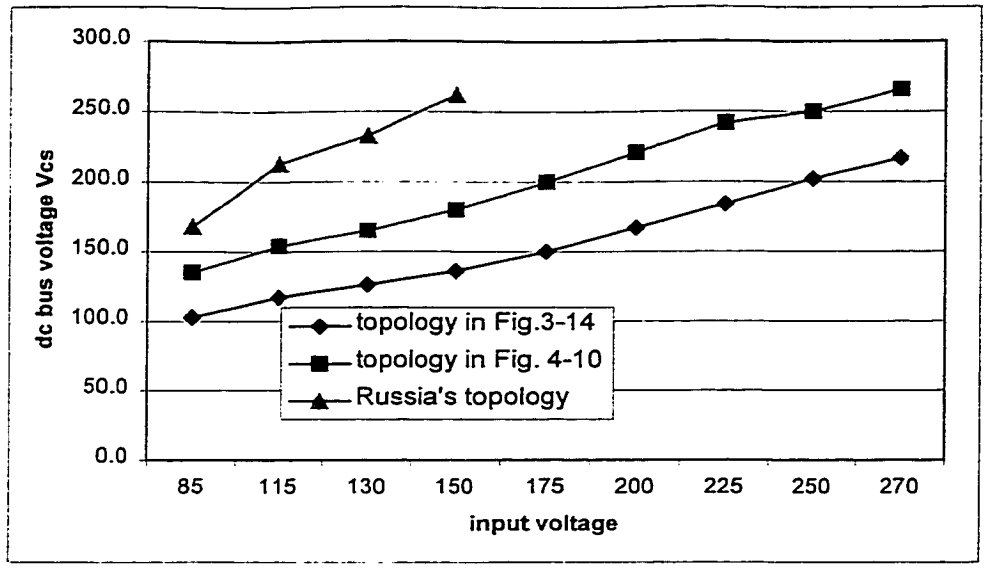


Fig. 4-23. Experimental dc bus voltage comparison with several similar topologies.

4.6 Summary

Direct power transfer (DPT) concept, with which input power is processed only once to reach the output, is introduced to implement high efficiency S^2 PFC converters while still keeping the tight regulation of the output voltage, high power factor and hold-up time. The concept is also suited for other configuration front-end converters such as two-stage PFC converters where an independent PFC cell cascades by another DC/DC cell.

A power correction factor (PFC) cell, called "flyboost", is presented. It combines functions of the flyback transformer and the boost inductor. While operating at flyback mode, the flyboost cell will directly transfer input power to the load; while at boost mode, it will transfer the input power to the storage capacitors for following DC/DC converter to conduct fast regulation for the output voltage. By having the flyboost cell operate at DCM, only a simple control will be required to achieve very high power factor (greater

than 0.97). By using the flyboost cell, the part of input power is processed only once by DPT approach, which will significantly improve the efficiency (increasing over 5% than converters without DPT at nominal line voltage). Another important characteristic of the flyboost cell is that it will also automatically limit the DC bus voltage through properly designed flyboost transformer and power train, which means that above combined converters can operate either DCM+DCM mode or DCM+CCM mode while still keeping simple control circuitry. As a result, the proposed converters are especially suitable for universal voltage applications with higher power handling capability than other known converters. By combining the flyboost cell and any family of other DC/DC conversion cell, we can obtain a new family of S^2 PFC converters. Both cells share one main switch and one controller.

As mentioned earlier, the single-ended boost converter is the most frequently used converter in the single-phase PFC applications. Proposed flyboost cell might also be suited for other any topologies to replace PFC cell and thus achieve high performance. Therefore it is predicted that the flyboost cell will challenge conventional PFC cells, such as boost, buck-boost, flyback, SEPIC and Cuk etc.

Finally, it is should be pointed out that more theoretical analysis still remains to be done. For instance, circuit modeling and converter design procedure need to be developed.

This work was supported by the grant from NASA.

5 COMPARISON STUDY OF HIGH POWER DOWN CONVERTERS

5.1 Introduction

It is known that the DC-DPS structure has been gaining increased popularity due to numerous attractions to industry. From the technical development point of view, future customers are driving not only high power factor, low THD and low cost, but also including increased concerns for overall efficiency, and high power-density. For these performance requirements, the front-end converters are very critical system components in any DPS. The research in Chapters 3 and 4 shows that the isolated S^2 converters, when used as front-end converters, are attractive due to their simple structure and control as well as potential low cost. However, their applications are limited to low power and average-performance requirements. For higher power and more critical applications, the two-stage structure front-end converters have to be employed to meet more stringent overall performance requirements. Its power handling capabilities for single module, while still keeping high operating frequency and using MOSFETs as main power switches, can range from a few hundred watts to several thousand watts. For larger scale DPS, system power can reach several hundred kilowatts, for instance, 48V/10kA output capability telecom power system.

As shown in Fig. 2-10, the second block entitled "DC/DC regulator" is also called *down converter* because it cascades after the PFC pre-regulator. In terms of current techniques under hard-switching operation, the PFC pre-regulator can implement about

95% efficiency and the second block can obtain around 92% efficiency. It is well known that high efficiency leads to improved performance such as power density, reliability and packaging, etc. Therefore, a natural motivation is to explore new approaches so as to improve the overall efficiency of a power system.

A relatively new circuit topology family, applicable to the down converters, uses soft switching techniques such as zero-voltage-switching (ZVS) or/and zero-current-switching (ZCS), or zero-voltage transition (ZVT), etc [24-27]. In the primary-side of the isolated down converter for high power applications (say higher than 1.5 kW), the combination of phase-shift control and full-bridge topology (PS-FB), realizing ZVT soft switching operation, has been recognized as one of the most excellent circuit topologies. However, when DC bus exceeds 500V that comes from PFC pre-regulator, particularly from three-phase PFC pre-regulator, PS-FB family of topologies is no longer available for down converters. So the question arises: *Under high input voltage, what kind of topology is available for high-power high-density down converters?*

In the secondary-side of isolated down converter for high power applications, the topologies are mainly limited to both types, namely, full bridge diode rectifier or center-tapped rectifier. Furthermore, in most of applications, the center-tapped one is the preferred rectification structure because it has only one diode forward voltage drop. In fact, there is another alternative rectification technique, i.e., current doubler topology. Unfortunately, it seems that the current doubler is conventionally recognized as the solution for large-current but low-power applications. Therefore, a complete comparison study is necessary while transplanting this technique to high power applications. It should be identified w*hat benefits can we get? And what issues will we encounter?* The objective

in this chapter is to attempt to answer the above questions.

5.2 Comparison Analysis of Primary-Side Topologies

5.2.1 Topology under Medium DC Input Voltage

Shown in Fig. 5-1 is the basic structure of a typical two-stage front-end converter. In single-phase ac universal input system, the intermediate DC bus voltage between the two stages is approximately 380Vdc. Typically, the total change in bus voltage is due to variations in line and load variations. The effect of the 120 Hz ripple current is limited within 5%, i.e., the DC bus voltage fluctuates in the range of 360V to 400V.

But for three phase ac input system with PFC pre-regulator, the intermediate voltage may range approximately from 800Vdc to 900Vdc. For example, three phase rectifiers with a power factor correction stage based on the step-up converter did.

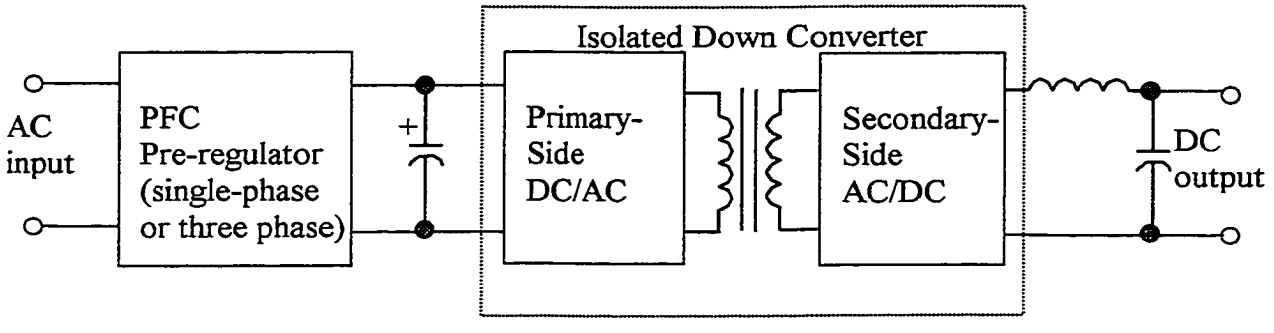


Fig. 5-1. Basic structure of a two-stage front-end converter.

When the intermediate DC bus voltage is around 380Vdc, there are a lot of alternative soft switching topologies that can be integrated into conventional FB converters, such as ZCS PWM, ZVZCS PWM, ZVT and various resonant FB converters.

Of these possible candidate schemes, ZVT-PS-FB is preferred because of its simple power circuit, high efficiency, low EMI levels and simple analysis than its resonant competitors.

Figure 5-2 shows a classical ZVT-PS-FB schematic. The parasitic body diodes and capacitors on the switches can be completely utilized to obtain the ZVT operation. In high power DC/DC conversion applications, its characteristics, theoretical analysis and design procedure have been well documented for the topology in Fig. 5-2 in the literature [68-73]. This circuit is capable of delivering high efficiency at high operating frequencies because it combines the advantages of zero voltage resonant transitions to reduce the switching losses and square wave power conversion to maintain optimal utilization of the semiconductors. Additional benefits are constant frequency operation, reduced EMI and the integration of the parasitic circuit components, junction capacitances, leakage inductance and MOSFET body diodes in the power circuit. A few possible shortcomings of the topology include the relatively complex phase-shift PWM algorithm and the potential loss of soft-switching at light load. In fact, there have been very mature control chips for phase-shift PWM such as UCC3875, UCC 3879 and UCC3895, etc.

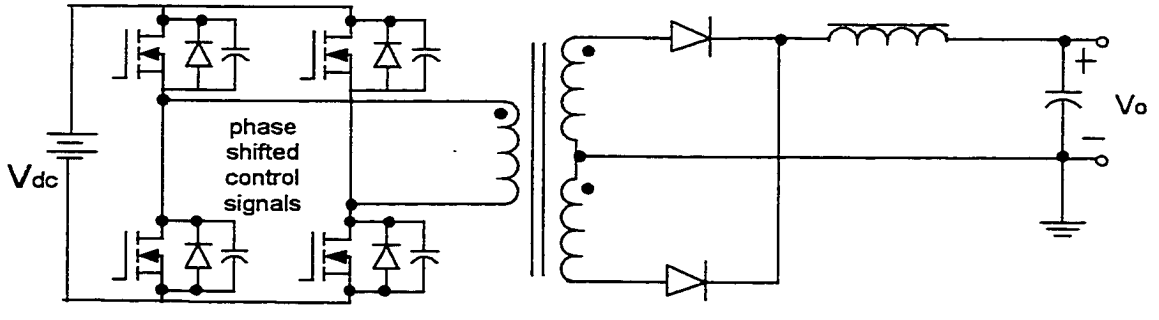


Fig. 5-2. A classical ZVT-PS-FB schematic.

The circuit on the primary side resembles the conventional full bridge converter

without the usual snubber circuits. Due to the phase-shift PWM control method applied to the circuit, the dominant turn-on losses of the MOSFET transistors are eliminated while soft-switching is maintained. However, turn-off losses are still present in the circuit. They can be significantly reduced by using a low impedance gate drive circuit for quick turn-off of the switching devices. The greatly reduced switching losses explain the absence of the snubber circuits commonly present in the conventional FB converters.

5.2.2 Topologies under High DC Voltage

As stated, ZVT-PS-FB converter is one of the best options for high-power high-frequency applications. However, the conventional FB PWM converter is not suitable for high input voltage applications, say over 800V DC bus voltage, because standard power MOSFETs with 500V/600V breakdown voltage cannot be used with 800 Vdc input for the topology ZVT-PS-FB. On the other hand, the high voltage devices, such as bipolar, IGBT, could not be used in high frequency operation, i.e., higher than 50kHz.

Efforts have been made to find alternatives for the conventional ZVT-PS-FB converter with the purpose of reducing the voltage stress across the switches allowing the use of low cost and low voltage MOSFETs devices with low losses. There are mainly two approaches to obtain available topologies used for high input voltage, namely, multilevel cell combination and multi-converter combination schemes. The viable topologies from the above two approaches are described as follows:

Topology #1: Based on the multilevel voltage cell with neutral point clamped [74]

As shown in Fig. 5-3, commutation cell uses series connected semiconductors with clamped circuits to ensure the voltage sharing across the blocking switches. The

clamping circuit consists of diodes and capacitors with the purpose of guarantying static and dynamic sharing of the voltage and also to limit the excessive dv/dt. The switches (S_1, S_2, S_3 and S_4) form the main switching leg.

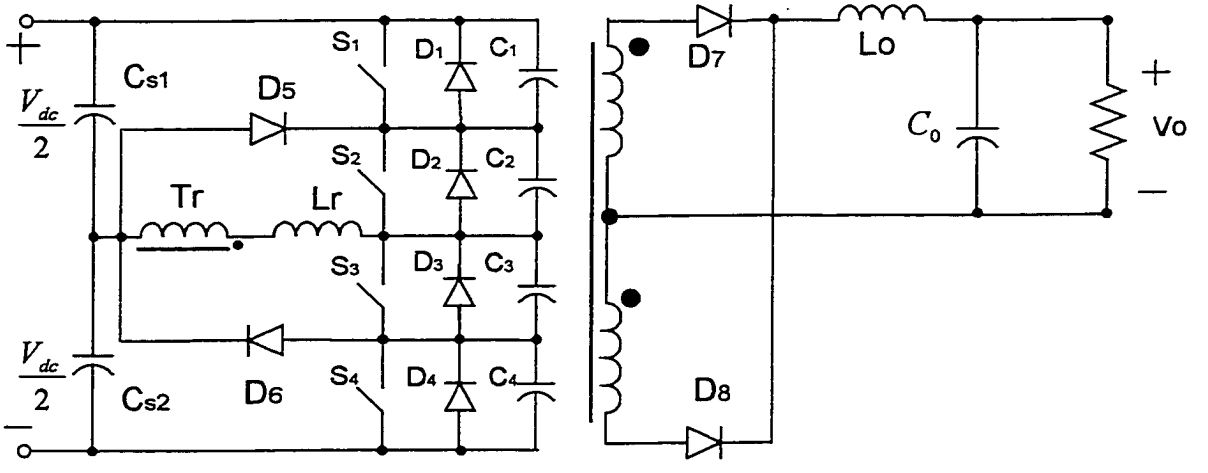


Fig. 5-3. Topology #1: based on the multilevel voltage cell with neutral point clamped.

This converter operates identically as the FB ZVS converter. By using the two capacitors as the two voltage sources, the diodes (D_5 and D_6) clamp the voltage across the switches at $V_{dc}/2$. This method reduces the voltage stress of primary switches by half.

The ZVS turn-on of all switches can be obtained through the resonance between inductor L_r and the capacitors C_1, C_2, C_3 and C_4. Its efficiency should be comparable with the topology ZVT-PS-FB working at lower bus voltage. Similar to the above ZVT-PS-FB, there is a trade-off among the choice of the extra inductor L_r, soft switching range and duty cycle loss.

Topology #2: Based on the multilevel voltage cell with a floating capacitor [75]

Figure 5-4 shows another ZVS-PWM converter proposed. It is based on the three level voltage cell with a modified floating capacitor. The two legs of a full-bridge converter (S_1-S_2 and S_3-S_4) are connected in series across the DC input voltage to form this converter. The node at which the two legs are joined is held at half of the input voltage, $V_{dc}/2$.

The voltage across the series capacitor must be kept at $V_{dc}/2$, applying the same duty cycle to the switches couples S_1-S_2 and S_3-S_4. The efficiency of this converter should be comparable to the ZVT-PS-FB, because the ZVS turn-on of the switches is obtained by an inductor L_r and the capacitors C_1, C_2, C_3, and C_4.

In fact, employing multilevel cell combination idea, the above two topologies can be further expanded into the so-called multiple stacked converters, namely, using two 3-level converters (four input series capacitors) stocked together, voltage stress for the device can be further reduced by one fourth.

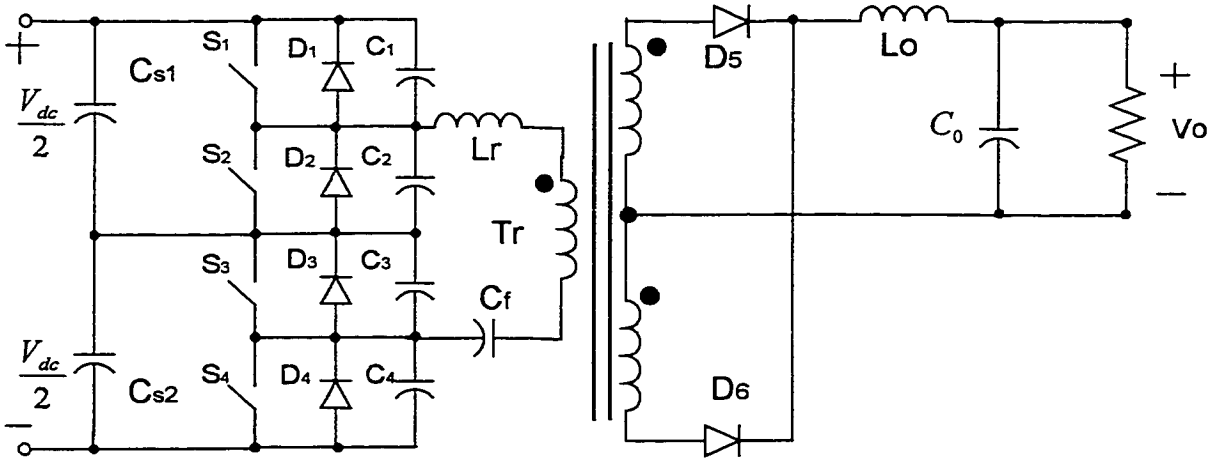


Fig. 5-4. Topology #2: based on the multilevel voltage cell *with* a floating capacitor.

Topology #3: Based on the series combination of half bridge converter [76, 77]

Topology #3 is a series combination of two isolated half-bridge converters. The first one is formed by capacitors C_{s1} and C_{s2}, switches S_1 and S_2 and transformer T_{r1}. The other one is formed by capacitors C_{s3} and C_{s4}, switches S_3 and S_4 and transformer T_{r2}.

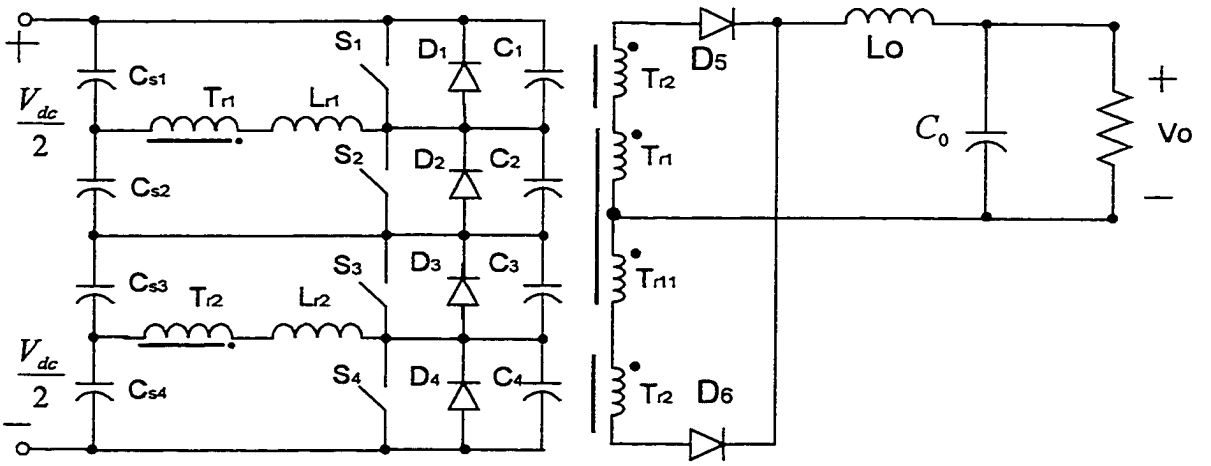


Fig. 5-5. Topology #3: based on the series combination of half bridge converter.

The ZVS turn-on of the switches is obtained by similar mechanism as the ZVS half-bridge converters. The operation may be sensitive to a good symmetry of the current path, a good coupling of the magnetic elements, and the symmetry of dive signals.

Topology #4: Double full bridge ZVS converter [78, 79]

The double full bridge ZVS Converter is shown in Fig. 5-6. It is a series association of two isolated full-bridge converters. Switches S1 to S4 form the first one and switches S5 to S8 form the second one. The node at which the two converters are joined is held at half of the input voltage. Thus, the voltage across the switches will be clamped at $V_{dc}/2$.

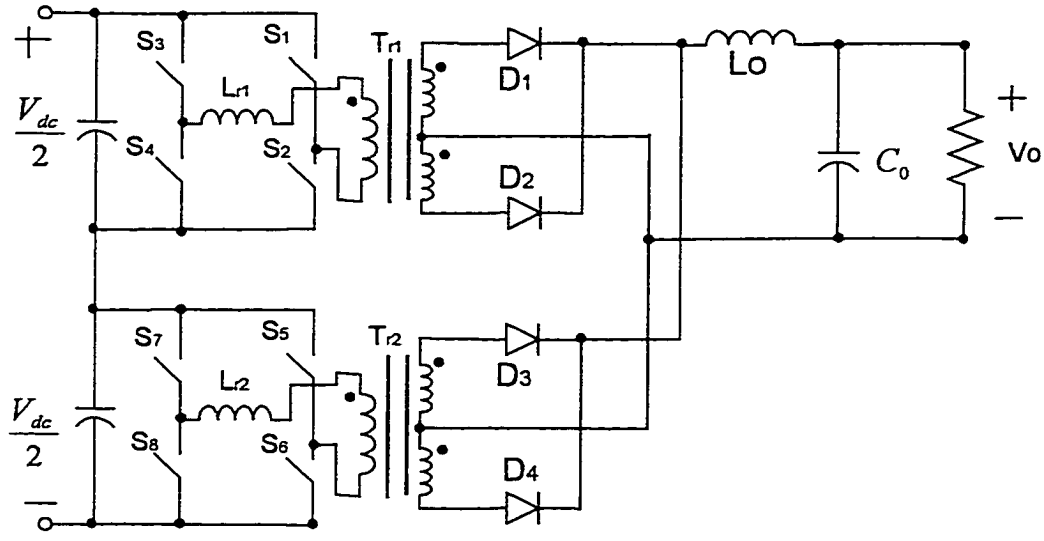


Fig. 5-6. Topology #4: double full bridge ZVS converter.

It should be pointed out that this circuit works properly only if the two converters are identical. Any small difference in the structure or operation process, for instance, will create unbalance on the capacitor voltages and will subsequently destroy the switches. When using such a method, an active control circuit must be able to correct all differences.

Topology #5: Double full bridge ZVS converter coupled by a transformer [78]

The method of using two full-bridge in series only work in practice if a perfect split of the voltage between the converters can be guaranteed at any time. This condition is attainable by coupling the converters with the power transformer. According to Fig. 5-7, the circuit uses two identical ZVS full-bridge converters. The bridges employ the same power transformer and are controlled by the same feedback loop. The transformer

contains two identical primary windings carrying the current from the two bridges. However, a single secondary winding provides the power to the load.

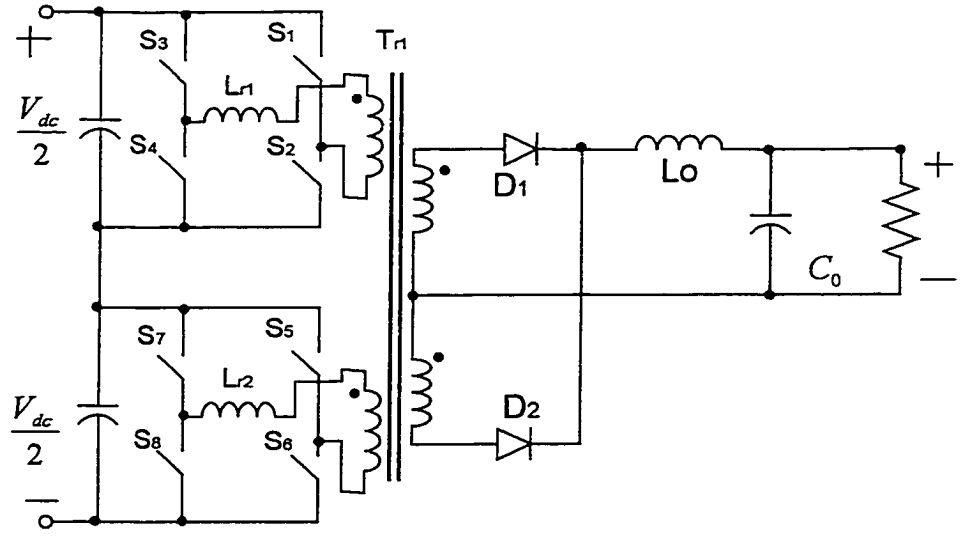


Fig 5-7. Topology #5: double full bridge ZVS converter coupled by a transformer.

As the two bridges share the same control circuit, identical transistors are switched on and off simultaneously. Any small difference on the input voltage is automatically corrected thanks to a small transfer of energy into the power transformer.

Topology #6: Double full bridge ZVS converter coupled by two transformers

If the power requirements become extremely high, it might be necessary to use more than one power transformer. Figure 5-8 shows the method of connecting the windings to achieve the desired effect.

By connecting the secondary windings in series, the secondary currents flowing in both windings are the same and therefore demand equal energy transfer from each power transformer. Consequently, as the primary current is the mirror image of the secondary

current, the power demand will be equally shared between the transistors. The correct division of the two input voltages is still controlled by the primary windings of the same transformer, which is also necessary to guarantee the same current flow in each primary winding.

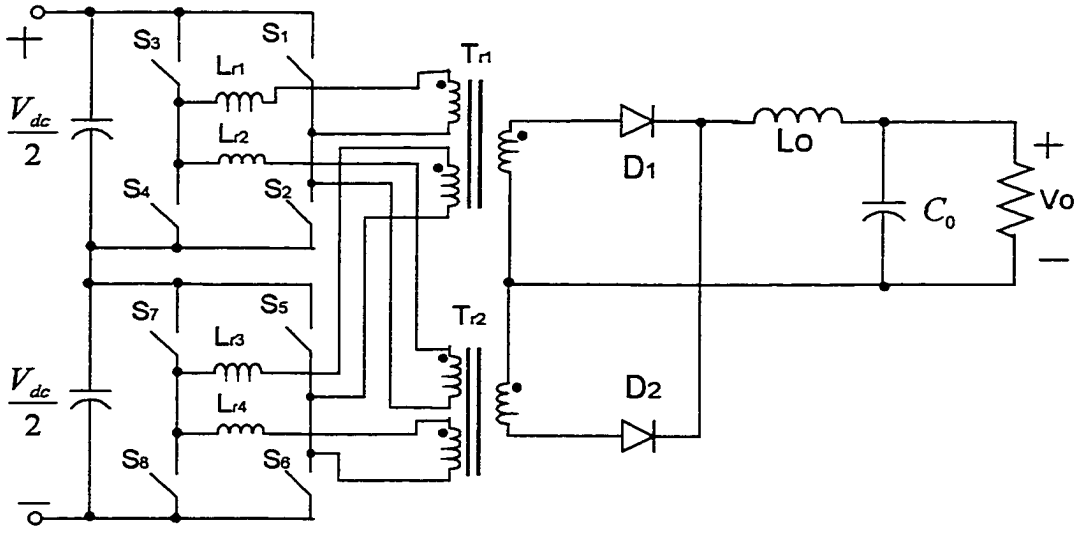


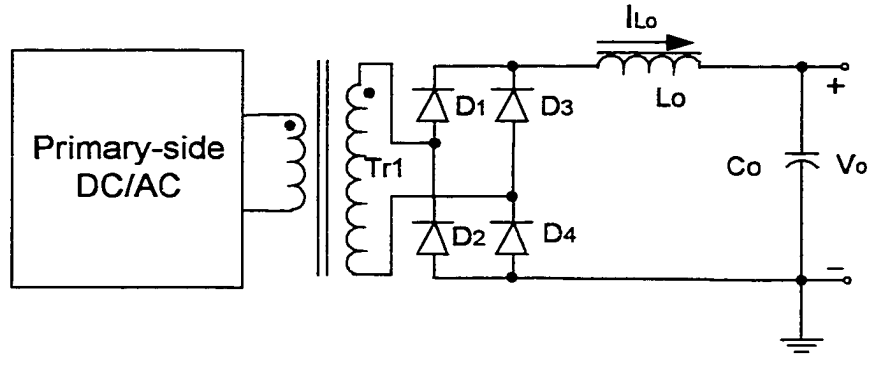
Fig. 5-8. Topology #6: double full bridge ZVS converter coupled by two transformers.

5.3 Comparison Study of Secondary-Side Topologies

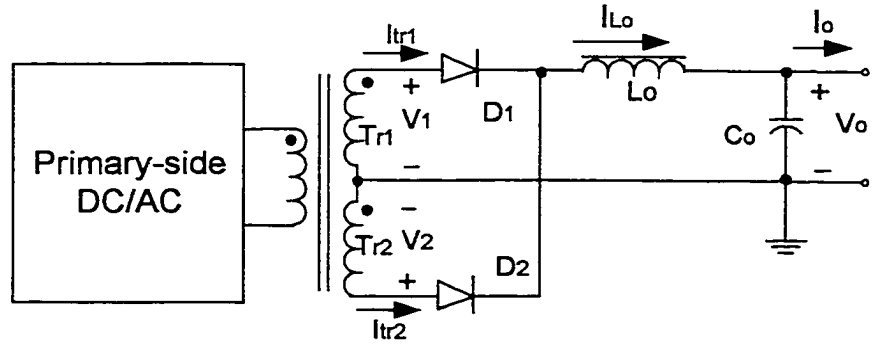
As mentioned before, for the primary-side of down converters, the most effective approach to reduce the switching losses in a bridge converter is to use phase shift control. When phase-shift control is applied, the bridge converter can be operated in soft switching, also called zero voltage transition mode. This technique combines the benefits of zero-voltage resonant transitions to reduce the switching losses and square wave power conversion to maintain the optimal utilization of the semiconductor switches. Unless

specified, the primary-side topology involved in the following circuits is all for phase-shift controlled full-bridge structure, as shown in Fig. 5-2.

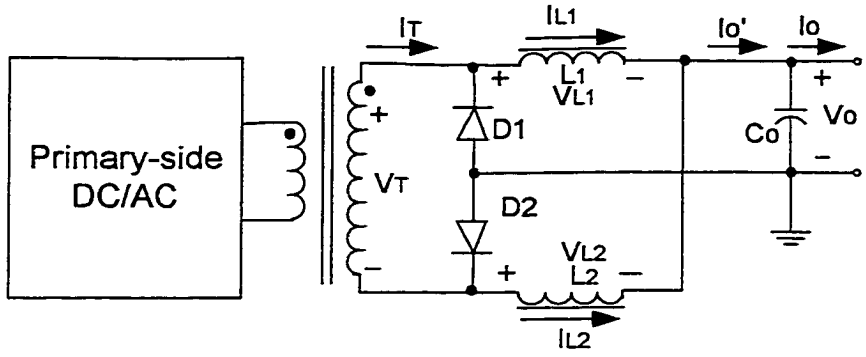
For the secondary-side of down converters, particularly for high power high current output converters, optimizing topology is also important. Basically, there are three alternative rectification topologies, namely, full-bridge rectification, center-tapped rectification and current-doubler rectification, as shown in Figs. 5-9(a), (b) and (c), respectively. Due to double diode forward voltage drop, full-bridge rectification has gradually been replaced by the latter two rectification topologies. Therefore, the following comparison study is focused on the center-tapped and current doubler, secondary-side topologies.



(a)



(b)



(c)

Fig. 5-9. Three commonly used secondary-side topologies: (a) full-bridge diode rectification, (b) center-tapped rectification, and (c) current doubler rectification.

5.3.1 Principle of Operation

The following analysis assumes a full-bridge converter using the phase-shifted control method. Consequently, the primary of the isolation transformer is short circuited in the freewheeling mode which has a profound effect on the current distribution in the secondary windings during that period. Based on the polarities and signal annotations of Figure 5-9(b), circuit operation is as follows:

Figure 5-10 shows the key waveforms of center-tapped rectification topology of Fig. 5-9(b). During the first active period when energy is transferred from the primary to the secondary side, the voltage across the T_{r1} is positive. D_1 is forward biased while the negative voltage appearing across T_{r2} keeps D_2 reverse biased. The current of the output inductor, L_o, is forced to flow through T_{r1} while T_{r2} carries no current. During the freewheeling period, the voltage across T_{r1} and T_{r2} becomes zero. In theory, the output current is evenly distributed between the secondary windings T_{r1} and T_{r2}. However, in practice, because of the leakage inductance associated with real magnetic structures, the output current is not shared evenly. The T_{r1} still conducts most of the output inductor

current while the current slowly builds up in T_{r2} depending on the value of the leakage inductance and the available voltage across it. In the next active interval, V_2 is positive, in which case T_{r2} and D_2 carries all the current of L_o while D_1 is reverse biased by T_{r1} having no current through them. In the next period, V_1 and V_2 are zero again and similar to the previous freewheeling period, the output inductor current will keep flowing in T_{r2}.

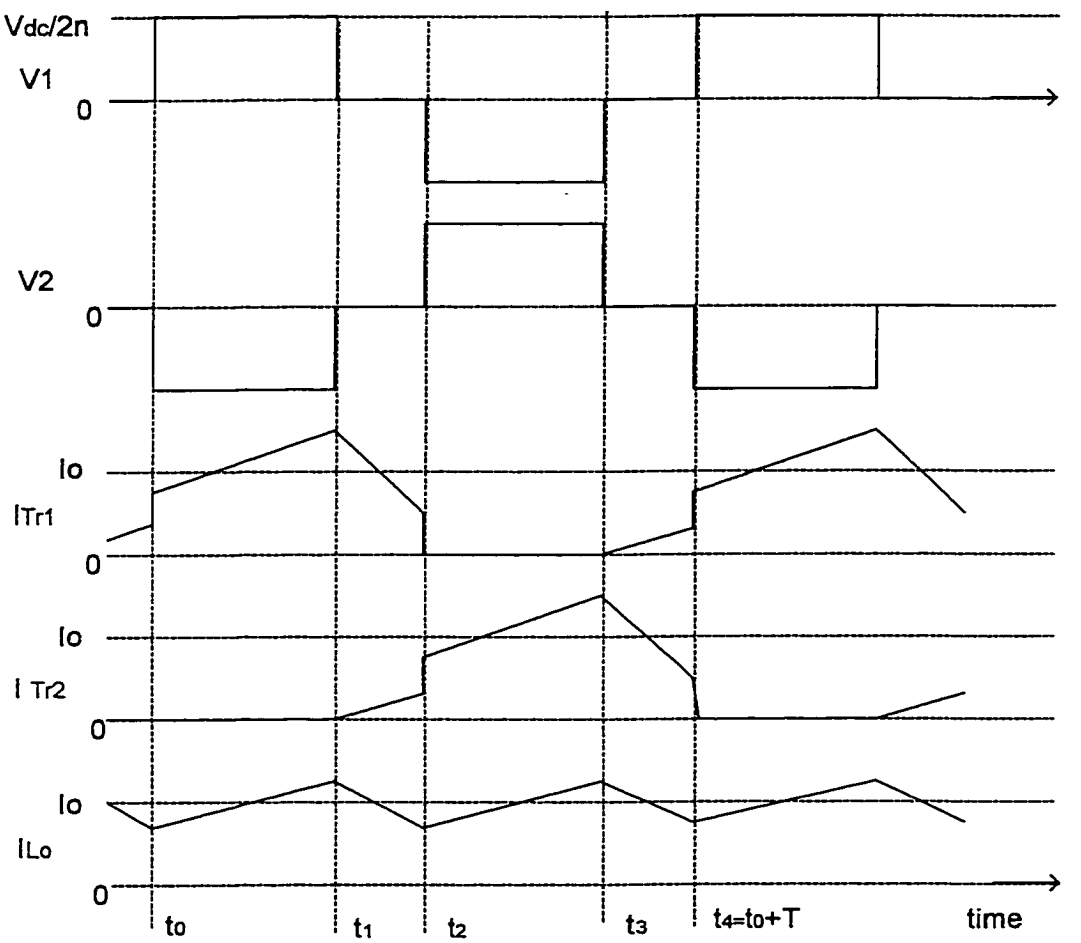


Fig. 5-10. Key waveforms of center-tapped rectification topology of Fig. 5-9(b).

The current doubler rectifier (two inductor rectifier) offers an alternative secondary-side rectification method. The circuit is composed of the secondary winding of

the isolation transformer, two rectifier diodes, two identical filter inductors and an output capacitor. In fact, the two-inductor rectifier was first reported in [80]. In recent years, it has been a popular technique, particularly for low-voltage, high-current, low-power DC/DC converter applications. However, a complete comparison study for high power applications still remains to be done [81-85].

Using the variables and symbols introduced in Figure 5-9 (c), Fig 5-11 shows the key operation waveforms of current doubler rectification topology. Circuit operation is as follows:

1) *Period 1 (t_0-t_1)*: During this period, D_1 is off and D_2 is on. Current flows in positive direction in both filter inductors. The sum of two inductor currents supplies the load current, and the current I_{L1} flows through D_2 and the transformer secondary. The voltage across L_1 equals V_T-V_o, and this positive voltage causes I_{L1} to increase. At the same time, L_2 freewheels through D_2 and I_{L2} decreases by the rate of V_o/L_2. The current through the secondary, I_T equals I_{L1} and it accounts for half of the total load current.

2) *Period 2 (t_1-t_2):* In this period, V_T is zero and D_1 and D_2 are both on. The voltage across L_1 becomes $-V_o$, producing a negative slope in I_{L1}, which now flows through D_1. The conditions for L_2 do not change and both inductors are in freewheeling mode.

3) *Period 3 (t_2-t_3):* During period 3, V_T across the secondary winding is negative, D_1 is on and D_2 is off. A positive voltage, V_T-V_o appears across L_2 and I_{L2} starts increasing. In this state, I_T equals to I_{L2}, thus only half of the load current flows in the secondary again. L_1 freewheels through D_1 and I_{L1} decays by the rate $-V_o/L_1$.

4) *Period 4 (t3-t4)*: The full operating cycle is completed by another

freewheeling period. The voltage V_T becomes zero and D_1 and D_2 are on simultaneously. $-V_o$ appears across L_2 causing its current to decrease and freewheel through D_2 while L_1 continues to freewheel as in period 3.

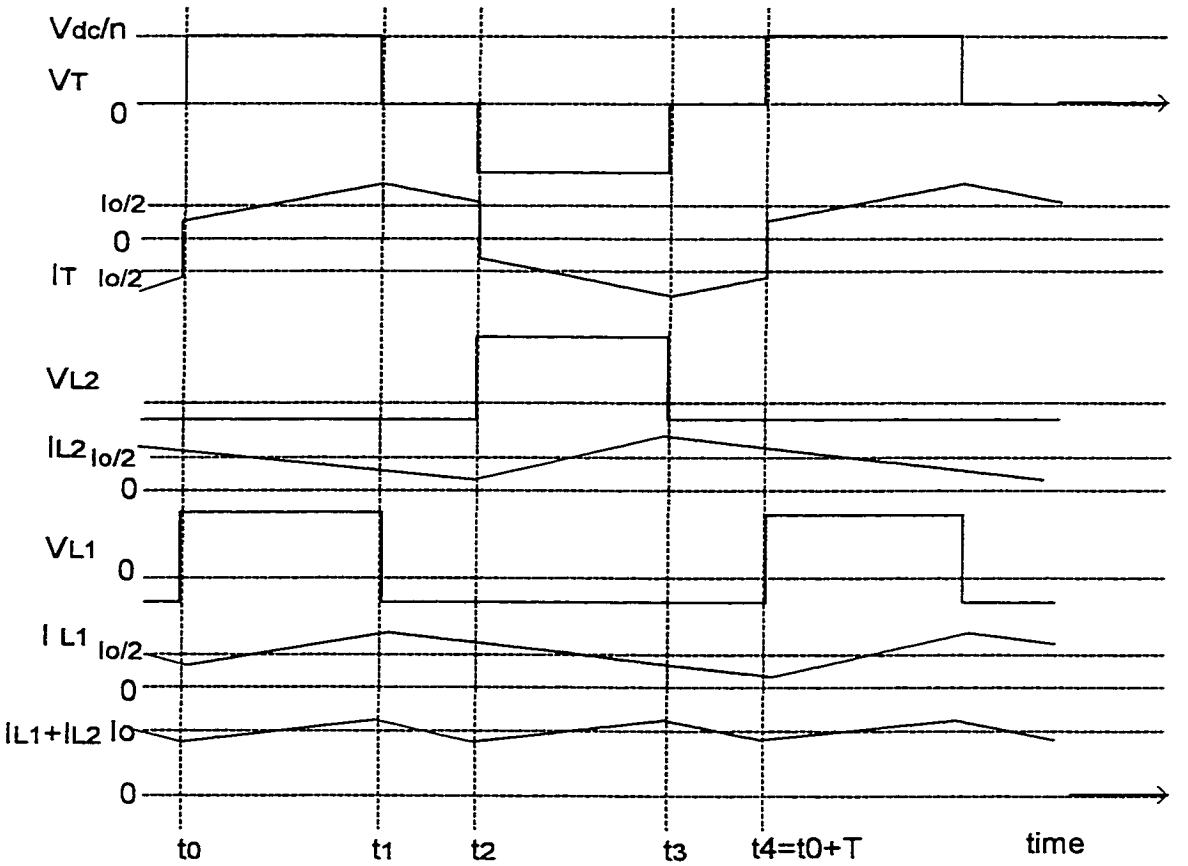


Fig. 5-11. Key operation waveforms of current doubler rectification topology.

5.3.2 Comparison Analysis

In order to obtain a direct comparison for merits and limitations for the above two rectification techniques when used in high power applications. A quantitative comparison is presented. Using a design procedure introduced in [68], assume that two converter are designed to meet the following major specifications:

- Target efficiency: 94.5%
- Input voltage: Vin=360V~400V
- Output voltage: Vo=44V~60V
- Rated and max output currents: 50A, 60A
- Rated output power: 2500 Watts (50V×50A)
- Max output power: 3500 Watts (60V×58.3A)
- Output voltage ripple limit: 200mVp-p
- ZVT range: 50%~100%
- Switching frequency: 100 kHz
- Primary controller: UC3879

Based on the simplified theoretical analysis, the key design parameters are compared in Table 5-1. For simplicity, the current values are not reflecting the effect of the AC components of the inductor currents. Comparison notes are listed below:

Note 1: The transformer core size (here area product) is roughly determined by:

$$area\_prouct = \frac{V_i I_{1rms} D}{K_u B_{\max} J_m f_s} \tag{5.1}$$

where, K_u: window factor

V_i: primary voltage

I_{1rms}: primary *rms* current

J_m: current density

B_{max}: max flux density

Note 2: Copper loss should be calculated by *rms* current value:

$$P_{cu} = \sum_{n} R_{eq,n} \times I_{rms,n}^{2} \tag{5.2}$$

Meanwhile, suppose that the winding loss in the primary and secondary side is designed to be almost balanced.

Note 3: The core losses of the inductors and transformer are approximately calculated as follows [86]:

1) For Ferrite materials

$$P_{core} = K_c f^{1.13} B_{pk}^{2.41} V_e \tag{5.3}$$

where, $B_{pk} = \dfrac{L\Delta I_L}{2A_e N}$

V_e: *rms* ac voltage (volts)

B_{pk}: peak ac flux density (gauss)

A_e: cross-sectional area (m^2)

N: number of turns

f: frequency (hertz)

ΔI_L: peak to peak value of inductor ripple current

2) For Kool-Mu material

$$P_{core} = f^{1.46} B_{pk}^{2.0} \tag{5.4}$$

where $B_{pk} = \dfrac{V_e 10^8}{4.44 A_e f}$, A_e: Cross-sectional area (cm^2)

3) for Powdered Iron

$$P_{core} = \frac{f}{\dfrac{a}{B_{pk}^{3}} + \dfrac{b}{B_{pk}^{2.3}} + \dfrac{c}{B_{pk}^{1.65}}} + (df^2 B_{pk}^{2}) \tag{5.5}$$

where coefficients a, b and vary with different materials [86]

Note 4: Suppose the inductor size (here area product) is approximately:

$$Area\_product = L\frac{I_{pk}I_{rms}}{K_u B_{\max} J_m} \tag{5.6}$$

Note 5: The comparison is conducted in terms of keeping the same switching frequency and the peak-peak value of voltage ripples. The efficiency of the current doubler rectification should be higher than that of the center-tapped structure rectification if the two filtering inductors are properly designed while using appropriate core material, otherwise, very high core loss caused by high ac peak current swing probably make the efficiency of the current doubler lower than expected one, because high ac peak current will cause greater core loss due to larger flux swing.

Summarizing the most important properties of the current doubler rectifier as revealed by the circuit configuration, operation mechanism and simplified analysis, the following advantages can be drawn:

- Simpler transformer structure;
- Improved window and copper utilization;
- Lower copper dissipation in secondary;
- Identical diode and capacitor stresses; and
- The same control strategy as center-tapped configuration.

The following arguments still exist while many merits are seen. The costs for the above two converters are comparable. The transformer of the current doubler configuration may be somewhat cheaper than that of center-tapped counterpart due to simpler structure. But the total price for two individual inductors is usually more expensive than single inductor used in the center-tapped structure.

Table 5-1 Comparison of center-tapped and current doubler rectifiers

Design parameters	Center-tapped		Current Doubler	
Transformer (Tr) Core Size[1]	EE55/21 ferrite		EE55/21 ferrite	
Switching frequency	100 kHz		100 kHz	
Tr Operating Frequency	100 kHz		100 kHz	
Tr Primary Windings	Lp		Lp	
Tr Primary Number of Turns	N		N	
Tr Secondary Windings	Ls1	Ls2	Ls	
Tr Secondary Number of Turns	1	1	2	
Tr Secondary winding resistance.	R	R	2R	
Tr Secondary average Current	25A (Io*0.5)	25A (Io*0.5)	25A (Io/2)	
Tr secondary-side *rms* current	~32A	~32A	Approximate 25A	
Current reflected to the primary	50*(1/N)*D		(50/2)*(2/N)*D	
Tr Winding Loss[2]	Ptr,cu		0.796Ptr,cu	
Tr core loss[3]	Ptr-core		Ptr-core	
Tr termination loss	High		Low	
Diode breakdown voltage	Vin*2/N		Vin*2/N	
Output Inductors	L1		L1	L2
Inductance of inductors	Assuming 14.5 uH		29 uH	29 uH
Inductor operating frequency	200 kHz		100 kHz	100kHz
Inductor current P-P value, ΔI	6A		12A	12A
Inductor current (DC average)	50A		25A	25A
Inductor current peak value	53		31A	31A
Inductor current *rms* value	50.1A		25.24A	25.24A
Inductor core loss[3]	Depending on core material			
Inductor winding loss[2]	Pwinding		>Pwinding	
Inductor Core Size (total)[4]	Ain		>2Ain if same material	
Output capacitor capacitance	3*3300 uF		3 *3300 uF	
Output capacitor ESR	25m or lower		25m or lower	
Voltage ripple magnitude	120mV		120mV	
Voltage ripple frequency	200 kHz		200 kHz	
Current ripple frequency	200 kHz		200 kHz	
Current ripple P-P value	6A		6A	
Relative cost	Baseline		A little higher	
Relative power density	Baseline		A little lower	
Relative efficiency[5]	Baseline		Potential higher	

In addition, the total inductor volume of the current doubler rectifier strongly depends on ripple limit where a larger inductance for each inductor is needed in order to keep the same magnitude output ripples, and also thermal constraint limits core material usage due to high core loss, but the transformer's size may be smaller than center-tapped

counterpart. Therefore, total magnetic volume is almost comparable for the two topologies. For particular applications, such as in a high power-density converter design, however, the current doubler rectifier offers the potential benefit of better distributed power dissipation. For instance, a part of intensive transformer loss could be transferred to two inductors and thus the same transformer can handle higher power.

5.3.3 Experimental Verifications

An experimental prototype of the converter using the ZVT-PS-FB topology has been built, as shown in Fig. 5-12. When used for the current doubler topology, two different inductors need to be connected to replace the on-board center-tapped filtering inductor. The pulse-width-modulation control chip, UC3879, is used to achieve ZVT closed-loop control. The magnetic cores with Kool-Mu material are used to make the two current-doubler inductors. Kool-Mu material has the comparable permeability as the powdered-iron material, but its cost is higher than the latter.

The primary-side operation of the prototyped converter at full load 53V@52A is demonstrated in Fig. 5-13. Figure 5-13(a) shows waveforms on the switch and (b) shows waveforms on the transformer. It is clear from the waveforms that the body diode is conducting before the gate signal comes. This means that the ZVT commutation is achieved for the main switches.

Figure 5-14 shows the interested operation waveforms of the current-doubler rectifier at the secondary-side. Note that practical individual inductance operating at full load (here 53V @ 52A) has only 20uH due to the effect of DC bias while the designed value is 29uH with using the Kool-Mu cores. The ripple current peak to peak value of the

two individual inductor currents is 17.5A, each, and the output current ripple before the output filter capacitor, i.e., the sum of two inductor current ripples, is reduced to 9.1A thanks to the cancellation of two inductor ripples. Figure 5-15 shows the secondary-side goes into the DCM operation when operating at very light load.

Figure 5-16 shows experimental efficiency comparison of the current doubler and center-tapped rectifiers implemented as a down converter of 3500W. Around rated power output, the efficiency of the current doubler is about 0.5% higher than that achieved by center-tapped rectifier. For 360V DC bus input, it seems that the advantage is more prominent than under 400V dc bus input.

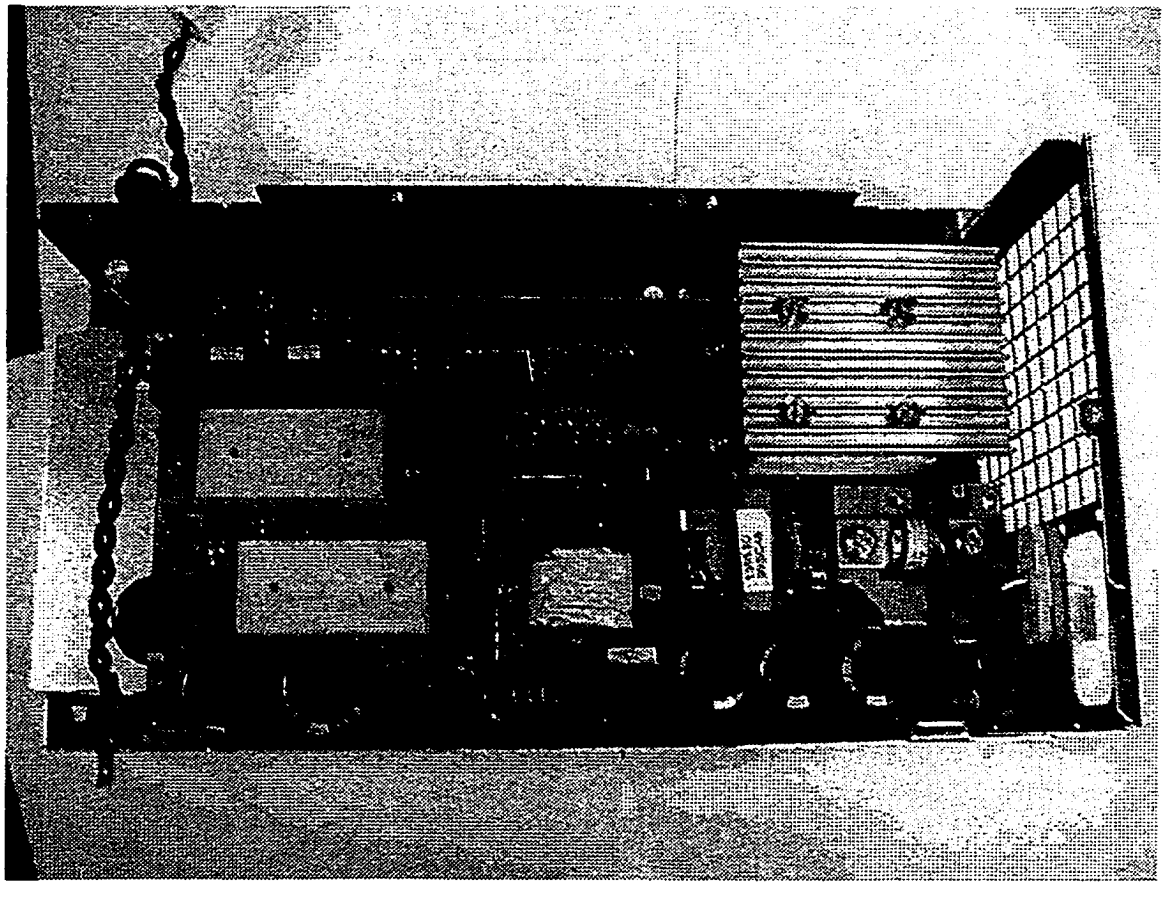
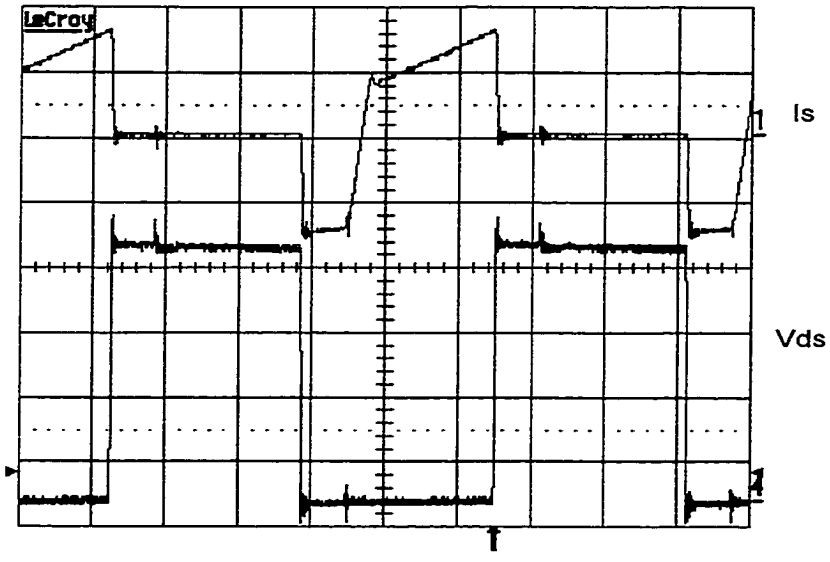
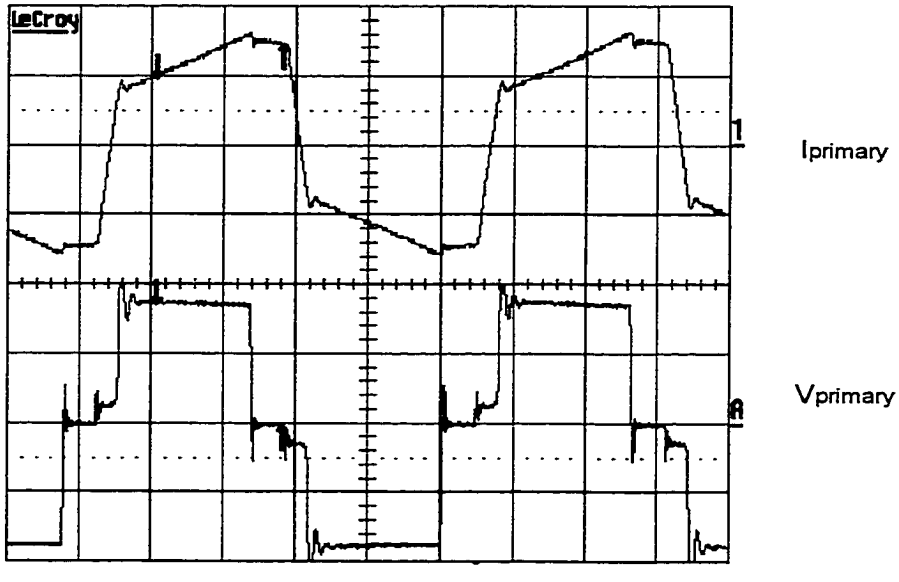


Fig. 5-12. Experimental prototype of a 3500W for comparing secondary-side topologies, using UC3879 as primary controller to realize ZVT.



(a)



(b)

Fig. 5-13. Operation waveforms at the primary-side (a) waveforms on the switch: positive and negative peak currents are 15.5A and 16.2A (10A/div); peak voltage 440V and DC bus voltage 400V (100V/div), f_s=95.272kHz (b) waveforms on the transformer at DC bus voltage 360V (upper trace:10A/div; lower trace: 400V/div).

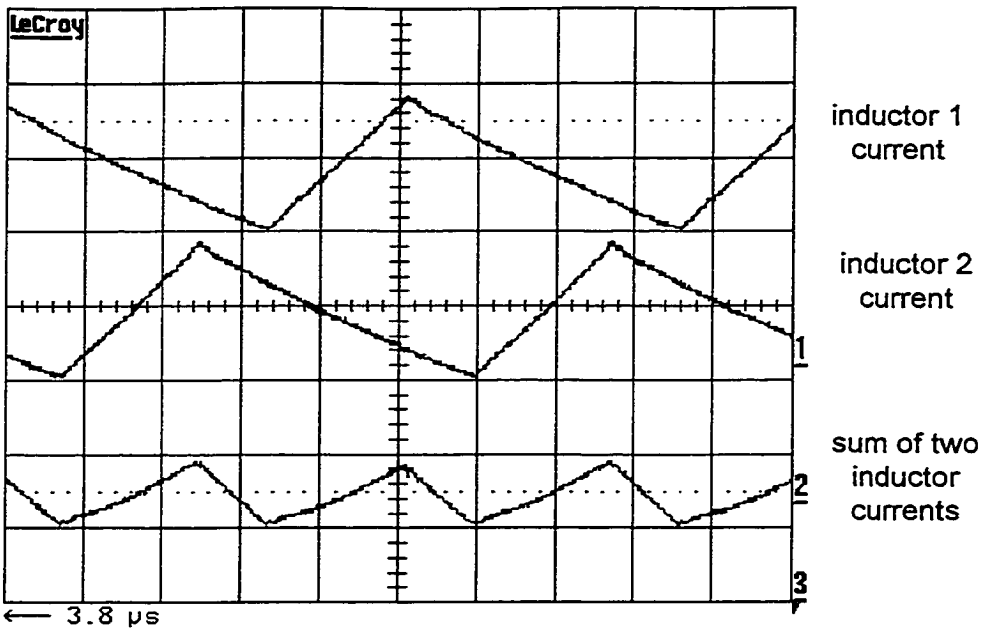


Fig. 5-14. Operation waveforms of secondary-side for current doubler at full load, current ripples $\Delta I_1=\Delta I_2=17.5A$, $\Delta I_o=9.1A$; 10A/div.

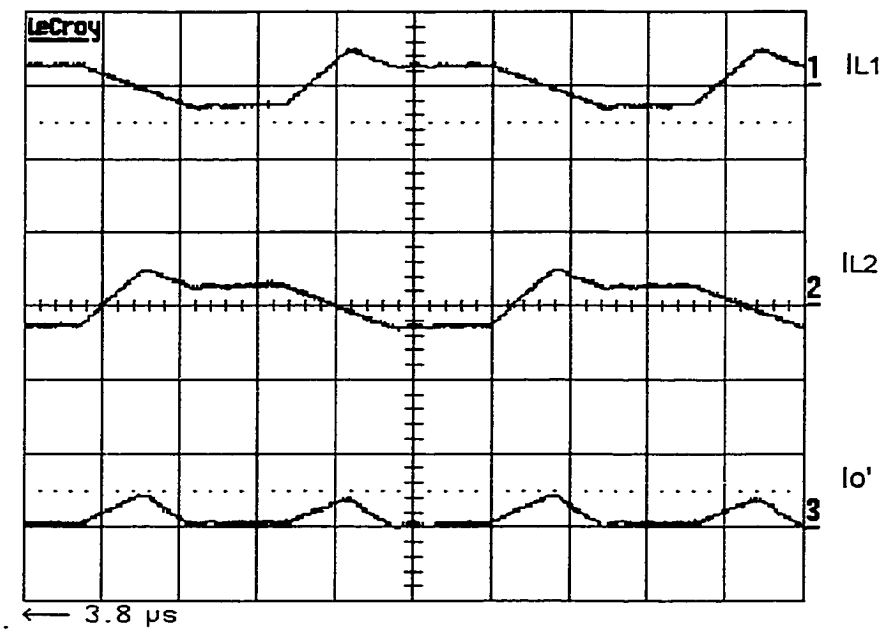
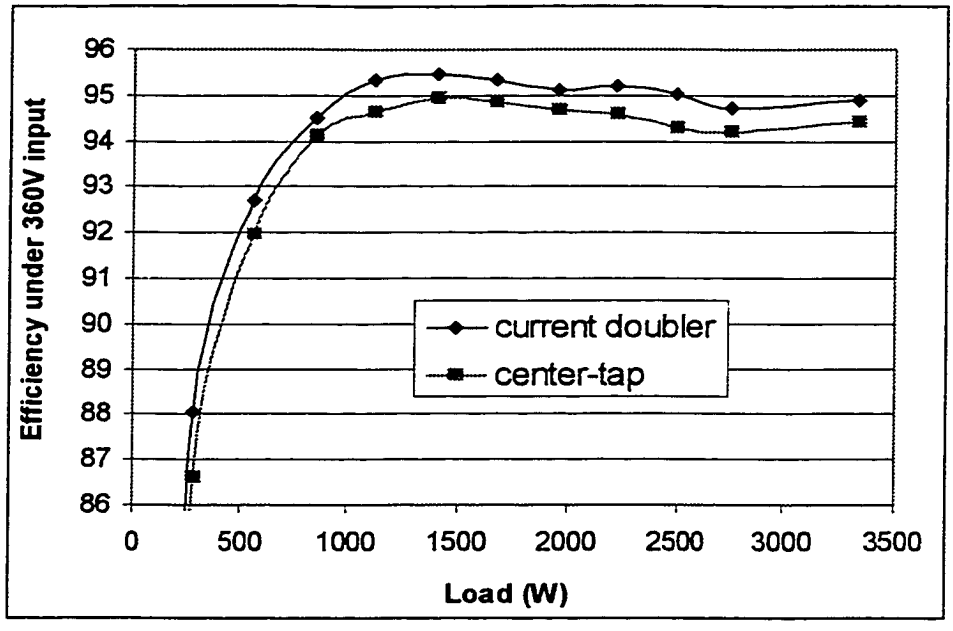
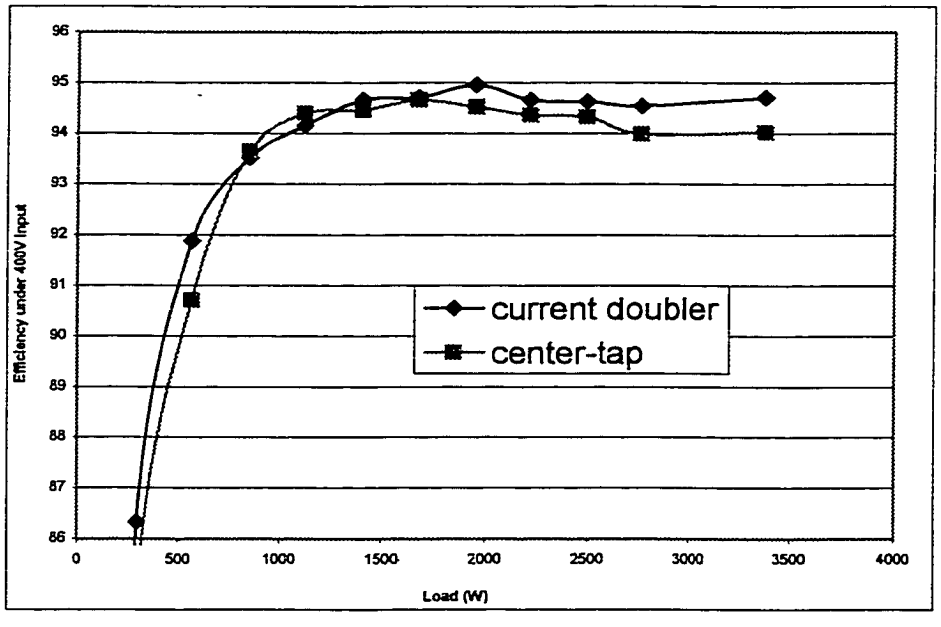


Fig 5-15. DCM operation of secondary-side for current doubler at light load, 53V @ 1A output, 10A/div.



(a)



(b)

Fig. 5-16. Experimental efficiency comparison (a) at 360V input, and (b) at 400V input.

5.4 Summary

In primary-side topologies for middle input voltage such as 400Vdc bus, the ZVT-PS-FB topology is deemed as the best choice. In the primary-side topologies under the high input voltage such as 800Vdc bus, the topologies #1 and #2 based on multilevel cells combination have relatively simple structure and low switch number. Also they do not have the problem of voltage sharing that appears on the converters based on capacitive clamping. The topologies #3, #4, #5 and #6, based on the association of converters, have higher magnetic volume than the structures based on multilevel cells association. This is because physically the topology usually needs two transformers. However, this is not a drawback when it applied into very high power where one power stage and one transformer cannot handle so high power.

For the secondary-side topologies, two fashionable rectifiers are investigated. Compared to center-tapped rectifier, the major properties of the current doubler rectifier can be summarized as follows:

- Simpler transformer structure;
- Improved window and copper utilization;
- Lower copper dissipation in secondary;
- Identical diode and capacitor stresses;
- The same control strategy as center-tapped configuration; and
- Potential higher efficiency.

It should be pointed out that in order to achieve higher efficiency while comparing current-doubler with center-tapped rectifier, a careful magnetics design should be taken into an overall design consideration. And though the current-doubler rectifier

has higher efficiency, the center-tapped counterpart may have somewhat benefits in terms of cost and power density.

In summary, regardless of primary-side or secondary-side topologies, desirable approach would vary depending on which criteria is deemed most critical, such as cost, size, or efficiency. It also varies depending on specific applications.

This work was supported in part by the grant from NSF.

6 SYSTEM INTEGRATION TECHNIQUE — INTERLEAVING

6.1 Introduction

System integration techniques cover very extensive research topics, such as interleaving techniques, paralleling, system simplifying, stacking, device integration, control integration and packaging integration, etc. System integration techniques can be used in "building blocks" to implement a wide range of power electronics circuits and systems.

Today's electronic systems become more and more sophisticated, and it is difficult for a single power converter or power supply to meet all system performance requirements. In particular, for a high power, high reliability and complex power system, system integration technology employing multiple power stages or multiple converters has gained rapid acceptance in recent years [47,48].

There are many benefits for using the interleaving technique in power conversion systems with either conventionally centralized power structure (single power stage) or distributed (parallel) power structure. Recently, the so-called "multiple-phase" (multiple-channel) interleaving technique has been developed and applied into power electronic systems [87-93]. However, it seems that conventional interleaving techniques are limited only to low power applications, in particular, for power supplies using single-ended topologies such as buck, forward, and flyback, and others. Actually, in low-power single-ended topology applications, the interleaving techniques have been well documented in

[87-93]. The above fact shows that proper interleaving methodology in high power applications need to be further developed and identified.

This chapter places an emphasis on interleaving technique of high power down converters where "secondary-side, double-frequency rectification" topologies are used. A novel interleaving method, known as quarter-cycle delay method in a two power stage case, is proposed. Comparative results using computer simulation for two power stages are given. The interleaving method can also be generalized for multiple power stage applications.

6.2 Conceptual Overview

Figure 6-1 shows a conceptual block diagram of power supply with interleaved power stage. The interleaved power stage, consisting of several individual power stages, is used as main power circuit of the power supply. The power supply share one controller, output filtering capacitor and/or output filtering inductor. Compared to power supply whose power stage simply consists of parallel-connected multiple power stages, there must be a specific phase shift (usually with stagger) for drive control signals among the power stages for interleaved power train.

Interleaved controller will employ phase-shift control technique to coordinate two power stages so that their individual input or/and output voltage ripples are out of phase and cancel each other. Actually, as for filters, switching ripple frequency has been doubled while still keeping the same switching frequency of active switch. Therefore, there are two options either keeping the original output inductor value of each module or decreasing the output capacitor to a value that maintain the required ripple or vise versa.

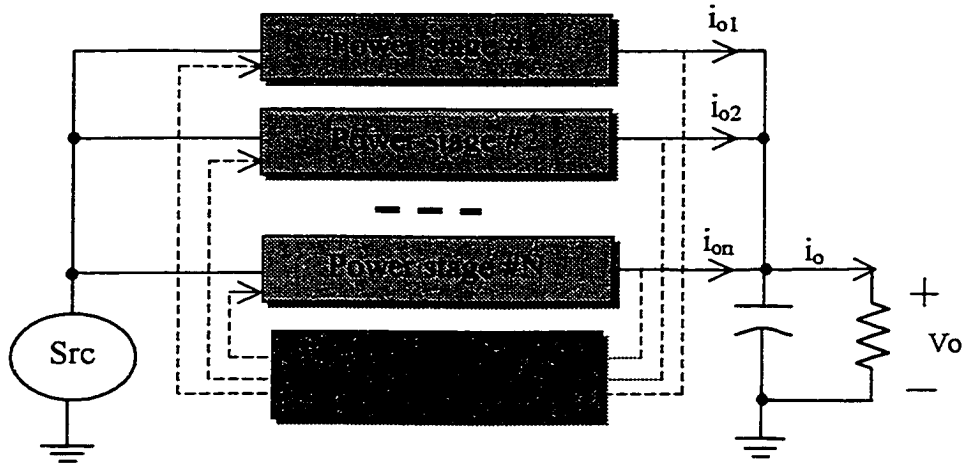


Fig. 6-1. Block diagram of power supply with interleaved power stages.

From the above discussion, interleaving might be a potential technique to increase the power density of power supply because it allows the reduction of the size of inductor and the EMI filter with increased ripple frequency. Additionally, input and output ripple currents dramatically cancel each other and result in a decreased output ripple peak-peak value. Further, thermal management is easily manipulated because thermal spark points are distributed with multiple power stages and switching devices. The effects of aggregation considerably reduce both acoustic noise (for other loads) and EMI.

The interleaving technique may also be potential technique to increase conversion efficiency because it allows lower frequency operation while keeping the same ripple and EMI filter size, due to ripple cancellation among power stages. The lower frequency operation provides a way to reduce switching loss and magnetic losses.

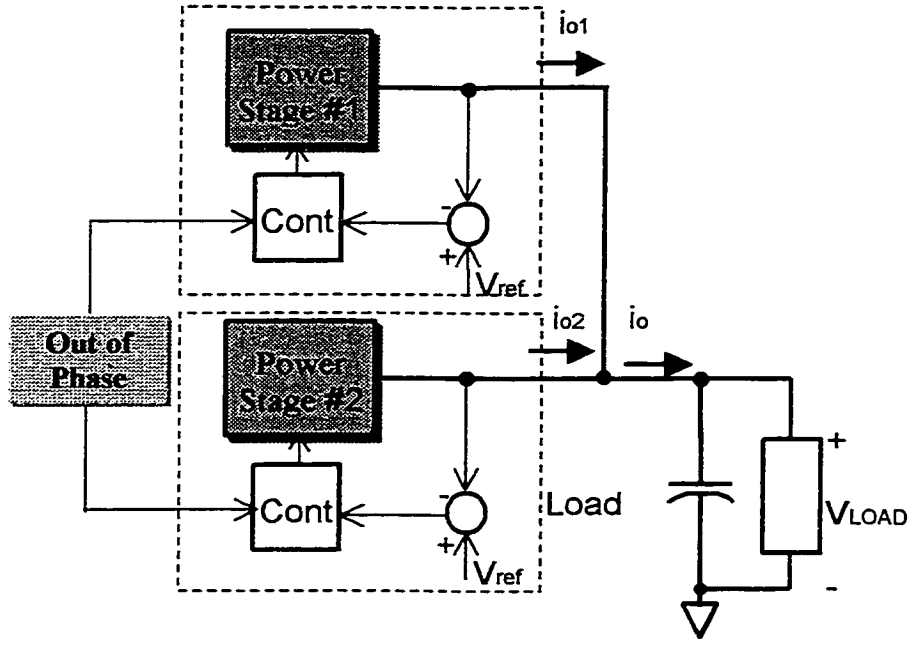
The major disadvantages of interleaving may be the use of more complicated control circuitry, power stage structure and PCB layout, as well as more component number and footprints. These potential disadvantages may make cost of interleaved converter higher than non-interleaved one, depending on repeated number of components

and overall cost account while considering thermal management and other system integration expense. It should be pointed out that we have to employ more than one power stage in higher power applications due to limited power handling capability with the single power stage. Especially, it is from the consideration of thermal management and commercially available power devices.

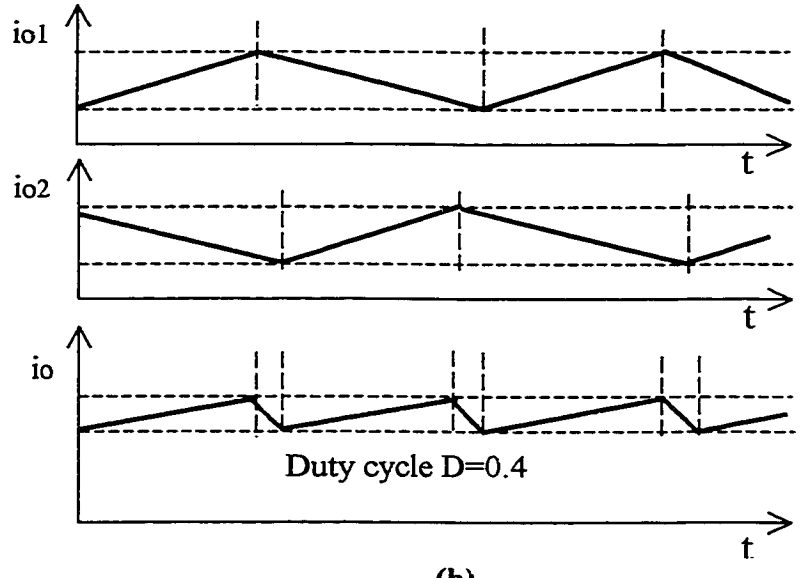
6.3 Limit of Conventional Interleaving Technique

Figure 6-2(a) shows an example of two power stages for implementing interleaving. Fig. 6-2(b) illustrates that best ripple cancellation could be achieved while control signals are made out of phase between two power stages. Moreover, it can be proved that the best ripple cancellation effect could be obtained when the phase shift of switch drive (control) signal for the second power stage is π over that of the first power stage [87]. Further, *for N power stage interleaving case, phase-shift of drive signals among power stages should be* $\frac{2\pi}{N}$

Power switches are turned on or off at the edges of a time clock. In these cases, the constant phase shift among the N modules to be interleaved can be obtained by the same amount of phase shift among their time clocks. A simple staggered clock generator can be constructed by using the standard CMOS ICs, such as NE555 and MC14018. For two interleaved power stages, there are many existing control ICs that can be used for interleaving purpose. These ICs may be any PWM controller with two output PWM signals keeping phase relationship out of phase, such as UC 3835, 3525, etc. For the cases more than two power stages, we may use mutiple-phase or mutiple-channel phase-stagger control ICs manufactured by companies TI, Intersil, etc.



(a)



(b)

Fig. 6-2. An example of interleaving implementation for two power stage case: (a) interleaved power stages, and (b) output ripple cancellation demonstration.

The traditional control strategy for interleaving is to implement phase shift $2\pi/N$ among N interleaved power stages such that the lowest magnitude of the total output ripple could be achieved. By analyzing the interleaving techniques described above and their implementation [88-93], we find that the above control strategy has the following limitations:

1) In order to obtain output ripple cancellation, topologies are required with characteristics that output ripple frequency of individual power stage at the secondary-side is the same as the switching frequency. Example topologies are forward, boost, Cuk, flyback, SEPIC, quasi-square-wave and two-switch forward.

2) In low power applications, especially for the applications where fast transient and relatively large output current is required, the so-called multiple phase or mutiple channel interleavingtechniques are used [4,91].

6.4 A Interleaving Method for High Power Topologies

In order to clearly state the application limit for the current interleaving techniques, it is necessary to reclassify topologies according to the relationship between switching frequency and output ripple frequency. The topologies, whose output ripple frequency is the same as the switching frequency, is referred to as secondary-side, same-frequency rectification topologies in this work; and the topologies, whose output ripple frequency is doubled as the switching frequency, is referred to as secondary-side, double-frequency rectification topologies in this dissertation.

Examples of secondary-side, same-frequency rectification topologies are conventional forward, boost, Cuk, flyback, SEPIC, quasi-square-wave and two-switch

forward circuits. The common feautres of this family of topologies are single-ended primary-side and single-ended, secondary-side topology structure, realtively simple circuit and control, being suited for low to medium power applications.

The secondary-side, double-frequency rectification topologies will be any combination consisting of one primary-side structure such as full bridge, push-pull or half-bridge and one secondary-side structure such as center-tapped, full-bridge or current-doubler rectifier. The common feautres of this family of topologies are their double-ended, primary-side and double-ended, secondary-side topology structure, realtively complex circuit and control, and being suited for medium to high power applications.

As for technical limitations of the conventional interleaving schemes described above, conceptually, *the conventional interleaving techniques are actually suitable only for the secondary-side, same-frequency rectification topologies*. Thus, the following questions are raised here:

1) Why don't researchers use interleaving techniques in the secondary-side, double-frequency rectification topologies?

2) What control strategy should be employed in order to achieve the equivalent ripple cancellation effect as the conventional interleaving method did?

3) How many benefits can we achieve if the interleaving technique is used in high power converters?

For the first question, possible answers may be given as follows:

1) It might be misunderstood that in order to get interleaved output effect, the duty-cycle should be less than 0.5; this is why interleaving technique is currently used

only for the secondary-side, same-frequency rectification topologies such as conventional forward and boost converters.

2) It might be confused by the fact that secondary-side, double-frequency rectification topologies have implied interleaved features, e.g., double-frequency output ripples, out of phase for ripple currents of individual branches, etc. Consequently, everyone think that it is not necessary to do interleaving again in those topologies.

3) No available controller IC is designed to implement interleaving for secondary-side, double-frequency rectification topologies.

As for as the second question, it can be proved that the benefits of ripple cancellation and ripple frequency-doubling effect provided by interleaving technique can be achieved in secondary-side, double-frequency rectification topologies if phase-shift of drive (control) signals among N power stages to be interleaved follows the following quantity relationship,

$$\frac{2\pi}{2N} = \frac{\pi}{N}$$

This relationship demonstrates that compared to the conventional control strategy, *phase-shift quantity among module control signals should be reduced by half over the conventional interleaving control strategy* (phase-shift 2π/N). This is because there has already been a two times relationship between output ripple frequency and switching frequency in secondary-side, double-frequency rectification topologies.

Typically, for the two-power stage case, a special *quarter-cycle phase-shift* between control signals is required, not previous half-cycle (180 degree) phase-shift. However, for currently available PWM controller ICs, such as UC 3525, and UC 3825,

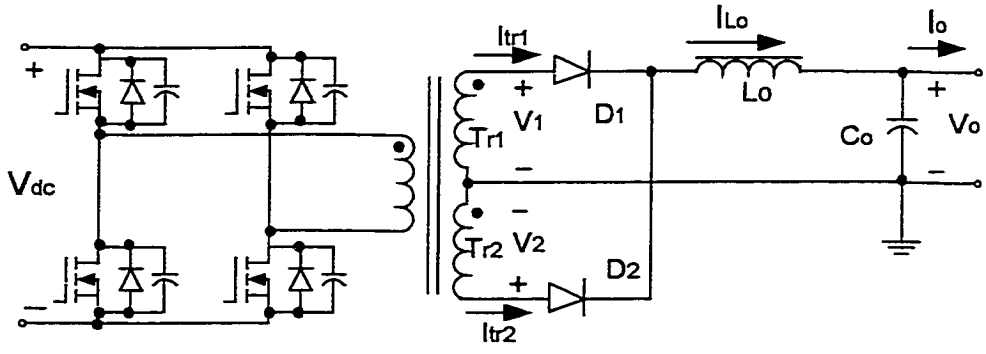
there is no such specific phase-shift function, namely, 90 degree phase-shift between two PWM output signals.

Ideally, it will be very easy to realize interleaving of high power topologies if the above phase-shift control strategy could be implemented into PWM control ICs (e.g. 3825, 3875, and 3895) by IC manufactures.

6.5 Comparison Analysis

For high power converter with given specifications, we can use either single power stage or interleaved power stages to implement power conversion, as shown in Fig. 6-3. Assume that the power converter are designed to meet the following major specifications:

- Target efficiency: 94%
- Input voltage: 360V~400V
- Output voltage: 44V~60V
- Rated output current: 100A
- Rated output power: 5300 Watts (53V×100A)
- Output voltage ripple limit: 200mVp-p
- ZVT range: 50%~100%
- Switching frequency: 100 kHz



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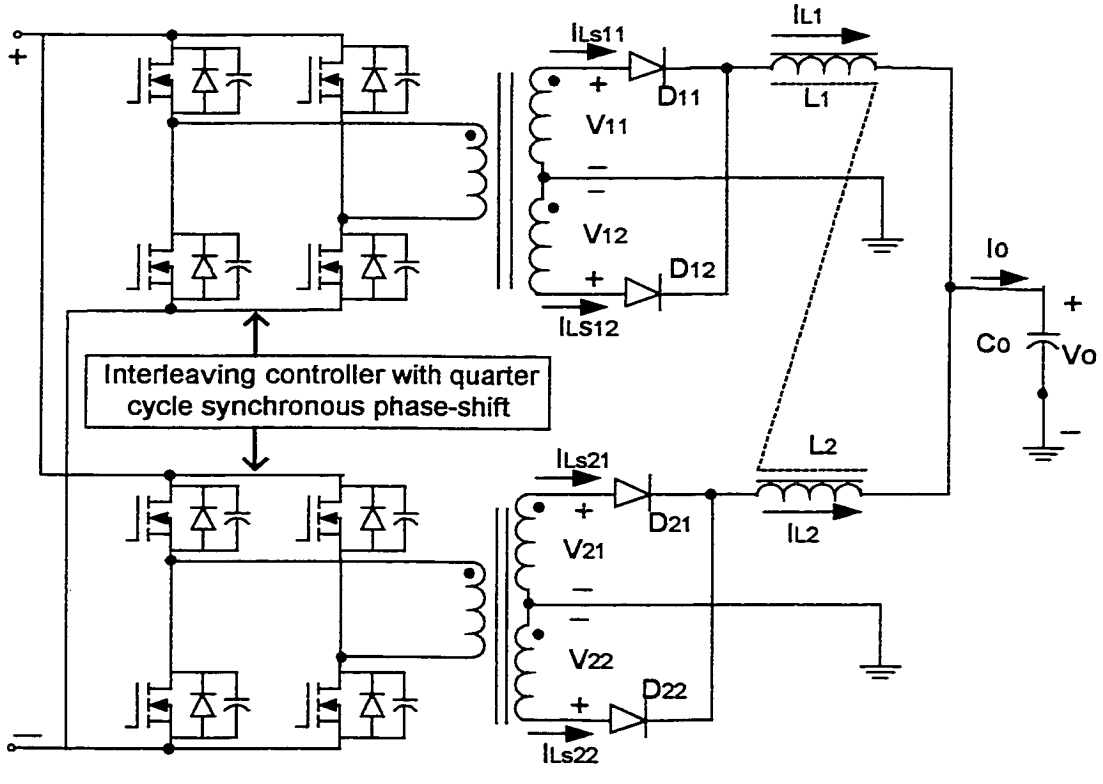


(b)

Fig. 6-3. Optional schematics to implement high power conversion: (a) single power stage, and (b) two-interleaved power stage.

Using similar analysis method in Section 5.3.2, based upon the simplified theoretical analysis from Eqs. (5.1)-(5.6), a quantitative comparison for designed parameters is presented in Table 6-1. For simplicity, the current values are not reflecting the effect of the AC components of the inductor currents. And though the two output inductors in interleaved power topology can be implemented through using coupled inductors, the indictors L_1 and L_2 in Table 6-1 are still regarded as two individual inductors with separate cores.

In Table 6-1, the comparison note 1 means that in order to obtain the same magnitude of output ripples, output filtering capacitance can be used smaller while keeping the same output filtering inductance and vice versa. The comparison note 2 means that ripple voltage cancellation rate is for the same filtering condition, i.e., the same inductance, capacitance and ESR of capacitors. 55% ripple cancellation rate is for full load (duty-cycle is about 0.7), the cancellation rate will be increased with reduced load, e.g., cancellation rate 62% at 70% load, and the rate 76% at 50% load. Theoretically, near 100% cancellation rate could be obtained at minimum load and under completely identical two power stages and controllers. Note 3 is from the point that EMI intensity strongly depends on the current ripple peak-peak value ΔI. The comparison note 4 means that this comparison item will strongly depends on the system power level and specific application.

Table 6-1 Comparison of single power stage and interleaved power stages

Structure	One power stage		Interleaved power stage			
Transformers (Tr)	T1		T1		T2	
Transformer (Tr) Core Size	2xEE55/21		EE55/21		EE55/21	
Switching Frequency	100 kHz		100 kHz			
Tr Operating Frequency	100 kHz		100 kHz			
Tr Primary Windings	Lp		LP1		Lp2	
Tr Primary Number of Turns	N		N		N	
Tr Secondary Windings	Ls1	Ls2	Ls11	Ls12	Ls21	Ls22
Tr Secondary Number of Turns	1	1	1	1	1	1
Tr Secondary winding res.	R	R	2R	2R	2R	2R
Tr Secondary average Current	50A	50A	25A	25A	25A	25A
Tr secondary-side rms current	65A	65A	33A	33A	33A	33A
Current reflected to the primary	100*(1/N)*D		2*50*(1/N)*D			
Tr Winding Loss	Ptr,cu		Ptr,cu			
Tr core loss	Ptr-core		Ptr-core			
Tr termination loss	Medium		Large			
Diode breakdown voltage	Vin*2/N		Vin*2/N			
Output Inductors	L1		L1		L2	
Inductance of inductors[1]	14.5 uH		14.5 uH		14.5 uH	
Inductor operating frequency	200 kHz		200 kHz		200 kHz	
Inductor current P-P value, ΔI	5.3A		5.8A		5.8A	
Inductor current (DC average)	100A		50A		50A	
Inductor current peak	102.65A		52.9A		52.9A	
Inductor current rms value	100.012A		50.028		50.028	
Inductor core loss	2Pcore		Pcore			
Inductor winding loss	Pwinding		<Pwinding			
Inductor Core Size (total)	2Ae,in		Ae,in			
Output capacitor capacitance	6 X 3300 uF		3 X 3300 uF (half)			
Output capacitor ESR estimated	25m		50m			
Voltage ripple P-P value	Same (128mV)		Same (126mV)			
Voltage ripple frequency	200 kHz		400 kHz			
Current ripple P-P value, ΔI	5.3A		2.7A (half)			
Current ripple frequency	200 kHz		400 kHz			
Ripple cancellation rate[2]	N/A		55%			
EMI intensity[3]	Baseline		Relatively low			
EMI filter size	Baseline		Relatively small			
Controller complexity	Simple		Complex			
Mosfets Number	Same		Same			
Circuitry layout	Simple		Complex			
Thermal management	Difficult		Easy			
Relative power density[4]	Baseline		A little higher			
Relative efficiency	Baseline		Comparable			
Relative cost	Baseline[3]		A little higher			

6.6 Simulated Results

Figure 6-4 shows simulated schematics based on the simulation platform OrCAD–Schematics 9.2. Main circuit parameters are: V_{in}=400V, primary resonant inductor L_r=4uH for single power stage and 8uH for each interleaved power stage, turns ratio of transformer n=4.5, and switching frequency f_s=100kHz, and output filtering inductor L_1=L_2=14.5uH and filtering capacitor C_o=3×3300uF for one power stage and 3300uF for interleaved power stage. In order to achieve faster simulation speed, output capacitance is selected smaller than the designed one.

Figure 6-5 shows interested simulation waveforms for the case with one power stage. From upper to lower traces, they are output voltage, output current and primary-side current of transformer. Figure 6-6 shows simulated waveforms of using interleaved power stage but implementing conventional interleaving control strategy, namely, phase-shift is made 180 degree. The results are the same as that of two simply parallel power stages and no benefit is obtained. Meanwhile, it is seen that the output ripples up to 562 mV are not acceptable. Figure 6-7 shows simulated results with new interleaving method, namely quarter-cycle phase-shift between drive signals of two power stages. The ripple magnitude is decreased by four times lower than conventional interleaving method under the same filter size, and also the ripple frequency is doubled. Fig. 6-8 gives simulated comparison for new interleaving method and conventional one under 50% load operation. Ripple magnitude is decreased to about 1/7th of that for conventional interleaving method under the same filter size, and also ripple frequency is doubled.

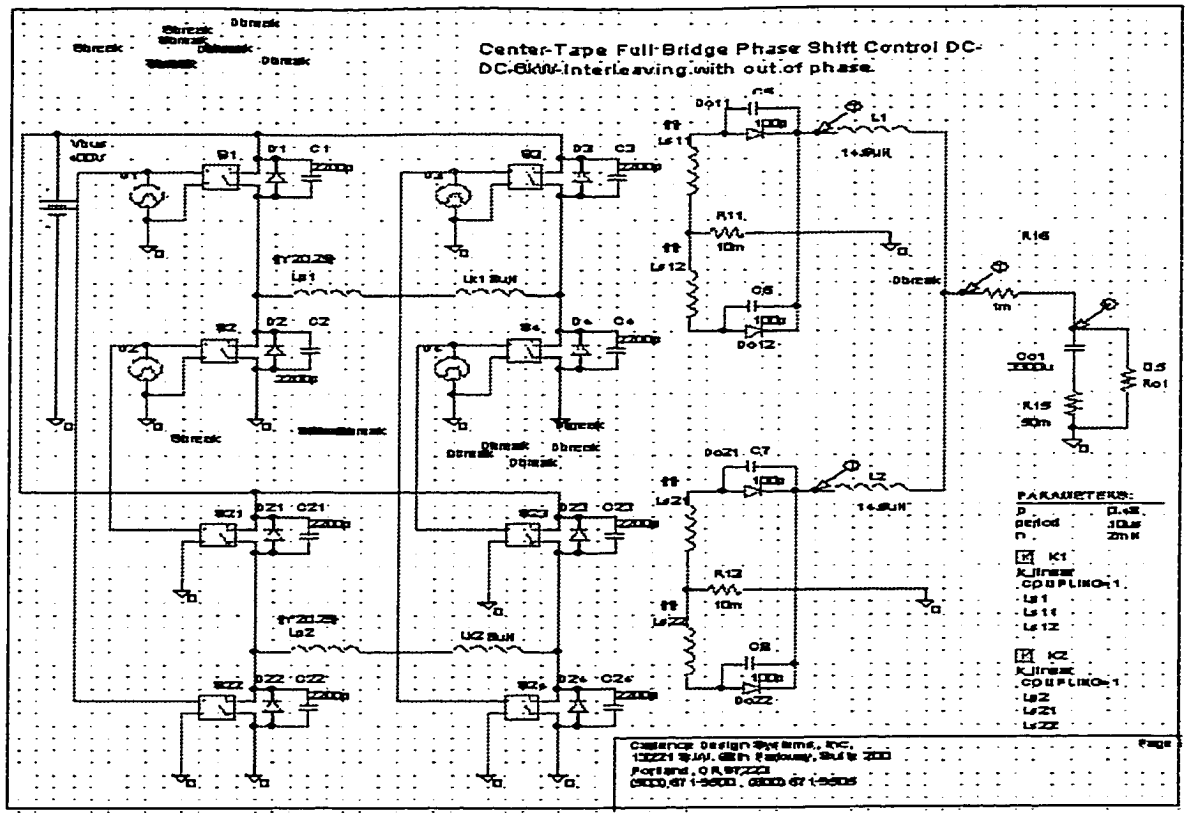


Fig. 6-4. Simulated schematics for interleaving power stage.

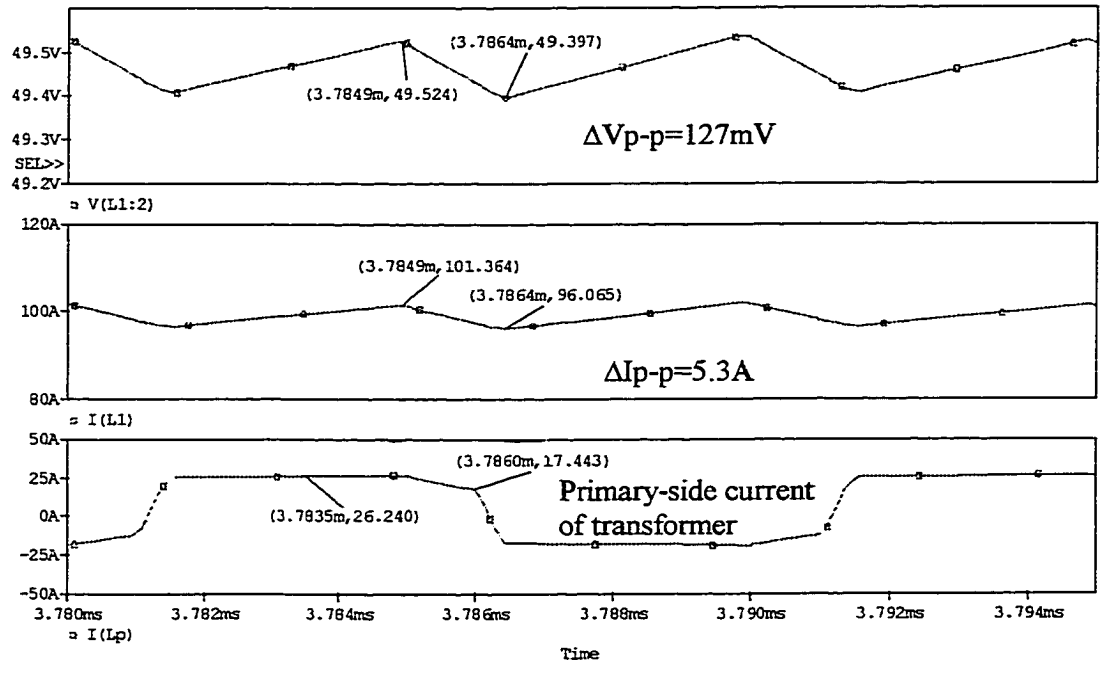


Fig. 6-5. Simulation waveforms for one power stage case.

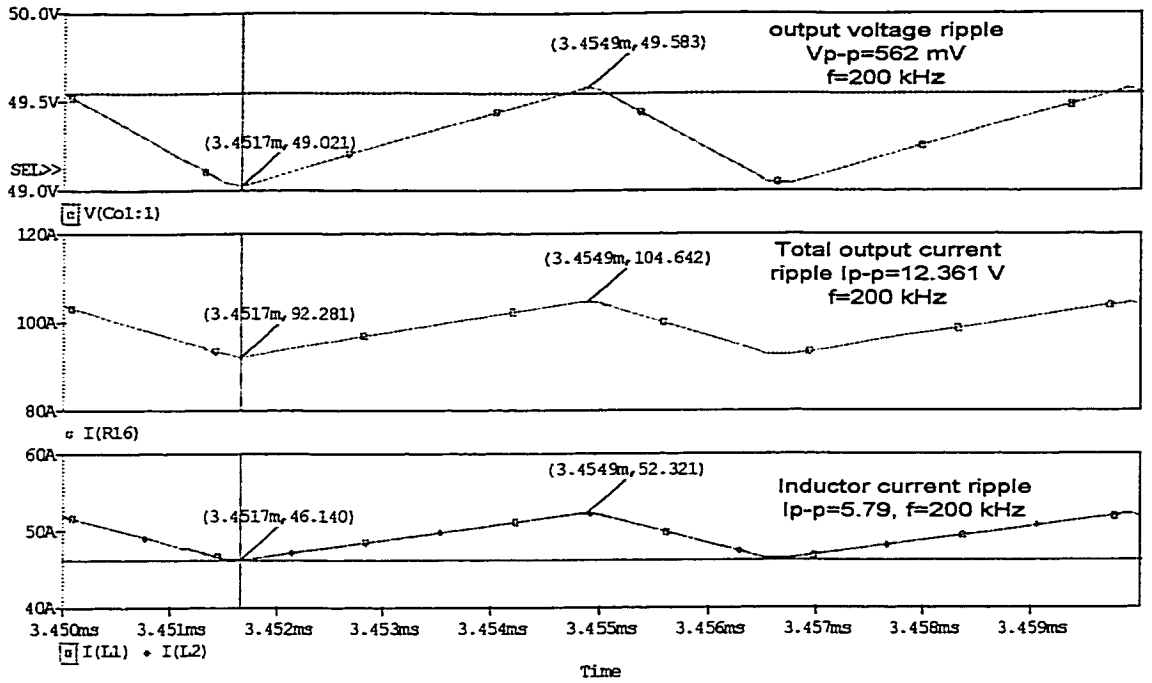


Fig. 6-6. Simulated waveforms of interleaved power stage implementation but using conventional interleaving control strategy.

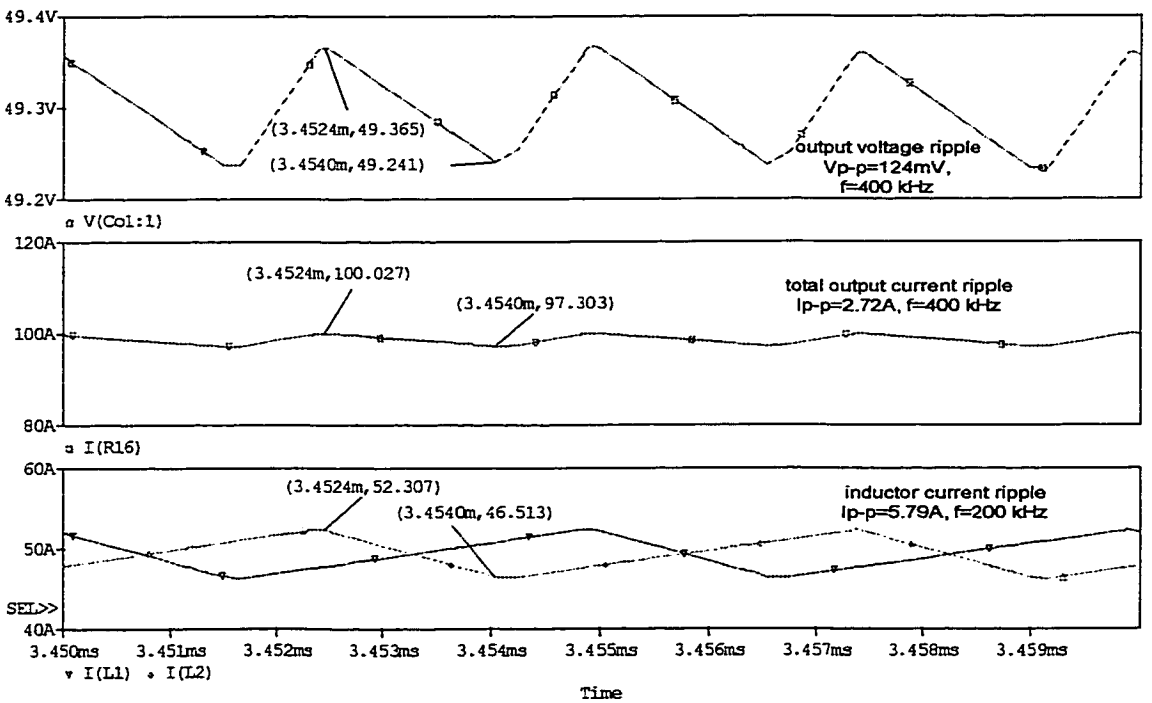
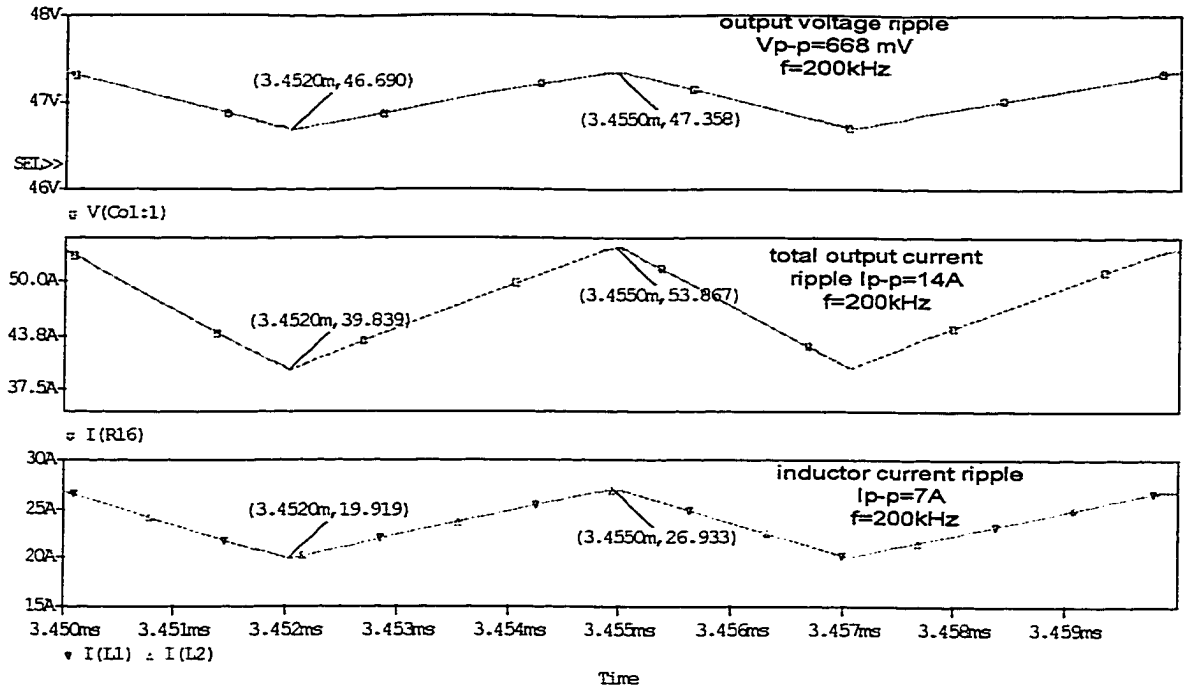


Fig. 6-7. Simulated results with new interleaving method.



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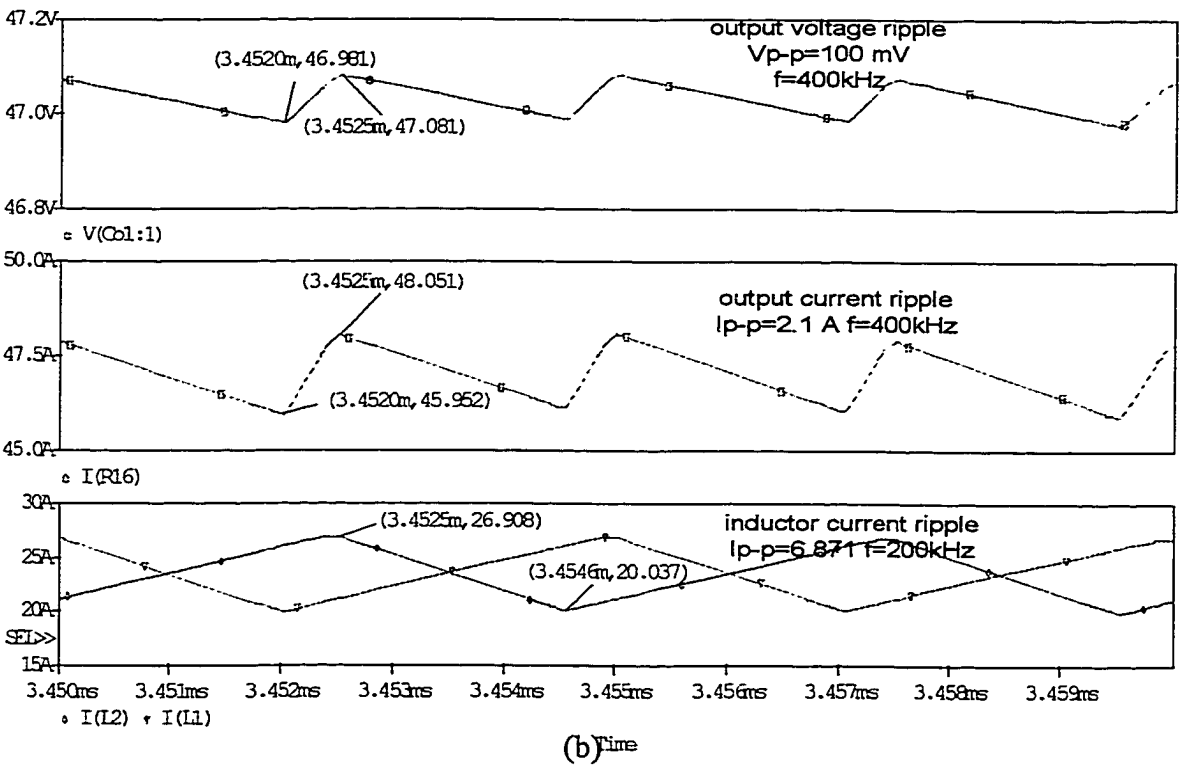


(b)

Fig. 6-8. Simulated comparison for different phase-shift strategy under 50% load operation: (a) conventional interleaving method, and (b) new interleaving method.

From the above simulation analysis, the following conclusions could be drawn:

1) Desirable performance of interleaving approach may vary with different operation condition, but still acceptable.

2) Almost the same effect of ripple cancellation can still be obtained while duty-cycle nears one, e.g. 0.9.

3) The better ripple cancellation effect can be achieved with decreased duty-cycle.

6.7 Summary

According to the frequency relationship between switching frequency and output ripple frequency, topologies are reclassified into secondary-side, same-frequency rectification topologies and secondary-side, double-frequency rectification topologies. It was found that the conventional interleaving technique is actually suitable only for the secondary-side, same-frequency rectification topologies. For secondary-side, double-frequency rectification topologies, phase-shift quantity among module control signals should be reduced to π/N. Typically, for the two-power stage case, a special quarter-cycle phase-shift between control signals is required, not previous half-cycle (180 degree) phase-shift.

Compared to non-interleaved converter under the same operating mode. Advantages and disadvantages of interleaved converters with secondary-side, double-frequency rectification topologies can be summarized as follows:

Advantages:

1) The frequency of total output ripples can be N times the frequency of individual power stage output ripples.

2) Output ripples can dramatically cancel each other to certain degree by the phase shift control strategy.

3) Ripples and EMI filters can be made smaller while keeping the same net ripple amplitude and EMI specifications.

4) Improved transient response due to using smaller output filters.

5) Obtain higher power level rectifier through interleaving multiple power stages based on existing rectifiers. Redundancy can be achieved by N+1 power stages structure.

6) Product development period could be shortened through modular design techniques.

Disadvantages:

1) More complicated power stage structure and printed-circuit-board (PCB) layout.

2) More complicated control circuits.

3) More component number and footprints.

4) Potential high cost.

7 SYSTEM INTEGRATION TECHNIQUE— PARALLELING

7.1 Introduction

As mentioned earlier, today's electronic systems become more and more sophisticated. In many of advanced application cases, it is difficult for a single power converter or power supply to meet all system performance requirements. In particular, for a high power, high reliability and complex power system, system integration technology employing multiple power stages or multiple converters have gained rapid acceptance in recent years [47,48]. In order to achieve desirable characteristics when operating converter modules in paralleling, a variety of approaches, with different complexities and current-sharing performances, have been proposed, developed, and analyzed in the recent past [94-150]. However, a comprehensive comparison of these methods is not presented in the open literature.

A classification and comparative evaluation of various paralleling methods is presented in this chapter. Emphasis is placed on discussion and assessment of the merits and limitations of the schemes, especially for active current-sharing methods. Finally, some of simulation results for a two-paralleled buck converter system are given.

7.2 Conceptual Overview

Generally, the paralleling of power converter modules offers a number of advantages over a single, high-power, centralized power supply. Paralleling of

standardized converter modules is an effect approach that is widely used in distributed power systems for both front-end and load converters.

An important characteristic of parallel operation is the possibility of configuring a redundancy system using more modules than the minimum required by the load. Usually $(m+r)$ modules are used, where m is the minimum number of modules required delivering the load power and r is the number of redundant units (usually 1) which gives the system the ability to tolerate failures without impact. Redundancy is desirable in many high reliability applications. A properly designed parallel configuration allows the on-line replacement (hot-swapping) of defective modules. This provides the means for non-interrupting maintenance and repair. In this way, the system reliability will be increased largely.

In addition, paralleling reduces electrical and thermal stress on semiconductor devices. In addition, higher switching frequency of parallel converters results in a higher control bandwidth, and so a parallel system can respond more quickly to abnormal and damaging system conditions, such as short circuits and overloads.

Figure 7-1 shows block diagram of a multiple converters system. It shows that paralleling can be used not only in front-end converters but also in load converters. For both applications current sharing (load sharing) is one of most important techniques in paralleling systems.

A desirable characteristic of a parallel supply system is that the individual converters share the load current equally and stably. Parallel modules are usually non-identical due to finite tolerances in the power stage and control parameters. If special provisions are not made to distribute the load current equally among paralleling supplies,

then it is possible that one or more units might deliver an excessive load current. This results in greater thermal stresses on specific units and a reduction in the system reliability [108,112 113 121,132,133,134,136].

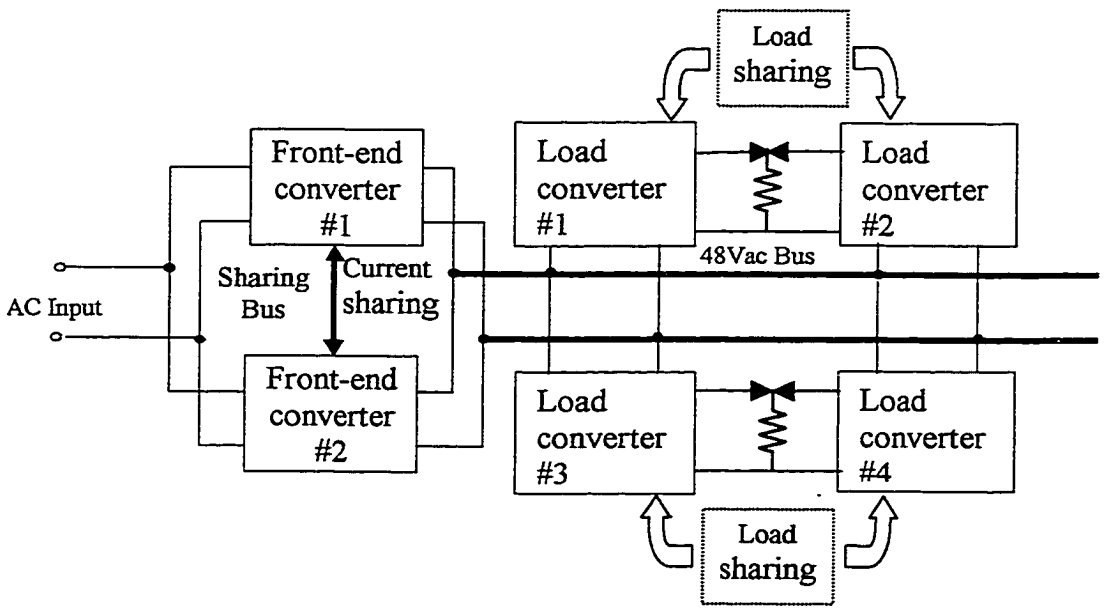


Fig. 7-1. Block diagram of a multiple converter system.

7.3 Classification of Paralleling Schemes

In this chapter, paralleling methods are classified into two basic categories from the viewpoint of the operating mechanism to current (or load) sharing, i.e., droop methods and active current (load) sharing methods. Figure 7-2 shows the classification of paralleling schemes. Based on how to get droop features, the droop methods can be further categorized into five types of conducting schemes. For active current-sharing methods, actually, *a conducting scheme consists of a specific control structure and a current-programming method.* There are three basic control structures from the viewpoint of current sharing control strategy, namely, inner loop regulation, outer loop regulation

and external controller structures. Also there are a number of current-programming schemes among the paralleled modules. Therefore, there are more than ten active current-sharing schemes composed of the control structures and the current-programming schemes.

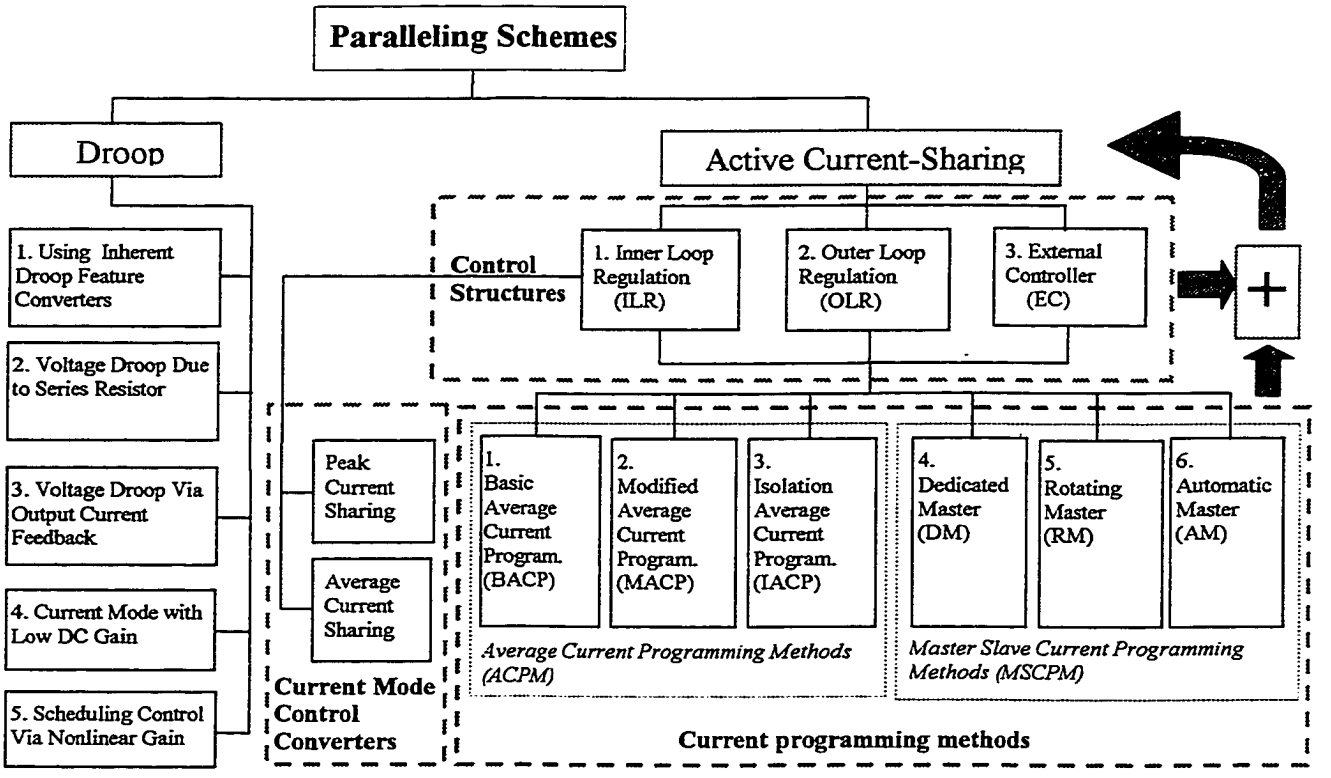


Fig. 7-2. Classification diagram for paralleling methods.

Table 7-1 shows some of active current-sharing schemes formed by three control structures and six current-programming methods. Of these schemes, in particular, ones with shadow sign are potential new schemes. (AM+OLR) scheme is employed by control chip UC 3907. Moreover, (BACP+ILR) and (BACP+OLR) schemes are also used extensively in practical parallel system (see detailed description in later section). It should be pointed out that converters employing peak and average current controls under

common outer loop have inherent peak and average current-sharing capability. Here we regard them as a special branch only under inner loop regulation structure, thus not to be included in Table 7-1.

Table 7-1
Combined active current-sharing schemes

Paralleling schemes		Current-programming methods					
		BACP	MACP	IACP	DM	RM	AM
Control structures	ILR	BACP + ILR	MACP + ILR	IACP + ILR	DM + ILR	RM + ILR	AM + ILR
	OLR	BACP + OLR	MACP + OLR	IACP + OLR	DM + OLR	RM + OLR	AM + OLR
	EC	BACP + EC	MACP + EC	IACP + EC	DM + EC	RM + EC	

7.4 Assessment of Paralleling Schemes

There are a number of schemes to parallel power supply modules. These schemes are described and discussed here, with an attempt made to investigate their principles, origins and applications, highlighting their merits and limitations.

7.4.1 Droop Schemes

A droop method can be defined as one in which the output voltage droops as the load current is increased. Its operating mechanism is to program output impedance to achieve current sharing among converters. Generally speaking, the better current sharing, the worse voltage regulation for the converters, so the reason conventional power supplies do not share current well is that they are designed to be good voltage sources

with a low output resistance. In other words, a converter's current-sharing ability can be determined by studying its output plane characteristic, i.e., the graph of the converter's output current versus output voltage.

This family of schemes needs no wire interconnections among control circuits of parallel converters, and so it is actually an open loop technique that individually programs the output impedance of each power supply. This dissertation presents five possible droop schemes that can be used to parallel power supplies or power converters.

Scheme #1 Using Converters with Inherent Droop Feature

A simple scheme to set up a parallel system is to properly choose converter modules with a droop feature. Some converters, such as the buck, boost converters operating in discontinuous inductor current mode, series resonant converter, etc, all under open loop, have inherent load-sharing ability, and probably be used in a paralleling system without tight regulation requirements [94,113].

Scheme #2 Voltage Droop Due to Series Resistor

In this paralleling scheme, all of the paralleled supplies have an initial setting that, via a potentiometer, are made almost identical. A resistor is placed in series with the output to provide an IR voltage drop in the output [110,120].

Obviously, the major disadvantage of this approach is the high power dissapation in the series resistor if the droop in output voltage is large. Because of added power dissipation, this scheme is normally used only for low power linear post-regulators.

Scheme #3 Voltage Droop via Output Current Feedback

In this method a voltage is sensed across a series resistor and amplified and used to produce a droop in the output voltage that is proportional to the output current of the

supply [110]. A block diagram is shown in Fig. 7-3. The output droop property can be expressed approximately as:

$$V_o = V_{initial} - I_o \times R_{droop} \tag{7.1}$$

where R_{droop} is referred to as the equivalent series droop resistor and is approximately equal to $H_i(R_1+R_2)/R_2$, and $V_{initial}$ represents the equivalent initial value of output voltage and is approximately equal to $V_{ref}(R_1+R_2)/R_2$.

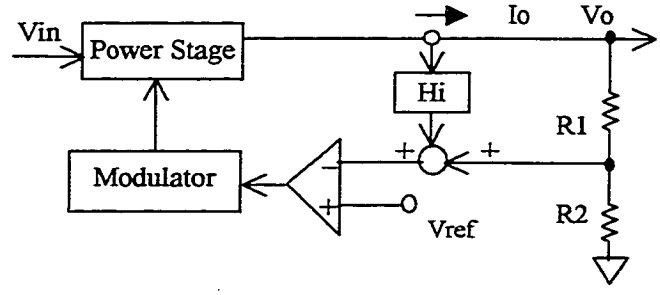


Fig. 7-3. Voltage droop via output current feedback.

Scheme **#4** Current Mode with Low DC Gain

This droop scheme is implemented by eliminating the series capacitor (DC isolation capacitor) in the feedback path of the error amplifier of a current-mode supply, namely, canceling the integrator in the transfer function. This greatly reduces the DC gain of the error amplifier, thus producing a droop in the output voltage. Otherwise, the differences between the reference voltages and the feedback voltage will be amplified sufficiently to cause a severe imbalance in the output current level of converter modules.

A block diagram of the scheme is shown in Fig. 7-4. The output droop property can be expressed approximately as:

$$V_o = V_{initial} - I_o \times \frac{R_1}{R_f} \times H_i \tag{7.2}$$

where H_i is the gain of the current sense circuit, and $V_{initial}$ represents the equivalent initial value of output voltage and is approximately equal to $V_{ref}(1+R_1/R_2+R_1/R_f)$.

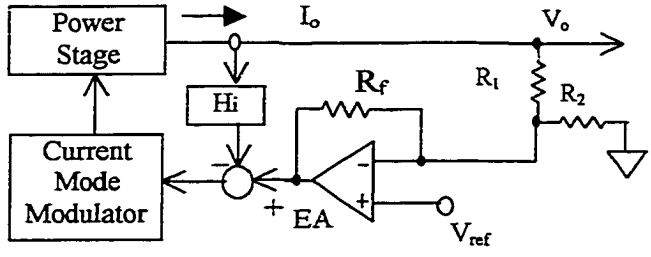


Fig. 7-4. Current mode with low DC gain.

Scheme #5 Scheduling Control Via Nonlinear Gain

This droop scheme is implemented by Nonlinear Gain scheduling, and a block diagram of the scheme is shown in Fig. 7-5. The total control gain $K=K_1\times K_2$, the higher the DC gain, K, the worse the current-sharing becomes, the better load regulation becomes. Thus, good current-sharing in required operating range can be scheduled and ensured, particularly in case of heavy load. In addition, this scheme is suitable for digital implementation, such as fuzzy control etc.

The five droop schemes mentioned are described only at the conceptual level. For more details of the output droop characteristics of paralleling DC/DC converter systems, refer to [110,112,113,115,120,126,138].

General features of the droop schemes are summarized as follows:

Advantages:

- easy to implement and expand paralleling system;
- no wire connection among control circuits of converters; and

• high modularity and reliability.

Disadvantages:

• degrading Load regulation to achieve droop characteristics; and

• poor current-sharing due to open loop for parallel system.

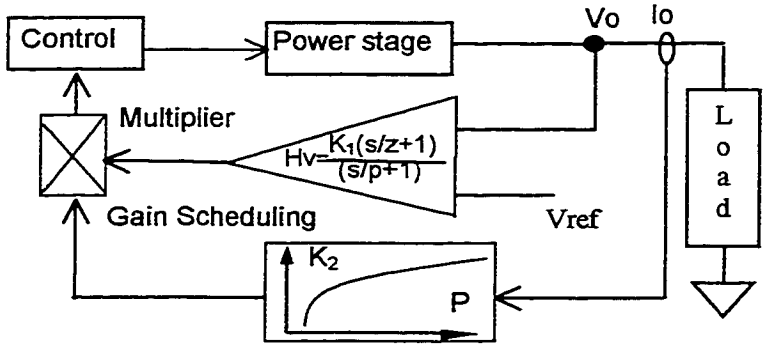


Fig.7-5. Scheduling control via nonlinear gain.

7.4.2 Active Current-Sharing Schemes

It is highlighted again that an active current sharing scheme here means a combination of a specific control structure and a current-programming scheme. Three control structures and six current-programming schemes are analyzed and discussed below. Their merits and limitations are reviewed.

Actually, as for single converter, it can be deemed that there is an additional adding control loop with active current-sharing control scheme, we refer it to as current-sharing control loop in this dissertation.

1) Control Structures for A Paralleling System

According to the operating mechanism of current-sharing in parallel converters, three basic control structures for the unbalanced sharing currents of converters in parallel are shown below, and their merits and limitations are noted.

Structure #1 Inner Loop Regulation (ILR)

This control structure implies that reference voltage, voltage feedback and compensator are common. A typical structure of this scheme is shown in Fig. 7-6 where G(s) is the transfer function of voltage error compensator, and Z_{c1},···and Z_{cn} represent cable impedance. Error signals (V_{se1} and V_{sen}) from a current-programming controller are used to adjust the output of the voltage loop compensator to obtain the appropriate operating control voltage V_{ci}, where $i = 1,2\cdots n$, which feeds the PWM generator of each converter in order to produce the desired current-sharing.

For peak and average current mode control converters under this sharing control structure, the current sharing can be achieved by providing the same control reference for the internal current loop of each module. For the peak current control, pulse-by-pulse peak current sharing can be obtained by the use of a fast-acting current loop even in the case of the mismatch in power stage parameters and no use of current-programming.

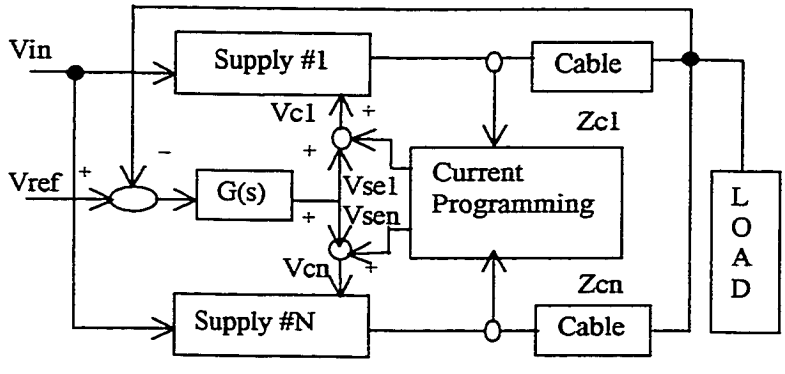


Fig. 7-6. A typical block diagram of inner loop regulation structure.

Merits and limitations of this control structure are summarized as follows:

Merits:

- stable current-sharing; and
- precise output voltage regulation.

As a result, output currents of the converters in parallel are in tight control with the fixed outer voltage loop, i.e., sharing error signals do not pass through the voltage loop compensator. Thus it is possible that the overall system response may be more stable and faster than that obtained with outer loop regulation (described in the next section).

Limitations:

- degrades the modularity of the system; and
- poor fault-tolerance.

Each module can't operate as an individual converter because they have the outer voltage loop in common. Consequently, the fault-tolerant capability for a paralleling system is relatively poor.

Structure #2 Outer Loop Regulation (OLR)

This structure uses current-programming error to adjust the reference or feedback terminal of the outer voltage loop until equal load current distribution is achieved. The concept of this control structure is graphically presented in Fig. 7-7. The key features of the structure are that reference voltage, output voltage feedback, and the voltage compensator of each converter module is independent, respectively.

The advantages and disadvandages of the sharing control structure are summarized as follows:

Advantages:

- good modularity and standardization for manufacturing;
- flexibility in system configuration, easy to expand and maintain the system; and

• excellent fault-tolerance against the failure of any single module.

Disadvantages:

• possibly unstable in transient [111,141].

For example, the output voltage of a parallel system may become unstable when reference voltages are adjusted by a set of variation (uncertain) sharing error signals.

• limited voltage-feedback gain.

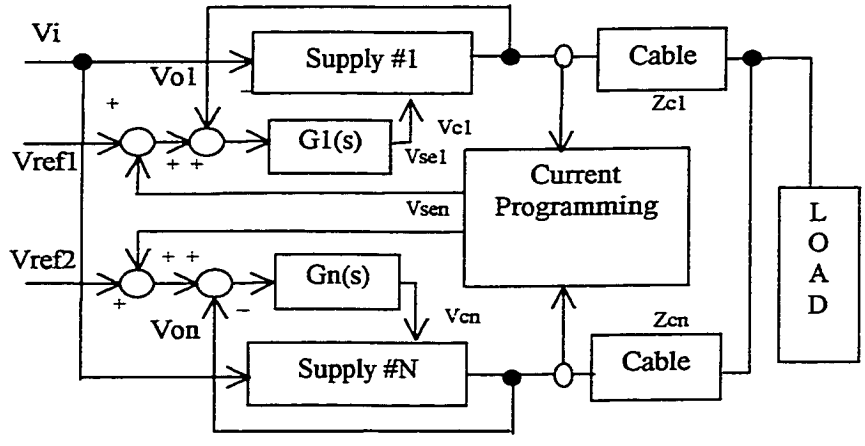


Fig. 7-7. A typical block diagram of outer loop regulation structure.

The infinite dc gain of the error amplifier sufficiently amplifies any finite mismatch between the voltage references of converter modules (unavoidable in practice) to cause a severe imbalance in the current level of converter modules. To avoid such a problem, the voltage feedback compensation must have a finite dc gain.

Structure #3 External Controller (EC)

Another alternative structure is to use an external controller to perform the current-sharing [108,124,130]. This is achieved by comparing all load sharing signals from the individual power units and adjusting the corresponding feedback control signal

to balance the load currents. A typical block diagram of this structure is shown in Fig. 7-8.

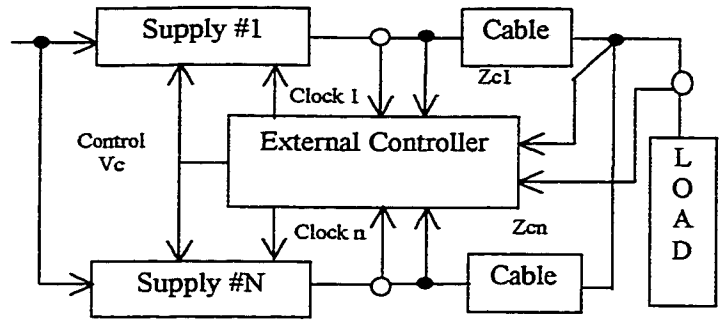


Fig. 7-8. A typical block diagram of external controller structure.

This system performs well but requires an additional controller and multiple connections among the contoller and each supply. In addition, a controller coordinates all converters, and so system reliability would be affected to a certain extent. Once the controller shuts down, the current-sharing situation no longer exists. Also, it may have a severe impact on overall system reliability due to the large number of interconnections and the increased possibility of single-point failure mode. Because of these reasons, this scheme might have been temporarily discarded in favor of one of active current-sharing techniques. However, in today's rapid development of distributed power systems, this technique should perhaps be examined in a new light [94].

Merits and limitations of this control structure are summarized as follows:

Merits:

- easy to implement active interleaving.

The control module can simultaneously provide control voltages and clock signals for each module of the paralleling system. Phased clocks can dramatically cut ripples.

- good current sharing and output voltage regulation;

- easy to implement failure monitoring capability; and
- good chance to fully utilize existing supervision system.

It may be possible to use a redundant high-level supervisory controller, leaving the individual cells to only manage gating and fault handling. This control mode can probably attain the highest performance because of the possibility of active interleaving.

Disadvantages:

- more interconnections among modules and external controller;
- degradation of modularity degree; and
- degradation of reliability due to more interconnections and a complicated control.

2) Current-Programming Schemes

Current-programming (CP) is an important link in an active current sharing scheme. The functions of the current-programming are to communicate control circuits of all paralleled converters, to acquire the current sharing error signal of each module, and then to feed the control circuit of each module by an adjustment amplifier.

Figure 7-9 shows a unified simplified block diagram that describes current-programming of *n* converters in parallel, which shows how the current reference signal, i_{refi}, is generated. $P_1(s)$, P_2,···, $P_n(s)$ represent transfer fuctions of adjustment amplifiers, μ_1,···and μ_n represent interface links of modules to a common sharing bus. The weighting functions, $W_1(s)$, $W_2(s)$···, $W_i(s)$ create the reference current signal in proportion to the desired current-sharing ratios. The differences between desired current levels, i_{refi}, and actual output current, i_{oi}, constitute the current error signal, i_{ei}. The desired output current level for each converter is the total current weighted by a function proportional to the

desired current-sharing ratio. Therefore, the dc summation of the weighting functions, $W_1(0)$ +··· +$W_2(0)$, shown in Fig. 7-9, is equal to unity. Also, Fig. 7-9 is suitable for signal processing for paralleling system with different rating power modules.

Unless otherwise stated, the following description is for paralleling of identical capacity power supplies or power converters.

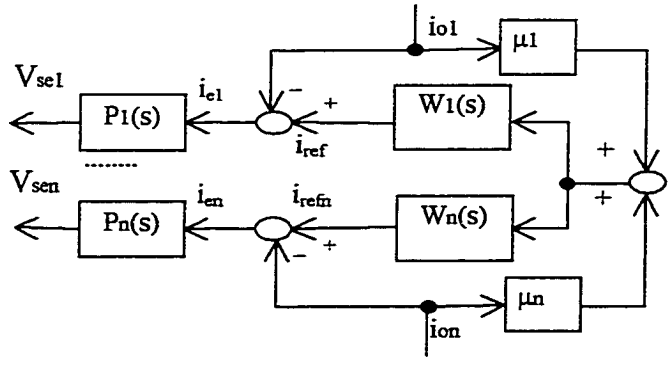


Fig. 7-9. A unified block diagram for current-programming.

a) Average Current-Programming Methods (ACPM)

In Fig. 7-9, when the functions μ_1 through μ_n are equal to one and the weight function $W_i(s)$ is gain in proportional to current rating of each converter in parallel system, we have the "average current-programming method". All converters provide signals proportional to their output currents, which are then weighted and averaged to get a sharing-current reference, i_{ref}, proportional to the average converter outpt current. In each converter, for example converter n, the reference i_{refn} is compared to the output current i_{on} of that converter to get a sharing-current error. This error is processed through the adjustment amplifier $P_n(s)$; the product $P_n(s)(i_{refn} - i_{on})$ is used in sharing control to adjust output voltage of converter n so that its output current is made approximately equal

to the weighted average the output current. All converters are maintained at "approximately" equal output current for the parallel system of identical capacity converter modules.

Scheme #1 Basic Average Current-Programming (BACP)

A typical implementation of the scheme is a patented technique, where each power module's current monitor drives a commonly shared bus via a resistor [109]. The scheme is called basic BACP in this paper, as shown in Fig. 7-10. The adjusting amplifier will sense if there is a differential across the resistor, equating to a load current imbalance, and adjust the control loop of the converters accordingly. The sharing bus where all resistors connect represents the average load current contribution. More detailed information can be found in [102,103,106,109,111,114,116,141,142,144].

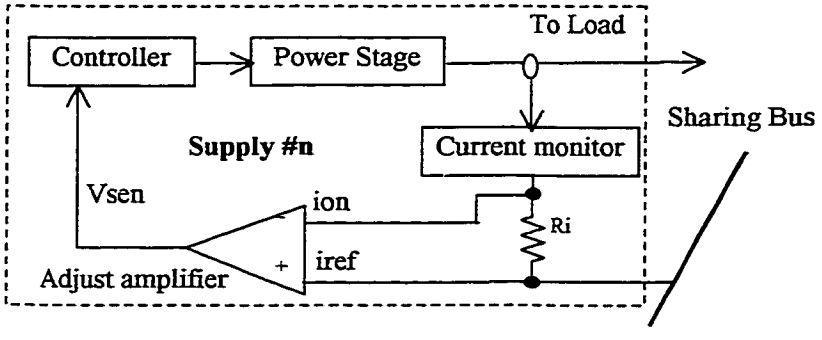


Fig. 7-10. A typical example for basic BACP.

Scheme#2 Modified Average Current-Programming (MACP)

A modified scheme is presented in [100], which does not employ the operational amplifier to generate the current-sharing error. The advantage of this modified scheme is its inherent stability. The main disadvantages mentioned above, however, also can be found in this scheme. Moreover, obvious poor transient response and additional ripples due to mismatching of the R, C parameters, may result in specific application problems.

Scheme #3 Isolation Average Current-Programming (IACP)

Based on the idea of ACPM, an isolation ACP is presented, which is called "frequency-based current-sharing technique" [96]. It employs the frequency domain method for encoding and communicating current-sharing information to implement galvanic isolation of current-sharing control circuits.

This scheme has significant advantages over existing methods, in particular, in eliminating the galvanic interconnections among module controllers. Thus, single point failure problem can be expected to be resolved by this new scheme, so it can be used wherever fault tolerance and high reliability are important to system requirements. Practical implementation and features of the scheme are presented in [96,98,104]. A potential problem of this scheme is high cost due to using a complicated circuit and techniques. In other words, this evolved scheme is still in the early development stage; more evaluation and practical design considerations need to be further explored in the future.

BACP is still dominant and is used widely in many practical field applications in the three schemes mentioned above. The advantages and disadvantages of the BACP are summarized below:

Advantages:

- relative stable and precise current sharing;
- single interconnection sharing bus; and
- noise immunity sharing control.

As compared below with the master/slave method, low frequency noise does not cause sharing control failure in this method.

Disadvantages:

- relatively poor reliability; and
- poor fault-tolerance.

While this scheme performs accurate current sharing, it can result in specific application problems. An example is when a supply runs into a current limit, causing the sharing bus to be loaded down and the output voltage to regulate to the lower adjusting limit. A similar failure mode will exist if any unit on the sharing bus is inoperative. Moreover, it is difficult to make weighted factor $W_n(s)$ change automatically; otherwise, high-cost, complicated control circuits have to be used.

b) Master Slave Current-Programming Methods (MSCPM)

Methods of current-programming with the master-slave concept can fall into three schemes according to the approaches of producing the master module, i.e., dedicated master, rotating master and automatic master, also called "democratic" master. The operating principle of MSCPM is similar to the ACPM except the current reference i_{ref} in Fig. 7-9 is simply one proportional to the master module output current.

Scheme #4 Dedicated Master (DM)

In Fig. 7-9, when one of μ_1 through μ_n is assigned to be one, and the others are zero as well as all $W_i(s)=1$, we get the block diagram of the dedicated master sharing scheme. That is to say, one module is dedicated to be the master; its output current will become the reference for current-sharing (CS) loops of the remaining modules (slaves).

The scheme does provide current sharing and can achieve stable output voltage regulation, but does not achieve redundancy, since the master failure disables the entire

system. Some analysis and discussions are described in references [97,117,121,124,129,141].

Scheme #5 Rotating Master (RM)

In Fig. 7-9, when any one of μ_1 through μ_n becomes one in turn and the other conditions are same as the dedicated master, we have the block diagram of this scheme.

The idea of the rotating master is proposed in reference [128]; it is indeed an advance compared with the dedicated master in the idea of enhancing system reliability. In this scheme, each module has the capability and chance of becoming a master according to specific control logic.

While this scheme improves system reliability, some specific application problems may occur. One possibility is that output voltage might fluctuate because of the continuous exchange of the master module. Another practical problem, obviously, is complicated implementation.

Scheme #6 Automatic Master (AM)

In Fig. 7-9, when μ_1 through μ_n become an ideal unidirectional rectifier, we get the block diagram of the automatic master. A typical implementation of this scheme is shown in Fig. 7-11. This scheme automatically selects a module with the highest output current to be the master, and adjusts accordingly control signals in a certain control mode to correct the imbalance of load current. This scheme is similar to the BACP scheme (Fig. 7-10) except that the resistor is replaced with an idea diode.

This scheme incorporates some advantages of the average current method and the dedicated master scheme, and so is an improvement over the former two schemes, which is also known as the "democratic current sharing" method in some literature.

In the above mentioned three master-slave schemes, the automatic master method gained popularity among power supply designers and is used widely in practical applications; in particular it is implemented in ICs UC3907 and UC3902 by Unitrode Inc. [94-97],105,108,111]. Features of the scheme are summarized as follow:

Merits:

- single interconnection sharing bus;
- good fault-tolerance; and
- easy to expand and modify paralleling system

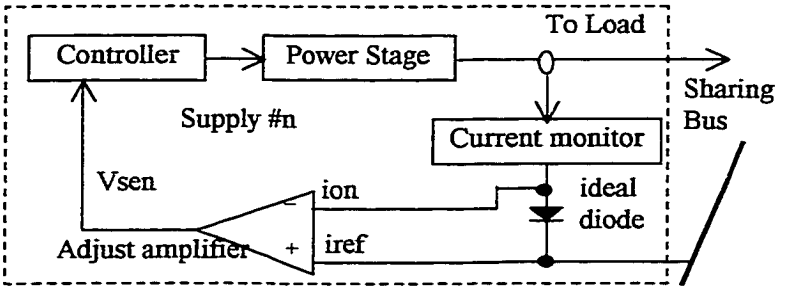


Fig. 7-11. A typical implementation of automatic master scheme.

Limitations:

- poor transient sharing performances.
- possible sharing control failure.
- noise sensitive sharing control.

7.5 Simulation Examples of New Paralleling Methods

The schematic used for simulation is shown in Fig. 7-12. The Saber simulation platform on workstation is used to simulate several typical cases. The simulated output voltage and currents are shown in Figs. 7-13(a) and 7-13(b), respectively. Figure 7-13(a)

shows excessive output voltage transients due to a step load change while the output is being regulated. From Fig. 7-13(b), we see that the output currents diverge to significantly different values due to the different equivalent resistances of inductors and cables in two converters, R_{L1}=0.01Ω and R_{L1}=0.09Ω.

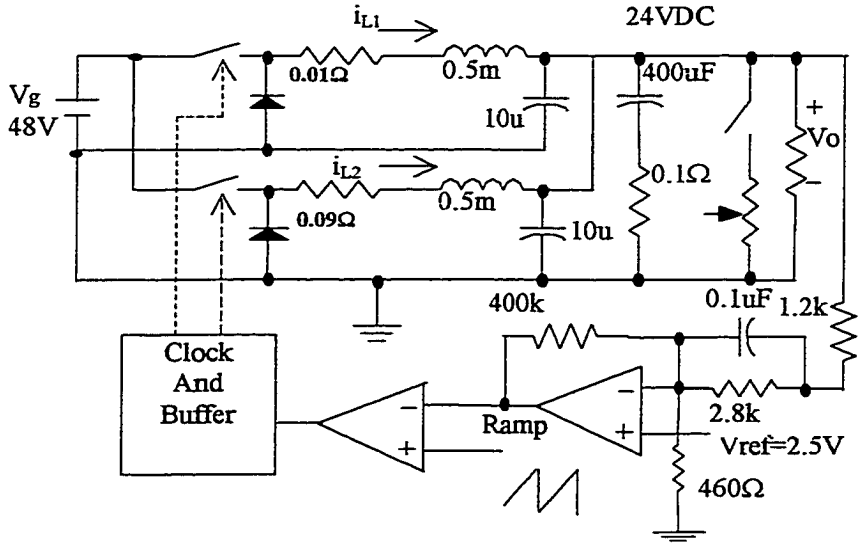


Fig. 7-12. Controller and power circuit used in simulation for two parallel-connected buck. converters under single-loop control.

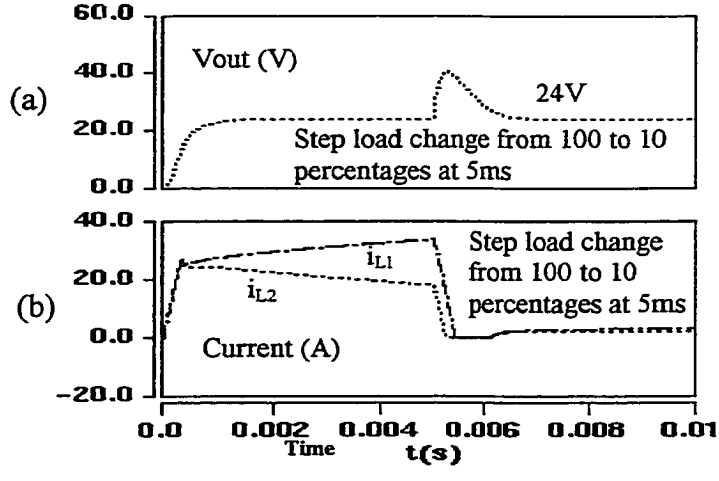


Fig. 7-13. Simulated results without sharing control: (a) Output voltage, and (b) Output currents of two buck converters under no current-sharing control (Step-load change at t=5ms).

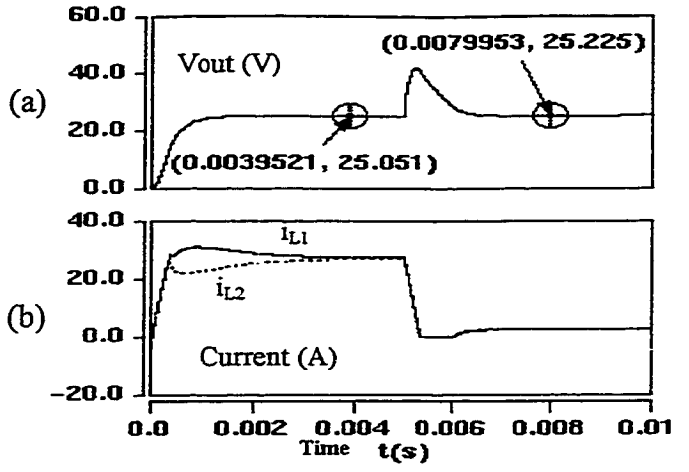


Fig. 7-14. Simulated results using (AM+OLR) sharing method, i.e., automatic master under outer loop regulation: (a) output voltage, and (b) output current.

It is shown in the following section that the difference between output inductor currents can be significantly reduced by the combined active current sharing schemes proposed by this thesis.

These results also illustrate some characteristics of the aforementioned schemes. From the comparison of Figs. 7-14 and 7-15, we can see that (BACP+OLR) method has better transient sharing characteristic than the (AM+OLR) method. This is because the (AM+OLR) method provides no control for the output current of the master converter, and relatively high output current overshoot during a transient start-up occurs. From the comparison of the Figs. 7-14 and 7-16, we can find out that the (AM+ILR) method has more precise output voltage regulation than (AM+OLR) method, this is because the reference voltage is adjusted in a timely fashion in (AM+OLR) method, while the reference voltage in (AM+ILR) method is not affected by sharing current control loop. In the above-mentioned methods, the (AM+ILR) method has overall the best characteristics, not only in steady-state but also in transient response. But its reliability may be affected by the common outer loop.

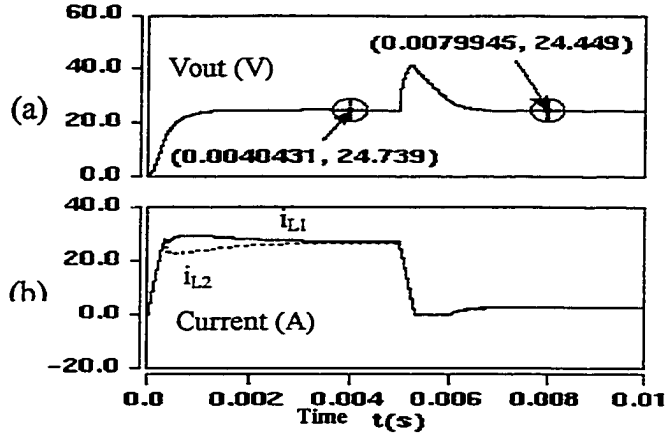


Fig. 7-15. Simulated results using (BACP+OLR) sharing method: (a) output voltage, and (b) output current.

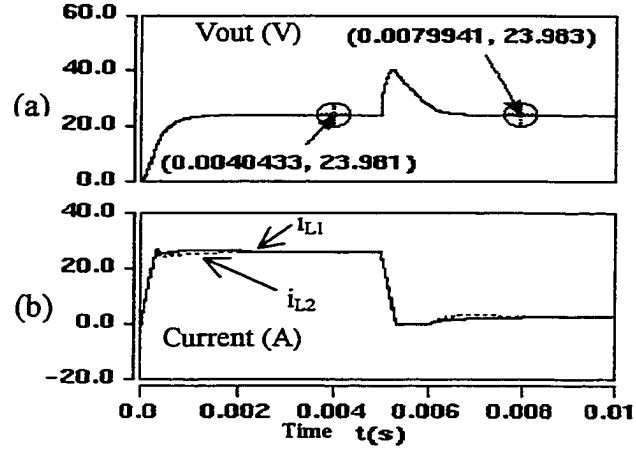


Fig. 7-16. Simulated results using (AM+ILR) sharing method: (a) Output voltage, and (b) Output current.

7.6 Summary

This chapter presented a classification of paralleling methods for power supply modules. Based on this classification, some new active current-sharing schemes can be obtained by proper combination of the sharing control structures and the current-programming methods listed. For instance, a combination of the inner regulation sharing

control structure and current-programming scheme of an automatic master can be expected achieve some special advantages. Future work will explore and discuss characteristics of some new combination schemes.

This chapter also presented a comprehensive review of paralleling schemes for power supply modules. Although it is impossible to cover each aspect of each scheme in one paper, we tried to present most of the methods and their issues that we deem are of common interest to practicing engineers in order to give a general picture of this field, while still including a few in-depth discussions on several special topics to provide some insights into paralleling system design.

In other words, each paralleling scheme has its own merits and limitations, and each application has different criteria. Some schemes and their design of a paralleling system still need to be assessed in more detail in the future. Ultimately, any design approach must achieve a balance between performance, reliability, and cost. Therefore, the author's opinion is that there is no single best scheme suited to all paralleling systems until now.

8 SYSTEM INTEGRATION TECHNIQUE — SIMPLIFYING BY HF AC BUS

8.1 Introduction

Basically, power architecture in current electronic systems remains the same as it was decades ago [1]-[5]. However, many of current power architectures are no longer effective in terms of performance and/or cost. Typically, in future computer systems, a power processing combination scheme of the silver box and VRM, as shown in Fig. 1-1, is finding its issues to practical design. These issues include not only improving efficiency, but also increased concerns regarding the cost and complexity of power supplying system. Instead, DC distributed power systems (DPS) may be viable approach. In DC-DPS, however, multiple power conversion steps are still needed to finish power conversion from ac input to final dc output, and thus the above issues still exist only with a slight alleviation.

As was discussed in Chapter 1, changing the "DC" power distribution to an "AC" power distribution can substantially mitigate the cost and complexity of DC-DPS. Other potential advantages of ac bus DPS include: simplified system configuration, high efficiency, ease of voltage and current transformation, effective ground noise isolation, and the possibility of connector-less distribution via a distributed transformer.

The above benefits are driving researchers to put more efforts into this subject. In currently available literature over the past several years, two types of AC-DPS with HF sine-wave bus and square-wave bus, featured with their respective advantages and

disadvantages, have been reported in [32]-[45]. However, HF AC-bus DPS have not been widely accepted in power system applications probably due to the following technical problems perceived:

1) So far there is no way to implement redundancy in an HF AC-DPS, which is critical for improving system level reliability, especially for field industry applications.

2) The other key issues, such as EMI noise, high frequency losses and bus distortion, etc, also need to be further identified for practical applications.

3) No systematical design literature is reported especially due to poorly defined tradeoff issues between system component design and system integration.

4) Post-regulator design is in light of the absence of the traditional method of PWM controlled converters.

In this chapter, a DPS with multiple HF PWM buses is proposed and experimental results are given, which demonstrates that the proposed system works well and is suitable for medium power (say several hundred watts) system applications.

As far as the first problem above, a DPS with trapezoidal waveform bus is presented that is expected to realize system redundancy. However, the idea is only in its conceptual stage and a lot of work remains to be done in the future.

8.2 A HF AC-DPS with Multiple PWM Buses

8.2.1 System Configuration

The proposed distributed power system is illustrated in Fig. 8-1. The whole system consists of three power stages (a) front-end AC/DC PFC stage, which employs a regular boost PFC converter; (b) front-end DC/PWM-bus inversion stage, which uses a

two-switches forward inverter that transforms DC to different voltage level PWM buses; (c) post-regulation stage, secondary-feedback control provides a regulated 5V DC output, other stable DC outputs are produced through magnetic-amplifiers (here abbreviated to Magamps) based on both PWM bus1 and bus 2.

It should be noted that in the system configuration of Fig. 8-1, the concept of conventional DPS with single ac bus has been expanded to multiple bus systems. Its advantage is in that a relatively higher efficiency can be obtained because we can appropriately design ac bus voltage to make magamps work more efficiently with decreased magnetic blocking area. For an instance, 12V output uses a bus and 5V and other lower than 5V outputs will share a common bus. Obviously, the limitation is in that the transformer structure is more complicated due to multiple secondary output windings. However, point-of-load regulation can still be obtained by these buses.

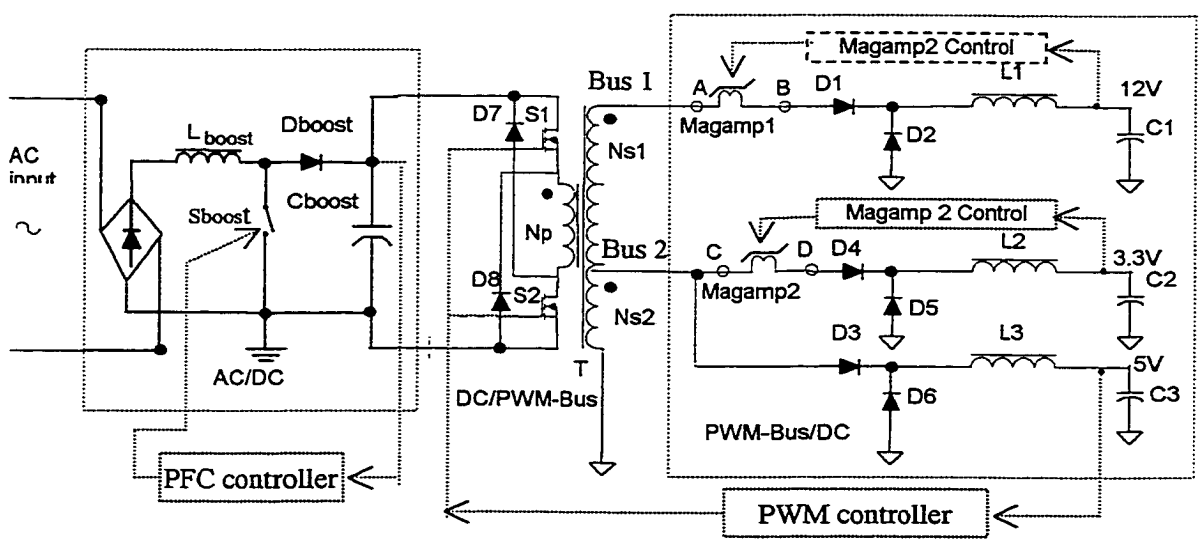


Fig. 8-1. System configuration block diagram of a new DPS with multiple PWM-wave bus.

Unlike front-end down converter in the traditional DC-DPS, we can see from the above diagram that in the front-end converter of this proposed ac system, a HF AC to DC (usually, 48Vdc) power conversion step is eliminated. Meanwhile, in post-regulators or the so-called VRMs, a HF DC to AC power conversion step is also eliminated. Therefore, the system structure is simplified and the system has potential higher efficiency.

The system shown in Fig. 8-1 demonstrates only three DC outputs. In fact, based on the bus 1 and the bus 2, more isolated outputs can be easily obtained just putting additional magamps before the loads so as to complete the final step of power conversion, i.e., HF AC to DC. As DC-DPS did, point-of-load related performance could be achieved by these magamps physically connected close to the local loads.

8.2.2 Principle of Operation

1) Front-end AC/DC PFC Stage

This stage consists of a boost choke L_{boost}, a boost switch S_{boost}, a rectifier diode D_{boost} and an output capacitor C_{boost}. One function of the controller in this stage is to control PFC stage so as to achieve a roughly regulated $400V_{dc}$ output to the next input of the following DC/PWM inverter. The other function of this stage controller is to shape input current to the envelope defined by the input voltage, thus achieving high power factor and low harmonic currents. Microlinear's IC 4824 is used in the control circuitry of the prototype.

2) Front-end DC/PWM-bus Inversion Stage

A two-switche forward converter is utilized to convert the $400V_{dc}$ bus to high-frequency PWM bus so that multiple outputs can be obtained by post-regulating based on

the high-frequency PWM bus. The high-frequency PWM bus is distributed with different DC voltage levels according to the requirements of the output voltages. In proposed system, the output regulation of 3.3V and 5V will share a common bus through secondary winding, N_{s2}, and the output regulation of 12Vdc will use the other isolated bus through the winding N_{s1}. As a result, each power train would be running under relatively optimized duty ratio, which significantly improves the efficiency of the whole system, especially for power trains regulated by magamps.

As shown in Fig 8-1, in the two-switche forward power stage, voltages of two buses reflected from the primary-side are determined by the turns ratios from primary winding to respective secondary winding. D_7 and D_8 provide reset path while turning the switches off, and at the same time have the reverse voltage of main switches clamped to the 400Vdc bus. The same controller IC 4824 is used to implement PWM control at this stage. Gate PWM signals pass through an isolated drive transformer to control each power MOSFET on or off.

3) Post-regulation Stage

In the proposed AC-DPS, two types of regulations are used to control final DC outputs, namely, regulation by PWM and regulation by Magamps. In Fig.8-1, the output at $5V_{dc}$ is regulated by PWM, and outputs of 3.3V and 12V are regulated by Magamps based on the ac bus 1 and bus 2. Therefore, the controller for $5V_{dc}$ output load determines the width of the PWM-wave buses.

As regular forward converter, L_3 and C_3 form output filter. D_3 provides rectification of the PWM wave and D_6 provides a conduction path for L_3 during the

freewheeling interval of the switching cycle. Usually, an additional pre-load is adopted to ensure the system stability.

The +12V output is post-regulated by magamp 1 from the high-Frequency PWM-wave bus 1. The high-frequency PWM voltage appearing on the transformer secondary winding of this output is first modulated by the magamp 1, and ac components are then filtered by L_1 and C_1. D_1 provides rectification of the square-wave and D_2 provides a conduction path for L_1 during the freewheeling period of the switching cycle. An additional pre-load is also adopted to ensure the system stability. The regulation mechanism of the +3.3V output is the same as that of the 12V output.

In fact, almost all conventional PWM topologies can be modified into magamp topologies. To help understand the operation principle of magamps, Fig. 8-2 gives an example circuit of half-wave magamp assuming where ideal magnetic core is being used. Three possible operating cases are listed in Fig. 8-3.

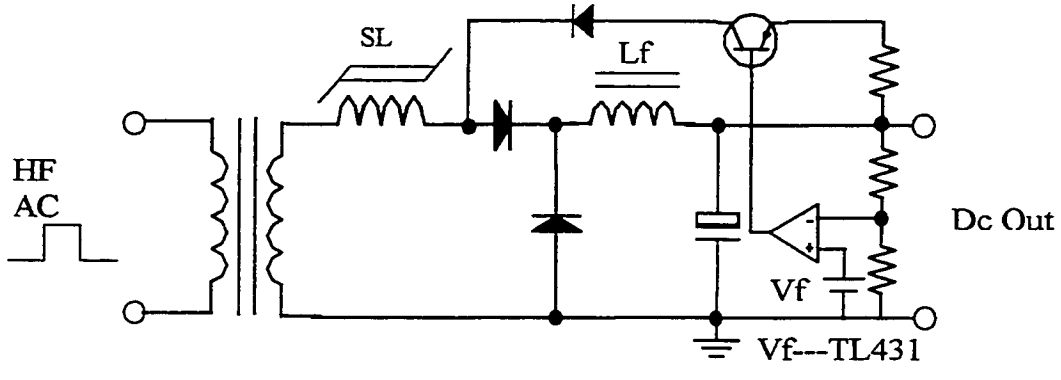
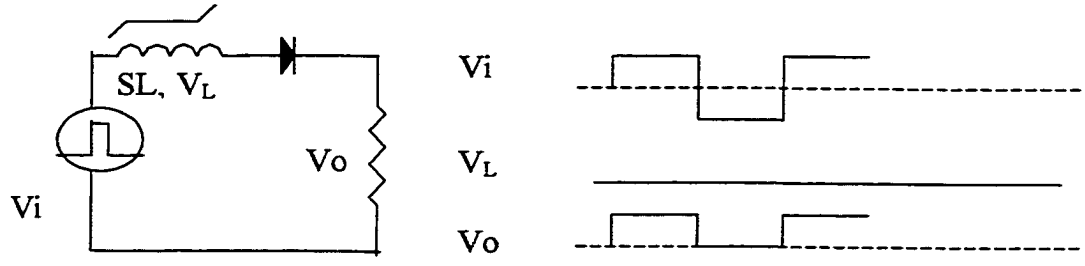


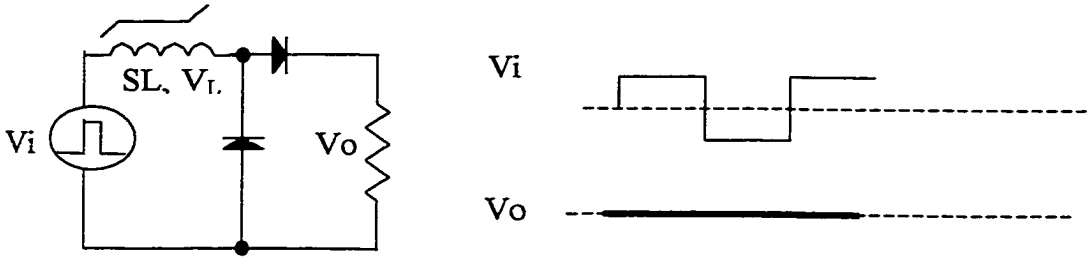
Fig. 8-2. An example circuit of half-wave magamp.

The operating principle of this magamp is similar to the forward converter. Its control circuit senses the output voltage and adjusts its output to drive transistor (or

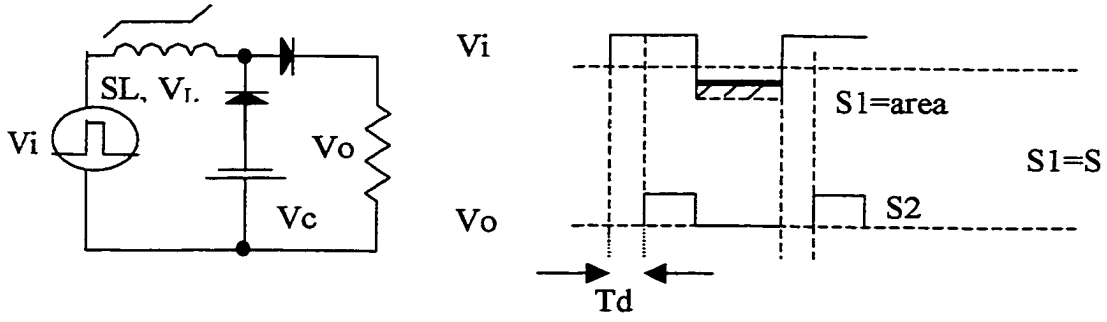
MOSFET). Magamp bias is generally from a fixed DC voltage source. The control voltage V_c determines how much current is allowed to reset the core of the magamp. Meanwhile, We can see from Figs. 8-2 and 8-3 that unlike PWM regulation of DC-DC converter, magamp's regulation against line and load variation is achieved by controlling the firing time (on-time as usual). Actually, it is done indirectly by controlling the blocking time (off-time as usual), T_d in the figure.



(a) Case 1: No de-magnitizing SL saturation, no inductance, so VL=0; Positive half-wave of Vi is outputted



(b) Case 2: enough de-magnitizing, no SL saturation, large inductance, large VL; Output equal to zero



(c) Case 3: partly de-magnitizing, S_1 is on after delaying T_d, portion of V_i is outputted

Fig. 8-3. Principle of operation for half-wave magamp using ideal magnetic core.

8.2.3 Basic Design Considerations

1) Front-end AC/DC PFC Stage

The output voltage of the boost converter is set to be higher than the peak value of the line voltage, typically with the value of $385V_{dc}$ to allow for a high line of 270Vac *rms*. In order to prevent ripple that will necessarily appear at the output of the boost circuit (typically about $15V_{ac}$ on a $385V_{dc}$ level), the bandwidth of the voltage loop is deliberately kept low. Therefore, for ac $170\sim270V_{ac}$ input, a range of DC output should be considered from $360\sim400V_{dc}$.

For 400Vdc output, active switch and diode with 600V stress can be used for this purpose, and of course, a snubber circuit is also necessary to the switch and diode.

The power stage inductor design is identical to the conventional boost converter. The inductance is determined by the switching ripple current. Under the worst case at low line and full load, the peak current is approximately given by:

$$I_{pk} = \sqrt{2} \cdot \frac{Po/\eta}{V_{in,\min}} \tag{8.1}$$

where, I_{pk}: the peak of inductor current

Po: the output power

$V_{in,min}$: the minimum *rms* value of input AC line voltage

η: the efficiency of the circuit.

The duty cycle corresponding to peak voltage could roughly be determined by:

$$D = \frac{V_{PFC} - \sqrt{2} \cdot V_{in.\min}}{V_{PFC}} \tag{8.2}$$

where V_{PFC} is the output voltage of the PFC stage

The required boost inductance can be determined by:

$$L_{boost} = \frac{\sqrt{2} V_{in,\min} \cdot DTs}{\Delta I} \tag{8.3}$$

where T_s is the switching period.

ΔI is the peak-peak inductor ripple current, usually, it is selected as 20% of peak current.

The main factor in selecting the output capacitance value for this circuit is the output voltage ripple caused by the second harmonic. The equation that defines the capacitance value is expressed as:

$$C_o = \frac{Po/\eta}{2\pi f_r \cdot V_{rpk} \cdot V_{PFC}} \tag{8.4}$$

where, V_{rpk} is the peak value of the output ripple voltage (the peak to peak value will be twice of this value), f_r is the second harmonic line frequency, and V_{PFC} is the PFC stage output voltage, as conservative design, it should be taken a max value, here $400V_{dc}$.

The design for control circuit can follow general design procedure given by IC manufacture manual.

2) Front-end DC/PWM Bus Inversion Stage

Fed by the DC output from the PFC stage, the two-switch forward inverter transforms the 400 V DC voltage into HF PWM wave outputs, which constructs the HF PWM bus for post-regulators. Required by magnetic core demagnetizing, maximum duty

ratio should be limited lower than 50%. The power transformer turns ratio should be carefully designed to fit variation of input voltage and load. Meanwhile, we should also consider bus voltage level so that different post-regulator could work more efficiently.

In this stage, the most important component is the transformer that will bring significant effect into both front-end inverter and post-regulators. The product of window area and core cross-area of the transformer operating at forward mode can be determined by

$$area\_product = \frac{2V_{PFC} I_{1rms} D}{K_u B_{max} J_m f_s} \tag{8.5}$$

where K_u: Window factor

I_{1rms}: total primary *rms* current reflected from each secondary-side.

J_m: current density, also depending on cooling condition.

B_{max}: max flux density, generally, taking $\frac{2}{3}(B_S)$.

D and f_s: duty ratio and switching frequency

The number of turns of primary-side of the transformer is determined by

$$N_P = \frac{DV_{PFC}}{A_C B_{max} f_s 10^{-6}} \tag{8.6}$$

The voltage of bus 1 is determined by

$$V_{bus1} = \frac{(V_{O1} + V_D + V_{mag})}{D} \tag{8.7}$$

where V_D is forward voltage drop for the diode, and V_{mag} is min voltage of magamp while working at saturate status and V_{O1} is the reference voltage of output #1 ($12V_{dc}$).

The voltage of bus 2 is determined by

$$V_{bus2} = \frac{(V_{O3} + V_D)}{D} \tag{8.8}$$

where the V_{O3} is the voltage of the output #3 and output #2 having lower voltage level will be automatically met.

Now turns of two secondary-side windings can be determined respectively by

$$N_{S1} = \frac{V_{bus1}}{V_{PFC,\min}} \times N_P \tag{8.9}$$

and

$$N_{S2} = \frac{V_{bus2}}{V_{PFC,\min}} \times N_P \tag{8.10}$$

3) Post-regulation Stage

The magnetic amplifier (Mag-Amp) technique is one of the most reliable and cost-effective post-regulation methods. This is especially true for high-current post-regulated outputs since at higher output currents that the efficiency of the linear post-regulators is unacceptably low, while the complexity of more efficient switch-mode post-regulators is associated with a significant cost.

To obtain good tradeoff design for magamps, the following constraints should be followed. First, blocking time t_{block} is calculated from basic Farady's law:

$$t_{block}(\text{sec}) = \frac{N_m A_e (B_{sat} - B_{reset})}{V_{bus}} \times 10^{-8} \tag{8.11}$$

where N_m: number of turns on magamp

A_e: magamp core area, cm^2

B_{sat}: saturation flux density, G

B_{reset}: reset point in flux density, G

V_{bus}: HF bus voltage, V

The t_{block} should be effectively smaller than max on-time in each PWM cycle while considering peak value and min value of bus voltage. Second, the maximum core loss can be estimated from

$$P_{core}(W/Kg) = K_c \times f_s^{1.57} \times (\frac{B_{sat} - B_{reset}}{2})^{1.70} \quad (8.12)$$

where B_{sat} and B_{reset} are in tesla, f_s is in hertz, and the factor K_c depends on the feature of core material. From the above formula, we can get insight how to choose proper core material with acceptable core cost/loss target.

8.2.4 Experimental Results

An experimental prototype has been built with a total of 210W output power for three independent outputs, i.e, 3.3V@30A, 5.0V@10A, and 12V@5.1A. The operation frequency of the front-end converter is designed to be near 100kHz and bus duty cycle at nominal operation condition is designed around 30% and its variation mainly depends on the variation of the load. The maximum duty cycle is limited to lower than 50%.

Key waveforms of major components in the power circuit were recorded by using Tektronix scope when the power supply was running at full load at 3.3V @ 30A, 5V @ 10A, and 12V @ 5.1A. Figures 8-4 and 8-5 show typical operating waveforms of lower switching MOSFET and clamp diode for a two-switch forward inverter. Figures 8-6 and 8-7 show working waveforms of key points for two magamps. The total efficiency is near 80% from ac input to three DC outputs. The efficiency will be further improved by optimizing nominal duty-cycle and power train components. These experimental results

initially verify the feasibility of the idea of utilizing high frequency multiple PWM buses in the distributed power system instead of DC bus in the conventional applications.

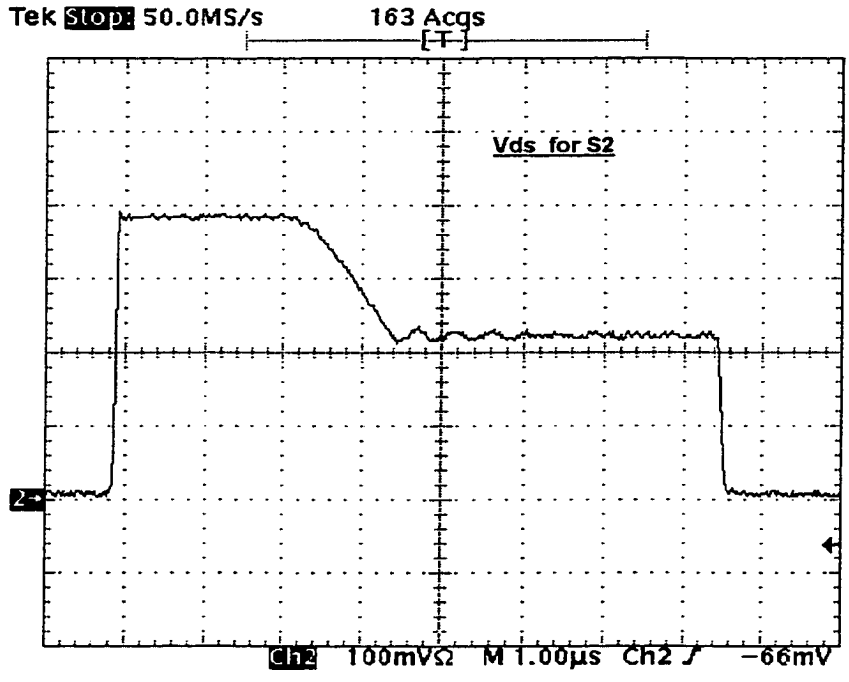


Fig. 8-4. Drain to source voltage for switching MOSFET S_2, 100V/div.

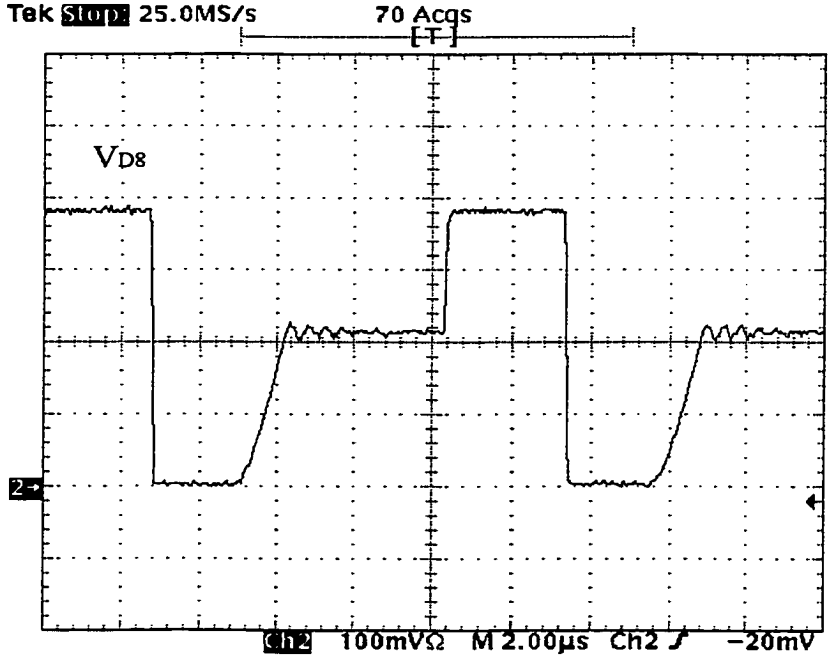


Fig.8-5. Blocking voltage on D_8.

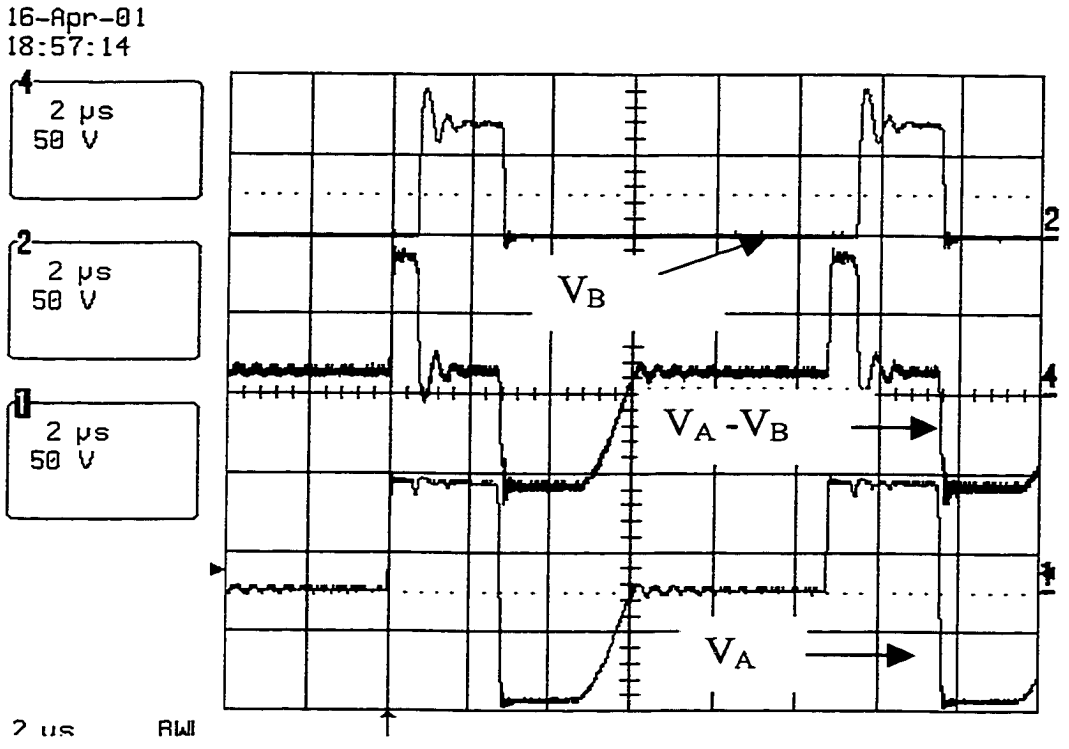


Fig. 8-6. Operating waveform of magamp at 12V output.

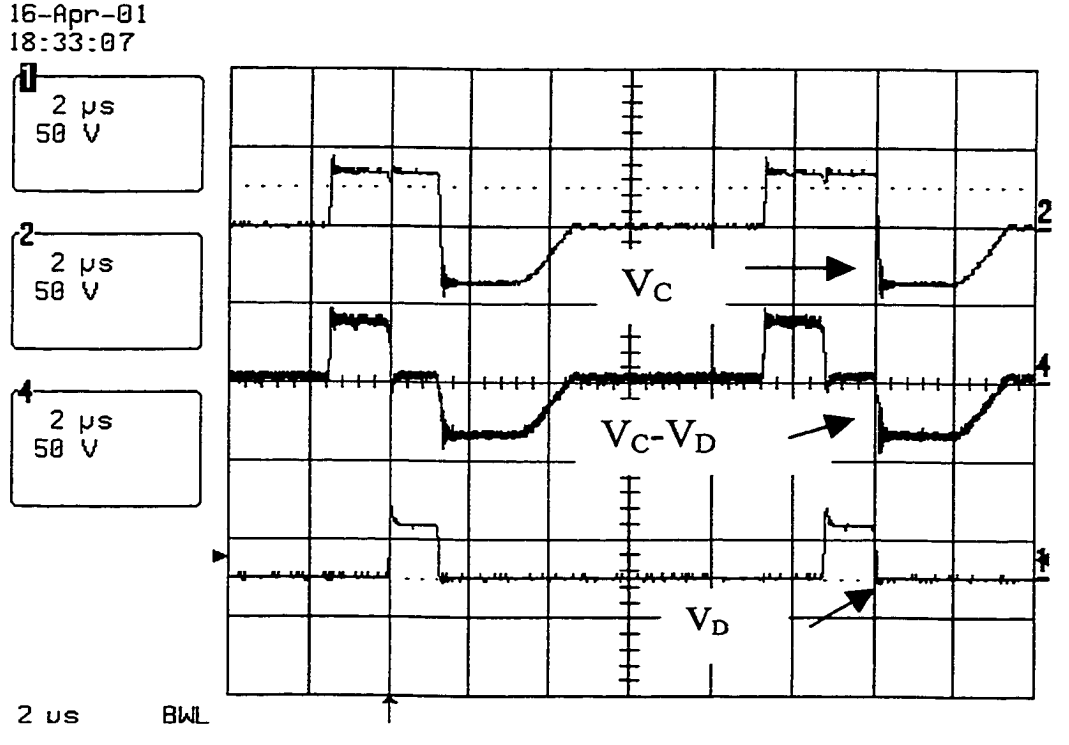


Fig. 8-7. Magamp waveform for 3.3V output.

8.3 A Redundant AC-DPS with Trapezoidal Waveform Bus

Basically, there are two waveform shapes to be used as ac bus waveforms, namely, sine-wave and square-wave/PWM waveforms. Advantages and disadvantages of the two buses are highlighted as follows:

Sine-wave bus advantages

- Relatively high efficiency for distribution to line transformer;
- Less potential noise and EMI related effects in distributed system; and
- The wide range load regulation is relatively more difficult.

Sine-wave bus disadvantages

- Almost impossible to construct redundant power system;
- Relatively low efficiency front-end converter caused by circulating energy ; and
- Several complicated ways to do load voltage regulation by using SRRs.

Square-wave bus advantages

- Simpler/cheaper for both front-end inverter and load converter;
- Most of HF PWM converters can be modified as front-end inverters; and
- The wide range load regulation is relatively easier.

Square-wave bus disadvantages

- Almost impossible to construct redundant power system;
- High harmonic contents and EMI level on the bus and distributed system; and
- Load converters seem to be limited to magamp types.

From the above comparison, we can see that the advantages and disadvantages for both buses are manifest. However, system redundancy becomes a common issue to block

HF AC-DPS into practical applications. Meanwhile, this common issue is also challenging, particularly under high frequency. For instance, three key factors on sine-wave bus, i.e., frequency, magnitude and phase for each front-end converter must be kept identical if system redundancy would be implemented. On the other hand, for a practical design consideration, bus waveform shape depends heavily on load features such as required regulation range, noise sensitivity and distribution distance, etc.

The key point of the design of power electronics systems is to seek for the best tradeoff of major technical specifications. Now the question comes up if we could find a bus waveform that will combine major advantages and eliminate main disadvantages for both of conventional sine-wave and square-wave buses. In order to reach the goal, a trapezoidal waveform bus is presented and possible redundant structure frond-end inverters are proposed below:

By comparison analysis, Major characteristics of trapezoidal waveform bus are:

- Redundant capability with (n+1) front-end converters paralleled;
- Compromised harmonic and EMI level; and
- High efficiency thanks to using converters of square-wave bus DPS.

Figure 8-8 shows a scheme to implement new AC-DPS with trapezoidal waveform. Bus waveform shape can be optimized by adjusting peak value and width of each inverter output. During normal operation, converters #1, #2 and #3 together maintain bus voltage. If anyone of the three front-end converters fails, the remaining two converters will power the bus and pick up the loads. Another important feature is that the bus voltage waveform is still trapezoidal waveform even if one unit fails. Hot-plug is possible under properly designed interface. This concept helps realize system redundancy

and improve system reliability by merely employing trapezoidal waveform bus concept. At the same time, a tradeoff for EMI level and efficiency could be obtained. Its major disadvantage is that system structure is relatively complicated due to using multiple front-end converters. However, in conventional DC-DPS, multiple front-end converters must be used when the system redundancy is necessary. Moreover, high power application generally requires multiple converter system. Therefore, multiple converter structure is not its inherent drawback for the AC-DPS with trapezoidal waveform bus.

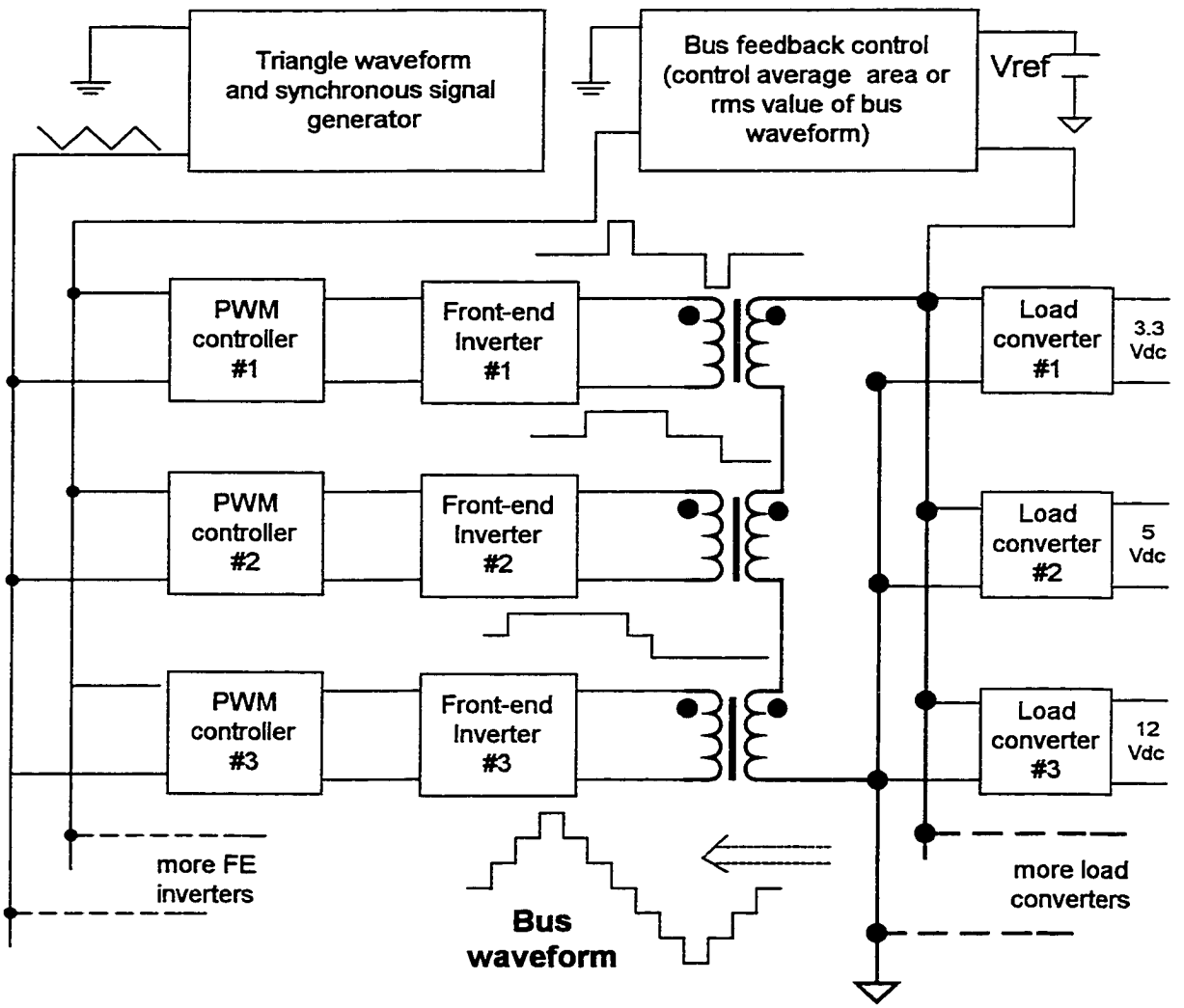


Fig. 8-8. Proposed scheme to implement AC-DPS with trapezoidal waveform bus.

8.4 Summary

In this chapter, a new DPS with multiple HF PWM buses is proposed and basic design considerations are given. Experimental prototype has been built with a total of 210W output power for three independent outputs, i.e, 3.3V@30A, 5.0V@10A, and 12V@5.1A. The experimental results demonstrate that the proposed system works well and a comparable efficiency around 80% can be obtained by this simple DPS system.

In order to realize system redundancy, a new AC-DPS with trapezoidal waveform bus is presented and a conducting scheme is proposed. Bus waveform shape can be optimized by adjusting peak value and width of each inverter output. The scheme is expected that will combine major advantages and eliminate main disadvantages coming from both conventional sine-wave and square-wave buses. However, the idea is only in the conceptual stage and a lot of work remains to be done in the future.

This work was supported by the grant from NSF.

9 CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

This dissertation explores front-end converter design and system integration techniques in distributed power systems, with the objective of achieving improvements in converter topology, system performance, system configuration and cost-effectiveness over conventional approaches. Key issues of S^2 PFC converters are addressed and the solutions to these issues are investigated. The optimization design procedure of a family of S^2 converters, which is based on the averaging circuit model and MathCAD tool, is developed and verified by both simulation and experiment. A new PFC cell is presented with direct-power-transfer (DPT) concept, and a new family of S^2 converters is derived and experimentally verified which has excellent characteristics that help push S^2 converters into medium power applications. A comparison study of high power down converters is conducted, and in particular, experimental comparison of high power level for secondary-side topologies is completed in this dissertation. Also, we investigate system level techniques such as paralleling, interleaving and configuration simplifying. A new interleaving method for high power converters is presented and simulated results demonstrate its potential for decreasing filter size and increasing power density. New paralleling methods for power converters have been obtained based on the comprehensive classification and evaluation of current paralleling approaches. The dissertation also describes the operation principle, design considerations, and

experimental results of an AC-DPS with multiple PWM-wave buses. Finally, a redundant AC-DPS with trapezoidal waveform bus is proposed. Major conclusions achieved by this dissertation work are summarized as follows:

First, current techniques in DPS are comprehensively reviewed and the issues and challenges in this research area are identified. These issues include not only improving efficiency, but also increased concerns regarding the cost and complexity of power supplying systems. Theoretically, changing the "DC" power distribution to an "AC" power distribution can substantially mitigate the cost and complexity of conventional DC-DPS. Other potential advantages using ac bus into DPS include simplified system configuration, high efficiency, and ease of voltage and current transformation, as well as effective ground noise isolation.

The high bus capacitor voltage-stress generally exists for S^2 PFC converters, which makes most of existed S^2 converters be impractical especially for universal input applications. The inherent reason of high DC bus voltage is in power unbalance between the input and the output. Simplified theoretical analysis and simulation show that both the series-charging, parallel-discharging capacitor scheme and the bus-voltage-feedback method are more viable than the other methods for alleviating bus voltage stress. Another challenging issue is wide dc bus voltage range, which makes the design of a high efficiency converter be very difficult. Based on the averaging circuit model and MathCAD tool, an optimization methodology, which is applicable to most of S^2 converters, has been presented and verified through both simulation and experiment on the basis of a 150 W prototype at 28 V output. From the research of target S^2 converters, it can be generalized that higher the turns ratio, lower dc bus voltage, wider bus voltage

range yielded, and larger boost inductor and wider duty cycle operation result in higher efficiency for the same operation mode. The crossover frequency of the controller in a DCM S^2 converter can be designed far higher that of conventional boost front-end converters employing averaging current control mode, so as to obtain better transient response.

A new PFC cell with DPT concept, called "flyboost", is presented. It combines the functions of a flyback transformer and a boost inductor. While operating in flyback mode, the flyboost cell will directly transfer input power to the load; while at the boost mode, it will transfer input power to the storage capacitors for the following DC/DC converter to conduct fast regulation for the output voltage. By having flyboost cell operated in DCM, only a simple control will be required to achieve high power factor (greater than 0.97). The flyboost cell also significantly helps improve the converter efficiency above 5% over the converter without flyboost. Another important characteristic of the flyboost cell is that it will also automatically limit the DC bus voltage through a properly designed flyboost transformer and power train, which means that the converters using flyboost cell can operate either DCM+DCM mode or DCM+CCM mode. As a result, the proposed converters are especially suitable for universal voltage applications with higher power handling capability than other known S^2 converters. By combining the flyboost cell and any family of other DC/DC conversion cell, we can obtain a new family of S^2 PFC converters. Further, proposed flyboost cell might also be suitable for other topologies to replace PFC cell and thus achieve high performance.

In high-power down converters, ZVT-PS-FB topology is the best choice for primary-side topologies under medium input voltage level such as 400Vdc. Under high input voltage such as 800Vdc bus, generally, the primary-side topologies based on multilevel cell combination have relatively simple structure and low switch number. Also it does not have the problem of voltage sharing that appears on the converters based on capacitive clamping. The topologies based on the association of converters have higher magnetic volume than the structures based on multilevel cell association. For the secondary-side topologies, though the current-doubler rectifier has higher efficiency, the center-tapped counterpart may have some advantages in terms of cost and power density. In summary, regardless of primary-side or secondary-side topologies, the desirable approach would vary depending on which criteria is deemed most critical, such as cost, size, or efficiency. It also varies depending on specific applications.

According to the frequency relationship between switching frequency and output ripple frequency, topologies are reclassified into secondary-side, same-frequency rectification topologies and secondary-side, double-frequency rectification topologies. It was found that the conventional interleaving technique is actually suited only for the secondary-side, same-frequency rectification topologies. For the secondary-side, double-frequency rectification topologies, phase-shift quantity among module control signals for N interleaved modules should be reduced to π/N. Typically, for the two-power stage case, a special quarter-cycle phase shift between two control signals is required, not the previous half-cycle (180 degree) phase shift. The characteristics achieved from the new interleaving method are as the same as those from the conventional one, such as increased output ripple frequency, automatic ripple cancellation, and less EMI level, etc.

Based on the classification of paralleling methods for power supply modules, some new active current-sharing schemes can be obtained by the proper combination of the sharing control structures and the current-programming methods. For instance, a combination of the inner regulation sharing control structure and current-programming scheme of an automatic master can be expected to achieve some special advantages. In summary, each paralleling scheme has its own merits and limitations, and each application has different criteria. Ultimately, any design approach must achieve a balance among performance, reliability, and cost. Therefore, the author's opinion is that there is no single best scheme suitable for all paralleling systems at present.

A new DPS with multiple HF PWM buses is proposed and experimental prototype has been built with a total of 210W output power for three independent outputs, i.e, 3.3V@30A, 5.0V@10A, and 12V@5.1A. The experimental results demonstrate that the proposed system works well and a comparable efficiency around 80% can be obtained by this simple DPS system. In order to realize system redundancy, a new AC-DPS with trapezoidal waveform bus is presented and a conducting scheme is proposed. The scheme is expected to combine major advantages and eliminate main disadvantages coming from both sine-wave and square-wave buses.

9.2 Future Work

Based on the work done in this dissertation, there are several directions in which the continued development of distributed power systems should proceed. The optimization design procedure developed in Chapter 3 considers only steady-state characteristics of target S^2 converter. In the future theoretical work, small signal characteristics and large signal transient behavior also should be taken into the overall optimization design considerations.

For the proposed new flyboost PFC cell and derived S^2 topologies, this dissertation completes only initial verifications and discussion for main characteristics and operation mechanisms. Obviously, a lot of theoretical analysis work still remains to be done. For instance, circuit modeling and systematic design procedure of new converters with DPT concept need to be developed.

Current S^2 converters generally have wide DC bus voltage range, and most of them operate in DCM + DCM mode. This results in their application strongly limited in low power range. Therefore, how to reduce the DC bus voltage range and push S^2 converters operating at double CCM mode with acceptable specifications will be interesting future work, which will improve overall performance and push the applications into medium power range such as 300-600W.

In primary-side topologies under high input voltage such as 800Vdc bus, the topologies are compared only by simple analysis. Characterizing these topologies by comprehensive simulation and experimental study is a necessary next step in their development.

The simulation study verifies interleaving method for secondary-side double-frequency rectification topologies. However, the simulation is completed only for the two interleaved power stages. Further efforts should a simulation based on the multiple interleaved power stages and validation of the technique by experiment.

The newly combined active current-sharing schemes listed in Table 7-1 need to be further investigated by more simulations and experiments. Some paralleling schemes and their system design still need to be assessed in more detail in the future.

In Fig. 8-8, a new AC-DPS with trapezoidal waveform bus has been proposed to realize system redundancy, but its research is put only at conceptual stage, and thus a lot of work remains to be done in the future, including theoretical and experimental efforts.

Indeed, changing the "DC" power distribution technique to an "AC" power distribution can substantially mitigate the cost and complexity of DC-DPSs. However, HF AC-bus DPSs have not been widely accepted in power system applications due to several challenging issues. In fact, currently open literature shows that on the HF AC bus topic, the research is still in its infancy. Further work might be directed at the following points:

1) Explore available approaches to implement system redundancy in an HF AC-DPS.

2) A complete comparison between the AC-DPS and DC-DPS needs to be conducted in terms of system cost, efficiency and other major performance.

3) Further identify EMI noise at the bus waveform, and high frequency losses at the bus distortion, ... etc.

4) Develop systematical design documents, particularly for tradeoff design methodology between system component design and system integration.

5) Develop high performance post-regulators, including ones to be suitable for the trapezoidal waveform bus.

6) In order to realize the simplest AC-DPS shown in Fig. 1-5, viable S^2 inverters should first be developed.

Last but not least, the development of proposed converters and DPSs for some specific industrial and/or commercial applications should be undertaken. This would allow direct performance and cost comparisons to be made with existing solutions, and would provide the most realistic framework possible for the assessment of the developed approaches.

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