NOVEL VOLTAGE REGULATOR CONTROLLERS AND TRANSIENT COMPENSATORS FOR POWERING MICROPROCESSORS

By

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ABSTRACT

This dissertation provides advanced solutions related to the power management of Intel's microprocessors. The main solutions presented here focus on the controller design and extremely fast transient compensation.

The analog controller described in this dissertation is a proportional ON-TIME system for portable usage. No pre-stage is needed for powering the voltage regulator to achieve better efficiency. It could be considered as improved hysteretic control with controllable "ON-TIME" duration. It is also very easy to achieve current sharing.

The digital controller introduced here is a current senseless system. Based on adaptive control theorem, it observes the instantaneous phase currents and load resistance. This is the basis of a novel peak current control method for achieving current sharing. Combined with hysteretic control, a simple and fast controller is built for next generation of voltage regulator.

An extremely fast transient compensator is presented for the next generation of high current slew rate microprocessors. It dramatically reduces the decoupling capacitors mounted around the CPU by compensating the parasitic resistance and inductance at traces, connections and sockets. For easy understanding, it can be considered a discrete voltage regulator which only works at high *di/dt* transient and behaves as a linear regulator.

To My Parents and Husband

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CHAPTER ONE

INTRODUCTION

1.1 Developing Tendency of Voltage Regulator Modules (VRMs) for New Generation of Microprocessors

Recent microprocessor technology enables the new generation processors to operate above 3GHz. The operation frequency will be further boosted in the near future. Due to the thermal problems, the new generation of chips is developed based on low-voltage operation. Furthermore, the semiconductor companies are targeting chips running below 1V for higher speeds. Meanwhile, the operating current for present Pentium 4 microprocessors already reaches the *70A* level and it will be larger than *100A* in the coming years.

The Pentium® family [1-6] allows the processor to operate in active mode and sleep mode (including three states, i.e., Stop-Grant, Sleep, and Deep Sleep) to reduce unnecessary energy consumption and thermal generation. For example, the microprocessor draws a high current (*70A*) from the power supply known as Voltage Regulator Modules (VRMs) during the "active-mode" state and low current (*5A ~10A*) when it switches to the "sleep-mode" state. The largest current slew rates during state shift might reach *500A/μs* level

for Pentium 4 processors. Thanks to the contributions of huge decoupling capacitors mounted beside the processor [3], the current slew rate at the VRM end is reduced dramatically to *1/10* of the processor's VCC output end, i.e. *50A/μs* level when the microprocessor switches from one state to the other [1-6]. However, it still causes voltage spikes at the VRMs' output end and processors' VCC end. Based on the design guidelines, these transient spikes must be limited to a certain maximum value such as *1%~2%*. Obviously, as the processors' operating voltage becomes lower, the allowed voltage deviation during the load transient becomes tighter.

What makes the challenge even more difficult is that the current drawn from the VRM by the microprocessor is unknown and time varying, since it depends on the operation task of the microprocessor. Furthermore, the VRM itself is a nonlinear system with switching elements, inductors and capacitors. All of these make it complicated to design a high performance controller [6-18].

Tables 1.1 shows the current and voltage specifications for Pentium® II, Pentium® III, and Pentium® 4 processors, respectively to show the developing tendency [1-6]. Table 1.2, Table 1.3 and Figure 1-1 give the operating voltage and current requirement for present Pentium 4 2.0GHz ~ 3GHz processors. Table 1.4 shows an estimated current and voltage roadmap for future generation. It shows how low the required voltage will be and how large the required current will be [1-6].

1.2 Technical Challenges of Low-Voltage High-Current Fast-Transient VRMs

Unfortunately, it is difficult to provide a satisfactory solution for the traditional power supply. Power management for the new and future generation computer systems is challenging mainly due to the following issues:

1) The current drawn from the VRM increases dramatically, resulting in significant power loss in components, causing difficulties in the thermal management.

2) Large load current changes and high current slew rate together with highly restricted transient voltage tolerance severely challenges the dynamic response performance of the VRM.

3) Noise and EMI immunity becomes dominant in such a low voltage system.

4) Lower static supply voltage tolerance 2% or less for future generation.

5) Because the output current of VRM is extremely high, the distinction between normal operation and short circuit operation becomes vague, resulting in difficulty in short circuit protection.

6) Due to the requirement of the high efficiency, current senseless topology is a demand for the controller.

7) Smaller size and lower cost are required for a high-integrated system board.

Hence, the "Driving Forces" for the future VRMs includes: reduced voltages, increased currents, faster response, lower output voltage deviation, reduced cost, increased reliability, increased efficiency, increased power density, improved electromagnetic compatibility (EMC), and improved packaging (Mainly, thermal management and surface-mount components).

In order to address the above technical challenges, the following research issues need to be emphasized:

1) Development of advanced control schemes, which should be fast and smart enough to react to the fast load change. Advanced Digital Signal Processing (DSP) controlling schemes are the strongest candidates for this purpose.

2) Development of advanced power conversion circuit topologies with optimized power system configurations and high efficiency to meet the even increase stringent specifications. This option seems to be somewhat limited since the most practical topologies until now are buck converter derived.

3) Development of advanced power devices, including high current and high frequency, low loss and high density magnetic components and low ESR and low ESL capacitors.

4) Development of advanced packaging techniques.

1.3 Contributions of this Dissertation

This dissertation introduces three advanced solutions for powering Pentium series microprocessors:

1) Active current compensation for compensating voltage drops during high current slew rate load changes. This idea not only solves the problem of transient voltage spikes it also dramatically reduces the size of the decoupling capacitors on the system board. Therefore, it provides a fast transient, small voltage deviation, small size (compared with tens of capacitors), and low cost solution (compared with tens of capacitors).

2) Time-varying current observer with digital feedback control for achieving current senseless control and realizing current sharing. This idea uses adaptive control method to estimate the time-varying load resistance and calculates instantaneous phase currents and load current. Based on those values, the digital controller can execute a novel peak current control as well as voltage hysteretic control for

multiphase VRMs. Therefore, it provides a low noise, low EMI, high efficiency and high integration solution.

3) Multiphase proportional ON-TIME control for wide input voltage systems like portable usage. This improves the defect of voltage hysteretic control in portable systems that the frequency varies dramatically when input voltage changes. The varying ON-TIME window based on the average phase current provides better current sharing performance compared with hysteretic control. Therefore, it provides a fast transient, good current sharing and low EMI solution for portable usage.

Table 1.1: Current and Voltage Specifications for Pentium Microprocessors

	V_{cc} (*V*)			I_{cc} (*A*)	
Pentium® II	2.8			(*MHz*)	Max
				233	11.8
				266	12.7
				300	14.2
Pentium® III	(*MHz*)			Max	
	600/600B		2.00	17.8	
	550			17.0	
	533B			16.7	
	500			16.1	
	450			14.5	
Pentium® 4	(*GHz*)	Min	Max	Max	
	1.4	1.560	1.700	40.6	
	1.5	1.555		43.0	
	1.7	1.530		52.7	

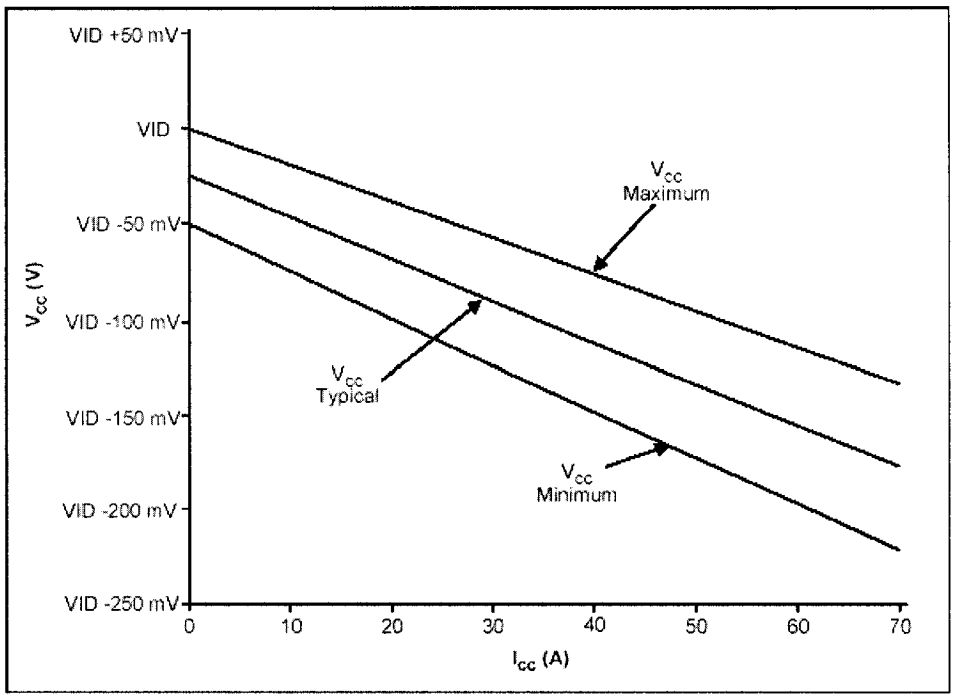


Figure 1-1: VCC static and transient tolerance

Table 1.2: Voltage and Current Specifications for Present Pentium 4 Processors

Symbol	Parameter	Min	Typ	Max	Unit
VCC (800MHz FSB)	VCC for CPU at VID=1.476		Refer to Table 1.3 and Figure 1-1		V
	2.4GHz	1.285		1.375	
	2.6GHz	1.280		1.370	
	2.8GHz	1.268		1.368	
	3GHz	1.265		1.350	
	3.2GHz	1.260		1.345	
	VCC for CPU at VID=1.600				
	2.4GHz	1.320		1.400	
	2.6GHz	1.315		1.395	
	2.8GHz	1.313		1.394	
	3GHz	1.290		1.375	
	3.2GHz	1.285		1.370	
	VCC for CPU at VID=1.625				
	2.4GHz	1.345		1.425	
	2.6GHz	1.340		1.420	
	2.8GHz	1.338		1.418	
	3GHz	1.315		1.400	
	3.2GHz	1.310		1.395	
	VCC for CPU at VID=1.650				
	3GHz	1.340		1.425	
	3.2GHz	1.335		1.420	
ICC (800MHz FSB)	ICC for CPU with multiple VIDs				A
	2.4GHz			52.4	
	2.6GHz			55.5	
	2.8GHz			55.8	
	3GHz			64.8	
	3.2GHz			67.4	

Table 1.3: VCC Static and Transient Tolerance

ICC (A)	Voltage deviation from VID Setting (V)		
	Maximum	Typical	Minimum
0	0.000	-0.025	-0.050
5	-0.010	-0.036	-0.062
10	-0.019	-0.047	-0.075
15	-0.028	-0.058	-0.087
20	-0.038	-0.069	-0.099
25	-0.048	-0.079	-0.111
30	-0.057	-0.090	-0.124
35	-0.067	-0.101	-0.136
40	-0.076	-0.112	-0.148
45	-0.085	-0.123	-0.160
50	-0.095	-0.134	-0.173
55	-0.105	-0.145	-0.185
60	-0.114	-0.156	-0.197
65	-0.124	-0.186	-0.209
70	-0.133	-0.177	-0.222

Table 1.4: International Technology Roadmap for Semiconductors (ITRS-1999)

Year Technology, μm		2002 0.13	2003	2004	2005 0.1
Power Supply voltage, V	Maximum (For best performance)	1.5	1.5	1.2	1.2
	Minimum (For lowest power)	1.2	1.2	0.9	0.9
Maximum Power with heat sink, W		130	140	150	160
Current (for maximum performance), A		87	93	125	133
P-P tolerance (±3% V_{nom}), mV		90	90	72	72
Chip frequency, GHz		2.1	2.49	2.952	3.5

References

[1] Intel Corporation, "VRM 8.1 DC-DC Design Guidelines", May 1997.

[2] Intel Corporation, "VRM 8.4 DC-DC Design Guidelines", November 1999.

[3] Intel Corporation, "VRM 9.0 DC-DC Design Guidelines", November 2001.

[4] Intel Corporation, "Intel Pentium 4 Processor VR-Down Design Guidelines", November 2002

[5] Intel Corporation, "Voltage Regulator-Down 10.0 (VRD) Design Guidelines", April 2003

[6] Intel Application Note AP-912, "Pentium® III Xeon™ Processor Power Distribution Guidelines," March 1999.

[7] B. Arbetter and D. Maksimocic, "DC-DC Converter with Fast Transient Response and High Efficiency for Low-Voltage Microprocessor Loads," IEEE Thirteenth Annual Applied Power Electronics Conference and Exposition, APEC'98, Vol. 1, pp. 156-162, 1998.

[8] P. Wong, F. Lee, X. Zhou and J. Chen, "Voltage Regulator Module (VRM) Transient Modeling and Analysis," IEEE 34th Annual Industry Applications Conference Record, IAS'99, Vol. 3, pp. 1669-1676, 1999.

[9] Y. Panov and M. Jovanovic, "Design and Performance Evaluation of Low-Voltage/High-Current DC/DC On-Board Modules," IEEE Fourteenth Annual Applied Power Electronics Conference and Exposition, APEC'99, Vol. 1, pp. 545-552, 1999.

[10] Y. Panov and M. Jovanovic, " Design Considerations for 12-V/1.5-V, 50-A Voltage Regulator Modules," IEEE Fifteenth Annual Applied Power Electronics Conference and Exposition, APEC'00, Vol. 1, pp. 39-46, 2000.

[11] M. Zhang, M. Jovanovic and F. Lee, "Design Considerations for Low-Voltage On-Board DC/DC Modules for Next Generations of Data Processing Circuits," IEEE Transaction on Power Electronics, Vol. 11, Issue 2, pp.328-337, March 1996.

[12] J. Renauuer, "Challenges in Powering High Performance, Low Voltage Processors," IEEE Eleventh Annual Applied Power Electronics Conference and Exposition, APEC'96 Vol. 2, pp. 977-983, 1996.

[13] Xunwei Zhou, "Low-Voltage High-Efficiency Fast Transient Voltage Regulator Modules", Ph.D. Dissertation, Virginia Polytechnic Inst. State Univ., Blackburg, 1999.

[14] O. Djekic and M. Brkovic, "Synchronous Rectifiers vs. Schottky Diodes in a Buck Topology for Low Voltage Applications," IEEE 28th Annual Power Electronics Specialists Conference, PESC'97 Record, Vol. 2, pp. 1374-1380, 1997.

[15] Art Brochschmidt, "Optimizing Distribution Bus Voltages," IEEE Thirteenth Annual Applied Power Electronics Conference and Exposition, APEC'98, Vol. 2, pp. 889-894, 1998.

[16] Yuri Panov and Milan M. Jovanovic, " Stability and Dynamic Performance of Current-Sharing Control for paralleled Voltage Regulator Modules," Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2001, APEC 2001, Volume: 2, Page(s): 765-771, 2001.

[17] Xunwei Zhou, Peng Xu, and Lee, F.C., " A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," IEEE Transactions on Power Electronics, Volume: 15 Issue: 6 Page(s): 1153-1162, Nov., 2000.

[18] Texas Instruments, "Designing Fast Response Synchronous Buck Regulators Using the TPS5210," Application Report, March 1999.

CHAPTER TWO

TECHNICAL REVIEW

2.1 Review of multiphase VRMs

Most of today's non-isolated Low-Voltage Regulator Modules (LVRMs) are buck derived such as the conventional buck, the synchronous buck and the Quasi-Square-Wave (QSW) buck [1-8]. While the isolated LVRMs are those such as symmetrical and asymmetrical half-bridge, active clamped forward, flyback forward and push-pull structures [9-12]. The secondary side of the isolated topology can have different schemes such as forward, center-tapped, or current-doubler as discussed in [12, 13].

The VRM and microprocessor systems are highly nonlinear and time varying. A high performance control loop is essential and requires extensive knowledge of converter behavior and load changes. In general, voltage PWM control, voltage hysteretic control, peak current control, average current control, and V^2 control are the most popular control methods [14].

Among the above-mentioned topologies and control methods, mainly the voltage hysteresis based synchronous buck converter is adapted in this dissertation.

2.1.1 Interleaved (Multiphase) Technique on a Buck Converter

It is well known, the current ripple depends on the inductor value, the larger the inductor, the smaller the current ripple. However, a large inductor does not only mean greater volume but also deteriorated dynamic response. The other method to reduce current ripple is to increase the switching frequency, unfortunately this will lower the efficiency due to switching loss. It must be also noted that adding large output capacitors to reduce the output voltage ripple is not practical since it will reduce the VRM power density.

The interleaved technique was introduced to reduce output ripple while maintaining transient performance and limiting inductor value [7, 14-18]. The essential principle of interleaved technique is to parallel switches and inductors between input voltage and output capacity. The reason for reducing the current ripple by interleaved technique is phase shifting among the different switches and the current delay they generate corresponding to the respective inductors. Obviously, output current is a summary of all branches and the total current ripple can be cancelled due to the phase shifting of each branch current. This is illustrated in Figure 2-1. In general, interleaved technique is tantamount to increasing switching frequency while the effective output inductor is reduced due to parallel.

There are many advantages for interleaved technology with N interleaved converters that include:

1) The output voltage ripple frequency is N times larger than switching frequency f_s of each individual converter in the interleaved VRM. Therefore, it reduces output ripple while maintaining high efficiency. This is because the switching frequency for power devices and inductors is only f_s.

2) The effective output inductor is N times smaller than each individual phase inductor which speeds the transient.

3) The total VRM output current is distributed into every individual phase which makes the VRM current carrying capability larger and reduces the conducting losses in power devices and inductors.

4) The dynamic performance is much better than the single-phase converter since the 2, 3, ...N branches can be turned on simultaneously for providing large slew rate current.

Interleaved technique is not limited in the buck converter, all the other converters like boost, flyback, push-pull, half bridge, full bridge, can use the interleaving technology for the same purpose. Actually, what need to do is duplicating switches, inductors or transformers, putting them in parallel and having a phase shift. In this dissertation, the adaptive digital controller is based on multiphase buck converters since this is the most popular topology of microprocessors' power supply in the industry.

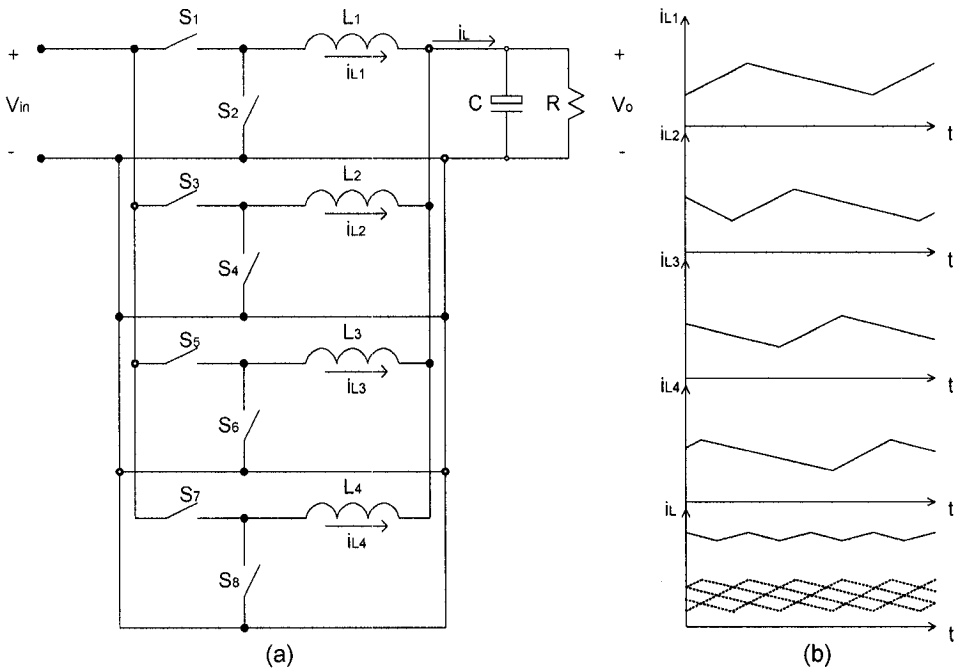


Figure 2-1: Multiphase buck converters and its output inductor currents
(a) Interleaved buck converter
(b) Current waveform of 4-phase interleave

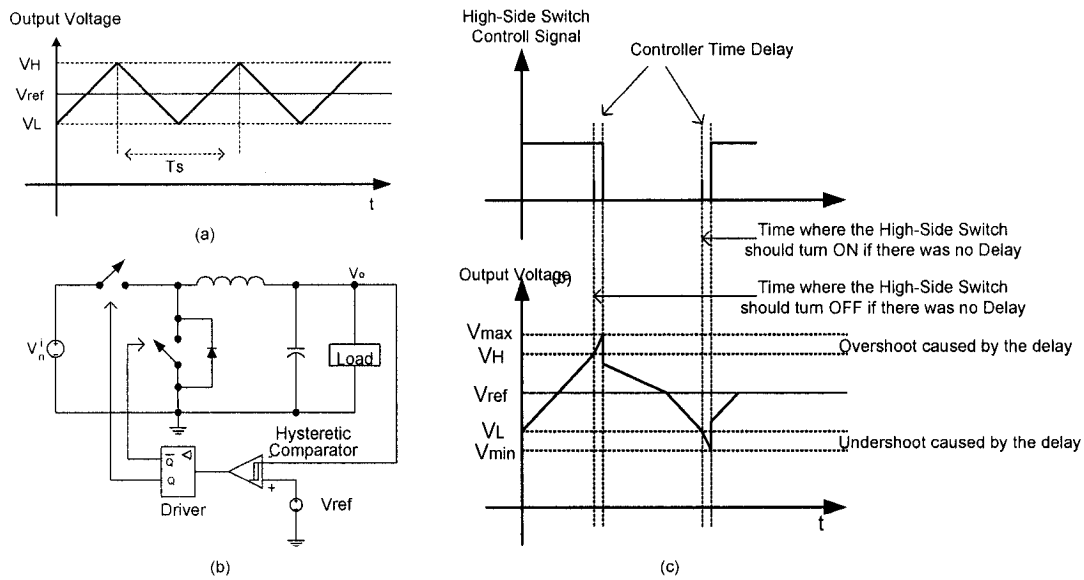


Figure 2-2: Voltage hysteretic control
(a) Theoretical hysteretic window
(b) Block diagram
(c) Actual output ripple waveform

2.1.2 Single-Phase Hysteretic Voltage-Mode Control

For a specific converter, there are many different control techniques to meet the output requirements. Choosing the most suitable one depends on the cost, physical size, logical complication, noise immunity, steady-state performance and dynamic response. The most popular control methods for interleaved converters are pulse width modification (PWM), peak current control, and voltage hysteretic control.

To control the output voltage ripple and limit it within a specific band centered at a reference voltage, the voltage hysteretic control is a good candidate [19]. It tracks the output voltage and keeps it between a maximum voltage (V_H) and a minimum voltage (V_L) as shown in Figure 2-2.(a).

Figure 2-2.(b) shows a simplified block diagram for a single-phase voltage-mode hysteretic controlled buck converter. The controller will turn-on the high-side switch and turn-off the low side switch if the output voltage drops below V_L, and it will turn-off the high-side switch and turn-on the low side switch if the output voltage exceeds V_H.

The feedback delay of the control loop generates an actual output voltage overshoot as shown in Figure 2-2.c. The extra small ripple caused by those delays must be considered in the design.

In addition to the advantage of controlling the ripple within a hysteretic window, it is also good because there is no need to consider loop compensation and the output voltage ripple becomes relatively independent of the output capacitor value. In fact, both the capacitor and the inductor values can now be selected more freely to satisfy only the transient requirements without taking into consideration the output voltage requirements since the operation of the hysteretic control can take care of it automatically. Also, the response of the controller is pretty fast since the switch control signals are derived directly from the output voltage ripple which allow the controller to respond within one switching cycle.

The digital controller in this dissertation is based on voltage hysteretic control. Due to the high current carrying in each mode, an adaptive current observer is designed for achieving current senseless control for high efficiency and small size purposes.

2.2 Review of Transient Improvement Circuits

For improving the dynamic performance of the VRM, two different kinds of methods have been presented [20-22]. One is to add a redundant circuit in parallel with the VRM, kicking in when load changes dramatically and kicking off at steady state; the other is focusing on the VRM itself, and speeds the transient by improving the control method.

ALL-ON and ALL-OFF control is one of the ideas for improving the control method. When it comes the fast transient, the load normally generates a voltage spike which is

sensed by the controller. If the voltage drops significantly, the controller will turn on all the high-side switches together to source more current. This is called ALL-ON control. If the voltage increases significantly, the controller will turn on all the low-side switches together to sink more current. This is so-called ALL-OFF control. This is a very popular method used in industry.

The other kind of solution is the redundant control. It focuses on adding an extra stage at the output of the VRM to improve the fast transient response. The typical structure is shown in Figure 2-3. The transient compensation circuit normally only operates at fast transient, not at steady state mode or slow transient mode.

There are two different dominant control methods as shown in Figure 2-4. The current regulator type compensator is used to generate a high *di/dt* current at transient to compensate the high current slew rate load changes. It only works when the *di/dt* of the load current is larger than the reference value. It stops after voltage recovery. The voltage regulator type compensator works like a linear regulator with voltage hysteresis. When the output voltage value is not in the hysteresis window, the linear regulator is triggered.

However, the main reasons of generating voltage drops at fast transient are caused by: 1) propagation delay compared with the huge *di/dt*; 2) controller delay; 3) inductor response delay. Therefore, transformer or inductor type compensators are not as effective as voltage regulator type compensators. Even the latter is not fast enough to respond to the microprocessor's load changes due to the propagation delay of the system board.

An active compensator proposed in this dissertation gives a voltage regulator type compensator somehow similar to the one in Figure 2-4 (b). But it monitors the voltage drop of the CPU core voltage rather than setting a hysteretic window for it. Also, it provides enough voltage drop cross the socket inductance and trace inductance and resistance, therefore it compensates the transient voltage spike by generating a large transient compensation current.

2.3 Review of ON-TIME Control

ON-TIME control is widely used in rectifiers, converters and inverters. It is different from PWM control since its switching frequency is not fixed like in PWM control. The controller regulates the ON-TIME duration of the switching circle with a specified rule, and the OFF-TIME of the circle is normally decided on the output value like output voltage [23-27]. Although it is variable frequency control, it is not the same as hysteretic control. The latter only set rule for output variation, and it does not take the ON-TIME, OFF-TIME duration and the switching frequency into account. Therefore, even the designer himself can only give a wide range of the frequency variation, and hardly to tell the ON-TIME duration. With the changes of the power switches, inductors, capacitors and loads, the frequency and ON-TIME duration will deviate. In this dissertation, we can see the advantage of the ON-TIME control, although it is variable frequency, the ON-TIME duration is known and regulated. It does not shift with the component or load changes.

Figure 2-5 shows the comparison of the three different kinds of controls. Figure 2-5 (c) shows a fixed ON-TIME control. However, the ON-TIME duration is not necessarily constant. It could be proportional to some control parameters or some system variables which is defined by the designer. Normal, the ON-TIME information is decided by the system behaviors, for example, the input voltage, reference voltage, output current, load current slew rate, temperature, phase difference, etc.

A buck converter with constant ON-TIME control is shown in Figure 2-6. When output voltage is lower than pre-determined value, the high-side switch is turned on. It is turned off after a preset period of Ton which can be achieved by a delay circuit. The output ripple and switching frequency, therefore, is determined by the Ton delay. The longer the Ton, the larger the output ripple and the lower the switching frequency.

ON-TIME control was used on VRM along with PWM control to improve efficiency [15]. At regular operation, PWM is used for low EMI purposes, while constant ON-TIME control is used for light load to improve efficiency. This kind of controller has a load current sensor to switch between these two control methods. At ON-TIME control, the output ripple is slightly larger than PWM control, while the switching frequency is smaller, so it greatly reduces switching loss, especially for multiphase converters.

An average duty ratio model for DC-DC converters employing constant ON-TIME control is derived in [25]. The conceptual circuit diagram for average duty ratio model is

given in Figure 2-7. And the final model is given in Equation (2-1) where *Ri* is the DC gain of the current sensing network and all the other variables are defined in Figure 2-7.

$$
\begin{aligned}
d &= \frac{d_p + d_r}{2} \\
d_p &= \frac{v_c - R_i i_L + \sqrt{(R_i i_L - v_c)^2 + (m_1+m_2)m_2}}{m_1+m_2} \\
d_r &= \frac{v_c - R_i i_L + \sqrt{(R_i i_L - v_c)^2 + (m_1+m_2)(m_2 + 2\delta v_c)}}{m_1+m_2} \\
m_1 &= \frac{R_i(v_g - v_o)}{L} T_{on} \\
m_2 &= \frac{R_i v_o}{L} T_{on} \\
\delta v_c &= \delta v_{ct} T_{on}
\end{aligned}
\tag{2-1}
$$

In this dissertation, the concept in Figure 2-6 is used and expended to multiphase VRMs for laptop usage. For this usage, the input voltage is changing in a wide range and the constant ON-TINE is expended to proportional ON-TIME with the definition of ON-TIME is proportional to the input voltage.

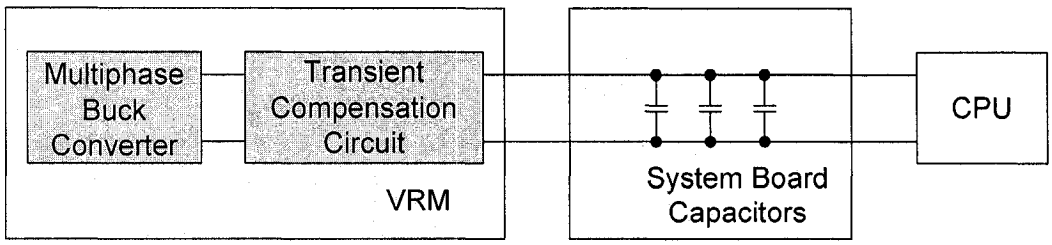
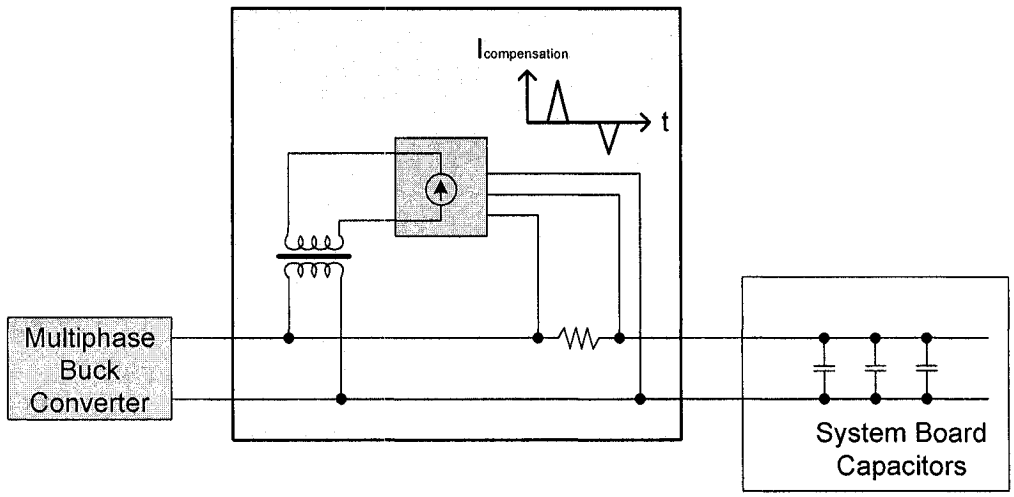
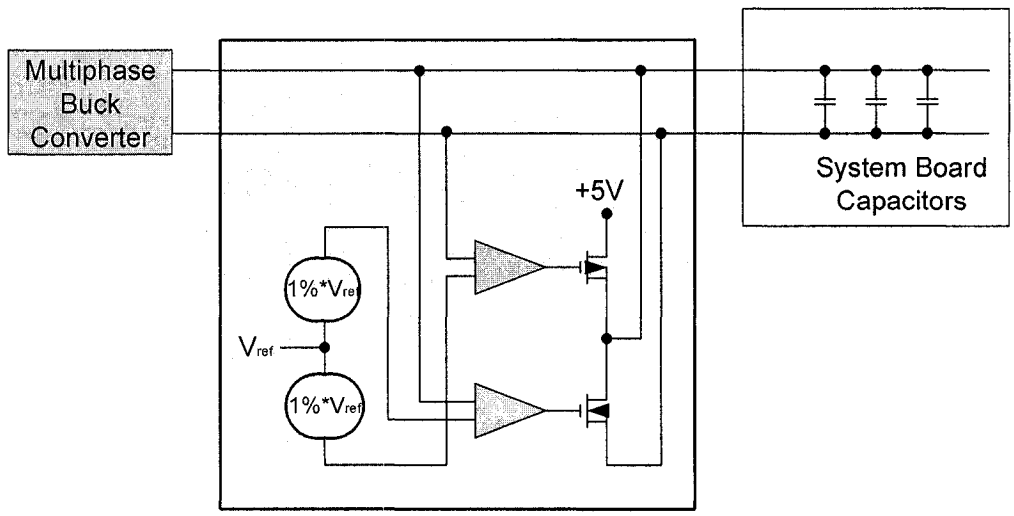


Figure 2-3: Fast transient compensation circuit



(a)



(b)

Figure 2-4: Fast transient compensation
(a) Current regulator type
(b) Voltage regulator type

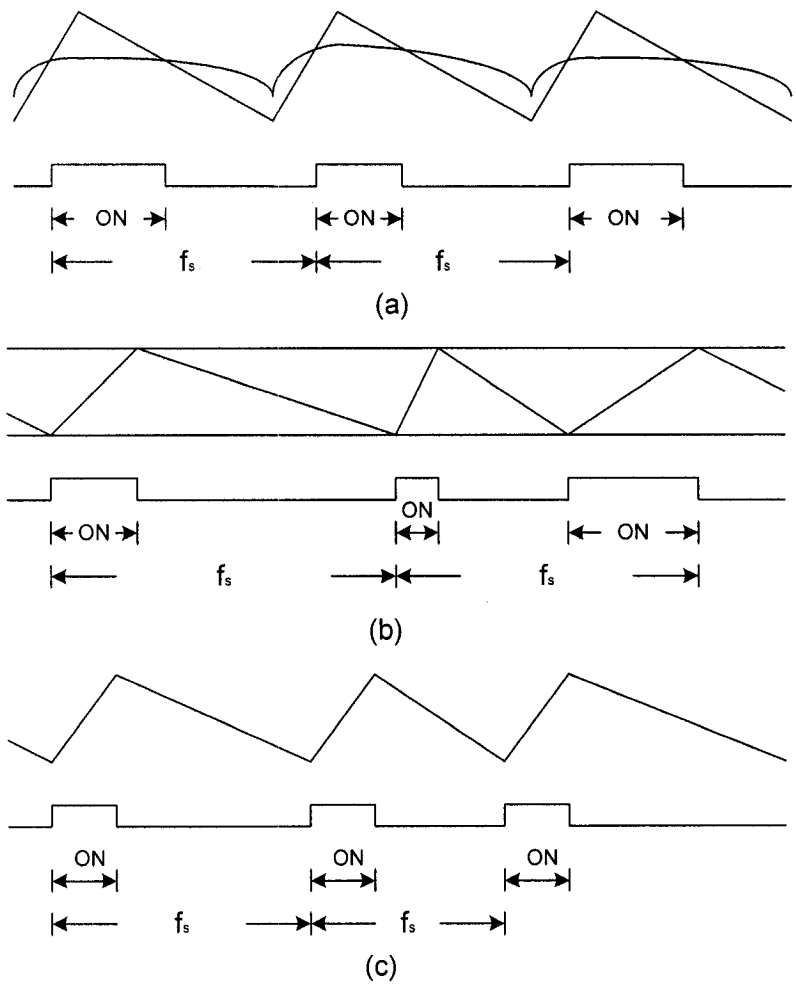


Figure 2-5: Comparisons of PWM, hysteretic and ON-TIME control
(a) PWM control
(b) Hysteretic control
(c) Constant ON-TIME control

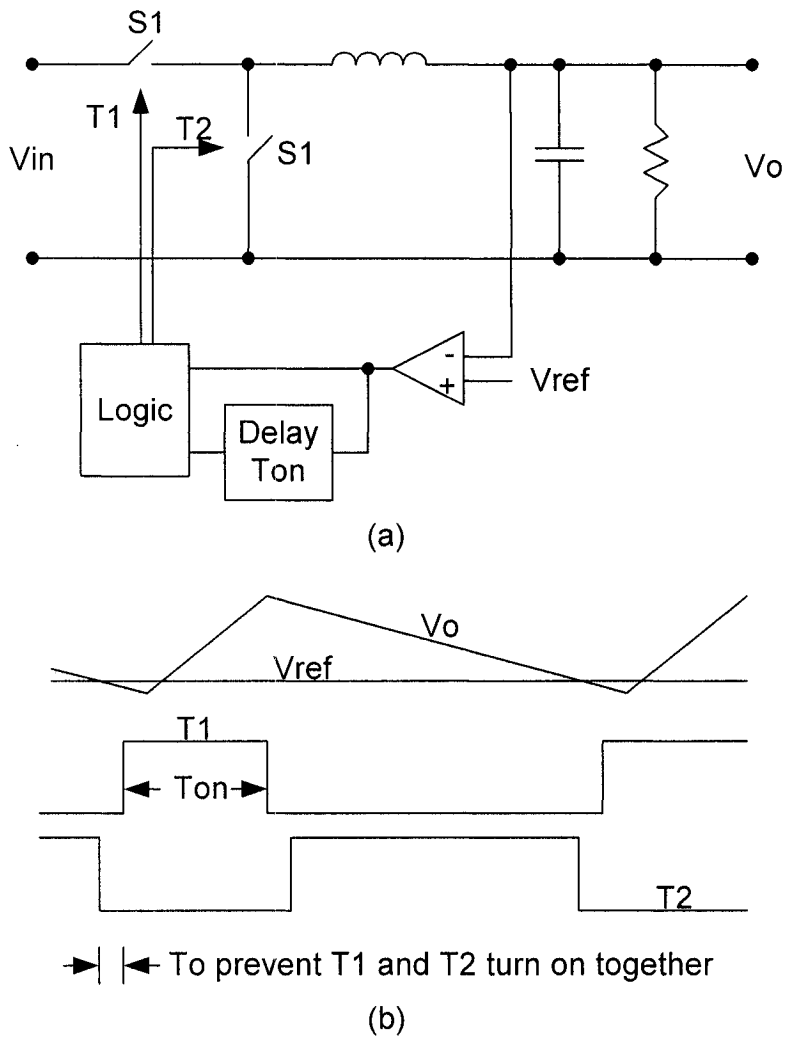


Figure 2-6: Constant ON-TIME control
(a) Power stage and control scheme
(b) Output waveform and switch driving signals

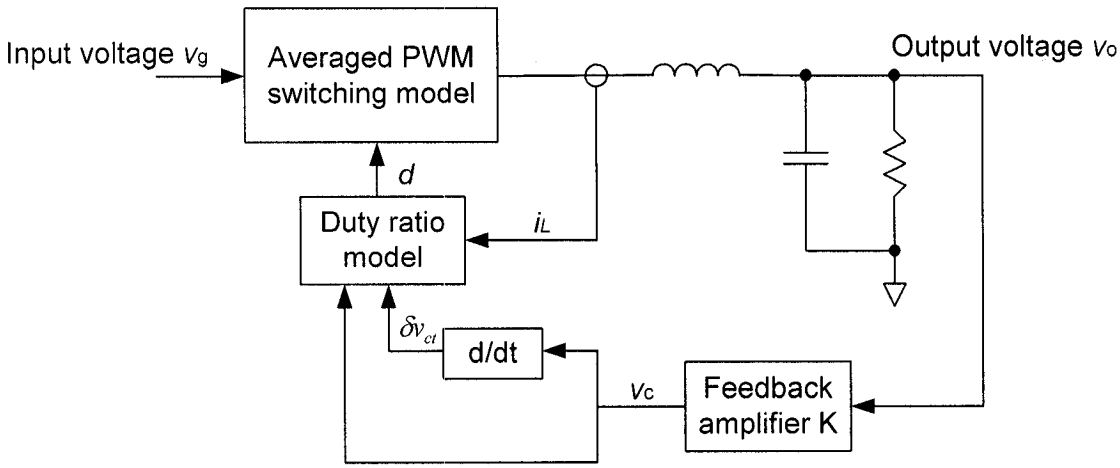


Figure 2-7: Conceptual circuit diagram for duty ratio model

References

[1] Xu, P.; Wei, J.; Lee, F.C.; "The active-clamp couple-buck converter-a novel high efficiency voltage regulator modules", Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE, Volume: 1, 4-8 March 2001 Page(s): 252 -257 vol.1

[2] Kaiwei Yao; Yu Meng; Lee, F.C.; "Control bandwidth and transient response of buck converters", Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual, Volume: 1 , 23-27 June 2002 Page(s): 137 -142 vol.1

[3] Peng Xu; Jia Wei; Lee, F.C.; "Multiphase coupled-buck converter-a novel high efficient 12 V voltage regulator module", Power Electronics, IEEE Transactions on, Volume: 18 Issue: 1, Jan. 2003 Page(s): 74 –82

[4] Pit-Leong Wong; Wu, Q.; Peng Xu; Bo Yang; Lee, F.C.; "Investigating coupling inductors in the interleaving QSW VRM", Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE, Volume: 2, 6-10 Feb. 2000 Page(s): 973 -978 vol.2

[5] Xunwei Zhou; Donati, M.; Amoroso, L.; Lee, F.C.; "Improve light load efficiency for synchronous rectifier buck converter", Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual, Volume: 1, 14-18 March 1999 Page(s): 295 -302 vol.1

[6] Deuty, S.; "Optimizing transistor performance in synchronous rectifier buck converters", Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE, Volume: 2, 6-10 Feb. 2000 Page(s): 675 -678 vol.2

[7] Abu Qahouq, J.A.; Jia Luo; Batarseh, I.; "Voltage regulator module with interleaved synchronous buck converters and novel voltage-mode hysteretic control", Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on, Volume: 2 , 14-17 Aug. 2001 Page(s): 972 -975 vol.2

[8] Panov, Y.; Jovanovic, M.M.; "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules", Power Electronics, IEEE Transactions on, Volume: 16 Issue: 6, Nov. 2001 Page(s): 776 –783

[9] Kaiwei Yao; Yu Meng; Lee, F.C.; "A novel winding coupled-buck converter for high-frequency, high step-down DC/DC conversion", Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual, Volume: 2, 23-27 June 2002 Page(s): 651 -656 vol.2

[10] Mao Ye; Peng Xu; Bo Yang; Lee, F.C.; "Investigation of topology candidates for 48 V VRM", Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE, Volume: 2, 10-14 March 2002 Page(s): 699 -705 vol.2

[11] Xu, P.; Lee, F.C.; "Design of high-input voltage regulator modules with a novel integrated magnetics", Applied Power Electronics Conference and Exposition, 2001.

APEC 2001. Sixteenth Annual IEEE, Volume: 1, 4-8 March 2001 Page(s): 262 -267 vol.1

[12] Jia Wei; Peng Xu; Lee, F.C.; "A high efficiency topology for 12 V VRM-push-pull buck and its integrated magnetics implementations", Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE, Volume: 2, 10-14 March 2002 Page(s): 679 -685 vol.2

[13] Peng Xu; Mao Ye; Lee, F.C.; "Single magnetic push-pull forward converter featuring built-in input filter and coupled-inductor current doubler for 48 V VRM", Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE, Volume: 2 , 10-14 March 2002 Page(s): 843 -849 vol.2

[14] Texas Instruments, "Designing Fast Response Synchronous Buck Regulators Using the TPS5210," Application Report, March 1999.

[15] Xunwei Zhou; Xu Peng; Lee, F.C.; "A high power density, high efficiency and fast transient voltage regulator module with a novel current sensing and current sharing technique", Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual, Volume: 1, 14-18 March 1999 Page(s): 289 -294 vol.1

[16] Xunwei Zhou; Peng Xu; Lee, F.C.; "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications", Power Electronics, IEEE Transactions on , Volume: 15 Issue: 6 , Nov 2000 Page(s): 1153 –1162

[17] Capponi, G.; Minneci, L.; Librizzi, F.; Scalia, P.; "Multiphase voltage regulator module with transient step changing phases", Power System Technology, 2000. Proceedings. PowerCon 2000. International Conference on, Volume: 1, 4-7 Dec. 2000 Page(s): 463 -467 vol.1

[18] Xiaoguo Liang; Jian Wei; Xinbo Ruan; "An interleaved three-level forward converter -- Suitable for the application of voltage regulator module (VRM)", Power Electronics Specialist, PESC. 2003 IEEE 34th Annual Conferece on, Volume: 1, June 15-19, 2003 Page(s): 127 –131

[19] Wei Gu; Weihong Qiu; Wenkai Wu; Batarseh, I.; "A multiphase DC/DC converter with hysteretic voltage control and current sharing", Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE, Volume: 2, 10-14 March 2002 Page(s): 670 -674 vol.2

[20] Hoffman, K.; Ledwich, G.; "Resonant link topologies for fast power system transient compensation", Advances in Power System Control, Operation and Management, 1993. APSCOM-93, 2nd International Conference on, 7-10 Dec 1993 Page(s): 108 -113 vol.1

[21] Peng, F.Z.; Akagi, H.; Nabae, A.; "Compensation characteristics of the combined system of shunt passive and series active filters", Industry Applications Society Annual Meeting, 1989, Conference Record of the 1989 IEEE , 1-5 Oct. 1989 Page(s): 959 -966 vol.1

[22] Bussmann, M.; Langmann, U.; "Active compensation of interconnection losses for multi-GHz clock distribution networks", Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, Volume: 39 Issue: 11, Nov. 1992 Page(s): 790 –798

[23] Suntio, T.; "Small-signal modeling of switched-mode converters under direct-on-time control-a unified approach", IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the], Volume: 1, 5-8 Nov. 2002 Page(s): 479 -484 vol.1

[24] Chen, D.S.; Lai, J.S.; "A study of power correction boost converter operating at CCM-DCM mode", Southeastcon '93, Proceedings., IEEE , 4-7 April 1993 Page(s): 6

[25] Sung-Soo Hong; Byungcho Choi; "Technique for developing averaged duty ratio model for DC-DC converters employing constant on-time control", electronics Letters, Volume: 36 Issue: 5, 2 March 2000 Page(s): 397 –399

[26] Lippincott, A.C.; Nelms, R.M.; Garbi, M.; Strickland, E.; "A series resonant converter with constant on-time control for capacitor charging applications", Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990, Fifth Annual, 11-16 March 1990 Page(s): 147 –154

[27] Ridley, R.B.; "A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM", Power Electronics Specialists Conference, 1990. PESC '90 Record, 21st Annual IEEE, 11-14 June 1990 Page(s): 382 –389

CHAPTER THREE

ACTIVE CURRENT COMPENSATION FOR LOW-VOLTAGE HIGH CURRENT FAST TRANSIENT VRMS

3.1 Introduction

The recent generation of microprocessors work at a low operating voltage, high current, and a high current slew rate. For example, Intel's Pentium 4 2.8G processor operates between *1.34V~1.42V @ 55.9A,* and *350A/μs* of current slew rate [1, 2]. To achieve such a high slew rate, a large capacitance is typically mounted on the microprocessor package and system board to absorb the voltage spike in load-change transient. Figure 3-1 shows an equivalent power delivery Pentium 4 model for transient response provided by Intel [1]. Under any transients, this system design can guarantee to limit the voltage variation within *4%*. The stringent transients of full-load to sleep mode and sleep mode to full load are shown in Figure 3-2. Here, *Icpu* is the total current flowing through the CPU.

The next generation of microprocessors will work at lower operating voltages, higher current and higher current slew rate as mentioned in chapter one. Therefore, more capacitance at VRM output is required. Unfortunately, the space in a microprocessor package is very limited, making it difficult to add more capacitors. Furthermore,

increased motherboard capacitance has little effect to limit the voltage spike in a fast transient due to the current response delay of large socket inductance and the ESL, ESR of capacitors. A simulation result is provided in Figure 3-3 to illustrate how voltage spikes could potentially reach *10%* above the nominal value. Even all the capacitances are doubled, the total voltage variation still reaches *12%* and cannot meet the stringent requirement. It should be noted that the steady-state voltage difference in Figure 3-3 is generated by voltage drops on interconnect resistance due to its high conduction current because the simulation is done in open loop.

A novel dynamic current compensator is presented here to minimize the voltage spike without additional capacitors. Instead, the capacitance on system board could reduce down to *2/3* of the present level; and the capacitance in microprocessor package can be decreased to approximate 3/4.

Another advantage of this compensator is its capability to compensate the transient response delay caused by large socket inductance under high current slew rate. Therefore, it provides for more freedom in package design.

Since this compensator works like a discrete linear regulator, by being active only during large load-change transients; the average power dissipation is very low. Hence, efficiency is reduced only a small amount.

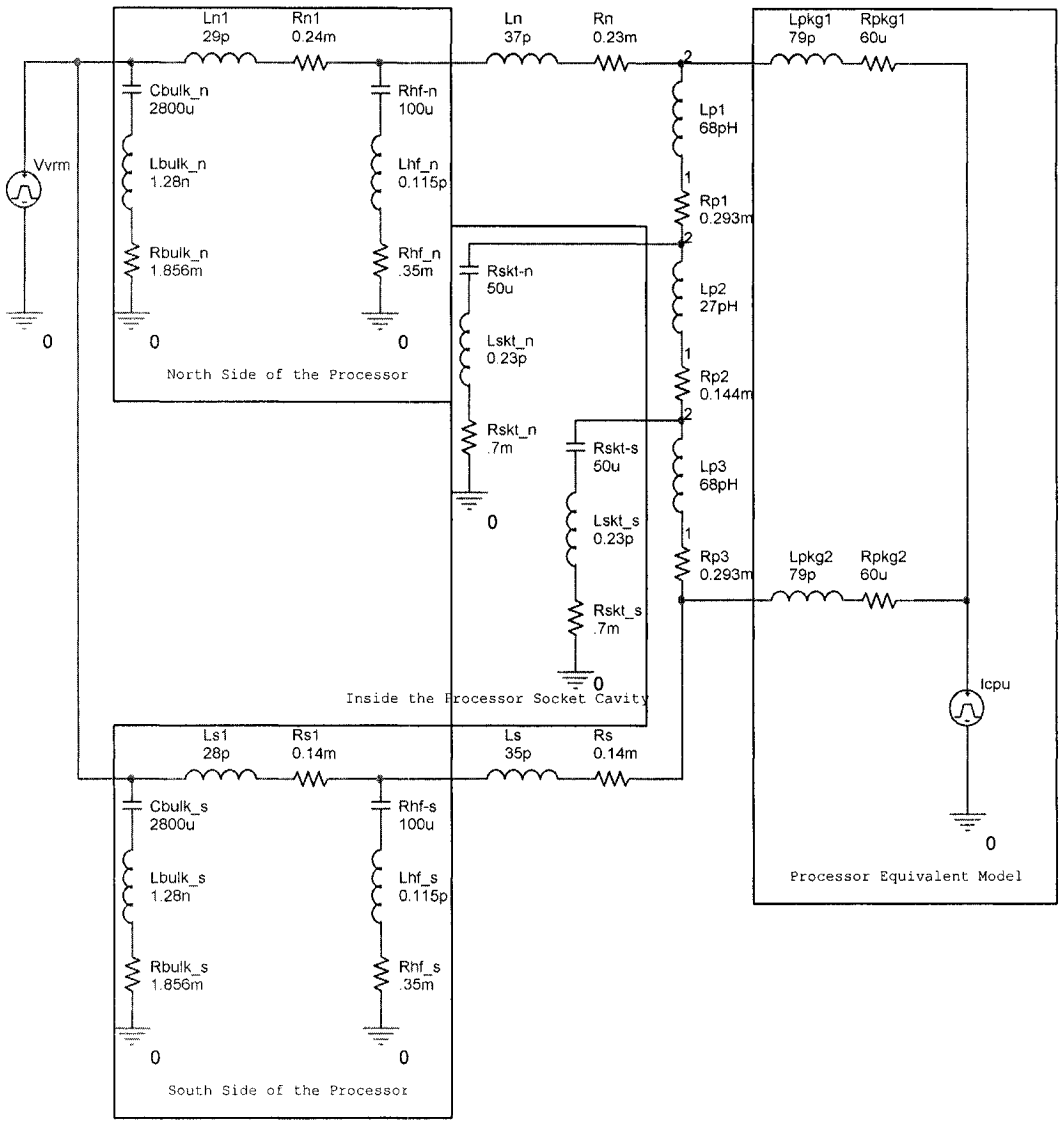


Figure 3-1: Power delivery model for transient response for Intel Pentium 4 processor

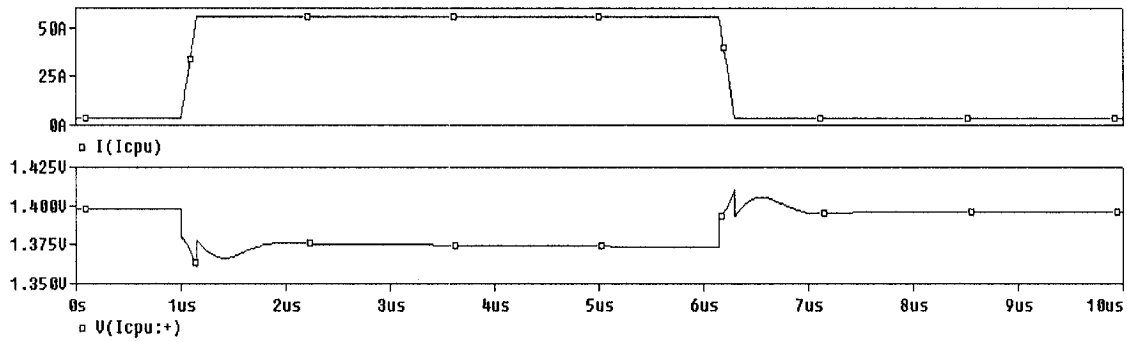


Figure 3-2: V_{cc} of processor when I_{cpu} changes from *5A* to *56A @ di/dt=350A/us*
Upper: Microprocessor load change
Lower: *Vcc* of microprocessor

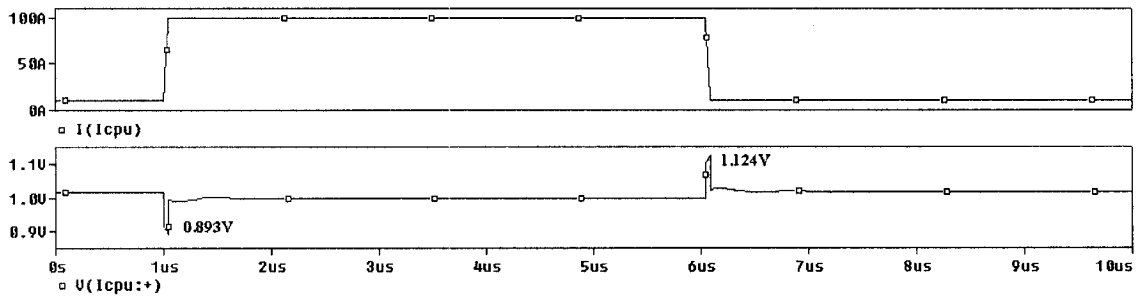


Figure 3-3: V_{cc} of microprocessor when I_{cpu} changes from *10A* to *100A @di/dt=2000A/us*
Upper: Microprocessor load change
Upper: Microprocessor load change

3.2 Transient Response Delay in a Fast Current Slew Rate System

High voltage spikes are caused during high slew rate load change because of the current response delay of socket inductance and the voltage drop across ESR and ESL of the capacitors.

For the high current slew rate model, the capacitor should be considered as a series of RLC circuits whose total voltage can be expressed as,

$$v_{c,total} = L_{ESL}\frac{di_c}{dt} + r_{ESR}i_c + v_c \qquad (3\text{-}1)$$

where, L_{ESL} and r_{ESR} are equivalent series inductance and resistance, and i_c and v_c are the current and voltage of the ideal capacity. To provide a current slew rate at *2A/ns*, the voltage drops across ESL and ESR of high-frequency capacitors will reach tens of millivolt level while the voltage drops across ESL of bulk capacitors will be larger than *1V*. Considering the operating voltage is *1V*, the actual current slew rate provided by capacitors is much smaller than desired so the voltage spike is generated. Therefore, few advantages can be achieved by paralleling more capacitors on system board.

Another reason for the transient response delay is the large connector and socket parasitic inductance as shown in Figure 3-1. If *2A/ns* of current slew rate is assumed through connection inductance, it can only by achieved by a *150mV* voltage drop, as calculated in Equation (3-2).

$$V_L = L_{skt}\frac{di_c}{dt} = 75pH \times 2A/ns = 150mV \tag{3-2}$$

The *150mV* voltage drop compared for a *1V* nominal output is significant and exceeds the required tolerance given in Figure 1-1. In Figure 3-1, the trace inductance is only *20~30pH*, while the socket inductance is about *60~80pH*. The challenge is that the socket inductance is very difficult to decrease and the VRM and capacitors have already been put as close as possible to the processor [3-6].

Based on the two reasons mentioned above, there is almost no effect on the voltage spike during such a fast load-change transient by simply adding more capacitors on system board. This is verified in simulation by doubling all the system capacitance mentioned before.

Hence, a novel compensation circuit will be introduced to increase the voltage drop across socket and trace inductances so that the current slew rate is not a limitation in fast transient response.

3.3 Presented Active Transient Current Compensator

An active transient current compensator is presented here to speed the transient response. The presented compensator is inserted between the microprocessor package and the on board capacitors. The new model is illustrated in Figure 3-4. The trigger signal of the

compensator comes from a built-in voltage monitor in the microprocessor package. Since the output high slew rate current in the compensator only appears in load-change transient, it does not influence VRM steady-state operation.

The details of the new topology are described in Figures 3-5 and Figure 3-6. The concept of this topology is similar to electrical static discharge (ESD) protection technique [7, 8], however the energy here is transferred bi-directionally. When the microprocessor operation changes from sleep mode to full-load mode, the compensator provides high slew rate current quickly. When the microprocessor operation changes from full-load mode to sleep mode, the compensator will absorb the extra current provided by VRM. Ideally, if energy flowing between VRM and the microprocessor is balanced, there will be no voltage spike in load-change transient.

What distinguishes this topology from any other fast transient VRMs [9, 10] is its fast response and the immunity to current delay caused by large socket inductance. That is because this compensation is not mounted tightly at the output of the VRMs, instead the voltage sensor is located at the Vcc of the CPU side. Therefore the linear regulator can provide sufficient voltage drops across the socket and trace inductance. Hence, it generates large slew rate current to minimize voltage spikes during transient. For other load-change corrections [9, 10], the compensators are combined with VRM and make the compensation impossible since they did not catch the main reason causing the current delay: the ESL and ESR of capacitors and the inductors of the socket and trace.

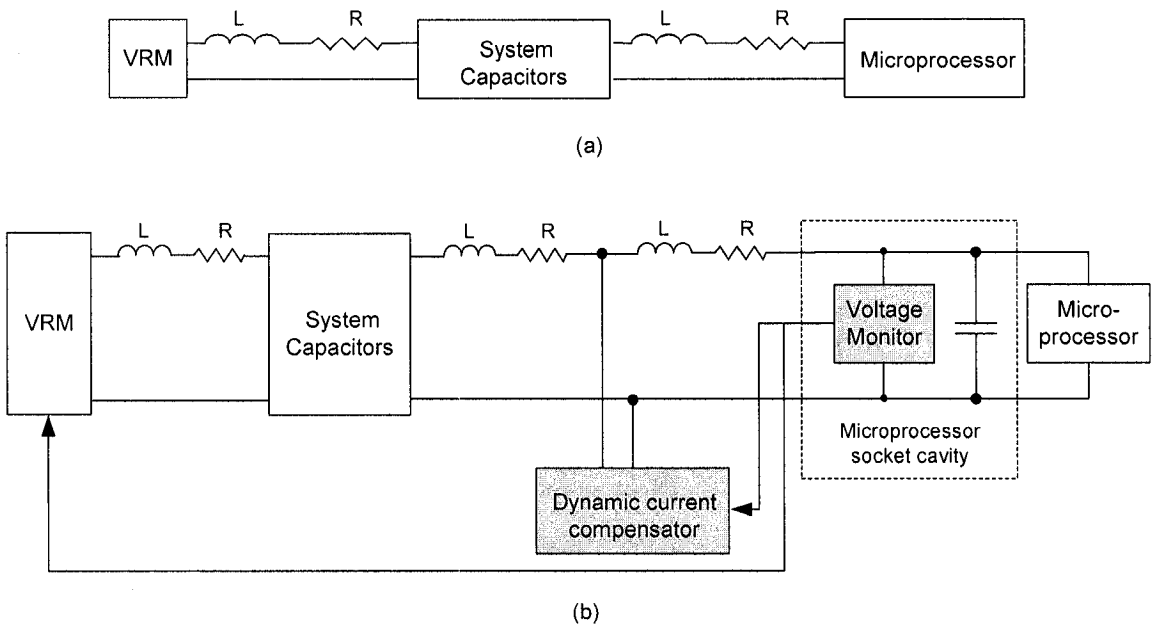


Figure 3-4: The different power delivery models for VRMs
(a) Present power delivery model
(b) Novel power delivery model

3.3.1. Voltage Monitor

The voltage monitor is mounted inside the socket cavity and very close to the microprocessor's *Vcc* pin so it can monitor voltage variation in no time. The whole monitor is composed of two parts as shown in Figure 3-5. One is for voltage undershoot; the other is for voltage overshoot. These two parts have the same circuit but different biasing values.

The function of the voltage monitor is to sense the core voltage change of the microprocessor by R_m and C_m. These two values with matching biasing V_{GS} value of Q1 can set voltage sensitivity and output pulse duration. Q2 circuit transfers the Q1 output into pulse output as shown in Figure 3-5 (b).

The input and output relationship of the voltage monitor is shown in Figure 3-5 (c). When the load changes from sleep mode to full-load mode, current increases and voltage decreases so undershoot circuit has output and vice versa.

Another function of the voltage monitor is to inform the VRM controller that the load-change transient has occurred so that the controller can make the interleaved VRM to operate at "ALL-ON" or "ALL-OFF" mode. Since there is almost no time delay for this monitor, it can improve VRM transient response as illustrated later.

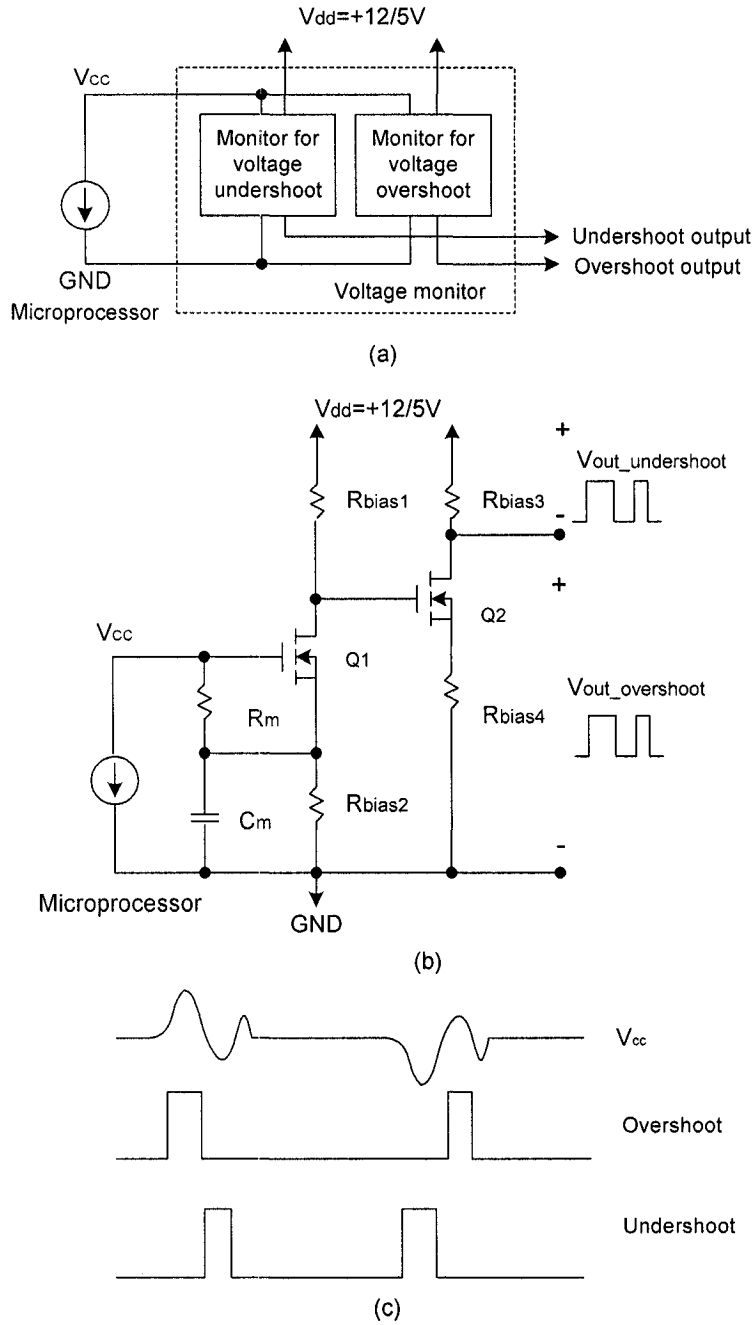


Figure 3-5: Voltage monitor
(a) Block diagram of voltage monitor
(b) Voltage monitor schematics (different biasing for undershoot and overshoot)
(c) Voltage monitor output

3.3.2 Active Transient Current Compensator

The transient current compensator is shown in Figure 3-6. The compensator is mounted on the motherboard very close to the microprocessor package. The energy comes from the *+5V/12V* power supply on the motherboard and low ESL and ESR capacity is mounted beside it.

As shown in Figure 3-6(b), the compensator is composed of one P-type and one N-type MOSFET. $R_{current\_limit}$ is optional and can be used to adjust injection current. When the load changes from sleep mode to full-load mode, P-FET is triggered by the undershoot output so current flows through PFET, $R_{current\_limit}$, $L_{package}$, $R_{package}$ to microprocessor package. Since the voltage drop across $L_{package}$ is large, current slew rate can be high enough to meet the load requirement. Therefore, the current change in the load is compensated so the voltage spike is minimized.

The current compensator works like a linear regulator. The regulation point is core voltage of the CPU, other than the VRM output end. Also, if the voltage changes are not large enough, the compensator circuit will not implement and no power is wasted during the stead state operation

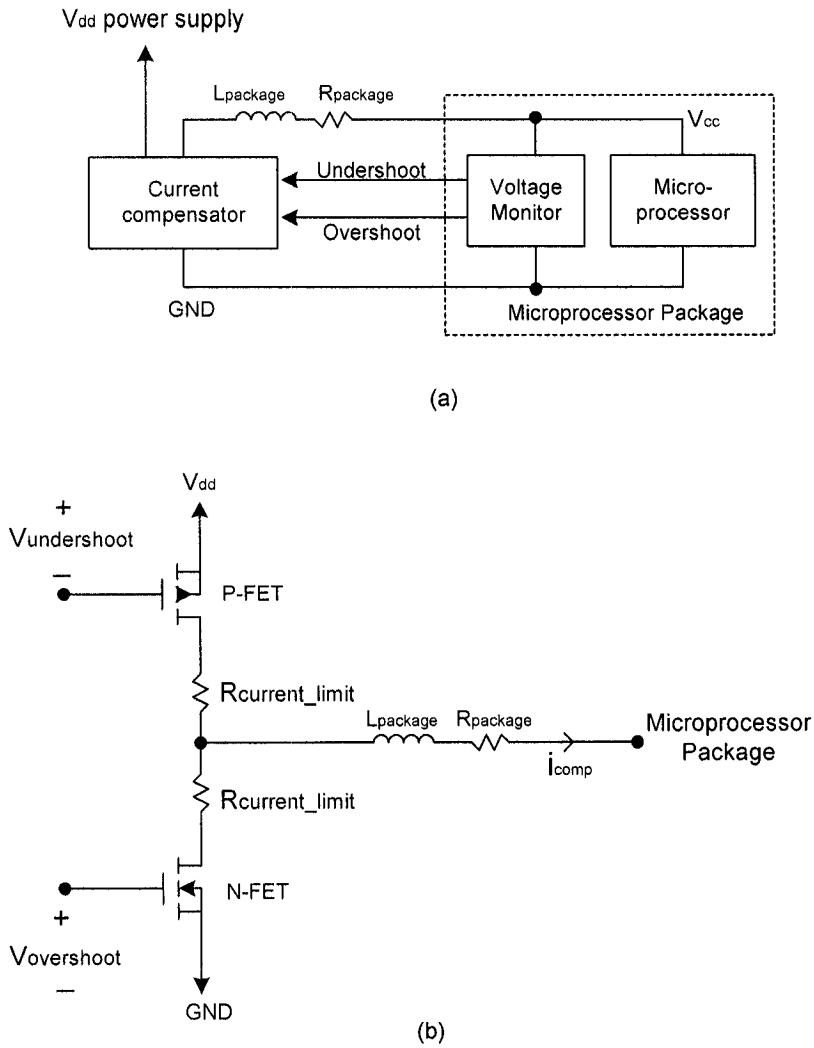


Figure 3-6: Active transient current compensator
(a) Block diagram of active transient current compensator
(b) Schematics

3.3.3 Complete Schematics for the Simulation

ASMC 0.8 micro CMOS process technology, C08DPDM is used to design the voltage monitor. The device specifications are listed in Table 3.1. Full schematics of the voltage monitor, compensator and power stage are given in Figure 3-7.

A top view of the voltage monitor IC chip and a typical application circuit are given in Figure 3-8 and Figure 3-9. Here, two input resistors and capacitors are moved out of the IC chip to provide more flexibility for frequency response. A layout of the undershoot circuit for the structure is shown in Figure 3-10. The overshoot circuit is symmetric with difference W/L scale.

Table 3.1: Device Specification of 0.8 micro CMOS Process

Device	Parameter	Specification			
		Min.	Average	Max.	Unit
	Vto_N	0.60	0.70	0.8	*V*
W/L 20/0.8	Isat_N	300	400	500	*uA/m*
N-Channel	BVdb_N	9	10	-	*V*
	Leff_N	0.65	0.75	0.85	*m*
	Vto_P	-0.8	-0.9	-1.0	*V*
W/L 20/0.8	Isat_P	-120	-160	-200	*uA/m*
N-Channel	BVdb_P	-9	-12	-	*V*
	Leff_P	-0.65	-0.75	-0.85	*m*

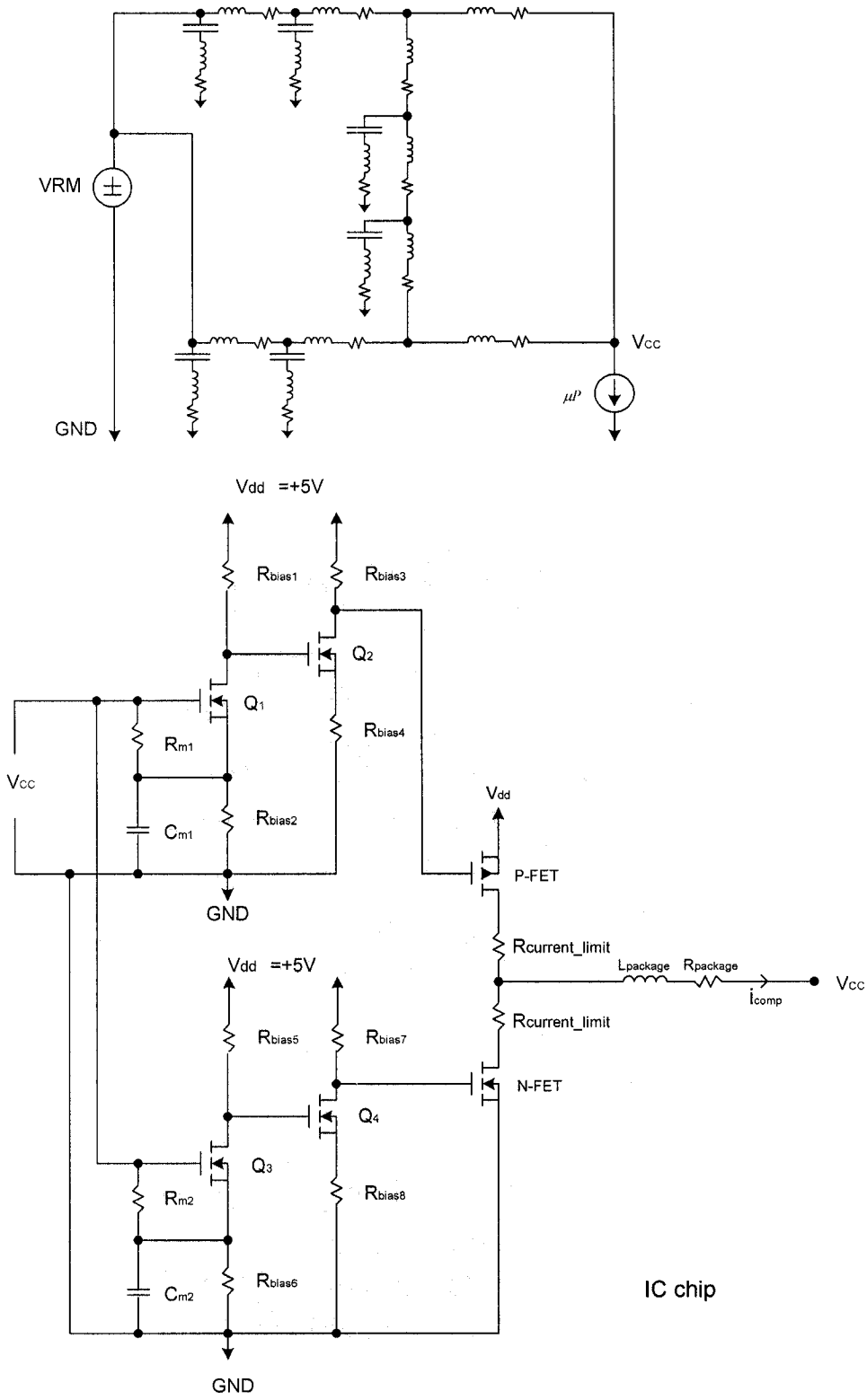


Figure 3-7: Schematics

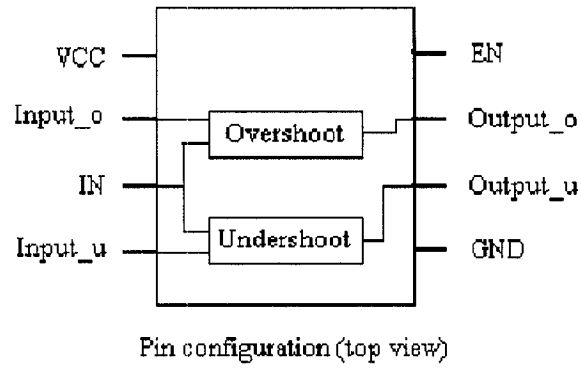


Figure 3-8: Pin configuration of the voltage monitor

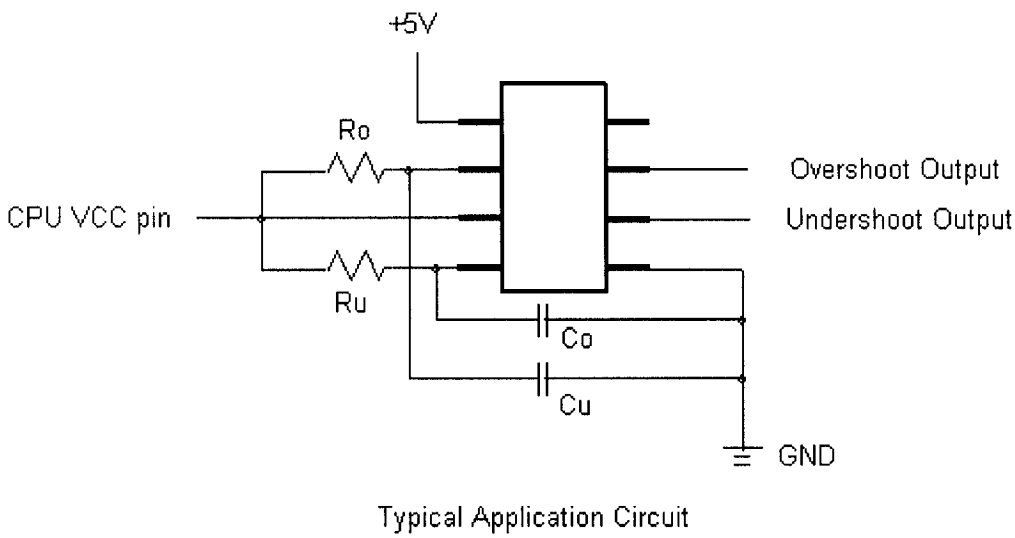


Figure 3-9: Typical application circuit of voltage monitor

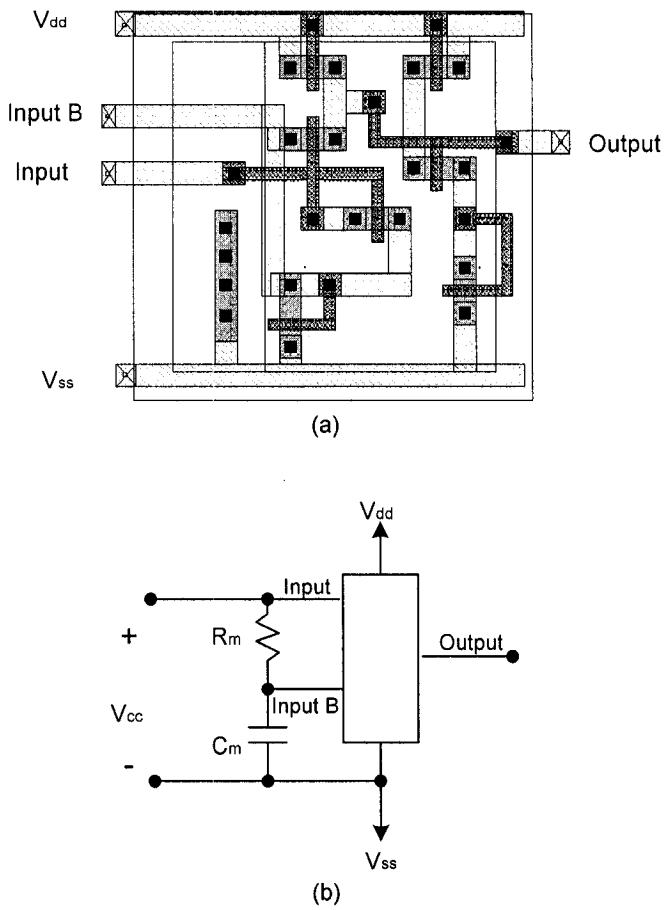


Figure 3-10: Voltage monitor layout and application circuit
(a) Layout for voltage monitor integrated chip
(b) Connection

3.4 Simulation Results

Simulation results for transient current compensation are shown in Figure 3-12. It is shown that the microprocessor operates at *1V* of V_{cc}, *100A* of I_{cc}, and *2A/ns* of current slew rate. All parasitic component values are the same as those in Figure 3-1 except package capacitance decreased to *3/4* of the present value and system capacitance reduced down to *2/3* of the present level. The top waveform in Figure 3-11 is the compensator's output current. It generates only in load-change transient. The bottom waveform is V_{cc} voltage of microprocessor. The total voltage variation is limited to *2.3%* These values are much smaller than those in Figure 3-3.

More data when microprocessor operates from sleep mode to active mode and load change within active modes are provided in Table 3-2 and Table 3-3 to illustrate the behavior of the compensator.

From Tables 3.2 and 3.3 we can see that the total voltage variation could be limited to a very small value, less than 4% of the nominal value. However, the smaller the transient voltage variation is, the longer the transient duration will be. It also makes the compensator operate more frequently and may cause instability.

When we decrease the values of capacitor C_m, the voltage monitor will not be so sensitive and it compensates less. Therefore, a tradeoff is always made by choosing the desired

voltage variation and the compensator's operating duration. Table 3.4 shows the compensation response versus capacitor value C_m. It is clear that the transient duration reduced (less compensation) when C_m decreased and the voltage variation increased.

Another consideration for the transient compensator is its stability, determined by the compensation for all the current change frequencies. If the compensator operates whenever the current changes, even when the voltage variation is very small, then the system will be unstable. The design target of the compensator is to compensate high current slew rate load changes not all load changes. Therefore, a minimum response value of the current slew rate should be set so that the compensator does not work when load change is slower than the critical value.

As discussed before, this can be adjusted by changing C_m, the voltage ratio of the two-stage amplifier. Table 3.5 is an example to show that the compensator only responds when current slew rate is higher than the specific value. The operating area for this compensator is above the curve. This is reasonable because the VRM could handle *50A/us* current slew rate and the decoupling capacitors on system board can also provide some extra *di/dt* currents. Obviously, the compensator is only on duty of high current slew rate range.

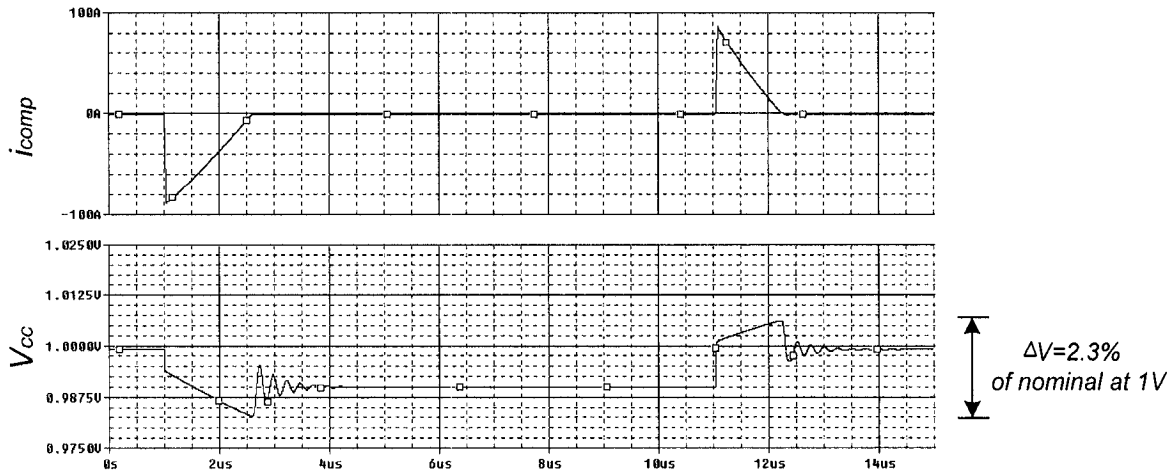


Figure 3-11: Simulation results after transient current compensation @V_{cc}=*1V*, I_{max}=*100A*, and current slew rate=*2A/ns* (C_m=*200n*)

Table 3.2: Compensation Result when Microprocessor Operates from Sleep Mode to Active Mode @ *2A/ns* Current Slew Rate and *1V* V_{cc} (C_m=*100n*)

Load change *(A)*	i_{comp} *(A)*	Transient time *(μs)*	ΔV_{cc}
10⇔100	88.1	2.55	3.2%
10⇔90	83.2	2.36	3.1%
10⇔70	58.2	1.5	2.4%
10⇔50	38.4	0.93	1.9%
10⇔30	18.8	0.4	1.8%

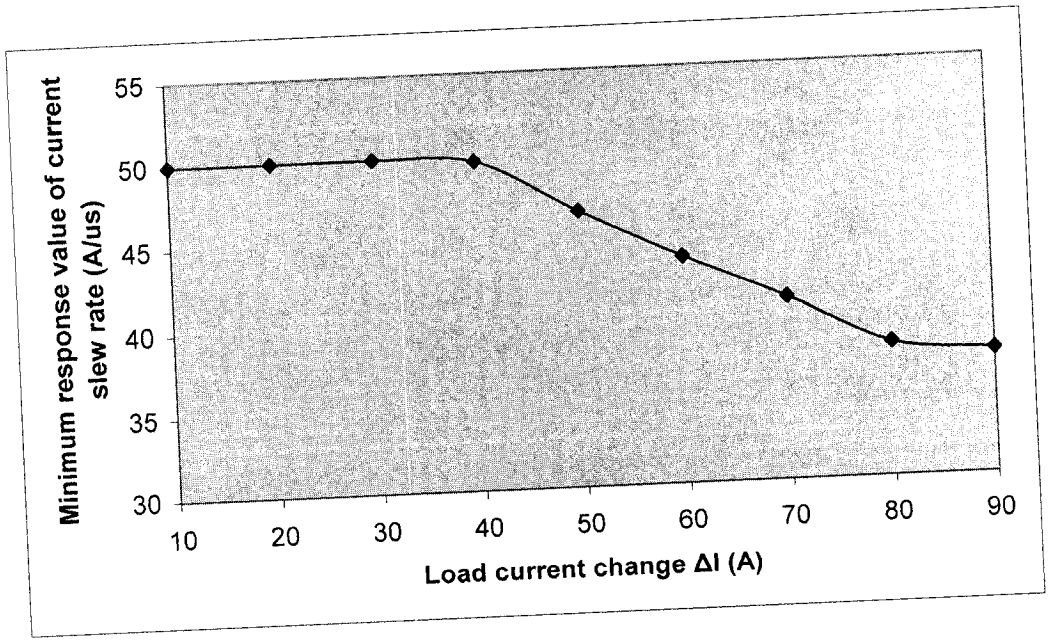
Table 3.3: Compensation result when Microprocessor Operates within Active Mode @ *0.5A/ns* Current Slew Rate and *1V* V_{cc} (C_m=*100n*)

Load change *(A)*	i_{comp} *(A)*	Transient time *(μs)*	ΔV_{cc}
50⇔30	18.8	0.43	1.8%
50⇔40	8.6	0.23	1.8%
50⇔60	8.7	0.25	1.8%
50⇔80	28.6	0.71	1.9%
50⇔90	38.4	0.98	2.0%

Table 3.4: Compensation Responses versus Capacitor C_m

Capacitor C_m (nF)	Transient time (μs)	ΔV_{cc}
200	3.21	2.3%
100	2.55	3.2%
80	2.23	3.4%
60	1.82	3.6%
40	1.34	4.1%
20	0.91	5.5%
10	0.84	17.5%

Table 3.5: Critical response value @ C_m=60nF



The output signal of the voltage monitor is shown in Figure 3-12. At steady state, the signal is small enough and will not turn on compensator's switches. During transient, it has a high voltage output with different voltage values to generate corresponding compensation currents. This is similar to a linear regulator. In general, one can say that the compensator switches off at steady state while it works like a linear regulator at transient.

A poorly designed compensator might have over compensation problems like those shown in Figure 3-13. It may generate ringing in transient process. This is because the first compensation is too big, and it causes the second spike to reverse trigger the compensator. This is the stability problem mentioned before. It can be resolved by decreasing the C_m value.

There is a large dynamic current flowing through the current compensator and it may cause a system voltage drop on the system board. As mentioned before, the energy of the compensator comes from the motherboard, hence capacitors should be mounted close to the compensator to avoid large voltage drops.

The total charge the compensator needed for each transient can be calculated in Equation (3-3),

$$\Delta Q = C \bullet \Delta V = \int_0^{t'} i(t)dt \qquad (3\text{-}3)$$

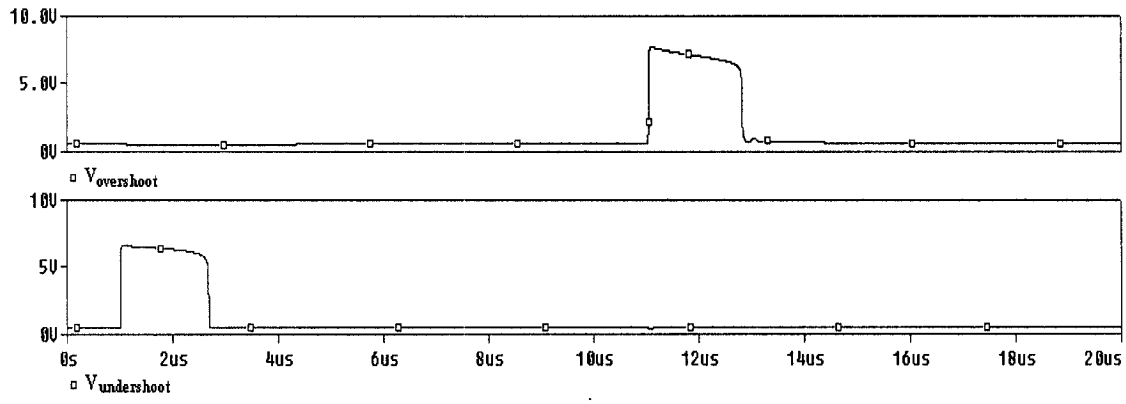


Figure 3-12: Voltage monitor output signal

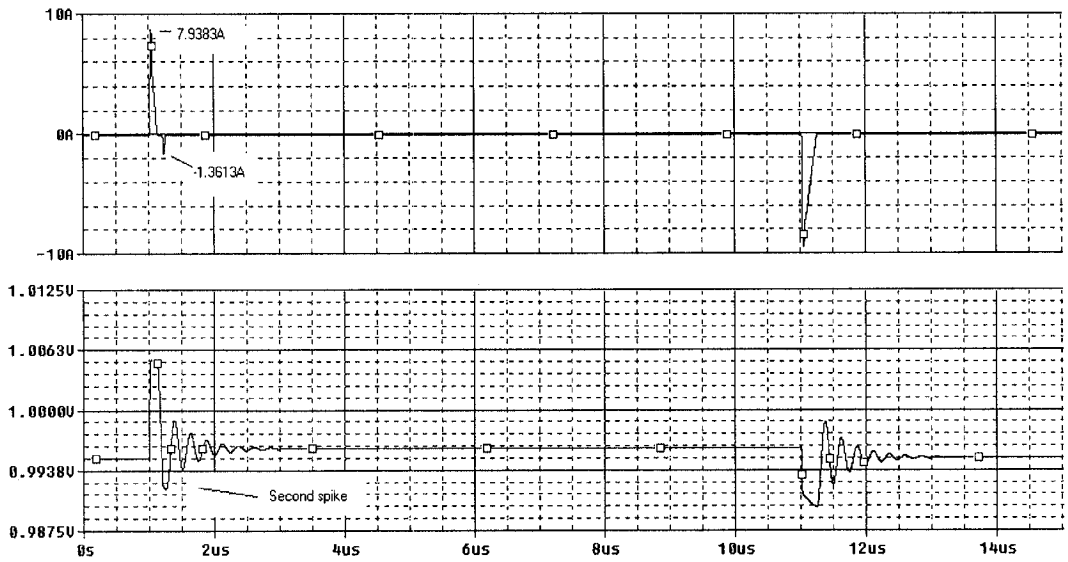


Figure 3-13: Compensation for second spike during transient

Using Equation (3-3), we can approximately obtain Equation (3-4) based on Figure 3-11.

$$\Delta Q = \frac{1}{2} \times 90 \times 1.7 = 76.5(\mu q) \tag{3-4}$$

Therefore, if the voltage drop in the power supply caused by the compensator current is 0.5V for a +5V power supply, the capacitance value for system voltage is

$$C = \frac{\Delta Q}{\Delta V} = \frac{76.5}{0.5} = 153(\mu F) \tag{3-5}$$

This value is very small compared with the bulk capacitance value and approximates the high frequent capacitance value on the motherboard. Therefore, it should not be a problem to mount such a capacitor beside the compensator.

3.5 Summary

A novel active transient current compensation is presented in this chapter to minimize the voltage spike during load-change transient for future generation of microprocessors. Therefore, the total voltage variation at V_{cc} can be limited within 2% (with 240nF capacitors) with the package and system capacitance both decreasing to a much smaller value. Since the compensator has good immunity to large inductance, the layout of system board can be designed more easily and the package inductance requirement will be easier to fulfill.

References

[1] Intel Pentium 4 Processor/Intel 850 Chipset Family Platform Design Guide

[2] Pentium 4 Processor VR-Down Design Guidelines

[3] J. Drnauer et. al., "Electrical Evaluation of Flip-Chip Package Alternatives for Next Generation Microprocessors", IEEE Trans. on Advanced Packaging, vol. 22, pp. 407-415, Aug. 1999

[4] D. J. Herrell and B. Beker, "Modeling of Power Distribution Systems for High-Performance Microprocessor", IEEE Trans. on Advanced Packaging, vol. 22, pp. 240-249, Aug. 1999

[5] R. Panda et. al., "Model and Analysis for Combined Package and On-Chip power Grid Simulation", ISLPED '00, Rapalla, Italy

[6] D. M. Hockanson, et. al., "FDTD and Experimental Investigation of EMI from Stacked-Card PCB Configurations", in IEEE Trans. on Electromagnetic Compatibility, vol. 43, pp.1-9, Feb. 2001

[7] J. E. Vinson and J.J. Liou, "ESD Protection techniques for Semiconductor Devices", Proceedings of International Conference on Microelectronics, vol. 1, pp. 311-321, 2000

[8] Z. H. Wang and Chen-Hui Tsay, "An on-chip ESD protection Circuit with Low Trigger Voltage in BiCMOS Technology", IEEE Journal of Solid-State Circuits, vol. 36, pp. 40-45, Jan. 2001

[9] F.N.K. Poon et. al., "Very Fast Transient Voltage Regulators Based on Load Correction", 1999 IEEE

[10] S.R. Sanders, Albert Wu, "Active Clamp Circuits for Switchmode Regulators Supplying Microprocessor Loads", 1997 IEEE

[11] Jia Luo, Xiaofang Gao, and Issa Batarseh, "Active compensator to improve transient response delay for future generation of microprocessor", Devices, Circuits and Systems, 2002. Proceedings of the Fourth IEEE International Caracas Conference, 17-19 April 2002, Page(s): P018-1 -P018-5

[12] Jia Luo, Issa Batarseh, Xiaofang Gao, and Tomas Wu, "Transient current compensation for low-voltage high-current voltage regulator modules", Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE, Volume: 1, 10-14 March 2002, Page(s): 223 -228 vol.1

CHAPTER FOUR

DIGITAL TIME-VARYING CURRENT OBSERVER AND FEEDBACK CONTROL FOR MULTIPHASE VRMS

4.1 Introduction

With the hardware development of the digital control technique, researchers get to think of using DSP controllers for low voltage high current VRMs. Changing the analog control methods to digital control methods can help to reduce the controller size, improve the EMI immunity, and enable on-board programming. Furthermore, it has powerful digital calculation capability, which is not comparable for analog controller.

For analog control systems, the PWM control and Hysteretic control methods are very common as stated in chapter 2. To achieve better current sharing, phase current feedback loop is also adapted like average phase current compensation and peak current control. Much research has been conducted on current sharing issues in analog control systems, which can be realized easily in a digital controller using methods presented here [1,2].

In this chapter, two different kind of time-varying current observers with parameter estimation are presented. The simple one is designed for PWM control only while the

other can be used for both PWM and hysteretic control methods. The former has fewer voltage sensing points and corresponding A/D converters to cut cost. However, the later is highly recommended due to its accurate and better parameter variation immunity.

4.2 Observer for PWM and hysteretic control

Voltage Regulator Modules (VRMs) for powering microprocessors require very low supply voltage while drawing high current. Current sharing is very important in multiphase VRMs to achieve low current stress and high efficiency. Therefore, different kinds of current sensing methods are developed to meet different control requirements.

The most common method for current sensing is to sense the average voltage across the low-side switches to obtain the average current [1]. However, this method does not show the peak values. For a fast dynamic system (very low inductor value), the difference between average and peak-to-peak value is significant due to inductance imbalance. Another current sensing method is to use a sensing resistor for each phase. This method generates large power losses and decreases efficiency in low voltage and high current situations. The third method is to sense current by integrating the voltage across the output inductor. However, this is an open-loop sensing without feedback correction, and the ESR value of inductors can also cause a sensing error or integrator saturation, if an error amplifier is used for current sensing [2].

A current observer is designed in [3] for inductor current sensing. The main problem is that the current sensor is still used to sense large load current because the load resistance value is unknown and varying with the load demands. The resultant VRM is considered to be a time-varying system. Thus, the time-varying load resistance have to be calculated for estimating the inductor current.

A time-varying current observer with load resistance estimation is designed here to estimate the instantaneous phase currents and load current in multiphase VRMs to achieve current sharing. The adaptive control method is applied to estimate the load changes and simplifies the time-varying system into a nonlinear time invariant system.

Another challenge of the switching power supply modeling is its nonlinear characteristic due to the switch mode changes [3]. It causes the observer to be nonlinear and a decoupling technique is designed to simplify this problem.

4.2.1 State Space Model for Power Stage

The power stage model of four phases buck converter is shown in Figure 4-1. The challenge for modeling switching mode converters is that they have multiple different operating modes. For example, a PWM controlled four phases buck converter as shown in Figure 4-1 has five operating modes when duty ratio $0 \le D < 0.25$, four additional operating modes when duty ratio $0.25 \le D < 0.5$, four additional operating modes when duty ratio $0.5 \le D < 0.75$, and one additional operating mode when duty ratio $0.75 \le D \le 1$. It

has a total of 14 modes making it difficult to model such a nonlinear system, not to mention design a state observer for it

An instantaneous voltage sensing is used here to decouple the complicated relationship caused by switching mode shift. In Figure 4-1, phase node v_1~ v_4 at the crossing points of the high-side and low-side switches are voltage-sensing points. It is similar to the average current sensing method and requires no extra sensing points. Then, all the switching information will react on the voltage waveforms of v_1~ v_4 and there is no need to consider the switching mode shift. Now, the inductor currents in the multiphase converter can be decoupled as shown in Figure 4-2. Here, R_c is the parasitic resistance of output capacitor C, R_{L1} is the parasitic resistance of output inductor L_1, and R_o is the load resistance. Another advantage of the instantaneous voltage sensing is that it avoids the influence of the switch on resistance differences and input voltage variation.

Based on Figure 4-1 and Figure 4-2, the state-space model for the power stage can be expressed in Equation (4-1). Here, v_o is the output voltage of the converter, v_c is the capacitor voltage, and i_1~i_4 are the corresponding inductor currents in the four phases. Obviously, load resistance R_o is an unknown and varying system parameter.

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{di_{L4}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} - \frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_o}{L_1(R_c+R_o)} \\ \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_{L2}}{L_2} - \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_o}{L_2(R_c+R_o)} \\ -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_{L3}}{L_3} - \frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_o}{L_3(R_c+R_o)} \\ -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_{L4}}{L_4} - \frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_o}{L_4(R_c+R_o)} \\ \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & -\frac{1}{(R_o+R_c)C} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ v_c \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_1} & & & \\ & \frac{1}{L_2} & & \\ & & \frac{1}{L_3} & \\ & & & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \qquad (4\text{-}1)$$

$$v_o = \begin{bmatrix} \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ v_c \end{bmatrix}$$

Defining the state and input variable as X and V, we can re-write Equation (4-1) below.

$$X = \begin{bmatrix} i_{L1} & i_{L2} & i_{L3} & i_{L4} & v_c \end{bmatrix}^T \qquad \dot{X} = AX + BV$$

$$V = \begin{bmatrix} v_1 & v_2 & v_3 & v_4 \end{bmatrix}^T \qquad v_o = CX + DV$$

$$A = \begin{bmatrix} -\frac{R_{L1}}{L_1} - \frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_o}{L_1(R_c+R_o)} \\ \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_{L2}}{L_2} - \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_o}{L_2(R_c+R_o)} \\ -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_{L3}}{L_3} - \frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_o}{L_3(R_c+R_o)} \\ -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_{L4}}{L_4} - \frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_o}{L_4(R_c+R_o)} \\ \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & -\frac{1}{(R_o+R_c)C} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & & & \\ & \frac{1}{L_2} & & \\ & & \frac{1}{L_3} & \\ & & & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{bmatrix}$$

$$D = 0$$

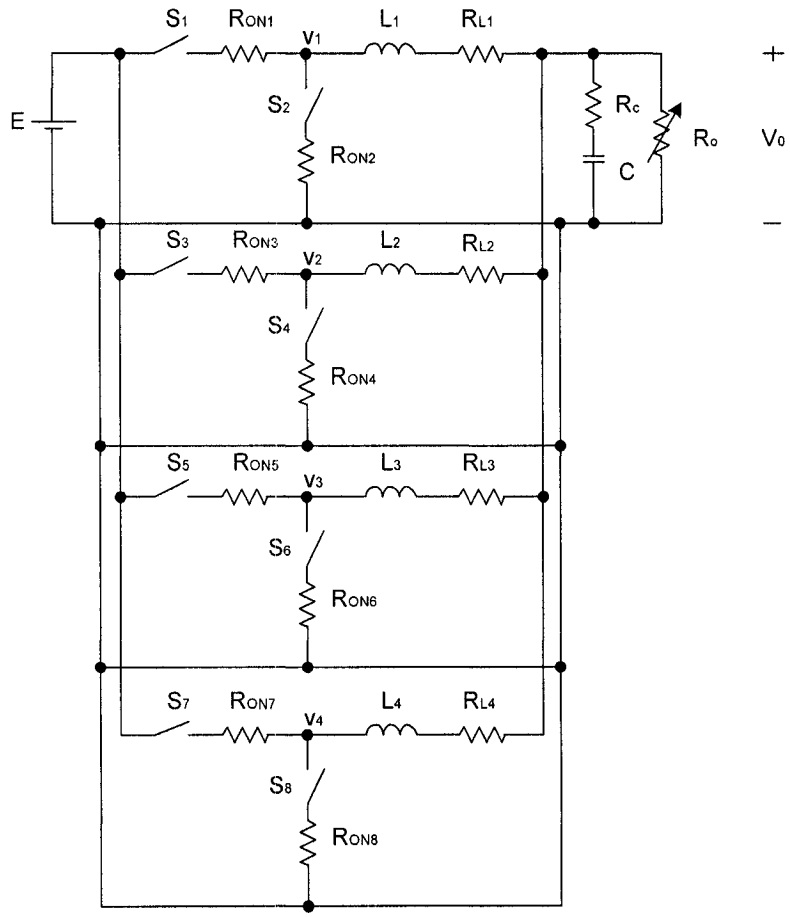


Figure 4-1: Multiphase VRM buck converter

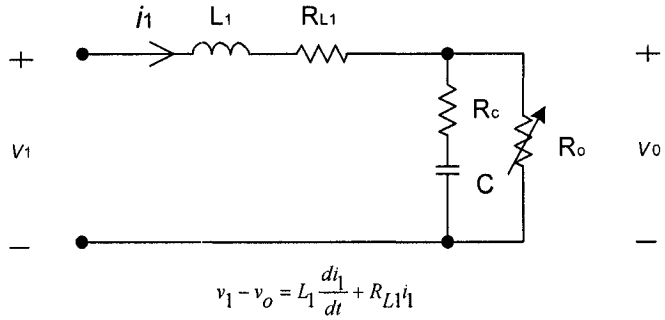


Figure 4-2: State space equation for phase one

Considering the output capacitors are composed of tens of bulk and decoupling capacitors in parallel, the parasitic resistance can be ignored for simplification. Therefore, all of the following analysis is derived by assuming $R_c=0$ and $V_c=V_o$. Hence, matrix A, B, and C are simplified as follows:

$$A=\begin{bmatrix} -\frac{R_{L1}}{L_1} & & & & -\frac{1}{L_1} \\ & -\frac{R_{L2}}{L_2} & & 0 & -\frac{1}{L_2} \\ & & -\frac{R_{L3}}{L_3} & & -\frac{1}{L_3} \\ & 0 & & -\frac{R_{L4}}{L_4} & -\frac{1}{L_4} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{R_o C} \end{bmatrix}$$

$$B=\begin{bmatrix} \frac{1}{L_1} & & 0 & \\ & \frac{1}{L_2} & & \\ & & \frac{1}{L_3} & \\ & 0 & & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix} \qquad (4\text{-}2)$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

4.2.2 Observability

Before designing the current observer, it is necessary to tell what part of the system state is detectable. Given

$$\vartheta(\theta)=\begin{bmatrix} C(\theta) \\ C(\theta)A(\theta) \\ C(\theta)A^2(\theta) \\ C(\theta)A^3(\theta) \\ C(\theta)A^4(\theta) \end{bmatrix} \qquad (4\text{-}3)$$

The definition of a system observability is [5]: The state $x_0 \neq 0$ is said to be unobservable if, given $x(0)=x_0$ and $u(t)=0$ (u is input matrix) for $t \geq 0$, then $y(t)=0$ (y is output matrix) for $t \geq 0$. The system is said to be completely observable if no nonzero initial state exist that is unobservable. This statement is equal to the observability matrix ϑ to be completely observable if and only if ϑ has full column rank n.

For here, when we substitute matrix A and C (in Equation (4-2)) into Equation (4-3)

$$Rank(\vartheta) = \begin{bmatrix} C \\ CA \\ CA^2 \\ CA^3 \\ CA^4 \end{bmatrix} = 5 \tag{4-4}$$

for the whole load change range of R_o. Therefore system is observable.

4.2.3 Adaptive Controller

For a time-varying system, the state space variables can be obtained by designing a state observer with parameter estimation [4-6]. The diagram of the adaptive controller is shown in Figure 4-3 [6]. The notation of $\wedge$ on symbols means it is an observed value, not a measured value. θ represents the time-varying parameter need to be estimated during observation. The definition of the full order adaptive controller is,

$$\dot{\hat{x}} = A(\hat{\theta})\hat{x} + B(\hat{\theta})U + K_x[y - C(\hat{\theta})\hat{x}] \tag{4-5.a}$$

$$\dot{\hat{\theta}} = K_p[y - C(\hat{\theta})\hat{x}] \tag{4-5.6}$$

where, y is the measured value of the output; K_x is gain matrix for state variable and K_p is gain matrix for system output (4^{th} and 1^{st} order for this case, respectively). The gain matrices can be chosen by the requirement of dynamic response and steady state error. Equation (4-5.a) is the state observing equation which is generally used in observer design; Equation (4-5.b) is the parameter estimation equation which is used to estimate the time-varying parameter θ by considering its derivative proportional to the observing error.

4.2.4 Current Observer Design

In our system, parameter θ represents load resistance R_o that is the time-varying parameter and is changing under the load's demand. Therefore, we can obtain the expression for the state observer and parameter estimator in Equation (4-6). By appending R_o as another state variable like *i1*, *i2*, *i3*, *i4*, *vc*, and appending the measured value of output voltage v_o as another input like *v1*, *v2*, *v3*, *v4*, these two equations can be integrated in Equation (4-7). It is clear that Equation (4-7) is 6^{th} order which is one order larger than Equation (4-6).

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{i}_{L3}}{dt} \\ \frac{d\hat{i}_{L4}}{dt} \\ \frac{d\hat{v}_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & -\frac{R_{L2}}{L_2} & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{R_{L3}}{L_3} & 0 & -\frac{1}{L_3} \\ 0 & 0 & 0 & -\frac{R_{L4}}{L_4} & -\frac{1}{L_4} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\hat{R}_o C} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{i}_{L4} \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} + \begin{bmatrix} K_1(v_o - \hat{v}_c) \\ K_2(v_o - \hat{v}_c) \\ K_3(v_o - \hat{v}_c) \\ K_4(v_o - \hat{v}_c) \\ K_5(v_o - \hat{v}_c) \end{bmatrix} \quad (4\text{-}6)$$

$$\dot{\hat{R}}_o = K_p[v_o - \hat{v}_c]$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{i}_{L3}}{dt} \\ \frac{d\hat{i}_{L4}}{dt} \\ \frac{d\hat{v}_c}{dt} \\ \frac{d\hat{R}_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1}-K_1 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & 0 & -\frac{1}{L_2}-K_2 & 0 \\ 0 & 0 & -\frac{R_{L3}}{L_3} & 0 & -\frac{1}{L_3}-K_3 & 0 \\ 0 & 0 & 0 & -\frac{R_{L4}}{L_4} & -\frac{1}{L_4}-K_4 & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\hat{R}_o C}-K_5 & 0 \\ 0 & 0 & 0 & 0 & -K_p & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{i}_{L4} \\ \hat{v}_c \\ \hat{R}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & K_1 \\ 0 & \frac{1}{L_2} & 0 & 0 & K_2 \\ 0 & 0 & \frac{1}{L_3} & 0 & K_3 \\ 0 & 0 & 0 & \frac{1}{L_4} & K_4 \\ 0 & 0 & 0 & 0 & K_5 \\ 0 & 0 & 0 & 0 & K_p \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_o \end{bmatrix} \tag{4-7}$$

This nonlinear 6th-order observer can be transferred to linear system by Jacobian matrix. The Jacobian matrix A_c for the closed-loop nonlinear observer is given in Equation (4-8), where $f(\,)$ and $g(\,)$ are state equations and output equations of the nonlinear system and K is the gain matrix of the observer [4-6].

$$\begin{aligned} &A_c = \left(\partial f / \partial x\right) - K\left(\partial g / \partial x\right) \\ &if \quad \dot{x} = f(x,u) \\ &\quad\; y = g(x,u) \end{aligned} \tag{4-8}$$

Therefore, we can obtain the final state-space equation for the closed-loop current observer with the parameter estimation in Equation (4-9). Here, $\bar{v}_c$ and $\bar{R}_o$ are equilibrium points of a Jacobian matrix which come from Equation (4-10).

Then, the corresponding characteristic polynomial of the observer is given in Equation (4-11). And the stability can be guaranteed by limiting the gain matrix K's range.

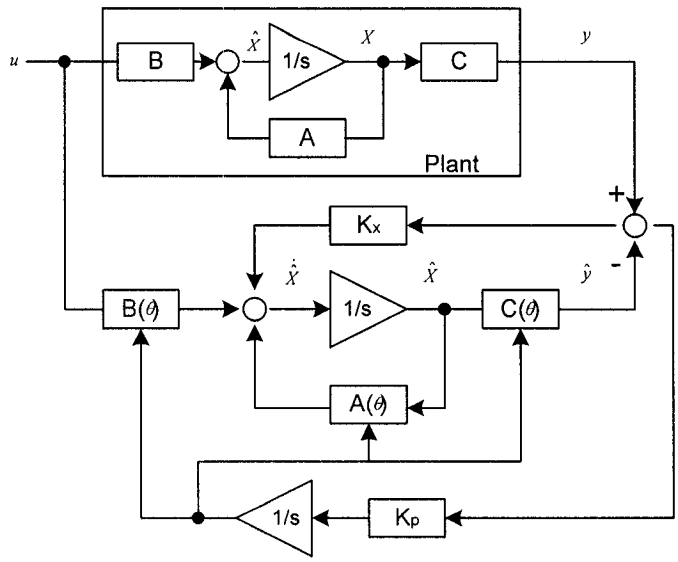


Figure 4-3: Adaptive controller for state observing and parameter estimating

$$\dot{\hat{X}} = A_c \hat{X} + B_c U$$

$$X = \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{i}_{L3} & \hat{i}_{L4} & \hat{v}_c & \hat{R}_o \end{bmatrix}^T$$

$$V = \begin{bmatrix} v_1 & v_2 & v_3 & v_4 & v_o \end{bmatrix}^T$$

$$A_c = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1} - K_1 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & 0 & -\frac{1}{L_2} - K_2 & 0 \\ 0 & 0 & -\frac{R_{L3}}{L_3} & 0 & -\frac{1}{L_3} - K_3 & 0 \\ 0 & 0 & 0 & -\frac{R_{L4}}{L_4} & -\frac{1}{L_4} - K_4 & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\overline{R}_o C} - K_5 & \frac{\overline{v}_c}{\overline{R}_o^2 C} \\ 0 & 0 & 0 & 0 & -K_p & 0 \end{bmatrix} \qquad (4\text{-}9)$$

$$B_c = B$$

where

$$\overline{v}_c = v_o$$

$$\overline{R}_o = \frac{v_o}{\frac{v_1 - v_o}{R_{L1}} + \frac{v_2 - v_o}{R_{L2}} + \frac{v_3 - v_o}{R_{L3}} + \frac{v_4 - v_o}{R_{L4}}}$$

$$\begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1} - K_1 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & 0 & -\frac{1}{L_2} - K_2 & 0 \\ 0 & 0 & -\frac{R_{L3}}{L_3} & 0 & -\frac{1}{L_3} - K_3 & 0 \\ 0 & 0 & 0 & -\frac{R_{L4}}{L_4} & -\frac{1}{L_4} - K_4 & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\overline{R}_o C} - K_5 & 0 \\ 0 & 0 & 0 & 0 & -K_p & 0 \end{bmatrix} \begin{bmatrix} \overline{i}_{L1} \\ \overline{i}_{L2} \\ \overline{i}_{L3} \\ \overline{i}_{L4} \\ \overline{v}_c \\ \overline{R}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & K_1 \\ 0 & \frac{1}{L_2} & 0 & 0 & K_2 \\ 0 & 0 & \frac{1}{L_3} & 0 & K_3 \\ 0 & 0 & 0 & \frac{1}{L_4} & K_4 \\ 0 & 0 & 0 & 0 & K_5 \\ 0 & 0 & 0 & 0 & K_p \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_o \end{bmatrix} = 0 \qquad (4\text{-}10)$$

$$|sI - A_c| = \begin{vmatrix} s + \frac{R_{L1}}{L_1} & 0 & 0 & 0 & \frac{1}{L_1} + K_1 & 0 \\ 0 & s + \frac{R_{L2}}{L_2} & 0 & 0 & \frac{1}{L_2} + K_2 & 0 \\ 0 & 0 & s + \frac{R_{L3}}{L_3} & 0 & \frac{1}{L_3} + K_3 & 0 \\ 0 & 0 & 0 & s + \frac{R_{L4}}{L_4} & \frac{1}{L_4} + K_4 & 0 \\ -\frac{1}{C} & -\frac{1}{C} & -\frac{1}{C} & -\frac{1}{C} & s + \frac{1}{\overline{R}_o C} + K_5 & -\frac{\overline{v}_c}{\overline{R}_o^2 C} \\ 0 & 0 & 0 & 0 & +K_p & s \end{vmatrix} = 0 \qquad (4\text{-}11)$$

To converter an analog observer into a digital observer accurately, Equation (4-12) can be used. However, for a 6th order system, the calculation delay will be unacceptable. Considering a fast sampling period T_s, an approximate method given in Equation (4-13) is used for simplification.

$$\begin{aligned} A_D &= \Phi(T_s) = e^{A_c T_s} \\ B_D &= \int_{T_s}^{kT_s - T} \Phi(kT_s + T_s - \tau) B_c d\tau = \int_0^{T_s} \Phi(T_s - \tau) d\tau B_c \end{aligned} \tag{4-12}$$

$$\begin{aligned} A_D &= I + A_c T_s + A_c^2 \frac{T_s^2}{2!} + A_c^3 \frac{T_s^3}{3!} + \ldots \\ B_D &= \left[T_s + A_c \frac{T_s^2}{2!} + A_c^2 \frac{T_s^3}{3!} + \ldots \right] B_c \end{aligned} \tag{4-13}$$

Defining

$$\begin{aligned} X[K] &= \left[\hat{i}_{L1}(K) \quad \hat{i}_{L2}(K) \quad \hat{i}_{L3}(K) \quad \hat{i}_{L4}(K) \quad \hat{v}_c(K) \quad \hat{R}_o(K) \right]^T \\ U(K) &= \left[v_1(K) \quad v_2(K) \quad v_3(K) \quad v_4(K) \quad v_o(K) \right]^T \end{aligned}$$

we have

$$\begin{aligned} & X(K+1) = A_D X(K) + B_D U(K) \\ & \hat{I}_o(K) = \frac{v_o(K)}{\hat{R}_o(K)} \\ & \textit{where} \\ & \overline{v}_c = v_o(K) \\ & \overline{R}_o = \frac{y(K)}{\frac{v_1(K) - v_o(K)}{R_{L1}} + \frac{v_2(K) - v_o(K)}{R_{L2}} + \frac{v_3(K) - v_o(K)}{R_{L3}} + \frac{v_4(K) - v_o(K)}{R_{L4}}} \end{aligned} \tag{4-14}$$

where, the input $v_1(K) \sim v_4(K)$ and $v_o(K)$ are measured value at moment of KT_s, and $\hat{i}_o(K)$ is the estimated value of load current. The complete matrix of A_D and B_D are given in Appendix. The accuracy of A_D and B_D is acceptable due to the T_s value is microsecond level so the relative err is tiny for the forth term in Equation (4-13).

4.3 Observer for PWM control

4.3.1 State Space Model for Power Stage

For single phase PWM control, the sampling frequency could be same as the switching frequency [3]. This is a nonlinear model with two different modes depending on the switching status of the two switches. this means that the duty ratio is the dominant control signal of the whole system.

But for an interleaved case, there is a 90° (4-phase) phase shift in each phase and each phase has two switching modes. Hence, in each switching period T, there are many different modes and different initial conditions. Moreover, the duty ratio changes with the load changing, which makes it more complicated. If the duty ratio is smaller than 0.25, no overlap happens; if the duty ratio is between 0.25 and 0.5, two phases overlap; if the duty ratio is between 0. 5 and 0.75, three phases overlap; otherwise, four phases overlap. In every case, the operating mode is different, and so are the initial conditions.

The simplest way to model the power stage is to set the sampling frequency as

$$f_s = N \times f \tag{4-15}$$

where f_s is the sampling frequency, f is the switching frequency and N is the number of interleaved phases. Therefore, it eliminates the phase shift in modeling. In another word, when one phase's high-side switch turns on, it begins a new sampling period.

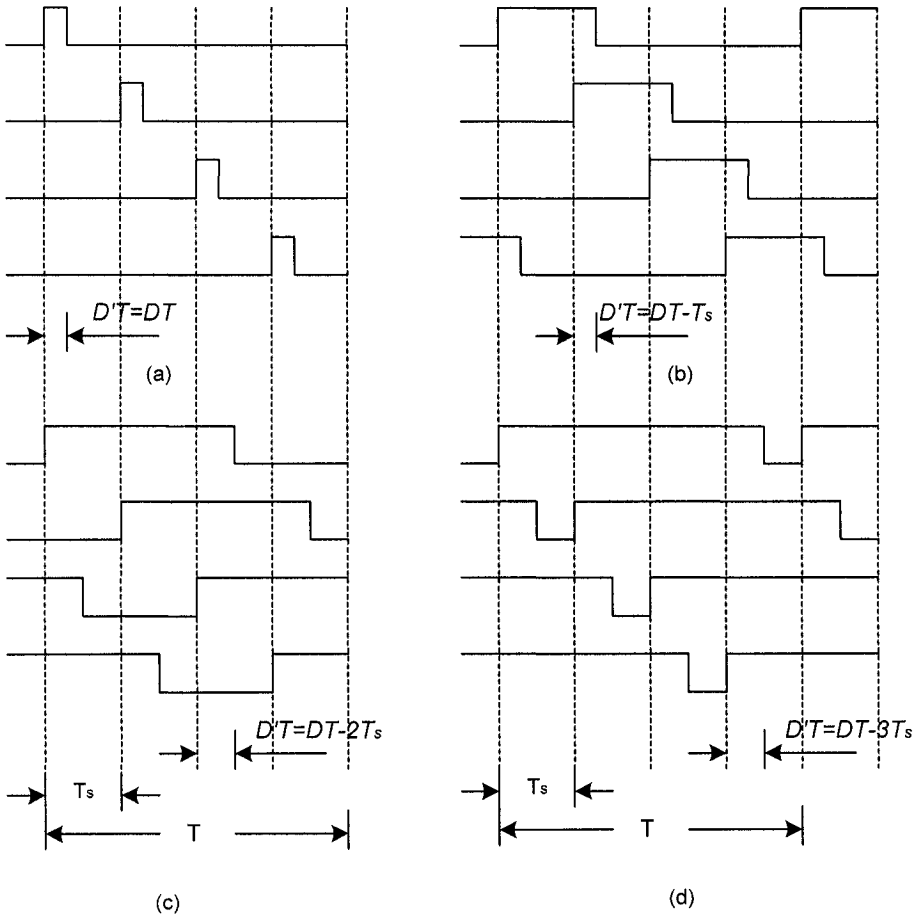
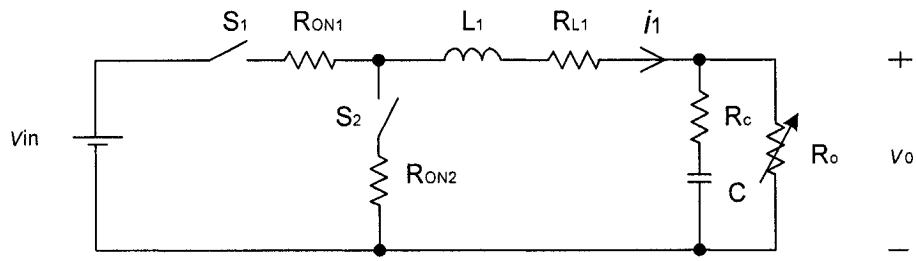


Figure 4-4: Different types of driving signal
(a) D≤0.25; (b) 0.25≤D<0.5; (c) 0.5≤D<0.75; (d) 0.75≤D<1



Mode 1: $vin - v_o = L_1 \frac{di_1}{dt} + (R_{on1} + R_{L1}) i_1$

Mode 2: $-v_o = L_1 \frac{di_1}{dt} + (R_{on2} + R_{L1}) i_1$

Figure 4-5: State space equation for phase one

Figure 4-4 shows the driving signal for the increased sampling frequency. D is the duty ratio and T is switching period; D' is the modified duty ratio corresponding to the sampling period of T_S. In type (a), there is no signal overlapping in sampling period, while in type (b), (c) and (d), there is two, three, or four signals overlapping in the sampling period, respectively. Therefore, in each sampling period, only one phase will change the switching status at moment of *D'T*. This simplifies the multiphase PWM modeling, making it like a single phase.

The state space equation for one phase is given in Figure 4-5. Assuming all the switches are chosen as the same model, the on resistance could be approximated to a fixed value $R_{on}=R_{on1}=R_{on2}$. Now, we get the state space model in Equation (4-16).

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{di_{L4}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}+R_{on}}{L_1} - \frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_o}{L_1(R_c+R_o)} \\ \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_{L2}+R_{on}}{L_2} - \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_o}{L_2(R_c+R_o)} \\ -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_{L3}+R_{on}}{L_3} - \frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_o}{L_3(R_c+R_o)} \\ -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_{L4}+R_{on}}{L_4} - \frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_o}{L_4(R_c+R_o)} \\ \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & -\frac{1}{(R_o+R_c)C} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \\ \delta_4 \end{bmatrix} v_{in}$$

$$y = \begin{bmatrix} \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ v_c \end{bmatrix}$$

(4-16)

where, y is the output voltage of converter and matrix δ is used to describe operating mode of each phase. When high-side MOSFET is on, $\delta=1$; when low side is on, $\delta=0$. Going back to Figure 4-4, there is only one phase on in every period in (a) so only one element in matrix δ is "1". Correspondingly, there are 2,3,or 4 elements equaling to "1" in (b), (c), and (d) respectively. At moment $D'T$, one phase will turn off while others remain unchanged. Then the corresponding element of matrix δ changes to "0". Obviously, for PWM control, the system is non-linear and time varying because of matrix δ and load resistance value.

Defining

$$X = [i_{L1} \quad i_{L2} \quad i_{L3} \quad i_{L4} \quad v_c]^T$$
$$V = [\delta_1 V_{in} \quad \delta_2 V_{in} \quad \delta_3 V_{in} \quad \delta_4 V_{in}]^T$$

we get another format for Equation (4-16)

$$\dot{X} = AX + BV$$
$$y = CA + DV$$
$$A = \begin{bmatrix} -\frac{R_{L1}+R_{on}}{L_1} - \frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_cR_o}{L_1(R_c+R_o)} & -\frac{R_o}{L_1(R_c+R_o)} \\ \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_{L2}+R_{on}}{L_2} - \frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_cR_o}{L_2(R_c+R_o)} & -\frac{R_o}{L_2(R_c+R_o)} \\ -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_{L3}+R_{on}}{L_3} - \frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_cR_o}{L_3(R_c+R_o)} & -\frac{R_o}{L_3(R_c+R_o)} \\ -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_{L4}+R_{on}}{L_4} - \frac{R_cR_o}{L_4(R_c+R_o)} & -\frac{R_o}{L_4(R_c+R_o)} \\ \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & \frac{R_o}{C(R_c+R_o)} & -\frac{1}{(R_o+R_c)C} \end{bmatrix}$$
$$B = \begin{bmatrix} \frac{1}{L_1} & & & \\ & \frac{1}{L_2} & & \\ & & \frac{1}{L_3} & \\ & & & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix}$$
$$C = \begin{bmatrix} \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_cR_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{bmatrix}$$
$$D = 0$$

(4.17)

If we have the same simplification like before, $R_c=0$, we can get

$$A=\begin{bmatrix} -\frac{R_{L1}+R_{ON}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & -\frac{R_{L2}+R_{ON}}{L_2} & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{R_{L3}+R_{ON}}{L_3} & 0 & -\frac{1}{L_3} \\ 0 & 0 & 0 & -\frac{R_{L4}+R_{ON}}{L_4} & -\frac{1}{L_4} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{R_o C} \end{bmatrix}$$

$$B=\begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & \frac{1}{L_4} \\ 0 & 0 & 0 & 0 \end{bmatrix} \qquad (4\text{-}18)$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

This is similar to Equation (4-2) except that the resistance in circuit loop includes the on-resistance of switches. Another difference is the input voltage; the former input voltage is sensed at the crossing point while there is no voltage sensor here for input voltage.

4.3.2 Design of Current Observer with Parameter Estimator

Using the same analysis procedure introduced before, we can get the observer in Equation (4-19)

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{i}_{L3}}{dt} \\ \frac{d\hat{i}_{L4}}{dt} \\ \frac{d\hat{v}_c}{dt} \\ \frac{d\hat{R}_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}+R_{ON}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1}-K_1 & 0 \\ 0 & -\frac{R_{L2}+R_{ON}}{L_2} & 0 & 0 & -\frac{1}{L_2}-K_2 & 0 \\ 0 & 0 & -\frac{R_{L3}+R_{ON}}{L_3} & 0 & -\frac{1}{L_3}-K_3 & 0 \\ 0 & 0 & 0 & -\frac{R_{L4}+R_{ON}}{L_4} & -\frac{1}{L_4}-K_4 & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\hat{R}_o C}-K_5 & 0 \\ 0 & 0 & 0 & 0 & -K_p & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ \hat{i}_{L4} \\ \hat{v}_c \\ \hat{R}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & K_1 \\ 0 & \frac{1}{L_2} & 0 & 0 & K_2 \\ 0 & 0 & \frac{1}{L_3} & 0 & K_3 \\ 0 & 0 & 0 & \frac{1}{L_4} & K_4 \\ 0 & 0 & 0 & 0 & K_5 \\ 0 & 0 & 0 & 0 & K_p \end{bmatrix} \begin{bmatrix} \delta_1 V_{in} \\ \delta_2 V_{in} \\ \delta_3 V_{in} \\ \delta_4 V_{in} \\ v_o \end{bmatrix} \qquad (4\text{-}19)$$

where, v_o is the measured output voltage of the converter and V_{in} is the input voltage. To be noted, V_{in} could be a sensed voltage or a fixed voltage if you think its variation is small enough to be neglected.

Defining

$$\hat{X} = \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{i}_{L3} & \hat{i}_{L4} & \hat{v}_c & \hat{R}_o \end{bmatrix}^T$$

$$U = \begin{bmatrix} \delta_1 V_{in} & \delta_2 V_{in} & \delta_3 V_{in} & \delta_4 V_{in} & v_0 \end{bmatrix}^T$$

$$A = \begin{bmatrix} -\frac{R_{L1}+R_{ON}}{L_1} & & & & 0 & -\frac{1}{L_1}-K_1 & 0 \\ & -\frac{R_{L2}+R_{ON}}{L_2} & & & & -\frac{1}{L_2}-K_2 & 0 \\ & & -\frac{R_{L3}+R_{ON}}{L_3} & & & -\frac{1}{L_3}-K_3 & 0 \\ & 0 & & -\frac{R_{L4}+R_{ON}}{L_4} & & -\frac{1}{L_4}-K_4 & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\hat{R}_o C}-K_5 & & 0 \\ & 0 & & & -K_p & & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & & & 0 & K_1 \\ & \frac{1}{L_2} & & & K_2 \\ & & \frac{1}{L_3} & & K_3 \\ & & & \frac{1}{L_4} & K_4 \\ & 0 & & & K_5 \\ & & & & K_p \end{bmatrix}$$

using Jacobian matrix again, we can get the final time invariant linear observer in Equation (4-20).

$$\dot{\hat{X}} = A_c\hat{X} + B_cU$$

$$\hat{X} = \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{i}_{L3} & \hat{i}_{L4} & \hat{v}_c & \hat{R}_o \end{bmatrix}^T$$

$$U = \begin{bmatrix} \delta_1 V_{in} & \delta_2 V_{in} & \delta_3 V_{in} & \delta_4 V_{in} & v_0 \end{bmatrix}^T$$

$$A_c = \begin{bmatrix} -\frac{R_{L1}+R_{ON}}{L_1} & 0 & 0 & 0 & -\frac{1}{L_1} - K_1 & 0 \\ 0 & -\frac{R_{L2}+R_{ON}}{L_2} & 0 & 0 & -\frac{1}{L_2} - K_2 & 0 \\ 0 & 0 & -\frac{R_{L3}+R_{ON}}{L_3} & 0 & -\frac{1}{L_3} - K_3 & 0 \\ 0 & 0 & 0 & -\frac{R_{L4}+R_{ON}}{L_4} & -\frac{1}{L_4} - K_4 & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{\bar{R}_o C} - K_5 & \frac{\bar{v}_c}{\bar{R}_o^2 C} \\ 0 & 0 & 0 & 0 & -K_p & 0 \end{bmatrix} \quad (4\text{-}20)$$

$$B_c = B$$

where

$$\bar{v}_c = v_o$$

$$\bar{R}_o = \frac{v_o}{\frac{\delta_1 V_{in} - v_o}{R_{L1}+R_{ON}} + \frac{\delta_2 V_{in} - v_o}{R_{L2}+R_{ON}} + \frac{\delta_3 V_{in} - v_o}{R_{L3}+R_{ON}} + \frac{\delta_4 V_{in} - v_o}{R_{L4}+R_{ON}}}$$

In this dissertation, the final discrete matrix is not given since the focus of this chapter is the hysteretic control. However, the analog to digital transfer method is still given in the following equations. Firstly, calculate the equilibrium points of the Jacobian matrix below

$$\bar{v}_c = v_o(K)$$

$$\bar{R}_o = \frac{v_o(K)}{\frac{\delta_1(K)E - v_o(K)}{R_{L1}+R_{ON}} + \frac{\delta_2(K)E - v_o(K)}{R_{L2}+R_{ON}} + \frac{\delta_3(K)E - v_o(K)}{R_{L3}+R_{ON}} + \frac{\delta_4(K)E - v_o(K)}{R_{L4}+R_{ON}}} \quad (4\text{-}21)$$

where, $\delta(K)$ is the operating mode state at moment of KT_s.

Defining

$$\hat{X}[K] = \begin{bmatrix} \hat{i}_{L1}(K) & \hat{i}_{L2}(K) & \hat{i}_{L3}(K) & \hat{i}_{L4}(K) & \hat{v}_c(K) & \hat{R}_o(K) \end{bmatrix}^T$$

$$U(K) = \begin{bmatrix} \delta_1(K)E & \delta_2(K)E & \delta_3(K)E & \delta_4(K)E & v_o(K) \end{bmatrix}^T$$

The discrete time equation of the observer can be calculated as follows

$$\begin{aligned}\hat{X}(KT_S + T_S) &= e^{AT_S}\hat{X}(KT) + \int_{KT_S}^{KT_S+T_S} e^{A_C(KT_S+T_S-\zeta)}B_c u(\zeta)d\zeta \\ &= e^{AT_S}\hat{X}(KT) + \int_{KT_S}^{KT_S+D'T_S} e^{A_C(KT_S+T_S-\zeta)}B_b U(K)d\zeta + \int_{KT_S+D'T_S}^{(K+1)T_S} e^{A_C(KT_S+T_S-\zeta)}B_b U(K,D')d\zeta \\ &= e^{AT_S}\hat{X}(KT) + \int_{0}^{D'T_S} e^{A_C(T_S-\zeta)}B_b U(K)d\zeta + \int_{D'T_S}^{T_S} e^{A_C(T_S-\zeta)}B_b U(K,D')d\zeta\end{aligned} \tag{4-22}$$

We can write Equation (4-22) to another format

$$\begin{aligned}\hat{X}(K+D') &= e^{A_c D'T_s}\hat{X}(K) + \left(e^{A_c D'T_s} - I\right)A_c^{-1}B_c U(K) \\ \hat{X}(K+1) &= e^{A_c T_s}\hat{X}(K) + e^{A_c T_s}\left(I - e^{-A_c D'T_s}\right)A_c^{-1}B_c U(K) + \left(e^{A_c(1-D')T_s} - I\right)A_c^{-1}B_c U(K,D')\end{aligned} \tag{4-23}$$

Obviously, it is a nonlinear expression with respect to the duty circle D'. The definition of D' is shown in Figure (4-4).

Hence, the final digital observer is

$$\begin{aligned}X(K+1) &= e^{A_c D'T_s}X(K) + \left(e^{A_c D'T_s} - I\right)A_c^{-1}B_c U(K) \\ \hat{I}_o(K+D') &= \frac{v_o(K)}{\hat{R}_o(K+D')} \\ X(K+1)v &= e^{A_c T_s}X(K) + e^{A_c T_s}\left(I - e^{-A_c D'T_s}\right)A_c^{-1}B_c U(K) + \left(e^{A_c(1-D')T_s} - I\right)A_c^{-1}B_c U(K) \\ \hat{I}_o(K) &= \frac{y(K)}{\hat{R}_o(K)}\end{aligned} \tag{4-24}$$

The first part is the estimated current value at moment of $KT_s+D'T_s$; and the second part is the estimated current value at the moment of KT_s. It is almost impossible to solve Equation (4-24) by hand. Readers could get those parameters by computer.

4.4 Design of Feedback Controller

The feedback controller designed here is a voltage hysteretic controller with peak current sharing. For a voltage hysteretic control, the feedback controller is designed to,

$$\zeta_{n+1} = \mathrm{sgn}(y, \zeta_n) = \begin{cases} 1, & \zeta_n = 1 \,\&\, y_{r,l} < y < y_{r,h} \text{ or } \zeta_n = 0 \,\&\, y < y_{r,l} \\ 0, & \zeta_n = 1 \,\&\, y > y_{r,h} \text{ or } \zeta_n = 0 \,\&\, y_{r,l} < y < y_{r,h} \end{cases} \tag{4-25}$$

where ζ_n is the original driving signal coming from the voltage hysteretic window at low limit of $y_{r,l}$ and high limit of $y_{r,h}$. For the interleaved technique, the driving signal should be distributed to each phase, i.e. each phase is turned on in turn as shown in Figure 4-6. Unlike normal voltage hysteretic control, Figure 4-6 shows three different kinds of turn on mode. This is used to provide a different choice of phase current slope and transient speed. How many phases should turn on at a specific moment depends on the load current and the demanded current slope.

The peak current control is designed to obey two rules. Firstly, always turning on the current minimum phase or phases to prevent current run-away. Equation (4-26) is the constraint condition for minimum current phase turn-on. The second condition for peak current control is maximum current turn-off. If the running phase current is larger than *5%* of the maximum phase current's peak value, the controller will turn it off no matter whether the output voltage hits the high limit or not. It is given in Equation (4-27).

Single phase turn on	Two - phase turn on together	Three - phase turn on together
$\eta_1 = \begin{cases} 1, & \hat{i}_{L1} < \hat{i}_{21}, \hat{i}_{L3}, \hat{i}_{L4} \\ 0, & \text{otherwise} \end{cases}$	$\eta_1 = \begin{cases} 1, & \hat{i}_{L1} \text{ is smallest two} \\ 0, & \text{otherwise} \end{cases}$	$\eta_1 = \begin{cases} 0, & \hat{i}_{L1} > \hat{i}_{21}, \hat{i}_{L3}, \hat{i}_{L4} \\ 1, & \text{otherwise} \end{cases}$
$\eta_3 = \begin{cases} 1, & \hat{i}_{L2} < \hat{i}_{21}, \hat{i}_{L3}, \hat{i}_{L4} \\ 0, & \text{otherwise} \end{cases}$	$\eta_3 = \begin{cases} 1, & \hat{i}_{L2} \text{ is smallest two} \\ 0, & \text{otherwise} \end{cases}$	$\eta_3 = \begin{cases} 0, & \hat{i}_{L2} > \hat{i}_{21}, \hat{i}_{L3}, \hat{i}_{L4} \\ 1, & \text{otherwise} \end{cases}$
$\eta_5 = \begin{cases} 1, & \hat{i}_{L3} < \hat{i}_{21}, \hat{i}_{L2}, \hat{i}_{L4} \\ 0, & \text{otherwise} \end{cases}$	$\eta_5 = \begin{cases} 1, & \hat{i}_{L3} \text{ is smallest two} \\ 0, & \text{otherwise} \end{cases}$	$\eta_5 = \begin{cases} 0, & \hat{i}_{L3} > \hat{i}_{21}, \hat{i}_{L2}, \hat{i}_{L4} \\ 1, & \text{otherwise} \end{cases}$
$\eta_7 = \begin{cases} 1, & \hat{i}_{L4} < \hat{i}_{21}, \hat{i}_{L2}, \hat{i}_{L3} \\ 0, & \text{otherwise} \end{cases}$	$\eta_7 = \begin{cases} 1, & \hat{i}_{L4} \text{ is smallest two} \\ 0, & \text{otherwise} \end{cases}$	$\eta_7 = \begin{cases} 0, & \hat{i}_{L4} > \hat{i}_{21}, \hat{i}_{L2}, \hat{i}_{L3} \\ 1, & \text{otherwise} \end{cases}$

(4-26)

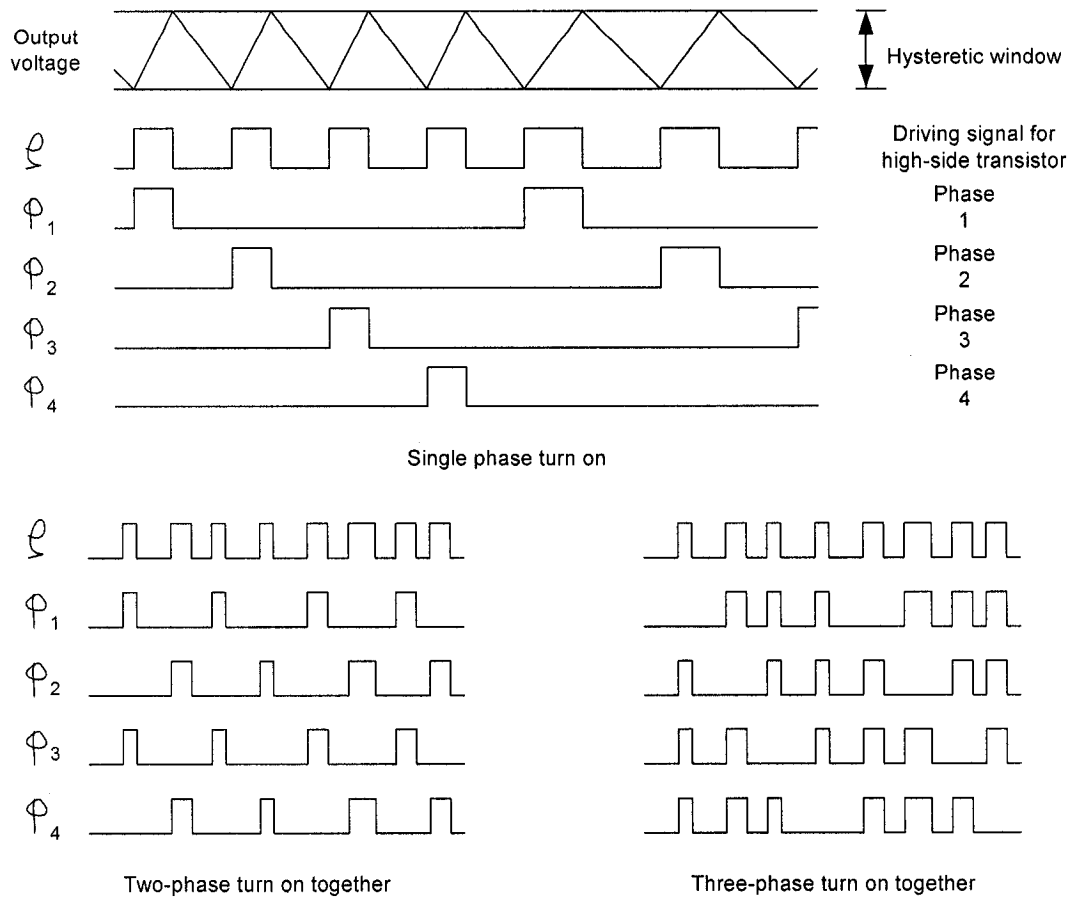


Figure 4-6: Driving signal for each phase

$$\beta_1 = \begin{cases} 1, & \hat{I}_{L1} > 105\% \times Max(\hat{I}_{L2}, \hat{I}_{L3}, \hat{I}_{L4}) \\ 0, & \text{otherwise} \end{cases}$$
$$\beta_2 = \begin{cases} 1, & \hat{I}_{L2} > 105\% \times Max(\hat{I}_{L1}, \hat{I}_{L3}, \hat{I}_{L4}) \\ 0, & \text{otherwise} \end{cases}$$
$$\beta_3 = \begin{cases} 1, & \hat{I}_{L3} > 105\% \times Max(\hat{I}_{L1}, \hat{I}_{L2}, \hat{I}_{L4}) \\ 0, & \text{otherwise} \end{cases}$$
$$\beta_4 = \begin{cases} 1, & \hat{I}_{L4} > 105\% \times Max(\hat{I}_{L1}, \hat{I}_{L2}, \hat{I}_{L3}) \\ 0, & \text{otherwise} \end{cases} \qquad (4\text{-}27)$$

Hence, the final high-side driving signal, φ, is given by

$$\varphi = \begin{bmatrix} \varphi_1 \\ \varphi_3 \\ \varphi_5 \\ \varphi_7 \end{bmatrix} = \zeta \begin{bmatrix} \eta_1 \\ \eta_3 \\ \eta_5 \\ \eta_7 \end{bmatrix} \bullet \begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \\ \beta_4 \end{bmatrix} \qquad (4\text{-}28)$$

To be noted, Equation (4-28) is only the driving signal for high-side switch while the low-side driving signal is complementary to the high-side ones.

At large load change transient, the output voltage reaches the overshoot value of hysteretic window so all the phases should be turned on or turned off together to get the fastest transient response. In this case, all of the control logic mentioned before is cancelled and the high-side driving signal is set to be

$$\varphi = \begin{bmatrix} \varphi_1 \\ \varphi_3 \\ \varphi_5 \\ \varphi_7 \end{bmatrix} = \begin{cases} \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} & \text{if } y \le V_{undershoot} \\ \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} & \text{if } y \ge V_{overshoot} \end{cases} \qquad (4\text{-}29)$$

This is the driving signal for AAL-ON or ALL-OFF cases to speed the transient process. As mentioned before, current slope control is used to provide different dynamic choice.

Therefore, the AAL-ON or ALL-OFF signal can also be regarded as maximum current slope control.

An experiment was completed to prove this control idea with minimum current phase turn-on and ALL-ON ALL-OFF control which is a combination of Equation (4-25), (4-26) and (4-29). The maximum current turn-off control is not implemented in this experiment. The experiment was designed by J. A. Abu-Qahouq and the DSP implementation was completed by N. Pongratananukul. Please refer [8] for the experiment setup and results.

4.5 MATLAB/SIMULINK Simulation Result and Experiment Verification for Observer

Matlab/simulink is used to simulate a two phases buck converter observer system. The schematic is shown in Figure 4-7. VM, VM1 and VM2 are voltage sensors for output voltage and crossing point voltages. The block called "cobserv" is the current observer which fulfils the current estimation based on Equation (4-14) – (4-16). The program is given in Appendix. The load resistance μp is 0.2Ω at the beginning and changes to 0.01Ω at the moment of $0.0015s$ $(\mu p+\mu p1)$. The parameters for this simulation are listed in Table 4.1.

The simulation results are shown in Figures 4-8 – Figure 4-13. In these figures, the measured values are those obtained from power stage by current and voltage sensors

shown in Figure 4-7. The observed values are those calculated from the observer (the output of block "cobserv").

As mentioned before, this observer is designed as a full order observer system, so we calculated the observed output capacitor voltage v_o, in the observer. Figure 4-8 shows the two waveforms of the measured value and the observed value. Since the whole simulation system is an open-loop system, there is no voltage compensation for the load changing; the output voltage at heavy load is lower than light load.

Figure 4-9 shows the waveforms of zoomed v_o. Due to the neglecting of the ESR of the output capacitors, there is a steady state error of 3 times the peak-to-peak value while the average value is equal.

Figures 4-10 – Figure 4-12 show the waveforms of measured and observed phase current value i_{L1}.and i_{L2} Obviously, there is almost no observing error in either transient and in steady state. To be noted, the two phase currents have 180° phase shift

Figure 4-13 shows the two phase currents in an imbalance phase inductor situation. The phase 1 inductor value changes to $L_1=320nH$ and $R_{L1}=1.1m\Omega$ while phase 2 value keeps unchanged. Therefore, both the average value and peak-to-peak value of phase 1 current is smaller than phase 2.

Table 4.1: Parameter List

Phase 1 Inductance	L_1	$300nH$
	R_{L1}	$1m\Omega$
Phase 2 Inductance	L_2	$300nH$
	R_{L2}	$1m\Omega$
Output Capacitor	C	$3.6mF$
	R_c	$2m\Omega$
Low-side and high-side Switch On-Resistor R_{on}		$10m\Omega$
Light Load Resistance μp		0.2Ω
Heavy Load Resistance $\mu p+\mu p1$		0.01Ω
Switching Frequency f_s		$1MHz$

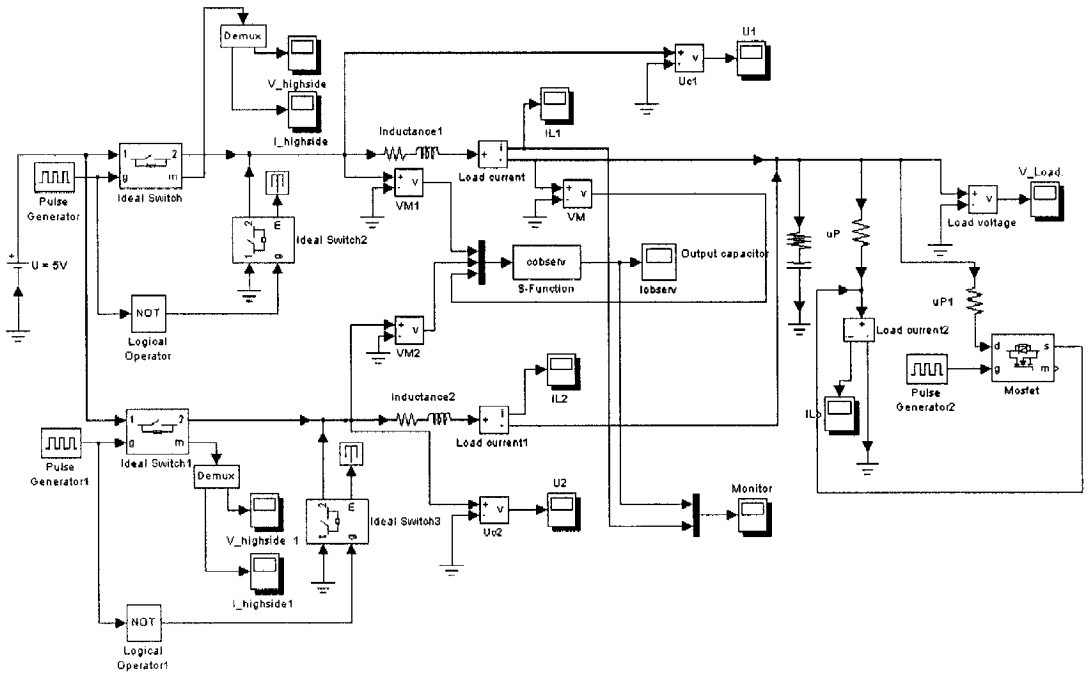


Figure 4-7: Schematics

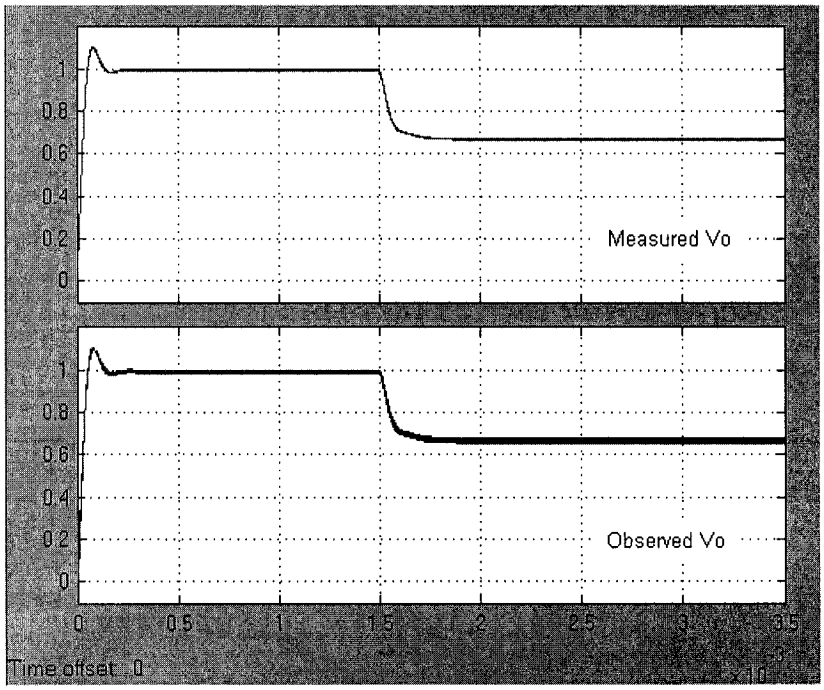


Figure 4-8: The waveforms of measured and observed output voltage v_o

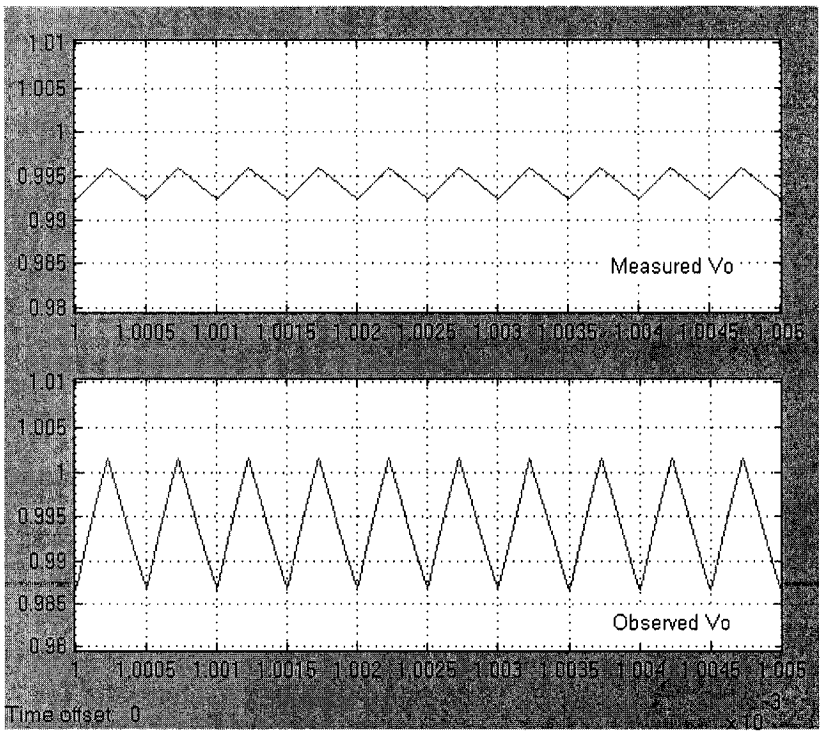


Figure 4-9: The waveform of Zoomed v_o

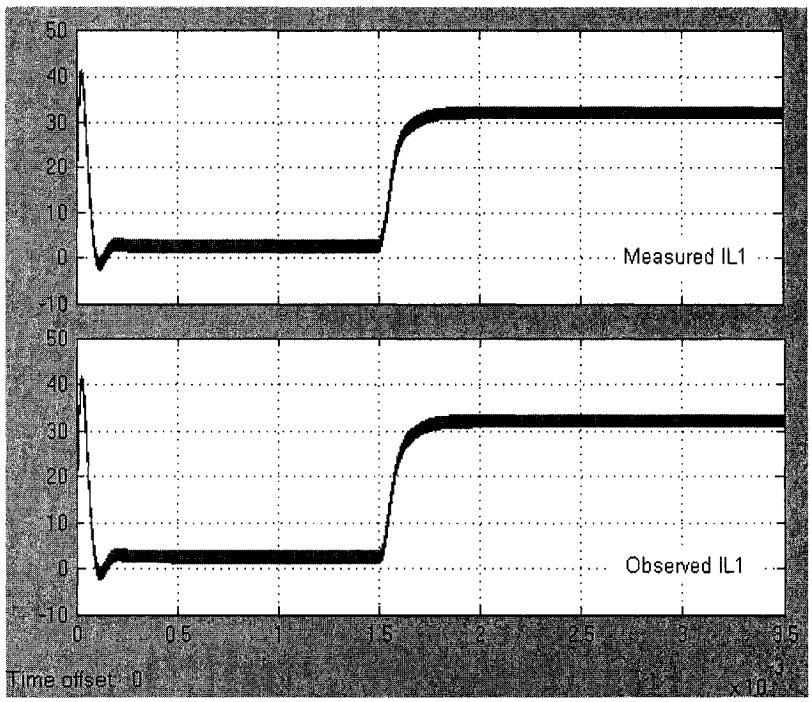


Figure 4-10: The waveforms of measured and observed phase current i_{L1}

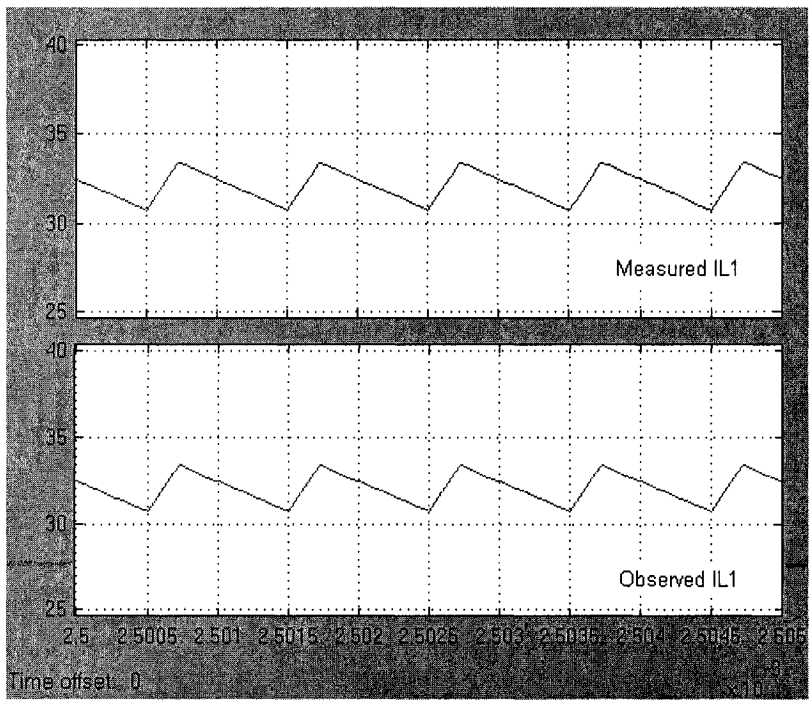


Figure 4-11: The waveforms of Zoomed i_{L1}

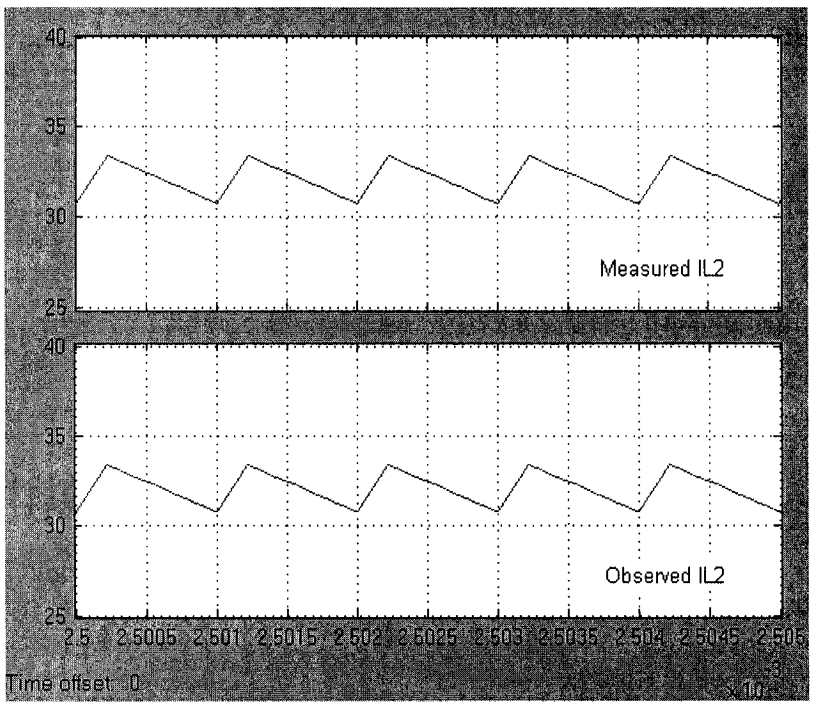
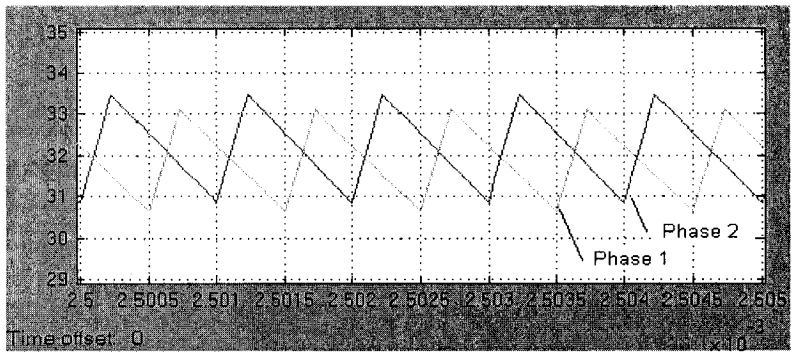
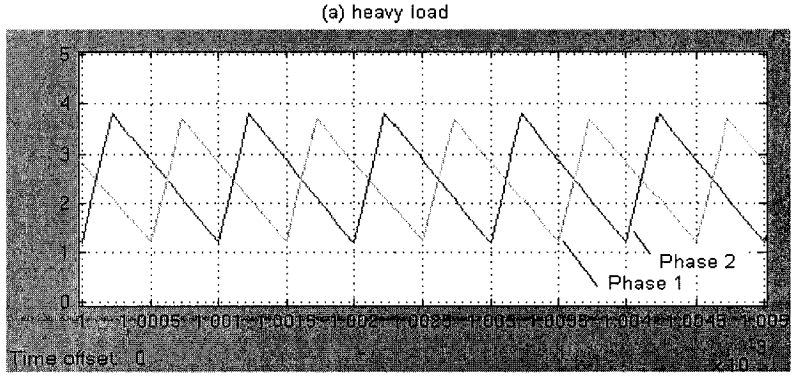


Figure 4-12: The waveforms of zoomed i_{L2}



(a) heavy load



(b) light load

Figure 4-13: The waveforms of imbalanced phase inductor current

An experimental setup was built in the laboratory to verify the analysis and simulation results. The VRM power stage is:

- MOSFET: SI4410DY
- MOSFET driver: TPS2836
- Output cap: 3 SANYO OSCON 820uF, 4V
- Output inductor: 28A, 1uH, T68-8/90 core, 7 turns, 16AWG wire

An experiment result is given in Figure 4-14 to show the phase currents. This experiment is based on a 2-phase buck converter working at *100kHz, 5V* input, *1V* and *20A* output. The average current of each phase in Figure 4-14 is 10A, and the peak-to-peak current ripple is *6.78A*. An observed result is given in Figure 4-15 by putting all the parameters in the program given in Appendix.The average observed phase current value is 10A for each phase and peak-to-peak current ripple is *7A* which is *3.24%* larger than *6.78A*.

4.6 Summary

A digital controller design for multiphase VRM is presented in this chapter. The feedback control method is voltage hysteretic control with peak-to-peak current sharing. The time varying current observer with load resistance estimation is introduced for sensing the instant phase currents. Both the dynamic and steady state observed values are tightly following the practical system. It is proven by the simulation results and experiment verification.

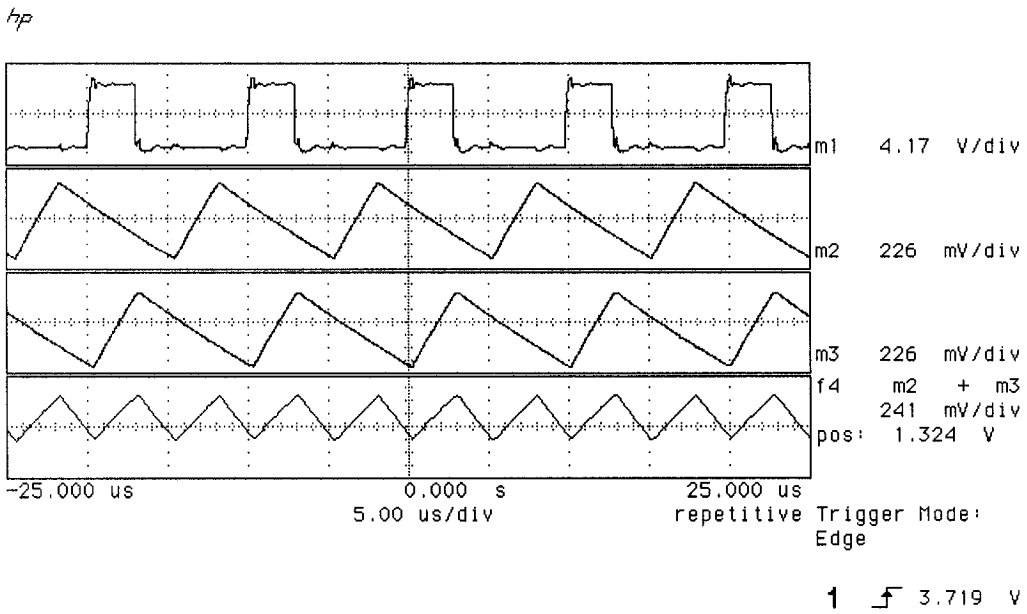


Figure 4-14: Experiment results of phase currents

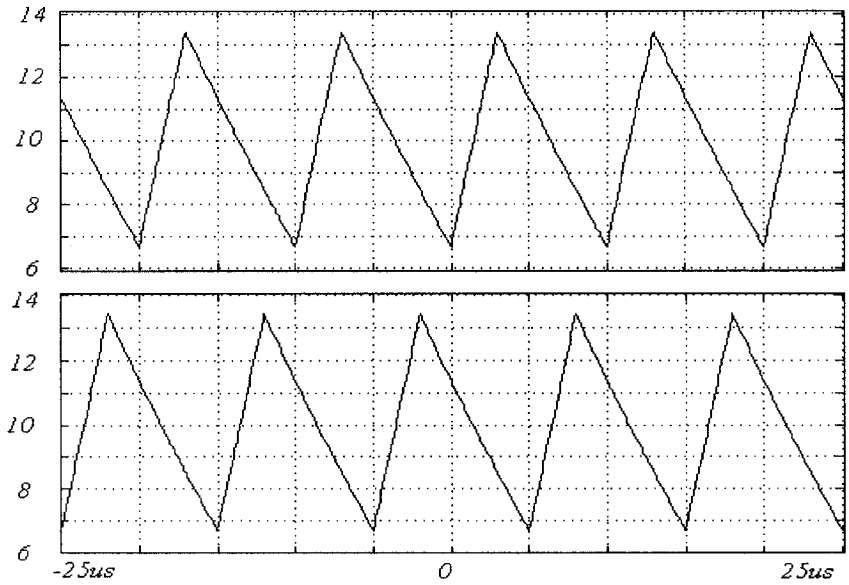


Figure 4-15: Experiment results of observed phase current

References

[1] Xunwei Zhou, "Low-Voltage High-Efficiency Fast Transient Voltage Regulator Modules", Ph.D. Dissertation, Virginia Polytechnic Inst. State Univ., Blackburg, 1999.

[2] B. Arbetter & D. Maksimovic, "DC-DC Converter with Fast Transient Response and high Efficiency for Low-Voltage Microprocessor Loads", Applied Power Electronics Conference and Exposition, 1998. APEC '98.

[3] P. Julian, A. Oliva, P. Mandolesi, H. Chiacchiarini, "Output discrete feedback control of a DC-DC buck converter", Industrial Electronics, 1997. ISIE '97

[4] Bernard Friedland, "A Nonlinear Observer for estimating parameters in dynamic systems ", Automatic, vol. 33, August 1997.

[5] R.H. Middleton & G.C. Goodwin, "Digital Control & Estimation— A Unified Approach", Prentice-Hall, 1990.

[6] P.P. Kanjilal, "Adaptive Prediction & Predictive Control", Peter Peregrinus, 1995

[7] C.P. Mracek, etl., "A New Technique for Nonlinear Estimation", Control Applications, Dearborn, MI, September, 1996

[8] Jaber A. Abu-Qahouq, Nattorn Pongratananukul, Issa Batarseh, and Takis Kasparis, " Multiphase Voltage-Mode Hysteretic Controlled VRM with DSP Control and Current Sharing Solution," APEC 2002

[9] Jia Luo, Nat Pongratananukul, Abu-Qahouq, J.A., and Issa Batarseh, "Time-varying current observer with parameter estimation for multiphase low-voltage high-current voltage regulator modules", Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE , Volume: 1 , 9-13 Feb. 2003, Page(s): 444 –450

[10] Jia Luo, Nattorn Pongratananukul, Jaber A. Abu-Qahouq, and Issa Batarseh, "Digital Time-Varying Current Observer and Feedback Control for Multiphase Low-Voltage High-Current Voltage Regulator Modules", Systemics, Cybernetics and Informatics, Orlando, FL, Augest, 2003

CHAPTER FIVE

PROPORTIONAL ON TIME VOLTAGE HYSTERETIC CONTROL WITH CURRENT SHARING FOR WIDE RANGE INPUT VOLTAGE VARIATION VRMS

5.1 Introduction

The advantages of fast feedback control loop and simple circuit configuration for voltage hysteretic control make it very popular for single phase low voltage high current VRMs. However, the current sharing difficulty for multiphase VRMs limits its usage. This is because both the on time duration and off time duration of the switches are non-controllable. It depends on the comparison of the output voltage and the hysteretic window. Once the output voltage hits the high limit, the high-side switches should be turned off. Once the output voltage hits the low limit, the high-side switches should be turned on. This process is irrelevant to do with current sharing. The only way to solve this problem is the variable hysteretic window for each phase,in other words the smaller average current phase has a larger hysteretic window to achieve longer ON-TIME for improving the phase current [1].

Another difficulty for low voltage high current VRMs is the wide range input voltage variation. This is not a problem for desktop PCs because their input voltage is fixed to *3.3V/5V/12V* depending on the system configuration. However, in communication systems and notebook systems, the input voltage of VRM has a wide range of variation. For example, the power supply for a notebook comes from a battery so its voltage may change from *6V* to *30V* which makes the duty ratio change significiently. If we still use regular voltage hysteretic controller, the switching frequency will vary in wide range. It seems that the voltage hysteretic control method is not a good candidate for wide range input voltage cases.

The PWM control with average current sharing or peak current control is dominant in this area for the above mentioned reasons. For N-phase VRMs, PWM controllers require N phase-shifted controllers which makes the whole control circuit very complicated and costly. The peak current control requires N-phase instantaneous current waveforms as well as N phase-shifted PWM based controllers, which are more complicated than PWM control.

In this chapter, a proportional ON-TIME voltage hysteretic control is used on multiphase buck converters to solve frequency variation problems [2-10]. The variation decreases to a very small range although the input voltage changes from *6V* to *30V*. A novel current sharing is developed by ON-TIME duration compensation and average voltage sensing at the phase nodes (crossing points of the high-side and low-side switches) is used for this compensation.

5.2 Control Method of the Proportional ON-TIME Voltage Hysteretic Control

As we are mentioned before, the regular voltage hysteretic control has a hysteretic window, which sets the high limit and low limit for the output voltage. While in this control method, only the low limit is set for the output voltage. However, where does the high limit come from? It does not come directly from the output voltage. Instead, it comes from the input voltage.

The name of proportional ON-TIME comes from the high-side switch, which is turned on when the output voltage hits the low limit, and its ON-TIME duration is reverse proportional to the input voltage. If the input voltage is higher, the on time duration is smaller. Therefore, the 30V input voltage has the smallest ON-TIME duration while the 6V input voltage has the largest ON-TIME duration. The advantage of this arrangement is to keep the operating frequency variation in a minimum range.

If the input voltage is 6V~30V and the output voltage is 1V, the duty ratio variation is:

$$\begin{aligned} D_{30} &= 1/30 = 0.033 \\ D_6 &= 1/6 = 0.167 \end{aligned} \tag{5-1}$$

Therefore, if we intend to make the ON-TIME duration like:

$$\begin{aligned} T_{on\_30} &= 0.033 \times \frac{1}{500k} = 66(ns) \\ T_{on\_6} &= 0.167 \times \frac{1}{500k} = 333(ns) \end{aligned} \tag{5-2}$$

They will have the same switching frequency of *500kHz*.

Since the power stage has power dissipation at the switches, inductors, capacitors, and connections, however, the actually duty ratio is always larger than the ideal ones. The reason why the actual system has switching frequency variation in this system is that the smaller the duty ratio is, the larger the duty ratio deviates. It is hardly to compensate for this deviation since the system designers may choose different components and layout structures. Still, the frequency variation is smaller than regular voltage hysteretic controllers in the same situation.

The low output voltage limit setting is similar to ones in regular hysteretic control, as shown in Figure 5-1. When output voltage is lower than the low limit, the circuit has an output called $V_{outcomp}$ setting at "1" to turn on the high-side switch of the power stage. Otherwise, the output is "0".

The controller design for the ON-TIME block is shown in Figure 5-2. When the $V_{outcomp}$ has output, the K1 switch is turned on, and the circuit begins to charge the capacitor C_{on} via resistor R_{on}. Since switches K1 and K2 are complimentary, K2 is turned off, and the voltage on C_{on} starts to increase. When it is larger than the reference voltage V_{on_ref}, the output V_{oncomp} has an output "1". This signal is used to turn off the high-side switch of the power stage. The charging time constant of $C_{on}R_{on}$ is decided by the on time duration of the power stage. The larger the time constant is, the slower the charging speed will be, resulting in a longer ON-TIME duration. Normally the discharge resistor is chosen to be smaller than R_{on} to shorten the discharge duration.

The timing for ON-TIME and OFF-TIME during one cycle is shown in Figure 5-3 (a). When the output voltage is lower than the reference voltage, the $V_{outcomp}$ has output to turn on the high-side switch. The on time block is triggered simultaneously so that the capacitor starts charging. When V_{on} is larger than its reference voltage, the V_{oncomp} has an output to turn off the high-side switch. At the same time, the on time capacitor discharges. The bottom waveform is the current waveform for the inductor. It is notable taht the output voltage always has some response delay so it is not at the same phase as inductor current.

The gate driver signal is shown in Figure 5-3 (b). The proportional ON-TIME control logic circuit is shown in Figure 5-4. Two dual positive-edge-triggered D-type flip-flops are used to hold and reset $V_{outcomp}$ and V_{oncomp}. An exclusive OR logic and an inverter are used to generate the gate driver signal. Pins of PRE and CLR are tied to high voltage to make the D-type flip-flop work at positive-clock-trigger mode.

The gate driver signal here is the initial driving signal for multiphase voltage hysteretic controller. The gate diver signal for each phase should be distributed as shown in Figure 5-5 (a). Figure 5-5 (b) is the logic of the gate driver signals. The four inverters are used to match the D-type flip-flop's timing.

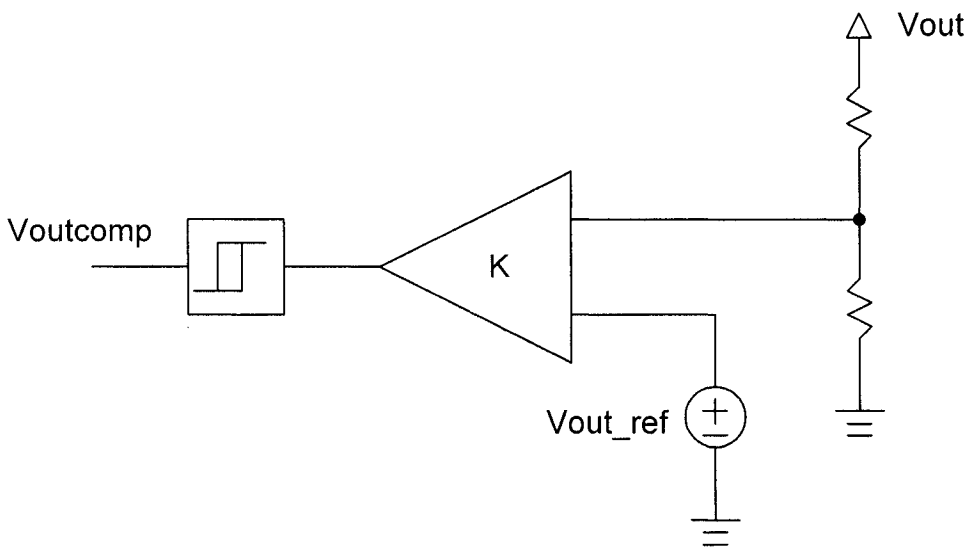


Figure 5-1: Low output voltage limit setting circuit

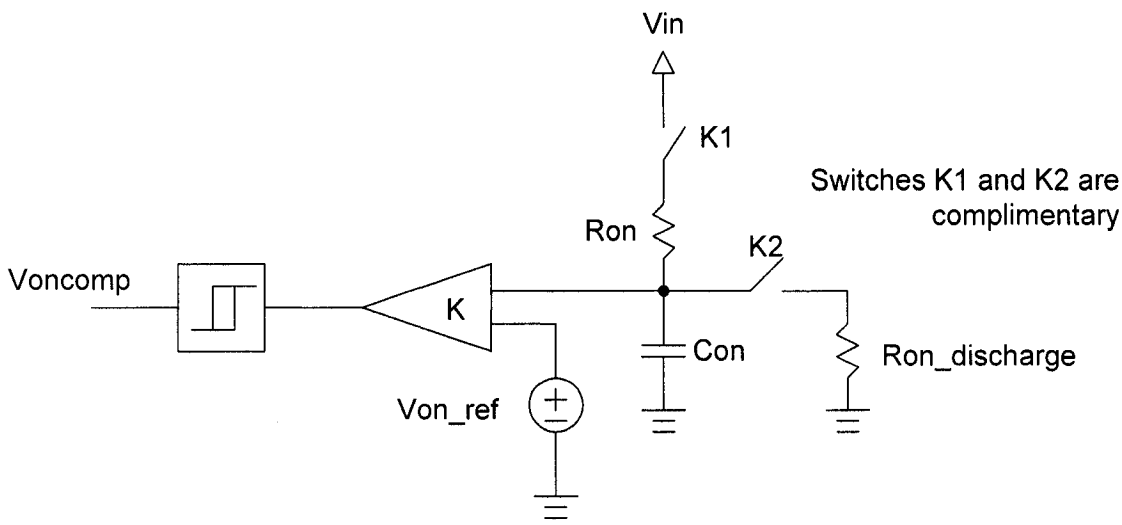


Figure 5-2: ON-TIME circuit

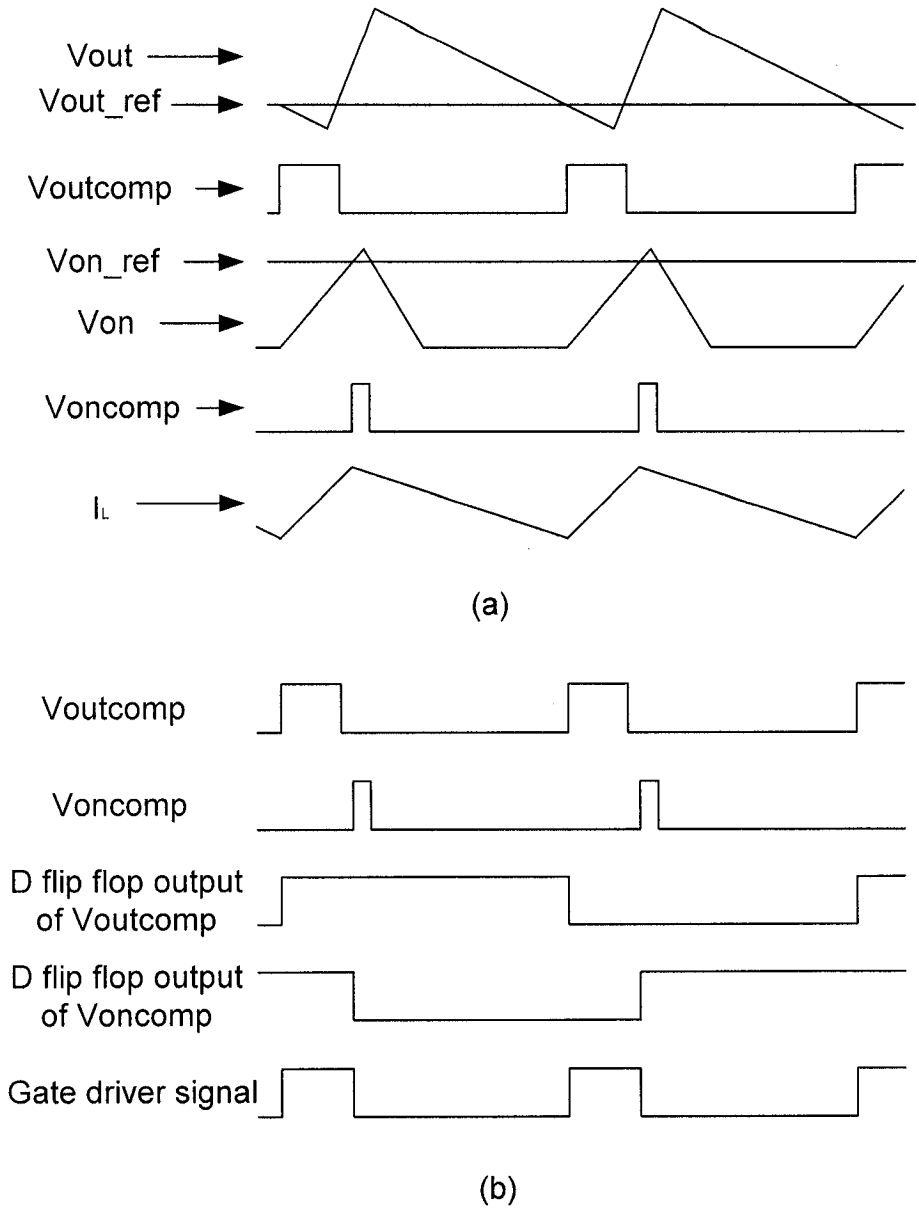


Figure 5-3: Proportional on time controller timing
(a) ON-TIME and OFF-TIME timing
(b) Logic circuit for ON-TIME control

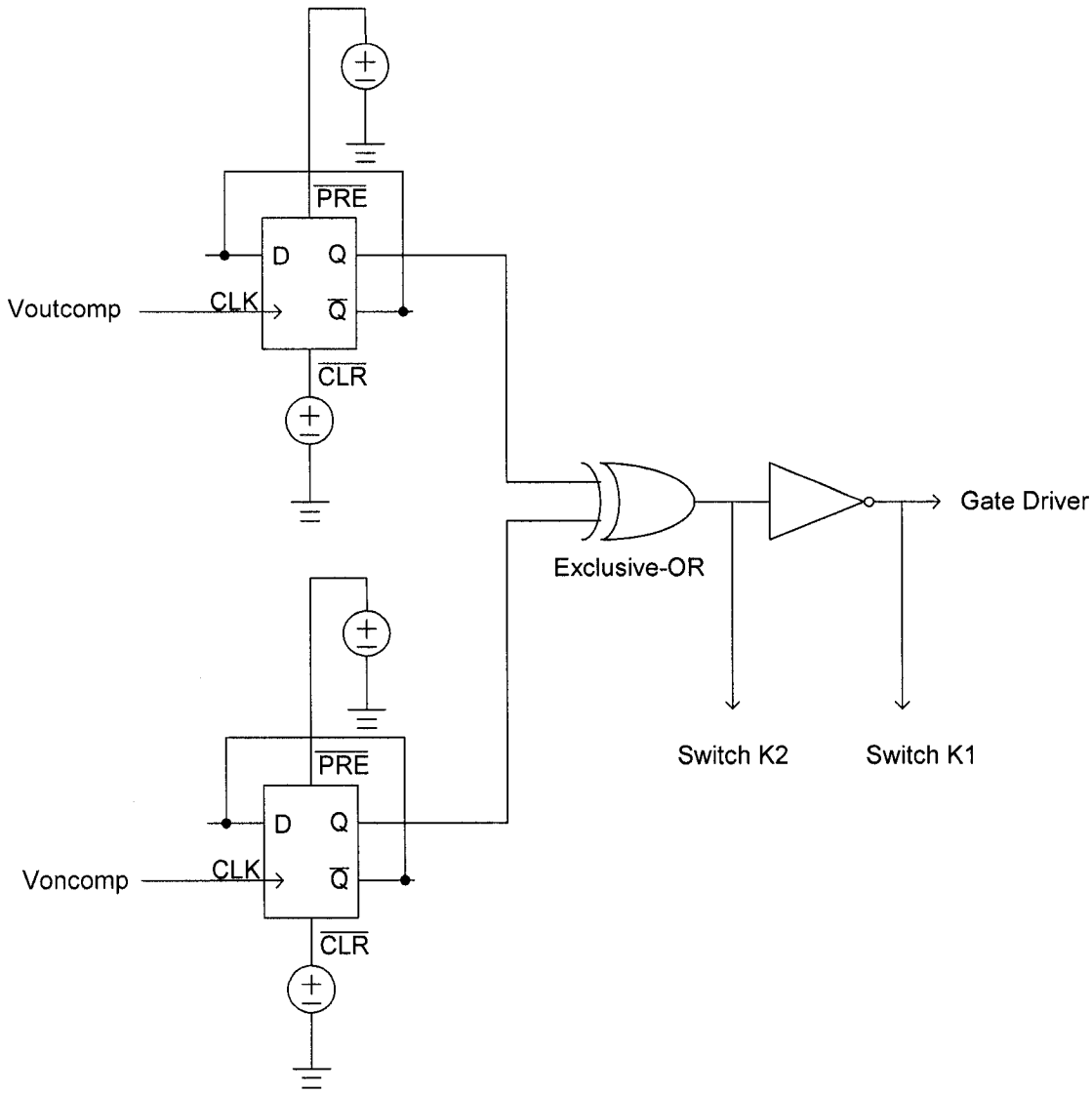


Figure 5-4: On time control logic schematics

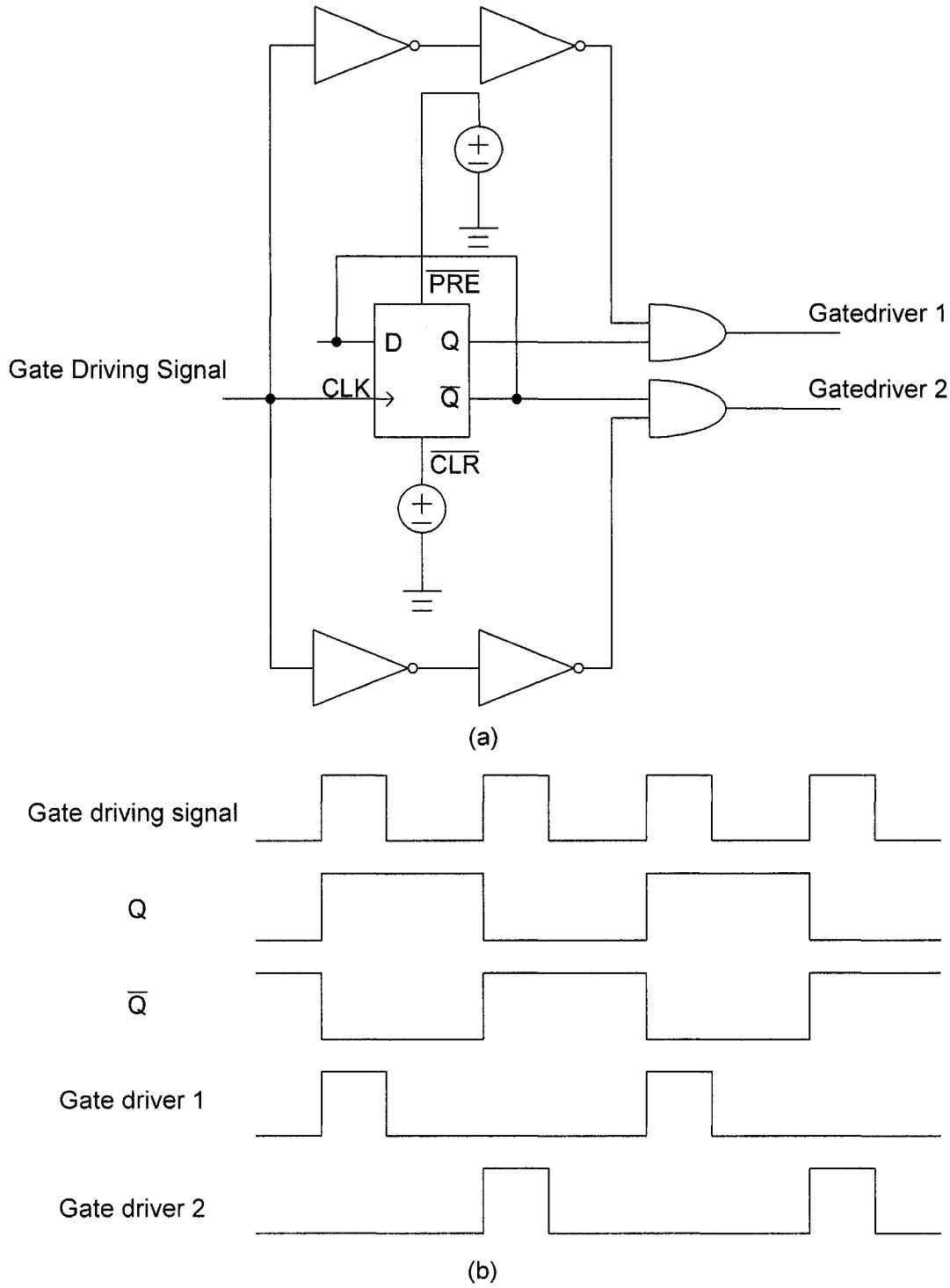


Figure 5-5: Gate driver signals and their logic
(a) Gate driving signal for a two-phase VRM
(b) Gate driving signal logic

Table 5-1: Simulation Parameter Values

	Single Phase	Two Phases
Inductor	1uH	500uH each phase
Connection resistance	0.5mΩ	0.5mΩ each phase
Switch on resistance	2 mΩ	2 mΩ
Output capacitor	220uF	220uF
Load resistance	10 mΩ	10 mΩ
Input voltage	9V~20V	9V~20V
Output voltage	1V	1V

5.3 Simulation Results for Proportional ON-TIME Voltage Hysteretic Control

Simulations were done for both single phase and two phases VRMs using proportional on time control method. The simulation parameter values are listed in Table 5-1.

Simulation results for single phase VRM are shown in Figure 5-6 - Figure 5-8. Figure 5-6 is with 9V input, Figure 5-7 is with 15V input and Figure 5-8 is with 20V input. The bottom waveforms are the output voltage and its hysteretic window is at low limit. Since the bandwidth of this system is not high enough, the output voltage has a undershoot, that is, a little lower than the low limit.

The waveforms of V_{on} and V_{on_ref} are waveforms of the on time duration control signals. When the high-side switch turns on, the capacitor C_{on} begins to charge until it hits the on time reference voltage $V_{on\text{-}ref}$. Then, the high-side switch turns off and the capacitor starts to discharge. In this simulation, $R_{on}=250k$ and $C_{on}=4p$. These two values make the switching frequency around *500kHz*. Improving these two values can decrease the switching frequency while reducing those values can increasing the frequency.

The simulation shows that, the total frequency variation is between *500kHz* to *540kHz*, less than 10%. This variation is generated by the power dissipation in the power stage, such as switch on-resistance, component ESR and connection resistance. Those values make the duty ratio nonlinear and they are never considered at design procedure since they are random and discrete.

Figure 5-9 shows the logic of the gate driving signal. The bottom waveforms are waveforms of two D-type flip-flop outputs.

From Figures 5-6, 5-7, and 5-8, we can see the excellent advantage of the proportional on time control, the advantage being that the output current ripple and voltage ripple are almost the same regardless of the input voltage and the duty ratio is. This is very helpful for choosing a output capacitance value.

A simulation result for two-phase VRM is shown in Figure 5-10. Figure 5-11 shows the control logic of two-phase VRM. The first two waveforms are gate drivers for two high-side switches. The third comes from the forth waveform via a frequency divider mentioned previously (The frequency divider is the output of D-type flip-flop output in Figure 5-5 (a)). And the forth one is the original gate driving signal coming from the proportional on time and hysteretic control. They are exactly the same as in single-phase controller.

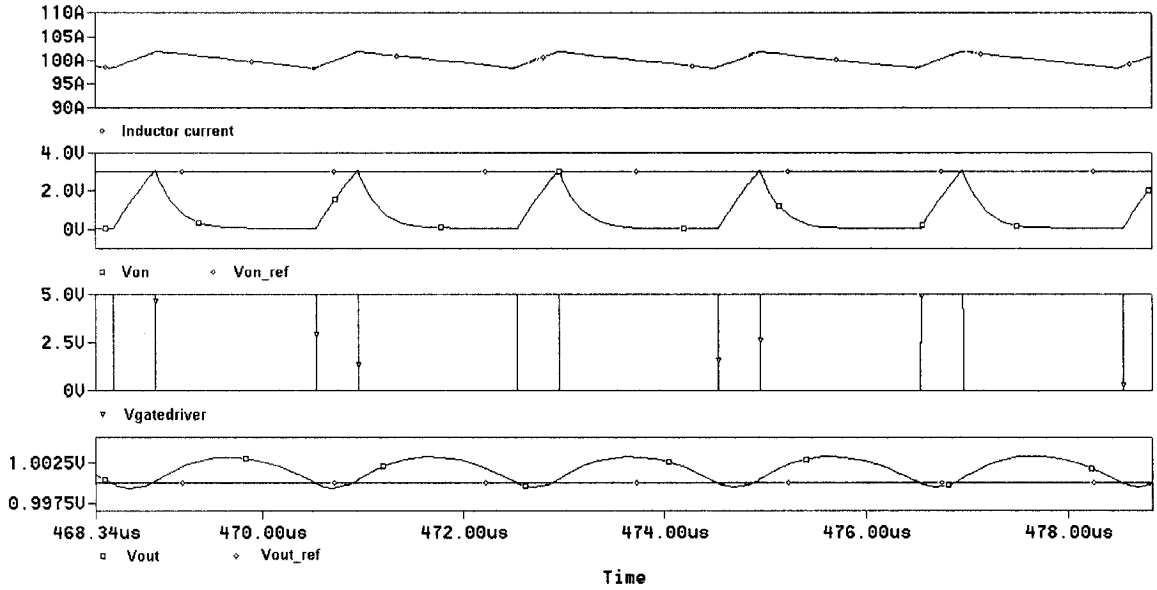


Figure 5-6: Single phase @ 9V input

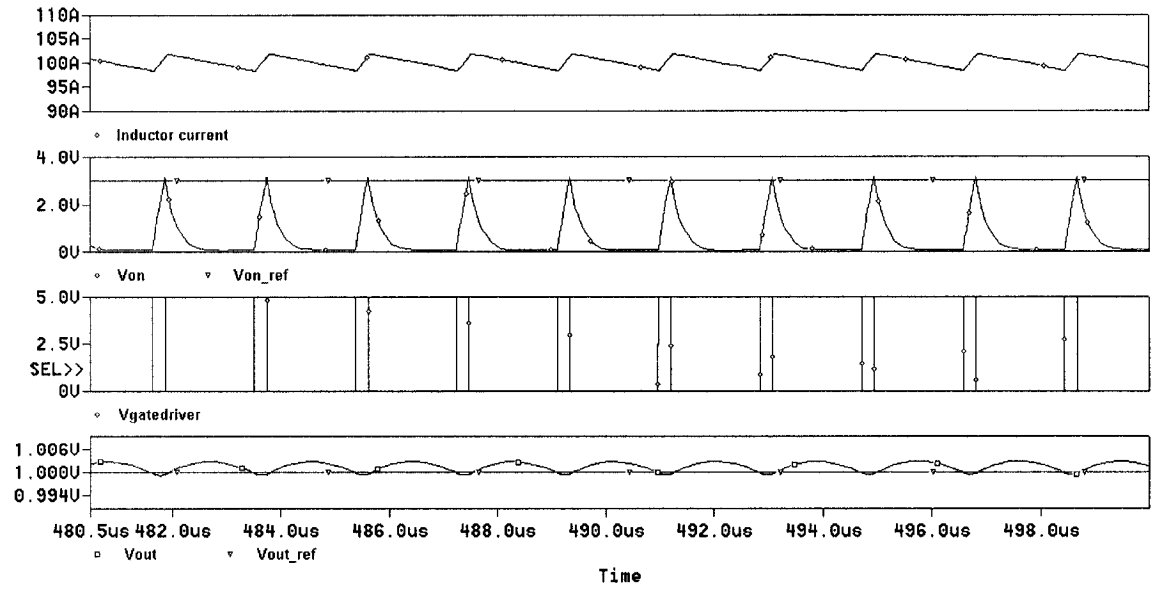


Figure 5-7: Single phase @ 15V input

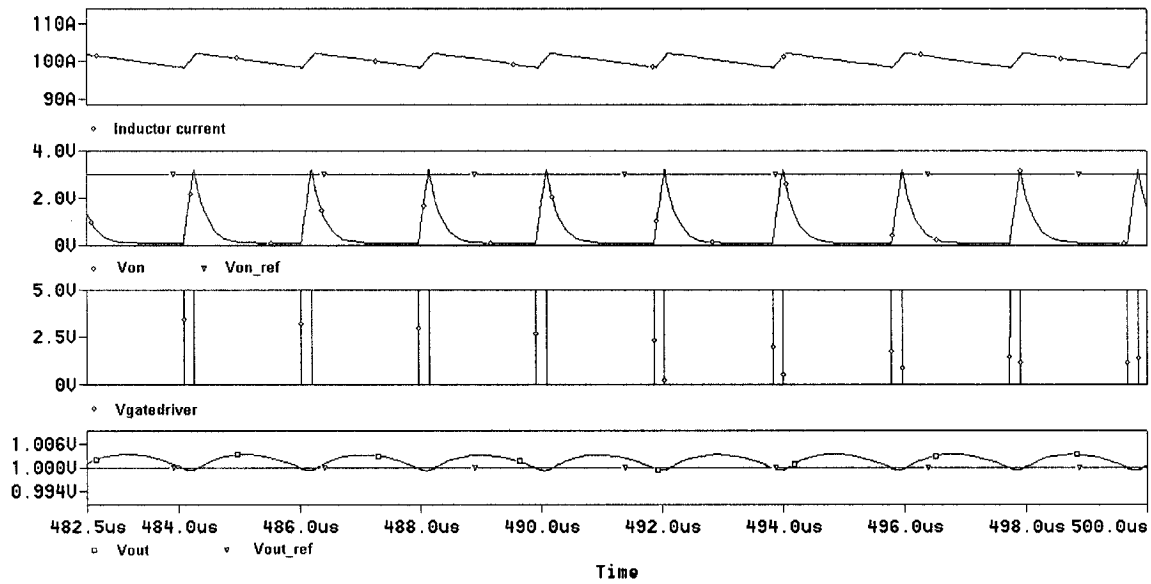


Figure 5-8: Single phase @ 20V input

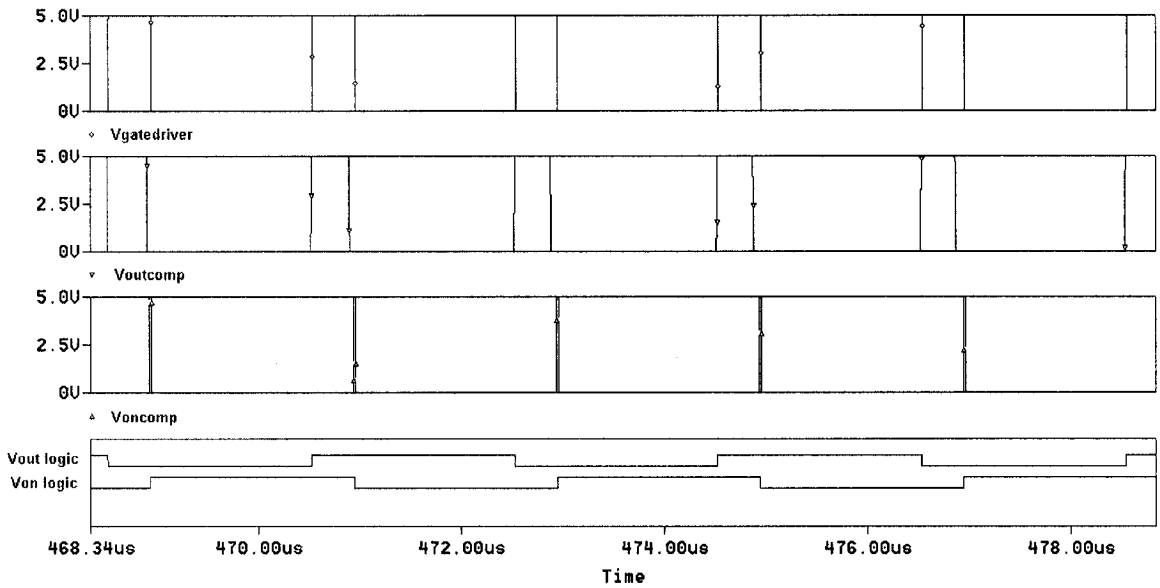


Figure 5-9: Gate driving signal @ 9V input

5.4 Current Sharing

Current sharing issues are a key point in multiphase VRM control. In proportional control, this is easily achieved and only a small amount of extra circuitry is added for average current sensing and ON-TIME reference voltage adjusting.

The goal of current sharing is to adjust the duty ratio in each phase. If the inductor current is higher, the duty ratio will be reduced. The duty ratio depends on the reference voltage and the capacitor charging speed, so it is easy to understand that adjusting the reference voltage can change the on time duration.

This is why we use the RC network to sense the average phase current. As we know, this voltage is proportional to the phase current. Therefore, we only need to feed it back to the reference voltage as shown in Figure 5-12. The output of "comp1" comes from V_{on_ref} minus V_1 and the output of "comp2" comes from V_{on_ref} minus V_2. Obviously, if phase 1 current is larger than phase 2, V_1 is also larger than V_2, so V_{comp1} is smaller than V_{comp2}. To be noted, the switches "S1" and "Son1" operate synchronously so do the "S3" and "Son2". Therefore, high-side on time duration of phase 1 is smaller than high-side on time duration of phase 2 since the on time reference voltage of phase 1 is smaller.

The timing of all the switches is given in Figure 5-13. It is clear that no extra logic circuit is needed.

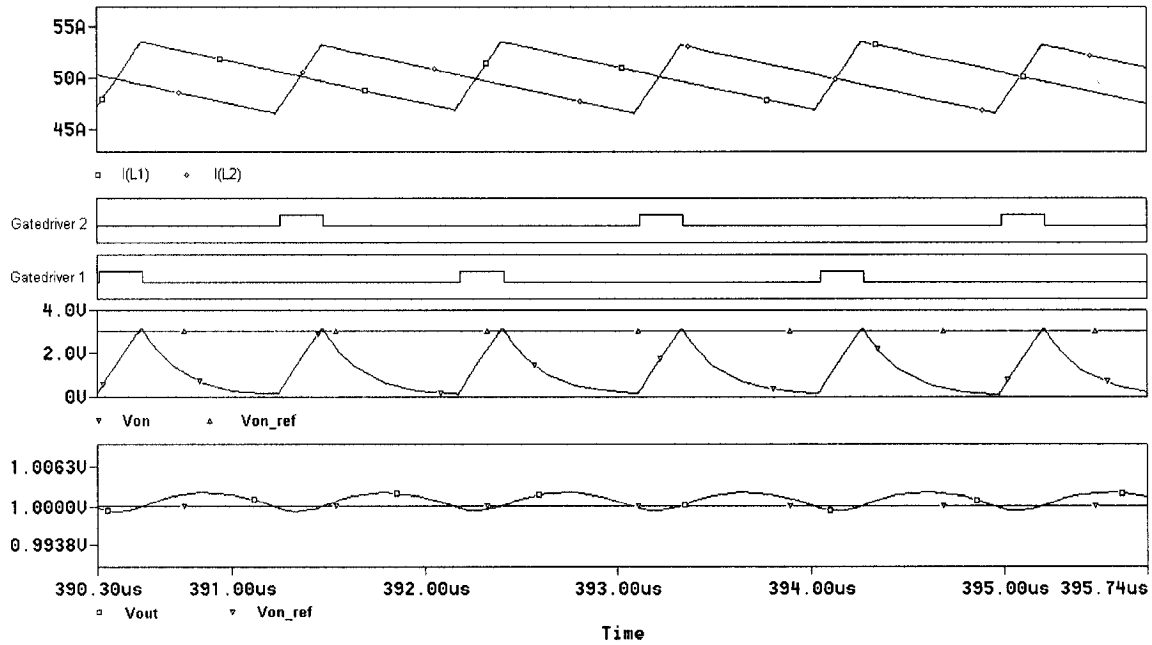


Figure 5-10: Two-phase VRM @ 15V input

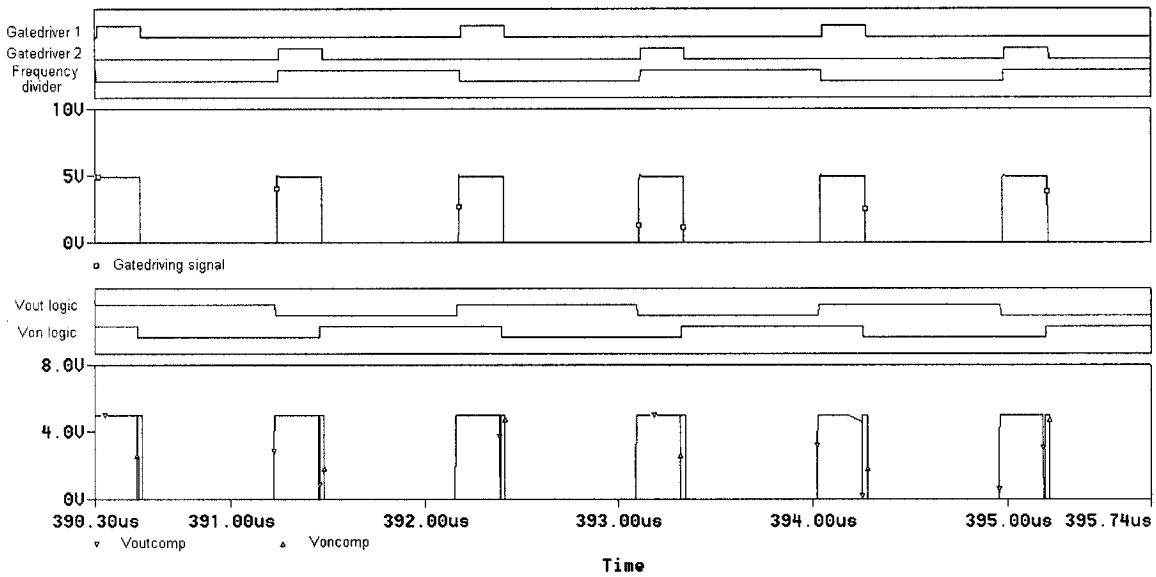


Figure 5-11: Control logic of two-phase VRM

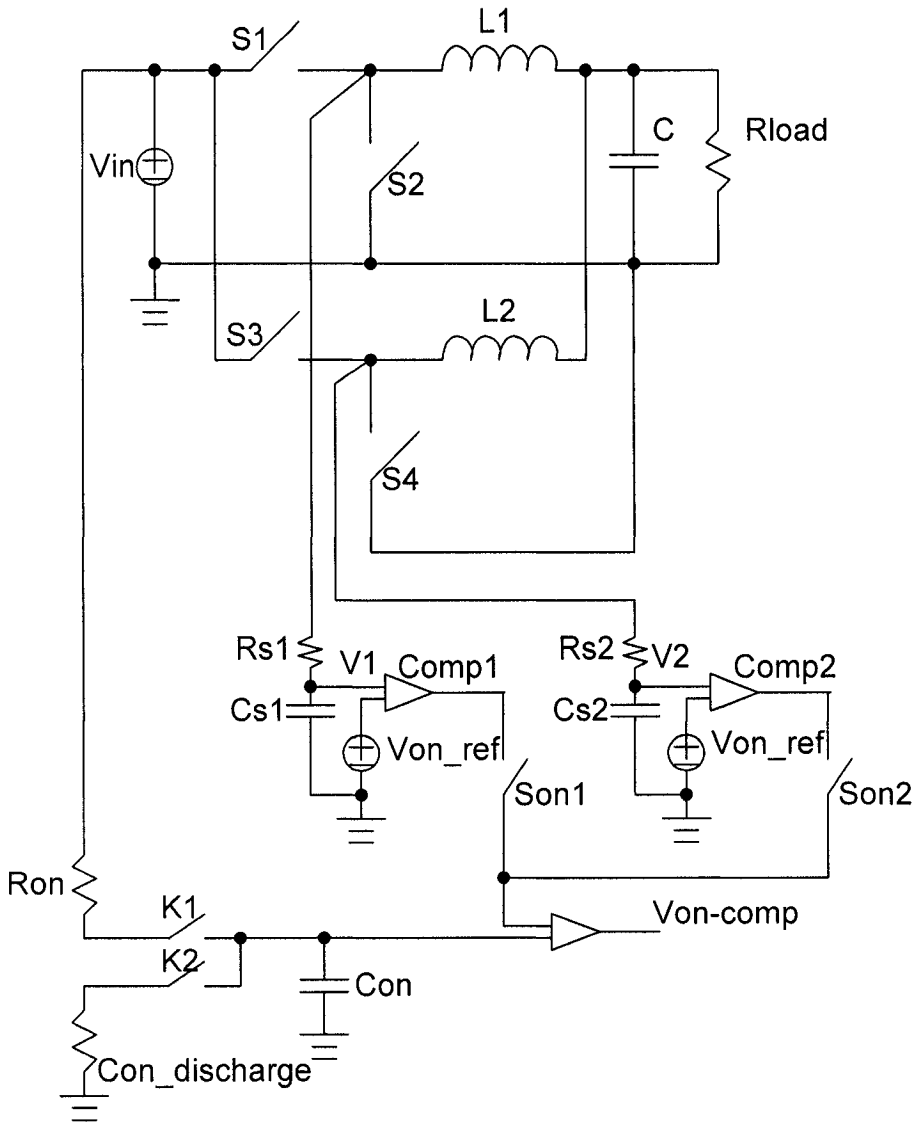


Figure 5-12: Current sharing control

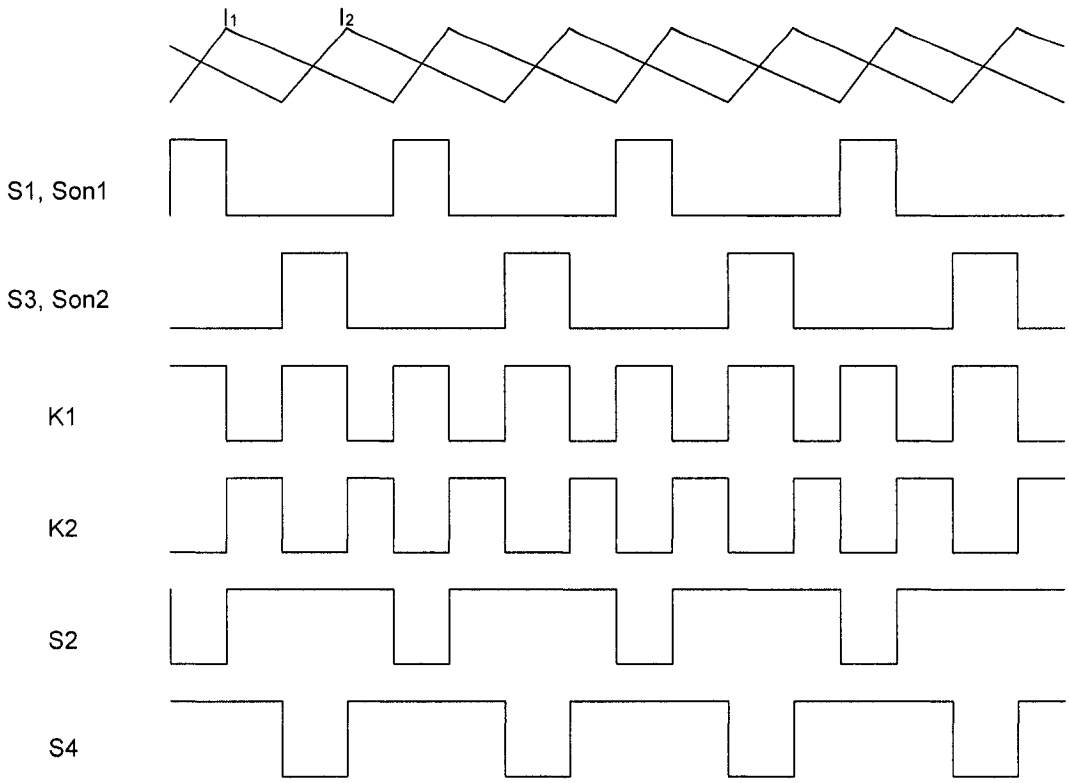


Figure 5-13: Current sharing switch timing

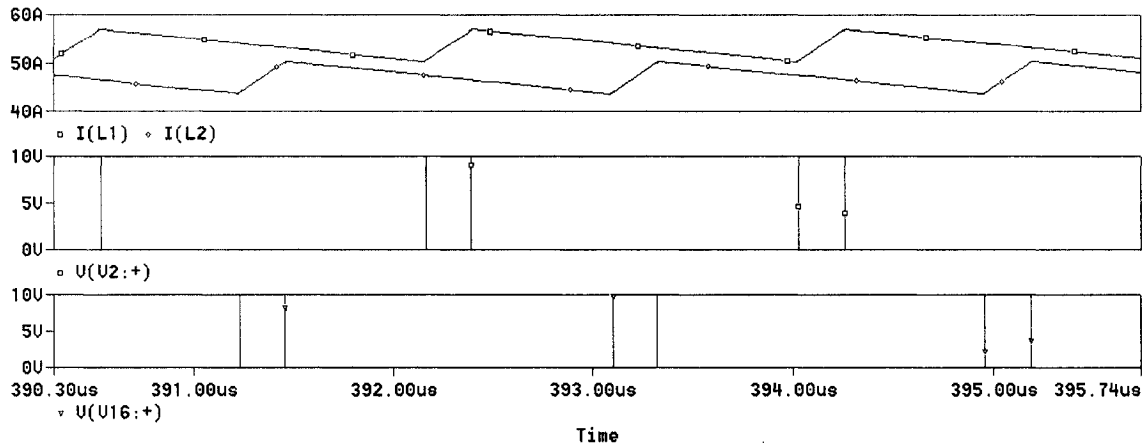


Figure 5-14: Two-phase VRM phase current without current sharing

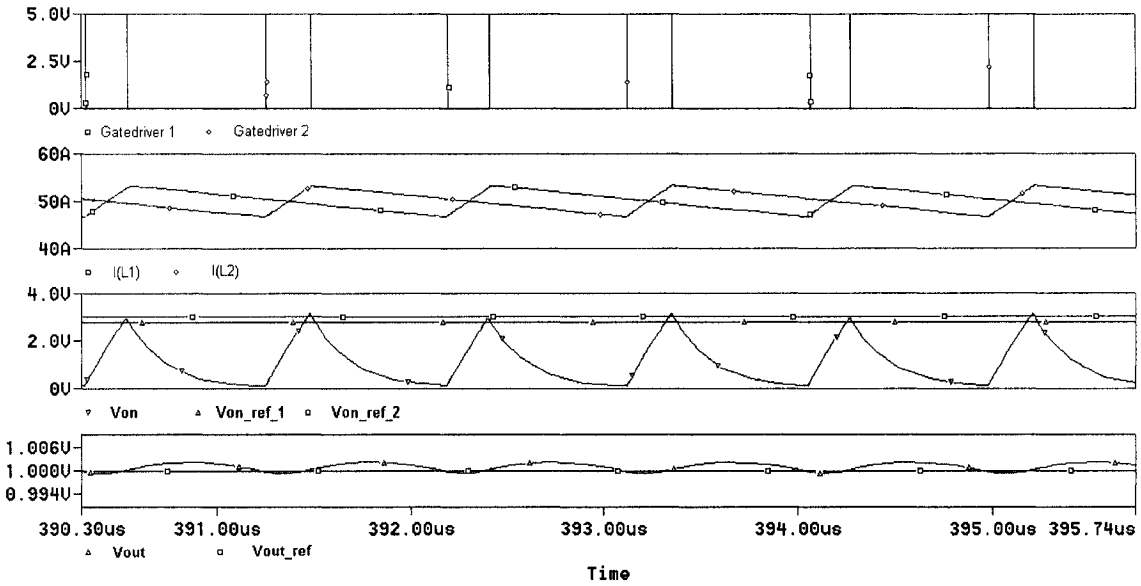


Figure 5-15: Two-phase VRM phase current with current sharing

5.5 Simulation Results for Current Sharing

Simulation results for a two-phase VRM without current sharing are shown in Figure 5-14. The total loop resistance in phase 1 is 0.2Ω while the total loop resistance in phase 2 is 0.5Ω. All the rest of the components in these two phases remain the same. The current difference is around $8A$ which is almost 16% of the average phase current.

The simulation result for current sharing is shown in Figure 5-15. These phase currents are almost the same. Although in figures do not make it clear, it is noticeable that the gate-driving signal of phase 1 is a little bit smaller than phase 2. The V_{on_ref} for the two phases has a difference of about $0.3V$. It is very clear that the peak voltage across the ON-TIME charging capacitor is not equal in phase 1 and phase 2 ON-TIME. Therefore, it can achieve the current sharing by adjusting the on time duration.

5.6 Block Diagram of the Proportional ON-TIME Hysteretic Control with Current Sharing

The block diagram of the proportional on-time hysteretic control with current sharing is shown in Figure 5-16. For simplification, it only shows two phases and the configuration is similar for four phases.

The function of current sharing block is to set up the ON-TIME reference voltage for all the phases. The function of Ton block is to set up the ON-TIME duration for different

phases. The function of the hysteretic window block is to set up the output voltage reference and the all-on and all-off control limits for fast transient. The function of the Toff block is to set up the off-time duration which should have minimum off-time limitation. The function of fast transient block is to set up the all-on and all-off signals if the output voltage is overshoot or undershoot. The function of the logic block is to enable or disable the gate driving signals for all phases at start process, fast transient, regular condition as well as over-voltage, under-voltage, over-current protections.

5.7 Experiment Results

Experiments were completed for verifying this control method. The key components we used are listed below

1. COOPER BUSSMANN DR127-2R2 inductor: *2.2uH*, *12.5A* I_{rms}, *25.5A* I_{sat}, *4mΩ* DCR (for single phase)
2. COOPER BUSSMANN DR127-1R0 inductor: *1.0uH*, *15.5A* I_{rms}, *40A* I_{sat}, *3mΩ* DCR (for two phases)
3. IRF7809 MOSFET: *30V* V_{DS}, *14.2A* I_D, *8.5mΩ* R_{DS}
4. Panasonic SP series EEFUEOE 221R capacitor: *220uF*, *2.5V*, *25mΩ* ESR
5. Semtech SC1205 high speed synchronous power MOSFET driver: *12ns* t_r and t_f, *3A* peak drive current

The experiment instruments are Tektronix TDS360 two-channel scope, Tektronix TM502A current probe, and Chroma 63103 DC electronic load.

5.7.1 Single Phase Experiment Results

Figure 5-17 ~ Figure 5-21 are waveforms of output voltage and high-side gate driving signals for single phase VRM. The input voltage varies from *9V* to *20V* while the output voltage is fixed at *1.2V*. The peak-to-peak output voltage ripple is 25 - *30mV*. Considering the small capacitor value, these are very satisfactory results.

To be noted, the magnitude of high-side driving signal in Figure 5-17 - Figure 5-21 is different. This is because the scope 's ground is not channel-to-channel isolated and the ground is taken at the power ground. Hence, the magnitude is not the actual magnitude across high-side MOSFET's gate and source and the high-side gate driving is floating driving.

5.7.2 Frequency Comparison between ON-TIME Control and Hysteretic Control

The switching period and frequency variation of ON-TIME control can be obtained in Table 5-2 and Table 5.3, respectively. The total switching frequency variation is 14%. Compared with voltage hysteretic control of *20mV* hysteretic window shown in Table 5.4, ON-TIME control has less frequency variation. TO be noted, the total switching frequency variation of voltage hysteretic control is 23% which is based on average value at a specific input voltage. The actual switching frequency at a fixed input voltage has

large deviation, no less than 10%, so the switching frequency variation range for hysteretic control is much wider.

5.7.3. Two Phase Experiment Results

Figure 5-22 - Figure 5-25 are waveforms of output voltage and output current for two-phase VRM. All the current steps are form *8A* to *20A* and from *20A* to *8A*, both at the current slew rate of *2.5A/us*. This is the maximum dynamic current output of the Chroma 63103. Since the current slew rate is not large enough, the output voltage changes very slowly, and no voltage spike is observed.

The total output voltage variation is *50mV*. This value can be reduced if the load is put on the same printed circuit board and close to the VRM output. The steady state voltage ripple is *15 ~ 20mV* which is smaller than the single-phase voltage ripple due to the interleaving configuration.

The high-side driving signal during the transient is shown in Figure 5-26 - Figure 5-29. Since the current slew rate is not high enough, the voltage transient is slow and no voltage spike is observed. The transient process is still clear. The driving signal is high density when the load changes from light to heavy and it becomes low density when the load changes oppositely.

There is a $50mV$ voltage drop with current increasing. This is long wires are used for connecting the power stage and the electronic load. Since the feedback point is at the output end of the power stage, the connection resistance is not compensated.

5.8 Summary

A proportional ON-TIME voltage hysteretic control is presented in this chapter. It can provide simple solution to a wide range of input voltage variation and save a pre-stage converter. This can minimize the physical size and cut cost. Compared with voltage hysteretic control, it has less frequency deviation, i.e. low EMI issue while keeps the identical fast transient. Compared with PWM control, it limits the minimum ON-TIME duration, so it has higher efficiency. The Simulation results and experiment results prove this idea.

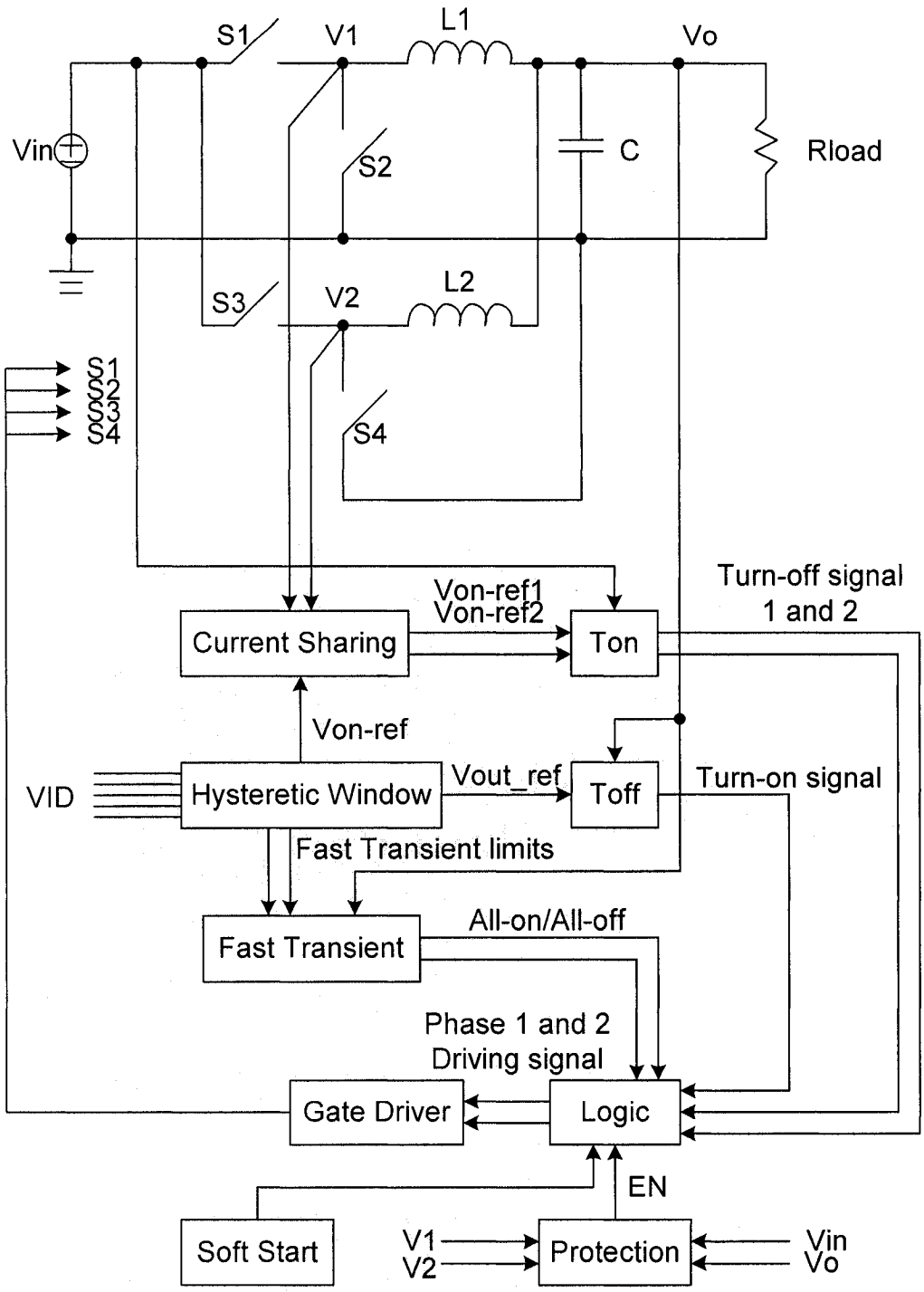


Figure 5-16: Block diagram

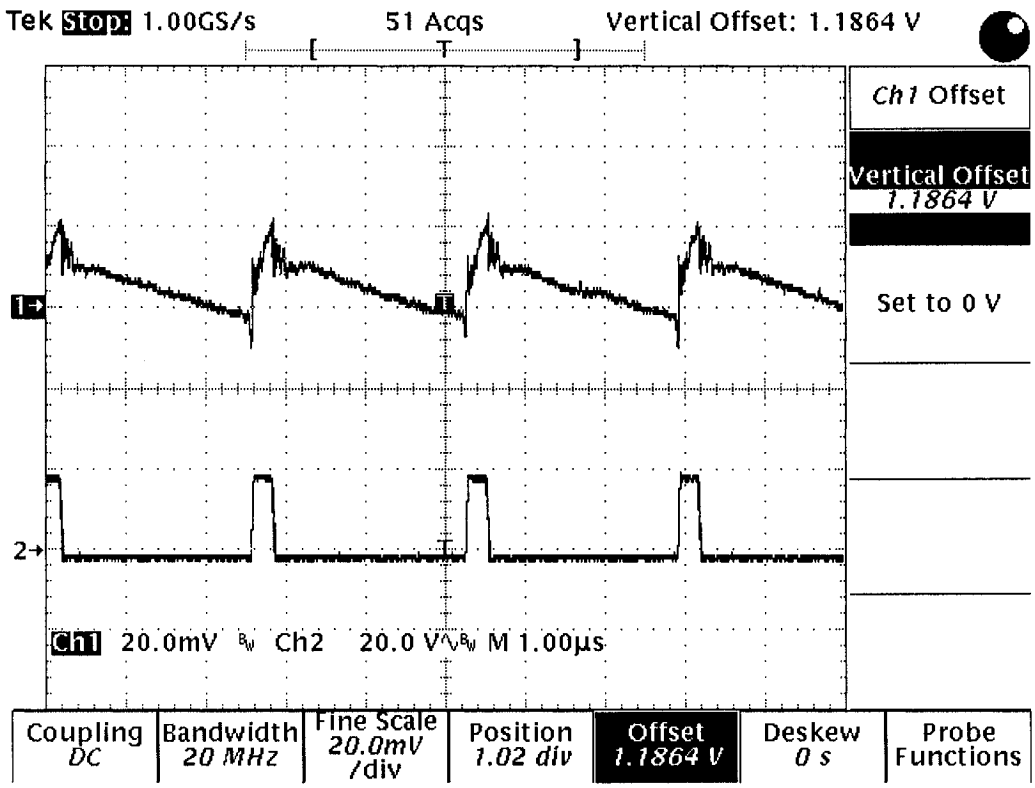


Figure 5-17: Waveforms of Single-phase 15V input 1.2V output @ 10A output current
Upper: output voltage with 30mV peak-to-peak ripple
Lower: high-side gate driving signal

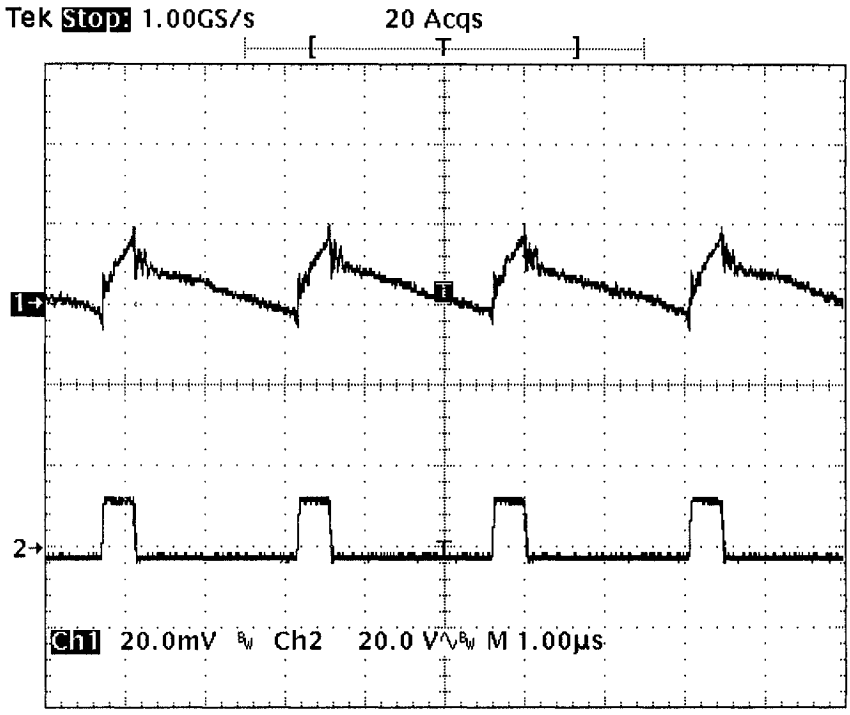


Figure 5-18: Single-phase 9V/1.2V 10A output voltage waveform

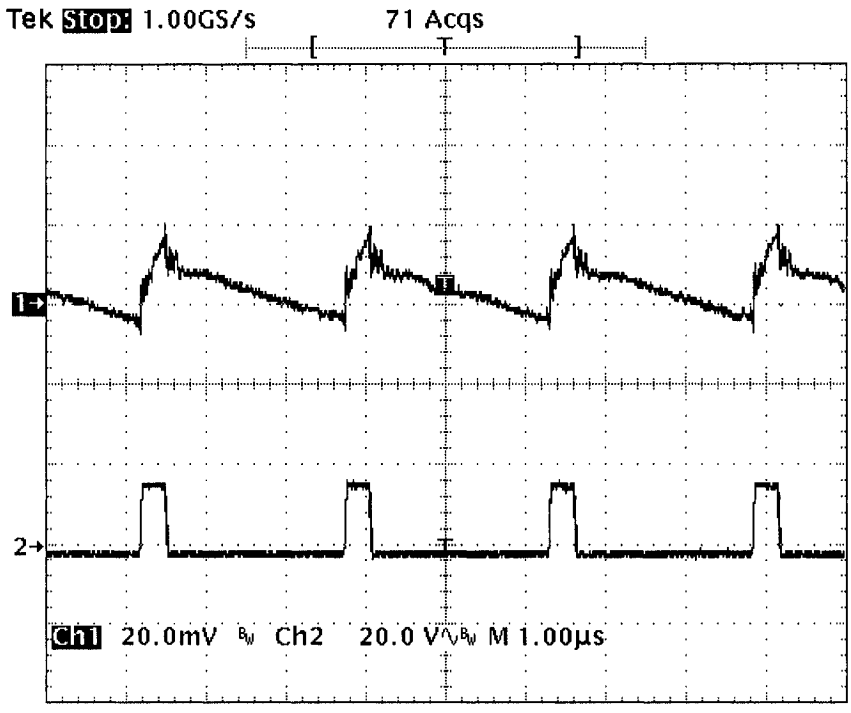


Figure 5-19: Single-phase 12V/1.2V 10A output voltage waveform

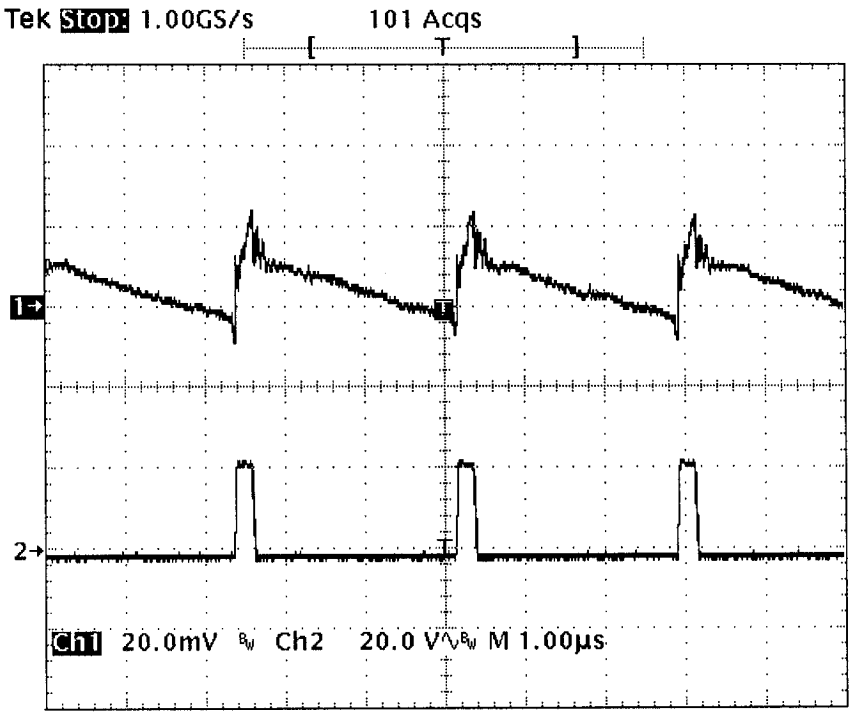


Figure 5-20: Single-phase 18V/1.2V 10A output voltage waveform

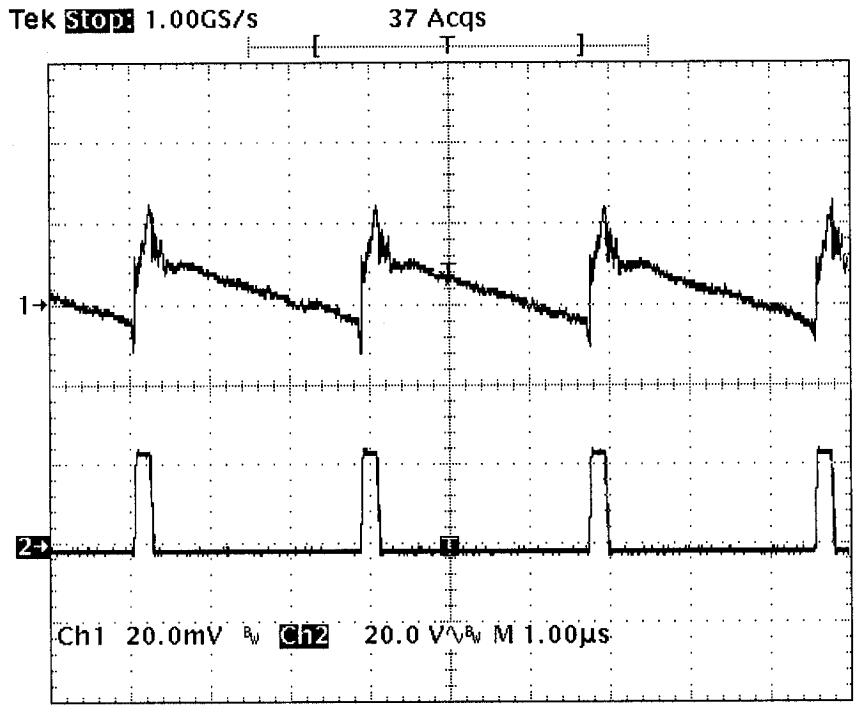


Figure 5-21: Single-phase 20V/1.2V 10A output voltage waveform

Table 5.2: ON-TIME Control Input Voltage vs. Switching Frequency

Input voltage (V)	Switching period (uS)
9	2.46
12	2.56
15	2.67
18	2.78
20	2.86

Table 5.3: Input Voltage vs. Switching Frequency

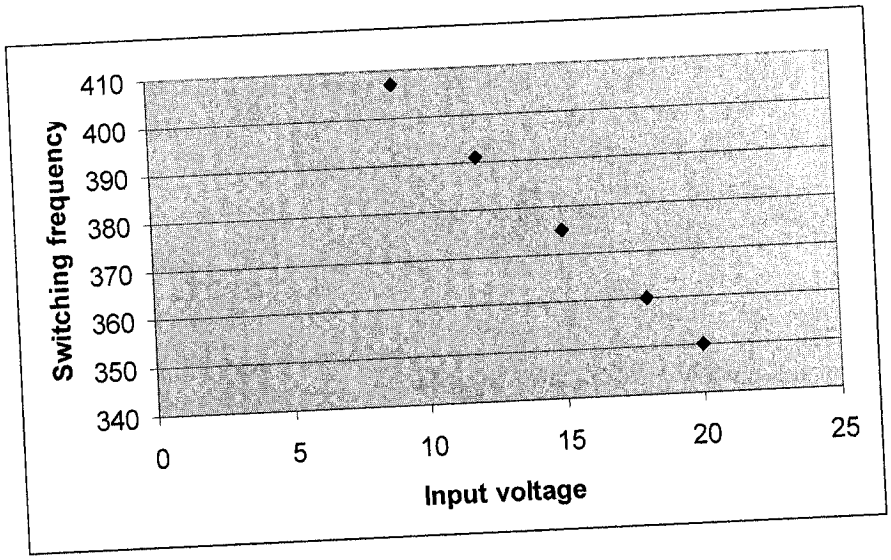
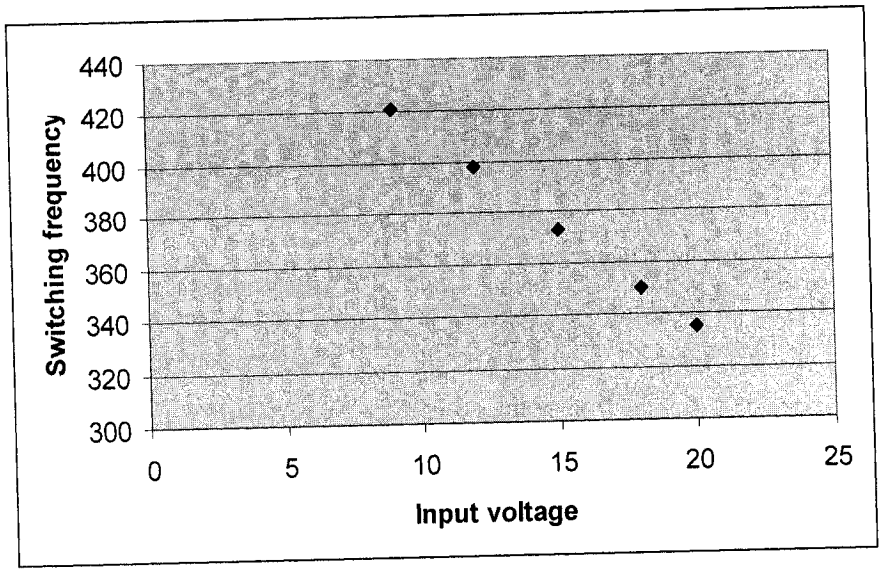


Table 5.4: Voltage Hysteretic Control Input Voltage vs. Average Switching Frequency



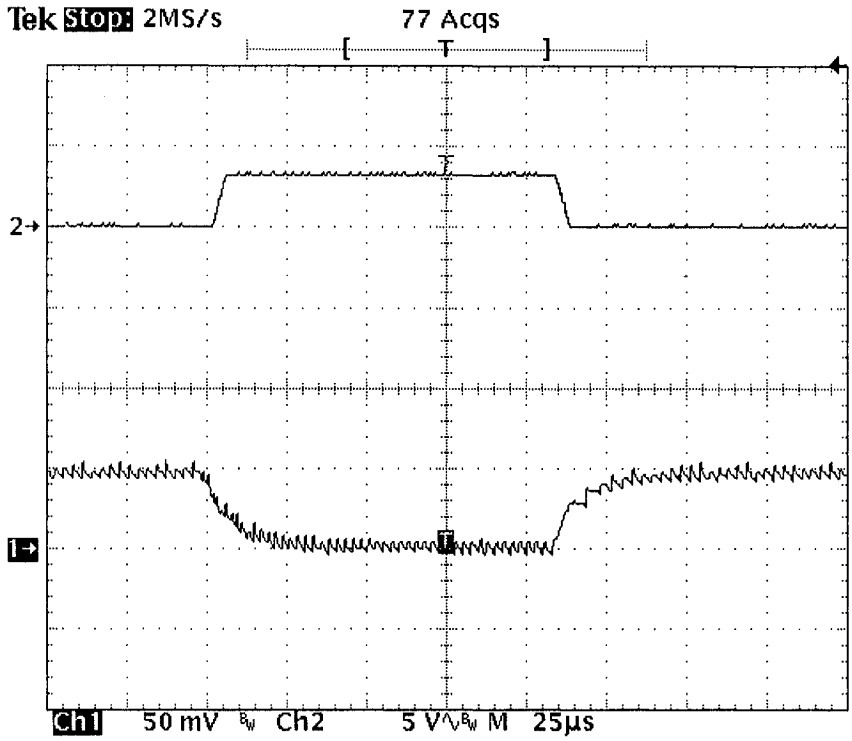


Figure 5-22: Two phases 10V input 1.2V output VRM @ 20A/8A

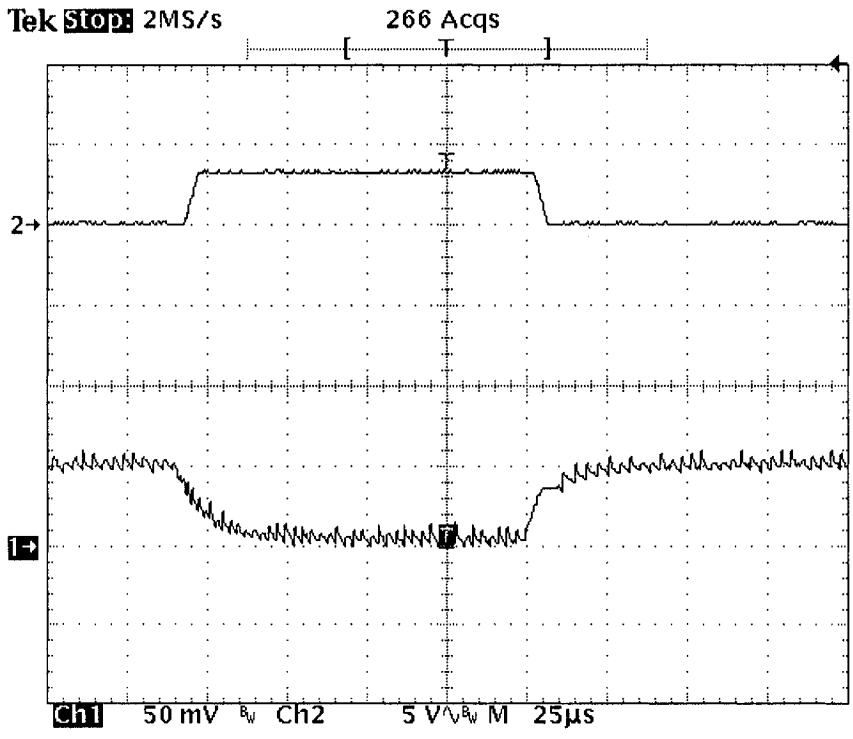


Figure 5-23: Two phases 15V input 1.2V output VRM @ 20A/8A

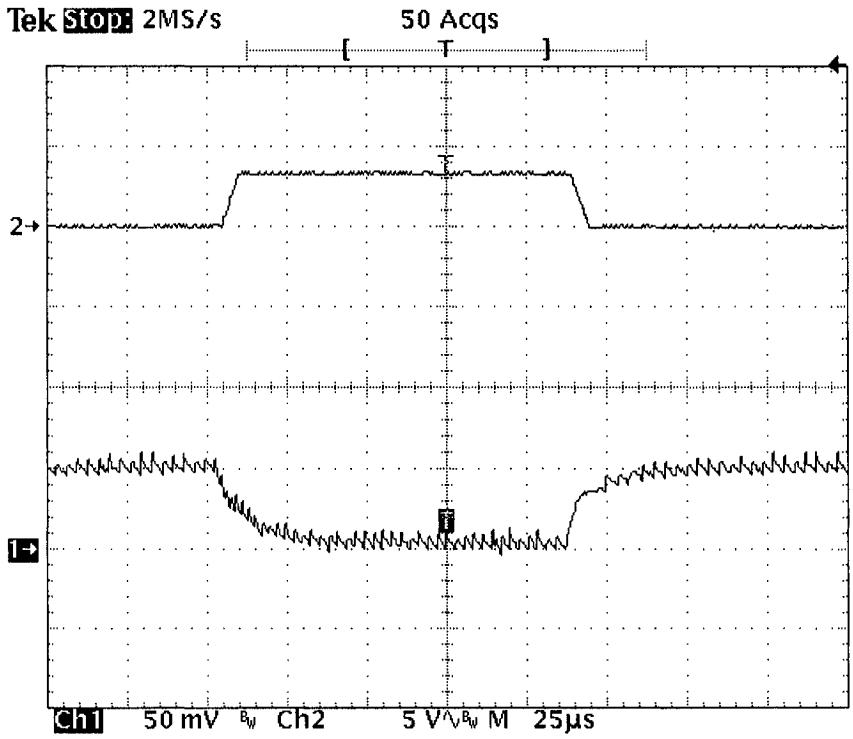


Figure 5-24: Two phases 20V input 1.2V output VRM @ 20A/8A

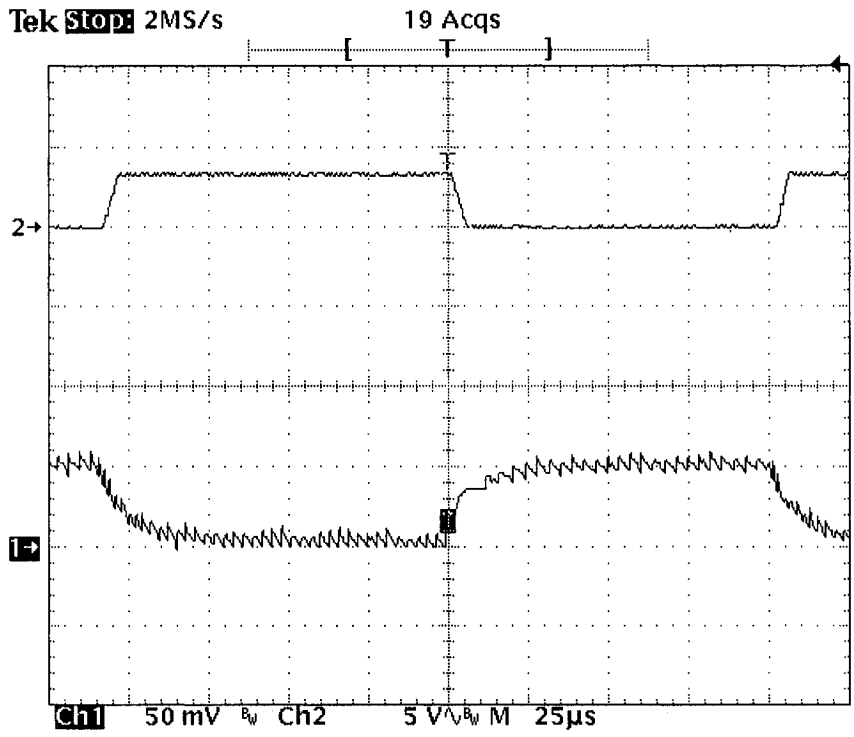


Figure 5-25: Two phases 25V input 1.2V output VRM @ 20A/8A

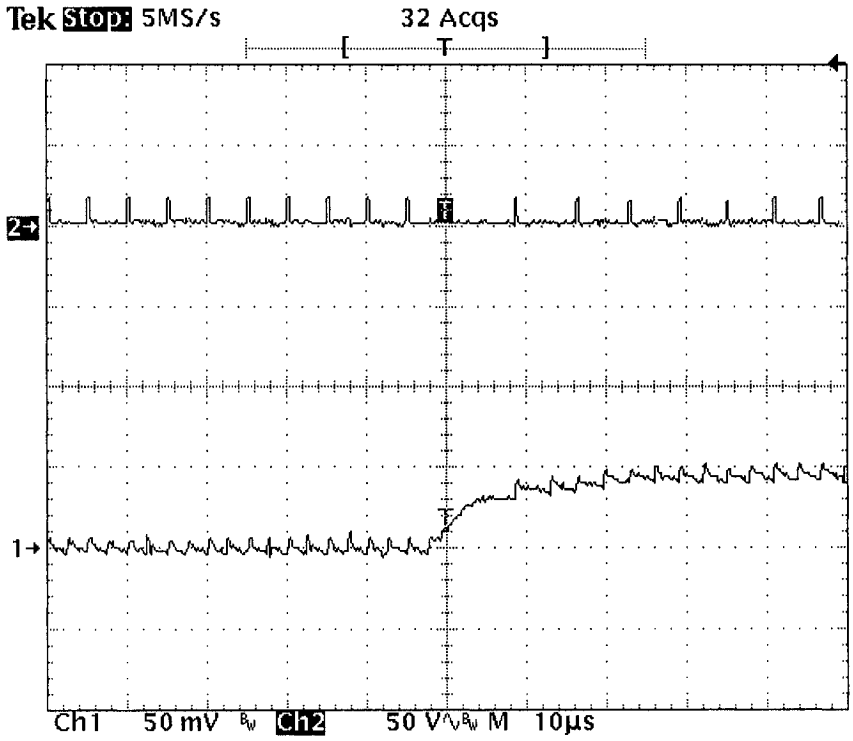


Figure 5-26: High-side driving signal @ *10V* input

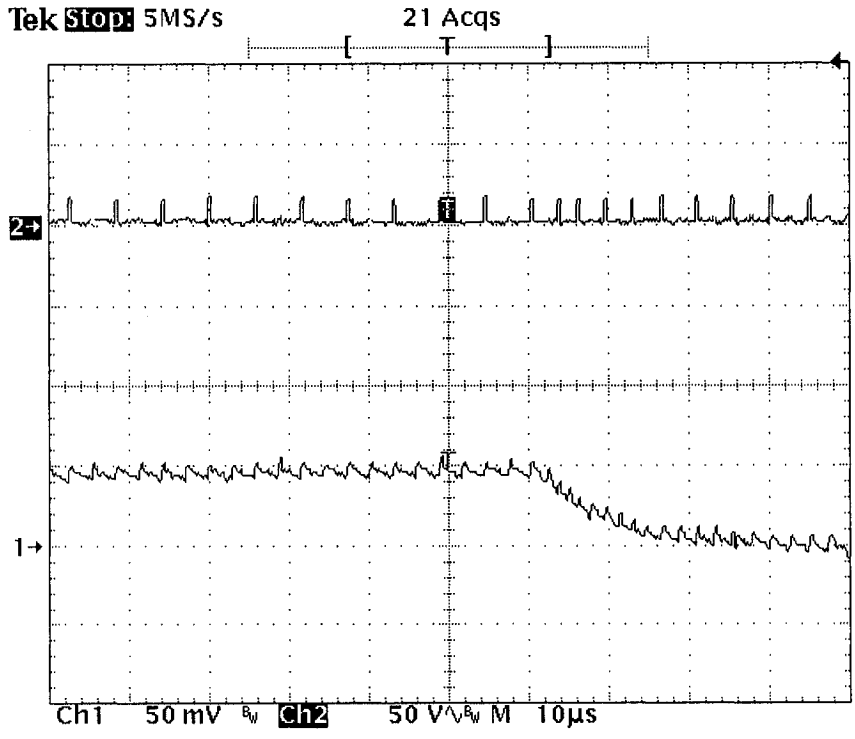


Figure 5-27: High-side driving signal @ *12V* input

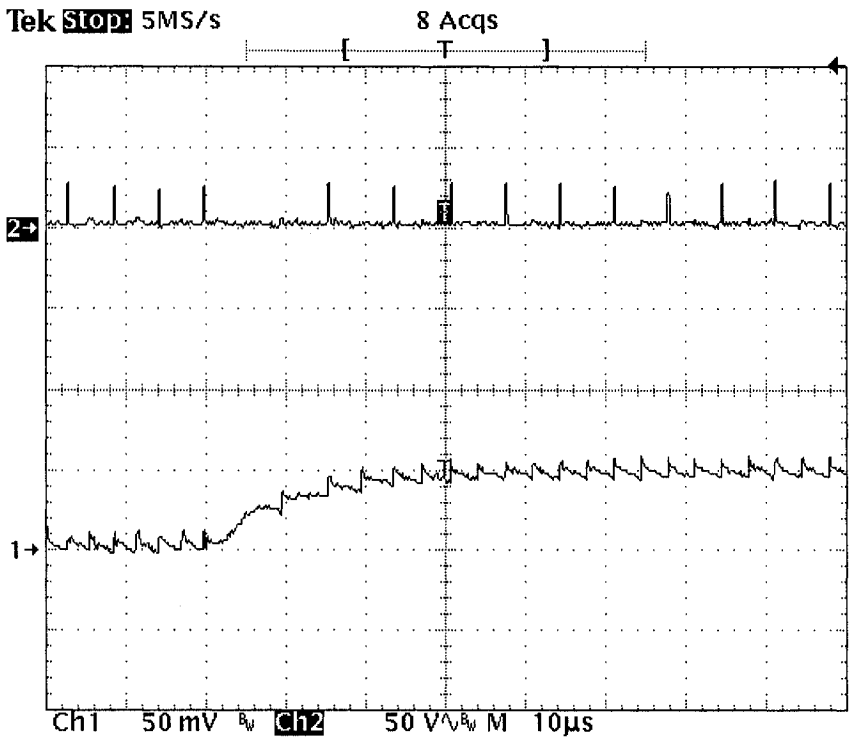


Figure 5-28: High-side driving signal @ *18V* input

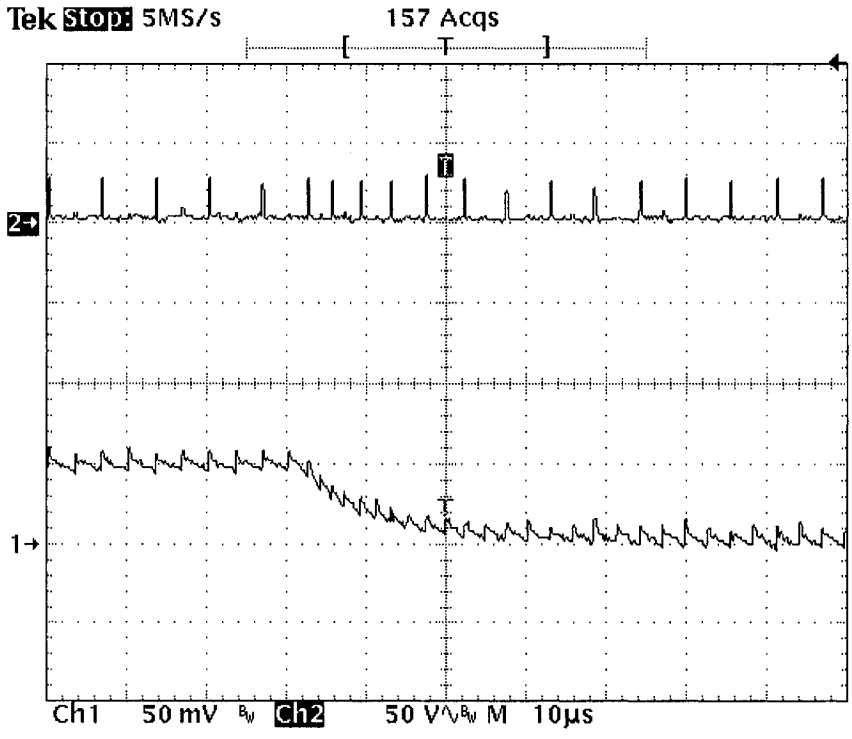


Figure 5-29: High-side driving signal @ *20V* input

References

[1] SC1476 datasheet from Semtech Corporation

[2] Wang, T.G.; Xunwei Zhou; Lee, F.C.; "A low voltage high efficiency and high power density DC/DC converter", Power Electronics Specialists Conference, 1997. PESC '97 Record, 28th Annual IEEE, Volume 1, 22-27 June 1997 Page(s): 240 -245

[3] Redl, R.; Erisman, B.P.; Zansky, Z.; "Optimizing the load transient response of the buck converter", Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998, Thirteenth Annual, Volume: 1, 15-19 Feb. 1998 Page(s): 170 –176

[4] Xunwei Zhou; Donati, M.; Amoroso, L.; Lee, F.C.; "Improved light-load efficiency for synchronous rectifier voltage regulator module", Power Electronics, IEEE Transactions on, Volume 15 Issue 5, Sept. 2000 Page(s): 826 -834

[5] SC1470 datasheet from Semtech Corporation

[6] Suntio, T.; "Small-signal modeling of switched-mode converters under direct-on-time control-a unified approach", IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the], Volume: 1, 5-8 Nov. 2002 Page(s): 479 -484 vol.1

[7] Chen, D.S.; Lai, J.S.; "A study of power correction boost converter operating at CCM-DCM mode", Southeastcon '93, Proceedings. IEEE , 4-7 April 1993 Page(s): 6

[8] Sung-Soo Hong; Byungcho Choi; "Technique for developing averaged duty ratio model for DC-DC converters employing constant on-time control", lectronics Letters, Volume: 36 Issue: 5, 2 March 2000 Page(s): 397 –399

[9] Lippincott, A.C.; Nelms, R.M.; Garbi, M.; Strickland, E.; "A series resonant converter with constant on-time control for capacitor charging applications", Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990, Fifth Annual, 11-16 March 1990 Page(s): 147 –154

[10] Ridley, R.B.; "A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM", Power Electronics Specialists Conference, 1990. PESC '90 Record, 21st Annual IEEE, 11-14 June 1990 Page(s): 382 –389

CHAPTER SIX

CONCLUSION

The development of microprocessor applications attracts lots of competition in the area of controller design. It has become a large market for desktop and portable power management IC chip manufacturers. Companies like Texas Instrument, Maxim Integrated Products, Linear Technology, Intersil, Analog Devices, Semtech, and many others have put lots of energy and research into developing control methods and improving power stage topology. The focus is on development of a product with low cost, high flexibility, easy application, high efficiency and high reliability while meeting all the requirements from Intel and the pre-stage power supply manufacturers.

Meanwhile, not only the power management IC chip designers focus on the topology and control method R&D area, even the Intel Corporation itself puts forth much effort in finding advanced solutions for next generation Pentiums. This is because the power supply requirements for extreme speed microprocessors has become much stricter due to the very low VCC voltage and very high current. Biggest problem with those requirements is the huge current slew rate of the CPUs. Creating positive and negative *1A/ns* current slew rate at *100A* current level is an impossible mission for present VRMs.

This throws a big burden on the system board and requires huge expensive capacitors to be placed around the CPU for dynamic reasons only.

In this dissertation, advanced topologies and methods are presented to provide complete system solutions. Those solutions include an analog controller and a digital controller for VRMs used in popular buck-based topologies, and an active dynamic compensator for the microprocessor's dynamic features. Those are introduced in Chapter 3, 4 and 5 respectively. The complete system solution is presented in Figure 6-1.

The analog controller introduced in Chapter 5 has a unique advantage in portable applications due to the wide input voltage variation ranges. It could be considered a variable window voltage hysteretic control while the input parameter of the hysteretic window is the system input voltage. To conquer the wide variable range of the system input voltage, normally a two-stage topology is used to converter the system input voltage to a fixed value before it powers the VRMs as shown in Figure 6-2. Otherwise, the ON-TIME duration might be too short for a fixed frequency control like the PWM control, or the frequency variation is too large for hysteretic control. The multiphase proportional ON-TIME controller overcomes those shortages. Tt is also easy to get the current sharing control by adjusting the ON-TIME duration for each phase.

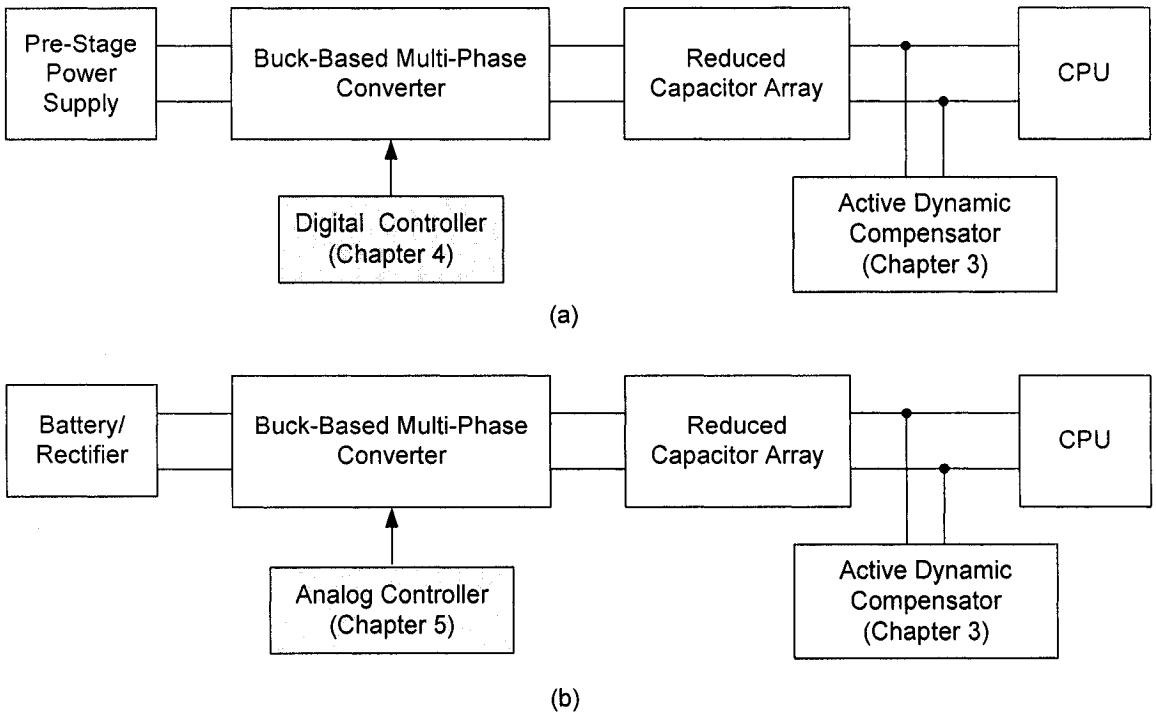


Figure 6-1: Advanced solutions for powering microprocessors

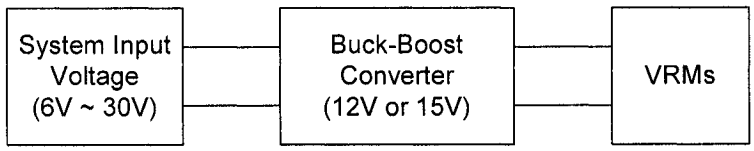


Figure 6-2: Two stage solution

The digital controller introduced in Chapter 4 is based on voltage hysteretic control with simplified peak current control for current sharing. The key technique in this controller is the time-varying current observer design since the load resistance is random. Adaptive control method is used here to design a parameter estimator along with the time-varying current observer. Therefore, current senseless control is achieved for high efficiency and low cost purposes. Peak current control is achieved for current sharing using the instantaneous phase current values.

The active current compensator introduced in Chapter 3 is a good candidate for powering high current slew rate loads. One can regard it as a discrete linear regulator. A discrete compensator does not work continuously. Actually, it only triggers at a pre-set current-slew rate value and operates at high frequency. The maximum complete compensation duration is only several microseconds. The best advantage of this compensator is the reduction of the decoupling system capacitors which were used for dynamic reasons only. It cuts overall costs while improving the VCC power supply performance.

APPENDIX A

COMPLETE DIGITAL OBSERVER

The complete digital observer is given below.

Defining

$$X[K] = \left[\hat{i}_{L1}(K) \;\; \hat{i}_{L2}(K) \;\; \hat{i}_{L3}(K) \;\; \hat{i}_{L4}(K) \;\; \hat{v}_c(K) \;\; \hat{R}_o(K)\right]^T$$
$$U(K) = \left[v_1(K) \;\; v_2(K) \;\; v_3(K) \;\; v_4(K) \;\; v_o(K)\right]^T$$

The state equations are

$$X(K+1) = A_D X(K) + B_D U(K)$$
$$\hat{I}_o(K) = \frac{v_o(K)}{\hat{R}_o(K)}$$

where

$$\overline{v}_c = v_o(K)$$
$$\overline{R}_o = \frac{y(K)}{\frac{v_1(K)-v_o(K)}{R_{L1}} + \frac{v_2(K)-v_o(K)}{R_{L2}} + \frac{v_3(K)-v_o(K)}{R_{L3}} + \frac{v_4(K)-v_o(K)}{R_{L4}}}$$

Here

$$A_D = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & a_{15} & a_{16} \\ a_{21} & a_{22} & a_{23} & a_{24} & a_{25} & a_{26} \\ a_{31} & a_{32} & a_{33} & a_{34} & a_{35} & a_{36} \\ a_{41} & a_{42} & a_{43} & a_{44} & a_{45} & a_{46} \\ a_{51} & a_{52} & a_{53} & a_{54} & a_{55} & a_{56} \\ a_{61} & a_{62} & a_{63} & a_{64} & a_{65} & a_{66} \end{bmatrix}$$

$$B_D = \begin{bmatrix} b_{11} & b_{12} & b_{13} & b_{14} & b_{15} \\ b_{21} & b_{22} & b_{23} & b_{24} & b_{25} \\ b_{31} & b_{32} & b_{33} & b_{34} & b_{35} \\ b_{41} & b_{42} & b_{43} & b_{44} & b_{45} \\ b_{51} & b_{52} & b_{53} & b_{54} & b_{55} \\ b_{61} & b_{62} & b_{63} & b_{64} & b_{65} \end{bmatrix}$$

and

$$a11 = 1 - \frac{R_{L1}}{L_1}T_s + \frac{1}{2}(\frac{R_{L1}}{L_1})^2 T_s^2$$

$$a12 = a13 = a14 = -\frac{1}{2}(\frac{1}{L_1 C} + \frac{K_1}{C})T_s^2$$

$$a15 = -(\frac{1}{L_1} + K_1)T_s + \frac{1}{2}(\frac{1}{L_1} + K_1)(\frac{R_{L1}}{L_1} + \frac{1}{\bar{R}_o C} + K_5)T_s^2$$

$$a16 = -\frac{1}{2}\frac{\bar{v}_c}{\bar{R}_o^2 C}(\frac{1}{L_1} + K_1)T_s^2$$

$$a21 = a23 = a24 = -\frac{1}{2C}(\frac{1}{L_2} + K_2)T_s^2$$

$$a22 = 1 - \frac{R_{L2}}{L_2}T_s + \frac{1}{2}(\frac{R_{L2}}{L_2})^2 T_s^2$$

$$a25 = -(\frac{1}{L_2} + K_2)T_s + \frac{1}{2}(\frac{1}{L_2} + K_2)(\frac{R_{L2}}{L_2} + \frac{1}{\bar{R}_o C} + K_5)T_s^2$$

$$a26 = -\frac{1}{2}\frac{\bar{v}_c}{\bar{R}_o^2 C}(\frac{1}{L_2} + K_2)T_s^2$$

$$a31 = a32 = a34 = -\frac{1}{2C}(\frac{1}{L_3} + K_3)T_s^2$$

$$a33 = 1 - \frac{R_{L3}}{L_3}T_s + \frac{1}{2}(\frac{R_{L3}}{L_3})^2 T_s^2$$

$$a35 = -(\frac{1}{L_3} + K_3)T_s + \frac{1}{2}(\frac{1}{L_3} + K_3)(\frac{R_{L3}}{L_3} + \frac{1}{\bar{R}_o C} + K_5)T_s^2$$

$$a36 = -\frac{1}{2}\frac{\bar{v}_c}{\bar{R}_o^2 C}(\frac{1}{L_3} + K_3)T_s^2$$

$$a41 = a42 = a43 = -\frac{1}{2C}(\frac{1}{L_4} + K_4)T_s^2$$

$$a44 = 1 - \frac{R_{L4}}{L_4}T_s + \frac{1}{2}(\frac{R_{L4}}{L_4})^2 T_s^2$$

$$a45 = -(\frac{1}{L_4} + K_4)T_s + \frac{1}{2}(\frac{1}{L_4} + K_4)(\frac{R_{L4}}{L_4} + \frac{1}{\bar{R}_o C} + K_5)T_s^2$$

$$a46 = -\frac{1}{2}\frac{\bar{v}_c}{\bar{R}_o^2 C}(\frac{1}{L_4} + K_4)T_s^2$$

$$a51 = \frac{T_s}{C} - \frac{1}{2}(\frac{R_{L1}}{L_1 C} + \frac{1}{\bar{R}_o C^2} + \frac{K_5}{C})T_s^2$$

$$a52 = \frac{T_s}{C} - \frac{1}{2}(\frac{R_{L2}}{L_2 C} + \frac{1}{\bar{R}_o C^2} + \frac{K_5}{C})T_s^2$$

$$a53 = \frac{T_s}{C} - \frac{1}{2}(\frac{R_{L3}}{L_3 C} + \frac{1}{\bar{R}_o C^2} + \frac{K_5}{C})T_s^2$$

$$a54 = \frac{T_s}{C} - \frac{1}{2}(\frac{R_{L4}}{L_4 C} + \frac{1}{\bar{R}_o C^2} + \frac{K_5}{C})T_s^2$$

$$a55 = 1 - (\frac{1}{\bar{R}_o C} + K_5)T_s - [\frac{1}{C}(\frac{1}{L_1} + K_1) + \frac{1}{C}(\frac{1}{L_2} + K_2) + \frac{1}{C}(\frac{1}{L_3} + K_3) + \frac{1}{C}(\frac{1}{L_4} + K_4) - (\frac{1}{\bar{R}_o C} + K_5)^2 + K_p(\frac{\bar{v}_c}{\bar{R}_o^2 C})]T_s^2$$

$$a56 = -\frac{1}{2}\frac{\bar{v}_c}{\bar{R}_o^2 C}(\frac{1}{\bar{R}_o C} + K_5)T_s^2$$

$$a61 = a62 = a63 = a64 = -\frac{K_p}{2C}T_s^2$$

$$a65 = -K_p T_s + \frac{1}{2}K_p(\frac{1}{\bar{R}_o C} + K_5)T_s^2$$

$$a66 = 1 - \frac{1}{2}K_p(\frac{\bar{v}_c}{\bar{R}_o^2 C})T_s^2$$

$$b11 = \frac{T_s}{L_1} - \frac{R_{L1}T_s^{\,2}}{2L_1^{\,2}}$$

$$b12 = b13 = b14 = b21 = b23 = b24 = b31 = b32 = b34 = b41 = b42 = b43 = b61 = b62 = b63 = b64 = 0$$

$$b15 = K_1(T_s - \frac{R_{L1}T_s^{\,2}}{2L_1}) - \frac{K_5T_s^{\,2}}{2}(L_1 + K_1)$$

$$b22 = \frac{T_s}{L_2} - \frac{R_{L2}T_s^{\,2}}{2L_2^{\,2}}$$

$$b25 = K_2(T_s - \frac{R_{L2}T_s^{\,2}}{2L_2}) - \frac{K_5T_s^{\,2}}{2}(L_2 + K_2)$$

$$b33 = \frac{T_s}{L_3} - \frac{R_{L3}T_s^{\,2}}{2L_3^{\,2}}$$

$$b35 = K_3(T_s - \frac{R_{L3}T_s^{\,2}}{2L_3}) - \frac{K_5T_s^{\,2}}{2}(L_3 + K_3)$$

$$b44 = \frac{T_s}{L_4} - \frac{R_{L4}T_s^{\,2}}{2L_4^{\,2}}$$

$$b45 = K_4(T_s - \frac{R_{L4}T_s^{\,2}}{2L_4}) - \frac{K_5T_s^{\,2}}{2}(L_4 + K_4)$$

$$b51 = \frac{T_s^{\,2}}{2L_1C}$$

$$b52 = \frac{T_s^{\,2}}{2L_2C}$$

$$b53 = \frac{T_s^{\,2}}{2L_3C}$$

$$b54 = \frac{T_s^{\,2}}{2L_4C}$$

$$b55 = K_1\frac{T_s^{\,2}}{2C} + K_2\frac{T_s^{\,2}}{2C} + K_3\frac{T_s^{\,2}}{2C} + K_4\frac{T_s^{\,2}}{2C} + K_5[T_s - \frac{T_s^{\,2}}{2}(\frac{1}{\overline{R_o}C} + K_5)] + K_p\frac{T_s^{\,2}\overline{V_c}}{2\overline{R_o}^{\,2}C}$$

$$b65 = K_pT_s - \frac{K_5K_pT_s^{\,2}}{2}$$

APPENDIX B

MATLAB PROGRAM FOR THE OBSERVER

The MATLAB program is given below for the observer. The line starting with "%" is a description line for explaining the functions of the following commands.

```
% Define function of cobserv and parameters

function [sys,x0,str,ts]=cobserv(t,x,u,flag)


global eq1;

global eq2;

global eq3;

global R;


% Enter RLC component values

Rl1=?;

Rl2=?;

L1=?;

L2=?;

C=?;


% Feedback constants
```

```
K1=?;  % Decide Vo response

K2=?;

K3=?;  % Decrease k3 to shorten DC gain

Kp=?;  % Increase kp to shorten transient, decrease it to decrease spike


if (t>0)

  eq1=u(1);

  eq2=u(2);

  eq3=u(3);


  % Calculate equilibrium point

  R=eq3/((eq1-eq3)/Rl1+(eq2-eq3)/Rl2);


else

  eq1=0;

  eq2=0;

  eq3=0;

  R=0.2;

end
```

```
% Enter matrix A,B,C & D from equations given in Appendix


A=[a11 a12 a13 a14 ;
   a21 a22 a23 a24;
   a31 a32 a33 a34;
   a41 a42 a43 a44];


B=[b11 b12 b13;
  b21 b22 b23;
  b31 b32 b33;
  b41 b42 b43];


C=[1 1 0 0];


D=[0 0 0];


switch flag,
case 0
```

```
    [sys,x0,str,ts]=mdlInitializeSizes(A,B,C,D); %Initialization


  case 1

    sys=mdlDerivatives(t,x,u,A,B,C,D); %Calculate derivatives

  case 3

    sys=mdloutputs(t,x,u,A,B,C,D); %Calculate output


  case{2,4,9} %Unused flages

    sys=[];


  otherwise

    error(['Unhandled flag=',num2str(flag)]); %Error handling


  end



% System size and initial conditions

function [sys,x0,str,ts]=mdlInitializeSizes(A,B,C,D)
```

```
sizes=simsizes;

sizes.NumContStates=4;

sizes.NumDiscStates=0;

sizes.NumOutputs=1;

sizes.NumInputs=3;

sizes.DirFeedthrough=0; %Matrix D is empty

sizes.NumSampleTimes=1;

sys=simsizes(sizes);


x0=zeros(4,1); %Initial condition


str=[ ]; %str is empty


ts=[0 0]; %Both the sample time and the offset time are 0


% Return the derivatives for continuous states

function sys=mdlDerivatives(t,x,u,A,B,C,D)

sys=A*x+B*u;
```

```
% Return the block output

function sys=mdloutputs(t,x,u,A,B,C,D)

sys=C*x+D*u;
```