INVESTIGATION OF DUAL-STAGE HIGH EFFICIENCY &DENSITY MICRO INVERTER FOR SOLAR APPLICATION

by

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ABSTRACT

Module integrated converters (MIC), also called micro inverter, in single phase have witnessed recent market success due to unique features (1) improved energy harvest, (2) improved system efficiency, (3) lower installation costs, (4) plug-N-play operation, (5) and enhanced flexibility and modularity. The MIC sector has grown from a niche market to mainstream, especially in the United States. Due to the fact that two-stage architecture is commonly used for single phase MIC application. A DC-DC stage with maximum power point tracking to boost the output voltage of the Photovoltaic (PV) panel is employed in the first stage, DC-AC stage is used for use to connect the grid or the residential application. As well known, the cost of MIC is key issue compared to convention PV system, such as the architecture: string inverter or central inverter. A high efficiency and density DC-DC converter is proposed and dedicated for MIC application.

Assuming further expansion of the MIC market, this dissertation presents the micro-inverter concept incorporated in large size PV installations such as MW-class solar farms where a three phase AC connection is employed. A high efficiency three phase MIC with two-stage ZVS operation for grid tied photovoltaic system is proposed which will reduce cost per watt, improve reliability, and increase scalability of MW-class solar farms through the development of new solar farm system architectures. This dissertation presents modeling and triple-loop control for a high efficiency three-phase four-wire inverter for use in grid-connected two-stage micro inverter applications. An average signal model based on a synchronous rotation frame for a three-phase four-wire inverter has been developed. The inner current loop consists of a variable frequency bidirectional current mode (VFBCM) controller which regulates output filter inductor current thereby achieving ZVS, improved system response, and reduced grid current THD. Active

damping of the LCL output filter using filter inductor current feedback is discussed along with small signal modeling of the proposed control method.

Since the DC-link capacitor plays a critical role in two-stage micro inverter applications, a DC-link controller is implemented outside of the two current control loops to keep the bus voltage constant. In the end, simulation and experimental results from a 400 watt prototype are presented to verify the validity of the theoretical analysis.

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CHAPTER ONE: INTRODUCTION

1.1 Background and Challenges

With ever dwindling natural resources and increasing demands for power, the need to seek out viable alternative sources of renewable energy is not just acute but urgent. Due to the fact that solar energy offers extraordinary merits including environmentally neutral, unlimited availability and low cost capable of competing with conventional sources with technology advances and mass production in the coming few years. The photovoltaic (PV) industry has seen over 25% growth on an average over the last 10 years [1].

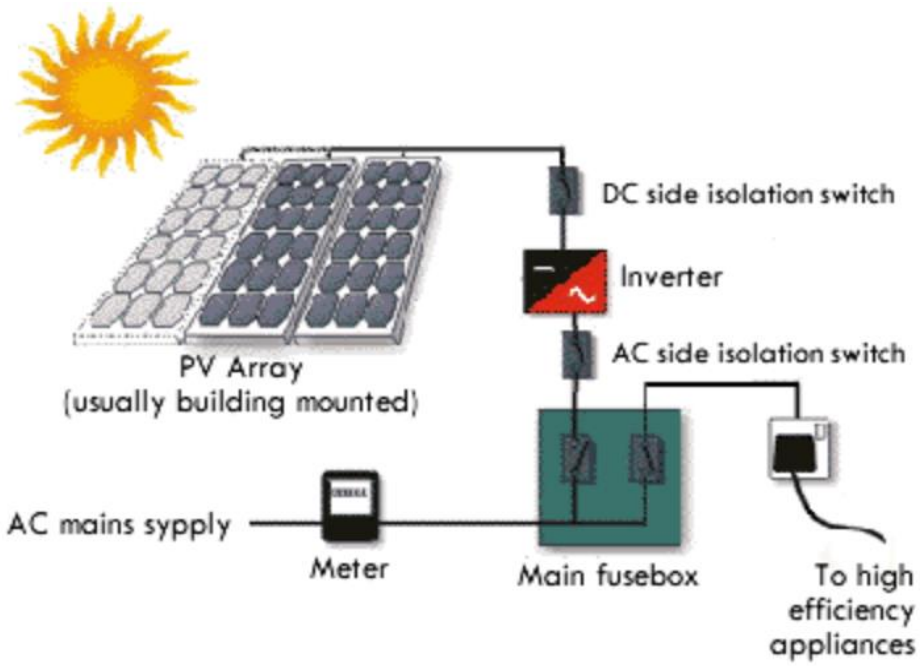


Figure 1.1 A typical PV system configuration for appliances [1]

Figure 1.1 shows a typical grid-connected PV system configuration for appliances application. The PV array is consisted with a couple of individual PV modules connected together to generate the required power with a suitable alternating current and voltage through a DC/AC converter.

Other than the PV panel itself, the inverter is the most critical device in a PV system both for off-grid or grid-connection applications. Currently, PV system architectures can be categorized into three basic classes with respect to the types of grid-tied inverter: Central inverter, String or Multi-string inverter, and Module Integrated Converter (MIC), also called Micro-inverter [2] [3] [4]. Although the Central inverter as shown in Figure 1.2 can operate at high efficiency with only one DC/AC power conversion stage, this structure has some disadvantages: (1) Each PV module may not operate at its maximum power point which results in less energy harvested. (2) Additional losses are introduced by string diodes and junction box; (3) Single point of failure and mismatch of each string or PV panel affects the PV array efficiency greatly.

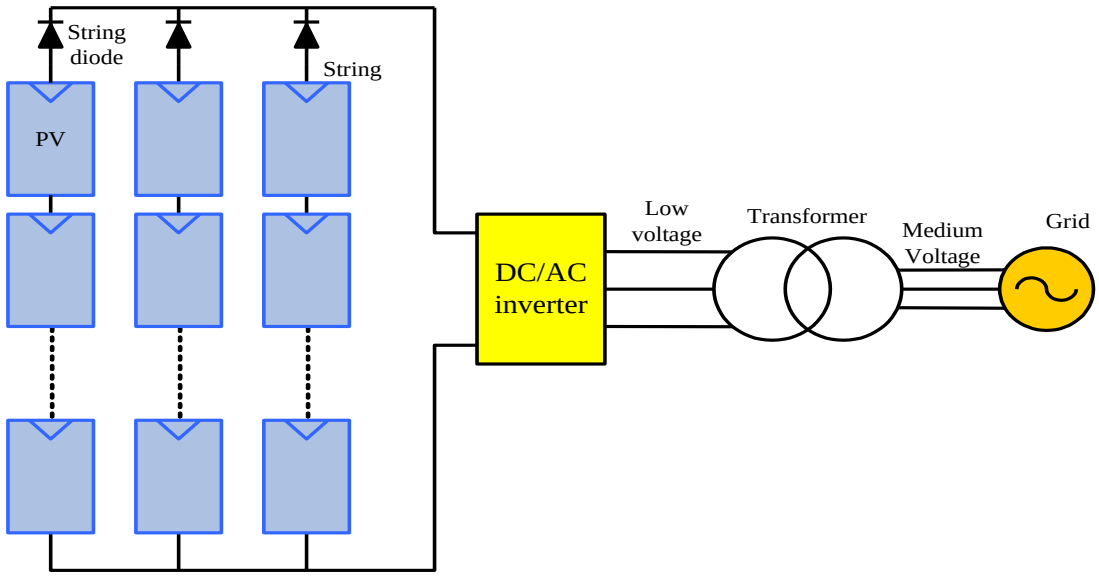


Figure 1.2 Diagram of central inverter architecture

Figure 1.3 shows a diagram of the String inverter that is a modified version of the Central inverter. It partially overcomes the issues arising in Central inverters however it still suffers some of the disadvantages of the central inverter. In an effort to maximize the power from each PV panel, a new approach was recently proposed which can be applied to either Central or String inverter architectures. A power maximizer (usually in the form of a DC/DC converter) is shown in figure 1.4, which is attached to each PV panel to implement maximum power tracking. Although the architecture maximizes power from each PV panel at the cost of additional DC/DC module, it still suffers from drawbacks such as high voltage hazard, single point failure, and difficulty in maintenance.

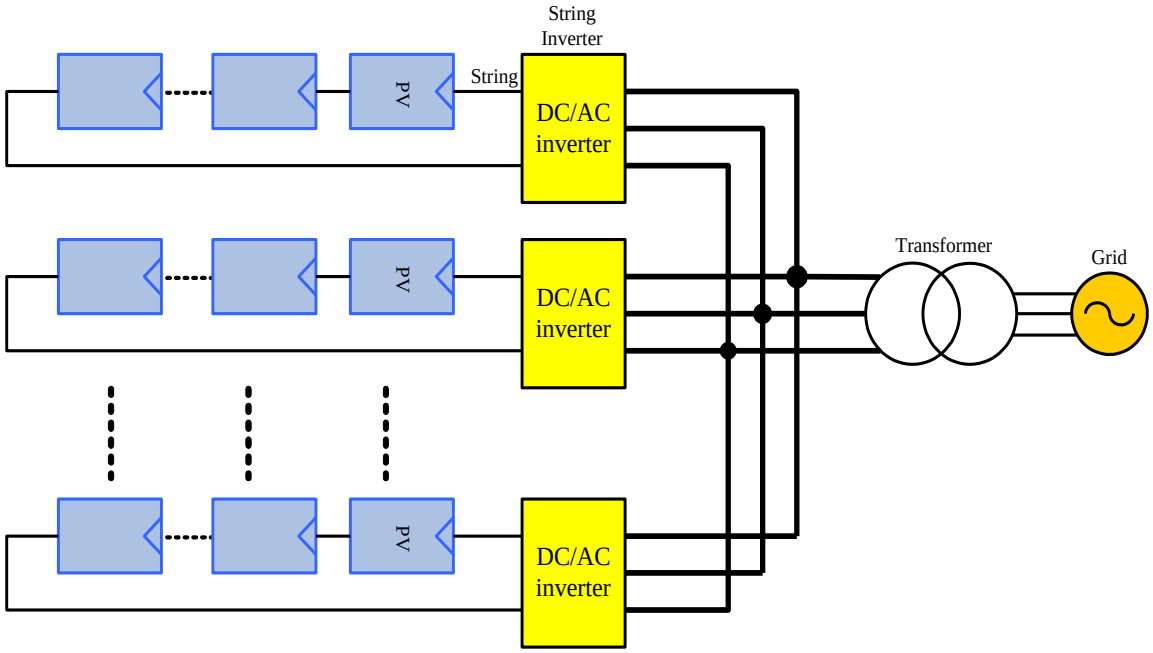


Figure 1.3 Diagram of string inverter based architecture

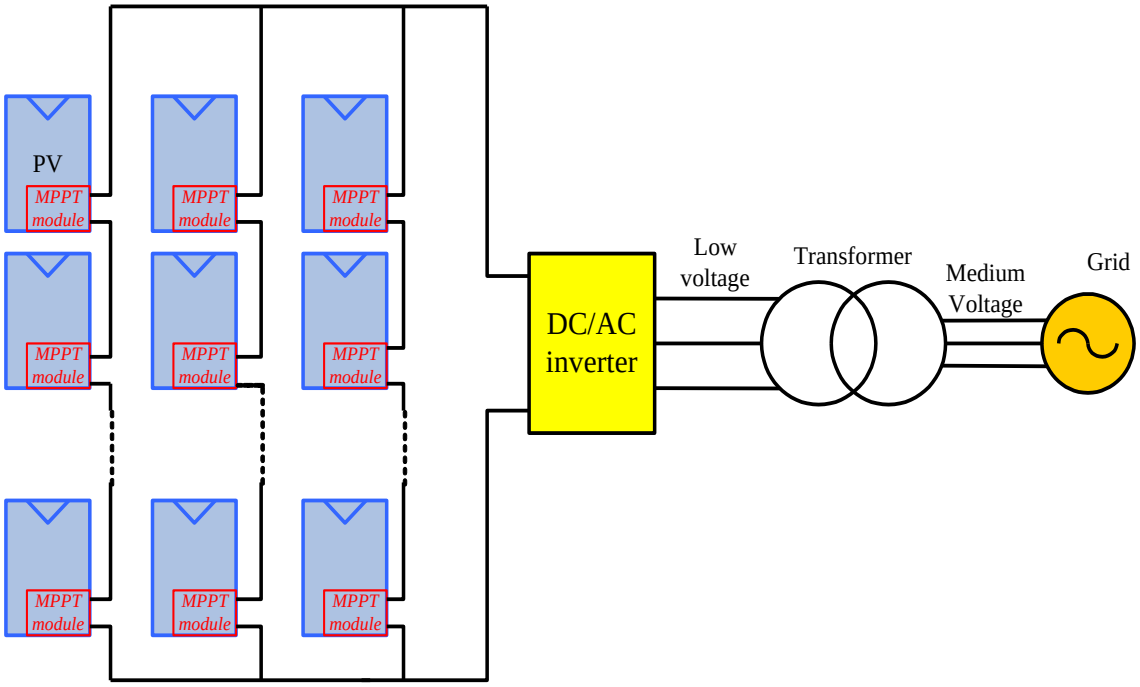


Figure 1.4 Maximum power tracking for each panel

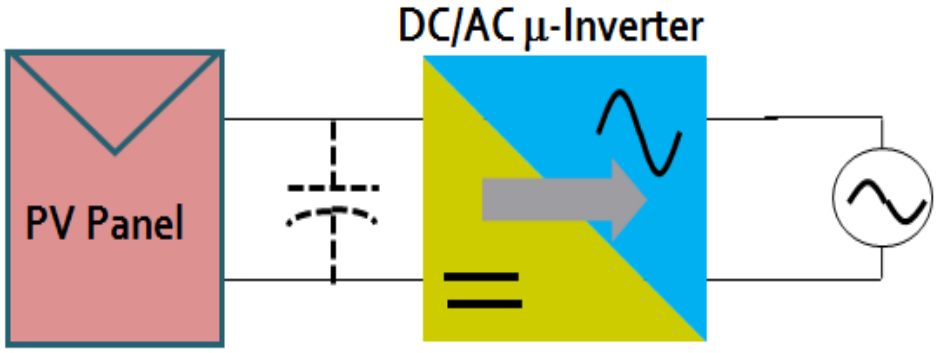


Figure 1.5 Configuration of micro-inverter for solar application

Module integrated converters (MIC) in single phase as shown in figure 1.5 have witnessed recent market success due to unique features (1) improved energy harvest, (2) improved system efficiency, (3) lower installation costs, (4) plug-N-play operation, (5) and enhanced flexibility and modularity. The MIC sector has grown from a niche market to mainstream, especially in the United States.

Assuming further expansion of the MIC market, this dissertation presents the micro-inverter concept incorporated in large size PV installations such as MW-class solar farms where a three phase AC connection is employed. A high efficiency three phase MIC with two-stage ZVS operation for grid tied photovoltaic system is proposed which will reduce cost per watt, improve reliability, and increase scalability of MW-class solar farms through the development of new solar farm system architectures.

The MIC typically used in distributed PV systems is a small grid-tie inverter of 150-400W that converts the output of a single PV panel to AC. The MIC AC outputs are connected in parallel and routed to a common AC coupling point. No series or parallel DC connections are made leaving all DC wiring at a relatively low voltage level of a single panel (typically <60Vdc). The MIC can be further integrated into PV modules to realize a true Plug-and-Play solar AC PV generation system. Thus, AC PV modules with integrated MIC, have significant advantages over traditional PV systems since they allow Maximum Peak Power Tracking (MPPT) on each solar panel to maximize energy harvesting, and offer distributed and redundant system architecture. In addition, MIC and AC PV systems greatly simplify system design, eliminate safety hazards, and reduce installation costs [3][5][6]. With these advantages, the AC module has become the trend for future PV system development. Although MIC and AC PV modules have witnessed recent market success, MIC still has many technical challenges remaining such as high efficiency, high reliability at module level, low cost and high level control issues. To date, research of the MIC has mainly focused on isolated topologies for the following two reasons: (1) from reported literature, most topologies with a few exceptions cannot meet the dual grounding requirement without transformer isolation according to the UL1741 standard. (2) Using transformer is the

best way to boost the low input voltage to high output voltage for AC grid with high efficiency. Since line transformers are bulky and costly, this architecture is not practical for MIC. This paper mainly focuses on the architecture employing a high frequency transformer.

The MIC with its high frequency transformer can be grouped into three architectures based on the DC-link configurations: DC-link, pseudo DC-link and high frequency AC [3] [4] [5]. Usually the MIC just pumps the power from PV to AC grid with unidirectional power flow. However, with the presence of the power decoupling capacitor, MIC can support the AC grid not only as an AC power source, but as a VAR and possibly a harmonics compensator as well [5]. For the latter two cases, bidirectional power flow is needed between AC grid and the power decoupling capacitor requiring MIC with bidirectional power flow capability.

For applications with power levels under several kilo-watts, the single phase connection is commonly used. However, the single phase connection has the disadvantage that the power flow to the grid is time varying, while the power of the PV panel must be constant for maximizing energy harvest, which results in instantaneous input power mismatch with the output instantaneous AC power to the grid. Therefore, energy storage elements must be placed between the input and output to balance (decouple the unbalance) the different instantaneous input and output power. Usually, a capacitor is used to serve as a power decoupling element [2]. However, the lifetime of different types of capacitors varies greatly, e.g. Electrolytic capacitors typically have a limited lifetime of 1000~12,000 hours at 105^0C operating temperature [7]. Although some researchers have developed various methods of reducing the required capacitance in single phase MICs in order to allow use of longer lifespan film capacitors [9][11]-[15], these approaches have the drawbacks of either complicating the inverter topology and control or reducing the overall

efficiency. Most presently available commercial MICs still use electrolytic capacitors as power decoupling storage elements due to their large capacitance, low cost, and volumetric efficiency. This tends to limit the lifespan of these MICs [7] [8].

The Distributed PV system, whether used in large-scale solar farms, tens of kilowatt installations, or even down to a single PV panel, will be a trend for future solar PV deployment due to its remarkable merits: (a) Easy modularization and scalability; (b) Elimination of single point failure; (c) Simple installation and maintenance; (d) High efficiency and low cost. FPEC (Florida Power Electronics Center) which is a research arm of UCF has first developed system architecture for a PV solar farm based on three-phase MICs with film capacitor shown in figure 1.6. A three-phase MIC (Micro-inverter) is attached or integrated directly into each PV panel. The outputs of each MIC are directly connected to low voltage three-phase grid and then through medium voltage transformer boost the low three phase voltage to high voltage at power transmission line side. Each MIC operates independently regardless of the failure of other MICs. This architecture will reduce the cost per watt, improve system reliability, and provide more cost effective and efficient power distribution. FPEC also commissioned market research that confirmed the viability of this PV system architecture.

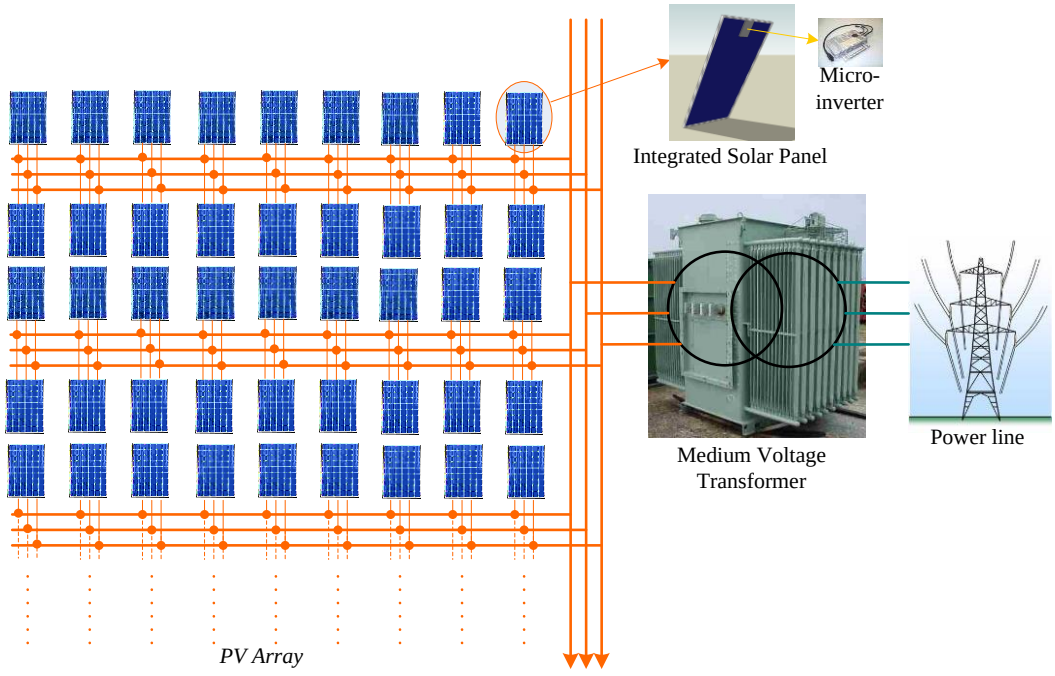


Figure 1.6 Three-phase micro-inverter based architecture for solar farm

Reference [10] shows that the most common commercial building electric service in North America is 120/208 volt wye (three-phase four-wire) which is used to power 120 volt plug loads, lighting, and smaller HVAC systems. In larger facilities the voltage is 277/480 volt and used to power single phase 277 volt lighting and larger HVAC loads. A large number of PV panels with MICs can be located on the roof of a commercial building or adjacent structure and the three phase AC outputs combined to supplement the building electrical service.

1.2 Objectives and Outline

The objective of this paper is to provide research background and motivation for use of a three phase topology in larger residential and small to medium solar farm applications. Since the MIC

is a critical component of any such system, this dissertation will present the design and implementation of a two stage high efficiency three phase MIC which uses no electrolytic capacitors. A two-stage micro inverter design suitable for high efficiency DC/AC conversion from a low-voltage (25-50V) DC input to a three-phase 308V AC grid-tied PV system will be discussed in this dissertation. The organization of this dissertation is classified as follows: The first chapter gives the background introduction of the PV system architecture for solar energy generation.

In Chapter 2, a high efficiency DC-DC stage configuration to interface with PV panel is proposed to boost high voltage from low voltage DC input. The specific design of the MPPT controller will not be discussed here due to focusing on the design of topology. Operating modes of the proposed ZVS three-phase four-wire DC/AC converter along with an average modeling is illustrated in Chapter 3. A control strategy for overall system based on trip-loop design will be presented in Chapter 4. As a relatively large area close to half the full prototype is occupied by passive components, such as dc link capacitor, output filter to connect grid while we take a view from the prototype, Chapter 5 will provide a design procedure to minimize the passive components size along with the value calculation based on the prototype's specification. Experimental results are verified using a 400 watt prototype that is shown in Chapter 6. The conclusion is given at the end.

CHAPTER TWO: DC-DC STAGE CONVERTER

2.1 Background and Motivation

Single panel PV array output voltages are relatively low and vary over a wide range under different operating conditions. A high step up dc-dc converter is typically required to boost this voltage to a value high enough for use in two stage grid-connected power applications [18] [22] which is shown in figure 2.1.

Many non-isolated topologies have been devised to obtain high step-up voltage gain in the past decade [19]-[25]. However, non-isolated converters are not discussed in this paper because most of them cannot meet the dual grounding requirement, thereby possibly losing the grid-connected opportunities [26]. In order to provide galvanic isolation, various isolated converters for high step up applications have been proposed [27]-[42]. In general, the topologies with galvanic isolation suitable for this application can be categorized into two groups: single switch topologies and multi-switch topologies. Single switch topologies mainly include fly-back and forward converters. Multiple-switch topologies include half bridge and full bridge.

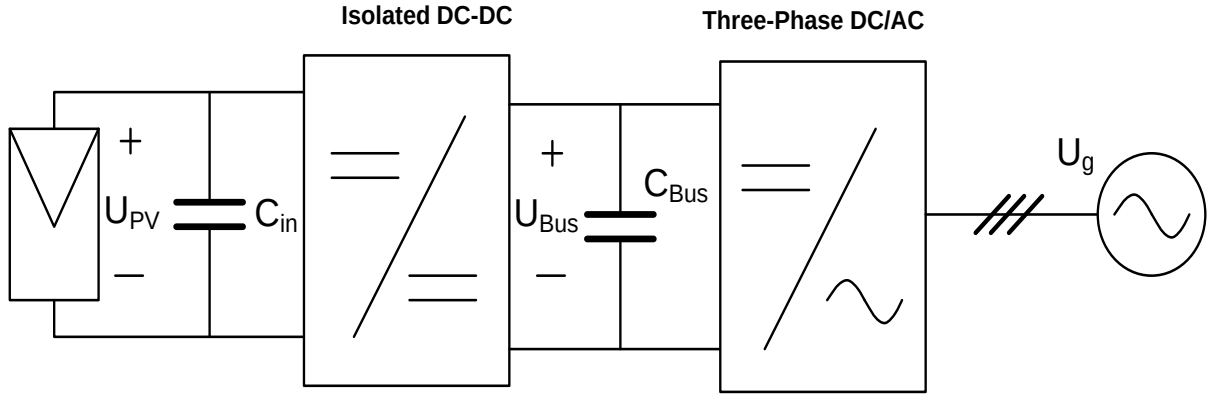


Figure 2.1 Simplified block diagram of two-stage MIC

Recently, LLC resonant topology has become attractive due to its desirable characteristics such as high efficiency and natural ZVS/ZCS commutation. This topology is widely utilized in front end DC/DC converters, PC power supplies, flat panel TV's, telecom, and many other commercial, military, and industrial applications. [27-29], [69]. Unfortunately, conventional LLC resonant topology is rarely chosen as the first stage of a PV step-up DC-DC converter due to its difficultly in maintaining high efficiency over a wide input range with varying load conditions. Hybrid operation of a LLC half bridge resonant converter by paralleling an auxiliary transformer with the resonant inductor was proposed by Liang [30]. In addition, a modified LLC converter with two transformers in series was also introduced to increase voltage gain [31]. Although these methods are effective in retaining the merits of LLC resonant topology while extending the input voltage range, the transition between operating modes is a function of input voltage and output power and is not smooth. In addition, control complexity increases which may negatively impact cost and reliability.

Since the power rating of a single PV panel is approximately 200 Watts, single switch flyback and forward topologies are good candidates for step-up DC-DC converter applications due to their simplicity, low cost, and good efficiency over a wide operating voltage range [32-36]. Note that the isolated flyback converter requires only one magnetic component since the transformer's magnetizing inductance serves as the energy storage element and this stored energy is transferred to the load during the transistor's off period [37]. Since energy is stored in the core air gap during the on time, The more the energy stored, the larger the air gap requirement. Thus, a flyback converter is not the best choice at higher power levels according to the general formula-core selection for different topologies [36, 43]. In addition, the value of output capacitor is

relatively high due to discontinuous output current resulting in a physically larger DC link capacitor in two-stage micro inverter applications. It is also difficult to handle the high peak current in the primary that is present with a typical PV panel voltage of less than 30V. Overall, the size of the flyback converter is a major concern especially when the power rating exceeds 100 Watts. Alternately, the energy in a forward converter is transferred to the load during the transistor's on time enabling more power to be delivered to the load for the same core size. Output voltage ripple is much smaller than that of a flyback due to the output filter inductor. However, the forward converter does need additional circuits or an auxiliary winding to reset the magnetizing current of the transformer.

The Forward-Flyback topology that merges the merits of each has been studied by many researchers over the past several decades [37-42]. A circuit that combines direct energy transfer with a wide operating range would have advantages over a forward or flyback converter by itself [37]. This topology (usually running in continuous current mode) is widely used for high input voltage and low output voltage application. In order to achieve zero voltage switching (ZVS) of the primary switch, an auxiliary switch such as an active clamp circuit is necessary but it has the aforementioned problems [41]. Recently, a Series-Connected Forward-Flyback converter that achieves high step-up conversion gain was published in [42], however the voltage balance on the output capacitors should be considered due to the series structure. Publications released over the last decade indicate that Forward-Flyback efficiency is still a major impediment to its widespread application.

In this chapter, a BMFFC with an efficient active LC snubber circuit is proposed as shown in Figure 2.2. This simple ZVS control scheme is utilized without increasing hardware cost. The

switching loss is greatly reduced since there is no reverse recovery current in the output rectifier diodes. In addition, a low voltage MOSFET can be used by selecting the proper transformer turns ratio. Due to rapid advances in the semiconductor industry, low voltage MOSFET on resistance has been significantly reduced. For example, the on resistance of a 150V MOSFET is less than 10 milliohms for D^2PAK package. With this in mind there is little difference in conduction losses between Continuous Current Mode (CCM) and Boundary Current Mode (BCM) operation. Energy stored in the transformer leakage inductance causes high voltage spikes in the MOSFET due to BCM, requiring a higher voltage (higher RDSon) MOSFET thereby reducing system efficiency. In order to suppress this voltage spike, an efficient active LC snubber circuit is employed. Although it has several discrete components, these can be low cost surface mount parts due to the small root mean square (RMS) current through the LC snubber circuit and low voltage stress. The gate signal of S_{sb} is the same as S_1; a pulse transformer is inserted between S_1 driver and S_{sb}. According to the parameters of a 200W experimental prototype in Table I, the total cost of the LC snubber circuit is $0.78 based on 10k PCS. Thus, there is very little impact on the system cost.

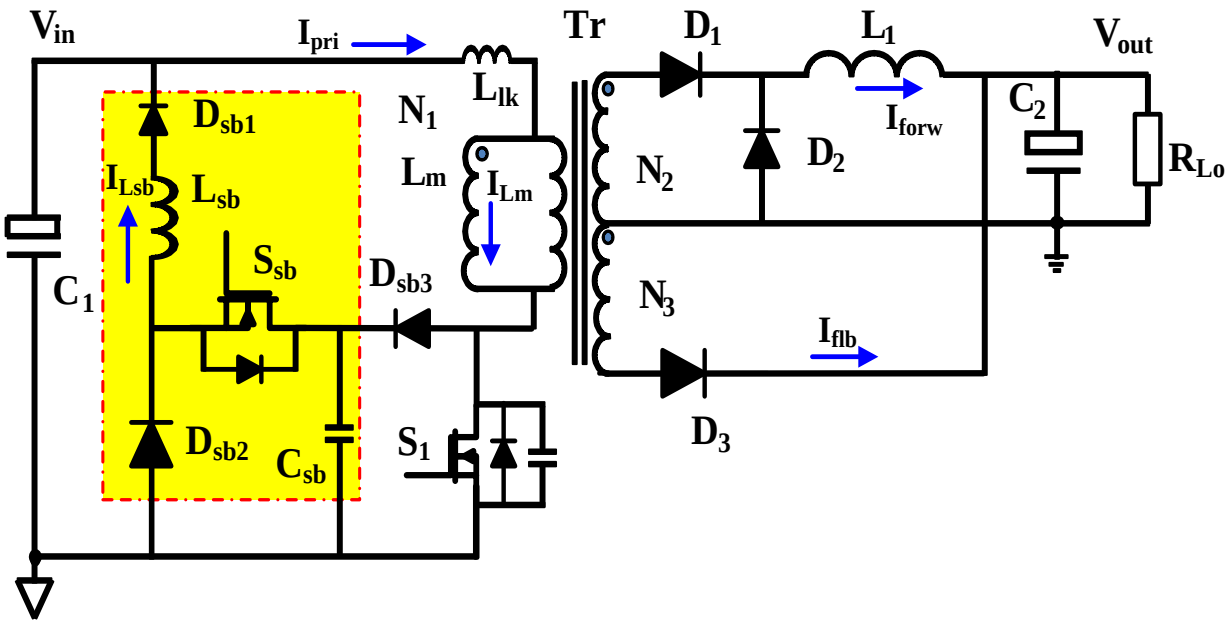


Figure 2.2 BMFFC with efficient active LC snubber circuit

2.2 Principle of Operation

In order to simplify analysis of the operating principle, the following assumptions are made over one switching period:

1) Capacitors C_1, C_2 are large enough thus V_{in} and V_{out} are regarded as a constant voltage source.
2) All passive components are considered to be ideal which implies the ESRs of inductors and capacitors are neglected.
3) Active switches and all diodes are regarded as ideal that are linearly on or off and the converter is operating in steady state.
4) Parasitic inductors, capacitors, and resistors of circuit traces are neglected.

The equivalent circuits of the BMFFC in different operating intervals are introduced in Figure 2.3. Figure 2.4 shows the theoretical waveforms of the BMFFC with an active LC snubber circuit. The operation of the converter within one switching cycle can be divided into nine intervals.

Prior to t_0, the main switch S_1 and the auxiliary switch S_{sb}, are both off. At t_o, S_1 and S_{sb} are simultaneously turned on. One portion of the energy from the input source is stored in the transformer, similar to a conventional flyback converter. Meanwhile, another portion of the energy is directly transferred to the load through the transformer and the output inductor L_1, similar to conventional forward converter operation.

Since the voltage across C_{sb} is deliberately designed to be at least as high as twice the input voltage, C_{sb} resonates with L_{sb} to discharge the energy stored in the snubber capacitor C_{sb} back to the input source. The voltage across the snubber capacitor $V_{C_{sb}}$, and the current through snubber inductor $I_{L_{sb}}$, can be represented respectively by:

$$V_{C_{sb}}(t) = V_{in} + V_{out}\frac{N_1}{N_3}\cos(\omega_0 t - \omega_0 t_0) \tag{2.1}$$

$$i_{L_{sb}}(t) = -\frac{V_{out}}{z_0}\frac{N_1}{N_3}\sin(\omega_0 t - \omega_0 t_0) \tag{2.2}$$

Where:

$\omega_0 = \frac{1}{\sqrt{L_{sb} * C_{sb}}}$: the resonant angular frequency

$z_0 = \sqrt{\frac{L_{sb}}{C_{sb}}}$: the characteristic impedance of the snubber circuit resonant tank

N_1 = number of turns in the transformer primary

N_3 = number of turns in the secondary flyback section

While the voltage across C_{sb} equals to Vin, the current $I_{L_{sb}}$ reaches the maximum value $\frac{V_{out}}{z_0}\frac{N_1}{N_3}$ at t'_1. After t'_1, the current I_{Lsb} is gradually decreasing due to the polarity change of the voltage across L_{sb}. This interval ends once the voltage across C_{sb} drops to zero. The duration of the resonance is given by (2.3).

$$\Delta t_1 = t_1 - t_0 = \cos^{-1}\left(-\frac{V_{in}}{V_{out}}\frac{N_3}{N_1}\right)\sqrt{L_{sb} * C_{sb}} \tag{2.3}$$

From (2.3), the length of this interval depends on input voltage after output voltage, turns ratio of transformer, and resonant parameters are determined. The maximum duration of Δt_1 is at $\pi\sqrt{L_{sb} * C_{sb}}$ while $\frac{V_{in}}{V_{out}}\frac{N_3}{N_1}$ equals one. Combining (2.2) and (2.3), we can see the current I_{Lsb} doesn't drop to zero if $\frac{V_{in}}{V_{out}}\frac{N_3}{N_1}$ is less than 1 at $t_1$with input voltage decrease. Because V_{csb} is already equal to zero at t_2, D_{sb2} is turned on if L_{sb} still has current. As a result, I_{Lsb} continues to decrease linearly due to input voltage across L_{sb}. The blocking diode D_{sb1} is turned off with ZCS when I_{Lsb} equals zero at t_2. The action of the non-dissipative LC snubber circuit is completed at t_2. S_1 continues to conduct during this interval.

The main switch S_1 is still on in this interval as it was in the previous two operating intervals. The magnetizing current I_{Lm} and the current through the output inductor I_{L1} continue to ramp up. The current I_{Lm}, I_{L1} and I_{pri} at t_3 can be calculated by:

$$i_{Lm}(t_3) = \frac{V_{in}}{L_m} \cdot (t_3 - t_0) + i_{Lm}(t_0) \tag{2.4}$$

$$i_{L1}(t_3) = \frac{V_{In} \cdot \frac{N_2}{N_1} - V_{out}}{L_1} \cdot (t_3 - t_0) + i_{L1}(t_0) \tag{2.5}$$

$$I_{pri}(t_3) = i_{Lm}(t_3) + i_{L1}(t_3) * \frac{N_2}{N_1} \tag{2.6}$$

Where:

L_m = the value of the primary magnetizing inductance

L_1= the value of the output inductor

N_2 = the winding turns in secondary side of forward section

$i_{Lm}(t_0), i_{L1}(t_0)$: the initial current of L_m and L_1 is zero at t_0

At t_3, S_1 and S_{sb} are simultaneously turned off. The parasitic output capacitor of the MOSFET C_{oss} in parallel with the snubber capacitor C_{sb} is immediately charged by the primary current I_{pri}. The voltage across S_1 and C_{sb} is increasing quickly due to high charging current I_{pri}. This period ends when the voltage across S_1 is equal to V_{in}.

When the voltage across S_1 is greater than input voltage V_{in} from t_4, the rectifier D_1 is blocked and D_2 is turned on since it is forward biased. Due to the output voltage across L_1, I_{L1} is freewheeling via D2. Consequently, the energy stored in L_1 is released to the load. At this time, the parallel combination of C_{oss} and C_{sb} is charged solely by the magnetizing current I_{Lm}. Since D_1 is off, the load current is not reflected in the primary side. The current through the MOSFET is far smaller than that through the snubber capacitor due to the fact that the value of C_{sb} is more than 10 times of C_{oss}. Thus, the turn off loss in the MOSFET is greatly reduced. This interval ends at t_5 when the voltage across the MOSFET is equal to input voltage V_{in} plus the output voltage divided by the turns ratio of N_3/N_1.

At t_5, the secondary side rectifier D_3 of the flyback section starts to conduct. The energy stored in the transformer is delivered to the load similar to a conventional flyback converter and the magnetizing current decreases linearly. Meanwhile, the current I_{L1} continues to decrease linearly. The total output current is summed up by the output current of the forward and flyback converter sections which can be represented by:

$$I_{D3}(t) = i_{Lm}(t_5)\frac{N_1}{N_3} - \frac{V_{out}}{L_{m*}\left(\frac{N_3}{N_1}\right)^2}(t - t_5) \quad (2.7)$$

$$I_{L1}(t) = i_{L1}(t_5) - \frac{V_{out}}{L_1}(t - t_5) \quad (2.8)$$

$$I_{out}(t) = I_{D3}(t) + I_{L1}(t) \quad (2.9)$$

This interval begins at t_6, when the current through D_3 decays to zero. In this case, D_3 is turned off under ZCS. As soon as D_3 is blocked, a primary side resonant circuit consisting of C_{oss} and L_m is formed and the voltage across S_1 decreases. The blocking diode D_{sb3} is reverse biased once the voltage across C_{oss} (V_{ds_S1}) is less than the voltage across C_{sb}, whose voltage will maintain unchanged until S_{sb} turns on at the next switching cycle. In the secondary, the energy stored in L_1 is being transferred to the output. During this time, the voltage across C_{oss}, and the current in the primary side can be represented respectively by:

$$V_{ds\_s_1}(t) = V_{in} + V_{out}\frac{N_1}{N_3}\cos\omega_c(t - t_6) \quad (2.10)$$

$$i_{pri}(t) = -\frac{V_{out}\frac{N_1}{N_3}}{z_c}\sin\omega_c(t - t_6) \quad (2.11)$$

Where:

$\omega_c = \frac{1}{\sqrt{L_{m*}C_{oss}}}$: the resonant angular frequency

$z_c = \sqrt{\frac{L_m}{C_{oss}}}$: the characteristic impedance of the resonant tank in the primary side

When the voltage across S_1 decreases to the input voltage V_{in}, it will be clamped to Vin due to the fact that the current through L_1 will be conducted through rectifiers D_1 and D_2 shorting the transformer secondary. Therefore, the current in the primary magnetizing inductance remains constant in this interval and is transferred to the load via D_1. Meanwhile, the current through D_2

continues to decrease due to the output voltage across L_1. This interval ends when the current through D_2 reaches zero. The currents flowing through the primary winding, D_1 and D_2 can be calculated respectively by:

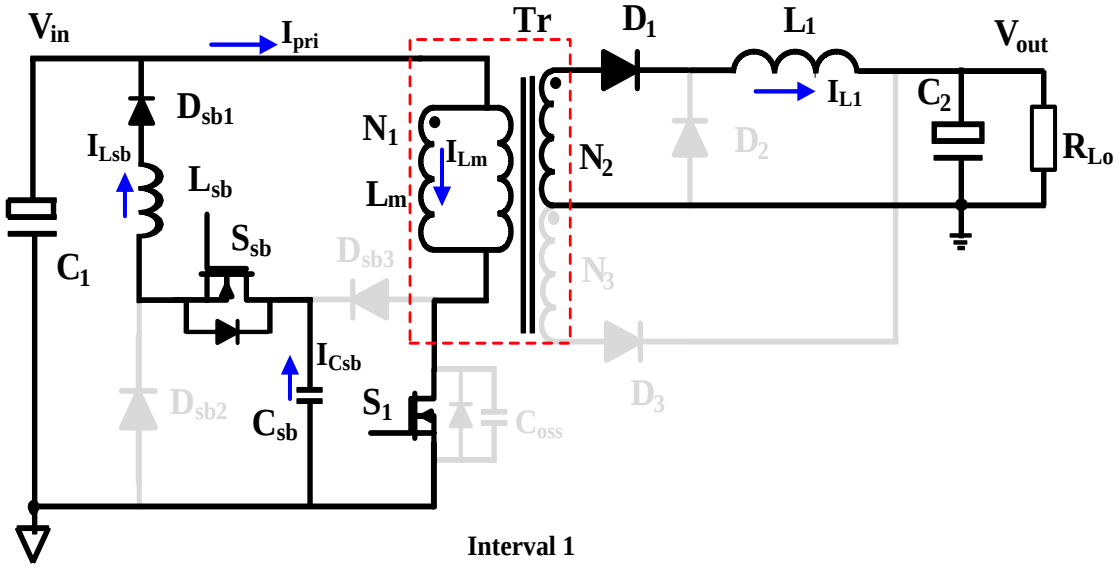
$$i_{Lm}(t) = \frac{V_{out}\frac{N_1}{N_3}}{z_c} \tag{2.12}$$

$$i_{D1}(t) = \frac{V_{out}\frac{N_1}{N_3}}{z_c} \cdot \frac{N_1}{N_2} \tag{2.13}$$

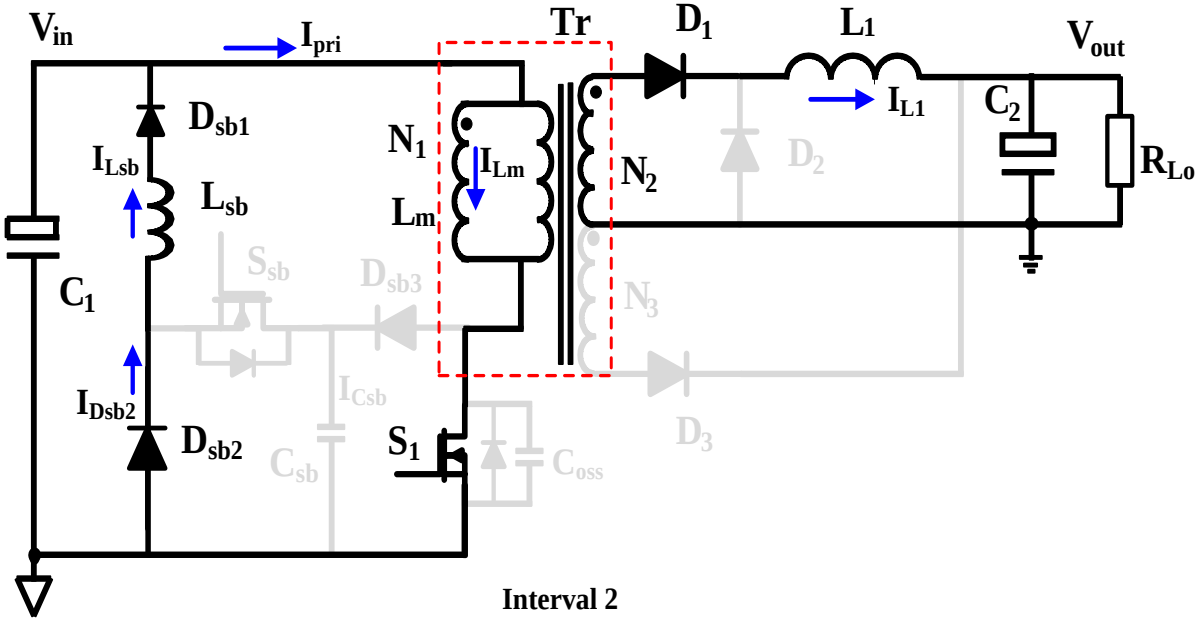
$$i_{D2}(t) = I_{L1}(t) - i_{D1}(t) \tag{2.14}$$

Once the current through D_2 reaches zero, the transformer is no longer shorted by output rectifiers D_1 and D_2. Thus, the current through the magnetizing inductor will change with the variation of voltage across the primary winding of the transformer. Because D_1 is still turned on during this time, the current through C_{oss} (I_{pri}) is equal to that of the magnetizing current I_{Lm} minus the reflected current of D_1 in the primary winding of the transformer. Consequently, the voltage across the MOSFET is decreasing due to the action of I_{pri}. As the resonant cycle progresses, the voltage across C_{oss} continues to decrease untill it reaches zero. After that, the body diode of the MOSFET S_1 conducts and the voltage across switch S_1 remains zero which produces zero-voltage switching. According to the Kirchhoff's Circuit Laws in this interval, the corresponding differential equations of current I_{pri}, I_{lm}, I_{D1} and voltage (V_{ds}) across C_{oss} can be represented by:

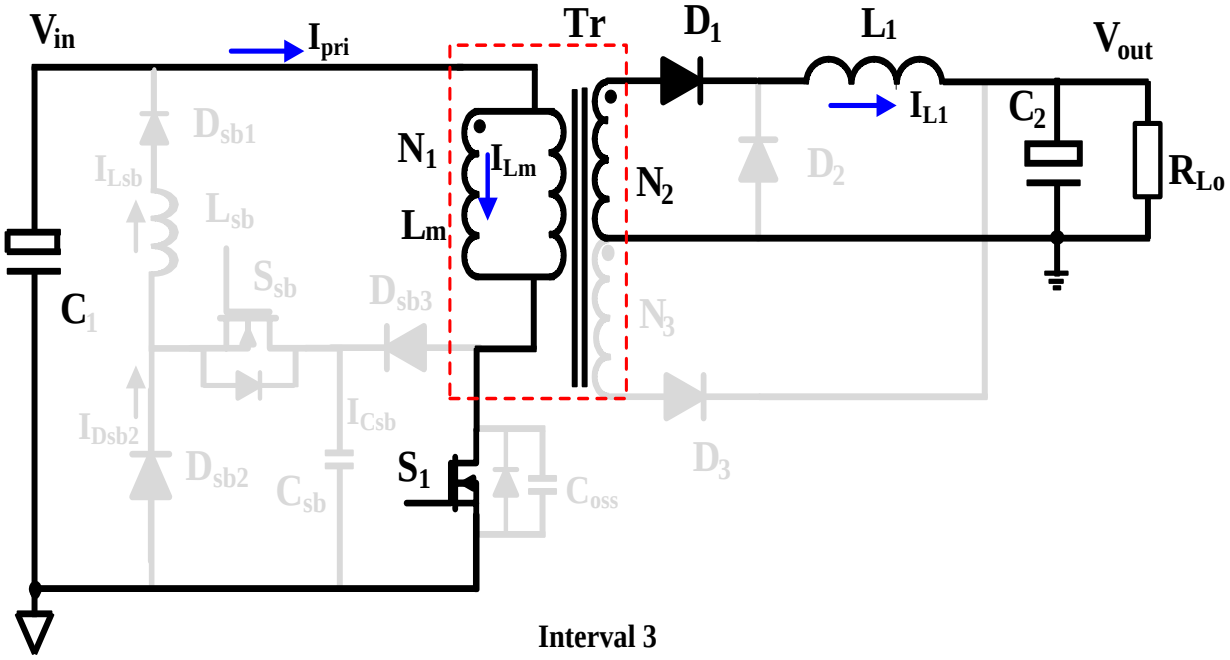
$$\begin{cases} L_m \frac{di_{Lm}(t)}{dt} + V_{ds}(t) = V_{in} \\ i_{Lm}(t) = \frac{N_2}{N_1} \cdot i_{D1}(t) + i_{Pri}(t) \\ i_{Pri}(t) = C_{oss} \frac{dV_{ds}(t)}{dt} \\ \frac{di_{D1}(t)}{dt} = \frac{-[V_{in} - V_{ds}(t)] \cdot \frac{N_2}{N_1} + V_{out}}{L_1} \end{cases} \tag{2.15}$$



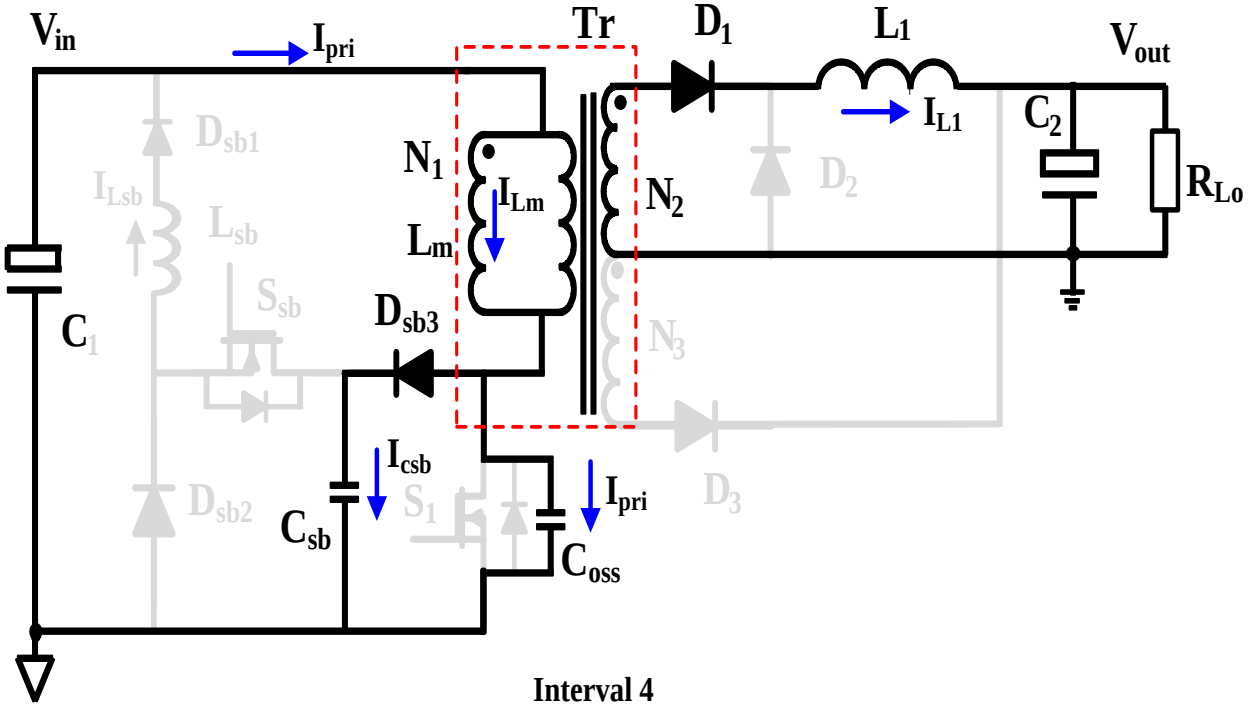
Interval 1



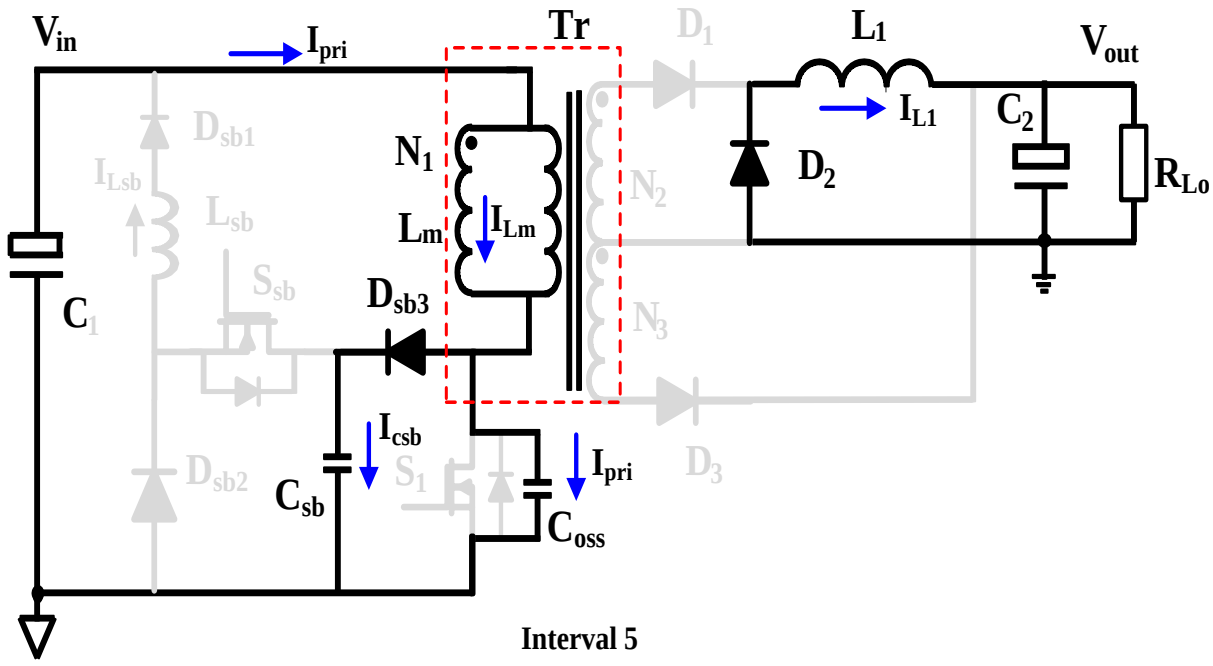
Interval 2



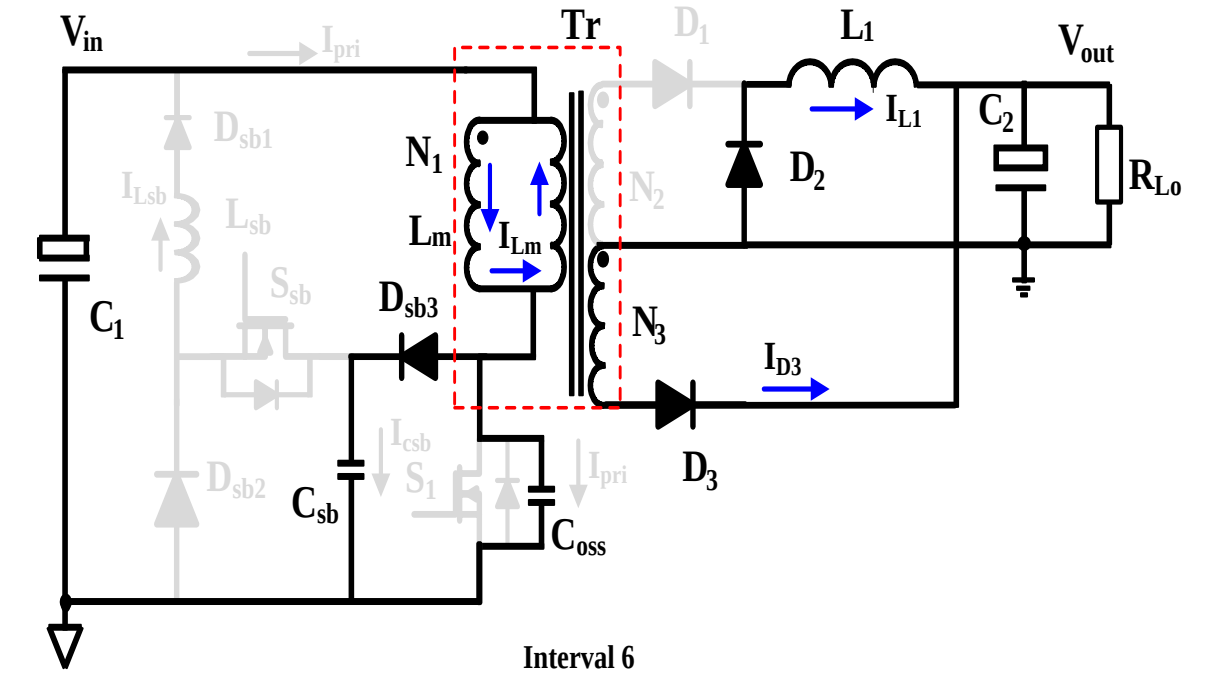
Interval 3



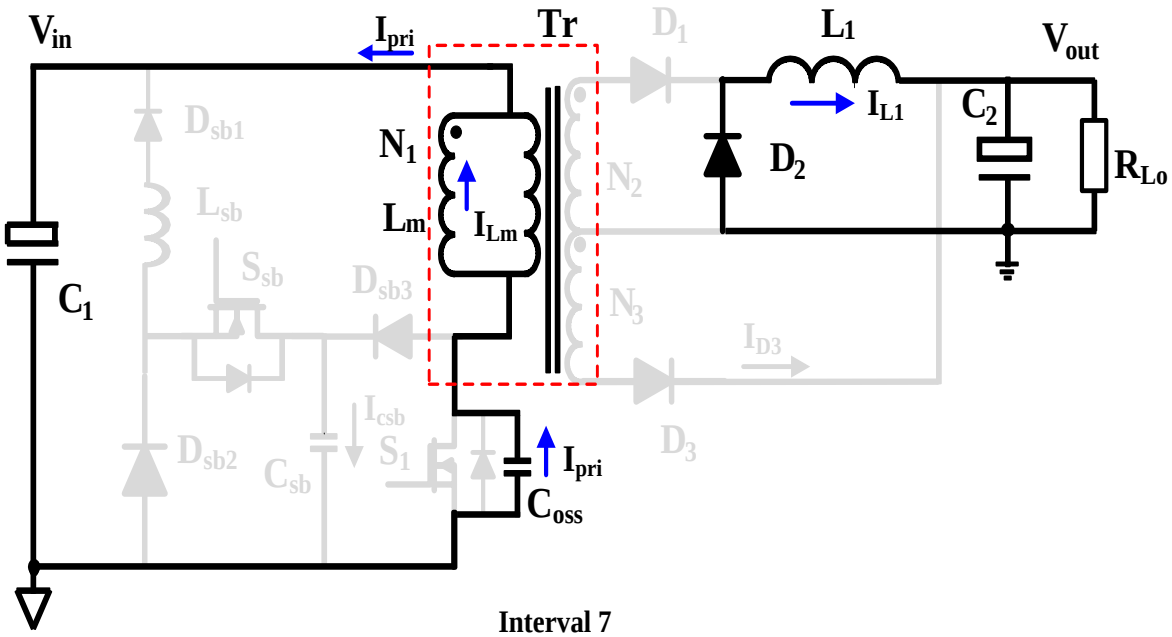
Interval 4



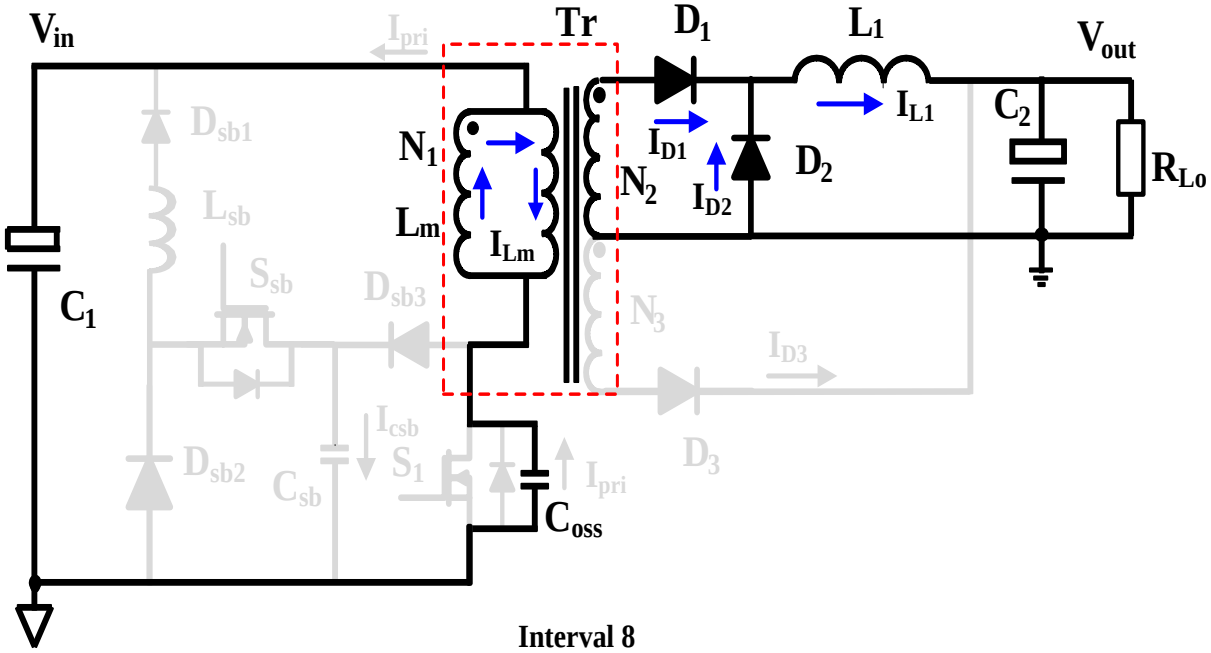
Interval 5



Interval 6



Interval 7



Interval 8

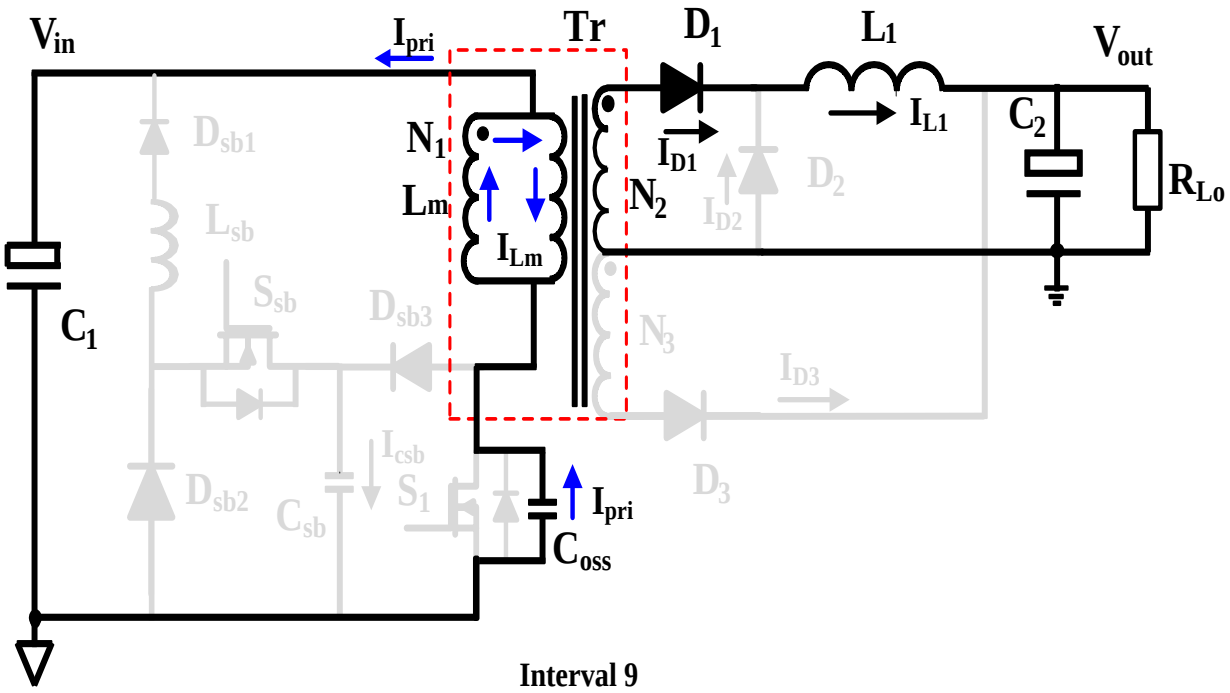


Figure 2.3 Operational intervals of ZVS Forward Flyback converter. (Interval 1) [t0-t1]. (Interval 2) [t1-t2]. (Interval 3) [t2-t3]. (Interval 4) [t3-t4]. (Interval 5) [t4-t5]. (Interval 6) [t5-t6]. (Interval 7) [t6-t7]. (Interval 8) [t7-t8]. (Interval 9) [t8-t0].

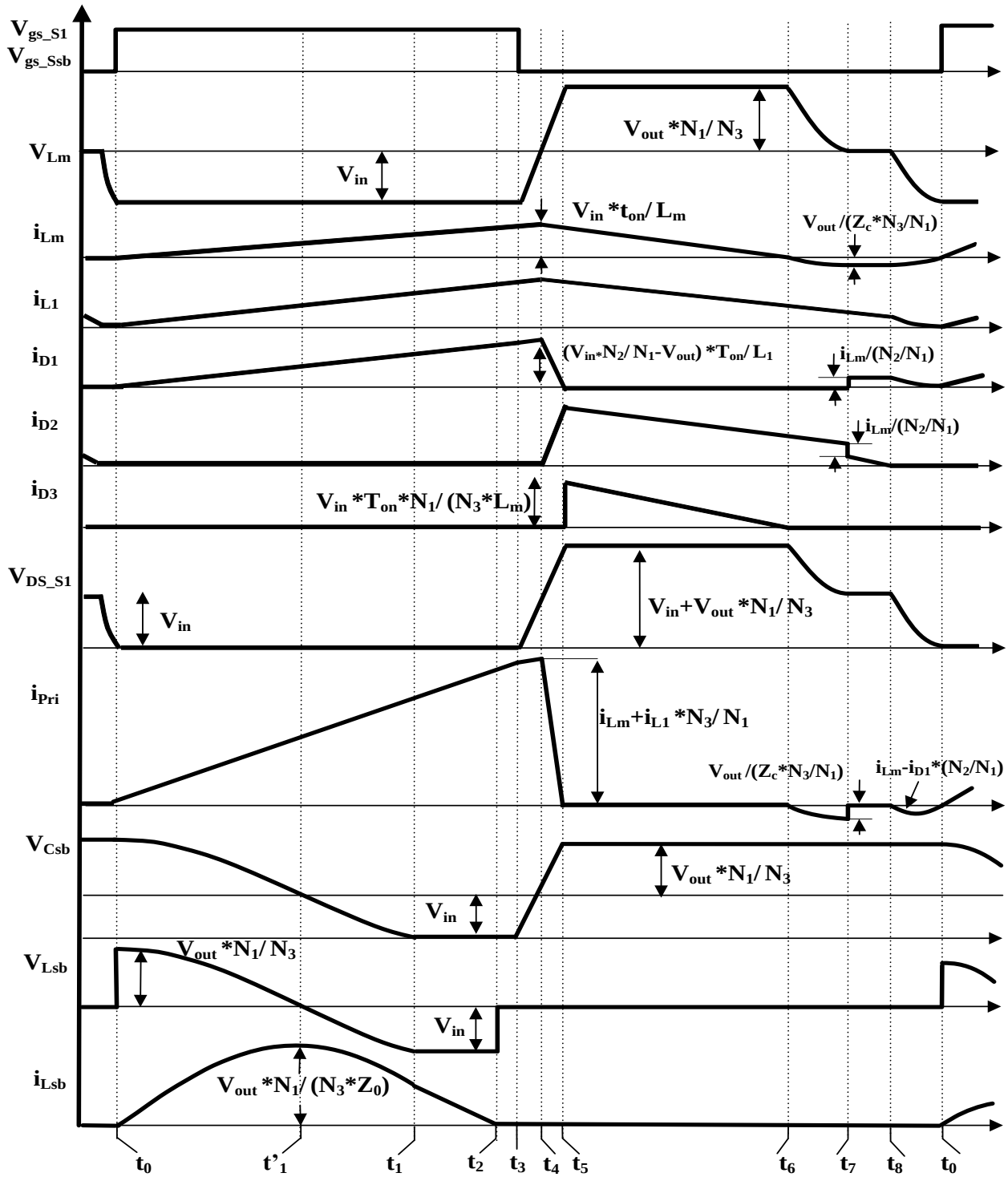


Figure 2.4 Theoretical waveforms of the BMFFC with efficient LC snubber circuit

2.3 BMFFC Steady State Analysis

Since both parts supply load current and are forced to have the same duty cycle, they are not independent [37]. Though we deliberately design BMFFC operates at boundary mode, the flyback and forward both have two operation regions of BCM and DCM with wide variation of input voltage. In order to analyze the steady state BMFFC characteristics, the normalized voltage ratio $V_{out}/(N*V_{in})$ at DCM is derived in this section. Followed the similar individual derivation of voltage ratio for the flyback converter and forward converter in [43], the average current from flyback and forward part is calculated as, respectively.

$$I_{fb_{avg}} = \frac{V_{in}}{2 \cdot L_m} \cdot \frac{N_1}{N_3} \cdot D \cdot T_s \cdot \frac{V_{in} \cdot D}{\frac{V_{out}}{\frac{N_3}{N_1}}} \tag{2.16}$$

$$I_{fw_{avg}} = \frac{V_{in}\frac{N_2}{N_1} - V_{out}}{2 \cdot L_1} \cdot D \cdot T_s \cdot \frac{V_{in}\frac{N_2}{N_1}}{V_{out}} \cdot D \tag{2.17}$$

Combining equations (2.16) and (2.17), the total output current (I_{out}) is the sum of both part's average current as

$$\frac{V_{in}}{2 \cdot L_m} \cdot \frac{N_1}{N_3} \cdot D \cdot T_s \cdot \frac{V_{in} \cdot D}{\frac{V_{out}}{\frac{N_3}{N_1}}} + \frac{V_{in}\frac{N_2}{N_1} - V_{out}}{2 \cdot L_1} \cdot D \cdot T_s \cdot \frac{V_{in}\frac{N_2}{N_1}}{V_{out}} \cdot D = I_{out} \tag{2.18}$$

And from [43] the output current of the forward converter and flyback converter required for a continuous conduction mode is maximum at D=0.5, then we get $I_{Lo\_max} = \frac{V_{in}T_s}{8*L_1}\frac{N_2}{N_1}$ and $I_{LB\_max} = \frac{V_{in}T_s}{8*L_m*\frac{N_3}{N_1}}$.

Substituting I_{Lo_max} and I_{LB_max} into (2.18), the normalized voltage ratio Vout/(N*Vin) of BMFFC can be expressed as (2.19).

$$V_N = \frac{V_{out}}{N * V_{in}} = \frac{1+k}{\frac{I_{out}}{4 \cdot I_{Lo,max}} + D^2} \cdot D^2 \tag{2.19}$$

Where, $k = \frac{\frac{N_3}{N_2} I_{LB,max}}{I_{L1,max}} = \frac{L_1}{L_m} \frac{N_1^2}{N_2 \cdot N_3}$ and $N = \frac{N_2}{N_1}$

The normalized voltage ratio is plotted, shown in Figure 2.5, as a function of I_{out}/I_{L1_max} for various values of duty ratio using (2.19), when k is selected as 0.3 from the parameters in Table I. The boundary between CCM and DCM is shown in Figure 2.5 by a dashed red line.

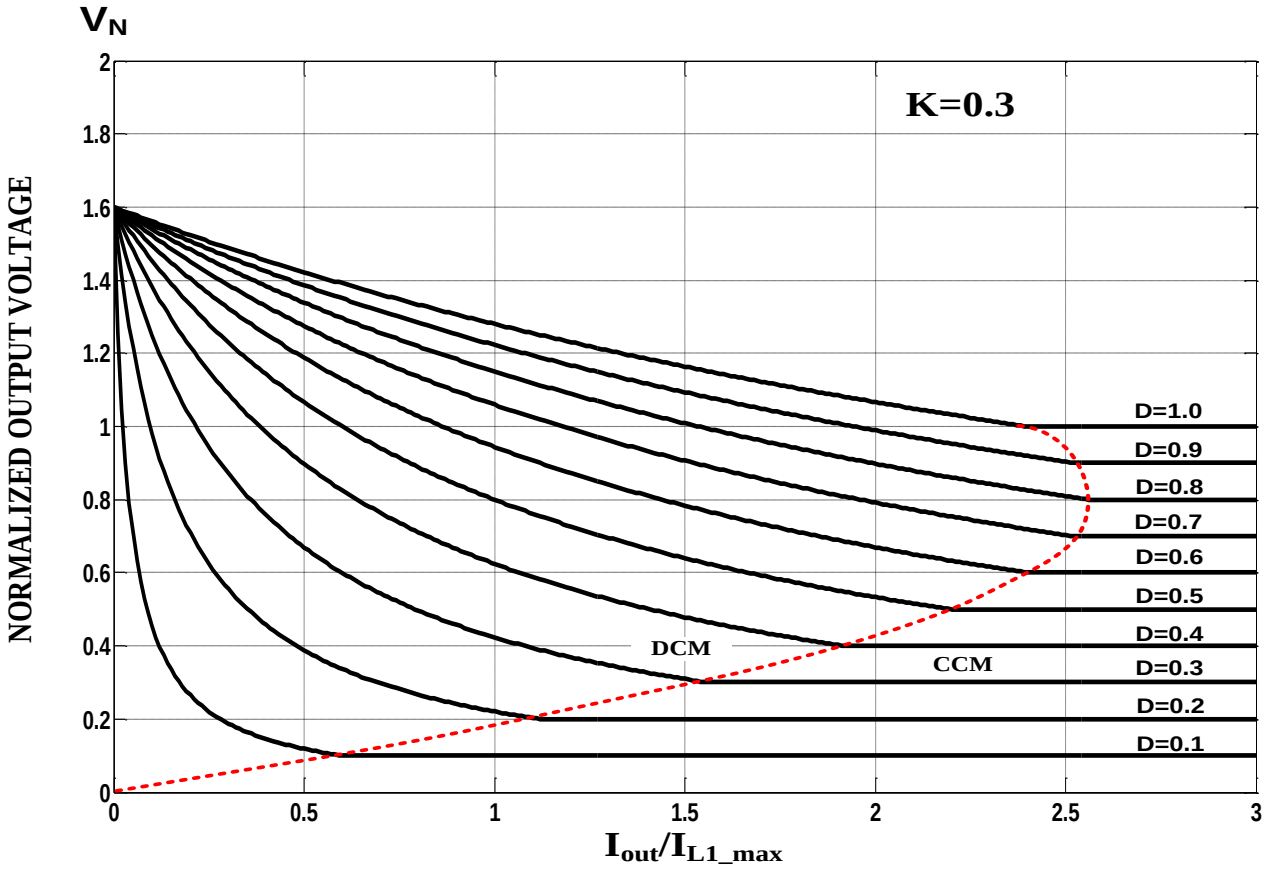


Figure 2.5 Continuous conduction mode CCM/DCM operation region of BMFFC

In order to intuitively see the variation of voltage ratio of BMFFC along with switching frequency, duty ratio, and output power change, a specific quantitative analysis as an example is provided based on the specification in Table I. The voltage ratio of BMFFC is rewritten while we

consider interval 7 and interval 9. The average output current of BMFFC is given by combining (2.6) and (2.7):

$$\begin{cases} I_{out} = i_{forward} + i_{flyback} = \frac{V_{in}\cdot\frac{N_2}{N_1} - V_{out}}{2L_1}\cdot t_{on}\cdot\frac{T_s-\tau}{T_s} + \frac{V_{in}}{2L_m}\cdot\frac{N_1}{N_3}\cdot t_{on}\cdot\frac{T_s-\tau-t_{on}}{T_s} \\ t_{on} = t_3 - t_0 = DT_s \\ \tau = \pi\sqrt{L_m C_{oss}} \end{cases} \tag{2.20}$$

From the load aspect, the output current can be also expressed by $I_{out} = \frac{V_{out}}{R_L}$. Then, voltage ratio can be derived by:

$$M = \frac{V_{out}}{V_{in}} = \frac{\left(\frac{N_2}{L_1N_1} + \frac{N_1}{N_3L_m} - \frac{N_1D}{N_3L_m}\right) - \frac{\tau}{T_s}\left[\frac{N_2}{L_1N_1} + \frac{N_1}{N_3L_m}\right]}{\frac{T_s-\tau}{T_sL_1} + \frac{2}{R_LDT_s}} \tag{2.21}$$

Let $\alpha = \frac{N_2}{L_1N_1}, \beta = \frac{N_1}{N_3L_m}, \gamma = \frac{T_s-\tau}{T_sL_1}, \delta = \frac{\tau}{T_s}$

$$M = \frac{\alpha+\beta(1-D)-\delta(\alpha+\beta)}{\gamma+\frac{2}{R_LDT_s}} \tag{2.22}$$

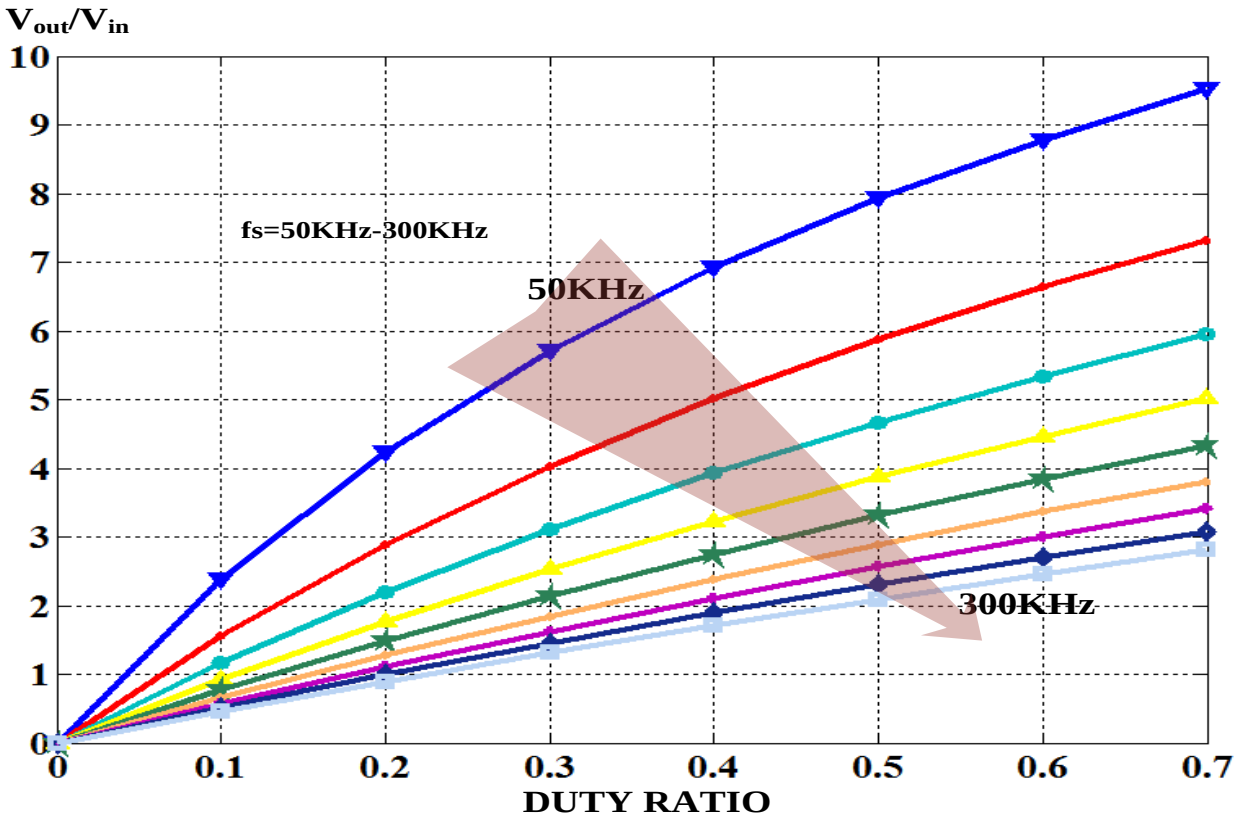


Figure 2.6 DC gain of BMFFC as a function of duty ratio

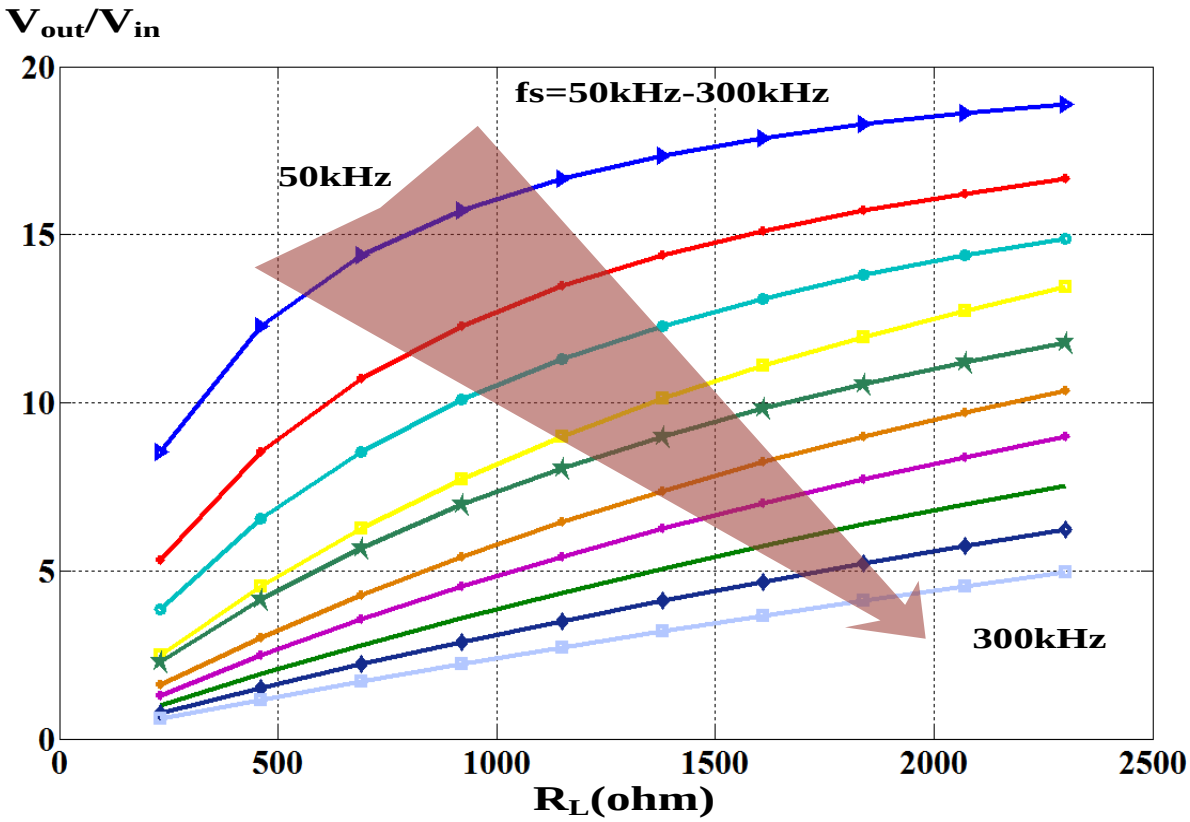


Figure 2.7 DC gain of BMFFC as a function of load

Using (2.20), the voltage gain of the BMFFC varies with duty ratio and switching frequency. The gain from 50 kHz to 300 kHz is plotted in Figure 2.6. Under this condition according to Table I: R_L=230ohm, $\alpha = 37037, \beta = 11122, \gamma = 3518, \delta = 0.05$. Figure 2.7 shows that the voltage gain varies with loads from 10% to 100% with a switching frequency between 50 kHz to 300 kHz.

2.4 ZVS Condition Discussion

Achieving ZVS depends heavily on the currents through D_3 and L_1. Based on whether current of D_3 reaches zero first or not in Interval 6, two ZVS conditions exist. For these two conditions the

ZVS design considerations are different. In this section, two ZVS conditions will be explored and circuit parameter constraints will be derived for each.

2.4.1 Output inductor current I_{l1} reaches zero first

The key waveforms are shown in Figure 2.8. This is the same as a conventional boundary mode flyback converter so the voltage across MOSFET can be expressed by (2.23).

$$V_{ds}(t) = V_{in} + V_{out}\frac{N_1}{N_3}\cos\omega_c(t - t_7) \tag{2.23}$$

If the turns ratio of N_3/N_1 is selected so that V_{DS}=0 in (2.23), and $\cos\omega_c(t - t_7)$ is equal to -1 after half of the resonant period, we can derive the ZVS condition from (2.23) in terms of the turns ratio of N_3/N_1 and the ratio of output voltage to input voltage as shown in (2.24).

$$\frac{N_3}{N_1} \leq \frac{V_{out}}{V_{in}} \tag{2.24}$$

Using (2.24) and the design specifications from Table I, the boundary of ZVS can be plotted as shown Figure 2.9. The range of turns ratio (N_3/N_1) required to achieve ZVS is indicated by the yellow area with a maximum of 9.2 at 25V input and 4.6 at 50V input.

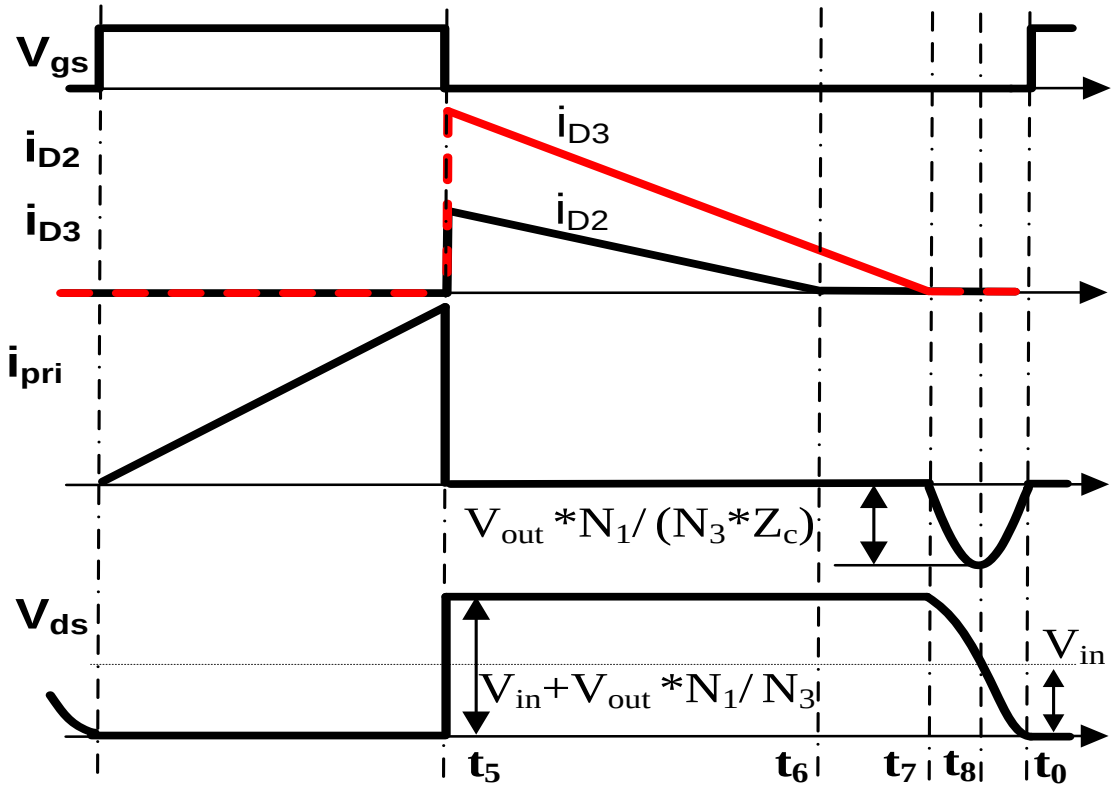


Figure 2.8 Key waveforms of BMFFC during off time

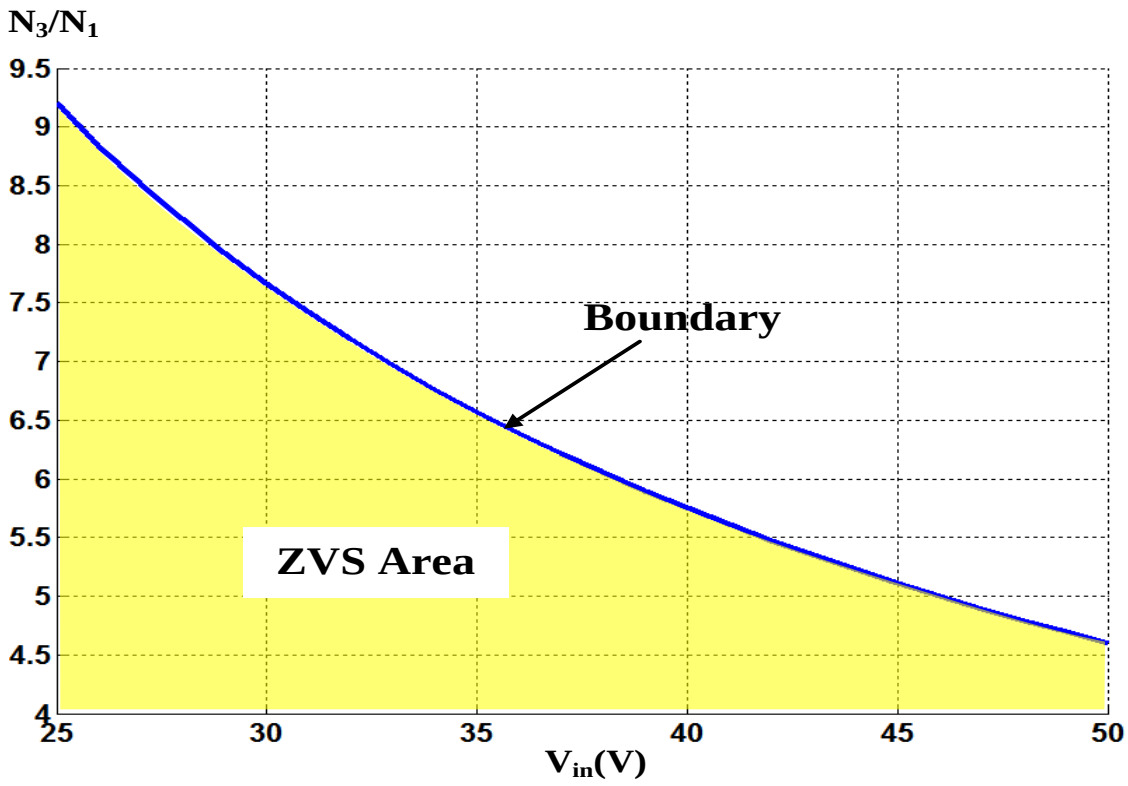


Figure 2.9 ZVS condition as a function of the input voltage and turns ratio (N3/N1)

2.4.2 Current I_{D3} reaches zero first

Before the I_{D3} reaches zero and when the voltage across the S_1 resonates to V_{in}, the primary magnetizing current transfers to the secondary due to shorting of the secondary winding via D_1 and D_2. The voltage across S_1 remains at V_{in} during this time. Once the current I_{D3} reaches zero, the resonance resumes and the ZVS condition can be calculated using (2.25). Per the description of Interval 9 in Section 2.2, and considering the leakage inductance of the transformer, the differential equation to describe the principle of operation can be represented by:

$$\begin{cases} L_{lk}\frac{di_{Pri}}{dt} + L_m\frac{di_{Lm}}{dt} + V_{ds} = V_{in} \\ i_{Lm} = \frac{N_2}{N_1}\cdot i_{D1} + i_{Pri} \\ i_{Pri} = C_{oss}\frac{dV_{ds}}{dt} \\ \frac{di_{D1}}{dt} = \frac{-(V_{in}-V_{ds})\cdot\frac{N_2}{N_1}+V_{out}}{L_1} \end{cases} \tag{2.25}$$

Simplify (2.25) and the differential equation can be expressed by (2.26):

$$\frac{(L_m+L_{lk})C_{oss}}{\left[1+\frac{L_m}{L_1}\left(\frac{N_2}{N_1}\right)^2\right]}\frac{dV_{ds}{}^2}{dt^2} + V_{ds} = V_{in} - \frac{\frac{L_m}{L_1}\frac{N_2}{N_1}}{\left[1+\frac{L_m}{L_1}\left(\frac{N_2}{N_1}\right)^2\right]}V_{out} \tag{2.26}$$

$$\text{Let } V_{pri}{}' = \frac{\frac{L_m}{L_1}\frac{N_2}{N_1}}{\left[1+\frac{L_m}{L_1}\left(\frac{N_2}{N_1}\right)^2\right]}V_{out} \tag{2.27}$$

By combining (2.26) and (2.27), the solution of the differential equation can be calculated in (2.28):

$$\begin{cases} V_{ds}(t) = V_{in}-V_{pri}{}' - \left[V_{in}-V_{pri}{}' - V_{ds}(t_8)\right]\cdot\cos\omega_{c1}(t-t_8) + z_{c1}\cdot i_{pri}(t_8)\sin\omega_{c1}(t-t_8) \\ i_{pri}(t) = C_{oss}\cdot\omega_{c1}\cdot\left[V_{in}-V_{pri}{}' - V_{ds}(t_8)\right]\cdot\sin\omega_{c1}(t-t_8) + C_{oss}\cdot z_{c1}\cdot\omega_c\cdot i_{pri}(t_8)\cdot\cos\omega_{c1}(t-t_8) \\ where \quad \omega_{c1} = \frac{1}{\sqrt{\frac{(L_m+L_{lk})C_{oss}}{1+\frac{L_m}{L_1}\left(\frac{N_2}{N_1}\right)^2}}};\ z_{c1} = \sqrt{\frac{(L_m+L_{lk})}{C_{oss}}} \end{cases} \tag{2.28}$$

And according to the initial condition at t_8:

$$\begin{cases} i_{Lm}(t_8) = -\frac{V_{out}\frac{N_1}{N_3}}{z_c} \\ V_{ds}(t_8) = V_{in} \\ i_{Pri}(t_8) = 0 \end{cases} \tag{2.29}$$

Then substituting (2.29) into (2.28), we get both functions of the voltage across S_1 and the current (i_{pri}) through C_{oss}:

$$\begin{cases} V_{ds}(t) = V_{in} - {V_{pri}}' + {V_{pri}}' \cos \omega_{c1}(t - t_8) \\ i_{pri}(t) = -C_{oss} \cdot \omega_{c1} \cdot {V_{pri}}' \cdot \sin \omega_{c1}(t - t_8) \end{cases} \tag{2.30}$$

From (2.30), ZVS condition can be expressed by (2.31) if the voltage across S_1 reaches zero:

$$V_{in} - {V_{pri}}' + {V_{pri}}' \cos \omega_{c1}(t - t_8) = 0 \tag{2.31}$$

Thus, after a half resonant period: $\omega_{c1}(t - t_8) = \pi$:

$$V_{in} - {V_{pri}}' - {V_{pri}}' = 0 \tag{2.32}$$

Plug (2.27) into (2.32) and simplify, we get (2.33):

$$\frac{\frac{L_m}{L_1}\frac{N_2}{N_1}}{\left[1+\frac{L_m}{L_1}\left(\frac{N_2}{N_1}\right)^2\right]} \cdot V_{out} \geq \frac{V_{in}}{2} \tag{2.33}$$

Let $\lambda = \frac{L_1}{L_m}, N = \frac{N_2}{N_1}, M = \frac{V_{out}}{V_{in}}$, then substitute λ, N, M into (2.33)

$$\frac{\frac{N}{\lambda}}{1+\frac{N^2}{\lambda}} \cdot V_{out} \geq \frac{V_{in}}{2} \tag{2.34}$$

Simplify (2.34)

$$\lambda \leq 2NM - N^2 \tag{2.35}$$

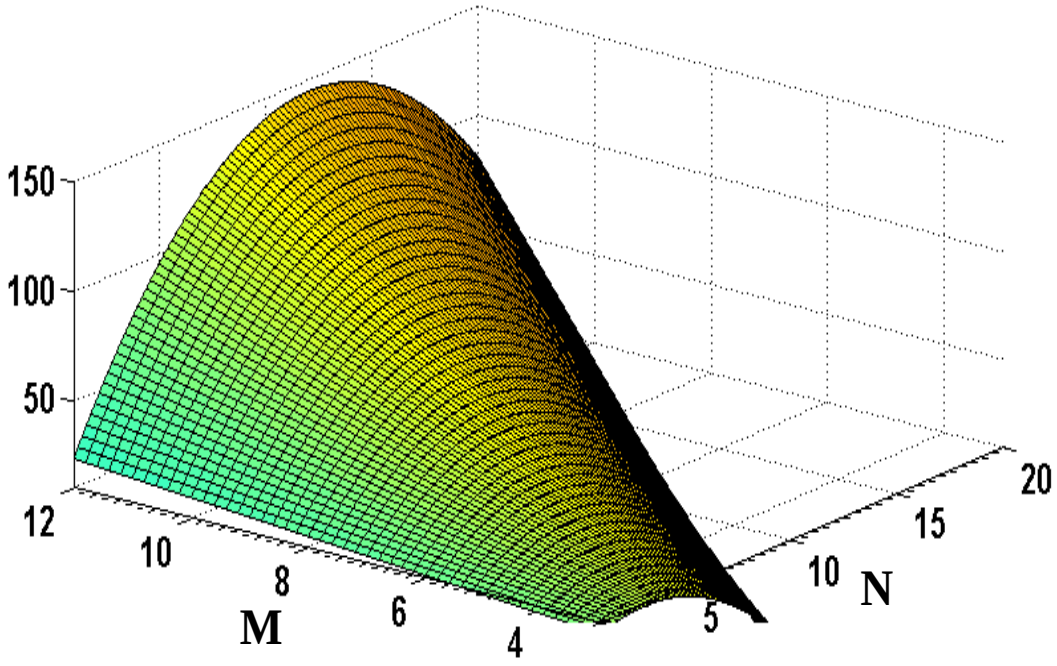


Figure 2.10 Three-Dimensional plot of the ratio λ (L1/Lm)

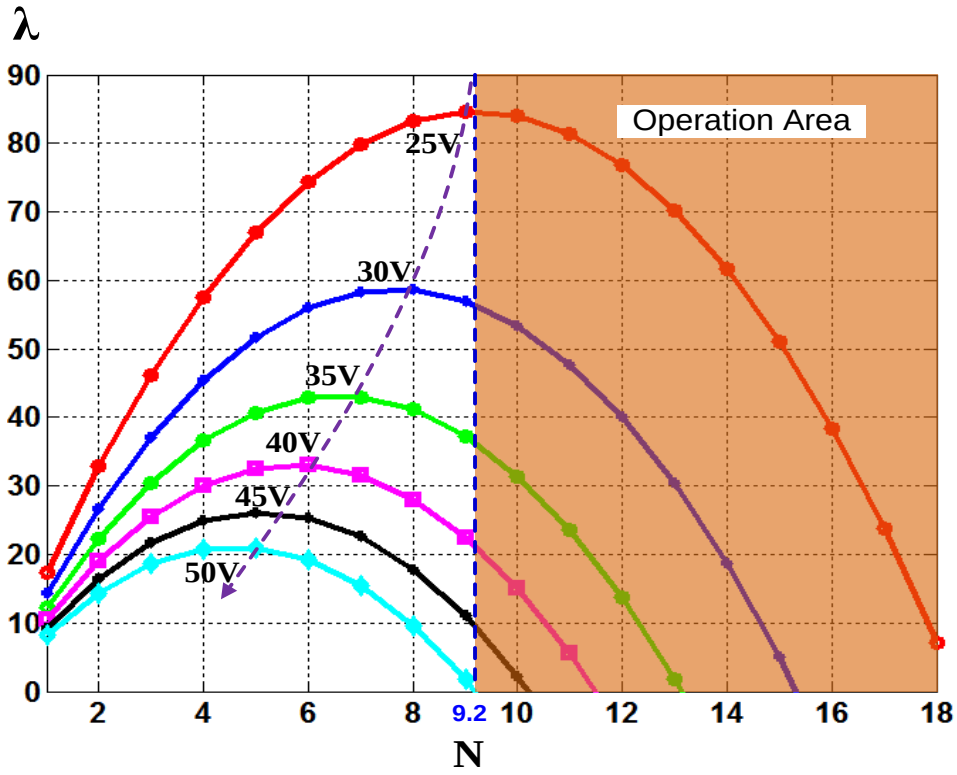


Figure 2.11 The ratio λ (L1/Lm) as a function of input voltage and turns ratio N (N2/N1)

In this case, the ZVS range is closely related to the ratio λ, the voltage gain M, and the turns ratio N_2/N_1 as illustrated in Figure 2.10. To clearly demonstrate the relationship between λ and turns ratio N with input voltage from 25V to 50V and a 230V output voltage, a 2-D graph is plotted in Figure 2.11. It can be seen from this that the region of parameter selection to achieve ZVS gradually decreases as input voltage increases which indicates ZVS is easier to achieve at low input voltages. Referring to the design specifications in Table I, the shaded operating ZVS area shows that the minimum turns ratio N (N_2/N_1) is 9.2 from (2.38). As shown in Figure 2.11, although ZVS will be lost at high input voltage, the efficiency at high input voltage generally is higher than low input voltage for most step-up DC-DC converters. Efficiency at the minimum input voltage determines the magnetic core selection, thermal design, and ultimately the size of the whole prototype. Therefore, the overall performance will be improved if the efficiency at low input voltage is significantly increased by trade-off design between high voltage and low voltage through the unique feature of BMFFC.

2.5 Design Guidelines

The key parameters in design of the BMFFC are discussed in this section with the following specifications:

Input voltage V_{in} = 25V-50V

Output voltage V_{out} = 230V

Output power P_{out} = 200W

Minimum switching frequency f_s = 50 kHz

2.5.1 Design of Turns Ratio of the Transformer (N_2/N_1&N_3/N_1)

In order to use 150V MOSFETs, the voltage stress across S_1 should be limited to 120V to provide some margin. Therefore, the turns ratio of N_2/N_1 should yield to (2.36) according to the voltage stress equation in Table I:

$$V_{in\_max} + \frac{N_1}{N_3} V_{out} < 120 \tag{2.36}$$

The turns ratios of N_3/N_1 can be simplified as:

$$\frac{N_3}{N_1} > \frac{V_{out}}{120 - V_{in\_max}} \tag{2.37}$$

Based on the specification: Vin_max=50V, Vout=230V, and the turns ratio of N_3/N_1 is selected as 3.3.

From the ZVS range analysis in section IV, the turns ratio N_2/N_1 strongly affects the ZVS condition with the variation of input voltage and λ. According to the plot in Figure 2.11, it is easier to achieve ZVS over the full input voltage range with a low turns ratio of N_2/N_1. Thus we need to choose the turns ratio of N_2/N_1 as small as possible. But according to the specification,

the lower limit of the turns ratio yielded by (2.38) is at the minimum input voltage of 25V. Therefore, the turns ratio of N_2/N_1 should greater than 9.2.

$$V_{in\_min} \cdot \frac{N_2}{N_1} > V_{out} \tag{2.38}$$

In general, efficiency increases with higher input voltages in a step-up DC/DC converter. With this in mind and referring to Figure 2.11, N=10 and λ=10 are chosen. Turn-on loss is still very small due to ZCS when compared to CCM hard switching even though ZVS is lost once the input voltage exceeds 43V.

2.5.2 Design of the Magnetizing Inductance L_m, and Output Inductance L_1

To simply the design, we assume the power converted from flyback operation and from forward operation is equal at the minimum input voltage and rated output power. The mathematical expressions can be given as:

$$\begin{cases} i_{forward} = i_{flyback} \\ I_{out} = i_{forward} + i_{flyback} \end{cases} \tag{2.39}$$

Considering load condition, the maximum output current is expressed by:

$$I_{out} = \frac{P_{out}}{V_{out}} \tag{2.40}$$

Substituting (2.40) and (2.39) into (2.20), we can derive the following constraints:

$$\frac{V_{in}}{2 \cdot L_m} \cdot \frac{N_1}{N_3} \cdot t_{on} \cdot \frac{T_s - \tau - t_{on}}{T_s} = 0.5 \cdot I_{out} \tag{2.41}$$

Simplify (2.41),

$$L_m = \frac{V_{in}}{I_{out}} \cdot \frac{N_1}{N_3} \cdot t_{on} \cdot \frac{T_s - \tau - t_{on}}{T_s} \tag{2.42}$$

As the current I_{L1} reaches zero first at 25V input, the DC gain of BMFFC can be expressed by $M_{Flyb} = \frac{N_3}{N_1}\frac{D}{1-D}$. Thus, the duty ratio is 0.736 and the turns ratio N_3/N_1= 3.3 is inserted in M_{Flyb}. Using (2.42) the designed value of the magnetizing inductance of the transformer L_m is 27uH with a switching frequency is 50 kHz at 25V input. Since λ (the ratio of L_1 to $L_{m)}$ was chosen to be 10, the designed value of the output inductor L_1 is 270uH.

2.5.3 Design of the Resonant Components in Snubber Circuit, C_{sb} and L_{sb}.

As we know, the voltage spike across MOSFET is caused by transferring the energy in the leakage inductor (L_{lk}) to the capacitor. Based on the law of conservation of energy, the resonant snubber capacitor value can be calculated by (2.43) under worst case conditions of maximum input voltage and full power:

$$\frac{1}{2}\cdot C_{sb}\cdot\left({V_{peak}}^2-{V_{in\_max}}^2\right)\geq\frac{1}{2}\cdot L_{lk}\cdot\left[i_{pri_{peak}}\right]^2 \tag{2.43}$$

Simplify (2.43):

$$C_{sb}=\frac{L_{lk}}{{V_{peak}}^2-{V_{in\_max}}^2}\cdot\left[i_{pri_{peak}}\right]^2 \tag{2.44}$$

In addition, the average input current is derived in (2.45) according to the specification:

$$\begin{cases} I_{in-avg}=\frac{1}{2}i_{pri_{peak}}\cdot\frac{t_{on}}{T_s}=\frac{1}{2}i_{pri_{peak}}\cdot D \\ I_{in-avg}=\frac{P_{in}}{V_{in}}=\frac{P_{out}}{\eta\cdot V_{in}} \end{cases} \tag{2.45}$$

Simplify (2.45) and the peak current can be expressed by (2.46):

$$i_{pri_{peak}}=\frac{2\cdot P_{out}}{\eta\cdot V_{in}\cdot D} \tag{2.46}$$

Then substitute (2.46) into (2.44):

$$C_{sb} = \frac{L_{lk}}{{V_{peak}}^2 - {V_{in\_max}}^2} \cdot \left(\frac{2 \cdot P_{out}}{\eta \cdot V_{in} \cdot D}\right)^2 \tag{2.47}$$

With D=0.46 from M_{Flyb}, voltage spike (V_{peak}) should not exceed 130V if we want to maintain a 20V margin for the 150V MOSFET. If an efficiency η=0.97 at 50V input is assumed at P_{out}=230W and L_{lk}=252nH from Table I, the calculated value of the resonant snubber capacitor C_{sb} using (35) is 8.48nF. The final value was chosen to be 9.4nF by paralleling two 4.7nF capacitors.

As analyzed in Section II, the interval from t_0 to t_2 is one half of the resonant period of the snubber capacitor C_{sb} and Lsb, which should be less than the minimum conduction time at the worst case condition of input voltage (50V) and output power (20W).

$$\pi \cdot \sqrt{L_{sb} \cdot C_{sb}} \leq t_{on} \tag{2.48}$$

Combining (2.6), (2.46) and (2.48), we get (2.49):

$$L_{sb} = \left(\frac{\frac{2 \cdot P_{out}}{\eta \cdot V_{in} \cdot D \cdot \pi}}{\frac{V_{in} \frac{N_2}{N_1} - V_{out}}{2 \cdot L_1} + \frac{V_{in}}{L_m}}\right)^2 \cdot \frac{1}{C_{sb}} \tag{2.49}$$

Thus, the calculated value of the resonant snubber inductor Lsb is 27.8uH. The known values of L_1, L_m, N_2, N_1 and D can be inserted into (37).

2.5.4 Design of the Output Capacitor C_2

Neglecting the interval shown in Figure 2.4 from t_3 to t_5 and from t_6 to t_0, voltage and current ripple of the output capacitor C_2 for one switching cycle is shown in Figure 2.12. The output

capacitor C_2 is charged by the sum of I_{L1} and I_{D3} during the period t_2-t_3. The output capacitor is discharging after t_3 while the load current (I_{out}) is greater than the sum of I_{L1} and I_{D3}.

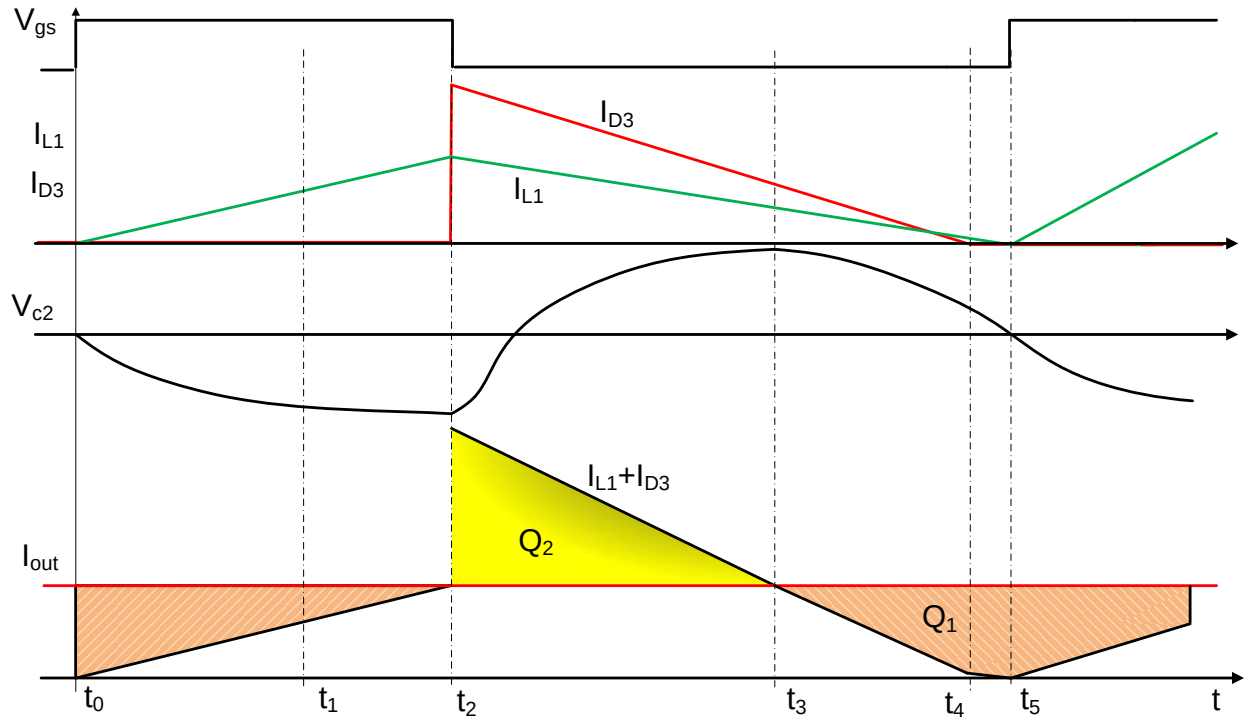


Figure 2.12 Voltage and current ripple in the output capacitor

The electric charge (Q_2) of the output capacitor from t_2 to t_3 can be represented by (2.50):

$$Q_2 = \int_{t_2}^{t_3} \left[i_{L1_{peak}} - \frac{V_{out}}{L_1} \cdot t + i_{D3_{peak}} - \frac{V_{out}}{\left(\frac{N_3}{N_1}\right)^2 \cdot L_m} \cdot t - I_{out} \right] dt \quad (2.50)$$

The equation after integration is:

$$Q_2 = \left(i_{L1\_peak} + i_{D3\_peak} - I_{out}\right) \cdot t \Big|_{t_2}^{t_3} - \frac{1}{2}\left[\frac{V_{out}}{L_1} + \frac{V_{out}}{\left(\frac{N_3}{N_1}\right)^2 \cdot L_m}\right] \cdot t^2 \Big|_{t_2}^{t_3} \quad (2.51)$$

Where:

$$t_3 - t_2 = \frac{(i_{L1\_peak} + i_{D3\_peak} - I_{out})}{\frac{V_{out}}{L_1} + \frac{V_{out}}{\left(\frac{N_3}{N_1}\right)^2 L_m}} \tag{2.52}$$

Substitute (2.52) into (2.51) and we get (2.53):

$$\mathrm{Q}_2 = \frac{1}{2} \cdot \left[\left(i_{L1\_peak} + i_{D3\_peak} - I_{out}\right) \cdot \frac{(i_{L1\_peak} + i_{D3\_peak} - I_{out})}{\frac{V_{out}}{L_1} + \frac{V_{out}}{\left(\frac{N_3}{N_1}\right)^2 L_m}} \right] \tag{2.53}$$

Then according to the equation $\mathrm{Q}_2 = C \cdot \Delta \mathrm{V}$, the capacitance can be calculated by (2.54):

$$C = \frac{\mathrm{Q}_2}{\Delta \mathrm{V}} = \frac{1}{2 \cdot \Delta \mathrm{V}} \cdot \left[\left(i_{L1\_peak} + i_{D3\_peak} - I_{out}\right) \cdot \frac{(i_{L1\_peak} + i_{D3\_peak} - I_{out})}{\frac{V_{out}}{L_1} + \frac{V_{out}}{\left(\frac{N_3}{N_1}\right)^2 L_m}} \right] \tag{2.54}$$

The output capacitor value is selected based on the current ripple through C_2 in one switching cycle and can be calculated as (2.55) for a resistive load.

$$C = \frac{\mathrm{Q}_2}{\Delta \mathrm{V}} = \frac{1}{2 \cdot \Delta \mathrm{V}} \cdot \left[\left(i_{L1\_peak} + i_{D3\_peak} - I_{out}\right) \cdot \frac{(i_{L1\_peak} + i_{D3\_peak} - I_{out})}{\frac{V_{out}}{L_1} + \frac{V_{out}}{\left(\frac{N_3}{N_1}\right)^2 L_m}} \right] \tag{2.55}$$

Given $i_{L1_{peak}} = 1A,\ i_{D3\_peak} = 3.9A, I_{out} = 1A$, and a desired output voltage ripple of 0.5V, the calculated value of output capacitor C_2 is 9.3uF. A value of 11uF was chosen by paralleling five 2.2uF ceramic capacitors.

2.6 Experimental Results Verification

Following the design guidelines in section 2.5, a 200W prototype was constructed to verify the performance of the BMFFC with non-dissipative LC snubber circuit. The specifications of the prototype are listed in Table I.

Table 1 Key parameters of a 200 W prototype

Input voltage	25V-50V	Rated output power	200W
Output voltage	230V	Switching frequency	50-220KHz
Turns number N_1:N_2:N_3	6:60:20	Magnetizing inductance	27uH
Leakage inductance	252nH	Output inductor L_1	270uH
Primary Mosfet S_1	FDB075N15A (2PCS)	Output rectifier D_1, D_2	STTH312S
Output capacitor C_2	C2220C225MAR2C (5PCS)	Output rectifier D_3	STTH310S
Trans Core Size	RM14	Snubber Capacitor C_{sb}	9.4nF
Snubber Inductor L_{sb}	CDRH127NP-270MC	Snubber switch S_{sb}	FDD7N20
Dsb1	B380	Dsb2,Dsb3	ES2D

A photograph of the laboratory prototype with 200W is shown in Figure 2.13. The experimental waveforms of BMFFC with different input voltages and power outputs are shown in Figure 2.14 through Figure 2.18. (CH1: voltage stress across S_1, CH2: output voltage 230V, CH3: output current, CH4: gate signal of MOSFET, the voltage and current scale is shown in the figures). Referring to Figure 2.14, with 25V input and 200W output, ZVS is achieved before the gate signal turns on. The voltage spike across S_1 is limited to 112V due to the effect of the LC snubber circuit. With the maximum input of 50V and 200W output, the voltage spike across S_1 is 128V as shown in Figure 2.15. The voltage across S_1 decreases to 14V at full power output

before the switch is turned on which reduces turn-on loss due to the fact that the current through MOSFET is already very small.

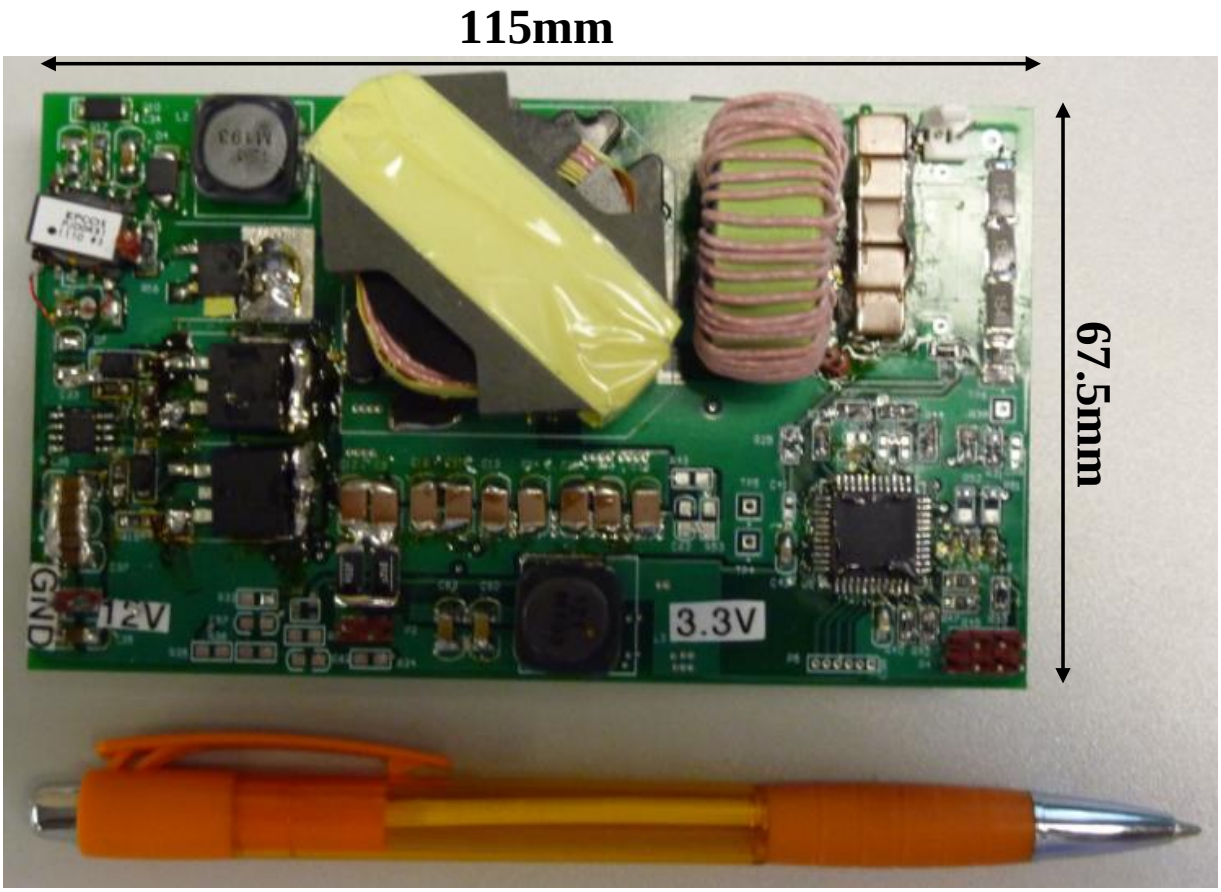


Figure 2.13 Photograph of the hardware prototype of BMFCC with 200W

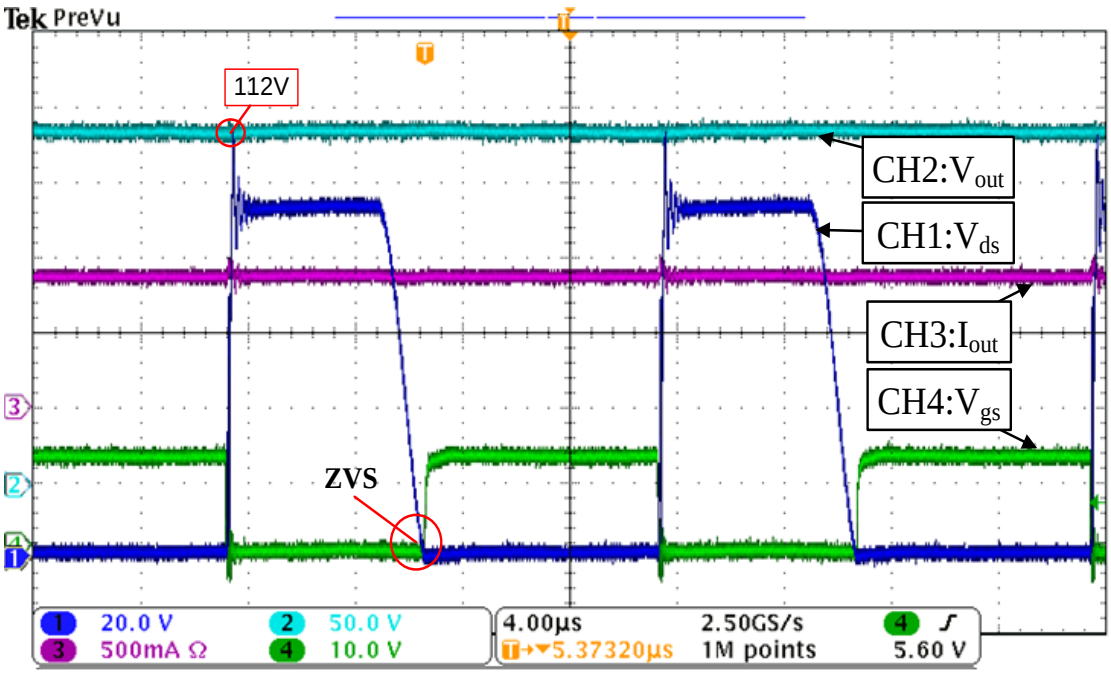


Figure 2.14 Measured waveforms of the BMFFC at 200W with 25V input

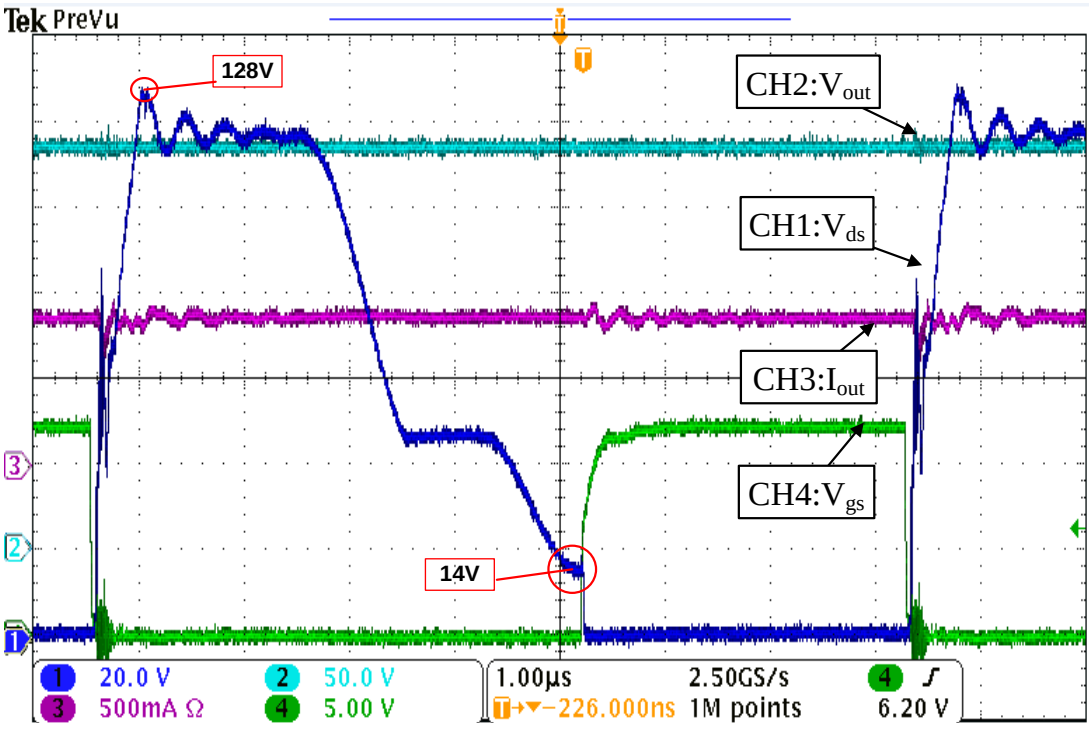


Figure 2.15 Measured waveforms of the BMFFC with 200W output and 50V input

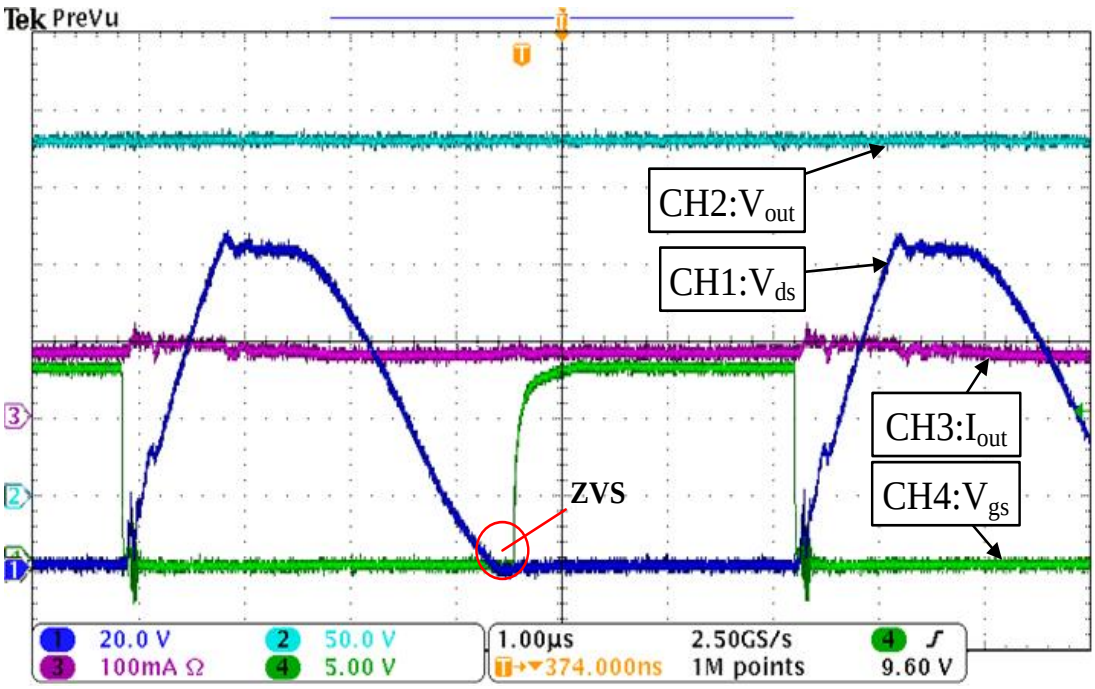


Figure 2.16 Measured waveforms of the BMFFC with 20W output and 25V input

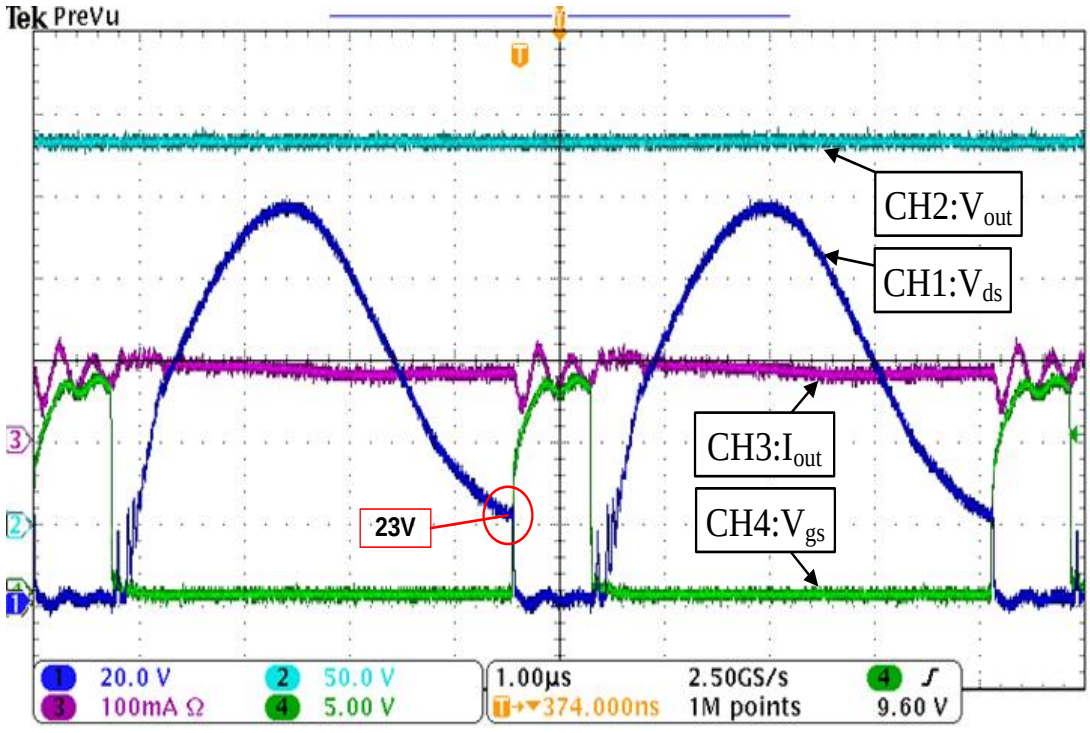


Figure 2.17 Measured waveforms of the BMFFC at 20W with 50V input

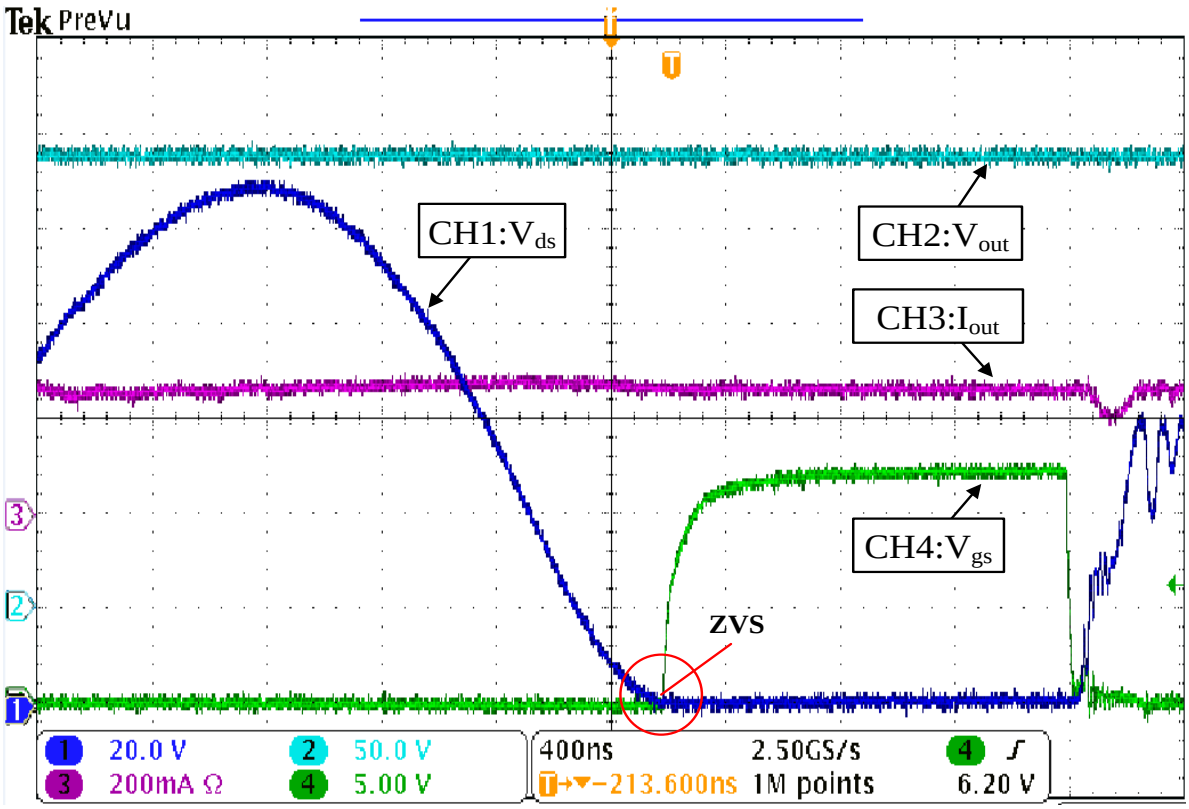


Figure 2.18 Measured waveforms of the BMFFC at 60W with 43V input

Figure 2.16 and Figure 2.17 show measured waveforms at 10% of rated power output at minimum and maximum input voltages. As seen in Figure 2.16, ZVS is still achieved at 10% of full load. Figure 2.17 shows experimental waveforms at maximum input voltage. The voltage across S_1 decreases to 23V at 20 watts output. Consequently, the turn-on loss of the BMFFC at light load is reduced. Figure 2.18 shows ZVS is still achieved even at 60 watts output with 43 input.

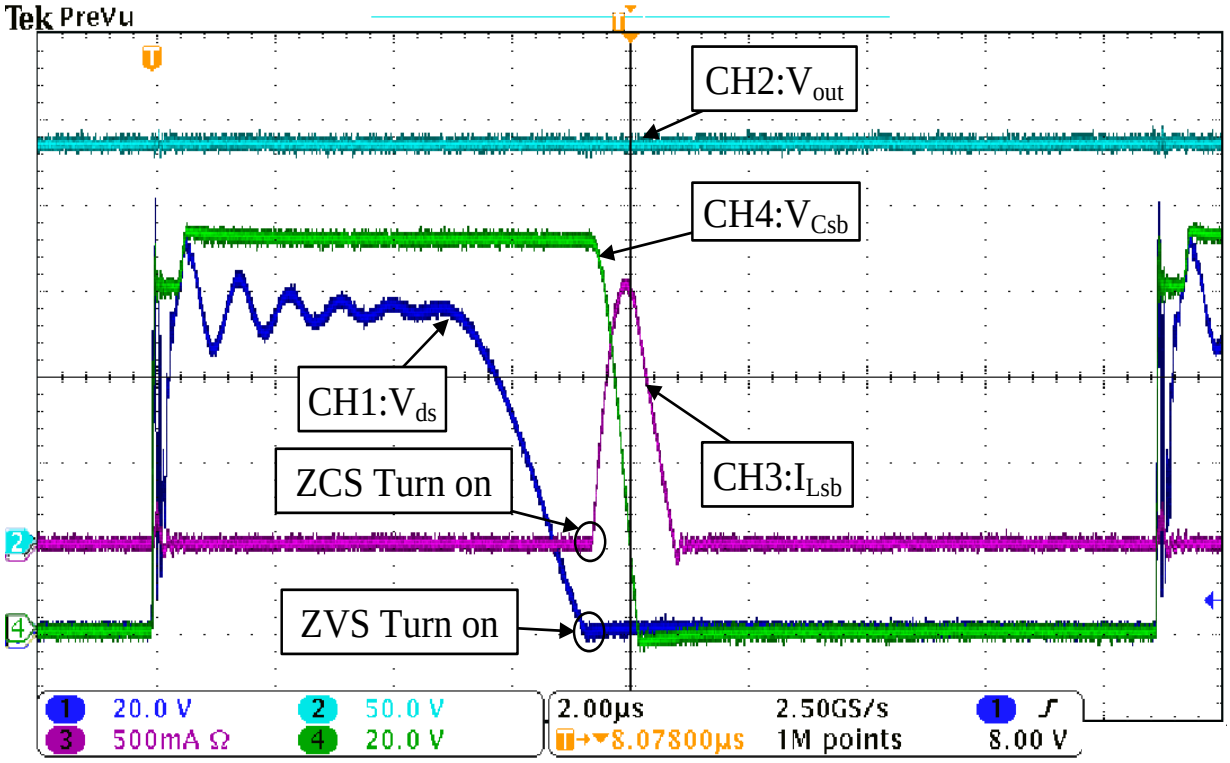


Figure 2.19 Measured waveforms of an efficient active LC snubber circuit

Figure 2.19 (CH1: voltage stress across S_1, CH2: output voltage 230V, CH3: the current i_{Lsb} through the snubber inductor L_{sb}, CH4: voltage stress across snubber capacitor C_{sb}) shows the measured voltage waveforms across the snubber capacitor C_{sb} and current waveform through the snubber inductor L_{sb}. As shown in Figure 2.19, the auxiliary switch S_{sb} is turned on with ZCS so its turn-on loss is small. The drive signal of S_{sb} is the same as that of S_1 and its current decreases to zero after a half of the sinusoidal resonant period so the turn-off loss in S_{sb} is also small. Figure 2.20 shows the measured output current which is the sum of i_{L1} and i_{D3} at 200W output with 25V input. Referring to Figure 2.20, the peak output current reaches 6.2A which is caused by energy stored in the leakage inductance of the transformer when D_3 starts to conduct.

Although the method of sandwich winding for BMFFC is employed as shown in Figure 2.21, the leakage inductance is still 252nH due to the separated forward and flyback windings in the secondary. Although an efficient LC snubber circuit is employed, efficiency is negatively impacted by transformer leakage inductance. Therefore, it is very important to minimize this parameter in production.

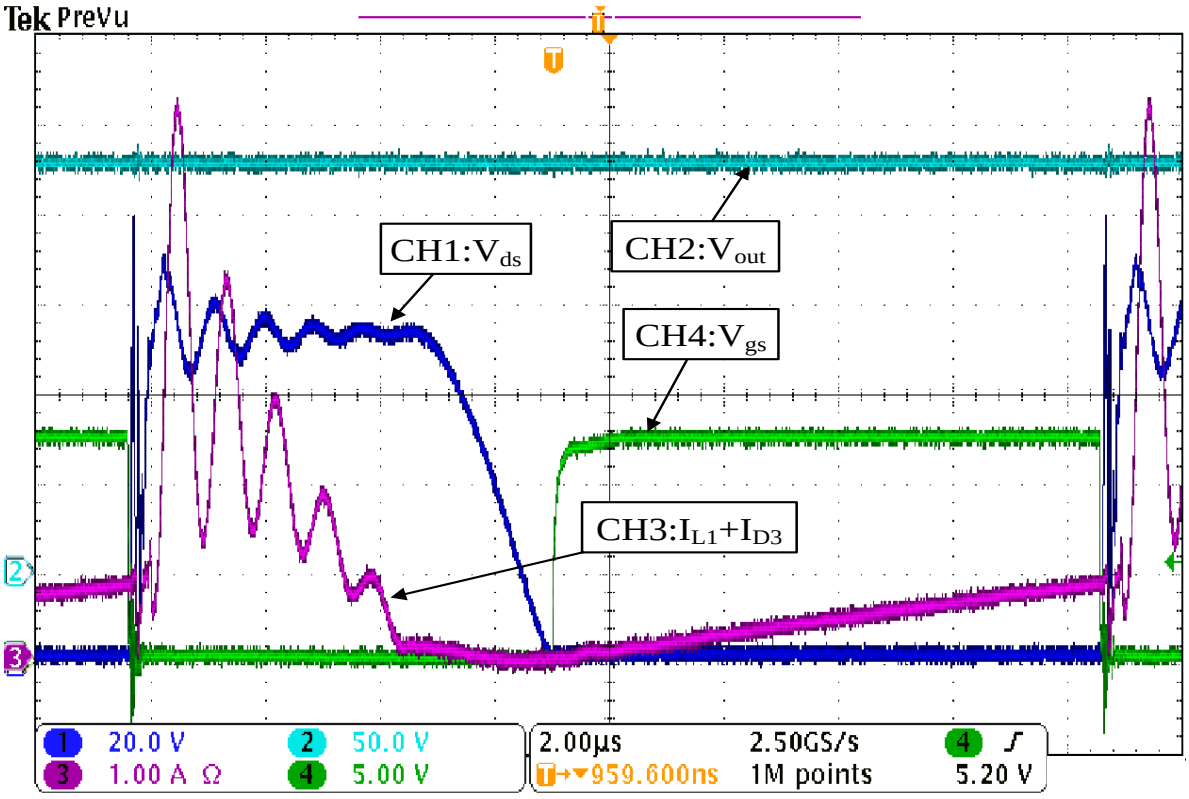


Figure 2.20 Sum of output current from Forward and Flyback sections

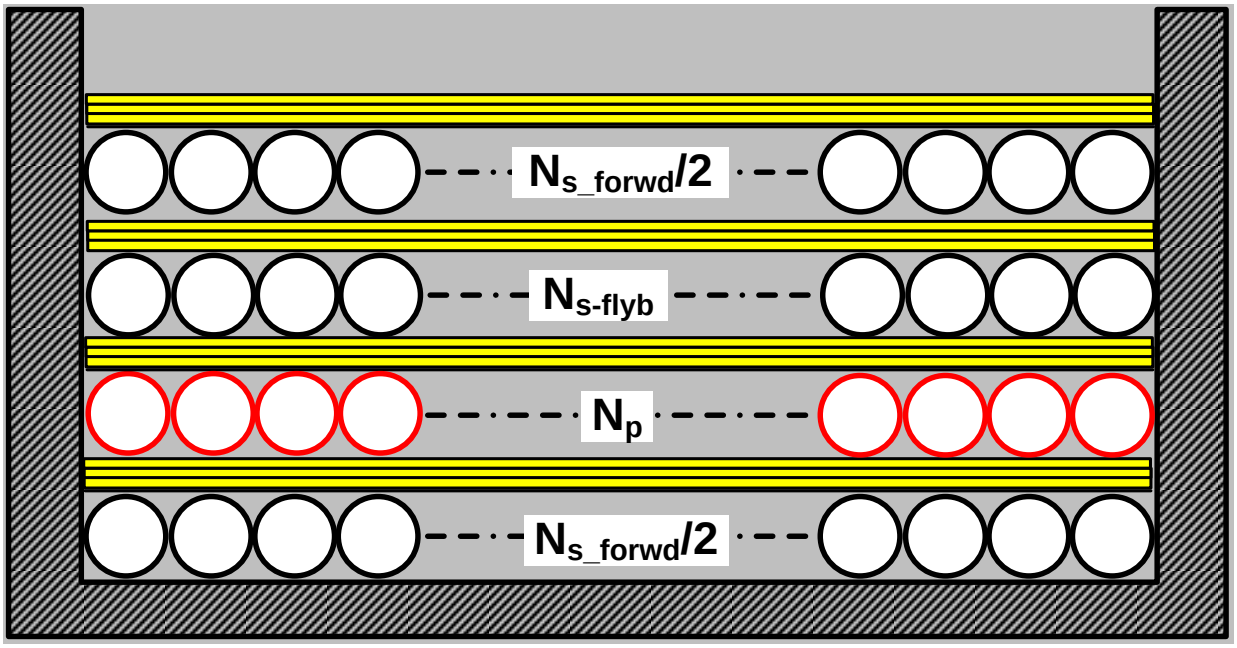


Figure 2.21 Transformer construction of BMFFC

The measured efficiency of the tested 200W prototype with different input voltages is shown in Figure 2.22. With 35V input voltage, the maximum efficiency is 97.2% and the efficiency at full load is over 96.5%. The efficiency at full load with 45-V input voltage is 96.7%. Even the input voltage is decreased to 25 V. The maximum efficiency of the tested prototype is still higher than 96.5%. According to the experimental data, peak efficiency is achieved at 35V instead of 50V. The interesting phenomena emerged because a variable switching frequency control scheme is employed over the entire range of input voltage and output power. The higher the input voltage, the higher the switching frequency is. Figure 2.23 shows measured efficiency of BMFFC with varying input voltage and output power.

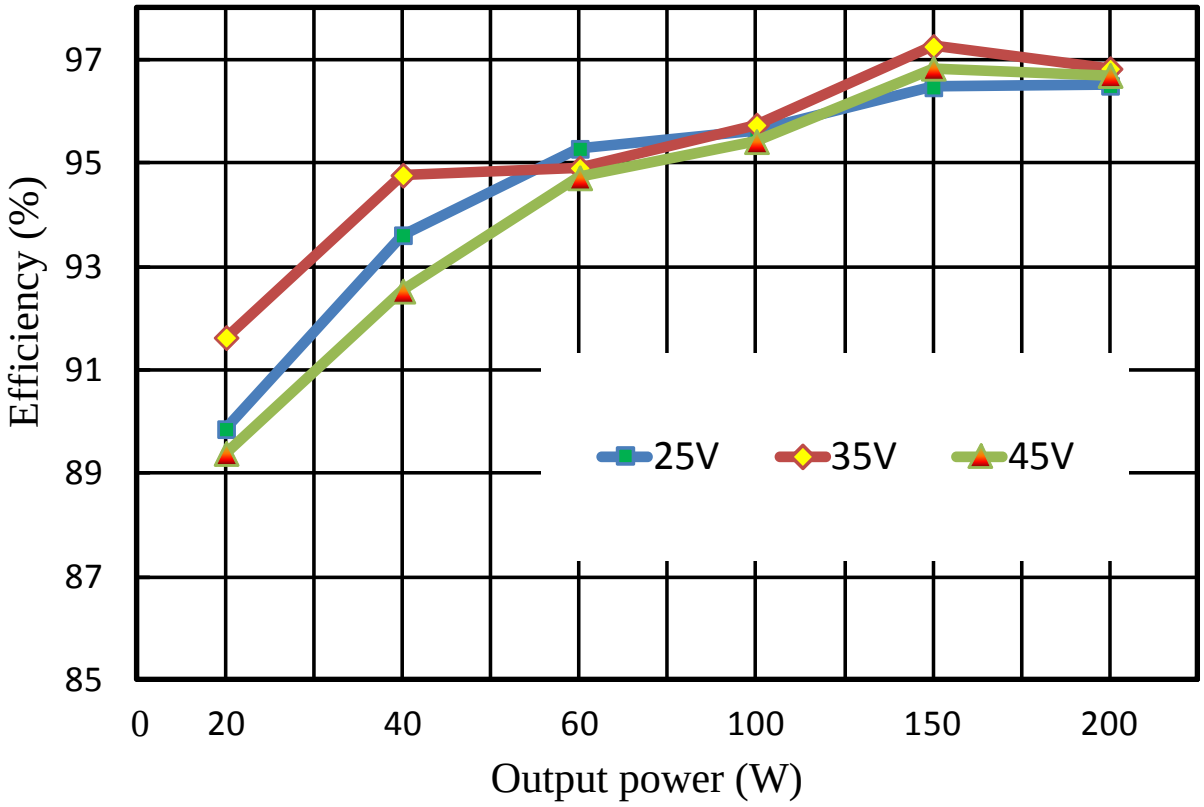


Figure 2.22 Measured efficiency of BMFFC according to the variation of the input voltage and output power

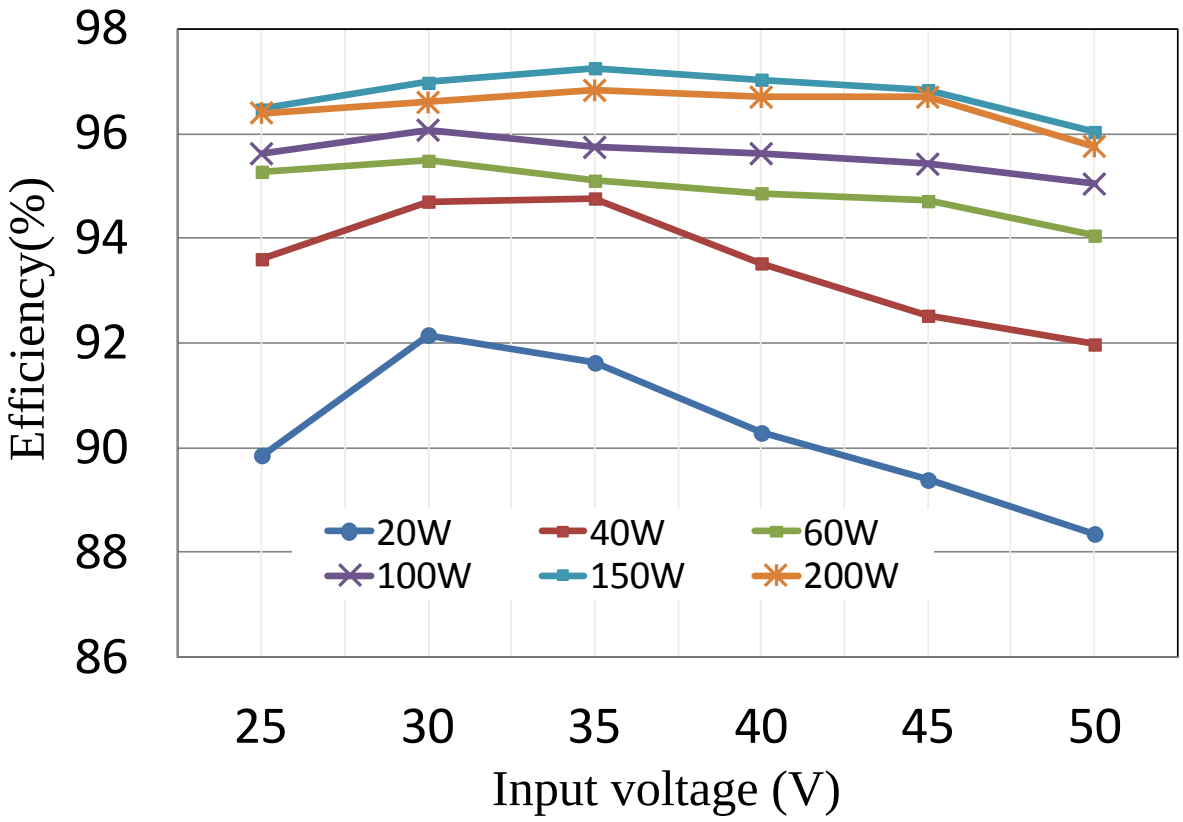


Figure 2.23 Measured efficiency of BMFFC according to the variation of the input voltage and output power

In order to observe the performance of an active LC snubber circuit, Figure 2.24 shows the measured waveforms of BMFFC without snubber circuit. As shown in Figure 2.24, the voltage spike across the MOSFET is 138V at 25V input and 200W output. Compared to Figure 2.14 with LC snubber circuit, the voltage spike is only 112V at the same condition. In addition, oscillation without the LC snubber circuit at turn off is worse than with LC snubber circuit. With the same transformer, MOSFET, and test bed, efficiency without the snubber circuit at 25V input and various power levels is shown in Figure 2.25. Note that 150V MOSFET should be changed to a higher voltage part if we want to measure efficiency without snubber circuit over the whole range of input voltage and output power. Obviously, the overall efficiency without the LC snubber circuit will drop due to conduction loss increase when a higher voltage MOSFET is used.

As mentioned previously, the efficiency at the minimum input voltage is a key factor in determining the size of the prototype. As shown in Figure 2.25, the overall efficiency without the LC snubber circuit is 0.5-1 percentage points less than with the LC snubber circuit. Therefore, it can be concluded that an active LC snubber circuit improves efficiency even though we select a point of comparison at 25V.

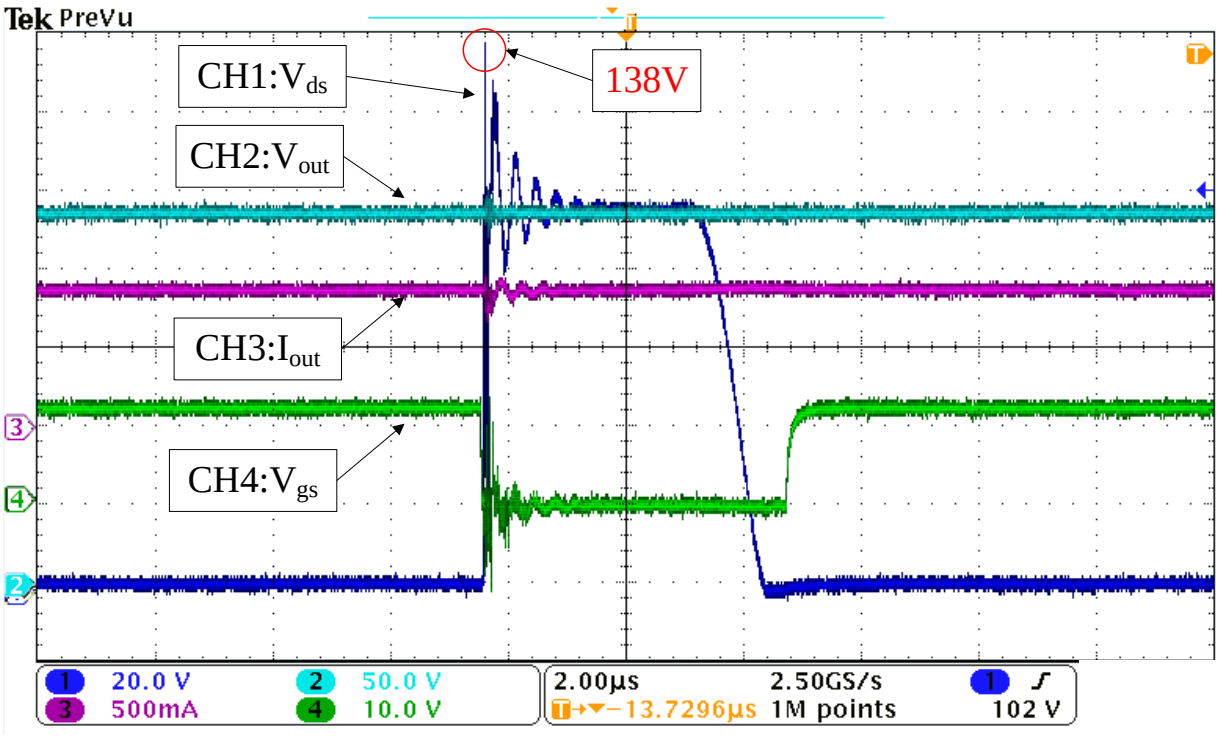


Figure 2.24 Measured waveforms of the BMFFC without LC snubber circuit at 200W with 25V

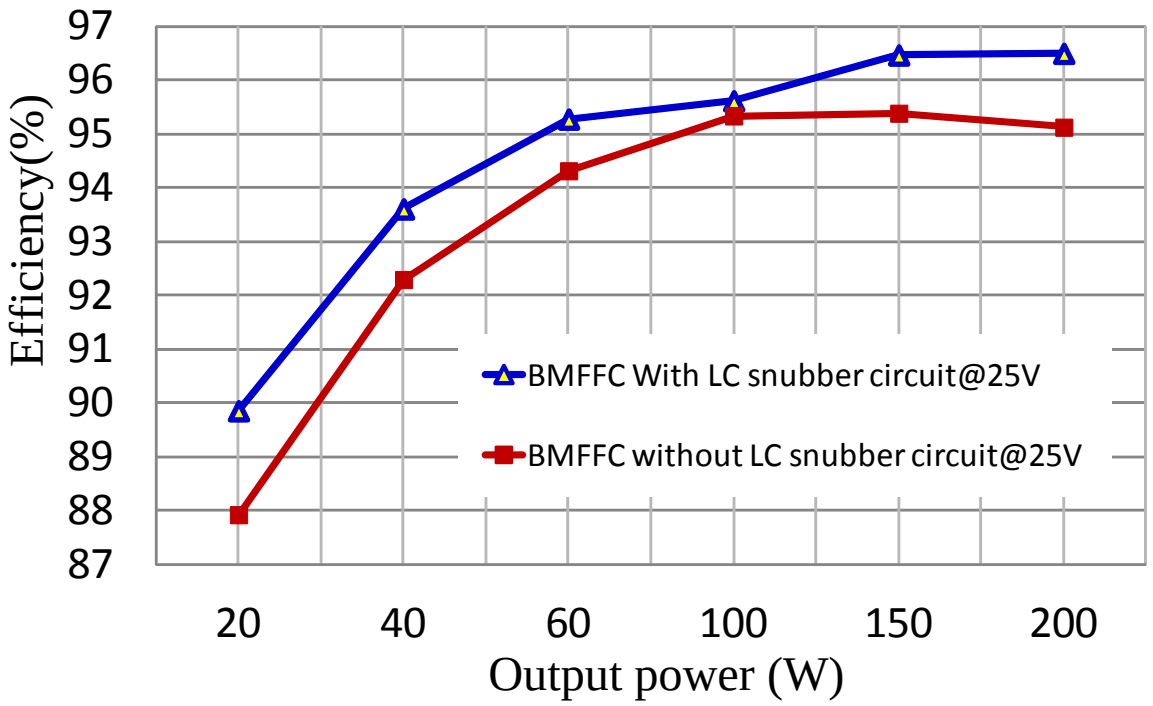


Figure 2.25 Efficiency comparison (with/without snubber circuit) with different output power at 25V input

In order to see the superior performance of BMFFC, a conventional quasi-resonant flyback converter (QRFC) with the same MOSFET and diode was built for comparison purposes. Since the RM14 core can't deliver 200W at 50KHz and 25V input in the QRFC topology, a larger PQ40 core was selected for comparison with the BMFFC. Leakage inductance greatly impacts the conversion efficiency for flyback converter so an interleaved winding technique was employed as shown in Figure 2.26, where the main primary winding is paralleled, and the secondary winding is in series . This resulted in approximately 12nH of primary leakage inductance. The primary peak current is 27A at 25V input and 200W output. A conventional RCD snubber circuit was employed to suppress the MOSFET drain voltage spike. Using [36], the parameters of RCD circuit are R=1K, C=4.7nF, and MUR460. Figure 2.27 shows the

efficiency with varying output power of the BMFFC and conventional QRFC at 35V input. The efficiency of BMFFC and QRFC at 35V input is measured with different output power, respectively. As seen in Figure 2.27, the peak efficiency of the BMFFC at 35V is 1.77 percent points higher than QRFC with the same power level. In addition, the CEC (California Energy Commission) weighted efficiency is also plotted in Figure 2.28 at different input voltage because CEC efficiency is widely accepted as a key index to evaluate the performance of micro-inverter [44]. The BMFFC CEC efficiency with varying input voltage is obviously 1-1.5 percent points higher than QRFC, even though a larger PQ40 core is used for the QRFC.

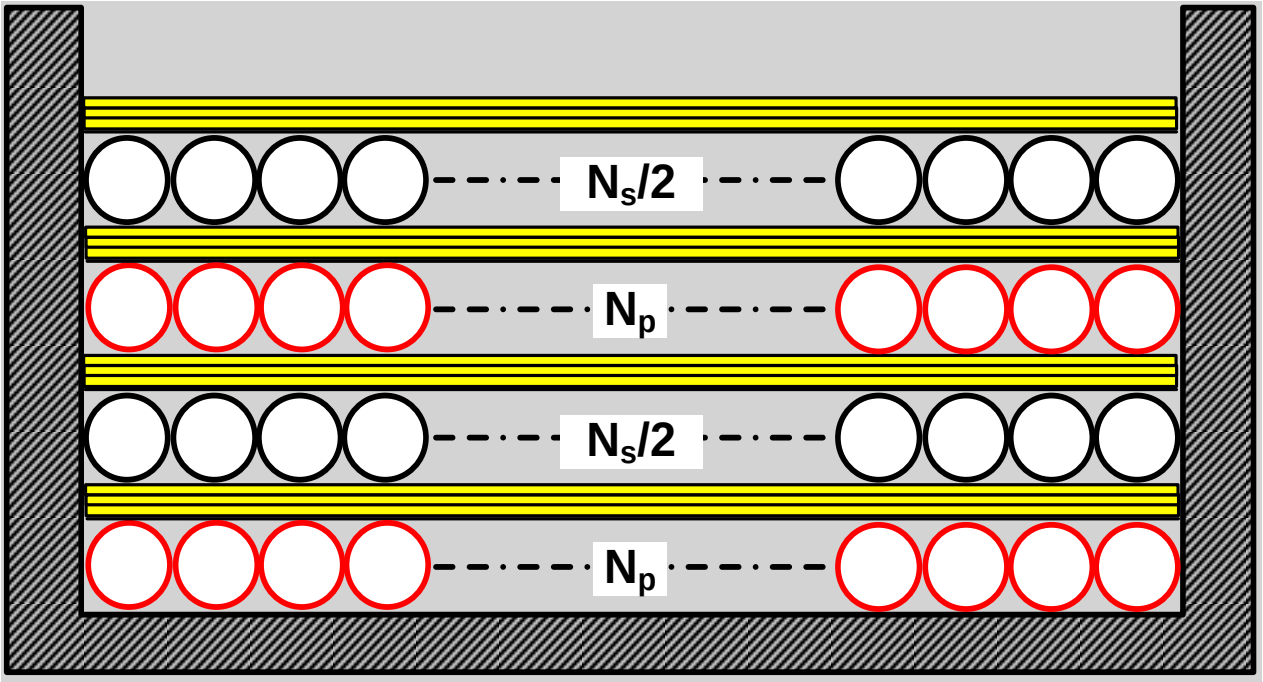


Figure 2.26 Transformer construction of QRFC (Np=6 Parallel in primary, Ns=36 series connection in secondary)

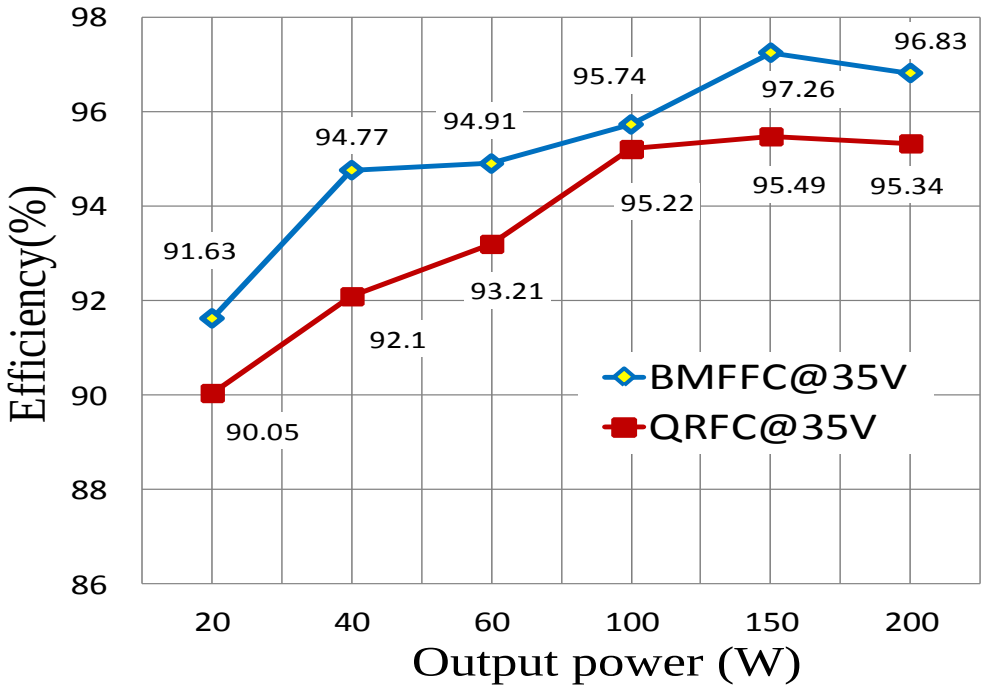


Figure 2.27 Efficiency comparison with different output power between BMFFC and QRFC at 35V

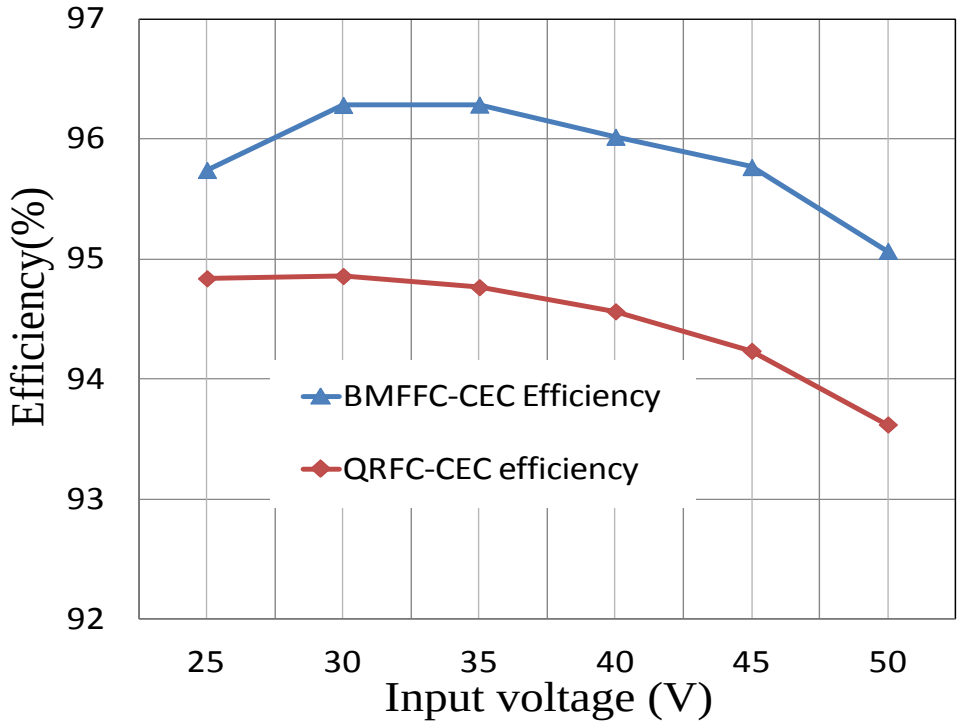


Figure 2.28 BMFFC CEC weight efficiency comparison with QRFC

2.7 Summary

A Forward-Flyback converter with boundary mode operation to achieve ZVS has been proposed in this chapter 2. To further improve the efficiency through reducing turning-off losses, an active LC snubber is employed to suppress the voltage spike across the primary MOSFET switch and to recycle energy stored in the transformer leakage inductance. The operation of the converter is analyzed and a detailed design procedure is given to facilitate optimal design of the converter. A 200W BMFFC prototype was built and tested. The measured maximum efficiency reached 97.2%. The experimental results demonstrating better efficiency of the BMFFC over full range operation not only validate the operation of the converter but also confirm the superiority of the BMFFC over the conventional Forward-Flyback converter for low power applications.

CHAPTER THREE: DC-AC STAGE CONVERTER

3.1 Introduction

For the three-phase DC/AC converter in the second stage, a variety of active soft switching topologies have been proposed in last three decades [45]-[58]. Most of them can be divided into three groups: auxiliary resonant commutated pole (ARCP) group [47]-[50], resonant DC-link inverter (RDCLI) group [51]-[56], and resonant AC-link converter (RACLC) [57] [58]. The ARCP can be applied broadly for the voltage-source-type single-phase or three-phase inverters but it requires a large number of auxiliary components. Compared to the ARCP, the RDCLI has the advantages of fewer auxiliary switches and a simpler circuit. Several soft switching topologies in [55]-[57] were proposed to achieve the minimum number of extra components. However, the driving signals of the auxiliary switches are very sensitive to the noise from the main circuit. Since the RACLC can achieve voltage boosting and electrical isolation at the same time, it is highly preferred for renewable energy power generation. Unfortunately, the control circuit for the RACLC is complex and bi-directional switches are required. In fact, auxiliary components are unavoidable for all of the soft switching topologies mentioned above.

The proposed soft switching technique shown in Figure 3.1 simplifies the inverter topology and reduces the cost since it does not require any auxiliary components. The body capacitors of the main MOSFETs and the output inductor L_1 are combined to form a resonant circuit. The inductor current is intentionally bi-directional within a switching cycle to generate ZVS conditions during commutation. Meanwhile the average inductor current is controlled to produce a sinusoidal current in L_1. The proposed soft switching technique is suitable for MIC applications where the

switching losses are usually dominant. Based on the above, Figure 3.1 shows the proposed high efficiency MIC architecture with both-stage zero voltage switching consisting of a full bridge LLC resonant dc-dc step up converter and three phase four-wire soft switching dc-ac converter. The detail operating modes in the three-phase four-wire DC/AC converter will be presented in the following sections.

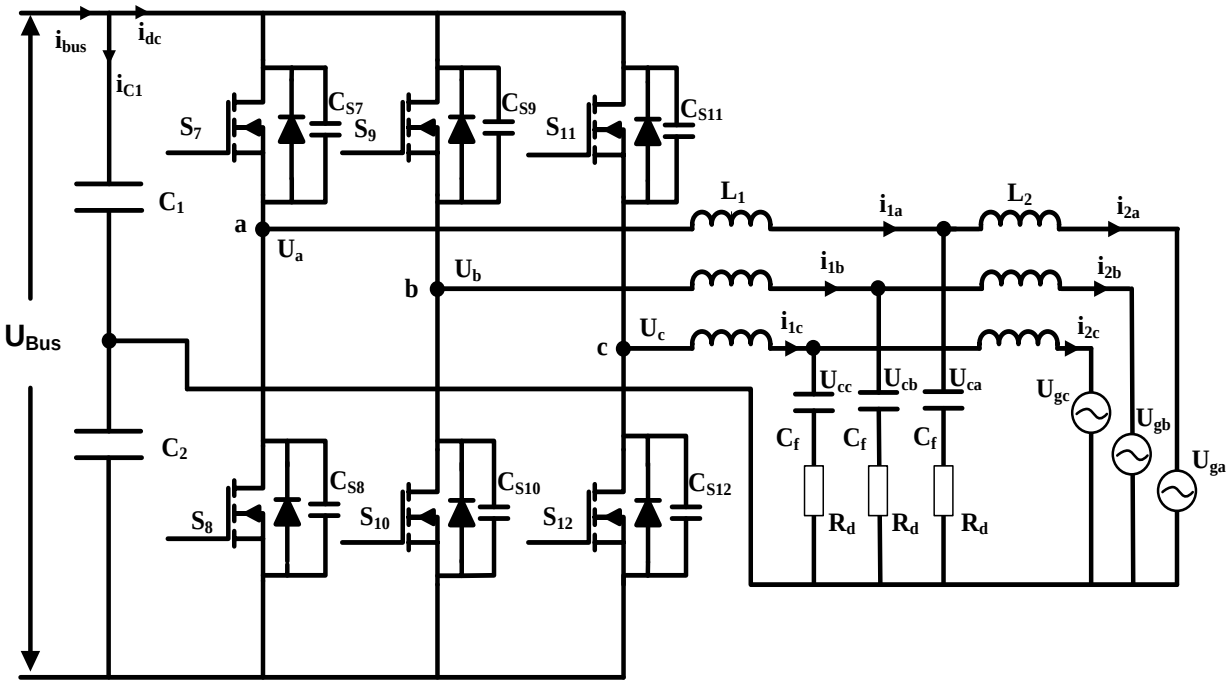


Figure 3.1 Three-phase four-wire DC/AC grid-connected converter

3.2 Operation principle

The operating modes of the proposed ZVS three-phase four-wire DC/AC converter are presented in this section. As shown in Figure 3.1, the three phases of the DC/AC second stage are

symmetrical around the neutral point therefore the analysis can be performed on a single phase as shown in Figure 3.2 and described below.

Interval 1 [t_0-t_1] Prior to t_0, S_7 is off and S_8 is still turned on. Assume that the current direction through L_1, as shown in Figure 3.2, is already from right to left at t_0. Then S_8 is turned off and the voltage across the parasitic capacitor C_{S8} of low side MOSFET S_8 starts increasing due to the inductor current. As C_{S8} charges; the voltage across S_7 decreases. This interval ends once the voltage across S_7 reaches zero.

Interval 2 [t_1-t_2] The body diode of S_7 will be conducting at t_1 and S_7 can be turned on with ZVS. The current flow decays linearly from right to left due to the fact that $U_{bus}/2$ minus the voltage across L_1. This mode ends when the inductor current decays to zero.

Interval 3 [t_2-t_3] S_7 is conducting and the current direction through L_1 is now changed from left to right and increasing linearly. This is the power delivery interval.

Interval 4 [t_3-t_4] At t_3, S_7 is turned off and its parasitic capacitor C_{S7} is charged by the inductor current while C_{S8} is discharging. Once the voltage across C_{S8} drops to zero, the parasitic body diode of MOSFET S_8 conducts since the current direction through L_1 does not change.

Interval 5 [t_4-t_5] Continuing from the previous interval 4, the body diode of S_8 continues conducting which creates a ZVS condition when S_8 is turned on. The length of this interval is typically quite short and ends once S_8 is turned on.

Interval 6 [t_5-t_6] S_8 is turned on under ZVS condition at t_5. The current through S_8 is gradually decreasing due to the fact that $U_{bus}/2$ plus the output voltage appears across the inductor L_1. During this interval the energy stored in the inductor is transferred to the load and the current

that was flowing in the body diode of S_8 now flows through the MOSFET on resistance thus reducing conduction losses.

Interval 7 [t_6-t_0] The current through S_8 continues to flow and the current direction will change once the current decays to zero at t_6. Once the current through S_8 changes direction from top to bottom as shown in Figure 3.2, a ZVS condition is created for S_7. When the current through S_8 reaches

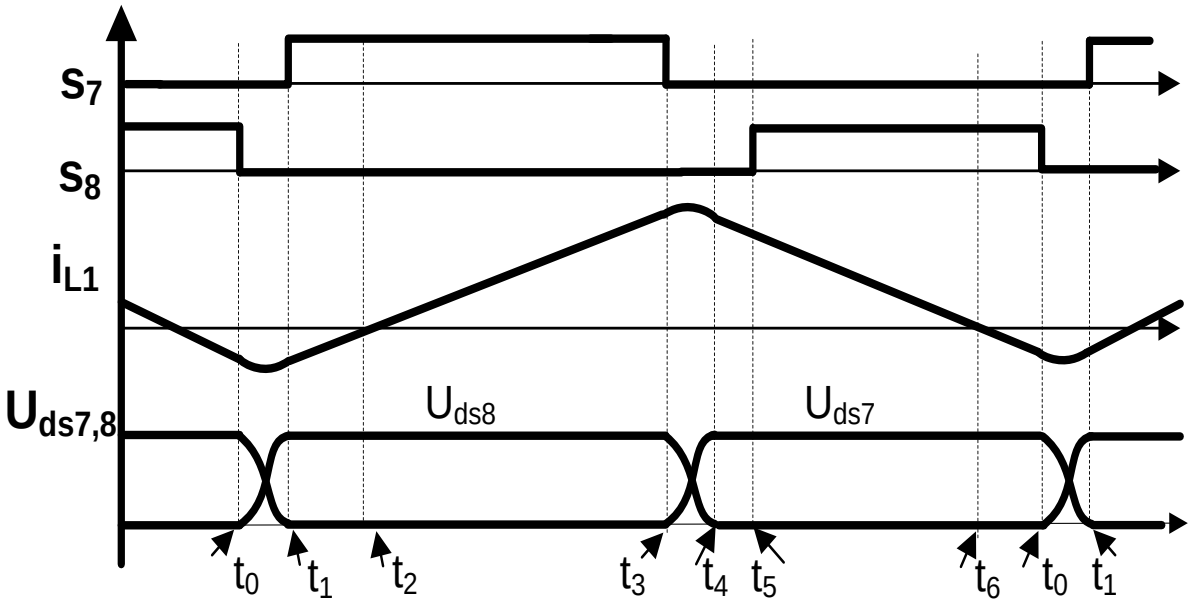


Figure 3.2 Theoretic Waveforms and Operating Intervals of a Single Phase DC/AC Converter

3.3 Modeling of three-phase four-wire grid-connected inverter

The schematic of a three-phase four-wire voltage source inverter (VSI) connected to the grid through an LCL filter is shown in Figure 3.1 The series resistances of the inductors (L_1&L_2) have been neglected in order to simplify the derivation of average model. An average model of three-phase four-wire inverter may be obtained by neglecting the high frequency components of both

the dc voltage and the ac phase currents. According to the Kirchhoff's current & voltage law, differential equations to illustrate current and voltage as shown in Figure 3.1 can be expressed by:

$$\dot{I}_1 = -\frac{R_d}{L_1} I_1 + \frac{R_d}{L_1} I_2 - \frac{1}{L_1} U_{cf} + \frac{U_{bus}}{L_1} D - \frac{U_{bus}}{2 \cdot L_1} \Gamma \tag{3.1}$$

$$\dot{I}_2 = \frac{R_d}{L_2} I_1 - \frac{R_d}{L_2} I_2 + \frac{1}{L_2} U_{cf} - \frac{1}{L_2} U_g \tag{3.2}$$

$$\dot{U}_{cf} = \frac{1}{C_f} I_1 - \frac{1}{C_f} I_2 \tag{3.3}$$

$$\dot{U}_{Bus} = \frac{i_{bus} - i_{dc}}{\frac{C_1}{2}} = \frac{2}{C_1} i_{bus} - \frac{2}{C_1} D^T I_1 \tag{3.4}$$

Where, $I_1 = [i_{1a} \ i_{1b} \ i_{1c}]^T$ $I_2 = [i_{2a} \ i_{2b} \ i_{2c}]^T$ $U_{cf} = [U_{ca} \ U_{cb} \ U_{cc}]^T$

$U_g = [U_{ga} \ U_{gb} \ U_{gc}]^T$ D=$[d_a \ d_b \ d_c]$ $\Gamma = [1 \ 1 \ 1]^T$

In the steady state, the grid phase currents i_{2a}, i_{2b}, and i_{2c} are controlled to be sinusoidal and in phase with the corresponding grid phase voltages U_{ga},U_{gb} and U_{gc} which can be expressed as:

$$\begin{bmatrix} U_{ga} \\ U_{gb} \\ U_{gc} \end{bmatrix} = \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ U_m \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.5}$$

Where U_m and ω are the amplitude of the phase voltage and angular frequency of the power source, respectively. The model in the stationary coordinates can be transformed into a synchronous reference (dq) frame by the transformation matrix T (Park's transformation) as follows:

$$T = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (3.6)$$

After transformation into the synchronous three-phase reference frame, the equations of the whole averaged model are expressed by (3.7)-(3.10) [59].

$$\dot{I}_{1dq} = -WI_{1dq} - \frac{R_d}{L_1} I_{1dq} + \frac{R_d}{L_1} I_{2dq} - \frac{1}{L_1} U_{cfdq} + \frac{1}{L_1} U_{dq} \quad (3.7)$$

$$\dot{I}_{2dq} = \frac{R_d}{L_2} I_{1dq} - WI_{2dq} - \frac{R_d}{L_2} I_{2dq} + \frac{1}{L_1} U_{cfdq} - \frac{1}{L_2} U_{gdq} \quad (3.8)$$

$$\dot{U}_{cfdq} = \omega U_{cfdq} + \frac{1}{C_f}(i_{1dq} - i_{2dq}) \quad (3.9)$$

Where $W = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$, $U_{dq} = U_{Bus} D_{dq}$

3.4 Small signal model

The small signal model can be obtained by using perturbation to the average model around the DC operating point, as shown in (3.10), X and $\hat{x}$ denote the DC operating point and the small signal perturbation, respectively.

$$x = X + \hat{x} \quad (3.10)$$

From (3.7) to (3.9), combing with the small signal perturbation (3.10), the mathematical model can be represented by a small signal mode of the form in linear time invariant state space.

$$\begin{cases} \dot{x}(t) = A \cdot x(t) + B \cdot u(t) + F \cdot \delta(t) \\ Y(t) = C \cdot x(t) + D \cdot u(t) \end{cases} \tag{3.11}$$

Where

$$x = \begin{bmatrix} \hat{I}_{1d} & \hat{I}_{1q} & \hat{I}_{2d} & \hat{I}_{2q} & \hat{u}_{cfd} & \hat{u}_{cfq} \end{bmatrix}^T$$

$$u = [\hat{u}_{dg} \quad \hat{u}_{dq}]^T$$

$$\delta = [\hat{u}_{gd} \quad \hat{u}_{gq}]^T$$

X is the normalized state vector selected as $\hat{I}_{1d}, \hat{I}_{1q}, \hat{I}_{2d}, \hat{I}_{2q}, \hat{U}_{cfd}, \hat{U}_{cfq}$, U is the normalized inverter output voltage, δ is the normalized grid voltage, and Y is the normalized injected grid current in the d-q reference frame. A, B, C, D and F are matrices with appropriate dimensions given in below.

$$A = \begin{bmatrix} -\frac{R_d}{L_1} & \omega & \frac{R_d}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ -\omega & -\frac{R_d}{L_1} & 0 & \frac{R_d}{L_1} & 0 & -\frac{1}{L_1} \\ \frac{R_d}{L_2} & 0 & -\frac{R_d}{L_2} & \omega & \frac{1}{L_2} & 0 \\ 0 & \frac{R_d}{L_2} & -\omega & -\frac{R_d}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & -\omega \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad \delta = \begin{bmatrix} 0 & 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} & 0 & 0 \end{bmatrix}^T$$

$$C = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}^T \quad D=0$$

Following the above procedure, the small signal equivalent circuit of the three-phase four-wire inverter with LCL filter is shown in Figure 3.3.

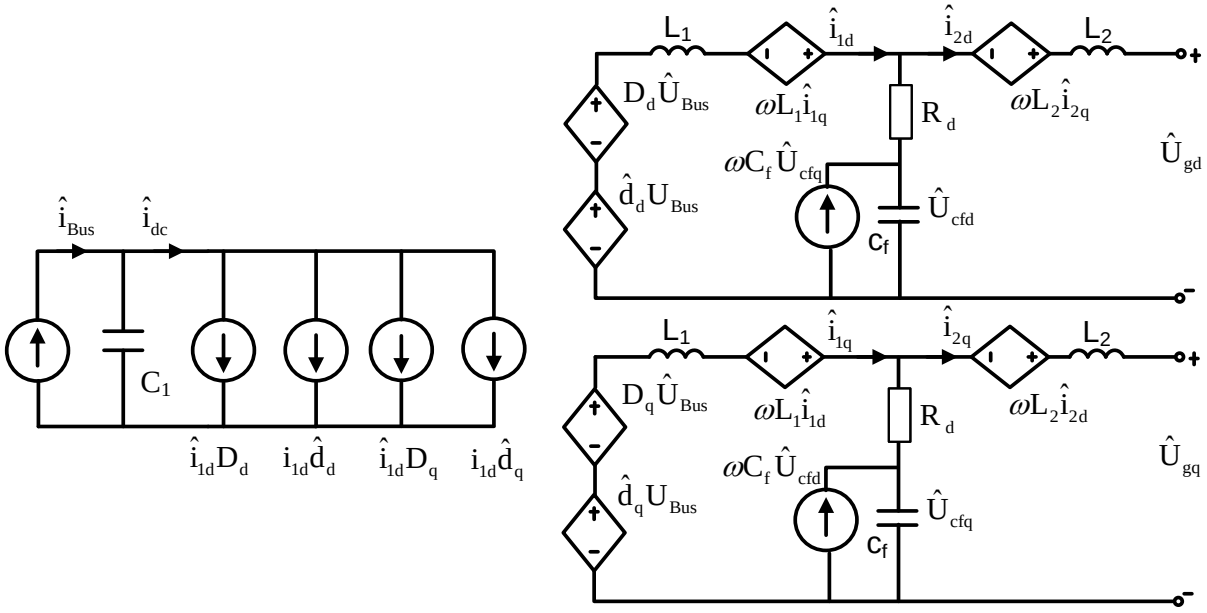


Figure 3.3 Equivalent circuit based on small signal modeling

CHAPTER FOUR: CONTROL DESIGN OF DC/AC STAGE

An overall control diagram for two-stage three-phase four-wire MIC PV system is shown in Figure 4.1. The voltage (U_{pv}) and current (I_{pv}) of PV panel are both sensed continuously to calculate the instantaneous power. The MPPT algorithm is based on variation of the instantaneous power of PV panel that changes the switching frequency of the LLC resonant DC-DC converter to track the maximum power output. In order to keep power balanced between the generator (PV panel) and the grid for two-stage MIC system, a bus voltage regulator is used to keep the voltage constant. The Bus voltage is regulated by controlling the amount of current injected into the grid. For example, if the irradiance is increasing, the bus voltage increases because the DC-DC stage is running with MPPT. When U_{Bus} is greater than U^*_{Bus}, the output value of the DC link regulator (I_d^*) increases and the inverter stage injects more current into the grid. Conversely, if the irradiance is decreasing, the inverter stage reduces the amount of current injected into the grid. Low THD is achieved by sensing the injected grid current via d/q transformation and causing it to follow the reference current I_d^*. If the power factor is assumed to be unity, the reactive current will be zero after d/q transformation (no phase shift). As described in section III, the bidirectional current through the high frequency inductor (L_1) is also sensed as a part of the internal current loop to achieve ZVS and improve the dynamic response of DC/AC stage. This will be discussed in more detail in Section V which follows.

According to the overall control diagram as shown in Figure 4.1, a MPPT CPI (center point iteration) algorithm is employed in the first stage, a more detailed description referring to this paper [60]. Step by step triple-loop controller design for the inverter stage is presented in this section followed by small signal modeling of the power stage. Due to the unity power factor

requirement for injected grid current, a control block diagram of the multi-loop controller in the d-axis as shown in Figure 4.2 will be presented. It can be seen that the inverter side inductor current is controlled by the VFBCMC in the inner current loop which improves dynamic response in the whole system. Followed by the inner current loop, grid current i_{2d} is also sensed to track the reference i_{2dref} by the PI controller $G_c(s)$. The detailed controller design of $G_c(s)$ will be described below. Because the first stage is used for tracking the maximum power of the PV panel, a bus voltage controller $G_v(s)$ of the outer control loop is employed in inverter stage to keep the bus voltage constant.

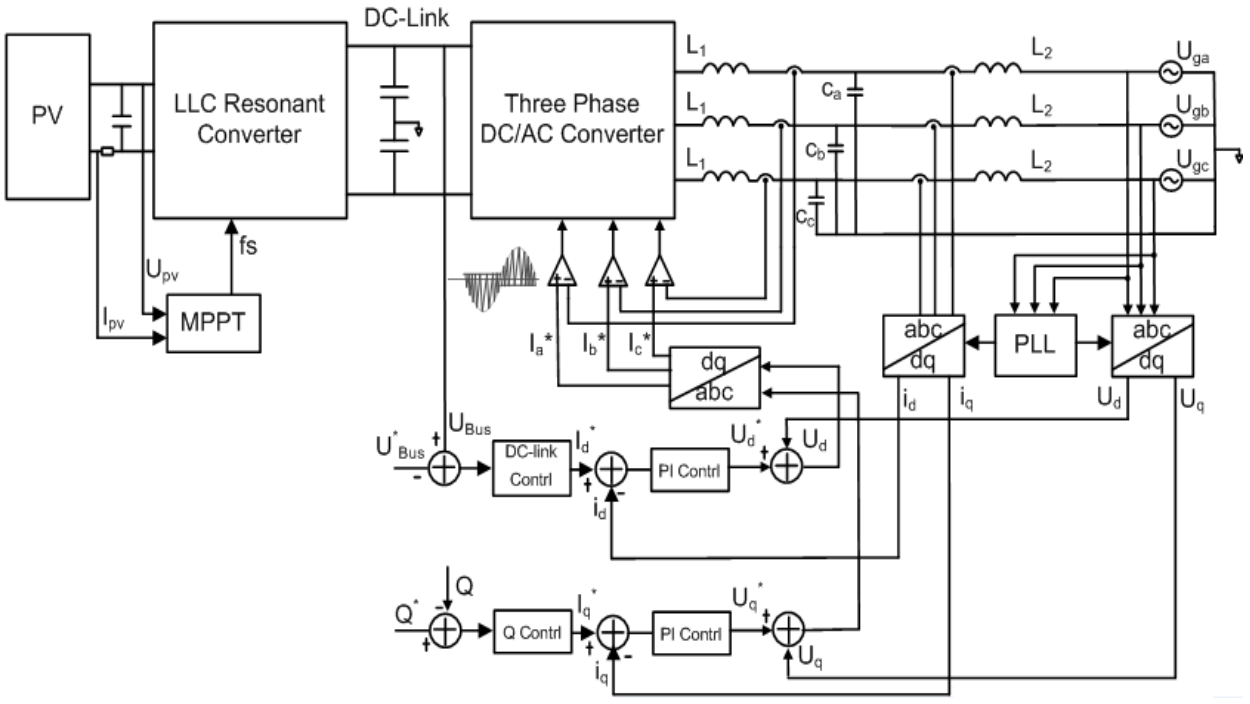


Figure 4.1 Overall control diagram of a two stage three-phase grid-tie inverter system

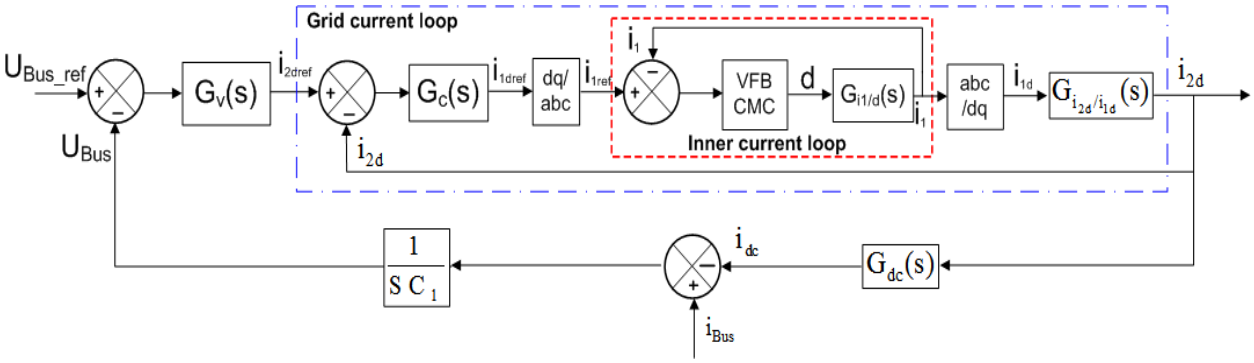


Figure 4.2 Diagram of triple-loop control in d-axis

4.1 Inner current loop control of the inverter side inductor

4.1.1 Implementation of the VFBCMC

ZVS in the inverter stage is achieved through bidirectional control of the inductor current in every switching cycle, as shown in Qian's paper [61]. Thus, VFBCMC is proposed to control the inductor L_1 current of the inverter side, and the current envelope of L_1 is followed with upper limit and lower limit as shown in Figure 4.3.

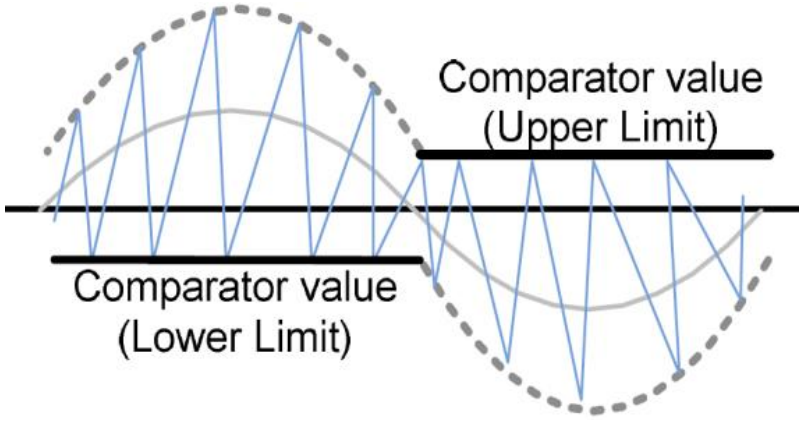


Figure 4.3 VFBCM of high frequency inductor L1

It can be seen from Figure 4.3, turn-on time is defined as the time required to keep the upper switch ON and make the inductor current traverse from the lower limit to the upper limit. The lower limit and the upper limit are determined by equation (4.1) and (4.2) according to the polarity of grid voltage. T-on is calculated according to the equation (4.3). Turn-off time is defined as the required time which lower switch should stay ON to make the inductor current traverse from the upper limit (i_{1ref}) to the lower limit. T-off is calculated according to equation (4.4). The switching frequency is derived using the T-on and T-off expressions according to equation (4.5).

$$\begin{cases} i_{1ref} = 2\sqrt{2} * I_m * \sin(\omega t) + B_0; \ if \ \sin(\omega t) > 0 \\ i_{lower} = -B_0 \end{cases} \tag{4.1}$$

$$\begin{cases} i_{1ref} = B_0; & \text{if } \sin(\omega t) < 0 \\ i_{lower} = 2\sqrt{2} * I_m * \sin(\omega t) - B_0 \end{cases} \tag{4.2}$$

Where,

I_m: output RMS current of three-phase inverter stage

B_0 is a comparator value at lower limit or upper limit as shown in Figure 4.3.

$$t_{on} = L_1 \frac{i_{1ref} - i_{lower}}{\frac{1}{2}U_{Bus} - U_m} \tag{4.3}$$

$$t_{off} = L_1 \frac{i_{1ref} - i_{lower}}{\frac{1}{2}U_{Bus} + U_m} \tag{4.4}$$

$$f_s = \frac{(\frac{U_{Bus}}{2})^2 - {U_m}^2}{L_1 \cdot U_{Bus} \cdot (i_{1ref} - i_{lower})} \tag{4.5}$$

Generally, efficiency is closely related to switching frequency. Based on the parameters shown in table II, the switching frequency versus output power during a line period is plotted in Figure 4.4 at CEC (California energy commission) weighted power levels [44]. The switching frequency range at rated output power (400W) is from 20 kHz to 185 kHz. The switching frequency range is only 45 kHz to 185 kHz even at 10% rated output power (40W). Experimental results in Section VIII verify the range of the switching frequency that is reasonable.

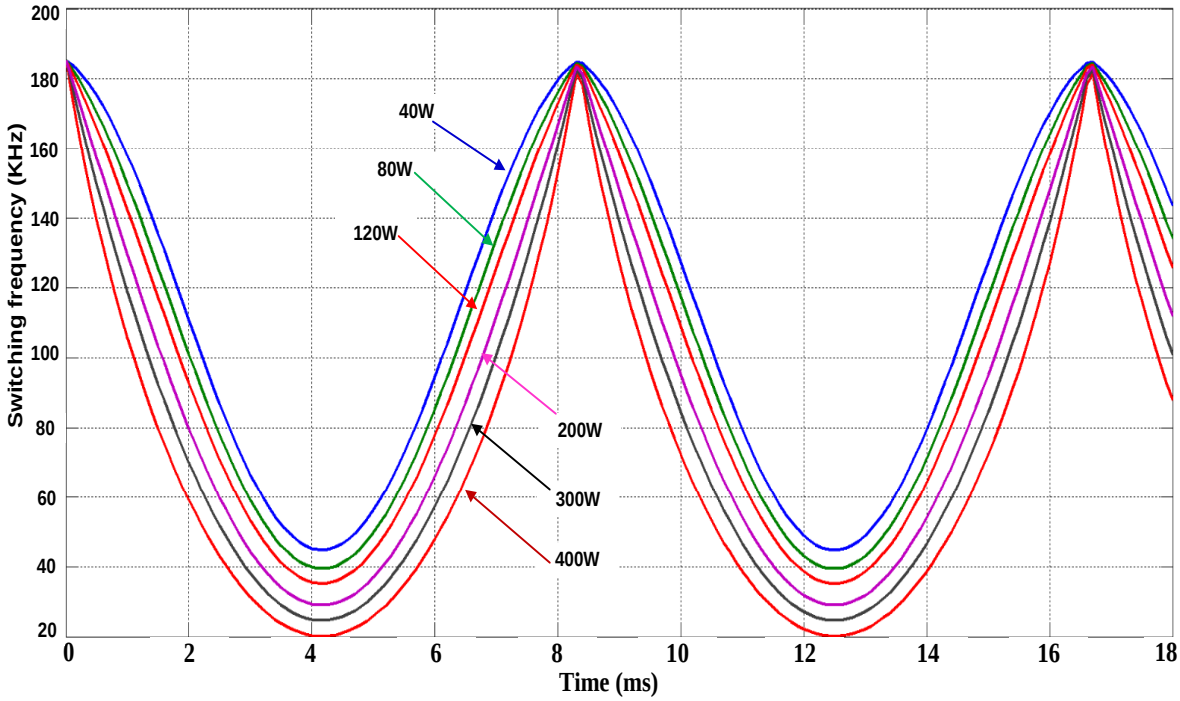


Figure 4.4 Switching frequency versus load range variation at a line period of output current

4.1.2 Small signal modeling of the VFBCMC for one phase of the half bridge inverter

From (4.5), switching frequency is variable at a line frequency with the variation of i_{upper} i_{lower} U_m. Because the duty cycle is nonlinear to control the inductor current in the variable switching frequency converter, there have been some limitations in the application of state space averaging techniques. In order to design the current loop of the inverter side inductor, referring to papers [62-66], the development of the small signal model of VFBCMC for a half bridge inverter and the derivation of the transfer function are presented in this section.

The half bridge inverter is modeled with an averaged circuit model [62] [63], which uses the PWM switch model. Since the neutral wire of three-phase four wire inverter is present as shown in Figure 3.1, each phase of the inverter is considered to be identical. One phase (as shown in Figure 4.5) of the three phase four wire topology is discussed in this segment. The following assumptions have been made in order to simplify analysis: 1) the parasitic resistance of L_1 and C_f is neglected 2) the effect in the grid side inductor L_2 will not be considered 3) the impedance of the grid is replaced by an ideal resistance R_g 4) the DC-link capacitance is large enough to regard U_{Bus} as an ideal voltage source 5) MOSFETs are assumed to be ideal switches.

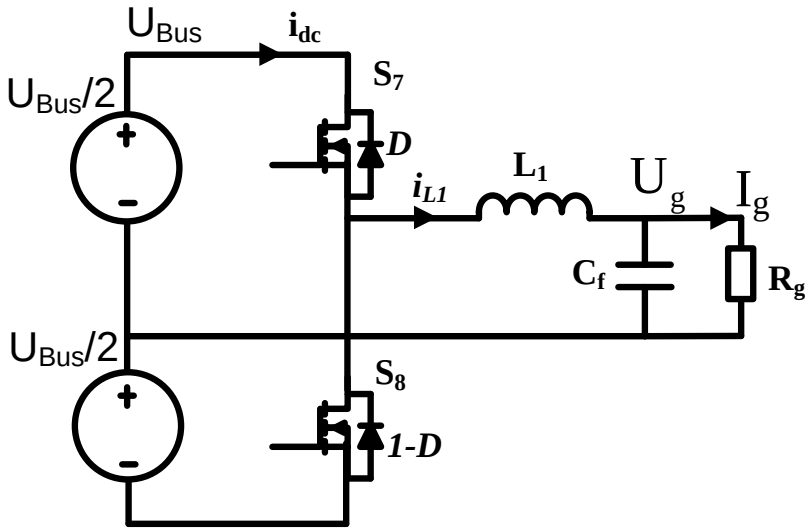


Figure 4.5 Half bridge topology of one inverter phase

The relationship among the input voltage (U_{bus}), output voltage U_g and the switch duty cycle D can be derived according to Figure 4.5, since in steady state the time integral of the inductor voltage over one time period (Ts) must be zero,

$$\left[\frac{1}{2}U_{Bus} - U_g\right] \cdot D \cdot T_s - \left[\frac{1}{2}U_{Bus} + U_g\right] \cdot (1 - D) \cdot T_s = 0 \tag{4.6}$$

Hence, steady dc voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$U_g = U_{Bus} \cdot (D - 0.5) \tag{4.7}$$

Assuming a lossless circuit, input power (U_{Bus}*i_{dc}) equals to output power (U_g*i_g) and the average current through L_1 (i_{L1}) is also equal to I_g.

$$U_{Bus} i_{dc} = U_g i_{L1} \tag{4.8}$$

Substitute (4.7) into (4.8),

$$i_{dc} = (D - 0.5)i_{L1} \tag{4.9}$$

By using perturbation to the average model around the DC operating point in (4.7) and (4.9), the small signal model of the PWM switch for one inverter phase can be obtained as (4.10) after neglecting second-order terms.

$$\begin{cases} \hat{u}_g = \left(U_{Bus}\frac{\hat{d}}{D-0.5} + \hat{u}_{Bus}\right)(D - 0.5) \\ \hat{\imath}_{dc} = I_{L1}\hat{d} + \hat{\imath}_{L1}(D - 0.5) \end{cases} \tag{4.10}$$

Where $\hat{d}, \hat{u}_{Bus}, \hat{\imath}_{L1}$ are the small signal variable of D, U_{Bus} and i_{L1}, respectively.

These two switches can be combined into one network with three terminals a, p and c [62] [63], which stands for active, passive, and common, respectively. Using the linear equivalent circuit, the small signal model of the PWM switch for one phase of the inverter is shown in Figure 4.6. Input signals of the power stage are the input voltage and duty cycle, while output signals are the inductor current and voltage.

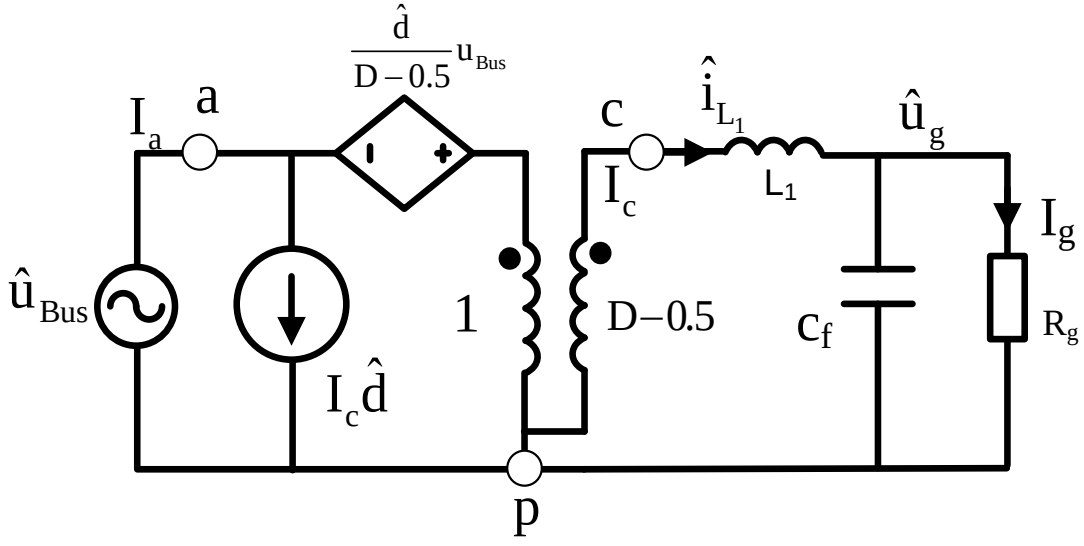


Figure 4.6 The equivalent circuit based on switch model for one inverter phase

The transfer function from duty cycle to inductor current can be expressed and further simplified as (4.11) while the impedance of the grid Rg is equal to zero at the ideal condition.

$$G_{i_{L1}/d}(s) = \frac{\hat{\imath}_{L1}(s)}{\hat{d}(s)}\Big|_{\substack{\hat{u}_g(s)=0 \\ \hat{u}_{bus}(s)=0}} = \frac{u_{Bus}}{R_g}\frac{1+sR_gC}{s^2L_1C+s\frac{L_1}{R_g}+1} \approx \frac{u_{Bus}}{sL_1} \tag{4.11}$$

Figure 4.7 shows the bidirectional inductor current waveform during a switching cycle. H is the difference between the upper trip point (i_{1ref}) and lower trip point ($-B_0$) of the PWM generator. A linearization of on-time (t_{on}) and switching period t_s is introduced to replace duty-ratio d as input variables.

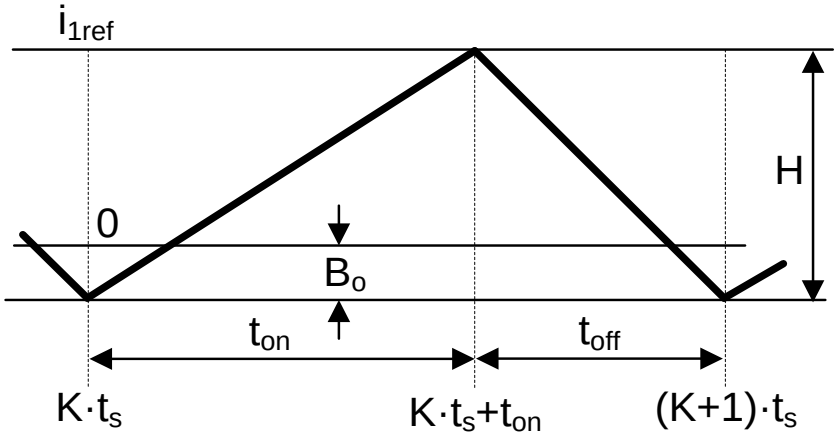


Figure 4.7 The extended instantaneous inductor current waveform

The off time constraint is determined as follows according to Figure 4.7:

$$t_s = t_{on} + t_{off} = t_{on} + L_1\frac{H}{u_g+\frac{1}{2}u_{Bus}} \tag{4.12}$$

With (4.12) small signal perturbed, the detail derivation procedure for the small signal model of the VFBCMC is shown in this segment. The relationship between the duty cycle, on time and

switching period is represented by (4.13) based on the perturbed and linearized small signal model [32-34],

$$\begin{cases} \hat{d} = \frac{\hat{t}_{on} - D \cdot \hat{t}_s}{T_s} \\ \hat{t}_s = \hat{t}_{on} + \hat{t}_{off} \end{cases} \tag{4.13}$$

And,

$$\hat{t}_{off} = \frac{2L_1}{u_g + \frac{1}{2}u_{Bus}} \hat{\imath}_{L1} - \frac{2L_1 \cdot i_{L1}}{\left(u_g + \frac{1}{2}u_{Bus}\right)^2} \left(\hat{u}_g + \frac{1}{2}\hat{u}_{Bus}\right) \hat{V}_o \tag{4.14}$$

Substituting (4.14) into (4.13) and simplifying, we get (4.15),

$$\hat{d} = \frac{\hat{t}_{on}(1-D)}{T_s} - \frac{2DL_1}{\left(u_g + \frac{1}{2}u_{Bus}\right)T_s} \hat{\imath}_{L1} + \frac{2DL_1 i_{L1}}{\left(u_g + \frac{1}{2}u_{Bus}\right)^2 T_s} \hat{u}_g + \frac{DL_1 i_{L1}}{\left(u_g + \frac{1}{2}u_{Bus}\right)^2 T_s} \hat{u}_{Bus} \tag{4.15}$$

From on-time constraints, the relationship between peak current and average current is derived as (4.16)

$$i_p = i_{L1} + \left(\frac{1}{2}u_{Bus} - u_g\right) \frac{t_{on}}{2L_1} \tag{4.16}$$

In order to remove $\hat{\mathrm{t}}_{\mathrm{on}}$ in (4.15), linearize (4.16)

$$\hat{t}_{on} = \frac{2L_1}{\frac{1}{2}U_{Bus} - U_g} \left(\hat{\imath}_p - \hat{\imath}_{L1}\right) - \frac{DT_s}{\frac{1}{2}U_{Bus} - U_g} \left(\frac{1}{2}\widehat{U}_{Bus} - \widehat{U}_g\right) \tag{4.17}$$

Substitution of equation (4.17) into (4.15) leads to,

$$\hat{d} = \frac{2(1-D)L_1}{\left(\frac{1}{2}u_{Bus}-u_g\right)T_s}\hat{\imath}_p - \left[\frac{2(1-D)L_1}{\left(\frac{1}{2}u_{Bus}-u_g\right)T_s} + \frac{2DL_1}{\left(\frac{1}{2}u_{Bus}+u_g\right)T_s}\right]\hat{\imath}_L + \left[\frac{DL_1 i_{L1}}{\left(u_g+\frac{1}{2}u_{Bus}\right)^2 T_s} - \frac{D(1-D)}{2\left(\frac{1}{2}u_{Bus}-u_g\right)}\right]\hat{u}_{Bus} +$$

$$\left[\frac{D(1-D)}{2\left(\frac{1}{2}u_{Bus}-u_g\right)} + \frac{2DL_1 i_{L1}}{\left(u_g+\frac{1}{2}u_{Bus}\right)^2 T_s}\right]\hat{u}_g \tag{4.18}$$

And we know the steady state equation (4.19) according to Figure 4.7.

$$\begin{cases} \frac{L_1 i_{L1}}{u_{Bus}T_s} = \frac{\left(\frac{1}{2}u_{Bus}-u_g\right)t_{on}}{u_{Bus}T_s} = \frac{(u_{Bus}-Du_{Bus})D}{u_{Bus}} = (1-D)D \\ \left[\frac{1}{2}u_{Bus}-u_g\right]D = \left[\frac{1}{2}u_{Bus}+u_g\right](1-D) \\ \frac{(1-D)}{\frac{1}{2}u_{Bus}-u_g} = \frac{D}{\frac{1}{2}u_{Bus}+u_g} = \frac{D}{\frac{1}{2}u_{Bus}+\frac{1}{2}u_{Bus}(D-\frac{1}{2})} = \frac{1}{u_{Bus}} \end{cases} \tag{4.19}$$

Substitution of equation (4.19) into (4.18) leads to,

$$\hat{d} = \frac{2L_1}{u_{Bus}T_s R_i}\hat{\imath}_{1ref} - \frac{2L_1}{u_{Bus}T_s R_i}2R_i\hat{\imath}_{L1} + \left[\frac{D(1-D)}{\left(\frac{1}{2}u_{Bus}+u_g\right)}\hat{u}_{Bus} - \frac{D}{2u_{Bus}}\hat{u}_{Bus}\right] + \left[\frac{2D(1-D)}{\left(\frac{1}{2}u_{Bus}+u_g\right)}\hat{u}_g + \right.$$

$$\left.\frac{D}{2u_{Bus}}\hat{u}_g\right] \tag{4.20}$$

Simplify (4.20), we get (4.21):

$$\hat{d} = \frac{2L_1}{u_{Bus}T_s R_i}\left(\hat{\imath}_{1ref} - 2R_i\hat{\imath}_{L1}\right) + \left[\frac{D(1-D)}{\left(\frac{1}{2}u_{Bus}+u_g\right)} - \frac{D}{2u_{Bus}}\right]\hat{u}_{Bus} + \left[\frac{2D(1-D)}{\left(\frac{1}{2}u_{Bus}+u_g\right)} + \frac{D}{2u_{Bus}}\right]\hat{u}_g \tag{4.21}$$

Where

$F_m = \frac{2L_1}{u_{Bus}T_s R_i}$; k=2;$k_c = 1$

In order to reduce the power consumption of the current sensing, a current transformer with the turn's ratio of 1:100 is used to replace conventional resistance sensing in the inverter side inductor. Based on the experimental prototype, the current sensing coefficient (R_i) is selected as 0.6. According to (4.21), a small signal model of one phase inverter with VFBCMC is shown in Figure 4.8.

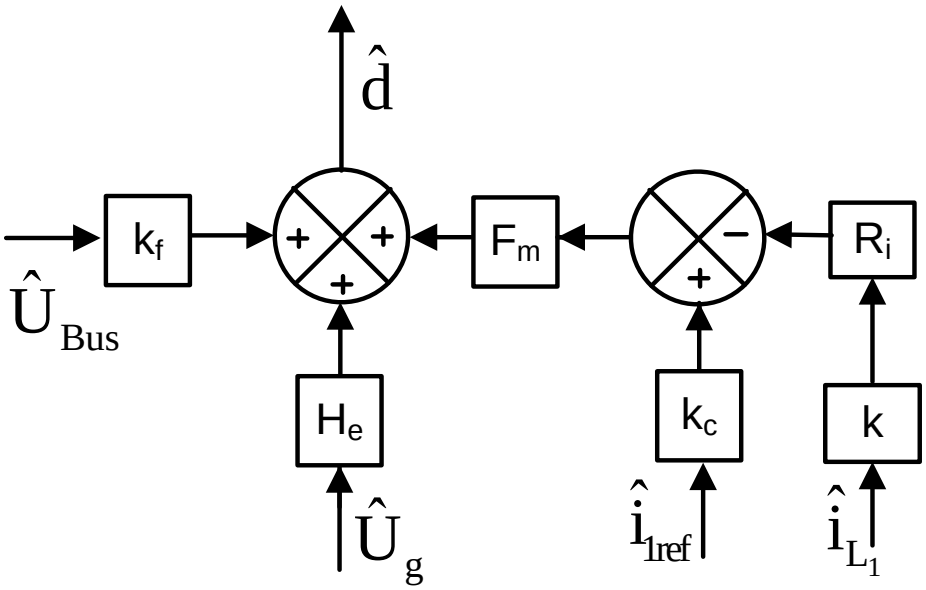


Figure 4.8 A small signal model diagram of the VFBCMC

From (4.21) and Figure 4.8, parameters of each block can be derived as follows:

$$k_f = \frac{\hat{d}}{\hat{u}_{Bus}} = \frac{D(1-D)}{\left(\frac{1}{2}u_{Bus}+u_g\right)} - \frac{D}{2u_{Bus}} \tag{4.22}$$

$$H_e = \frac{\hat{d}}{\hat{u}_g} = \frac{2D(1-D)}{\left(\frac{1}{2}u_{Bus}+u_g\right)} + \frac{D}{2u_{Bus}} \tag{4.23}$$

$$\frac{\hat{d}}{\hat{\imath}_{1ref}} = \frac{2L_1}{u_{Bus}T_s R_i k_c} \tag{4.24}$$

$$\frac{\hat{d}}{\hat{\imath}_{L1}} = \frac{4L_1}{u_{Bus}T_s} \tag{4.25}$$

4.1.3 Complete Model with VFBCMC for one Inverter Phase

By combining the small signal model of the control loop and the equivalent circuit of the power stage based on the previously derived PWM switch model, a complete model of the inner loop control with VFBCMC for one inverter phase can be derived as shown in Figure 4.9.

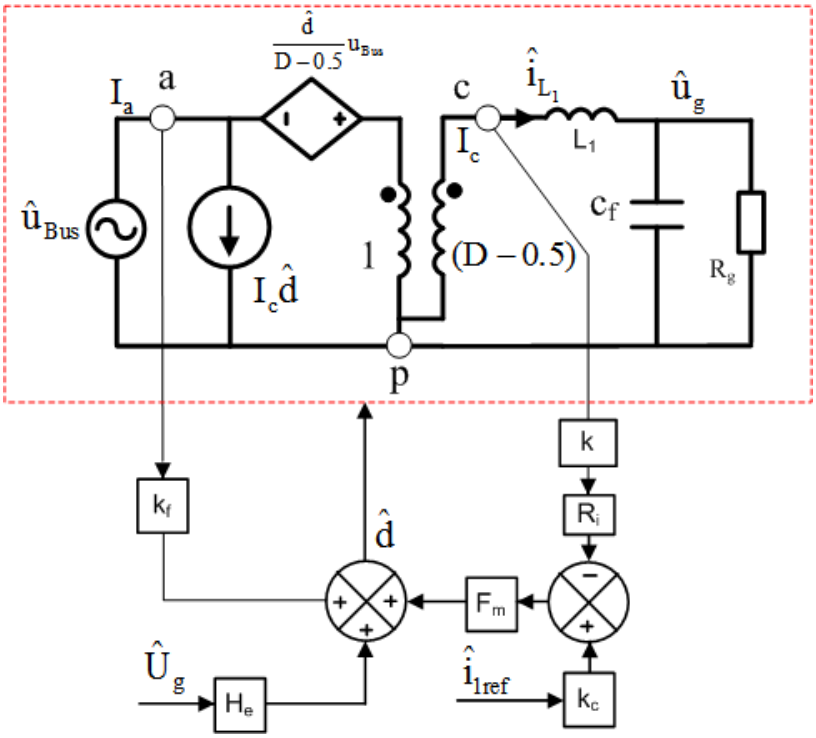


Figure 4.9 The inner current loop diagram of one inverter phase with VFBCMC

From Figure 4.9, the complete model of the inner current loop has three input signals and an output signal. Generally speaking, the purpose of the current loop is to make the inductor current follow the control signal. Without the consideration of the disturbances of $U_{bus}(s)$ and $U_g(s)$, according to (4.21) and Figure 4.9, the inner current loop dc gain of the transfer function $G_{c1}(s)$ from i_{1ref} to i_{L1} is

$$G_{c1}(s) = \frac{i_{L1}(s)}{i_{1ref}(s)} = F_m k_c G_{i_{L1}/_d}(s) \tag{4.26}$$

4.2 Controller design of the grid current loop

In order to achieve high loop gain at the harmonic frequency and improve the stability of the system, a second current control loop is implemented by sensing the injected grid current. If I_q^* is set to zero in the system control diagram of Figure 4.1, unity power factor can be obtained at the grid side. The grid current controller design in the d axis is discussed in this section. Because the inner current control loop can be regarded as a real-time control system, the response of the inner current loop is much faster than that of the grid current loop. The VFBCMC of the inner loop is replaced by $G_{c1}(s)$ as shown in Figure 4.10.

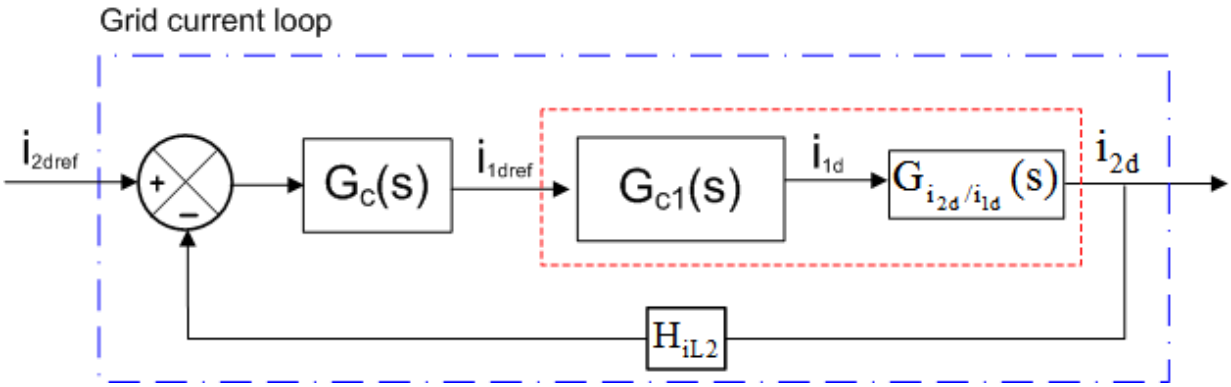


Figure 4.10 The grid current control diagram in d-axis

Ignoring grid disturbances and referring to the equivalent circuit in Figure 3.3, the transfer function $\hat{i}_{2d}(s)/\hat{i}_{1d}(s)$ from the reference of the inductor (L_1) current to the grid side current in d axis can be expressed by

$$G_{\frac{i_{2d}}{i_{1d}}}(s) = \frac{\hat{\imath}_{2d}(s)}{\hat{\imath}_{1d}(s)} = \frac{sR_dC_f+1}{s^2L_2C_f+sR_dC_f+1} \tag{4.27}$$

Figure 4.11 shows the bode plot of the product of $G_{c1}(s)$ and $G_{i2d/i1d}(s)$ in the grid current control loop according to parameters in Table 3. A PI controller is designed to increase the low frequency gain and reduce the steady-state error between the desired and the actual injected grid current. The transfer function of the PI controller is given by

$$G_c(s) = k_p + \frac{k_i}{s} = \frac{k_p s+k_i}{s} \tag{4.28}$$

The loop gain of the grid current loop is

$$T_{oL2} = G_c(s) \cdot G_{c1}(s) \cdot G_{\frac{i_{2d}}{i_{1d}}}(s) H_{iL2}(s) \tag{4.29}$$

Substitution of (4.26), (4.27) and (4.28) into (4.29) leads to

$$T_{oL2} = k_{kc} \frac{a_2s^2+a_1s+a_0}{b_4s^4+b_3s^3+b_2s^2+b_1s+b_0} \tag{4.30}$$

Where

$k_{kc} = H_{iL2};\ b_4 = L_2C_fT_sR_i; b_3 = C_fT_sR_iR_d; b_2 = T_sR_i; b_1 = b_0 = 0$

$a_2 = k_pC_fR_d; a_1 = k_p + k_iC_fR_d; a_0 = k_i$

The controller $G_c(s)$ is designed to make the overall system satisfy the following requirements: 1) zero steady state error, 2) more than 45^0 phase margin, 3) greater than 2 kHz system bandwidth. The bode plot of the compensated grid current control loop that meets the design requirements is shown in Figure 4.12. The PI controller parameters are designed to obtain a PM of 58^0 at the gain

crossover frequency of 3 kHz. To achieve the required frequency response, the parameter ki/k_p is selected as 714 (kp =14), respectively. As shown in Figure 4.12, low frequency gain is significantly improved and the gain margin (GM) is 12 dB .

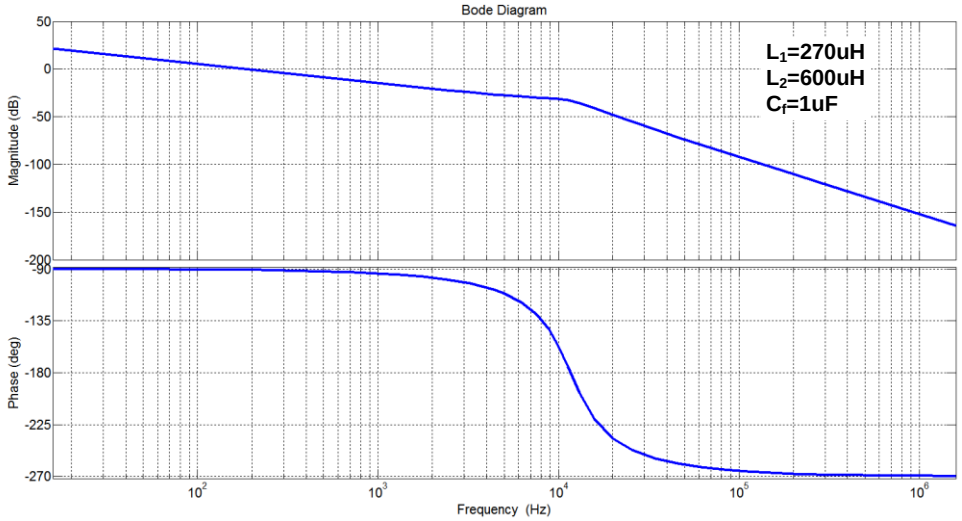


Figure 4.11 Bode plot of current control loop without controller

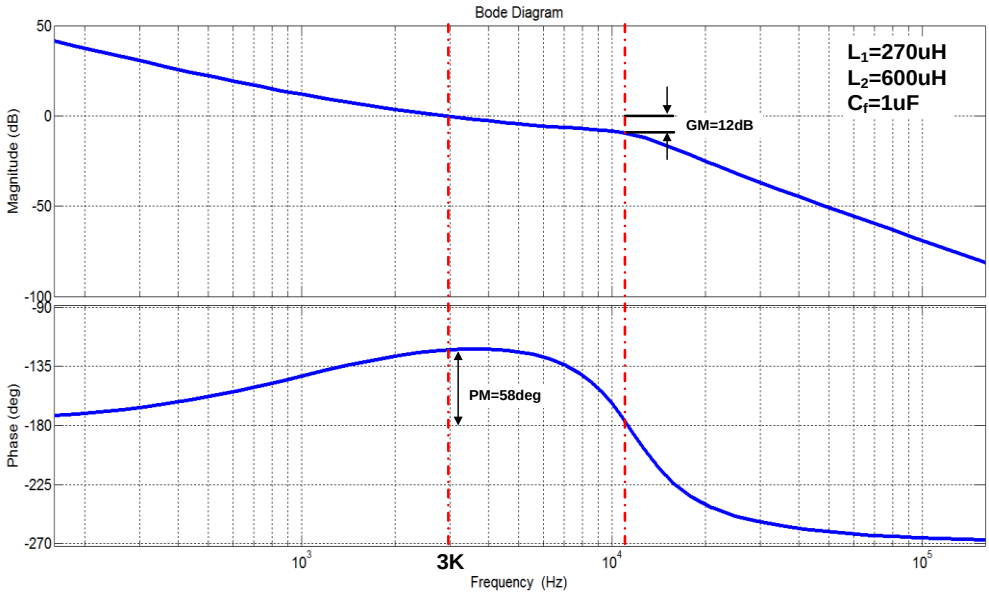


Figure 4.12 Bode plot of current control loop with PI controller: PM=580 at fc=3kHz

4.3 Controller Design of the Bus Voltage Loop

The outer voltage control loop regulates the bus voltage at the reference value by changing the injected grid current according to the overall control block diagram as shown in Figure 4.2. Two current control loops are assumed as a part of the control object in the voltage control loop. The control diagram of the DC link voltage is redrawn in Figure 4.13 showing the inner current control loop and outer bus voltage control loop with the d-axis current loop inside the dashed block.

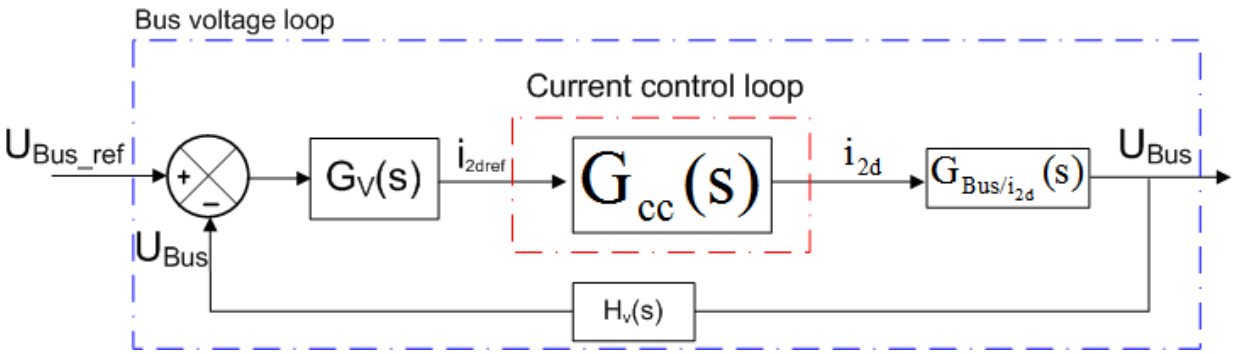


Figure 4.13 Outer bus voltage control loop diagram

As shown in Figure 4.2, the grid voltage U_g and the output current of the first stage DC/DC converter i_{Bus} are regarded as the disturbances to the inner current loop and the outer dc-link voltage control loop, respectively. In most cases the PV MPPT algorithm is relatively slow and grid voltage disturbances are small. As a result, these disturbances can be neglected to a certain extent. Consequently, the transfer function from the injected grid current i_{2d} to dc link voltage can be derived as $G_{Bus/i_{2d}}(s)$ as shown in Figure 4.13. Usually, the bandwidth of the outer

voltage loop should be lower than the current loop in order to ensure the stability of the system. These two loop controllers are designed independently and their interaction can be neglected. The outer voltage control loop regulates the output voltage at the reference value by setting the inductor current reference. According to Figure 4.13, the open loop transfer function of the bus voltage loop is expressed by (4.31). The bode plot of the voltage control loop gain is shown in Figure 4.14. The PI controller parameters are calculated to achieve a PM of 74^0 at the gain crossover frequency of 100Hz. The parameter k_{iv}/k_{pv} is obtained as 117.4 (kpv=8.5).

$$G_{Bus\_open}(s) = G_v(s)G_{cc}(s)H_v(s)G_{\frac{Bus}{i_{2d}}}(s) \tag{4.31}$$

Where:

$$G_{cc}(s) = \frac{1}{1+3\cdot s\cdot T_{delay}} = \frac{1}{1+10^{-4}s}\,[73]; H_v(s) = \frac{1}{200}; G_v(s) = k_{pv} + \frac{k_{iv}}{s}; G_{\frac{Bus}{i_{2d}}}(s) = \frac{\sqrt{3}}{4sC_1}$$

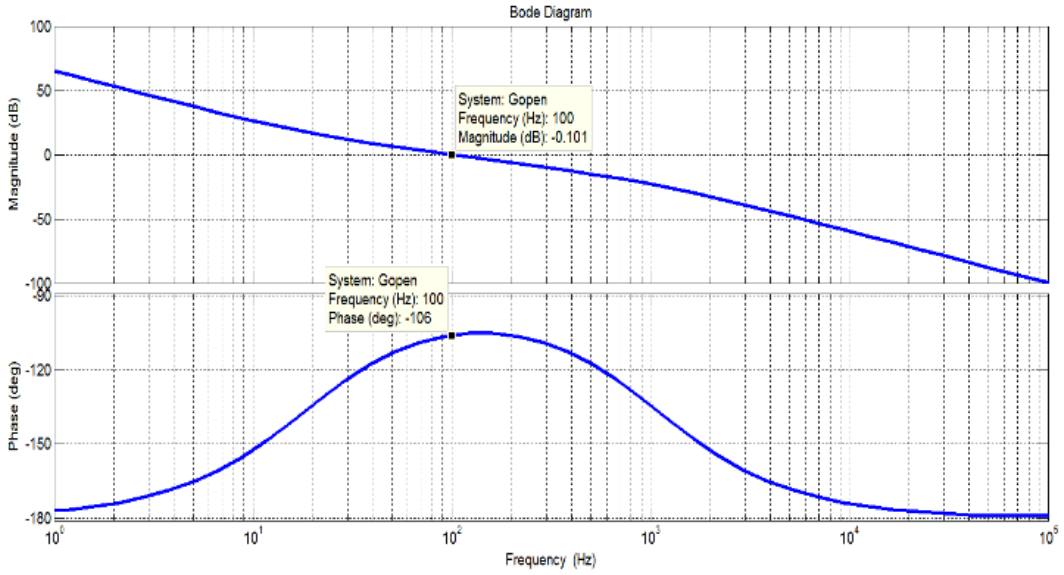


Figure 4.14 Bode plot of outer bus voltage loop with PI compensation: PM=740 at fc=100Hz

CHAPTER FIVE: PARAMETERS CALCULATION OF PASSIVE COMPONENTS

The DC/DC stage and DC/AC stage are decoupled due to the action of the DC link capacitor, simplifying the controller design for both stages. Electrolytic capacitors are typically used in the dc link but the life of electrolytic capacitors is a major concern [7] [8]. Because of the three-phase DC/AC converter in the second stage, the value of the dc-link capacitor can be smaller for a given MIC power rating. Thus the reliability of whole system will be significantly improved if the electrolytic capacitors are replaced by film capacitors. Although the capacitance value of DC-link based on the Qualitative Analysis is not large in a three phase balanced system, the grid quality must be taken into account in a grid tied MIC. The DC-link and input capacitance requirement is determined by many factors such as capacitor voltage variation, grid voltage dips and surges, and disturbance response time. Generally, these factors can be classified into steady conditions and dynamic conditions of MIC according to the specification. Calculation of the input capacitance in the DC/DC stage is also discussed under severe conditions in this section.

5.1 DC-Link Capacitance Calculation

Referring to the small-signal model of the DC-link capacitor shown in [67], the DC-link capacitance is determined by grid disturbance and generator disturbance. Because the MPPT iteration time is relatively slow, the DC-link capacitance is only calculated based on grid disturbance of an unbalanced three-phase system in this paper. Asymmetrical faults lead to drops in one, two, or three phases with not all phases having the same drop. The resulting voltage drops

and phase-angle shifts depend on a number of factors. The different types of voltage sags present in a generic distribution system are summarized in Table 2 [68].

Table 2 Three-phase unbalanced dips due to different fault types and transformer connections

	Location of dip		
Fault type	I	II	III
Three-phase	A	A	A
Three-phase-to-ground	A	A	A
Two-phase-to-ground	E	F	G
Three-phase	C	D	C
Single-phase-to-ground	B	C	D

The voltage variations on the DC-link capacitor with type D dips for a three-phase unbalanced system is investigated as follows: The equation of output voltage and current for each phase can be expressed by:

$$\begin{cases} U_{ga}(t) = (\sqrt{2}U_m + \Delta U)\sin(\omega t) \\ U_{gb}(t) = \sqrt{2}U_m \sin(\omega t) \\ U_{gc}(t) = \sqrt{2}U_m \sin(\omega t) \end{cases} \tag{5.1}$$

$$\begin{cases} I_{2a}(t) = \sqrt{2}I_m \sin(\omega t) \\ I_{2b}(t) = \sqrt{2}I_m \sin(\omega t) \\ I_{2c}(t) = \sqrt{2}I_m \sin(\omega t) \end{cases} \tag{5.2}$$

Where Um is the RMS AC output voltage, Im is the RMS AC output current, and ΔU is the voltage dip. From the output power of the grid side, we can get the instantaneous power of three-phase system:

$$P_{ac}(t) = U_{ga}(t)I_{2a}(t) + U_{gb}(t)I_{2b}(t) + U_{gc}(t)I_{2c}(t) \tag{5.3}$$

Substitute (20), (21) into (22), then simplify it:

$$P_{ac}(t) = 3U_m I_m + \frac{\sqrt{2}}{2} I_m \Delta U - \frac{\sqrt{2}}{2} I_m \Delta U \cos 2\omega t \tag{5.4}$$

Assuming no power loss in the DC-DC stage, we get the instantaneous generated power of PV panel that can be expressed by $P_{pv} = U_{PV} I_{PV}$.

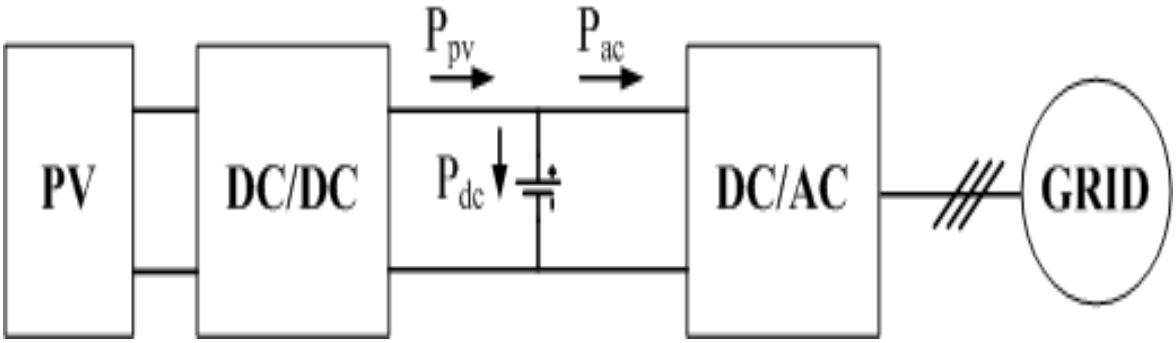


Figure 5.1 Simplified block diagram of two-stage MIC

Then based on Figure 5.1, we get:

$$P_{pv} = P_{dc} + P_{ac} \tag{5.5}$$

Combining (5.3) and (5.4), the energy stored in DC-link capacitor can be calculated under type D dip condition:

$$E_{dc} = \int_0^{\frac{1}{2f}} \left| P_{pv} - 3U_m I_m - \frac{\sqrt{2}}{2} I_m \Delta U + \frac{\sqrt{2}}{2} I_m \Delta U \cos 2\omega t \right| dt \tag{5.6}$$

Alternately, the energy stored in DC-link capacitor can also be expressed by (5.7)

$$E_{dc} = \frac{C(U_{Bus,max}^2 - U_{Bus,min}^2)}{2} = C U_{Bus} \Delta U_{Bus} \tag{5.7}$$

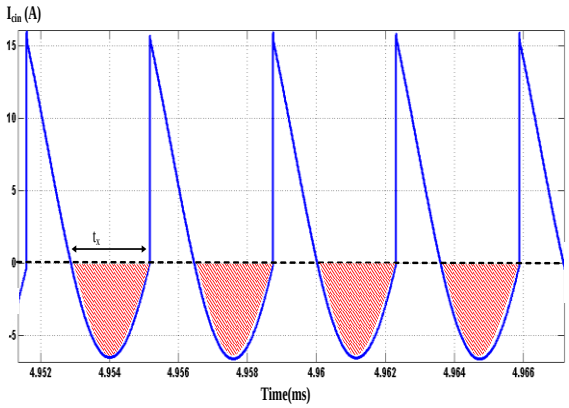
Substitute (5.6) into (5.7), and we find $P_{pv} = 3U_m I_m$ for three-phase balanced system, the DC-link capacitance is represented by (5.8) after simplification:

$$C = \frac{\frac{\sqrt{2}}{2} I_m \Delta U}{2U_{Bus} \Delta U_{Bus} f} \tag{5.8}$$

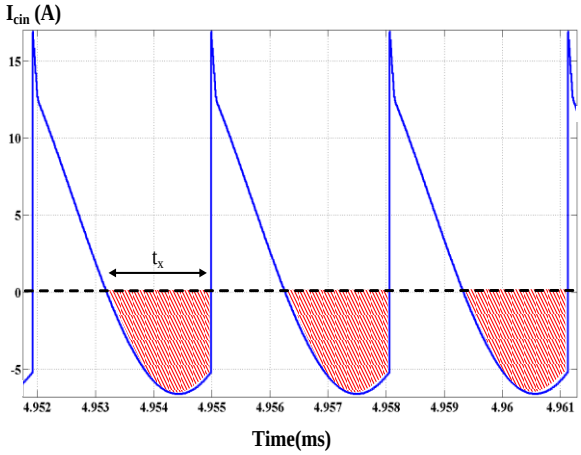
For a maximum output power of 400 watts, the power rating of each phase is 133 watts. The DC-link voltage (U_{Bus}) is selected as 400V with voltage ripple (ΔU_{Bus}= 20V) and voltage dip ($\Delta U = 40V$). The capacitance is 35.3uF based on the calculation in (5.8) with a line frequency f=60Hz and I_m=1.2A.

5.2 Input Capacitance Calculation for LLC Resonant Stage

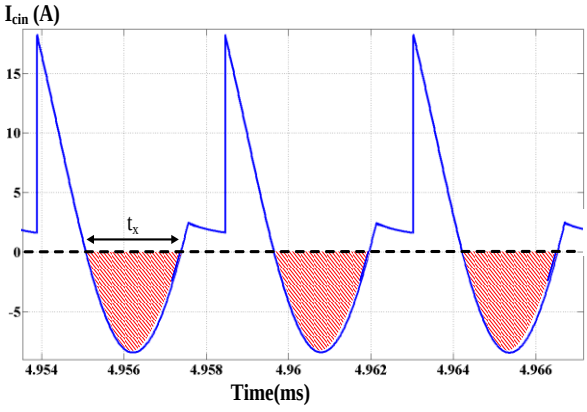
As mentioned previously, the LLC stage is decoupled from the inverter stage by the DC-link capacitor therefore grid disturbances have little impact on the calculation of input capacitance. The input capacitance is a function of the steady state and dynamic characteristics of the PV panel and the LLC resonant converter. Since the execution of the maximum-power-point-tracking (MPPT) algorithm is slow, PV panel irradiance change is not a critical factor when calculating input capacitance. For the LLC resonant converter operating at maximum input current and maximum ripple on the input capacitor, the basic equation $\int i_{C_{in}} = \int C_{in} \frac{dU_{C_{in}}}{dt}$ is used to calculate the capacitance. The parameters for the LLC DC/DC stage are as shown in Table II (Lr=1.9uH, Lm=10.3uH, Cr=680nF and turns ratio of the transformer N=4.5) and are given according to Xiang's numerical model for the LLC resonant converter as referenced in [69]. For demonstration purposes, the current ripple of the input capacitor is plotted by Matlab Simulink at the maximum output power (400W) as shown in Figure 5.2 with three different input voltage conditions, fs<fr, fs=fr and fs>fr. Under the severe condition of the maximum power output at 35V (fs<fr), input capacitor current is higher than two other conditions as illustrated in Fig. 16-C, where tx ≤2.3us and the LLC resonant cycling period is 7.14us due to the values of Lr and Cr. Thus, input capacitance could be calculated with (5.9). Assuming the voltage ripple on the input



fs=fr



fs>fr



fs<fr

Figure 5.2 Input capacitor current with various switching frequency at 400W output and different input voltage: (a) fs=fr; (b)fs>fr; (c)fs<fr

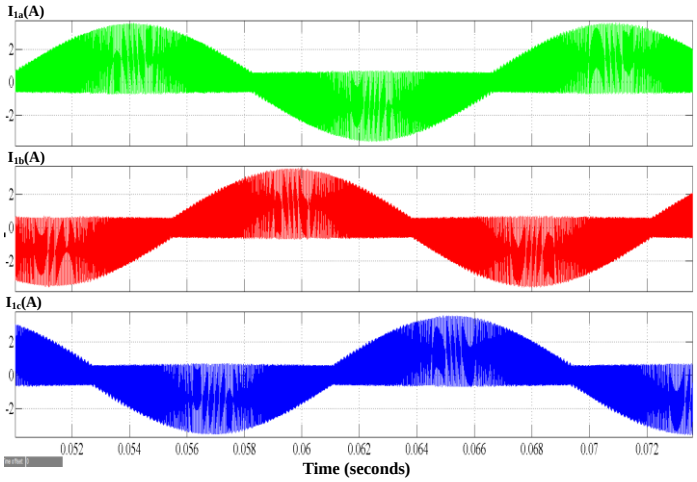
capacitor (ΔU_{Cin}) is less than 0.25V, and $Ic_{in,peak}$ equals to 9.2A as shown in Figure 5.2, the input capacitance is 83.16uF when those values are substituted into (5.9). The input capacitance is selected to be 85.8uF in this prototype using 26PCS 3.3uF ceramic capacitors in parallel.

$$C_{in} = \frac{\int i_{C_{in}}}{\Delta U_{Cin}} = \frac{\int_0^{t_x} I_{Cin,peak}(\sin\frac{t}{\sqrt{L_r C_r}})dt}{\Delta U_{Cin}} = \frac{I_{Cin,peak}\sqrt{L_r C_r}}{\Delta U_{Cin}} \quad (5.9)$$

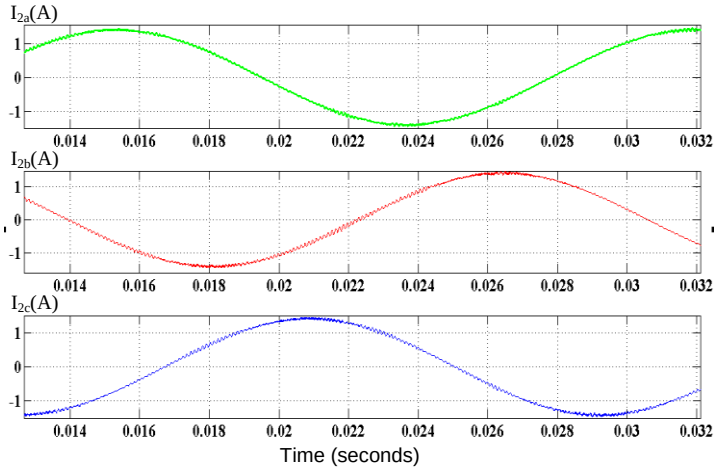
CHAPTER SIX: SIMULATION &EXPERIMENTAL RESULTS

6.1 Simulation results

A three phase two stage micro inverter with triple-loop compensation was simulated with MATLAB/Simulink.



(a) Each phase inductor current



(b) Three-phase injected grid current

Figure 6.1 The inductor current waveform and injected grid current in the inverter stage

Figure 6.1(a) shows the current waveform of inverter side inductor L_1 and Figure 6.1(b) shows the injected grid current of each phase with less than 0.5% THD.

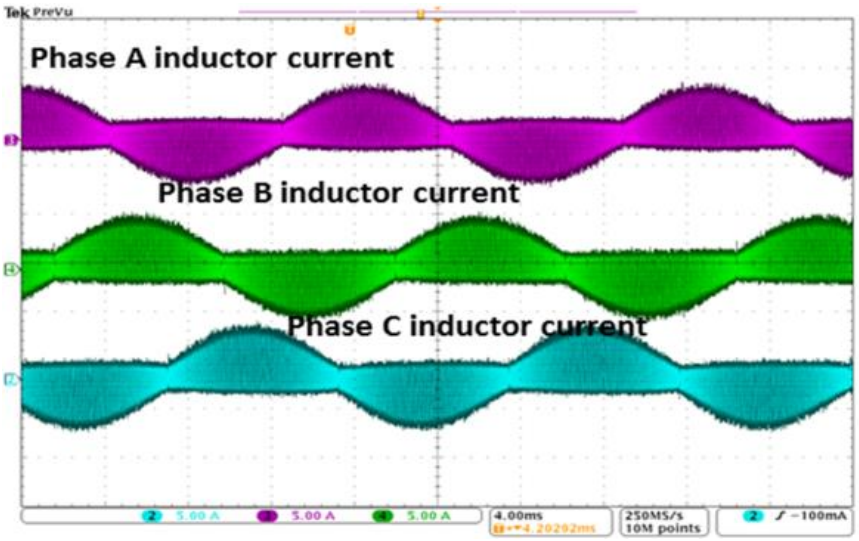
6.2 Experimental results

A three-phase four-wire micro inverter prototype with both-stage ZVS was built based on the following specifications: maximum output power 400W and output voltage 208/120VAC. Key parameters are shown in Table 3. The input voltage range of the PV panel for maximum power tracking is from 35VDC to 55VDC.

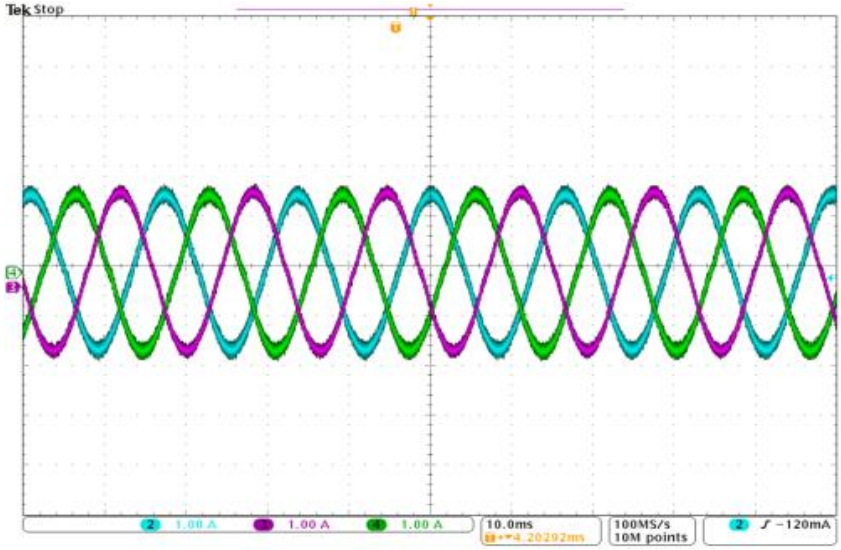
Table 3 Key parameters of the experimental prototype

Three-phase Four-wire DC-AC Converter	
Output voltage	120Vac
Output frequency	60Hz
Rated output power	400W
Bus Voltage (U_{Bus})	400V
Secondary switch S_7- S_{12}	FCB20N60TM
Inductor L_1	270uH
Grid interface inductor L_2	600uH
Output capacitor C_f (B32923 X2 MKP)	1uF (R_d=10mohm)
Switching frequency fs	20-180 kHz
Grid current sensing coefficient H_{iL2}	1.2

A three-phase four-wire voltage source inverter is employed in the second stage that connects the dc bus to the grid through an inductance of 600uH. The nominal dc-bus voltage is 400V and the grid voltage RMS value is 120V L-N.



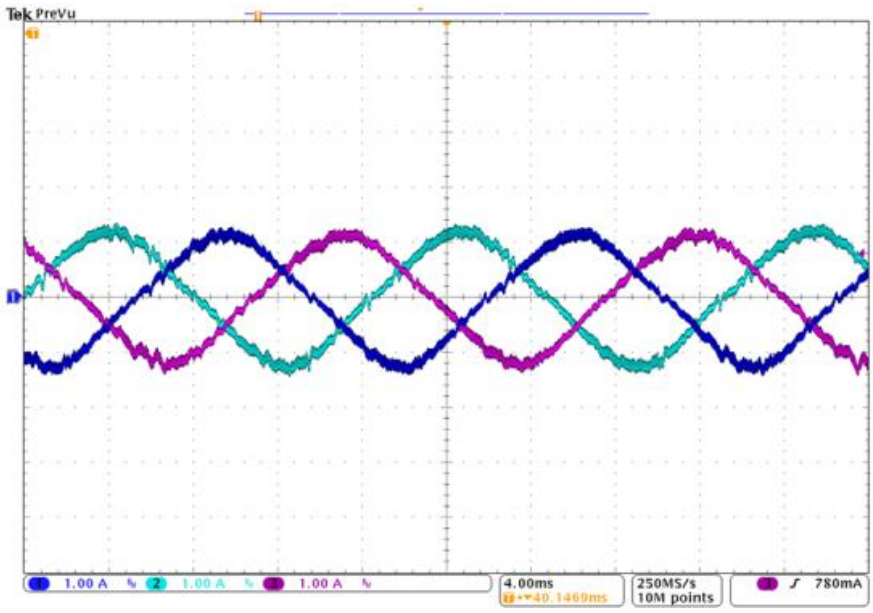
(a) Each phase inverter side inductor current



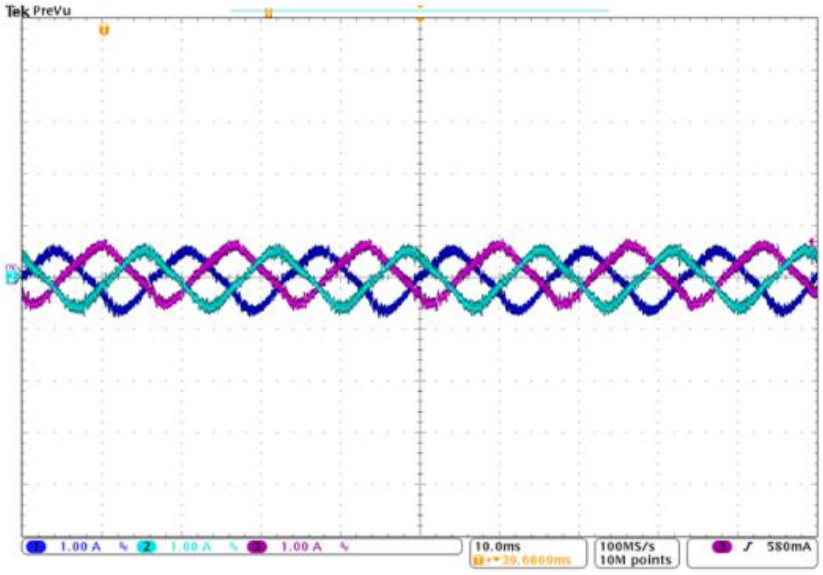
(b) Three-phase injected grid current

Figure 6.2 The inductor current waveform and injected grid current in the inverter stage

The inverter side inductor current waveform and injected grid current at rated output power in the three-phase inverter are shown in Figure 6.2.



(a) Three-phase injected inductor current (50% rated output power)



(b) Three-phase injected inductor current (20% rated output power)

Figure 6.3 The injected grid current with different power levels

Although the inverter side inductor current has a high ripple, the THD of the injected grid current is less than 2.5% and meets the IEEE 1547 standards [70]. In addition, Figure 6.3 shows the experimental waveforms of the injected grid current at different power level with 20% and 50% of rated output power. According to the theoretic analysis and simulation, low THD of the injected grid current still can be achieved even at small output power. From Figure 6.3, the injected grid current THD has a little bit higher than full rated output power. The reason is that the relative error of the measurement of the current sensor is high at light output power. The injected grid current THD will be reduced with the current sensing improvement. Figure 6.4 shows the inverter output dynamics with a step change of the current reference from 0 to 50% rated output power. It can be seen from Figure 6.4, the injected grid current tracks quickly the current reference due to the action of VFBCM control in the inner current loop. In addition, the dynamic response of the inverter to a step change in the grid voltage from 120Vrms to 80Vrms is shown in Figure 6.5. In order to observe the performance of the soft start function, the measured waveform of the injected grid current increased gradually is shown in Figure 6.6.

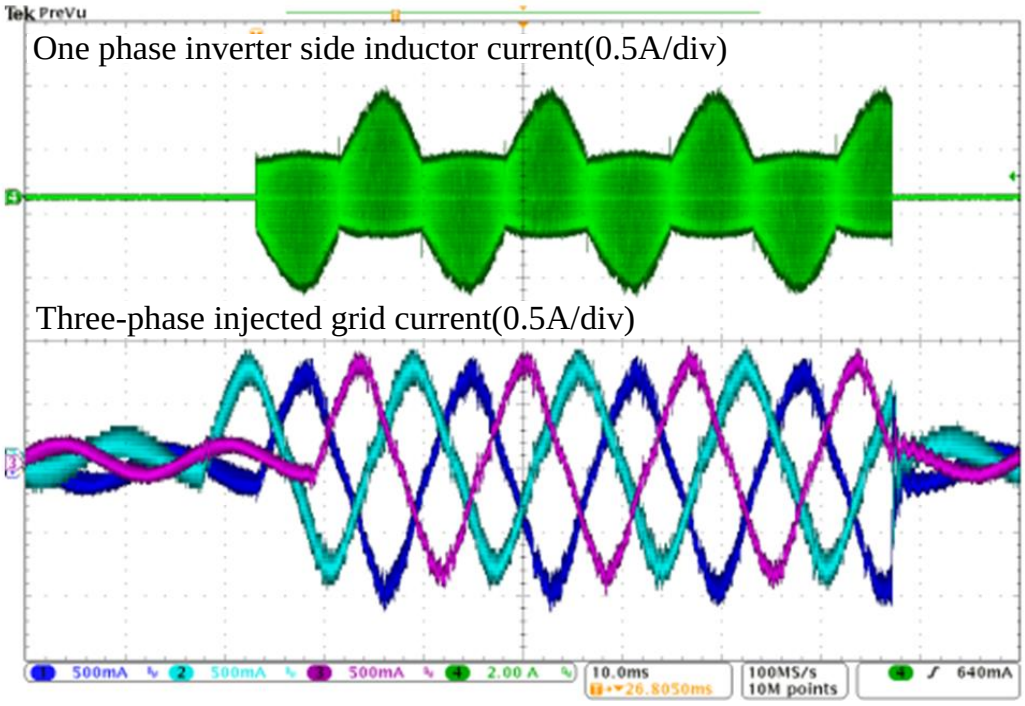


Figure 6.4 The load dynamic response of the inverter to a step change 0 to 50% rated output power

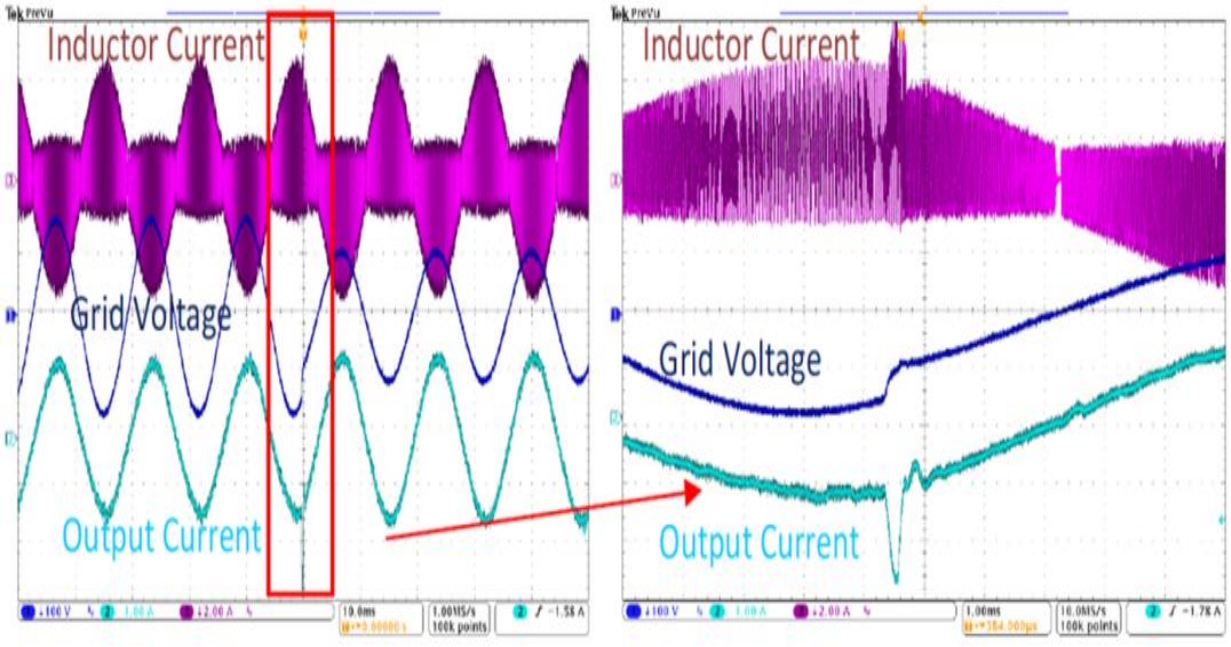


Figure 6.5 Dynamic response to a step change in the grid voltage from 120V to 80V

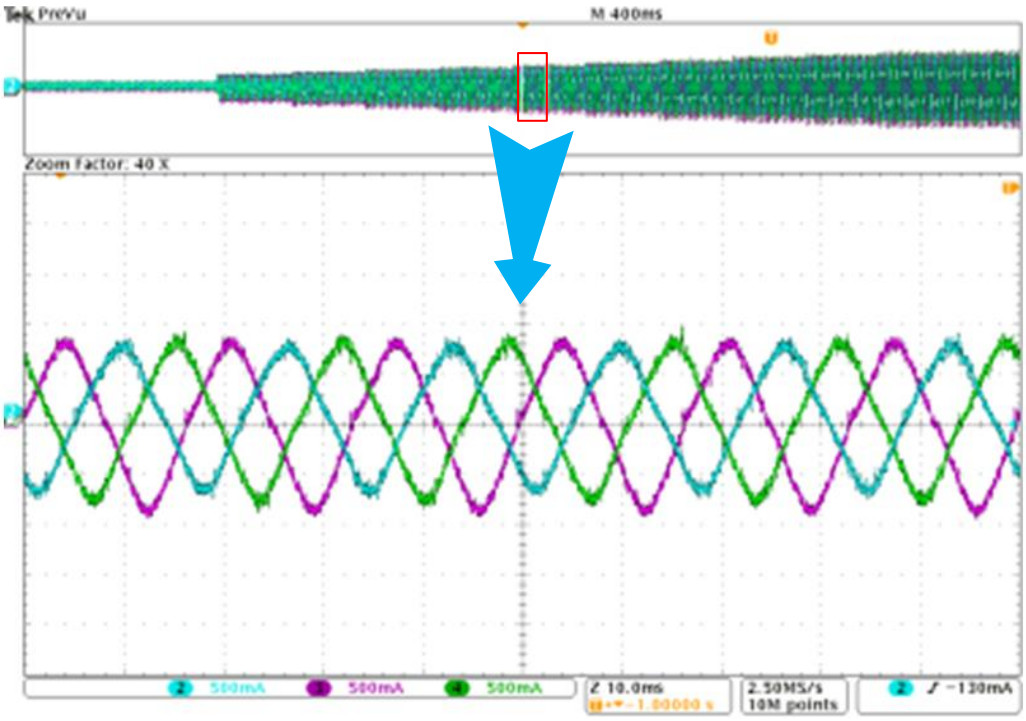


Figure 6.6 Soft start function of the three-phase four-wire grid-connected inverter (0.5A/div)

Figure 6.7 shows the experimental waveform of overall system when connected to the grid. The DC-link regulator is employed to keep the bus voltage constant while the CPI MPPT algorithm is active. As shown in Figure 6.7, the injected current (green channel) to the grid is gradually increasing with the MPPT which is tracking the maximum power of the PV panel.

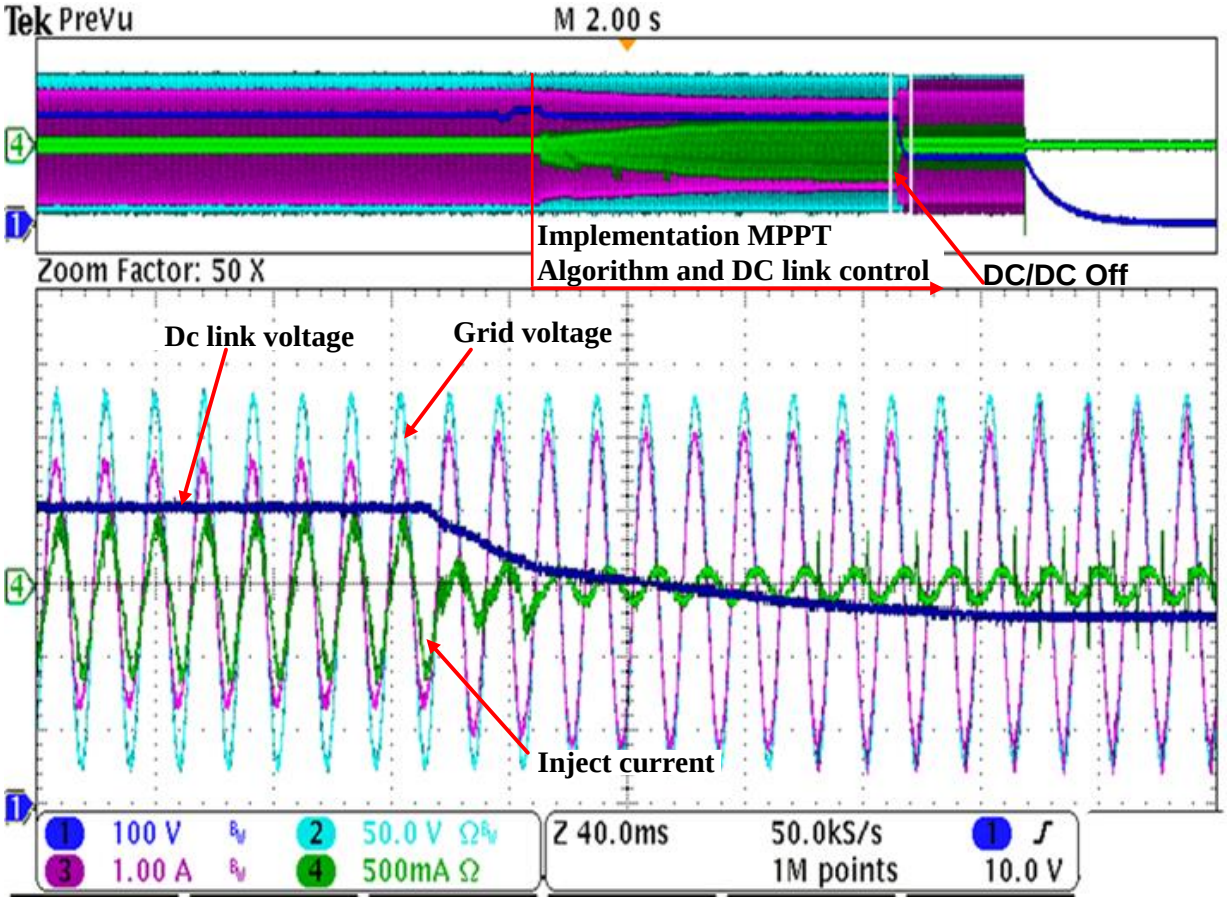


Figure 6.7 The experimental waveform of overall system with grid-connected

CHAPTER SEVEN: CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In this dissertation, several type architectures for micron inverter application are analyzed. Focusing on two-stage architecture for single phase micro inverter, a Forward-Flyback converter with boundary mode operation to achieve ZVS has been proposed in this dissertation which is employed in the first stage to boost the output voltage of PV panel. To further improve the efficiency through reducing turning-off losses, an active LC snubber is employed to suppress the voltage spike across the primary MOSFET switch and to recycle energy stored in the transformer leakage inductance. The operation of the converter is analyzed and a detailed design procedure is given to facilitate optimal design of the converter. A 200W BMFFC prototype was built and tested. The measured maximum efficiency reached 97.2%. The experimental results demonstrating better efficiency of the BMFFC over full range operation not only validate the operation of the converter but also confirm the superiority of the BMFFC over the conventional Forward-Flyback converter for low power applications.

A small signal model of the inner loop control with VFBCMC is presented. The fast dynamic response of the three-phase four-wire grid-connected inverter is achieved due to VFBCM control. In order to use the PI regulator of the grid current control in the second loop, a small signal equivalent circuit of three-phase four wire inverter in the rotating synchronized frame is derived based on average signal model. Once the design of the two inner current control loops was completed, design of the DC link controller was addressed for two-stage micro-inverter applications. Lastly, the modeling and triple loop controller design from the inner current loop to

outer bus voltage loop are verified by experimental results based on a 400 watt two stage micro inverter prototype.

7.2 Future work

By feeding back all of the states in a completely controllable system, it is possible to place the closed-loop poles anywhere in the complex plane. This is equivalent to saying that any desired response can be achieved with the help of a feedback controller. The technique of pole placement will be presented for finding the gains in a feedback controller that will place the closed loop poles at a desired location. A natural way to the pole placement is the direct pole placement based on the open loop poles and the desired dynamics of the closed loop system. For most control systems the measurement of the full state vector is impractical. In order to reduce the number of system sensors and implement a design based on full state feedback, the estimate the states of a system using measurements are practical. The state estimation is accomplished by designing a set of equation for the computer that estimates the states using all information available. According to control theory, the roots of the characteristic equation of the closed loop system are the roots obtained by the pole placement design plus those of the observer. Hence, the pole placement design is independent of the observer design. In order to further improve the dynamic response of three-phase four-wire DC/AC converter, controller design using pole placement and observer techniques based on state-space modelling will be investigated in the future research.

APPENDIX A: LIST OF PUBLICATIONS

Journal papers

[1] **Lin Chen**, Haibing Hu, Ahamad Amirahmadi, Qianzhang and Issa Batarseh, "Boundary Mode Forward-Flyback Converter with Efficient Active LC Snubber Circuit" IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 29, NO. 6, JUNE 2014, pp.2944-2958.

[2] **Lin Chen**, Ahamad Amirahmadi, Qianzhang Nasser Kutkut and Issa Batarseh, "Design and Implementation of Three-phase Two-stage Grid-connected Module Integrated Converter", is accepted for publication, IEEE Transactions on Power Electronics.

[3] **Frank Chen**, Emil Auadisian, John Shen and Issa Batarseh, "Soft Switching Forward-Flyback DC-DC Converter", Journal of Electrical and Control Engineering, Vol. 3 No. 5, 2013 PP. 26-35 www.joece.org/ © American V-King Scientific Publishing

[4] **Lin Chen**, Ahamad Amirahmadi, Qianzhang Nasser Kutkut and Issa Batarseh, "Modeling and Triple-loop Control of Three-phase Four-wire ZVS Grid-connected Inverter for Two-stage Micro-inverter Application", under review-recommended publication, IEEE Transactions on Power Electronics.

Conference papers

[1] **Frank Chen**, Qiang Zhang, Ahmad Amirahmadi and Issa Batarseh, **"**Modeling and Analysis of DC-Link Voltage for Three-Phase Four-Wire Two-Stage Micro-Inverter" is accepted by APEC2014 and will be presented at Fort-Worth, TX on March 16-20, 2014.

[2] **Frank Chen**, Ahmad Amirahmadi and Issa Batarseh, "Zero Voltage Switching Forward-Flyback Converter with Efficient Active LC Snubber Circuit" is accepted by APEC2014 and will be presented at Fort-Worth, TX on March 16-20, 2014.

[3] **Frank Chen**, Qiang Zhang, Ahmad Amirahmadi and Issa Batarseh "Design and Implementation of Three-phase Grid-connected Two-stage Module Integrated Converter" The 14th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL),23-26 June 2013 at Salt lake city, UT.

[4] **Frank Chen,** Emil Auadisian, John Shen and Issa Batarseh,"Forward-flyback mixed ZVS DC-DC converter with non-dissipative LC snubber circuit", published in IEEE Applied Power Electronics Conf.(APEC),17-21 March 2013 at long beach, CA.

[5] **Frank Chen**, Somani Utsav,John Shen and Issa Batarseh,"new Architecture single-phase micro inverter with cascaded low voltage DC/DC cells", Proc telecommunications energy conference(INTELEC),Sept.30-OCT.4 2012 IEEE 34th international, at Scottsdale,AZ.

[6] **Frank Chen**; Hu, Haibing; Shen, John; Batarseh, Issa; Rustom, Khalid; "Design and analysis for ZVS forward-flyback DC-DC converter" Energy conversion Congress and Exposition (IEEE-ECCE),17-22 Sep 2011.

APPENDIX B: LIST OF REFERENCES

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