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IMPROVED FAMILY OF RESONANT DC-TO-DC AND DC-TO-AC POWER CONVERTERS

by

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ABSTRACT

A family of dc-to-dc boost derived isolated resonant power converter topologies and new modified boost isolated dc-to-ac zero-voltage-switching inverter topology are proposed. The dc-to-dc converters include the basic isolated boost, modified isolated boost with active clamp and a modified isolated boost with output resonant network. The principle of operation and steady-state analyses for all these topologies are presented. It is shown that the dc-to-dc converters proposed operate at zero-voltage switching and have better control characteristic performance with improved efficiency and lower current and voltage stresses. The application of the proposed topologies is not limited to dc-to-dc and dc-to-ac power supplies but can also be used for improving power factor. Simulation of these converters using PSPICE is given to verify the theoretical and experimental results. In addition, the new isolated dc-to-ac modified boost converter is proposed which achieves zero-voltage switching for the main power switch. Furthermore, parasitic components in the circuit are utilized to achieve resonance condition essential for zero-voltage switching for the two switches employed in this topology. As a result, enhanced performance and improved efficiencies are achieved in the newly developed inverter. Steady state analysis, PSPICE simulation, small signal modeling and experimental results are given to verify the theoretical, simulation and experimental results. The simulation and experimental results for the dc-to-ac inverter are in good agreement with the predicted results.

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I dedicate this thesis to my grandfather Gulamrab Abdul Rahim Khan and his vision.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Power electronics, which is multi-disciplinary in nature, principally deals with energy processing and control of power flow by using power semiconductor devices. Generally the power processor circuits rely on solid-state semiconductor devices operating on switched mode, i.e. either on or off. Ideally these switches should have no voltage drop when on and carry no current when in the voltage blocking stage. [13,14,15] The power electronic circuits are used to process power efficiently using semiconductor devices, modern control techniques, mathematical tools and computer simulation. The processing involves power conversion (dc-to-ac, ac-to-dc, dc-to-dc and ac-to-ac) for industrial, commercial and residential application. Because of a continuing demand for smaller, lighter and more efficient power processing equipment, significant improvements in circuit topologies, control techniques, simulation tools and semiconductor devices have been reported in recent years. [1-10] Converters will be used to refer to single power conversion stage to perform any of the following functions defined by the nature of its input and output: ac to dc, dc to ac, dc to dc and ac to ac.

Due to switching, power electronic circuits normally exhibit square current and voltage waveforms. Also they produce nonlinearities, which introduce harmonic frequency components resulting in waveform distortion and reduction in power factor. Power factor is defined as the ratio of the real power to the apparent power in the circuit. Power factor can be enhanced by either passive elements like inductor and capacitors, which introduce phase shifts in the current waveforms resulting in unity power factor angle, or by active switching circuits that are used to program input current waveform to follow the line voltage. Improvement of power factor in switching power electronic circuits also implies reducing the total harmonic distortion.[3-10]

The reduction of power factor caused by switching circuits causes the power electronic equipment to get approximately two-thirds of the power available at the mains [4]. Due to the increase of power electronic equipment connected to the utility system, various national and international agencies have been considering limits on harmonic current injection to maintain good power quality. Various standards and guidelines are established that specify limits on the magnitudes of harmonic currents and harmonic voltage distortion at different harmonic frequencies. [24]

Efforts to solve the problem of poor power factor have been made for many years. [2-10] Generally, two methods are used for power factor correction: passive and active methods. The passive methods used implementing passive elements, like inductors and capacitors, only adjust the phase difference in the current and voltage waveforms. The overall energy efficiency remains the same because of some losses occurring in the inductor. This

method is good for linear systems but not for dc-to-dc nonlinear systems. The disadvantages of this method are cost, size and losses. [6]

The second method used is the active shaping of the input line current. This method uses different types of active power converter to achieve unity power factor. The choice of the electronic power converter used is based on the following considerations:

(1) The need for electrical isolation between the utility input and the output of the power electronic system. In some cases, this can be provided in the second converter stage as in the switch-mode dc power supplies.

(2) In most applications it is desirable or acceptable to have regulated dc output voltage at a higher voltage than the maximum of the ac input. Hence, boost converters can be used in these applications.

(3) The cost, power losses, and size of the current shaping circuit should be as small as possible.

Since the topologies here belong to two classes of power electronic circuits, it will be useful to review the different classes of power circuits. The power converters can be generally classified as: [15]

i) Ac-to-dc converters (Rectifiers): These converters have used thyristors with phase control and ac line commutation to convert ac-to-dc power for applications like dc drives and electro-chemical processes.

ii) Ac-to-ac converters (Ac controllers or Cycloconverters) Thyristor or triac ac voltage controller (same output frequency) implementing phase control is widely used in applications like heating control, light dimming control etc.

iii) Dc-to-ac converters (Inverters): These inverters are generally classified as voltage-fed and current-fed types primarily used in ac motor drives, UPS (Uninterruptible power supplies), and induction heating. The voltage-fed type inverter is the most popular for industrial applications.

iv) Dc-to-dc converters (Choppers): They convert unregulated dc voltage to a regulated or controlled dc voltage at different level commonly used in dc motor drives and switching mode power supplies. These types of converters are further classified as:

1) PWM type converter, which can be further, classified as buck, boost or buck-boost type. A single-quadrant drive uses buck converter; a two-quadrant drive uses buck and boost types in combination, whereas a four-quadrant drive uses an H-bridge that uses buck and boost functions. High power converters use an H-bridge that provides buck and boost functions for either direction of rotation. High power converters generally use BJT, IGBT, or GTO switches with up to several kHz switching frequency, and low power low voltage converters use power MOSFETs at much higher frequency.[15]

2) For higher switching frequencies, resonant and soft-switching converters are used. There is reduction in switching losses but there is an increase in magnetic and capacitor losses. There is a LC tank circuit that generates quasi-sine waves that permits zero-voltage and zero-current switching. At

very high frequencies in the MHz range the tank elements are so small that the parasitic elements are used for this purpose.

1.1.1 Basic Active Power Factor Correction Circuits

There are three basic active power factor correction circuits, namely, Buck, Boost and Buck-Boost topologies. These topologies use current control or voltage control mode to achieve the goal of power factor correction. Input current or voltage is used as the parameter to be controlled in this control strategy. Also another classification of control methods is based on the continuity of the input current through the converter. The two methods are CCM (continuous-conduction mode) and DCM (discontinuous-conduction mode). [16] CCM control requires that the current through the converter be continuous at every instant. In other words, the value of the current can be calculated at a given instance in time. This is not a requirement in DCM control that makes it a simpler control implementation.

a. Buck power factor correction circuit

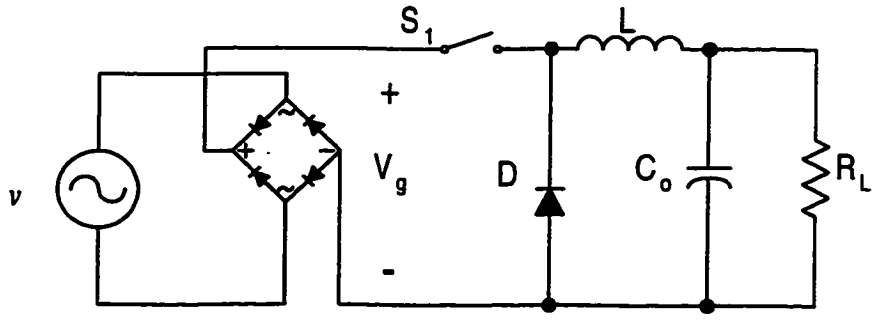

Fig. 1.1(a) Buck Power Factor Correction Topology

Figure 1.1(a) shows a typical buck converter with ac input and a full-wave rectifier.

The operation of the converter is the same as a dc-to-dc buck converter. The input to the converter is an unregulated dc input (which is the output of the full-wave rectifier). The control purpose is different for duty cycle control of this configuration. The transfer function, H(s), and input impedance, $Z_{in}(s)$, of this configuration are given by

$$H(s) = \frac{d}{s^2 LC_o + sL/R_L + 1}; \tag{1}$$

$$Z_{in}(s) = \frac{R_L}{d^2} \frac{s^2 LC_o + sL/R_L + 1}{sRC_o + 1} \tag{2}$$

Proper control of duty cycle d is used to achieve pure resistive input impedance to obtain a unity power factor in practice. [2,16,22] Generally voltage mode control is used for this topology. The voltage of the input inductor or capacitor is controlled by the duty cycle in this voltage mode control technique.

b. <u>Boost power factor correction circuit</u>

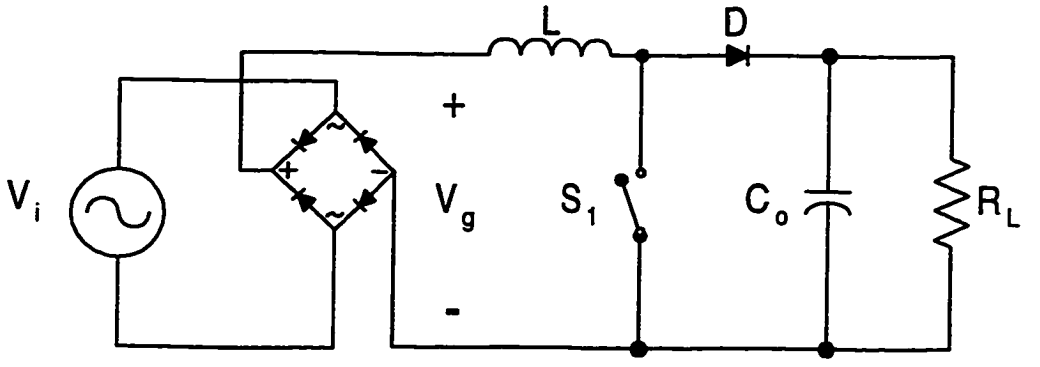

Fig. 1.1(b) Boost power factor correction topology

Figure 1.1(b) shows a typical boost power factor correction topology. The input to the boost converter is unregulated dc output from the full-wave rectifier.

The transfer function, H(s), and input impedance, $Z_{in}(s)$, of this configuration are given by

$$H(s) = \frac{1/d'}{s^2(L/d'^2)C_o + s(L/d'^2)/R_L + 1}; \quad (3)$$

$$Z_{in}(s) = d'^2 R_L \frac{s^2(L/d'^2)C_o + s(L/d'^2)/R_L + 1}{sR_L C_o + 1} \quad (4)$$

where $d'=1-d$

The equivalent inductance of the topology is controlled by the duty cycle. Current control method is used in this configuration which programs the input current to achiever unity power factor. Therefore, there is control over the magnitude and phase of the impedance. This means better control to achieve "pure resistive impedance" and unity power factor.

c) **Buck-Boost power factor correction circuit**

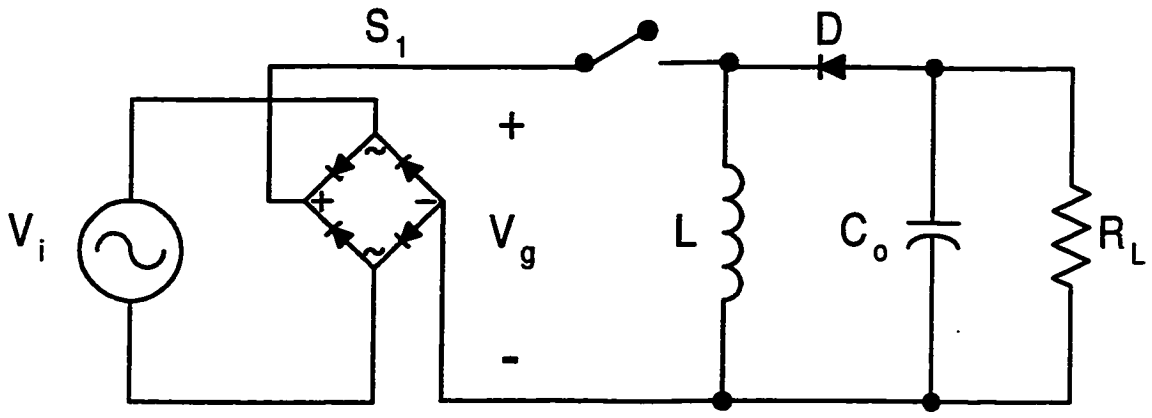

Fig. 1.1(c) Buck-Boost power factor correction topology

Figure 1.1(c) shows the buck-boost power factor correction topology. The transfer function, H(s), and input impedance, $Z_{in}(s)$, of this configuration are given by,

$$H(s) = \frac{d/d'}{s^2(L/d'^2)C_o + s(L/d'^2)/R_L + 1}; \quad (5)$$

$$Z_{in}(s) = \left(\frac{d'}{d}\right)^2 R_L \frac{s^2(L/d'^2)C_o + s(L/d'^2)/R_l + 1}{sR_LC_o + 1} \quad (6)$$

Again, this topology uses the control of the duty cycle to achieve the current or voltage control to achieve unity power factor. Buck-boost topology combines the advantages of the buck and boost topologies.

1.2 Proposed Work

The topologies presented in this dissertation are based on the boost configuration operating in continuous conduction mode. The proposed work is divided into two parts. The purpose of the first part is to analyze the three proposed different dc-to-dc power converter

topologies. The first topology is a basic isolated modified converter. The equivalent circuit of the basic isolated converter is shown below in Figure 1.2. [11] The steady state waveforms, simulation results, circuit performance parameters and experimental results are discussed.

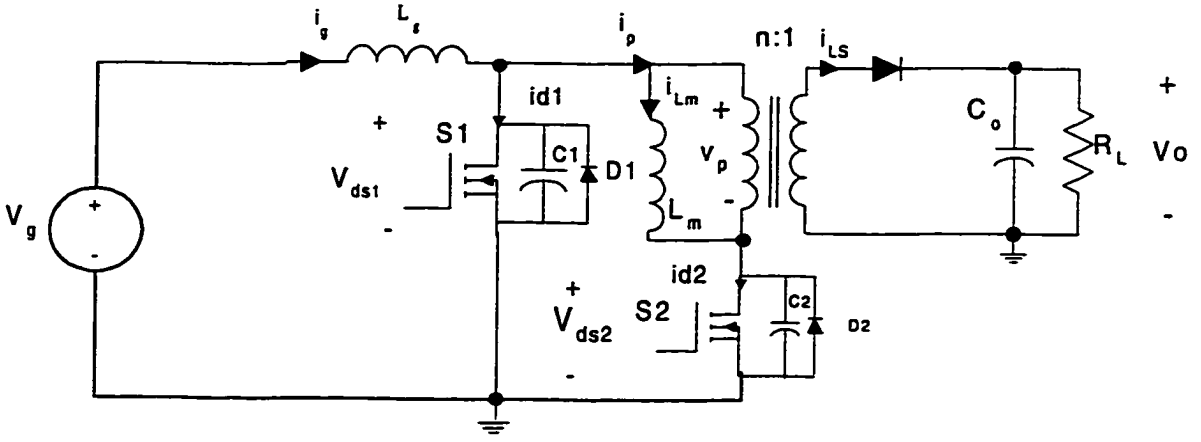

Figure 1.2 Basic Isolated Boost derived ZVS converter

This topology is derived from the basic boost topology having a transformer to isolate the output and a second switch is introduced to provide transformer core-resetting. The performance parameters mainly voltage stress across the two switches, are discussed. The analysis shows that the primary switch is hard switched while the secondary switched, switched complimentary to the primary switch, achieves zero-voltage switching.

The second topology is a boost derived modified converter using an active clamp circuit to clamp the voltage across the secondary switch. This circuit is shown in Figure 1.3.

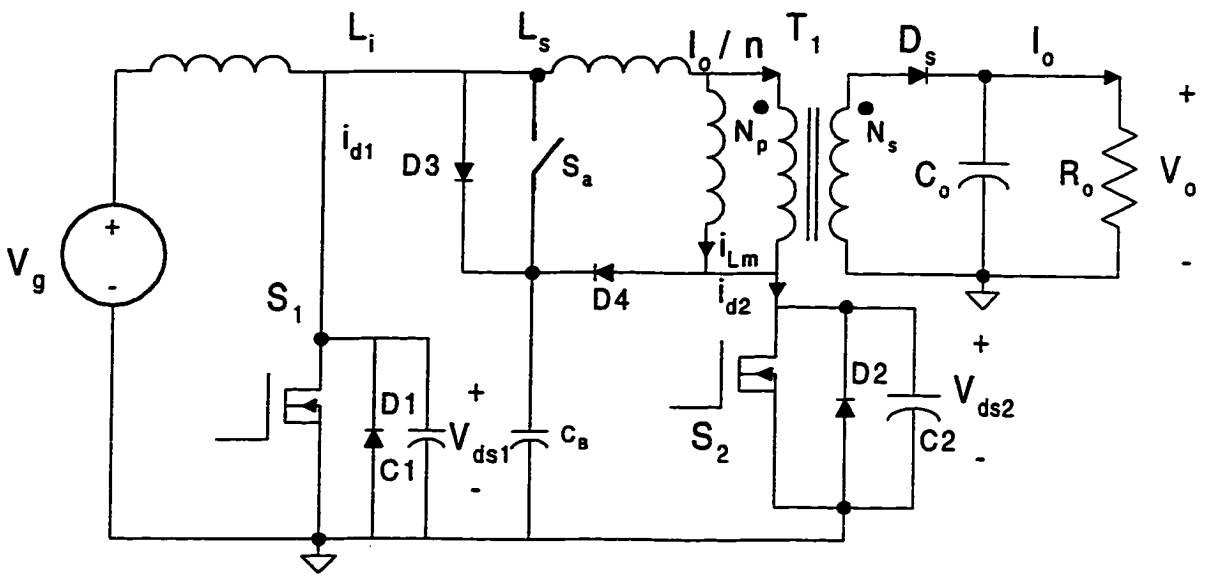

Figure 1.3 Modified basic isolated converter with active clamp

It will be shown that the secondary switch in Fig. 1.3 operates at zero-voltage switching (ZVS) but the primary switch is still hard switched. The current rating of the secondary switch is much lower than the primary switch.

The third converter is the modified basic converter with an additional winding in the isolation transformer and a diode network at the output side of the converter as shown in Fig. 1.4.

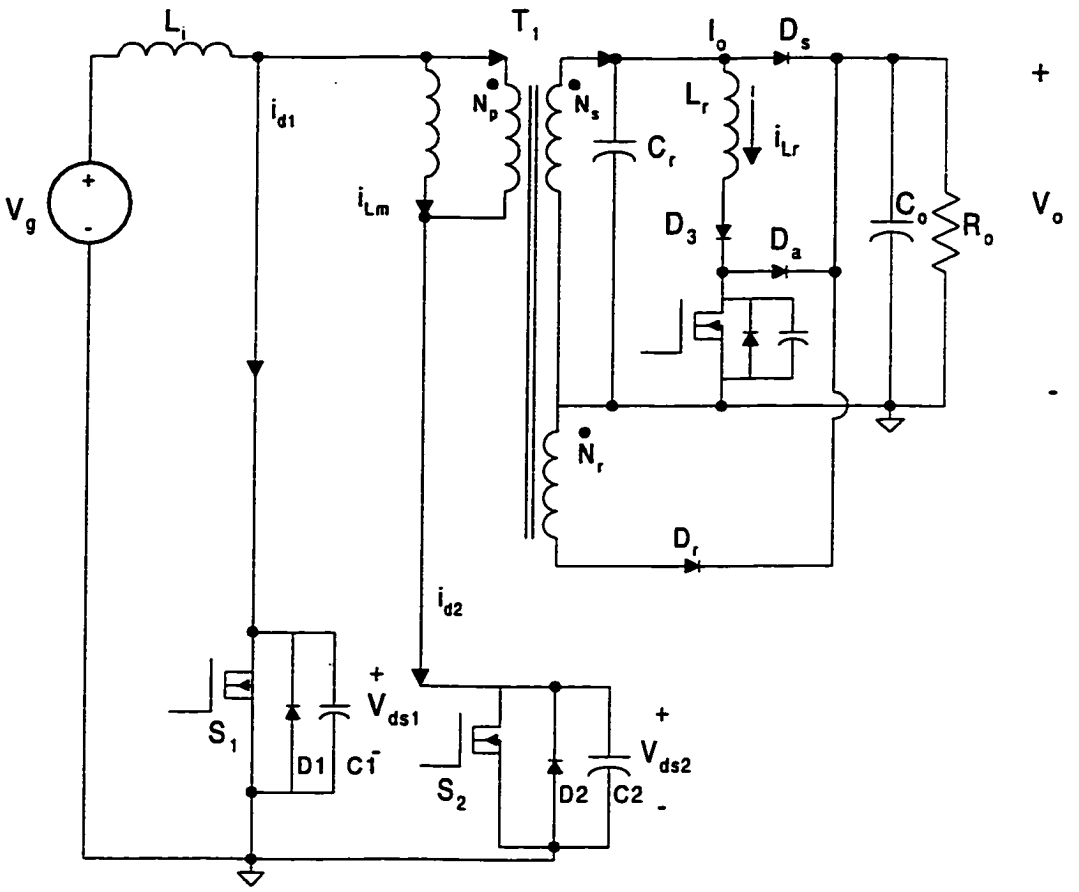

Figure 1.4 Modified basic isolated converter with output diode network

Zero-voltage switching is achieved for both the primary and secondary switches. Switching losses are reduced as a result of ZVS for the primary switch also. There is also reduction in voltage peaks across the secondary switch. The ZVS switching for both reduces switching providing efficiency of about 92%. [12] The Pulse-width modulation technique is used for all these converters. These converters have potential applications in power factor correction, which can be implemented with relative ease

The second part of the proposed work is dc-to-ac resonant inverter used to produce high frequency ac output. Resonance technique is used similar to the dc-to-dc converters. Steady-state analysis using state-space approach along with PSPICE simulation is completed. Mathematical analysis is done with sinusoidal approximation for the secondary voltage across the transformer. Characteristic performance curves are derived and developed with the help of MATLAB. Comparison of simulation and theoretical mathematical values is successfully performed. The dc-to-ac inverter proposed is shown in Figure 1.5 is a modified basic converter with a LCC (series-parallel resonant tank) circuit at the output side of the inverter. The LCC tank provides symmetrical output voltage from a dc source at the input. The parasitic capacitance's across the two switches are used along-with the magnetizing inductance of the transformer to provide ZVS for both the switches.

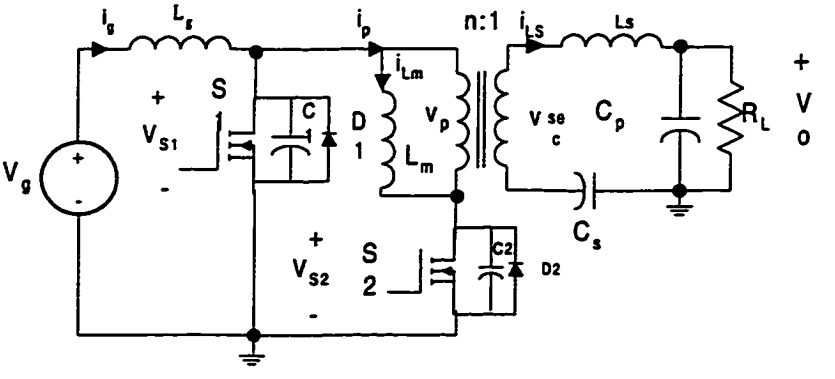

Figure 1.5 Boost derived resonant dc-to-ac inverter proposed

The closed loop circuit for this inverter is frequency modulated, as ZVS is hard to maintain with the PWM approach under greater load variations. The voltage -controlled

oscillator is used in place of the PWM circuit to achieve the desired control maintaining the resonance.

For the above described dc-to-dc converters and dc-to-ac inverter, mathematical analysis, PSPICE simulation and experimental results will be presented. Comparison of the theoretical, simulation and experimental results will be made.

Chapter 2 outlines the steady-state waveforms, principle of operation of the three dc-to-dc converter topologies. Chapter 3 explains the simulation and experimental waveforms for the three dc-to-dc converters. Comparison of the important parameters for the three topologies is given in this chapter. Chapter 4 gives the dc-to-ac inverter steady-state analysis with waveforms. A steady-state mathematical model is presented along with the sinusoidal approximations. Performance curves of the inverter is presented that are used to present a detailed design procedure for an example of the inverter. The simulation and experimental results for the inverter topology will be given in Chapter 5. A table making comparison between the simulation and experimental results. Chapter 6 shows the small signal model developed for the dc-to-ac inverter. The frequency response plots of the input-to-output and control-to-output transfer functions are given for various load conditions. Conclusions are made, for the proposed improved resonant power converters, in Chapter 7.

CHAPTER 2

FAMILY OF ISOLATED DC-TO-DC ZERO-VOLTAGE SWITCHING CONVERTERS

2.1 Introduction

Electrical isolation between the input and output load is required in many power electronics applications. High frequency transformers in series with a switch are used to achieve this requirement. The challenge with implementing this method is the saturation problem of the transformer. This requires core resetting when the series switch is off which results in higher voltage stress across the switch and higher turn-off loss [23]. This is due to the energy stored in the transformer. An additional reset circuit with voltage clamp will reduce the voltage stress across the secondary switch.

Zero-voltage switching (ZVS) isolated boost converters are analyzed and investigated in this chapter. The magnetizing inductance of the isolation transformer and the parasitic capacitance of the switches resonate to provide ZVS for the secondary switches. The steady-state analysis will be presented to explain the circuit operation. The converters are simulated using PSPICE. The simulation and experimental results of these three converters are presented and performance comparison is done in Chapter 3.

2.2 Topology 1: Basic isolated boost converter

Figure 2.1 shows the circuit for the basic isolated boost converter. A series switch S_2 is connected in series with the isolation transformer to allow core resetting. Switch S_1 is the primary switch of the boost converter shown. The magnetizing inductance L_m of the transformer resonates with the parasitic capacitance C2 of switch S2 to provide ZVS for S_2. The transformer provides energy transfer from the input inductor L_g to the output.

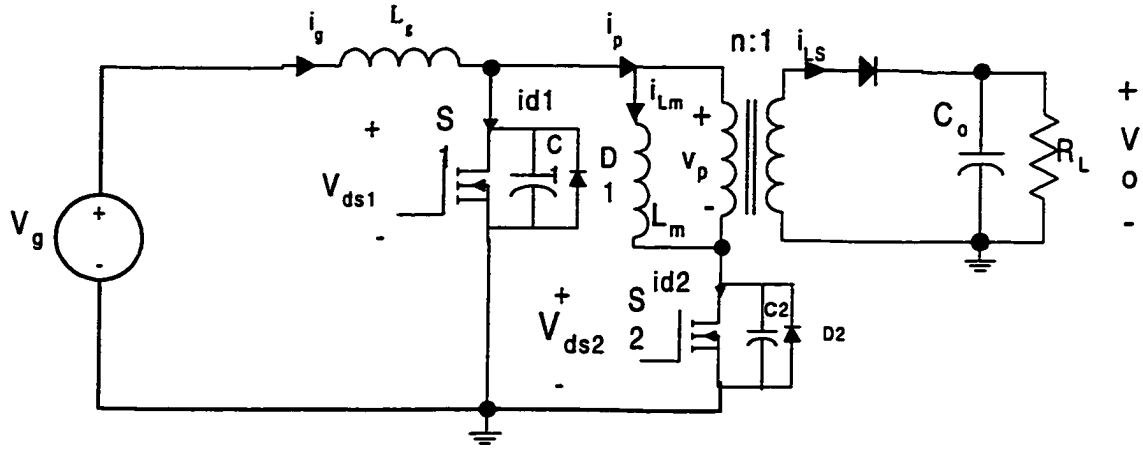

Figure 2.1 Basic isolated boost converter

The steady-state waveforms for this converter are shown in Figure 2.2.

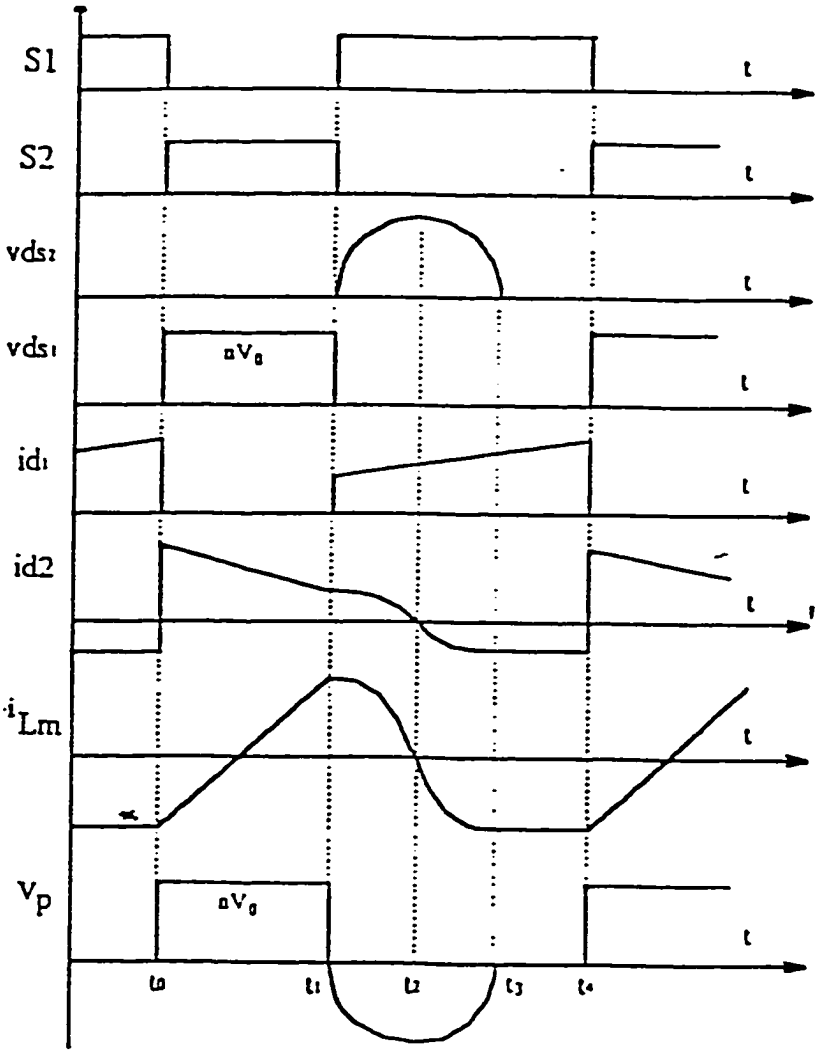

Figure 2.2 Steady state waveforms of the basic isolated boost converter

Switch S_2 turns on at t_0 and v_{ds1} reaches its maximum value of nV_o and goes to zero when S_1 turns on at t_1. During this time v_{ds2} remains at zero. At t_1 v_{ds2} resonates sinusoidally to its maximum and goes down to zero at time t_3. At this time diode D_2 turns on and clamps the v_{ds2} at zero and current iL_m remains at its

negative minimum. At time t_4, S_2 turns on again and starts another cycle of the converter where i_{Lm} increases back to its positive maximum.

By equating magnetizing energy equal to energy storage in C_2, the maximum voltage stress $V_{ds2,max}$, is given by,

$$V_{ds\,2.max} = n\pi V_0 (1 - D) \frac{\omega_o}{\omega_s}$$

where ω_s and ω_o are the switching and radial resonant frequencies defined as,

$$\omega_S = \frac{T_S}{2\pi}, \quad \omega_O = \sqrt{\frac{1}{L_m C_2}}$$

The condition on ZVS operation for S_2 is expressed by

$$\frac{\omega_s}{\omega_o} \leq 2D \qquad (2.2)$$

From Equation (2.2), it is seen that S_2 operates at ZVS for a certain of duty cycle D and S_1 operates with hard switching which causes high switching losses. The disadvantage with this converter is that, it is difficult to keep S_2 operating with ZVS and keep the voltage it to a minimum over a wide load range [11].

2.2.1 Modes of Operation

Mode I : $t_0 < t < t_1$ [S_2 ON , S_1 OFF]

There are four modes of operation over one switching cycle as discussed below. Voltage across S_1 is nVo (reflected output voltage where n is the isolating transformer turns ratio). Current i_{d2} flows through S_2 and diode D_2 is not "on". Magnetizing current i_{Lm} is increasing linearly and i_{d2} is decreasing linearly.

Mode II : $t_1 < t < t_2$ [S_1 ON , S_2 OFF]

Input inductor L_m and C_2 resonate causing voltage across S_2 v_{ds2} to increase sinusoidally and reaching its peak at t_3. Current through S_1 ramps up sinusoidally and i_{Lm} decreases sinusoidally.

Mode III : $t_2 < t < t3$ [S_1 ON, S_2 OFF]

Voltage across S_2 decreases from maximum to zero sinusoidally at t_3. i_{Lm} is decreasing to its negative maximum. Here the magnetizing current is changing polarity which resets the output isolating transformer core (avoids saturation of transformer core).

Mode IV : $t_3 < t < t_4$ [S_1 ON , S_2 OFF]

Diode D_2 turns "on" as voltage across S_2 is zero and current across it is negative. This clamps the voltage v_{ds2} to zero providing Zero-voltage-switching (ZVS) for switch S_2. The proper duty cycle design of this converter is critical to ensure the ZVS for S_2. There should be enough time for the positive half of the sinusoid of v_{ds2} to come back to zero to ensure that the voltage across S_2 is zero when it is turned "on" in the next cycle.

2.3 Topology 2: Modified ZVS boost converter with active clamp circuit

Figure 2.3 shows the modified boost converter with clamp circuit. S_a, D_3, D_4 and C_B form the clamp circuit to reduce the voltage across S_2. There is inclusion of an additional switch, which makes this converter more complex and costly [17].

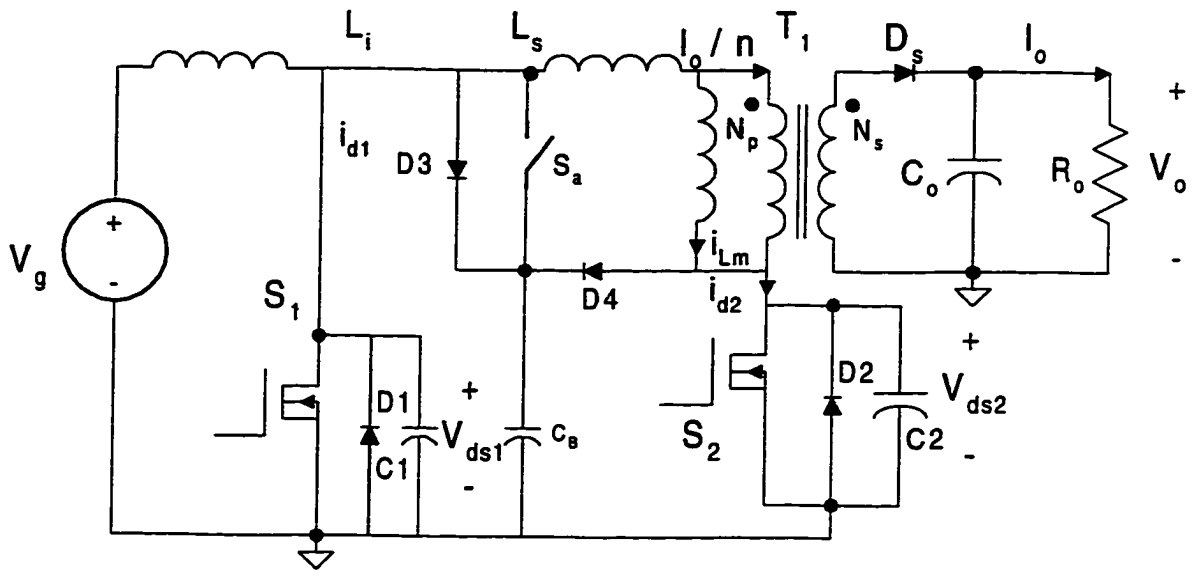

Figure 2.3 Modified boost converter with clamp circuit

Figure 2.4 shows the typical waveforms of the modified boost converter showing the clamped voltage across S_2.

2.3.1 Modes of operation

Mode I : $t_0 < t < t_1$ [S_1 OFF, S_2 and S_a ON]

During t_0-t_1, S_1 is turned off and S_2 and S_a are turned on. The excess energy stored in C_B can is delivered to the output through the transformer so that the voltage across C_B can be balanced.

Mode II : $t_1 < t < t_2$ [S_1 ON, S_2 and S_a OFF]

At time t_1, S_1 is turned on and S_2 turned off. The magnetizing current i_{Lm} sinusoidally decreases, due to the resonance between the magnetizing inductance L_m and C_2, and during this time the input inductor current decreases through S_1.

The magnetizing current i_{Lm} charges C_2 which causes vds2 to increase sinusoidally and will be clamped by voltage C_B at t_2, where D_4 starts conducting.

Mode III : $t_2 < t < t_4$ [S_1 ON, S_2 and S_a OFF]

After t_2, the magnetizing current decreases linearly since a negative nV_o is applied to the primary winding of the transformer. Voltage across S_2 decreases to zero at t_4 and i_{Lm} flows through D_2 at its negative maximum constant value. Consequently S_2 is turned on at zero-voltage.

Mode IV : $t_4 < t < t_5$ [S_1 ON, S_2 and S_a OFF]

Current i_{d2} is at negative maximum and i_{Lm} is constant at negative maximum. Voltage across S_2 is clamped at zero by diode D_2. S_1 is turned off at t_5 while S_2 and S_a are turned on. V_{ds1} is clamped to V_{CB} and then clamped to the reflected output voltage nV_o. Without C_B and D_3, V_{ds1} would have high ringing transient voltage due to the resonance between parasitic capacitance C_1 and the leakage inductance of the transformer. From Figure 2.6, it is observed that S_2 can be operated at ZVS while S_1 is still hard switched.

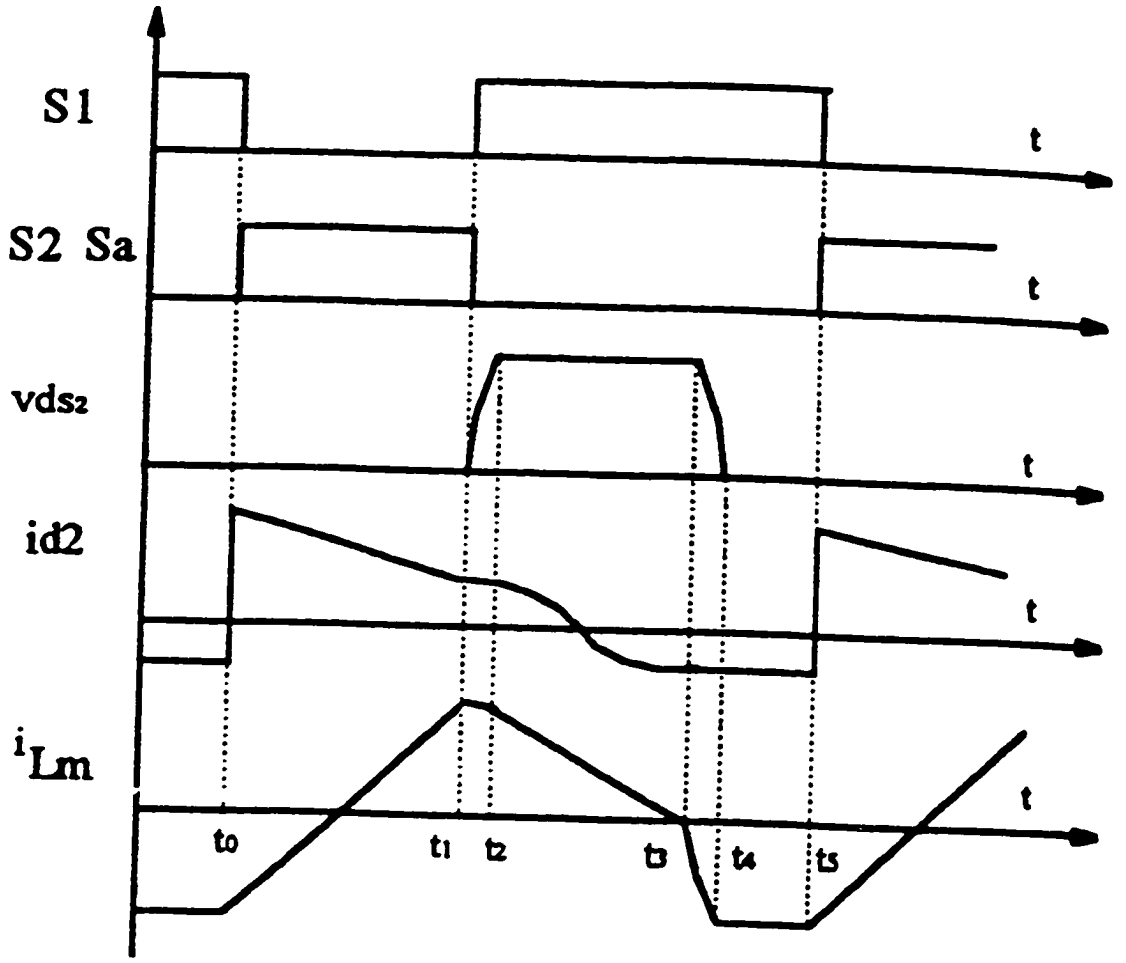

Figure 2.4 Steady state waveforms for modified boost converter with clamp circuit.

2.4 Topology 3: Modified boost converter with network on the output side

The next topology is a modified boost converter with a network on the output side of the transformer. An extra winding N_r and a diode D_r network is introduced for transformer core resetting. This also suppresses the voltage stress across S_2 and transfers partial magnetizing energy to the output. The network consists of a resonant inductor L_r, an auxiliary switch S_a, diode D_a and resonant capacitor C_r. This network is implemented to achieve ZVS for switch S_1. Figure 2.5 shows the circuit diagram of this converter.

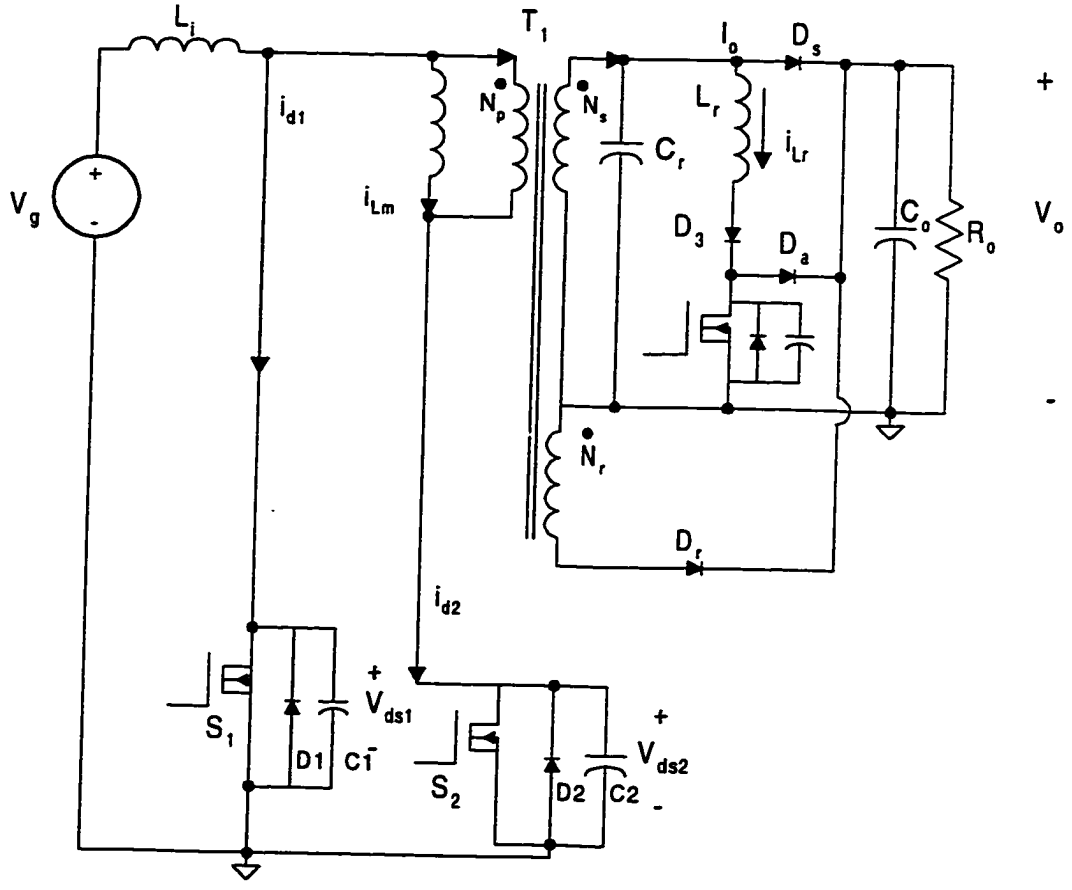

Figure 2.5 Modified ZVS boost converter with a small diode network at the output stage.

The steady-state waveforms for this converter are shown in Figure 2.6 below. At time t_1, the auxiliary switch S_a is turned on. The duration of time from t_1 to t_2 is given by

$$t_2 - t_1 = \frac{I_o}{V_o / L_r}$$

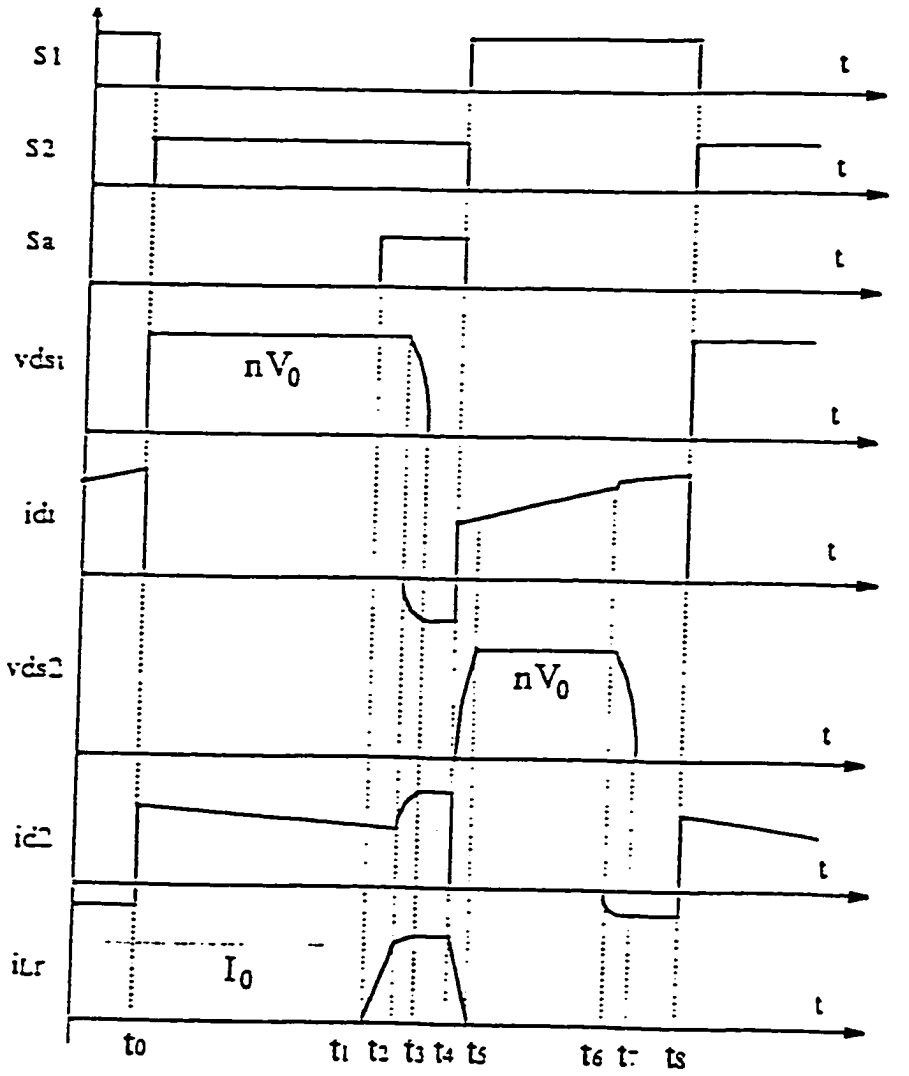

Figure 2.6 Steady state waveforms for the modified boost converter with an output network

The current through the inductor L_r increases linearly upto I_o while the current through D_S decreases linearly and D_S will be naturally turned off at t_2 when $i_{Lr} = I_o$. The current through the resonant inductor L_r increases sinusoidally while the resonant capacitor C_r discharges during this period. C_r comprises of the output capacitance of S_1 , the junction capacitance of diode D_S . The resonant voltage and current can be expressed as

$$v_{cr} = V_o \cos \omega_{o2}(t - t_2) \tag{2.3}$$

$$i_{Lr} = I_o + \frac{V_o}{Z_o} \sin \omega_{o2}(t - t_2) \tag{2.4}$$

where $\omega_{o2}=1/\sqrt{L_rC_r}$ and $Z_o = \sqrt{\frac{L_r}{C_r}}$. Energy stored in these parasitic capacitors is completely transferred to the inductor L_r at t_3, where the voltage across C_r and D_1 decrease to zero and D_1 begins to conduct. The resonant inductor current i_{Lr} flows through the secondary winding at a constant value. In order to achieve ZVS, the turn-on gate signal S1 should be applied during this period. Both switches operate at ZVS reducing switching losses. It is seen that ZVS is achieved for S_1 with the help of L_r , S_a , and C_r while ZVS of S_2 is achieved by resonance of L_m and C_2 . The voltage across S_2 is clamped to nV_o through the extra secondary winding N_r and D_r [17].

2.4.1 Modes of operation

Mode I $t_0 < t < t_1$

In steady state, there are eight modes of operation as discussed below. S_2 is turned on and S_1 is turned off at t_0. Diode D_S is on while clamp diode D_r is off. Power is transferred to the output through the transformer in this mode. The duration of this mode is given by $t_{1-2} = \frac{I_o}{V_o / L_r}$

Mode II $t_1 < t < t_2$

At t1 auxiliary switch S_a is turned on. The current through L_r ramps up linearly until it becomes equal to I_o at time t_2, where diode D_S will be turned off.

Mode III $t_2 < t < t_3$

Inductor L_r and capacitor C_r start to resonate at time t_2. Current through L_r increases in sinusoidal form while voltage across C_r decreases. At t3, voltages v_{cr} and v_{ds2} decrease to zero and body diode D_1 turns on to clamp the voltage across S_2 to zero. The duration of this mode is determined by

$$t_{2-3} = \frac{\pi}{2}\sqrt{L_r C_r} \qquad where\ C_r = C_1 + C_{tr} + C_j$$

$C1 = capacitance\ of\ switch\ S_1$

$C_{tr} = capacitance\ of\ the\ transformer$

$C_j\ is\ the\ junction\ capacitance\ of\ the\ D_S$

Mode IV $t_3 < t < t_4$

Body diode D1 of switch S1 is on. The switch S1 is turned on during this time to achieve ZVS.

Mode V $t_4 < t < t_5$

At t_4, S_2 and S_a are turned off when S_1 is turned on. Current through L_r decreases to zero while voltage across S_a clamps to V_o due to D_a being on. Magnetizing current iLm linearly charges C2 capacitor. This mode is on until t_5 when v_{ds2} ramps up to nV_o, when D_r turns on at ZVS.

Mode VI $t_5 < t < t_6$

When D_r is on at t_5, the voltage across S_2 clamps to nV_o. Energy stored in L_m is transferred to the load through winding N_r and diode D_r. This mode stays on until i_{Lm} becomes zero when L_m and C_2 start to resonate.

Mode VII $t_6 < t < t_7$

When L_m and C_2 start to resonate, at t_6, the energy is transferred from C_2 to L_m, which makes i_{Lm} negative at t_7. Time t_7 is determined by the time taken for vds2 to go to zero.

Mode VIII $t_7 < t < t_8$

At t_7, v_{ds2} is zero and diode D_2 turns on. This makes i_{Lm} a constant in this mode. Therefore, switch S_2 operates at ZVS when it turns on at t_8 [11].

CHAPTER 3

SIMULATION AND EXPERIMENTAL RESULTS FOR THE DC-TO-DC CONVERTER TOPOLOGIES

In this chapter, we will give the detailed simulation and experimental results for the three dc-to-dc topologies discussed in chapter 2. In these circuits, in order to simplify, we use a constant input V_g. The line current is in continuous conduction modes and can be programmed to achieve unity power factor.

3.1 Basic Isolated Boost converter

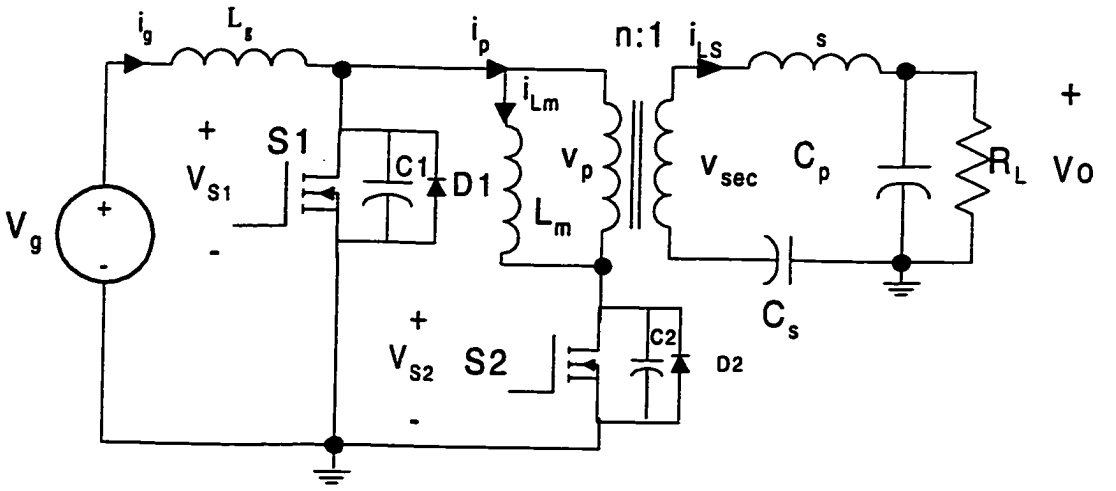

Figure 3.1 Basic isolated boost converter

3.1.1 Simulation results

The simulation results for the basic converter shown in Figure 2.1 is shown in Figure 3.2. The voltage across S_2 is high with ZVS and S_1 is hard switched by high frequency ringing voltage after S_1 is turned off. Magnetizing current I_{Lm} changes polarity to ensure transformer core resetting by varying from its positive maximum to its negative minimum and back.

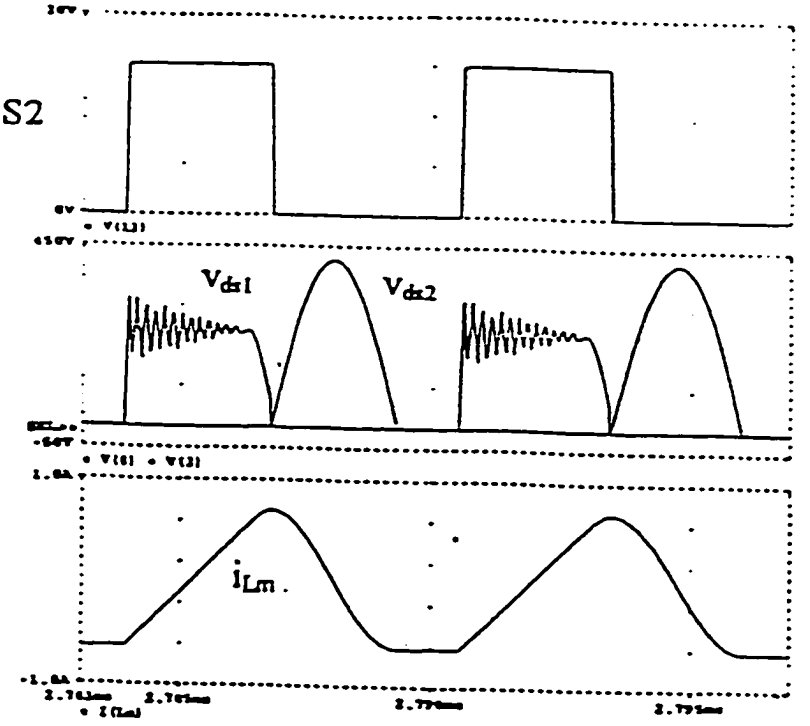

Figure 3.2 Simulation results for the isolated boost converter

3.1.2 Experimental Results

Let us consider a specific design example with the following design specifications:

V_o=200V	Lm=415uH	Lg=380μH
C1=C2=1.15nF	Co=650μF	Ro=400Ω

n=15/14

The experimental waveforms for the basic isolated boost converter are shown in Figure 3.3. The experimental waveforms closely match the simulation results.

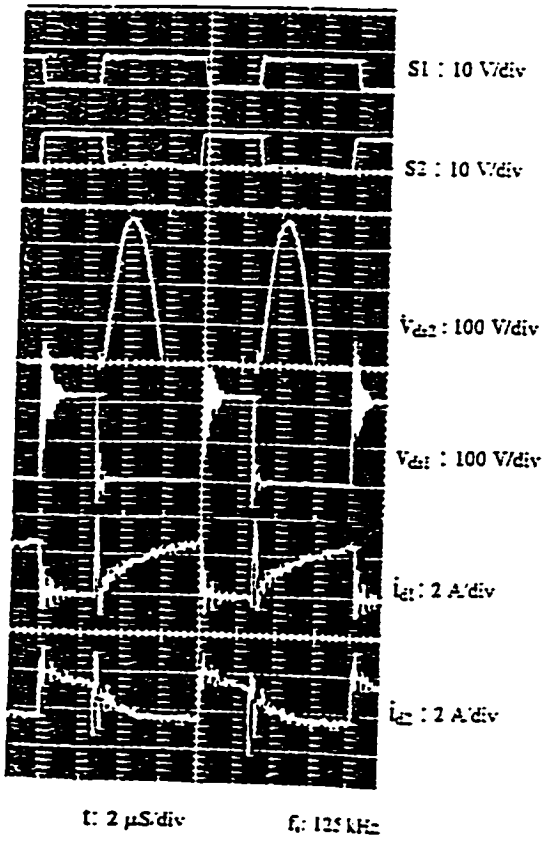

Figure 3.3 Experimental Waveforms for the isolated boost converter

3.2 Modified boost converter with active clamp circuit

The modified boost converter with active clamp circuit is shown below in Figure 3.4.

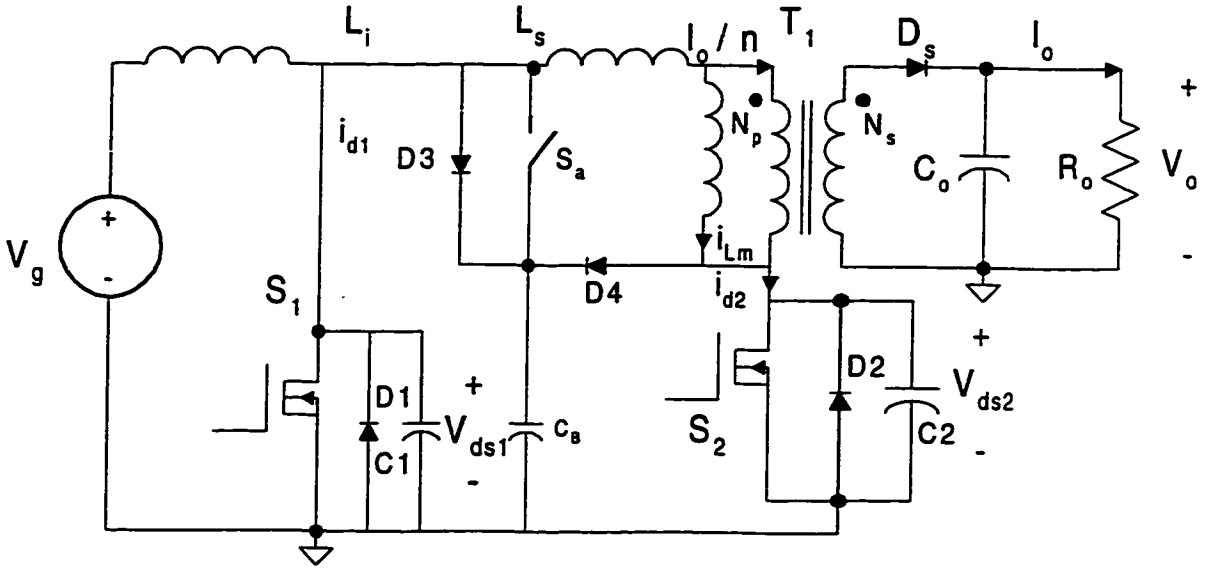

Figure 3.4 Modified boost converter with active clamp circuit

3.2.1 Simulation results

The simulation waveforms for this modified boost converter with active clamp is shown in Figure 3.5. It is seen that the volatge across S_1 is hard switched while operating S_2 at ZVS. The low frequency ringing current in i_{d2} is due to the discharge of capacitor C_B through the leakage inductance to the load. The voltage v_{ds2} is clamped to the reflected output voltage n V_o. The complementary switching of the two switches is seen and the input current is continuous as expected from the designed converter.

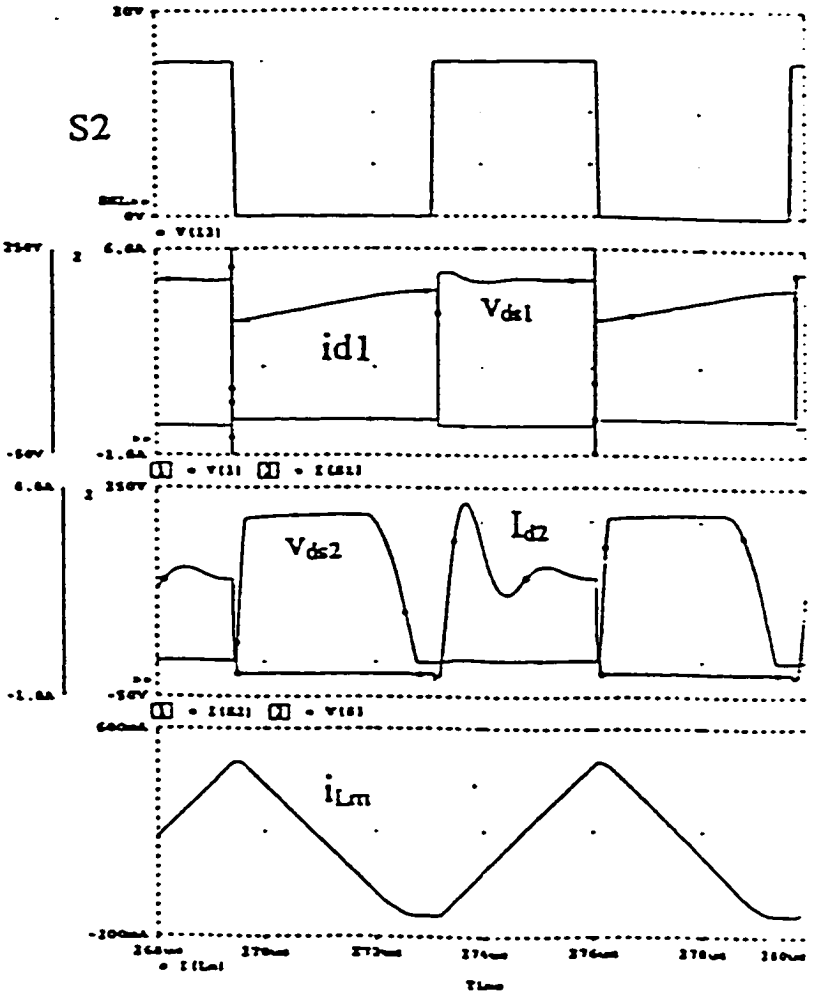

Figure 3.5 Simulation waveforms for the modified boost converter with active clamp.

3.2.2 Experimental results

Let us consider a specific design example with the following design specifications:

V_o=200V	Lm=535uH	Lg=380μH	C2=680pF
Co=650μF	Ro=400Ω	n=15/12	f_S = 150kHz

The experimental waveforms for the basic isolated boost converter are shown in Figure 3.6.

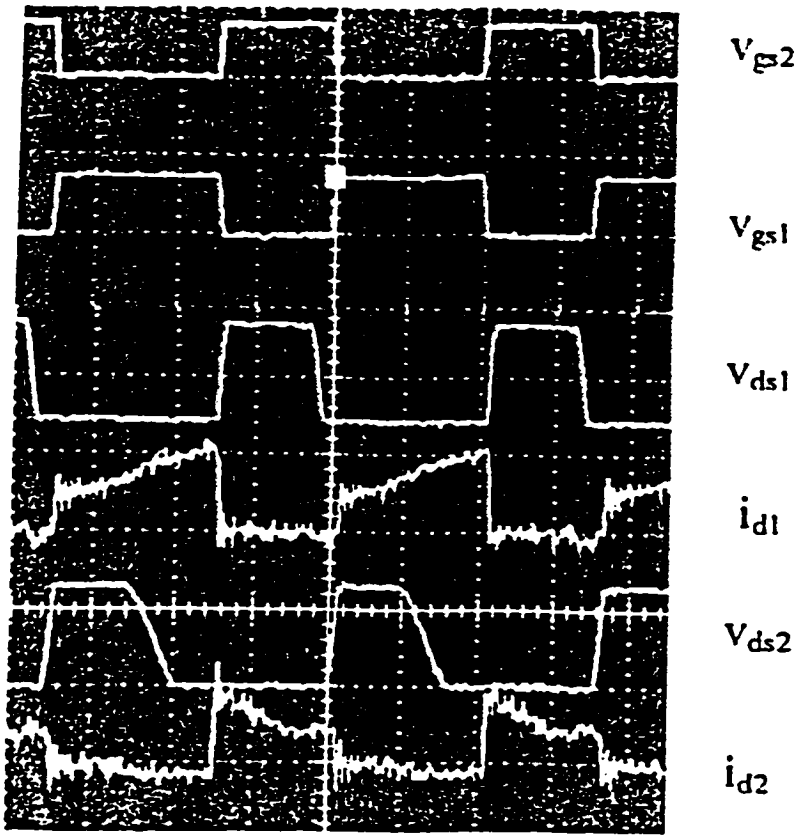

Figure 3.6 Experimental results for the modified converter with active clamp circuit

3.3 Modified boost converter with output network

The modified boost converter with output network is shown below in figure 3.7

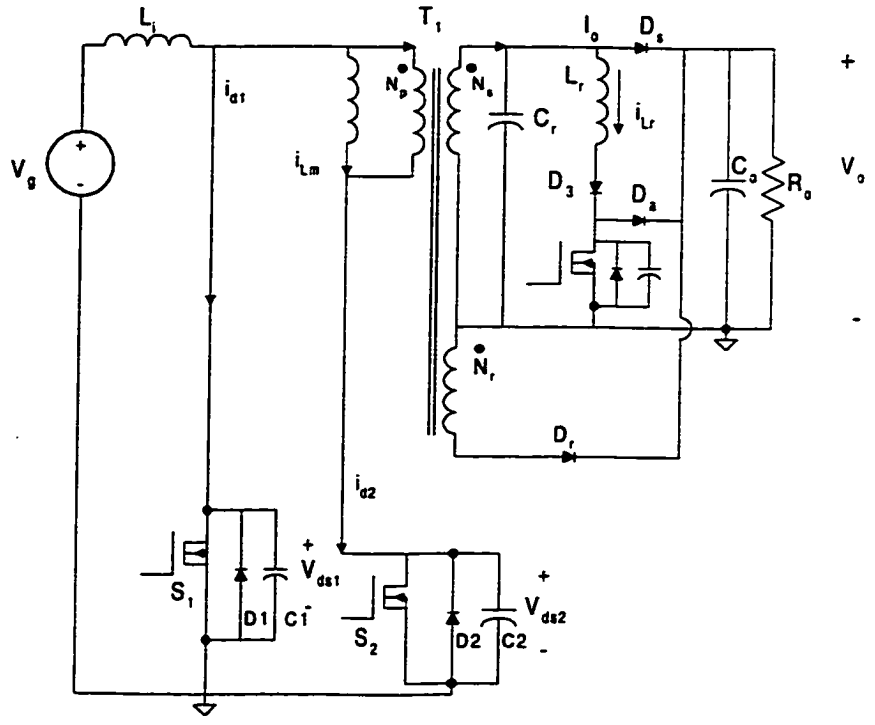

Figure 3.7 Modified ZVS boost converter with a small diode network at the output stage.

3.3.1 Simulation Results

Simulation results for this topology is shown in Figure 3.8. Voltage v_{dS1} is not ringing compared to the basic isolated boost converter. A high current pulse i_{d2} exists during the transition period. Both S_1 and S_2 are operating at Zero-voltage-switching. Most of the waveforms compare to the basic boost topology except

during the transition time when i_{d2} is a high current pulse compared to the basic topology.

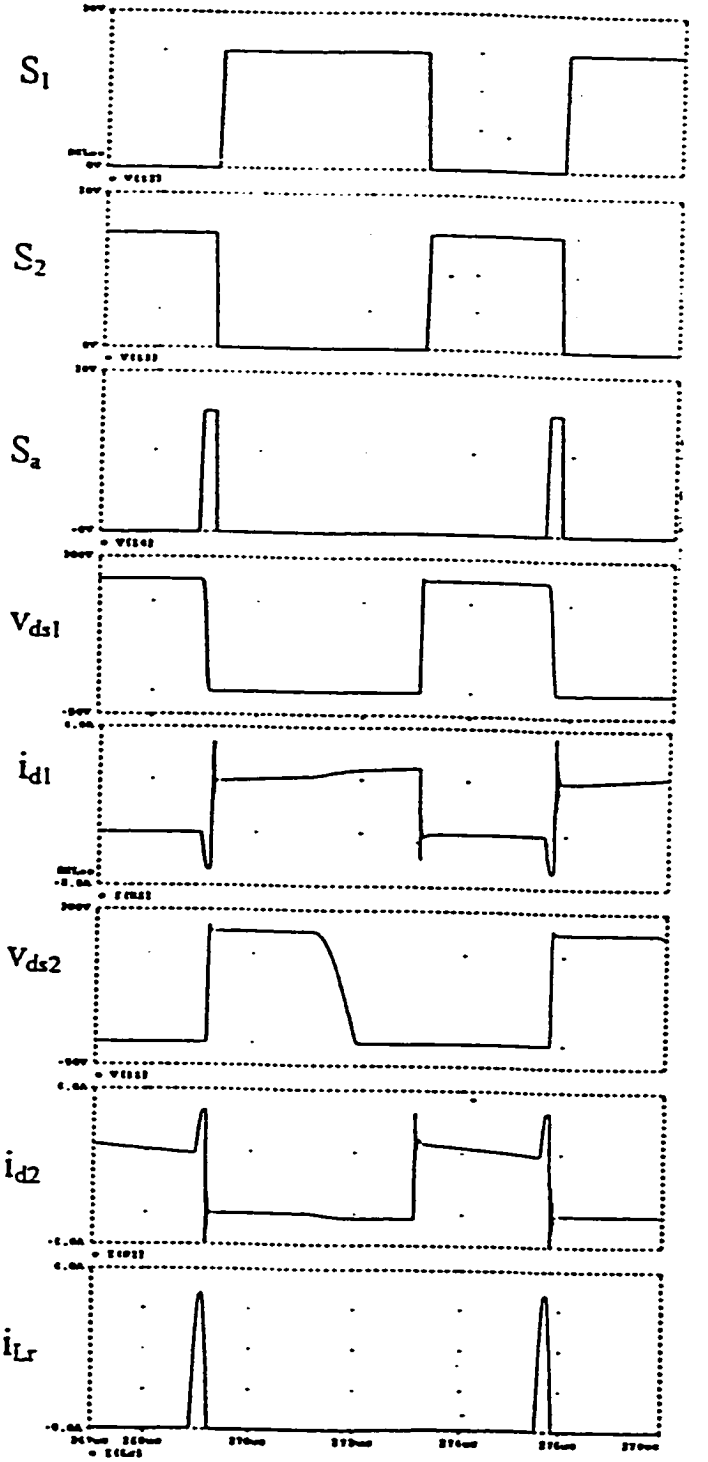

Figure 3.8 Simulation results for modified boost converter with output network

3.3.2 Experimental Results

Specifications:

Lm=535μH Lr=6μH C1=C2=450pF Ro=266Ω

Co=650μH n=15/14 fs=150kHz

The experimental waveforms for the modified boost converter with output network are shown below in Figure 3.9.

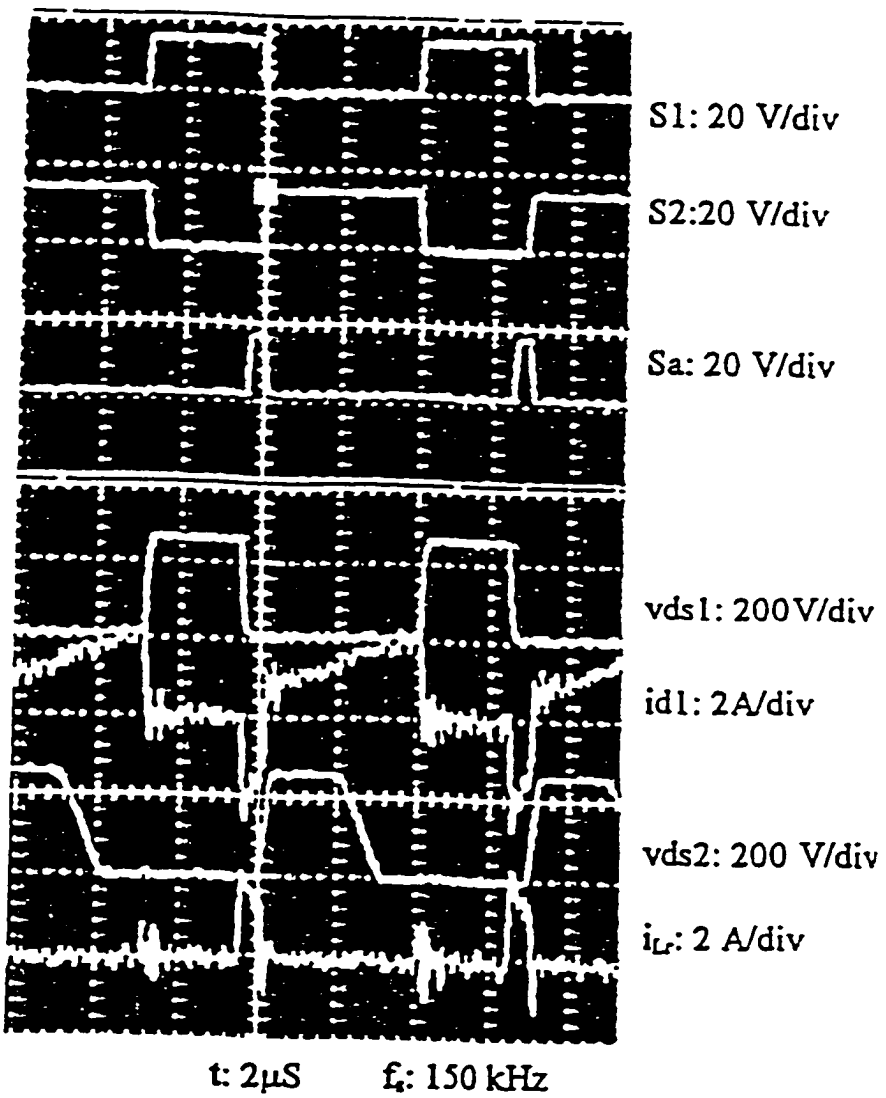

Figure 3.9 Experimental Waveforms for the modified boost converter with output network

Both switches operate at ZVS with minimized voltage stresses. The converter efficiency is 92% with less power loss.

3.4 Comparison of the three topologies

Tables 3.1 and 3.2 summarize the parameters of comparison for the three converters for voltage and current stresses, respectively.

Table 3.1: Voltage Stress of switches

Topology / Switch	*Basic Converter Fig. (3.1)*	*Converter with active clamp. Fig. (3.4)*	*Converter with output network. Fig. (3.7)*
S_1	nV_o *high freq. Ringing*	nV_0	nV_o
S_2	$nV_o(1-D)f_o/f_s$	nV_o	nV_o
S_a	*NA*	nV_o	nV_o

Table 3.2: Current Stress through switches

Switch / Topology	*Basic Converter Fig. (3.1)*	*Converter with active clamp. Fig. (3.4)*	*Converter with output network. Fig. (3.7)*
S_1	$I_i + \frac{DV_sT_s}{2L_i}$	$I_i + \frac{DV_sT_s}{2L_i}$	$I_i + \frac{DV_sT_s}{2L_i}$
S_2	$I_i + \frac{DV_sT_s}{2L_i}$	$I_i + \frac{DV_sT_s}{2L_i} + I_{CB}$	$I_i + \frac{DV_sT_s}{2L_i} + V_o\sqrt{\frac{C_r}{L_r}}$
S_a	*NA*	I_{CB}	$I_o + V_o\sqrt{\frac{C_r}{L_r}}$

Table 3.3 compares the performance of these topologies with respect to soft-switching and complexity.

Table 3.3: Soft switching, complexity and efficiency

Topology / *Parameter*	*Basic Converter Fig. (3.1)*	*Converter with active clamp. Fig. (3.4)*	*Converter with output network. Fig. (3.7)*
Switch : S_1	*Hard switched*	*Hard switched*	*ZVS*
S_2	*ZVS*	*ZVS*	*ZVS*
S_a	*NA*	*ZCS*	*ZCS*
Circuit Complexity	*Simple*	*Medium*	*Medium*
Efficiency	*Medium*	*Medium*	*Higher*

3.4.1 Basic Isolated Boost Converter

The disadvantage of this converter is higher switching losses and high voltage stress due to hard switching of S_1 and resonance between the magnetizing inductance and parasitic capacitance of switch S_2. Switch S_2 may lose its soft switching ability due to an incorrect duty ratio. To keep S_2 in soft switching mode over a wide range, S_2 may be subjected to significant voltage stress. This is a simple configuration with lower cost. The efficiency is about 88%.

3.4.2 Modified Boost Converter with active clamp circuit

This configuration has less voltage stress on switch S_2 because of the active clamp circuit. The voltage across S_2 is clamped at the reflected output voltage nV_o (n is transformer turns ratio). There is an added current stress in i_{d2} due to the low frequency ringing current caused by the discharge of C_B through the leakage inductance to the load.

3.4.3 Modified Boost Converter with output network

The converter has a small network in parallel with the secondary winding of the transformer. The switches operate at lower voltage stresses compared to the other topologies. The parasitic components such as output capaictance of the switches, leakage inductance, winding capacitance of the transformer and junction capacitance of the diodes can be used a part of the resonance design. The efficiency of this converter is about 92%.

From Table 3.1 we see that the basic converter has high frequency ringing across the main switch equal to the reflected output voltage. This is the same value for the other two topologies but without ringing. The same reflected output voltage is the stress across the auxiliary switch in the converters in Fig. (3.4) and (3.7). There is no auxiliary switch for the basic boost converter. The current stresses are shown in Table 3.2 for the three converters. The current stresses for the two switches is the same for the basic topology in Fig. (3.1). For the topology with active clamp in Fig. (3.4) a little more current stress than the basic topology is present to provide current to capacitor CB for the second switch. The current stress for the main switch is the same. The topology with output network has added current stress compared to the basic topology for the second switch. This added

current is used, by the resonant tank circuit, in the output side of the converter transformer for the converter in Fig. (3.7). The main switch of the basic converter and the converter with active clamp is hard-switched while the second switch achieves ZVS. The auxiliary switch for the converter with active clamp achieves ZCS. The converter with output network in fig. (3.7) has all three switches that are soft-switched. The circuit complexity and efficiency for the converter with output network is higher compared to the basic converter and the converter with active clamp.

CHAPTER 4

DC-TO-AC RESONANT ZERO VOLTAGE SWITCHING INVERTER

4.1. Introduction

There is a pressing demand to design off-line ac inverters with Zero-Voltage-Switching (ZVS) and electrical isolation with improved power factor. The topology proposed can be used for power factor correction because the input current, is the inductor current, can be programmed. Research activities, in the design and development of high power-factor correction circuits, continue to grow since mid 1980's. As the use of non-linear loads in today's electronic systems continues to increase, utility power systems continue to suffer from low power factor [4,16,23]. Over the last ten years, different converter topologies (passive and active) have been introduced to serve as an interface module between the ac mains and non-linear loads to enhance power factor [3-14]. Recent research emphasis is focused on the active power factor correction because of their many advantages over the passive ones. The commonly used PWM active power-factor correction circuits are the buck, boost and buck-boost [6]. Unlike the buck and buck-boost, the boost converter topology is the most commonly used topology to improve power factor since it draws a continuous input current from the mains. This topology has limited application due to the absence of an isolation transformer at the output side and low frequency of operation. This disadvantage is avoided in the push-pull configuration when a three winding transformer is used.

A new modified dc-to-ac converter with ZVS and output electrical isolation was first introduced in [11]. In this paper, using sinusoidal approximation, a new set of characteristic curves and a design procedure are presented. Compared to the conventional inverters, this inverter has several advantages including output isolation, ZVS of all power switches, low EMI radiation. In electronic ballast designed for high frequency gas-discharged lamps, the new converter reduces the acoustic phenomena in high intensity gas discharged lamps. Since a frequency modulation technique is applied in this converter for both controlling power flow and avoiding the acoustic phenomena to be observable. In Section 4.2, the basic circuit operation and the corresponding circuit modes are presented. The state-space equations for the steady state models are given in Section 4.3 and the sinusoidal approximation technique is given in Section 4.4.

4.2. Basic Circuit Operation

Figure 4.1 shows the simplified dc-to-ac converter circuit with output isolation and zero-voltage-switching (ZVS).

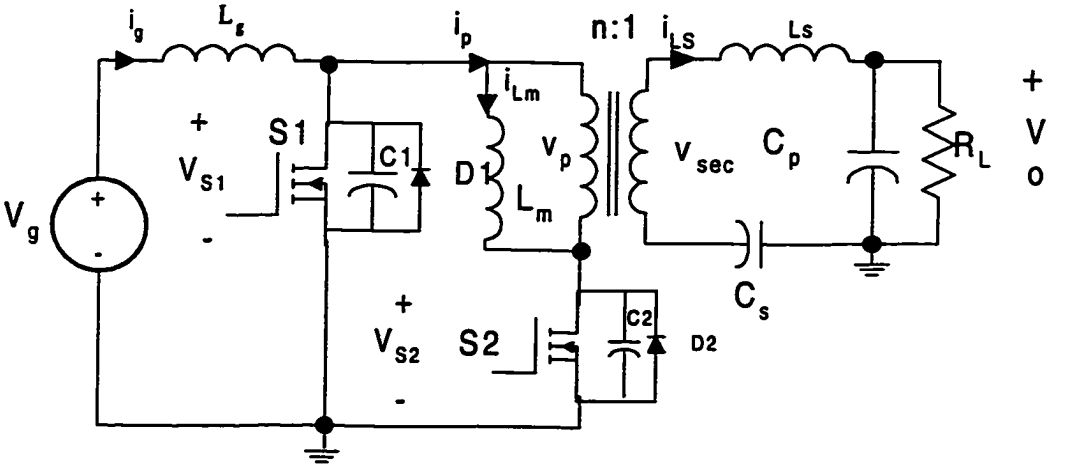

Fig. 4.1 DC-to-AC ZVS converter with isolation

The input inductor L_g is the main inductor with two MOSFET's S_1 and S_2 switching in complementary fashion. The capacitors C_1 and C_2 maybe used as the MOSFET's parasitic capacitance, and inductor L_m is the transformer magnetizing inductance. The components C_p, C_s and L_s form the output resonant tank circuit that selects the output frequency and provides the resonance behavior to achieve ZVS for S_1 and S_2.

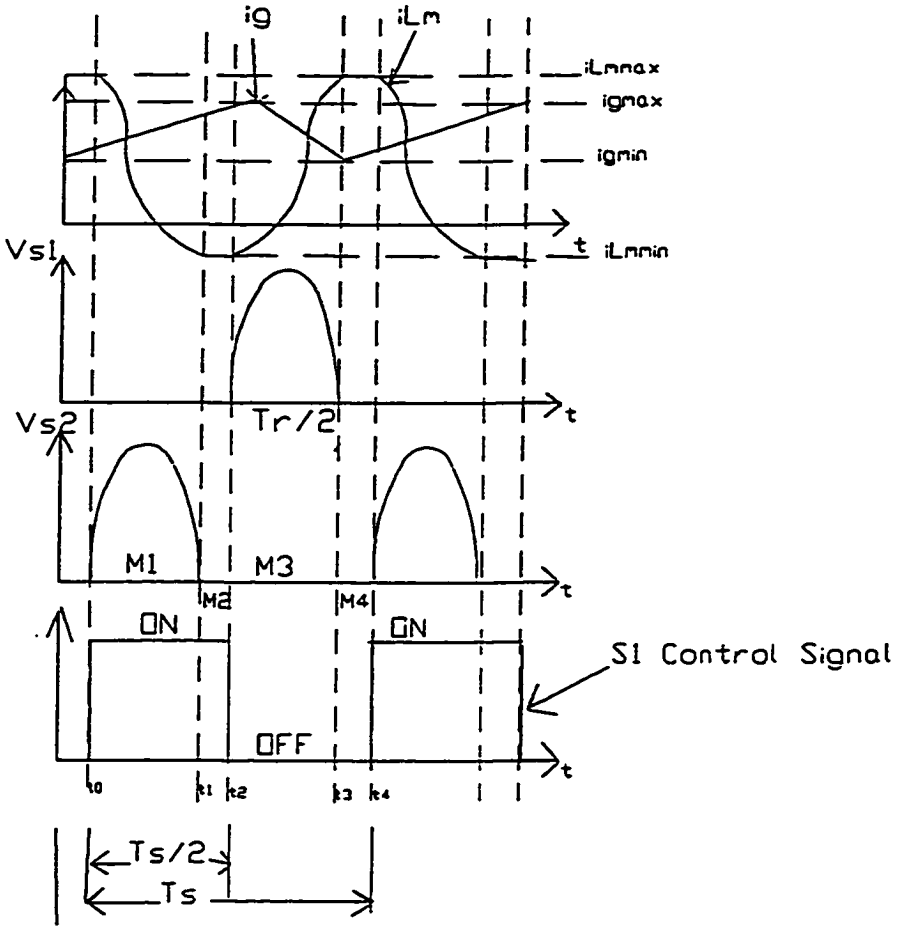

Fig. 4.2 Typical steady state waveforms

Figure 4.2 shows typical steady state waveforms of the input current, i_g, transformer magnetization current, i_{Lm}, the voltage across shunt switch S_1, v_{S1}, the voltage across switch S_2, v_{S2}, and the driving signal for switch S_1. The different modes of the circuit operating condition are shown in Fig. 4.3.

The basic circuit operation can be discussed as follows: At time t_0, assuming steady state of the converter is in mode M1, S_1 is turned on and S_2 is turned-off, causing L_m, C_2 to form a resonant tank circuit across the transformer primary side. From t_0 to t_1, the magnetization current sinusoidally drops from its positive peak, $I_{Lm,max}$, to its negative peak $I_{Lm,min}$. In Fig. 4.2, we define T_r as the resonant period of the tank circuit formed by C_1-C_2-L_m-C_S-C_P-L_S. Also within this time interval, v_{S2} resonates sinusoidally for half a cycle to t_1 while S_1 is on. When v_{S2} decreases to zero at time t_1, the circuit mode changes from M1 to M2. In mode M2, diode D_2 conducts with v_{S2} clamped to zero voltage and i_{Lm} at its minimum, $I_{Lm,min}$, providing zero-voltage turn-on condition for D_2. This mode remains till time t_2, entering mode M3 when switch S_1 is turned off and S_2 turned on. From t_2 to t_3 S_1 is turned-off and S_2 turned-on, resulting in the buildup of sinusoidal voltage across capacitor C_1 from zero to its positive peak and back to zero again. During this time interval, the magnetization current, i_{Lm}, sinusoidally increases from its negative minimum, crosses zero, and reaches its positive maximum. At time t_2, i_g increases sinusoidally until v_{s1} becomes equal to V_g, and then for $v_{S1}>v_g$, i_g decreases nonlinearly until the time when v_{S1} becomes less than V_g when i_g increases non-linearly again, until time t_3 when v_{s1} reaches zero. At $t = t_3$, v_{s1} becomes zero, turning on D_1, while i_{Lm} is positive entering the circuit mode M4, in which i_{Lm} is maintained constant at its positive maximum. The voltage v_{S1} remains at zero allowing zero-voltage turn-on for S_1. The switching cycle repeats again at $t_4 = T_S + t_0$ when S_1 is turned on and S_2 is turned off.

4.3. Steady State Mathematical Model

In order to solve for the steady state response, the mathematical models for the four circuit modes of operation must be derived. The Transformer ratio is given by $n=N_2/N_1$. In this section, we provide mathematical model that must be solved to obtain the steady state response for the four modes given in Fig. 4.3.

Mode 1: ($t_0 \le t < t_1$):

In this mode, S_1 is on, S_2 is off, resulting in state variable Eq. (4.1). We should point out that when a switch is on, it implies that either the main switch is on or its fly-back diode D_1 is on. In order to simplify the analysis, we assumed that the input current, i_g, is constant represented as I_g. Hence, this topology may be referred to as a current driven dc-to-ac converter [11].

$$\frac{d}{dt}\begin{bmatrix} vC1 \\ vC2 \\ vCS \\ vCP \\ iLS \\ iLm \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_2} & \frac{1}{C_2} \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p R_o} & \frac{n^2}{C_p} & 0 \\ 0 & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & 0 & 0 \\ 0 & -\frac{1}{L_m} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} vC1 \\ vC2 \\ vCS \\ vCP \\ iLS \\ iLm \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} I_g \qquad (4.1)$$

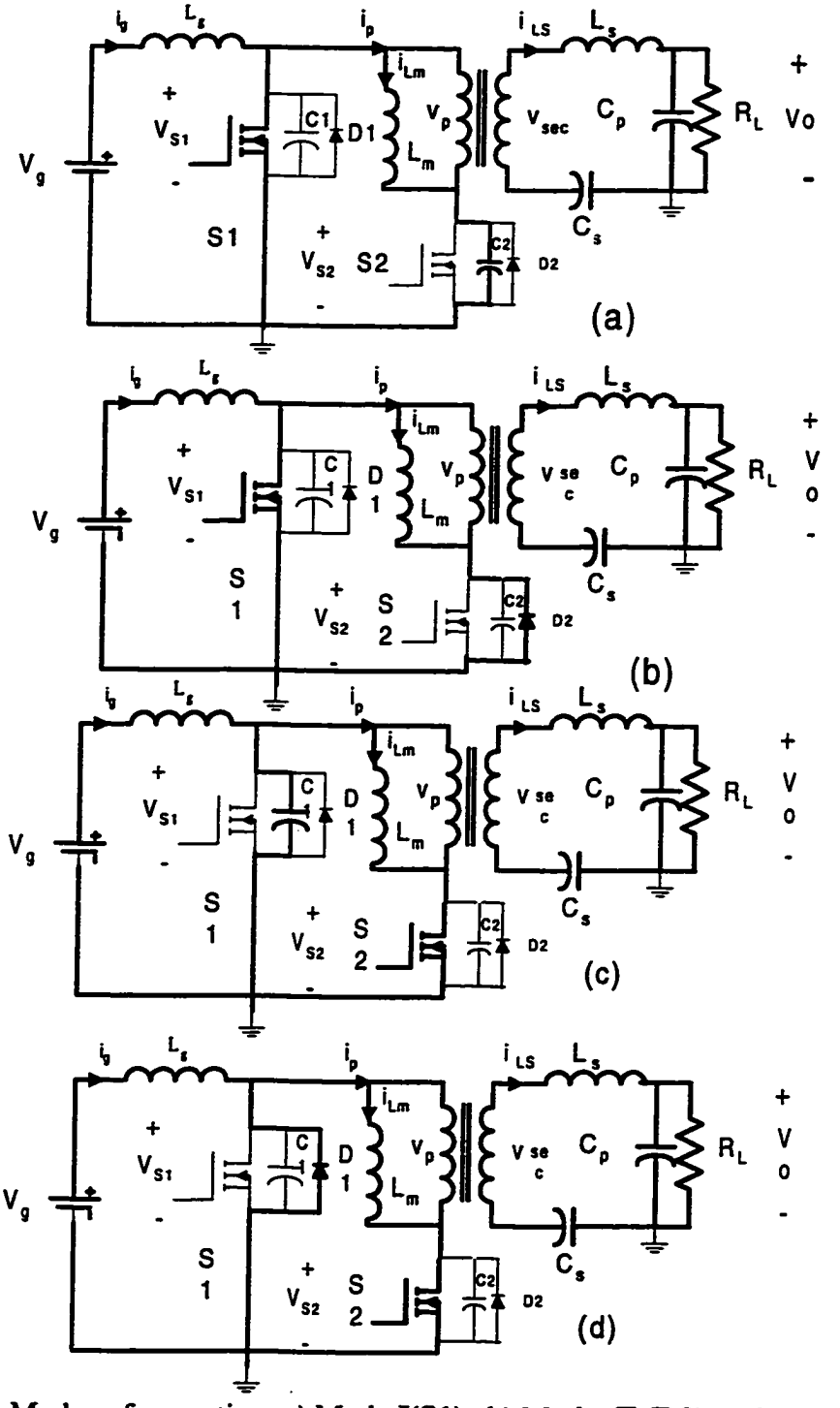

Fig. 4.3 Modes of operation: a) Mode I(S1), b) Mode II (D2), c) Mode III (S2), d) Mode IV (D1)

Equation (4.1) may be represented in a compact form as follows,

$$\dot{X} = A_1 \bullet X + B_1 \bullet I_g \qquad (4.2)$$

$$X = \begin{bmatrix} v_{C1} & v_{C2} & v_{CS} & v_{Cp} & i_{LS} & i_{Lm} \end{bmatrix}^T \qquad (4.3)$$

where **X** is the state vector given by,

Mode 2 ($t_1 \leq t < t_2$):

In this mode, S_1 is on and D_2 is on. The state-space equation is given by,

where $\mathbf{A_2}$ and $\mathbf{B_2}$ are given by,

$$\dot{X} = A_2 X + B_3 I_g \qquad (4.4)$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p R_o} & \frac{n^2}{C_p} & 0 \\ 0 & 0 & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Mode 3 ($t \le t < t_3$):

This mode is similar to Mode 1, except that the resonant voltage is v_{S1} The state space equation is given by,

$$\dot{X} = A_3 \bullet X + B_3 \bullet I_g \qquad (4.5)$$

where $\mathbf{A_3}$ and $\mathbf{B_3}$ are given by,

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p R_o} & \frac{n^2}{C_p} & 0 \\ \frac{1}{n^2 L_S} & 0 & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & 0 & 0 \\ \frac{1}{L_m} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, B_3 = \begin{bmatrix} \frac{1}{C_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Mode 4 ($t_3 < t < t_4$):

In this mode, S_2 and D_1 are on. Magnetizing current is greater than input current and voltage across S_1 is held zero due to diode D_1 being on. The state space equation is given by

Equation (4.6) as follows,

$$\dot{X} = A_4 \bullet X + B_4 \bullet I_g \qquad (4.6)$$

$$A_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p R_o} & \frac{n^2}{C_p} & 0 \\ \frac{1}{n^2 L_S} & 0 & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_4 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

when $\mathbf{A_4}$ and $\mathbf{B_4}$ are given by,

The above four state space equations represent a 6^{th} order non-linear system, and give the complete mathematical model for the converter. Solving these equations is time consuming and difficult. Instead, sinusoidal approximation is used to obtain the steady state response. In the next section, we present such an analysis from which design characteristic curves are derived followed by a design procedure.

4.4 Mathematical Analysis

4.4.1 Sinusoidal Approximation

In order to simplify the analysis, sinusoidal approximation is used to derive expressions for the capacitor voltages, v_{s1}, v_{s2} and the output voltage, v_o. The voltage across the transformer primary winding $v_p(t)$ is shown in Fig. 4.4.

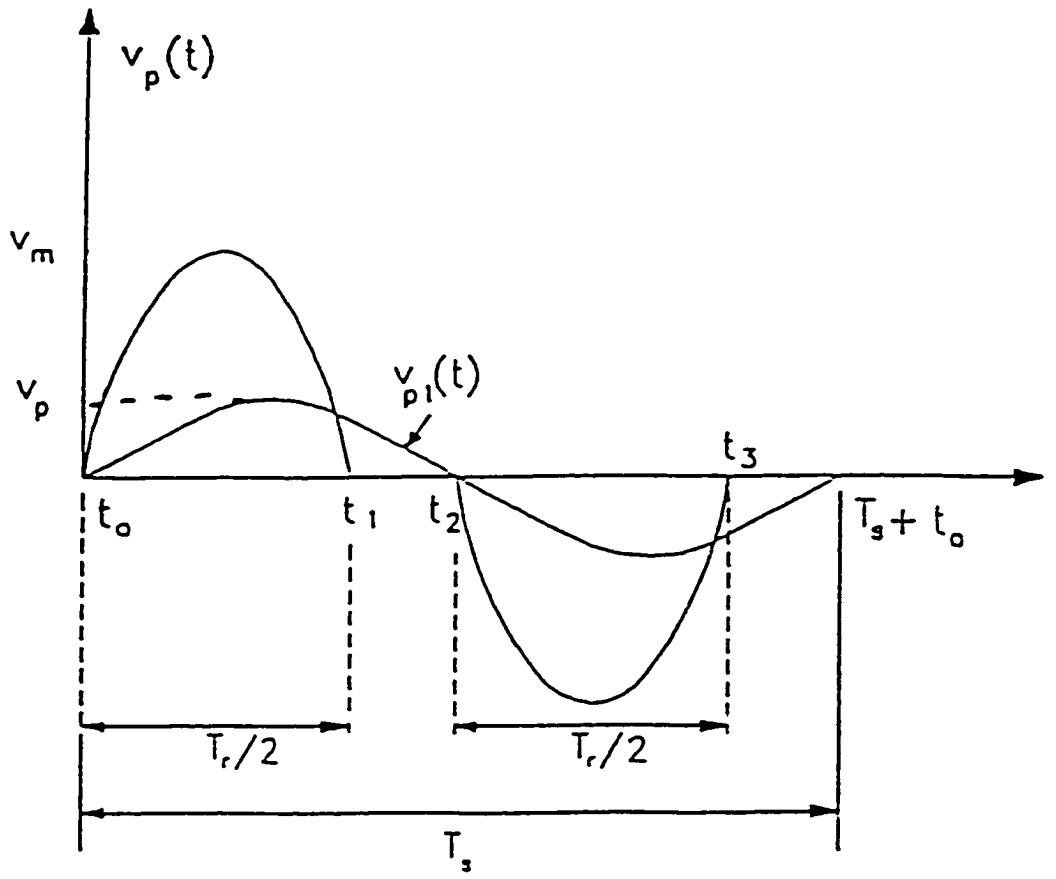

Figure 4. 4 Primary voltage $v_p(t)$

The voltage $v_p(t)$ is the difference between the capacitor voltages v_{s1} and v_{s2} as shown by Eq. (4.7).

$$v_p(t) = v_{s1} - v_{s2} \qquad (4.7)$$

We can express $v_p(t)$ as a Fourier series whose general form is given by:

$$f(t) = F_O + \sum_{n=0}^{\infty} a_n \cos n\omega t + b_n \sin n\omega t \qquad (4.8)$$

where $\omega=2\pi/T$, T is the period of the periodical waveform and F_o is its DC component. Since v_p is symmetrical and odd around $(t_1+t_2)/2+t_0$, its DC component is zero, hence, the fundamental component is given by,

$$f_1(t) = a_1 \cos\omega_s t + b_1 \sin\omega_s t \qquad (4.9)$$

$$= F_1 \sin(\omega_s t - \theta)$$

where,

$$F_1 = \sqrt{a_1^2 + b_1^2}$$

$$\theta = \tan^{-1}\frac{b_1}{a_1}$$

$\alpha v\delta$ $\omega_s = 2\pi/T_s$, T_s is the switching frequency and the coefficients a_1, and b_1, are given by,

$$a_1 = \frac{2}{T_s} \int_0^{T_s} f(t) \cos(\omega_s t)\, dt \qquad (4.10)$$

$$b_1 = \frac{2}{T_s} \int_0^{T_s} f(t) \sin(\omega_s t)\, dt \qquad (4.11)$$

In our case, the function $f(t)$ is $v_p(t)$ which is not continuous over one switching cycle, hence, we split the integration into two intervals: $0 < \omega_s t < \pi - \alpha$ and $\pi < \omega_s t < 2\pi - \alpha$, where the dead time α is defined as below:

$$\alpha = \omega_s \frac{(T_s - T_r)}{2} = \pi (1 - f_{ns})$$

where $f_{ns} = f_s / f_r$, and $f_s = 1/T_s$ and $f_r = 1/T_r$ are the switching and the resonant frequencies of the converter, respectively. It can be shown that f_r is given by,

$$f_r = f_{ir} \sqrt{1 + \frac{L_m / n^2 L_s}{1 + f_{nor}^2}} \qquad (4.12)$$

where f_{ir} and f_{or} are the input and output side resonant frequencies defined by,

$$f_{ir} = \sqrt{1 + \frac{L_m / n^2 L_s}{1 + f_{nor}^2}}, \quad f_{or} = \frac{1}{2\pi \sqrt{L_s (C_T / n^2)}} \qquad (4.13)$$

where $C = C_1 = C_2$, $C_T = C_S C_P / (C_S + C_P)$.

The normalized output frequency, f_{nor}, is expressed as f_S / f_{or}. Let the fundamental component of $v_p(t)$ be given by,

$$v_{p_1}(t) = V_p \sin(w_s t + \theta) \qquad (4.14)$$

V_p is the peak voltage of the fundamental component as shown in Fig. 4.4 and is given by

$$V_p = \sqrt{a_1^2 + b_1^2}$$

It can be shown that a_1 and b_1 are given by,

$$a_1 = \frac{(V_m/\pi)\sin(\pi/2 f_{ns})}{(1/f_{ns})^2 - 1}\left[2\sin\alpha\cos(\alpha/f_{ns}) - \frac{2}{f_{ns}}\cos\alpha\sin(\alpha/f_{ns}) + \frac{2}{f_{ns}}\frac{1-\cos(\pi/f_{ns})}{1-(1/f_{ns})^2}\right]$$

$$b_1 = \frac{2V_m}{\pi}\sin(-\pi/2 f_{ns})\left[\frac{\cos(\alpha/f_{ns})\cos\alpha + \frac{1}{f_{ns}}\sin(\alpha/f_{ns})\sin\alpha}{(1/f_{ns})^2 - 1}\right]$$

where V_m is the peak voltage of v_{S1} and v_{S2} as shown in Fig.4. 4.

4.4.2 The output circuit analysis

The equivalent output circuit shown in Fig. 4.5, is a linear circuit driven by the fundamental component $v_{p1}(t)$ whose voltage gain is given by

$$M = \frac{v_o(t)}{v_{sec}(t)} = \frac{v_o(t)}{n v_p 1(t)} \qquad (4.15)$$

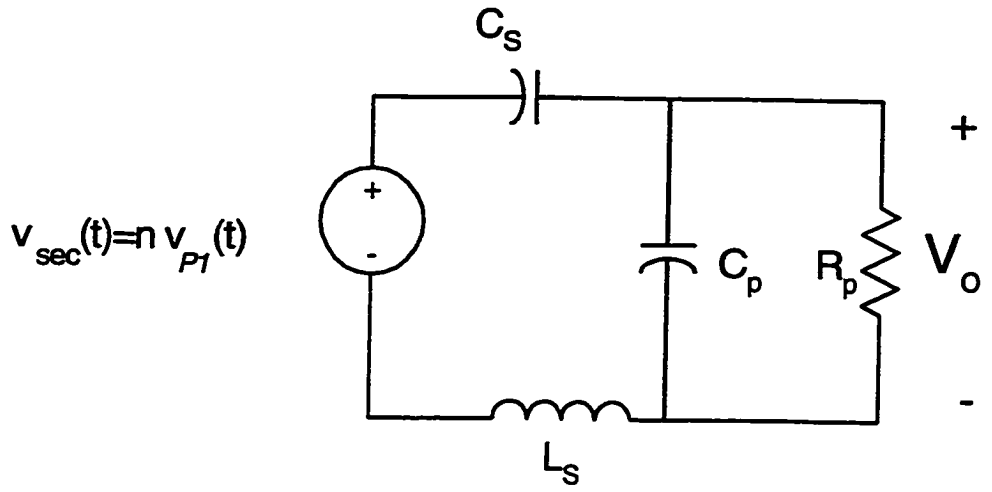

Figure 4.5 Equivalent output circuit

From Fig. 4.5, we obtain the following transfer function,

$$\frac{V_o}{V_{P1}} = \frac{1}{n} \frac{[R_o // -\frac{j}{\omega_s C_p}]}{(R_o // -\frac{j}{\omega_s C_p}) + j(\omega_s L_s - \frac{1}{\omega_s C_s})}$$

and the magnitude of the voltage gain is given by:

$$M = \frac{1}{n\sqrt{(1 + C_p / C_s)^2 (f_{nor}^2 - 1)^2 + \frac{1}{Q_o^2}(\frac{1}{f_{nor}(1 + C_s / C_p)} - f_{nor}^2)}}$$

where Q_o is the output quality factor (normalized load) given by

$$Q_o = \frac{R_o}{Z_{or}} \qquad (4.16)$$

Z_{or} is the output characteristic impedance given by $Z_{or} = \sqrt{L_s/C_T}$. Figure 4. 6 shows M vs. f_{nor} under different normalized loads, Q_o, and for $C_s/C_p = 6$. As expected, this is a boost converter whose voltage gain is larger than one.

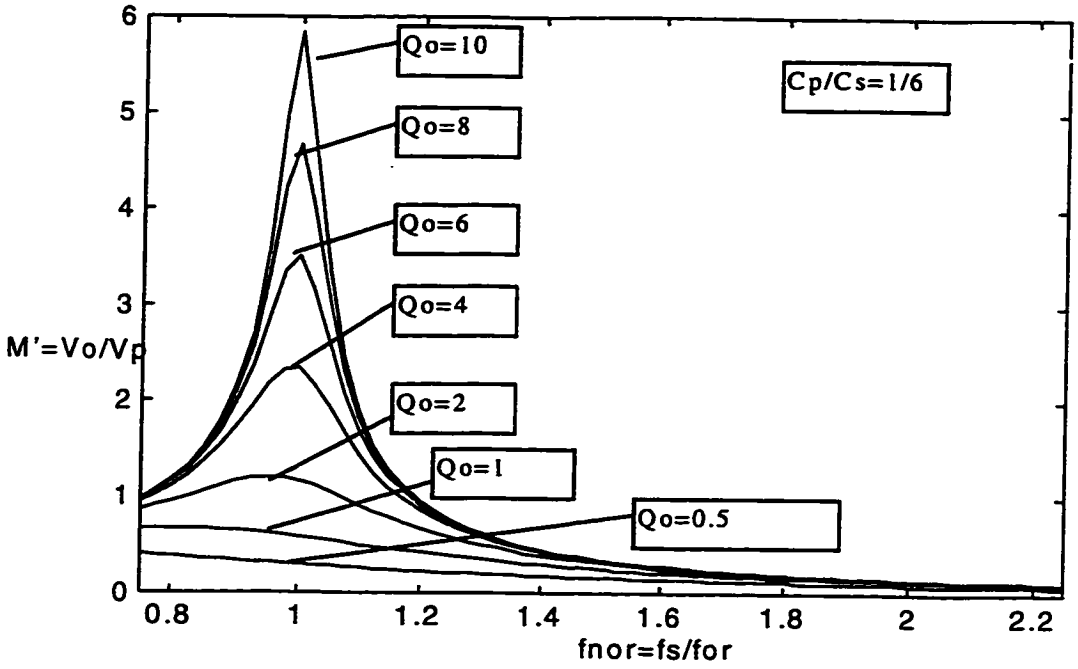

Figure 4.6 Performance curves of the converter

4.4.3 The input circuit analysis

Next we turn to the input side to relate V_g to the voltage across the primary windings. The equivalent circuit for Mode 1 and Mode 3 are identical, since we assume $C_1 = C_2$, as shown in Fig. 4.7.

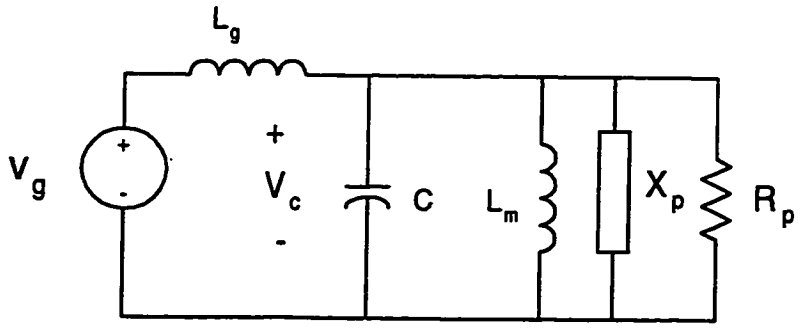

Fig.4.7 Equivalent input circuit for Modes I and III

The impedances X_p and R_p are given by,

$$R_p = X_{s'}\left(\frac{R_{s'}}{X_{s'}} + \frac{X_{s'}}{R_{s'}}\right)$$

$$X_p = R_{s'}\left(\frac{R_{s'}}{X_{s'}} + \frac{X_{s'}}{R_{s'}}\right)$$

where

$$R_{s'} = Z_o\left[\frac{n^2 Q_o}{1 + f_{nor}^2 (1 + C_p/C_s)^2 Q_o^2}\right]$$

$$X_{s'} = Z_o f_{nor}\left[\frac{(f_{nor}^2 - 1) n^2 Q_o^2 (1 + C_p/C_s)^2}{1 + f_{nor}^2 (1 + C_p/C_s)^2 Q_o^2}\right]$$

Assume the transition between the modes makes it possible to treat the voltage across C_1 or C_2, v_c, as a transient voltage given by,

$$v_c(t) = Ae^{-t/\tau} \sin\omega_r t \qquad (4.17)$$

where

$$\tau = 2R_{p'}C$$

The constant A is obtained from the initial condition. In order to evaluate A, we obtain the average value of v_c (t) and set it to V_g, as follows,

$$V_g = \frac{1}{T_s}\int_0^{T_s} v_c(t)\,dt \qquad (4.18)$$

From Equations (4.17) and (4.18), we obtain,

$$A = V_g T_s \frac{(1/\tau^2 + \omega_r^2)}{\omega_r(1 + e^{-\pi/\tau\omega_r})}$$

Hence, $v_c(t)$ is given by,

$$v_c(t) = \frac{V_g T_s(1/\tau^2 + \omega_r^2)}{\omega_r(1 + e^{-\pi/\tau\omega_r})} e^{-t/\tau} \sin\omega_r t \qquad (4.19)$$

If we let the peak voltage of $v_c(t)$ occur at $t=t_{max}$, $V_{c.peak}(t)$ is given by,

$$V_{c.peak} = \frac{V_g T_s(1/\tau^2 + \omega_r^2)}{\omega_r(1 + e^{-\pi/\tau\omega_r})} e^{\frac{t_{max}}{\tau}} \sin(\omega_r t_{max}) \qquad (4.20)$$

In terms of normalized quantities, we obtain

$$V_{nc.peak} = \frac{2\pi}{f_{ns}}\left[\frac{1 + (f_{ns}/\tau_n)^2}{(1 + e^{-\pi f_{ns}/\tau_n})}\right] e^{-\theta_m/\tau_n} \sin(\theta_m / f_{ns})$$

where,

$$\tau_n = \frac{2(a^2+1)n^2 Q_o f_{nor}(C/C_T)}{1 + f_{nor}^2 Q_o^2 (1 + C_p/C_s)^2}$$

$$\theta_m = f_{ns} \tan^{-1}(\tau_n / f_{ns})$$

$$a = f_{nor}(f_{nor}^2 - 1)(1 + \frac{C_p}{C_s})^2 Q_o$$

$$t_{max} = \frac{1}{\omega_r} \tan^{-1}(\omega_r \tau)$$

4.5 Characteristic Curves

The characteristic curve for $V_{nc,peak}$ vs f_{ns}, under different Q_o, is given in Figure 4.8. Figure 4.9 gives the characteristic curve for $V_{nc,peak}$ vs. f_{ns} under different values of f_{nor}. These curves are derived under fixed circuit parameters.

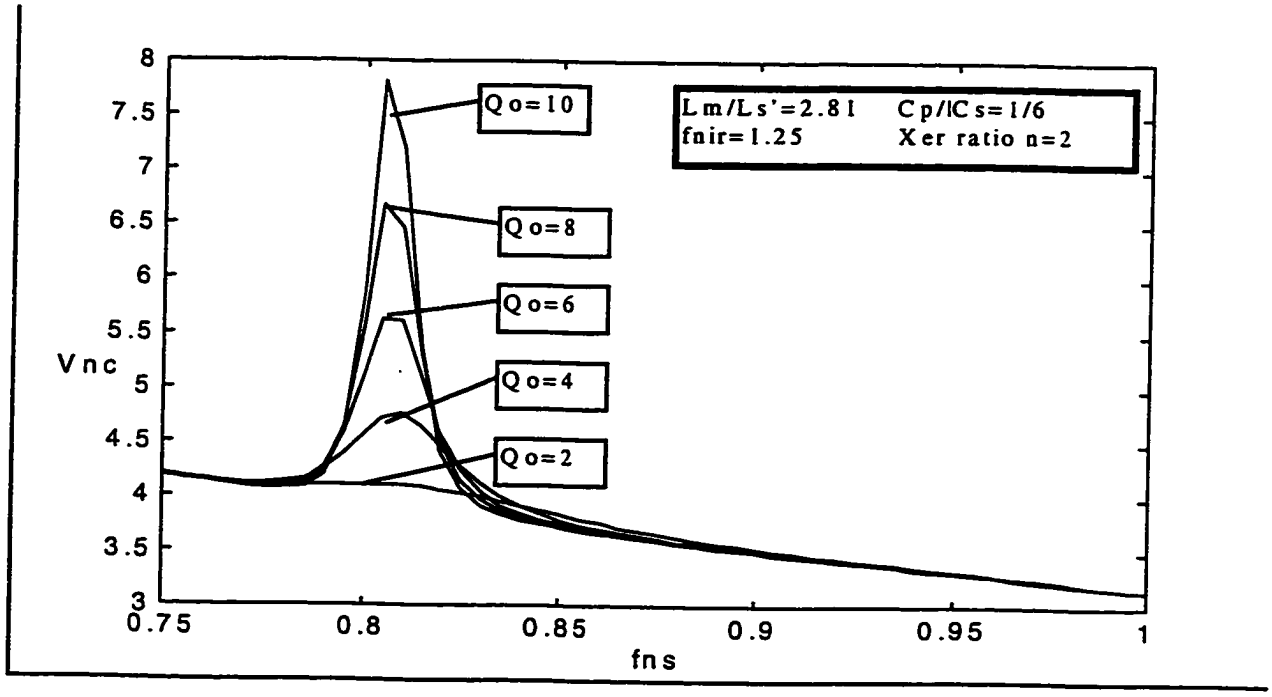

Figure 4.8. Characteristic curve for $V_{nc,peak}$ vs. f_{ns} under different values of Q_o

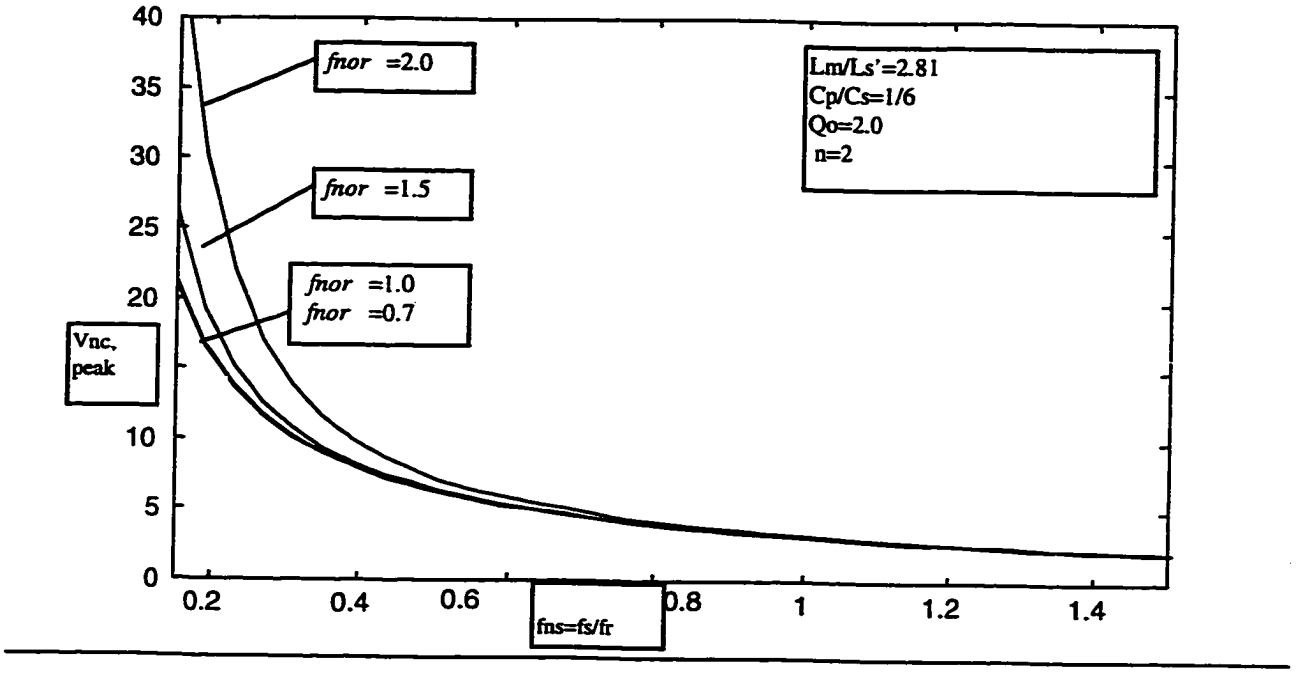

Fig. 4.9 Characteristic curves for $V_{nc.peak}$ vs. f_{ns} under different values of f_{no}

4.6 Design Procedure and Example

Consider the following design specifications:

- Switching frequency, f_s = 100kHz
- Input voltage, Vg = 60V
- Output power, P_o = 100W
- Component Ratios: $L_m/L_s' = 2.81$, $C_p/C_s = 1/6$.

We follow the design procedure outlined as follows:

1) We choose f_{ns}=1, f_{nor} = 1.2 and Q_o=2.0. This region is a compromise between a sensitive region at low f_{ns} (0.5-1), and the flat response for f_{ns} > 1.5. From Fig. 4.8,

we obtain an approximate value for $V_{nc,peak} \approx 3.34$.

2) The actual $V_{c,peak}$ value is 206.4 V.

3) For given f_s and f_{nor}, we obtain f_{or} = 166.7 kHz.

4) From Fig. 4.6, with given f_{nor} and Q_o, we obtain M=0.671, hence, the output voltage V_o = 138.5 V.

5) With P_o given, we obtain $R_o = 100\Omega$.

6) From R_o and Q_o, we obtain $Z_o = 50\Omega$

7) Z_o and f_{or} are solved for resonant components L_s and C_T,

$C_T = 1/2\pi f_{or} Z_o \qquad L_s = 2\pi f_{or}/P_o$

This yields L_s=86.11μH, C_p=47nF and C_s=270nF C_T=39.91nF

8) For given f_{ns} and f_{nor}, we obtain f_{ir} from Eq. (4.12) and (4.13), f_{ir} = 136.4KHz, where $fns = fr/fs$ normalized switching frequency

9) Solving f_{ir} and f_r for L_m and C, we obtain:

L_m = 0.97mH, $C=C_1=C_2$ =10.0nF

$$\frac{\Delta I_g}{T_s/2} = \frac{V_g}{L_g}$$

10) Finally, we estimate L_g by limiting I_g to 5% ripple on its average value, using the following relation,

We obtain L_g = 3mH.

To summarize the design, Table 4.1 below shows the calculated parameters for this design.

Table 4.1

PARAMETERS	DESIGN VALUE
$V_{nc,peak}$ (normalized)	3.44
$V_{c,peak}$ (actial value)	206.4 V
f_{ns}	1.0
f_{nor} (normalized)	1.2
f_{or} (actual value)	166.7kHz
Qo	2.0
M	0.671
V_o	138.5 V
R_o	100.0 Ω
Z_{or}	50.0 Ω
C_T	39.91nF
C_P	47.0 nF
C_S	270.0 nF
f_{ir}	136.4kHz
L_S	86.11μH
L_m	0.97mH
L_g	3.0mH
C1=C2=C	10.0nF

CHAPTER 5

SIMULATION AND EXPERIMENTAL RESULTS FOR THE DC-TO-AC INVERTER TOPOLOGY

5.1 Modified DC-to-AC Zero Voltage Switching Inverter Topology

Figure 5.1 shows the simplified dc-to-ac converter circuit with output isolation and zero-voltage-switching (ZVS).

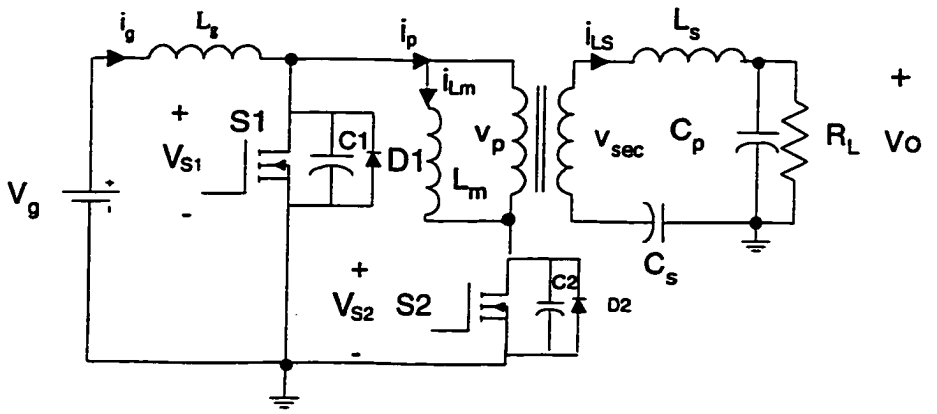

Fig. 5.1 DC-to-AC ZVS inverter with isolation

5.2 Simulation Results for the dc-to-ac inverter

5.2.1 Schematic for simulation

Figure 5.2 shows the PSPICE™ schematic diagram for the topology shown in Figure 5.1. The input voltage is a dc source of 60V. The values of the different parameters are

according to the design parameters determined in Section 4.6. A low value resistor R_3 is inserted in series with the primary of the isolating transformer for simulation purposes only. PSPICE does not accept a non-resistor inductor loop formed by the transformer TX2 and L_g. This avoids convergence problems in the transient analysis of this topology. Ideal switches are used instead of MOSFETS. The MOSFET model is approximated by using D1 and D2 as the MOSFET's body diodes. Capacitor C1 and C2 are equivalent parasitic capacitances of the switch. This model also helps to understand the different modes of operation corresponding to the steady state waveforms.

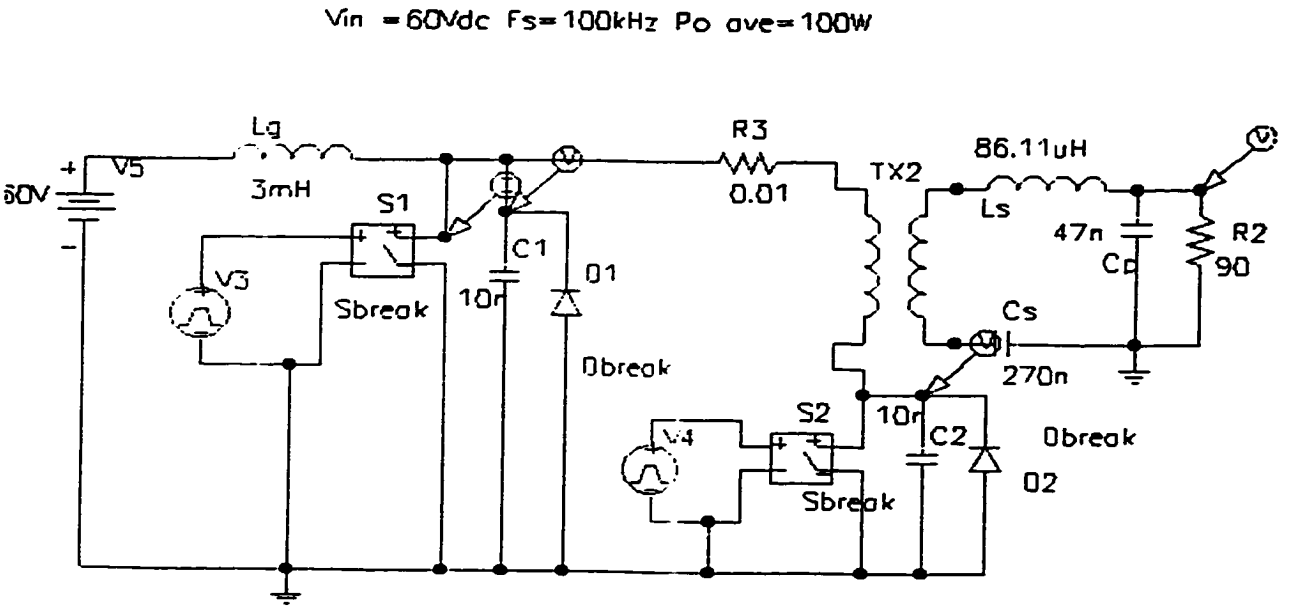

Figure 5.2 PSPICE schematic for the dc-to-ac ZVS inverter

5.2.2 Simulation waveforms

5.2.2.1 Input inductor current i_{Lg} and gate control voltage for switch S_1

Figure 5.3 shows the input inductor current i_{Lg} and the gate control voltage for switch S_1. The current i_{Lg} is about 2.0 Amps and corresponds to the switching of gate voltage pulse of S_1. The current increases linearly when the switch is on and vice versa.

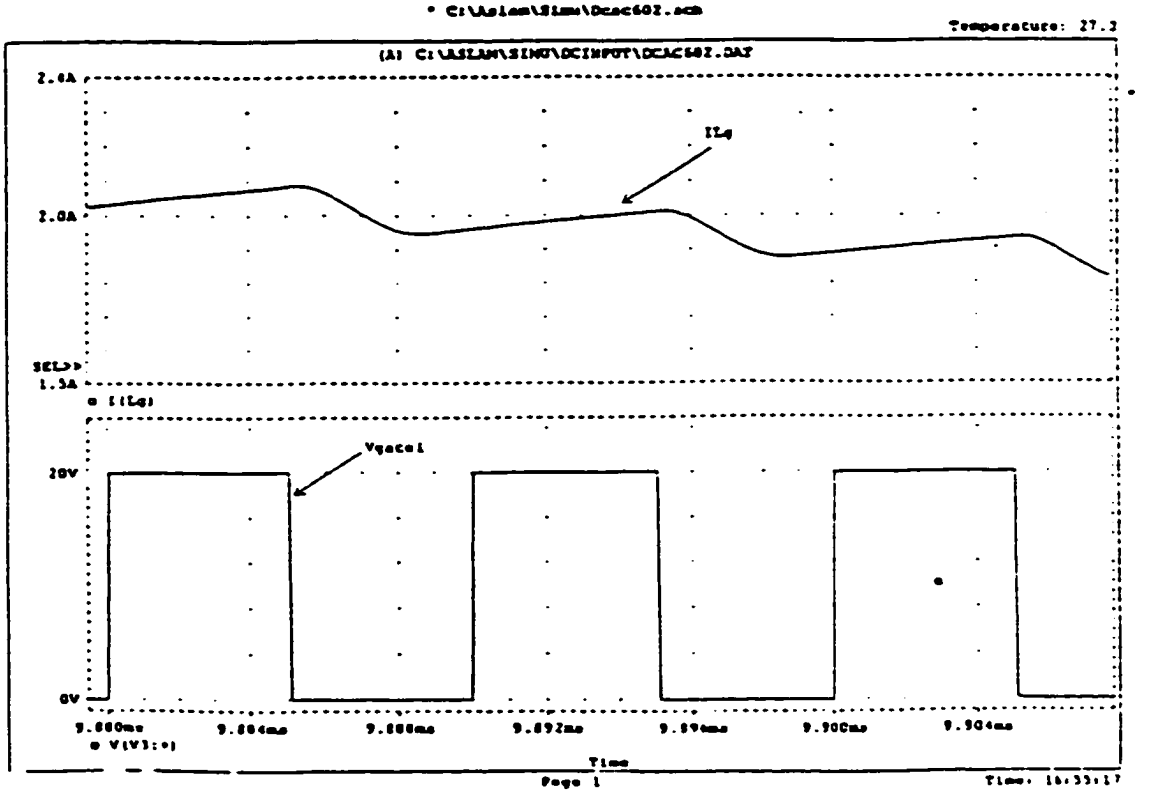

Figure 5.3 Simulation waveforms for input inductor current (i_{Lg})and S1 gate voltage (V_{gS1})

The gate voltage pulse is at 100kHz switching frequency. The gate control voltage of switch S_2 is the complement of S_1 gate voltage.

5.2.2.2 Output voltage V_o and voltages across switches S_1 and S_2

Figure 5.4 shows the ouput voltage v_o and the voltage across the switches S_1 and S_2. The output voltage is a good sinosoidal with amplitude of 144.05V as shown in the simulation. The output voltage frequency is about 100 kHz as seen in the figure.

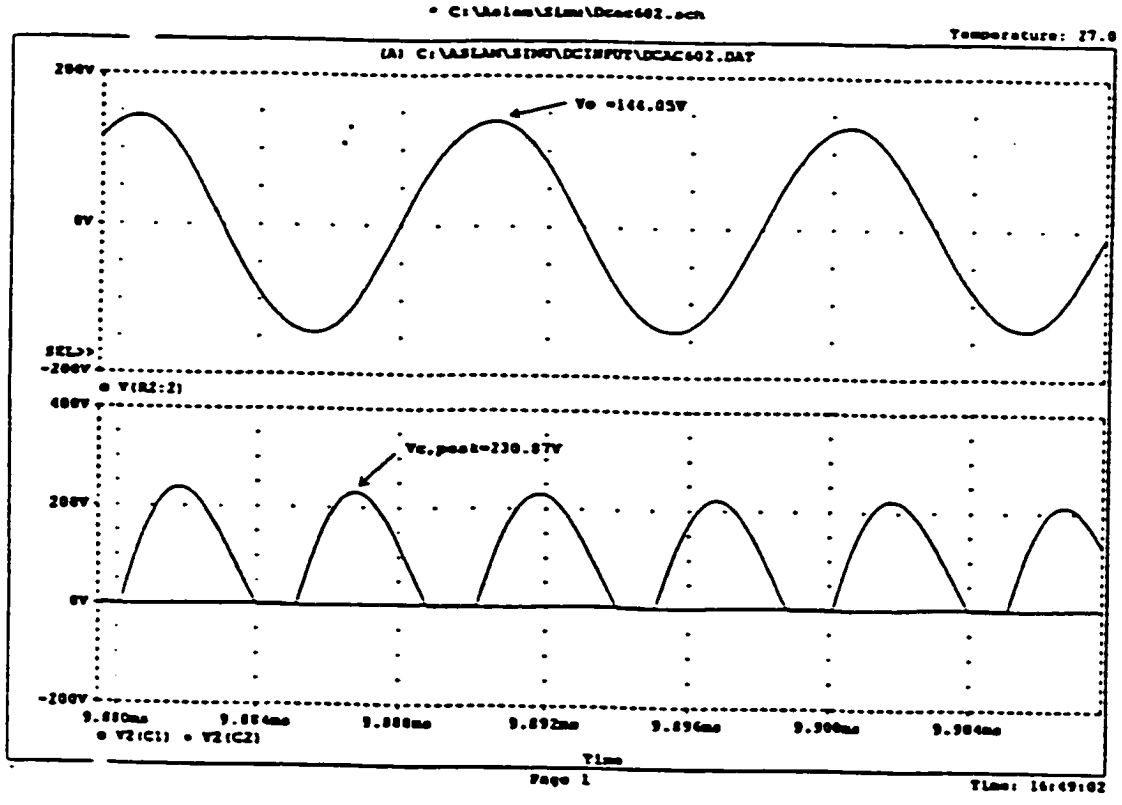

Figure 5.4 Simulation waveforms for output voltage (V_o) and voltage across S_1 and S_2

The voltage waveforms for switches S1 and S2 are shown below the output voltage waveform. They correspond to voltages across the capacitors C1 and C2 respectively. The peak voltage stresses are identical and is 230.87 V. We can see that both theses voltages are sinusoids and increase to their maximum values and come down to zero. Zero voltage switching is achieved when the corresponding switch is turned on when the voltage across it is zero.

5.3 Experimental results for the dc-to-ac inverter

The circuit was built according to the design procedure described and explained in Section 4.6. A 100 MHz digital oscilloscope by Hewlett Packard was used to capture the waveforms in a .ttf format and converted to image files to be used in this chapter. Additional forced cooling was necessary on the load resistor that was rated for 75W, used on a 100W output of the inverter. Wires were twisted and arranged to have the shortest possible length to minimize stray and mutual inductance. To simplify the experimental setup, the input voltage was assumed constant, V_g. Therefore, no measurements were made for the power factor and total harmonic distortion.

5.3.1 Experimental waveforms

5.3.1.1 Gate control and voltage across switch S_1

Figure 5.5 shows the experimental waveforms for the gate control pulse (top) and the voltage across switch S_1 V_{cpeak} (below) for the dc-to-ac inverter. The voltage stress at the main switch was measured at 233.03 V. The resonant frequency for this voltage across S_1 is 100.07kHz. There is some ringing on the gate pulse of switch S1 in this figure.

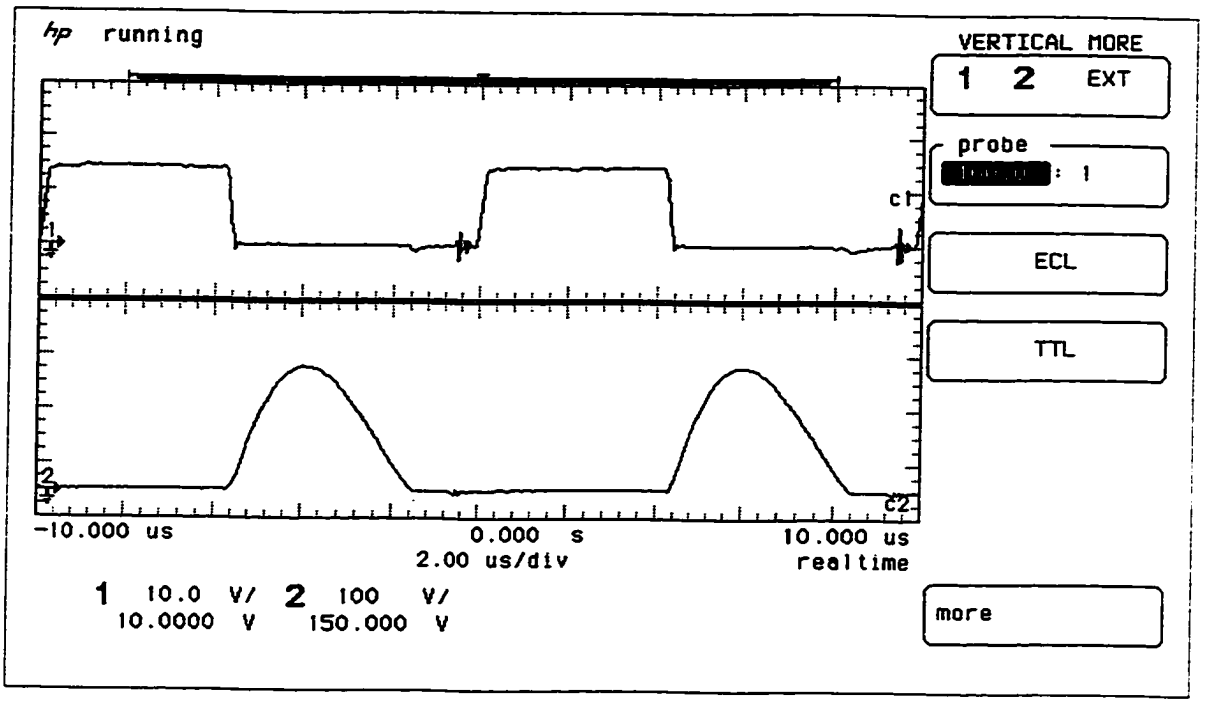

Figure 5.5 Experimental waveforms for the gate control pulse and voltage across S_1

5.3.1.2 Gate control pulses for switches S_1 and S_2

Figure 5.6 shows the experimental waveforms for the gate control pulses for switches S_1(top) and S_2 (bottom). The two waveforms switch complementarily and are clear square waveforms. The switching frequency of these waveforms is 100 kHz. (f_s) which is according to the design procedure in Chapter 4.

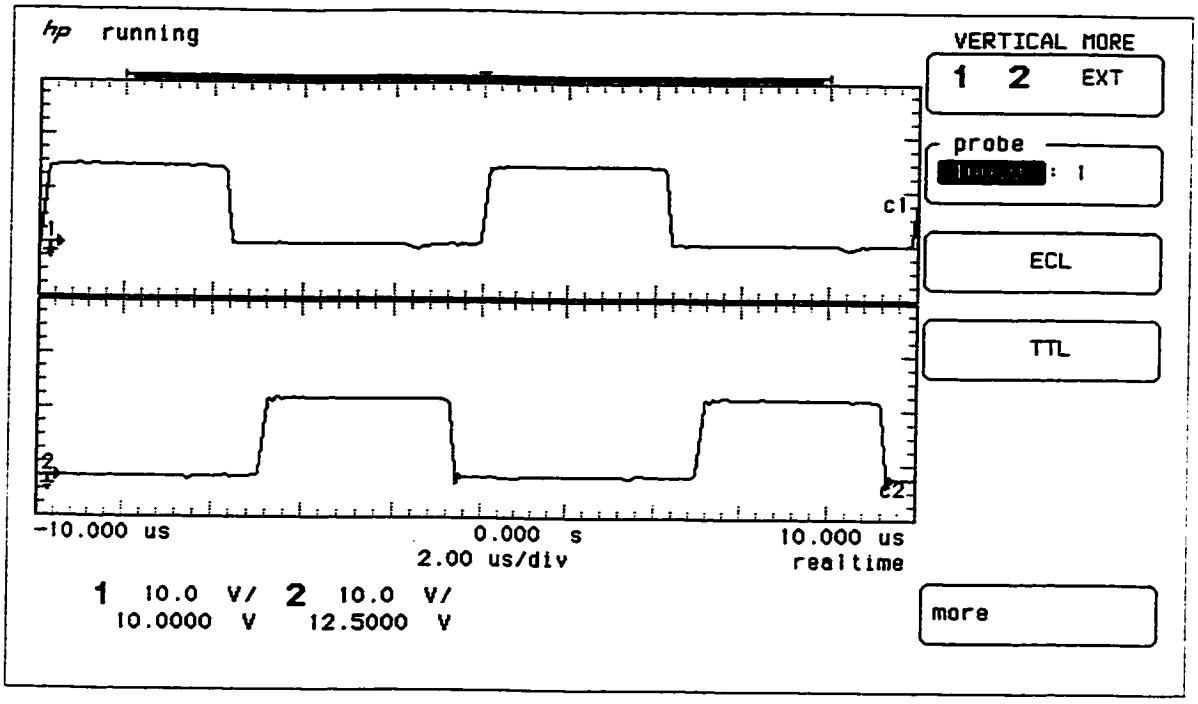

Figure 5.6 Experimental waveforms for the gate control pulses for S_1 and S_2

5.3.1.3 Gate control pulse of S1 and output voltage v_o

Figure 5.7 shows the experimental waveforms for the gate control pulses for switch S_1 (top) and the output voltage of the inverter V_o (bottom). The control pulse is square wave at 100 kHz switching frequency. There is slight ringing just before the rising edge of the gate control pulse to the switch S_1. The output voltage of the dc-to-ac inverter circuit, v_o, is a clean sinusoidal voltage waveform. The amplitude of this signal is 145.68Volts and a frequency of about 100 kHz. The signal is symmetrical with regards to the positive and negative amplitude as wells as the quality of the sinusoid.

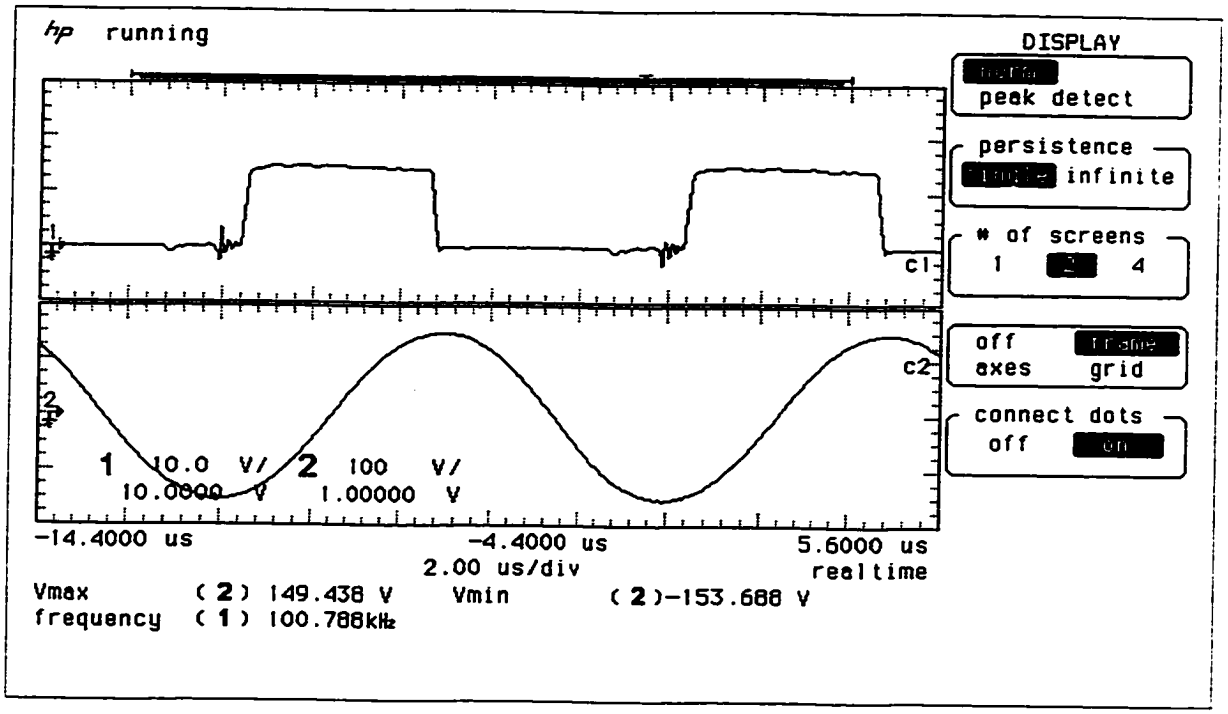

Figure 5.7 Experimental waveforms for the gate control pulses for S_1 and output voltage V_o

5.3.1.4 Gate control pulse of S_1 and output series inductor current i_{LS}

Figure 5.8 shows the gate control pulse of switch S_1 (top) and the current through series inductor L_S , i_{LS}, (bottom). The gate pulse is clean square waveform at its switching frequency of 100 kHz. The current through the series inductor L_S is a sinusoid waveform. This current is the addition of the load output current and the current through the parallel resonant capacitor C_P.The load current is much larger than the current through CP. This

current, i_{LS}, closely represents the load output current through load resistor R_o. The output current is approximately 1.1 Amps. This results in the output power of about 110W.

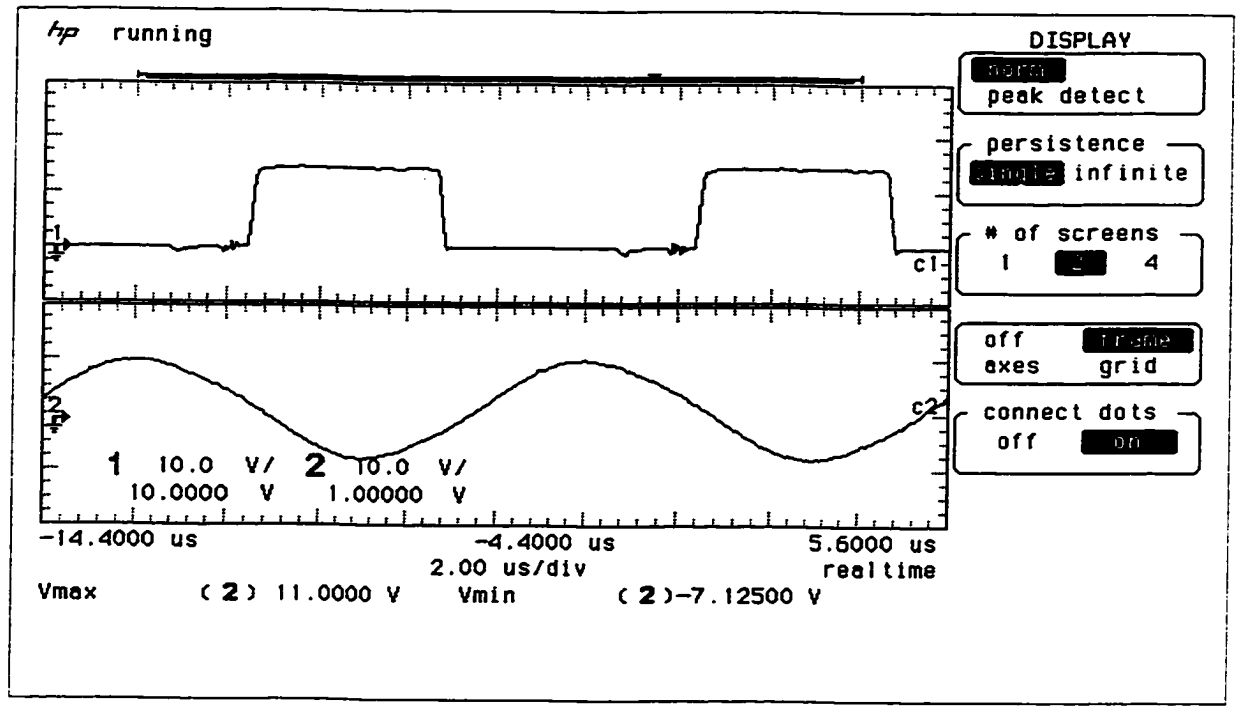

Figure 5.8 Experimental waveforms for the gate control pulses for S_1 and current i_{LS}

5.3.1.5 Gate control pulse of S_2 and input inductor current i_{Lg}

Figure 5.9 shows the experimental waveforms for the gate control pulse for switch S_2 (top) and the current through the main input inductor L_g, i_{Lg}, (bottom). The gate pulse is a clean square wave with a switching frequency of 100 kHz. The inductor current, i_{Lg}, goes down when switch S2 is on because the energy is supplied by the inductor for the core

resetting during Mode III of the steady state analysis. And when S2 is off (S1 is on), the current through the input inductor ramps up during Mode I in the steady state analysis of this inverter.

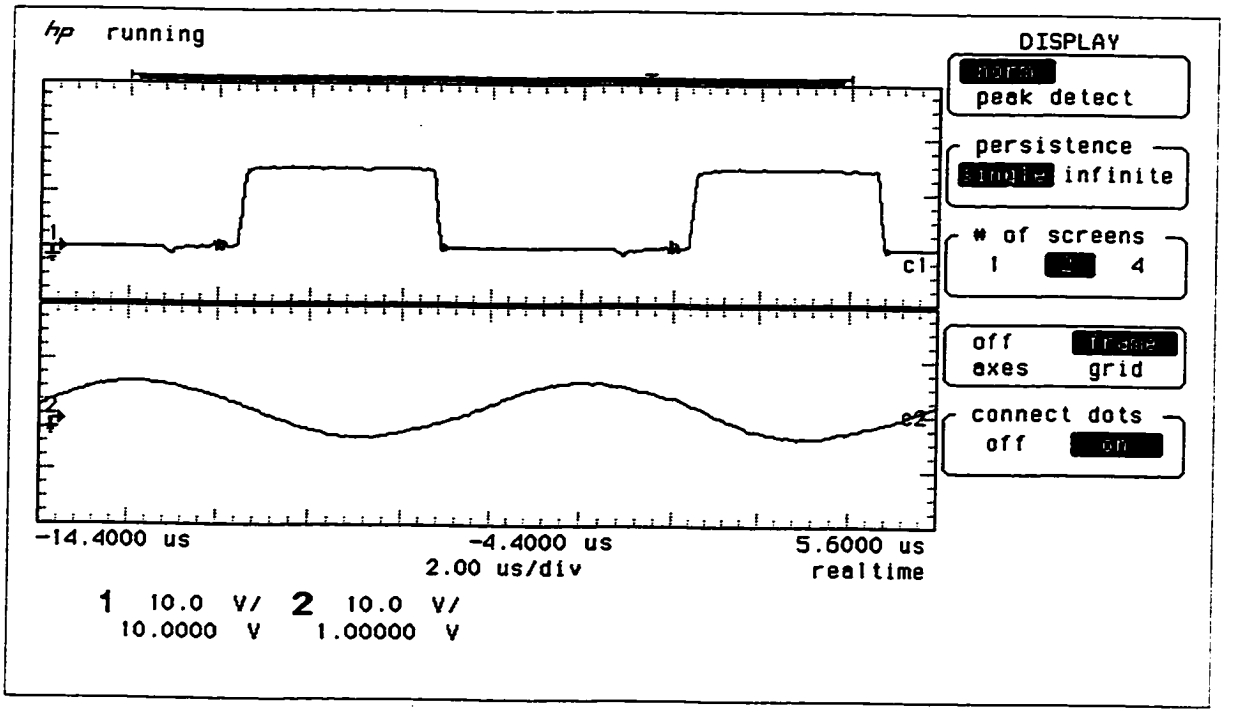

Figure 5.9 Experimental waveforms for the gate control pulses for S_2 and i_{Lg}

5.3.1.6 Gate control pulse of S1 and V_{cpeak} of S_2

Figure 5.10 shows the experimental waveforms for the gate control pulses for switch S_1 (top) and the voltage across the switch S_2, V_{cpeak}, (bottom). The gate pulse is a square wave of 100 kHz of switching frequency. The voltage across switch is a half-positive

sinusoid. When the sinusoid goes to zero, the body diode of the switch turns on to clamp this voltage to zero to achieve zero voltage switching. The voltage stress at this switch was measured at 233.03 V. The resonant frequency for this voltage across S_1 is 100.07kHz.

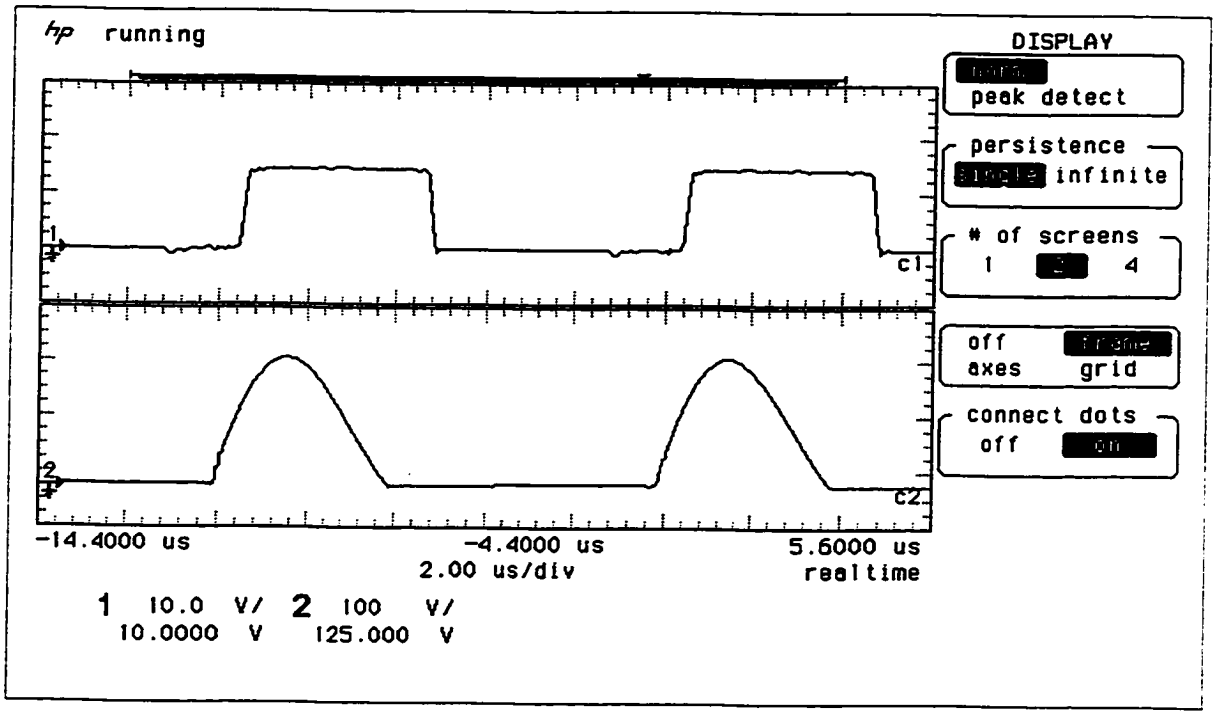

Figure 5.10 Experimental waveforms for the gate control pulses for S_1 and V_{cpeak} for S_2

5.4 Comparison of Simulation and Experimental Results

Table below shows the comparison of the simulation and experimental results of the dc-to-ac inverter.

PARAMETER	SIMULATION	EXPERIMENT
V_{cpeak}	230.87V	233.03V
V_o	144.05V	145.68V
F_r	105.4kHz	100.2kHz
F_s	100kHz	100kHz
$P_{o,ave}$	93W	110.2W
Diode	Ideal body diode	Actual body diode of IRF730
Switch	Ideal	MOSFET (IRF730)

It is clear from the above results that the simulated and experimental values are in good agreement. The output voltage rms and frequency values are within 1% of the experimental and theoretical values.

CHAPTER 6

SMALL SIGNAL MODELING OF THE DC-TO-AC RESONANT INVERTER

6.1 Introduction

The small signal model for the open-loop system must be obtained to study the effect of a small variation in the input current signal on the output voltage on one hand, and the effect of a small signal variation in the switching frequency on the output voltage, on the other hand. The above suggests that a transfer function between the input current to the output voltage must be obtained, which represents the dynamic response for the power stage. Whereas, the effect of the switching frequency variation on the output require the determination of the transfer function between the control line to the output voltage which represents the dynamic response of the feedback circuit. A simplified block diagram for a closed-loop system for a switching converter is shown in Figure 6.1. In this chapter, using state space averaging technique, we will derive the small-signal equivalent mathematical model for the dc-to-ac inverters given in Chapter 4. Based on this model, input-to-output and control-to-output transfer function will be derived. Such transfer functions are used for the closed-loop controller design. Frequency for the two transfer functions will be given in Section 6.4.

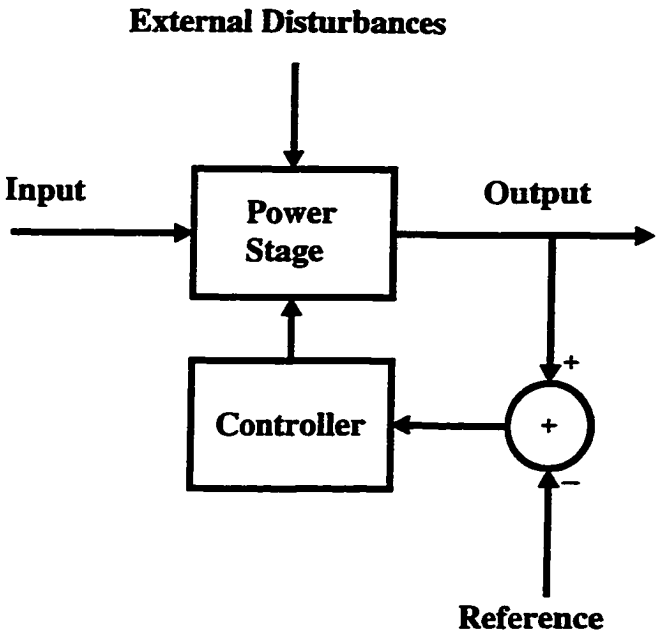

Figure 6.1: Block diagram representation for power converter with transfer functions

6.2 Basic Concepts

In steady state, the independent inputs are the dc input current and the constant switching frequency. Where as in the dynamic state, the two independent inputs are the line and control signal perturbations. Because of the presence of the switching devices, the closed-loop system is a non-linear structure. Figure 6.2 shows the Large signal (both dc and ac qualities) block diagram under both line and control perturbations.

$$i_{Lg} = I_{Lg} + \hat{i}_{Lg}$$

$$v_o = V_o + \hat{v}_0$$

$$f_S = F_S + \hat{f}_S$$

where I_{Lg}, V_o, and f_s, are the steady state dc values and $\hat{i}_{Lg}$, $\hat{v}_o$ and $\hat{f}_s$ are the small signal perturbation of the converter variables.

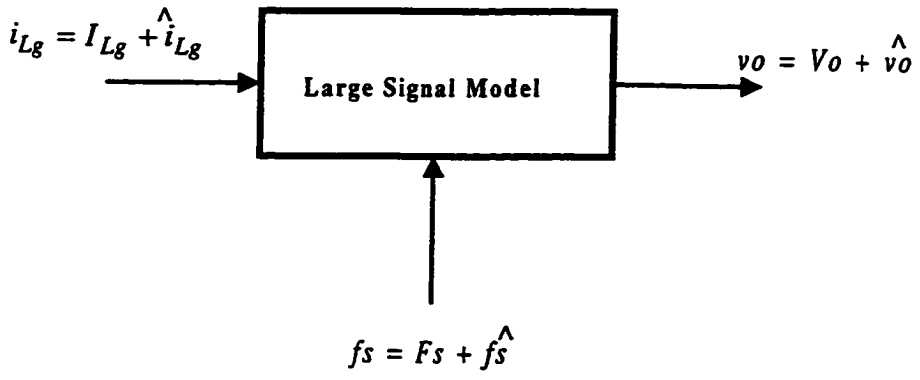

Figure 6.2: Large signal model diagram representation for power converter

The objective is to derive two small-signal transfer functions, namely:

1) Input-to-output transfer function:

$$H_1(s) = \frac{\hat{v}_o(s)}{\hat{i}_{Lg}(s)} \qquad \text{when } \hat{f}_s = 0 \tag{6.1}$$

2) The control-to-output transfer function:

$$H_2(s) = \frac{\hat{v}_o(s)}{\hat{f}(s)} \qquad \text{when } \hat{i}_{Lg} = 0 \tag{6.2}$$

Other transfer functions such as input and output impedance are also important for the design of inverters. In this chapter we only consider the above two transfer functions. To determine $H_1(s)$ and $H_2(s)$ transfer functions, a state-space averaging technique will be used as discussed in the next section.

6.3 State-Space Averaging

In this section, we will use the state-space averaging method to obtain the converter transfer function. Since this converter is a sixth order systems, we will review the sixth order state vector representation. The state-space averaging approach is a convenient and simple method that combines the state-space modeling (mathematical representation) and the averaging technique (equivalent circuit representation). The state-space technique uses numerical analysis methods to obtain the dynamic model from exact state-space equations for the power stage. Using this technique, a unified representation for this dc-to-ac converter was derived. Whereas, using the averaging method, the power stage is represented by equivalent linear circuit model, which in terms can be analyzed and synthesized using the well-known linear circuit method. Whether using state-space averaging or circuit averaging, the next two steps are needed in the process of obtaining a simplified transfer function of the power stage: *perturbation* and *linearization*. In the final analysis, general equations are obtained from the averaged linearized model from which both steady state (dc) and dynamic (ac) performances can be assessed.

6.3.1 Averaging technique

In this DC-to-Ac converter, conversion takes place through repetitive switching between four linear circuit modes as shown in earlier chapters. Each mode represents a switched-state. Each of these circuit modes can be represented by linear independent state variables, forming what is known as state-space equations. Furthermore, the order of the state-space equation for a given circuit model is determined by the number of storage capacitors and inductors. Even though, each mode is represented by a linear set of state-space equations, the four modes together represent a non-linear system. The goal is to be able to combine the four systems into one linear set of state-space equations. Meanwhile the final system is accurate enough to represent the behavior of the original system.

Figure 6.3 shows the block diagram representation for the dc-to-ac inverter where i_g represents the input and v_o is the output voltage. The objective is to obtain the set of Ai, Bi and Ci matrices for the four modes of operation (i=1, 2, 3, 4)

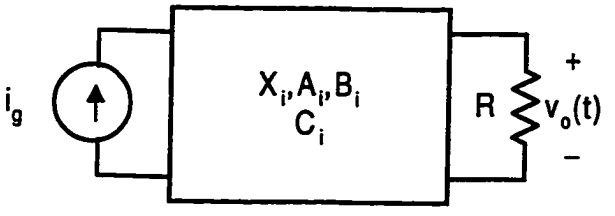

Figure 6.3 Block diagram representation for the dc-to-ac inverter

The four modes of operation are represented in state space equations as follows:

Mode I [$0 < t < t_1$]

First let us define the state vector x(t) as follows:

$$X = [v_{C1}\ \ v_{C2}\ \ v_{CS}\ \ v_{CP}\ \ i_{LS}\ \ i_{Lm}]^T$$

From the equivalent circuit model during Mode I, we may represent the mode mathematically by Equation (6.3) and (6.4)

$$\dot{x}_1 = A_1 x_1 + B_1 i_g \tag{6.3}$$

$$y_1 = C_1 x_1 \tag{6.4}$$

where A_1, B_1 and C_1 are given by,

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_2} & \frac{1}{C_2} \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_P R_O} & \frac{n^2}{C_P} & 0 \\ 0 & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & 0 & 0 \\ 0 & -\frac{1}{L_m} & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C_1 = [0\ 0\ 0\ 1\ 0\ 0]$$

Mode II [$t_1 < t < t_2$]

During Mode II, the state space equations are given by Equations (6.5) and (6.6)

$$\dot{x}_2 = A_2 x_2 + B_2 i_g \tag{6.5}$$

$$y_2 = C_2 x_2 \tag{6.6}$$

where the state matrices are given by,

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{Cs} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p R_o} & \frac{n^2}{C_p} & 0 \\ 0 & 0 & -\frac{1}{n^2 Ls} & -\frac{1}{n^2 Ls} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C2 = [0\ 0\ 0\ 1\ 0\ 0]$$

Mode III [$t_2 < t < t_3$]

During Mode III, the state space equations are given by Equations (6.7) and (6.8).

$$\dot{x}_3 = A_3 x_3 + B_3 i_g \tag{6.7}$$

$$y_3 = C_3 x_3 \tag{6.8}$$

where the state matrices are given by,

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & -\frac{1}{C1} & -\frac{1}{C1} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{Cs} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_pR_o} & \frac{n^2}{C_p} & 0 \\ \frac{1}{n^2Ls} & 0 & -\frac{1}{n^2Ls} & -\frac{1}{n^2Ls} & 0 & 0 \\ \frac{1}{Lm} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_3 = \begin{bmatrix} \frac{1}{C_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C_3 = [0\ 0\ 0\ 1\ 0]$$

Mode IV [$t_3 < t < t_4$]

During Mode IV, the state space equations are given by Equations (6.9) and (6.10)

$$\dot{x}_4 = A_4 x_4 + B_4 i_g \qquad (6.9)$$

$$y_4 = C4 x_4 \qquad (6.10)$$

where the state space matrices are given by,

$$A_4=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_P R_o} & \frac{n^2}{C_P} & 0 \\ \frac{1}{n^2 L_S} & 0 & -\frac{1}{n^2 L_S} & -\frac{1}{n^2 L_S} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad B_4=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C_4=[0\ 0\ 0\ 1\ 0]$$

The state-space averaging is obtained by taking the *average* of the six state-space equations models of switching converter as follows:

$$\dot{X}_{ave}=\dot{x}_1\frac{T_r}{2}+\dot{x}_2\frac{(T_S-T_r)}{2}+\dot{x}_3\frac{T_r}{2}+\dot{x}_4\frac{(T_S-T_r)}{2} \tag{6.11}$$

$$y_{ave}=\dot{y}_1\frac{T_r}{2}+\dot{y}_2\frac{(T_S-T_r)}{2}+\dot{y}_3\frac{T_r}{2}+\dot{y}_4\frac{(T_S-T_r)}{2} \tag{6.12}$$

$$\dot{X}_{ave}=\frac{(x_1-x_2+x_3-x_4)}{2}T_r+\frac{(x_2+x_4)}{2}T_S \tag{6.13}$$

where T_r is the resonant frequency and T_S is the switching frequency.

Rearranging the above two equations, it can be shown that the linear continuous state-space mathematical representation can be given by;

$$\dot{X}_{ave} = Ax + Bi_g$$

$$y = Cx$$

where,

$$A = \frac{1}{T_S}\left[\frac{(A_1 - A_2 + A_3 - A_4)}{2}T_r + \frac{(A_2 + A_4)}{2}T_S\right]$$

also A can be rewritten as $A = \frac{1}{T_S}(\alpha T_r/2 + \beta T_S/2)$

where matrices $\alpha = (A_1 - A_2 + A_3 - A_4)$ *and* $\beta = (A_2 + A_4)$

$$B = \frac{1}{T_S}\left[\frac{(B_1 - B_2 + B_3 - B_4)}{2}T_r + \frac{(B_2 + B_4)}{2}T_S\right]$$

also B can be rewritten as $B = \frac{1}{T_S}(\theta T_r/2 + \delta T_S/2)$

where matrices $\theta = (B_1 - B_2 + B_3 - B_4)$ *and* $\delta = (B_2 + B_4)$

Finally the C matrix is given by,

$$C = \frac{1}{T_S}\left[\frac{(C_1 - C_2 + C_3 - C_4)}{2}T_r + \frac{(C_2 + C_4)}{2}T_S\right]$$

also C can be rewritten as $C = \frac{1}{T_S}(\lambda T_r/2 + \phi T_S/2)$

where matrices $\lambda = (C_1 - C_2 + C_3 - C_4)$ *and* $\phi = (C_2 + C_4)$

It is clear that above expressions represent the average of matrices A_1, A_2 , A_3 and A_4, B_1, B_2, B_3 and B_4, and matrices C_1, C_2, C_3, C_4 over one switching cycle. The exact expression is complicated and numerical solution is needed to obtain the solution for X.

6.3.2 State variable perturbation

We will now perturb the values in the state equations to get started with the small signal analysis,

$$\dot{X} + \dot{\hat{x}} = (\alpha T_r/2 + \beta(T_S + \hat{t}_S)/2)(X + \hat{x}) + (\theta T_r/2 + \delta(T_S + \hat{t}_S)/2)(I_g + \hat{i}_g)$$

where α=0 to give,

$$\dot{X} + \dot{\hat{x}} = (\beta(T_S + \hat{t}_S)/2)(X + \hat{x}) + (\theta T_r/2 + \delta(T_S + \hat{t}_S)/2)(I_g + \hat{i}_g)$$

Rearranging and collecting terms in the above equation we get,

$$\dot{X} + \dot{\hat{x}} = AX + BI_g + A\hat{x} + B\hat{i}_g + \frac{\beta \hat{t}_S}{2}X + \frac{\beta \hat{t}_S}{2}\hat{x} \qquad (6.14)$$

Ignoring the last term that is a product of two perturbations we get,

$$\dot{X} = AX + BI_g \quad \text{and} \quad \dot{\hat{x}} = A\hat{x} + B\hat{i}_g + \frac{\beta \hat{t}_S}{2}X$$

$\frac{\hat{t}_S}{2} = \frac{1}{2\hat{f}_S}$ where $\hat{f}_S$ is the perturbed switching frequency .

We have separated the DC and the perturbed (small signal) expressions from the Equation (6.14).

Rewriting the small signal expression from Equation (6.14) in terms of parameters of the inverter we obtain,

$$\dot{\hat{x}} = A\hat{x} + B\hat{i}_g + M\hat{f}_S \qquad (6.14a)$$

where

$$A=\begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{2C_1Fr} & \frac{-1}{2C_1Fr} \\ 0 & 0 & 0 & 0 & \frac{-1}{2C_2Fr} & \frac{-1}{2C_2Fr} \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S F_S} & 0 \\ 0 & 0 & 0 & \frac{-1}{2C_p R_o F_S} & \frac{n^2}{2C_p F_S} & 0 \\ 0 & \frac{1}{2n^2 L_S Fr} & \frac{1}{n^2 L_S Fr} & \frac{1}{n^2 L_S Fr} & 0 & 0 \\ \frac{-1}{2L_m Fr} & \frac{1}{2L_m Fr} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$B=\begin{bmatrix} \frac{1}{2C_1Fr} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad M=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{n^2}{C_S F_S} & 0 \\ 0 & 0 & 0 & \frac{-1}{2C_p R_o F_S} & \frac{n^2}{2C_p F_S} & 0 \\ \frac{1}{2n^2 L_S Fr} & 0 & \frac{1}{n^2 L_S Fr} & \frac{1}{n^2 L_S Fr} & 0 & 0 \\ \frac{1}{2L_m Fr} & \frac{-1}{2L_m Fr} & 0 & 0 & 0 & 0 \end{bmatrix}$$

6.4 Derivation of transfer function

In general, a sixth order system may be presented in a state variable form as follows,

$$\dot{x}(t) = Ax(t) + Bi_g(t) \tag{6.15}$$

$$y(t) = Cx(t) \tag{6.16}$$

where,

$$X^T = [x_1 \quad x_2 \quad x_3 \quad x_4 \quad x_5 \quad x_6]$$

x: 6x1 state vector where

A: 6x6 state coefficient matrix

B: 6x1 input state coefficient matrix

C: 1x6 output state coefficient matrix

i_g: 1x1 source vector

y: 1x1 output vector

Matrices A, B and C are defined earlier.

In linear systems, the coefficients of matrices A, B and C are constant, i.e. function of the system components. These will be a function of system parameters like the switching frequency.

If we assume a linear system, then applying Laplace transformations to Equations (6.11) and (6.14) will obtain:

$$X(s)=(sI-A)^{-1}BI_g(s) \tag{6.17}$$

$$Y(s)=CX(s) \tag{6.18}$$

where, I is a 6x6 identity matrix.

Substituting Equation (6.17) into (6.18) we obtain the general solution for Y(s):

$$Y(s)=C(sI-A)^{-1}BI_g(s) \tag{6.19}$$

The objective is to represent the dc-to-ac inverter by a continuous state-variable response as shown in Equation (6.19).

Since we are used to analyzing a linear system, we will apply linearization to the averaged model and obtain a linear time invariant system. The continuity approximation is valid when the input signal frequency is much lower than the switching frequency. Whereas, the linearization approximation is valid when the perturbation around the steady state is very small when compared to the steady state operating point. The use of this technique is motivated by the difficulty of solving switched circuits which are highly nonlinear.

The small signal transfer function of the output-to-input can be found for the state space equation by using the following equation

$$\frac{\hat{v}_0}{\hat{i}_g} = C[sI - A]^{-1} B \tag{6.20}$$

where the A, B and C matrices are defined in Section 5.2.

Applying these matrices with the values of the different parameters of the dc-to-ac inverter from the Table shown below will yield the solution for the dynamic model.

PARAMETERS	DESIGN VALUE
$V_{nc,peak}$ (normalized)	3.44
$V_{c,peak}$ (actial value)	206.4 V
f_{ns}	1.0
f_{nor} (normalized)	1.2
f_{or} (actual value)	166.7kHz
Qo	2.0
M	0.671
V_o	138.5 V
R_o	100.0 Ω
Z_{or}	50.0 Ω
C_T	39.91nF
C_P	47.0 nF
C_S	270.0 nF
f_{ir}	136.4kHz
L_S	86.11μH
L_m	0.97mH
L_g	3.0mH
C1=C2=C	10.0nF

Substituting the above designed values in Equation (6.13), Equation (6.18) is the numerical representation of Equation (6.13) given by,

$$\dot{\hat{x}} = 10^5 \begin{bmatrix} 0 & 0 & 0 & 0 & -500 & -500 \\ 0 & 0 & 0 & 0 & 500 & 500 \\ 0 & 0 & 0 & 0 & 37 & 0 \\ 0 & 0 & 0 & -2.13 & 212.8 & 0 \\ .06 & -.06 & -.116 & -.116 & 0 & 0 \\ -.005 & .005 & 0 & 0 & 0 & 0 \end{bmatrix} \bullet \begin{bmatrix} \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{CS} \\ \hat{v}_{CP} \\ \hat{i}_{LS} \\ \hat{i}_{Lm} \end{bmatrix} + \begin{bmatrix} \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{CS} \\ \hat{v}_{CP} \\ \hat{i}_{LS} \\ \hat{i}_{Lm} \end{bmatrix} \bullet \hat{i}_g \quad (6.21)$$

$$+ 10^5 \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 3.7E6 & 0 \\ 0 & 0 & 0 & -2.12E9 & 2.12E7 & 0 \\ 5806 & 0 & -11613 & -11613 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \bullet \begin{bmatrix} \hat{v}_{C1} \\ \hat{v}_{C2} \\ \hat{v}_{CS} \\ \hat{v}_{CP} \\ \hat{i}_{LS} \\ \hat{i}_{Lm} \end{bmatrix}$$

The Equation (6.21) shows that the perturbed x vector is dependent on the system components and the perturbed switching frequency.

The input-to-output transfer function is given by Equation below

$$H_1(s) = \frac{\hat{v}_0(s)}{\hat{i}_{Lg}} \quad \text{when } \hat{f}(s) = 0 \qquad (6.22)$$

From Equation (6.19) and (6.22) we can get the transfer function $H_1(s)$,

$$H_1(s) = C(sI - A)^{-1}B \qquad (6.23)$$

Substituting for C, B and A in Equation (6.23), we obtain the following transfer function for $H_1(s)$,

$$H_1(s) = \frac{1.6943E^{19}s^2 - 7.64E^{29}}{s^5 + 2.128E^5 s^4 + 9.87E^{11}s^3 + 1.574E^{17}s^2} \qquad (6.24)$$

The frequency response of the magnitude and phase of $H_1(j\omega)$ is shown in Figure 6.4.

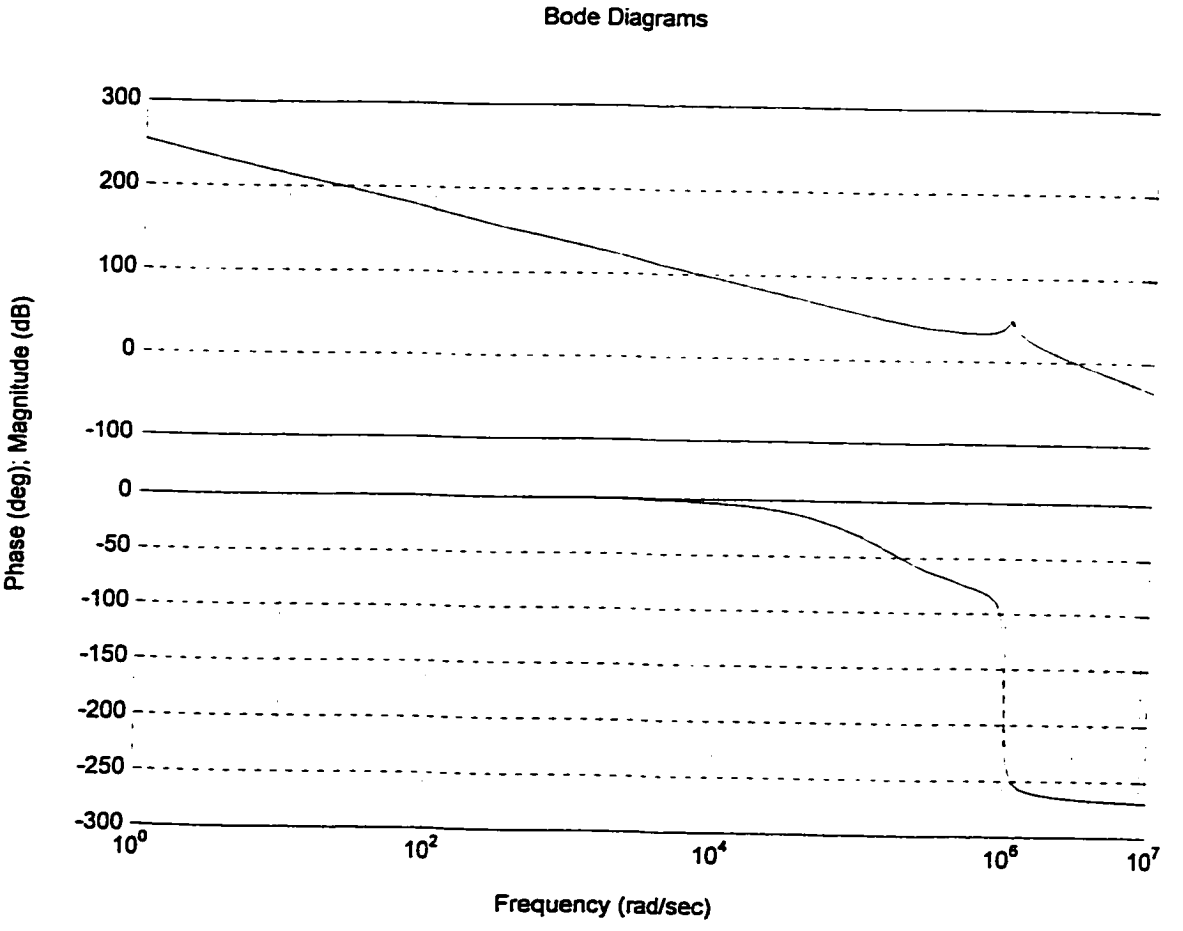

Figure 6.4 Frequency response plot of the magnitude and phase of $H_1(s)$

The control-to-output transfer function is given by Equation below

$$H_2(s) = \frac{\hat{v}_0(s)}{\hat{f}(s)} \text{ when } \hat{i}_{Lg} = 0 \tag{6.27}$$

From Equation (6.19) and (6.22) we can get the transfer function $H_1(s)$,

$$H_2(s) = C(sI - A)^{-1}M$$

From Equation (6.16) and (6.19) we can get the transfer function $H_1(s)$,

$$H_2(s) = \frac{4.371E^8 s^2 - 1.528E^{19}}{s^4 + 2.128E^5 s^3 + 9.87E^{11} s^2 + 1.574E^{17} s} \tag{6.28}$$

The frequency response of the magnitude and phase of $H_1(j\omega)$ is shown in Figure 6.5.

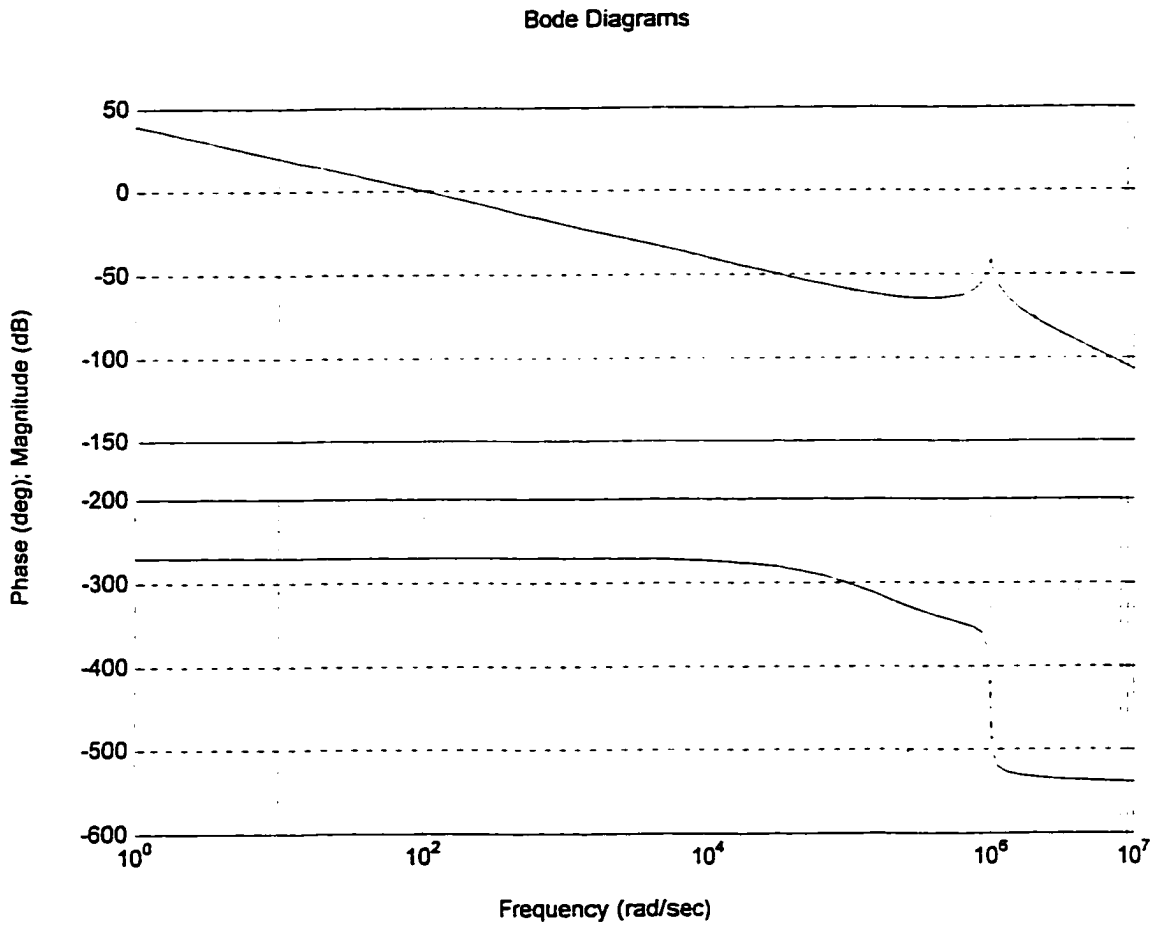

Figure 6.5 Frequency response plot of the magnitude and phase of $H_2(s)$

6.5 Frequency Response for various load values

The input-to-output transfer function for the load resistor values are derived and their frequency response are plotted. The different load resistor values used are 50, 70, 80, 90 and 100 Ω.

Figure 6.6 shows the magnitude and phase plots for the input-to-output transfer function for the above mentioned values of the load resistor.

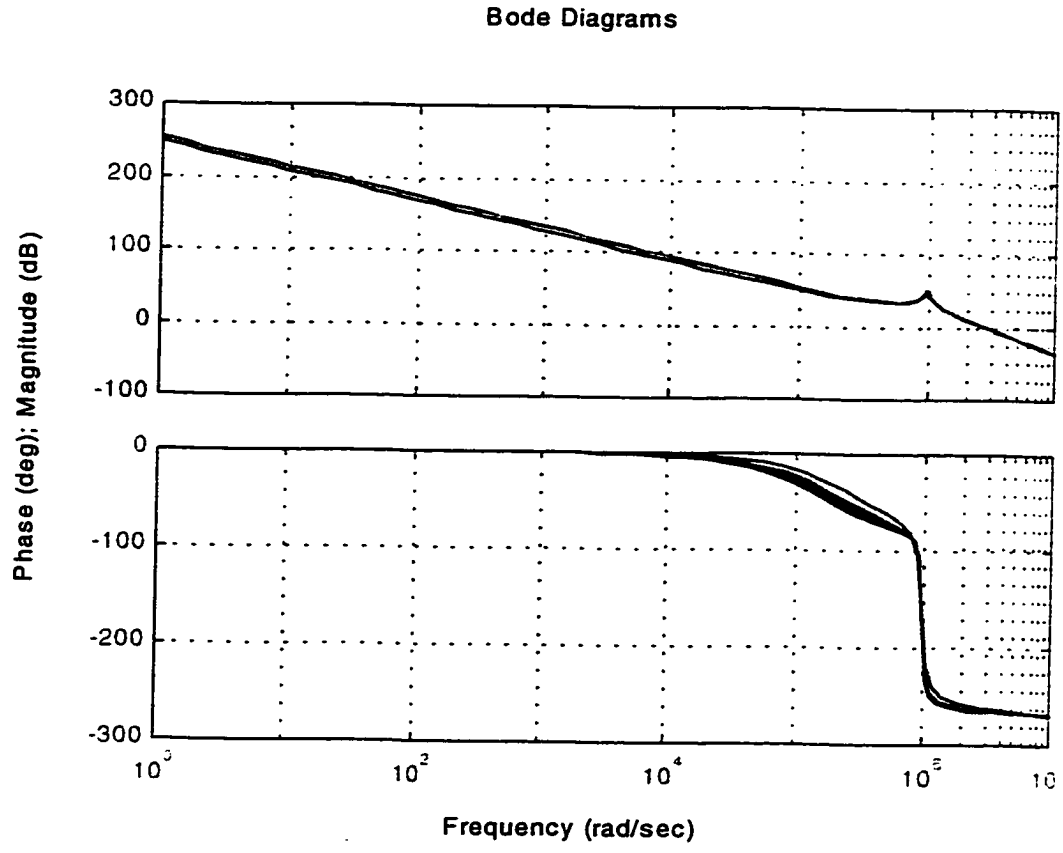

Figure 6.6 Frequency response plot of the magnitude and phase of $H_1(s)$ for different load values

Similarly, the control-to-output transfer function is derived for various values of the load resistor. The magnitude and phase frequency response plot of the transfer function for the load values of 50, 70, 80, 90 and 100 Ω is shown in figure 6.7.

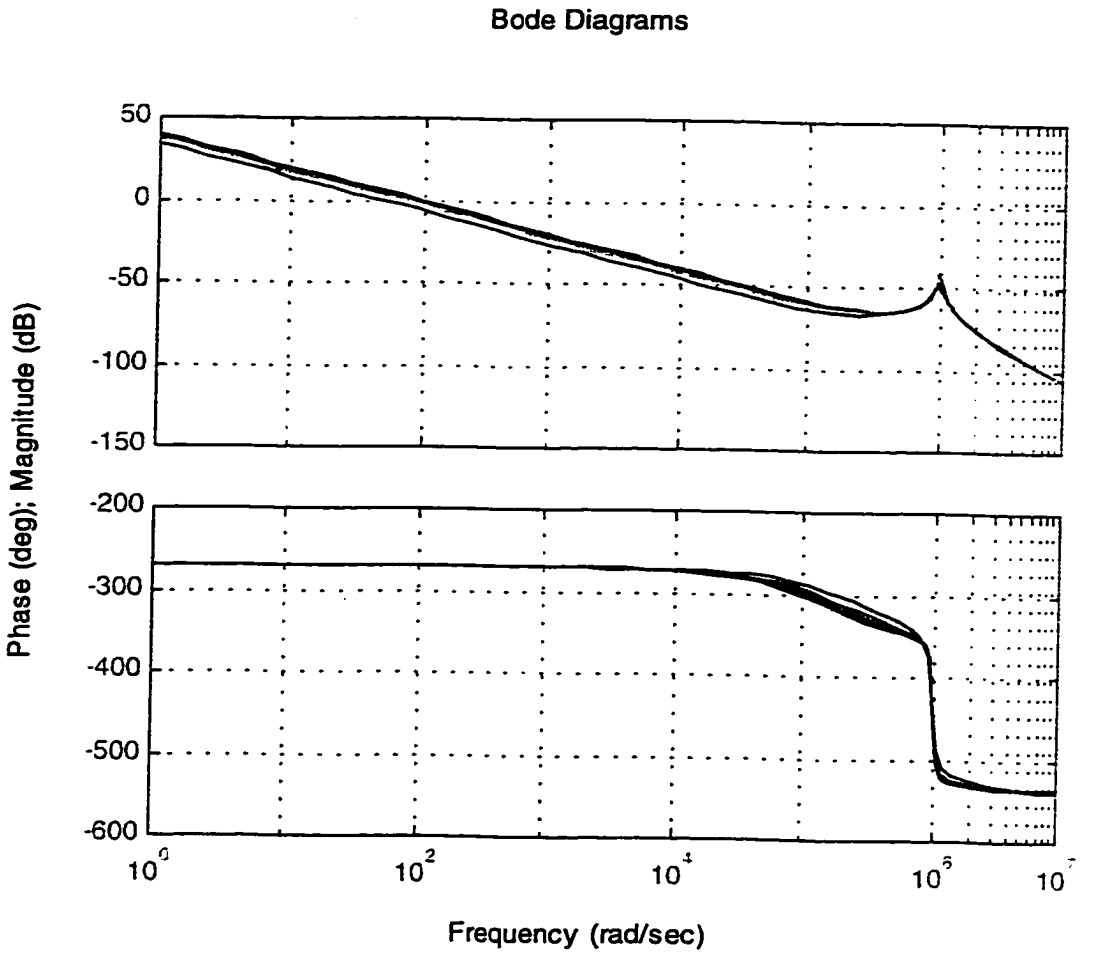

Figure 6.7 Frequency response plot of the magnitude and phase of $H_2(s)$ for different load values

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

The three isolated modified boost converters are presented with their topological diagram and basic circuit operations. The three topologies are the basic isolated boost, modified boost converter with active clamp and a modified boost with output network is introduced. The steady state analyses of these converters along-with their steady-state timing diagrams are presented. Zero-voltage-switching operations of these converters are demonstrated through theoretical, simulation and experimental results. It was shown that the theoretical, simulation and experimental results are in agreement for the three converter topologies. Comparison tables are presented to compare the various parameters for evaluation. Various conclusions are drawn from these tables. We have shown that the basic isolated boost converter is simple with hard-switched main switch and ringing voltage stress across the main switch. The modified boost converter with active clamp is more complex with hard-switched main switch. The modified boost converter with an output network has more circuit complexity, achieves soft switching for both switches and higher efficiency.

The basic isolated boost converter has a disadvantage of higher switching losses and high voltage stresses due to hard switching of both switches resulting in overall efficiency of 88%.

It was shown that the modified boost converter with active clamp has an advantage of lower switching losses compared to the basic topology.

Finally, due to zero-voltage-switching, the modified boost converter with an output network has an advantage of lower voltage stress, for a wide load range. The efficiency of this converter is 92%.

By utilizing the parasitic components and adding a resonant tank circuit, an isolated modified boost dc-to-ac inverter was introduced with its topological diagram. The topology is an isolated modified inverter with zero-voltage switching for both switches. A detailed principle of operation is presented with steady-state timing waveforms and an explanation of the four modes of operation is given. The steady-state analysis of this inverter is presented and a mathematical model was given in a matrix representation. Calculations for the output to input steady-state gain is calculated along with the peak voltage stresses for the two switches. The characteristic plots of this inverter are presented to show the relationship between the voltage gain versus the normalized switching frequency, normalized peak voltage stress versus the normalized switching frequency under different load values and normalized resonant frequency. Based on these characteristic curves, a detailed design example is given to demonstrate the ability to make design changes by following the design outline presented.

Based on these design parameters calculated, simulation on PSPICE is performed to verify the theoretical steady-state waveforms. The MOSFET model was approximated with an ideal switch with a diode and capacitor in parallel to simulate the dc-to-ac inverter. The simulation and theoretical waveforms are in full agreement, as shown with the detailed waveforms for various parameters of the dc-to-ac inverter.

An experimental inverter built was built and tested and its experimental waveforms were presented. The components used for this experimental circuit are based on the design parameter calculations done in the design example.

The experimental waveforms included all the related theoretical and simulation waveforms for comparison. A comparison table is presented to illustrate the agreement between the experimental, simulation and theoretical results.

Finally, small signal modeling of the dc-to-ac inverter is performed to show the behavior of the inverter with small perturbations in the input and switching frequency. State space averaging technique is utilized to linearize the four nonlinear modes of the inverter from the detailed steady state mathematical average model. The input-to-output and control-to-output transfer functions are derived and a specific numerical transfer function for the inverter in the design example is presented. The frequency response of the magnitude and phase of the two transfer functions are presented. A comparison of the transfer function frequency response is done for various load values.

As mentioned in Chapter 1, there is a need to have improved power factor correction topologies to improve the harmonic injection into the utility lines by the switching power supplies. There is a need for soft switching power converter topologies with higher efficiency and power density. A very strong interest in digital dc and ac motor drives is prevalent in the industry at the moment. Total digital drives are very reliable and easy to maintain with extensive troubleshooting and fault codes. The additional safety, convenience and performance features are an obvious advantage in the digital drives area. There is an inherent need for better and more reliable power converter topologies in the areas of vector-controlled, variable frequency scalar drives. The

improvement in the control strategy and power converters in the digital drives area has good prospects. The interfacing between the power converters and the "digital control" logic circuit is important with many challenges to get high performance drives.

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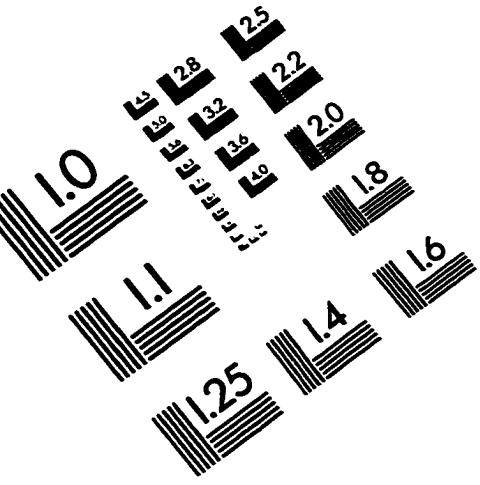
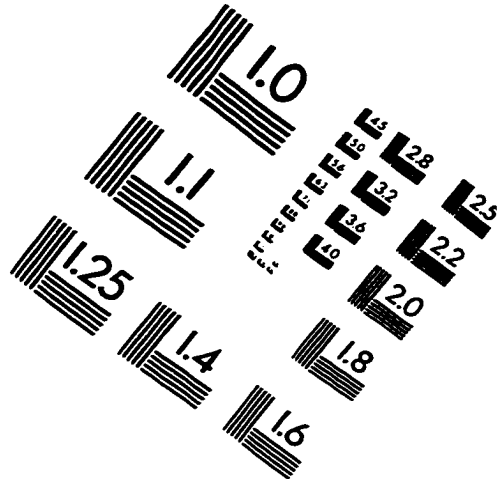
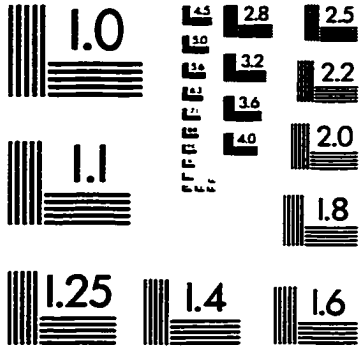
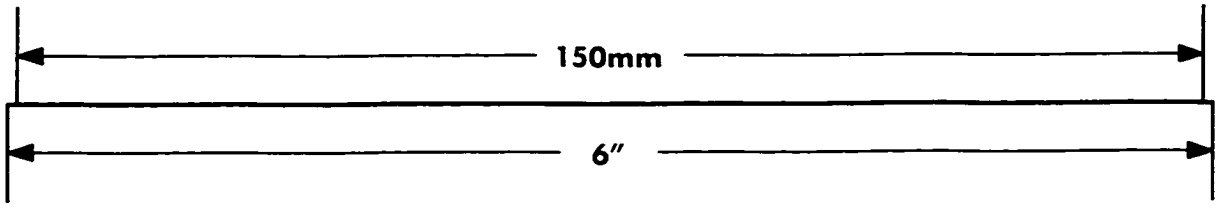
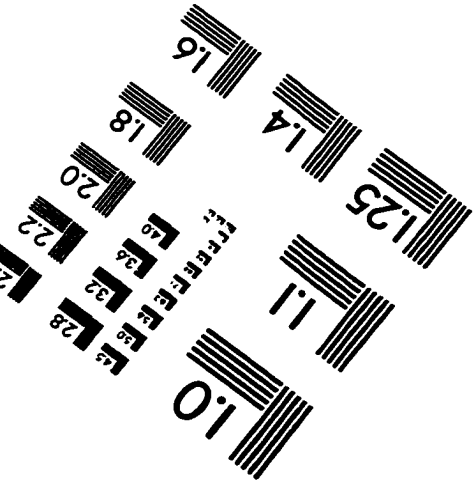
IMAGE EVALUATION TEST TARGET (QA-3)

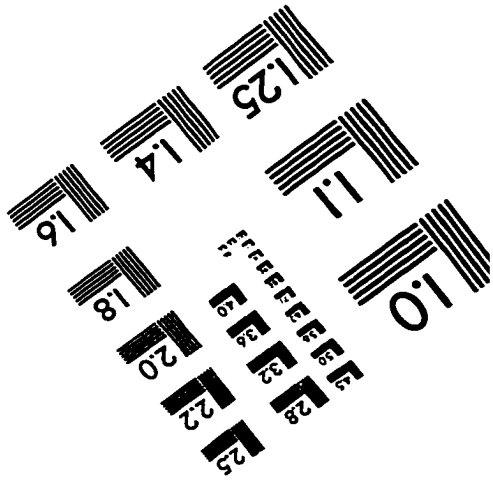












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