High-density And High-efficiency Soft Switching Modular Bi-directional Dc-dc Converter For Hybrid Electric Vehicles

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HIGH-DENSITY AND HIGH-EFFICIENCY SOFT SWITCHING MODULAR BI-DIRECTIONAL DC-DC CONVERTER FOR HYBRID ELECTRIC VEHICLES

by

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                     John Shen

ABSTRACT

This dissertation[1] presents the design of a high-density and high-efficiency soft-switching bi-directional DC-DC converter for hybrid-electric vehicles. The converter operates in a new bi-directional interleaved variable-frequency quasi-square-wave (QSW) mode, which enables high efficiency, high switching frequency, and high power-density. The converter presented utilizes a new variable frequency interleaving approach which allows for each module to operate in an interleaved position while allowing for tolerance in inductance and snubber capacitor values. The variable frequency interleaved soft-switching operation paired with a high-density nanocrystalline inductor and high-density system structure results in a very high performance converter, well exceeding that of the current technology. The developed converter is intended to achieve three specific performance goals: high conversion efficiency, high power density, and operation with 100 °C coolant. Two markedly different converter prototype designs are presented, one converter using evaporative spray cooling to cool the switching devices, with the second converter using a more traditional coldplate design to cool the switching devices. The 200 kW (25 kW per module) prototype converters exhibited power density greater than 8 kilowatts/liter (kW/L), and peak efficiency over 98%, while operating with 100 °C coolant.

To my loving wife, my supportive family, and my beautiful son

ACKNOWLEDGMENTS

Thank you to my advisors Dr. Issa Batarseh and Dr. John Shen for their unyielding support and guidance throughout the development of this work, as well as my academic progression. Few students are as blessed to have advisors who are so giving, knowledgeable, and respected. Also thank you to the members of the Florida Power Electronics Center for their contributions and support of this work. The development of the outstanding power converters presented in this dissertation has been a collaborative work between members of the University of Central Florida, the Advanced Power Electronics Corporation, and the United States Army, any of whom without would have been a great detriment to the project. The exceptional work of Rene Kersten, Michael Pepper, Keith Mansfield, Khalid Rustom, and Adje Mensah deserves special recognition. Additionally, thank you to my committee members Dr. Thomas Wu and Dr. Louis Chow. Also thank you to Dr. Kasemsan Siri for being an excellent technical reference throughout my academic career. And last but not least, thank you to my wife Lindsey and my parents for their support and inspiration.

Sincerely,

John Elmes

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CHAPTER 1: INTRODUCTION TO DC-DC CONVERTERS FOR ELECTRIC VEHICLE AND HYBRID/ELECTRIC VEHICLE APPLIACTIONS

Transportation vehicles are a mainstay of the world economy, and are embodied in many forms, including bicycles, cars, and mass transit vehicles. The basic technology for propelling a vast majority of automobiles is the internal combustion engine (ICE), which is generally inefficient, and has many potential environmental and social implications. In the more recent history of automobiles, there has been a great degree of advancement in the efficiency and overall function of vehicles, with a general trend towards the use of electric motor drive systems and on-board bulk energy storage. These newly developed vehicles often will have varying drivetrain structures, but will usually contain an electrochemical battery, a motor-drive inverter, and an electric traction motor. One important component in the modern electrical drivetrain is the high-power DC-DC converter, which can process the energy flow between the vehicle drive system and the traction battery or ultracapacitor, which is where the focus of this dissertation lies. Extensive overviews of electric and hybrid-electric vehicle configurations and structures can be found in [1] and [2]

EV/HEV Advantages

A electric vehicle (EV) or hybrid-electric vehicle (HEV) has the distinct ability to efficiently transfer the potential energy from the vehicle battery to kinetic energy in the vehicle during acceleration, and later convert the kinetic energy back into potential energy in the battery during regenerative braking. This ability is a significant step forward in comparison to a traditional ICE drivetrain, which can only transfer the potential energy of the fuel into heat and kinetic energy. Another advantage of the HEV is that the addition of electrical energy storage

can enable the vehicle to absorb load transients (acceleration and deceleration) with the electric drivetrain and battery, allowing the ICE to operate in a more steady and efficient manner, further increasing overall fuel economy. Some more modern examples of electrified vehicles with varying drivetrain architectures are shown in Figure 1.

Figure 1 General Motors EV1, Honda Insight, Chevrolet Volt, Toyota Prius

Simple Electric Vehicle Structure

The structure of the most simple electric vehicle drivetrain is shown in Figure 2. In this architecture, the battery will feed a DC-AC inverter, which modulates the DC input voltage using a 3-phase (typically) phase leg configuration, creating the necessary AC waveform to drive the motor. This structure is found in many smaller and inexpensive electric vehicles, such as a golf cart or neighborhood electric vehicle (NEV). This basic structure doesn't have provisions for an additional energy source from a ICE, and is typically lower in efficiency. A key reason for lower efficiency is that the nominal voltage of the battery tends to be lower, and since there is no DC-DC converter to increase the motor drive voltage, the motor drive system tends to be inefficient

and less powerful with lower voltages, due to less efficient motor design and higher RMS currents for a given power level.
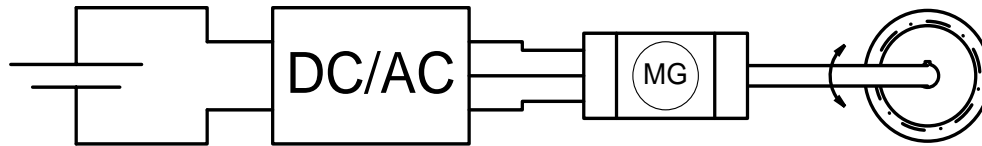
Figure 2 Basic Electric Vehicle Architecture

HEV System Topologies with DC/DC Converters

Hybrid-electric vehicles will often utilize a bidirectional DC-DC converter to boost the voltage from the traction batteries to a higher voltage DC bus, which allows for higher voltage electric motor drivetrains. A typical example system configuration is a vehicle with a 300 V traction battery, and a 650 V DC motor drive bus. The DC-DC converter has the potential to significantly increase the system efficiency, as it allows for the separate optimization of the battery voltage and the motor drive system. Furthermore, there is the potential for many system topologies and operating modes. Depending on the specific application, intended use of the vehicle, and the desired performance of the vehicle, there are numerous ways to configure the major power and drivetrain components. The following figures, Figures 3-9, outline most of the potential configurations.
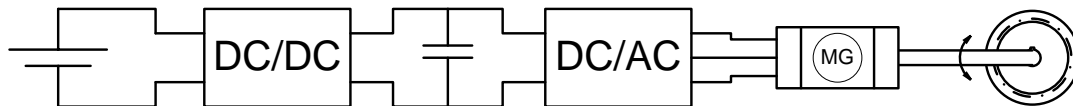
Figure 3 Electric Vehicle Architecture with DC-DC Converter

Figure 3 shows a typical architecture for a pure electric vehicle. In contrast to Figure 2, this configuration utilizes a bidirectional DC-DC converter. This converter must execute multiple control objectives simultaneously. The primary goal of the DC-DC converter is to

regulate the bus voltage, with the secondary goals of protecting the battery from over/under voltage conditions, or excessive charge or discharge currents. The direct benefit is that the battery can be optimized in design independently from the optimization of the motor and motor drive system. Although it is not theoretically bound, typically electric vehicle batteries are generally optimized for performance, cost, and reliability to have a bus voltage of around 300 VDC. As the battery voltage increases, the number of individual cells in series increases, which adds additional critical failure points, and complexity to the battery equalization circuitry. At lower voltages, the complexity of equalization is reduces, as well the number of critical failure points, but the system efficiency and cost will suffer, due to higher currents and the necessity for larger conductors. Currently the optimal motor drive voltage tends to be significantly higher than the typical battery voltage, generally 550 VDC - 700 VDC. At this higher voltage, the conductors in the motors can be smaller, allowing for higher density and higher power rating motor drive components. Additionally, the semiconductor industry has tended to produce high-power IGBT devices, which are in quantified voltage rating steps. If the bus voltage increases too much, the cost and possibly performance of the motor drive DC-AC converters may suffer. Also, increased bus voltage will also increase the necessity for more high voltage isolation in the motor drive system, which can have negative impacts on the overall design.

Another important potential feature of an EV utilizing a bidirectional DC-DC converter is the ability for the system to dynamically change the voltage of the DC bus depending on operating conditions, increasing the overall system efficiency.
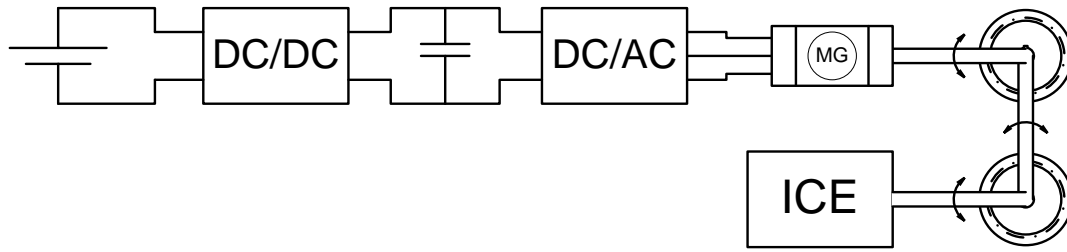
Figure 4 Parallel HEV Architecture

The architecture shown in Figure 4 is a parallel HEV system, where an ICE directly drives the driveshaft, in parallel with the electric drivetrain, which also drives the driveshaft. In this implementation, both the engine and the electric motor rotate at the same speed, as defined by the current speed of the vehicle. This topology allows for the electric drivetrain to augment the propulsion from the ICE, which is especially beneficial during acceleration. Also, this configuration allows the motor to act as a generator, and recharge the batteries during deceleration. This system architecture is the simplest of the HEV architectures, and as such, has some significant detractions. One major issue is that both the engine and the electric motor must always rotate, which can be wasteful, especially in cases where only the power from the ICE or the battery is desired. Also, this configuration doesn't allow the motor or ICE to operate in its most efficient rotational speed and output power, since it is physically coupled to the driveshaft.
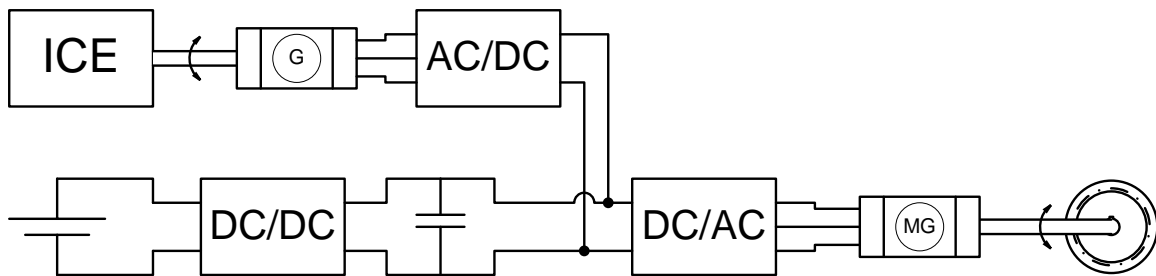
Figure 5 Series HEV 1 Architecture
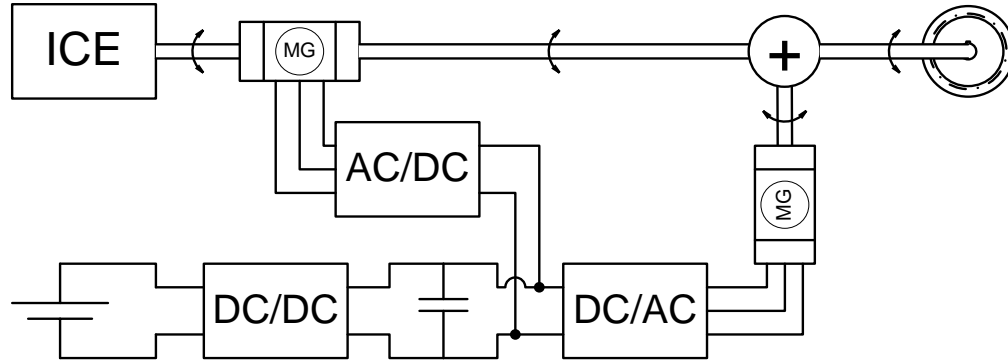
The HEV architecture shown in Figure 5 is known as a series hybrid, where the ICE drives a generator, of which the output is rectified by an AC-DC converter, to push power to the

DC bus. This system will allow the ICE to operate completely independently of the drivetrain, in a manner where the engine is capable of operating at the most efficient rotational speed and output power. The ICE will generate power which will drive the traction motor, and can also recharge the battery. Once the power from the ICE is not needed, the vehicle can turn off the engine, and allow the vehicle to operate as a pure EV. In this way, the fuel economy can be greatly increased in comparison to the parallel HEV. A negative of this system is that the total potential drive power is dictated by the traction motor, whereas the parallel HEV allows both the drive motor and the ICE to directly supply power to the driveshaft, increasing performance. Also, there is an additional penalty in the addition of the generator, which is not necessary in the parallel HEV.
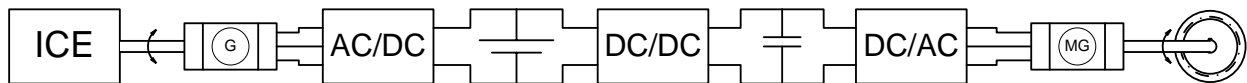
Figure 6 Series HEV 2 Architecture

The architecture shown in Figure 6 is another series hybrid configuration, where the ICE drives a generator, which creates power to recharge the battery and drive the motor drive system. This topology is different in comparison with the series HEV #1 in that the generator feeds the terminals of the battery instead of the HV bus. This may be more advantageous in a system where the power from the ICE is very high, and the engine will generally run for a shorter amount of time, and quickly recharge the battery. In this case, by removing the DC-DC converter from the power path from the generator, the battery recharging efficiency can be increased.

Figure 7 Series-Parallel HEV 1 Architecture

The system architecture in Figure 7 is an increasingly complex configuration, where two motor/generators are used in conjunction with an ICE and a differential gear to drive the output shaft. One of the motor/generators are directly in series with the output shaft of the ICE, which drives one input to the differential gear. The other motor/generator drives the other input to the differential gear. In this way, by precisely controlling the rotational speed of the motor/generators, the motor/generators can allow the ICE to maintain operation at an optimal rotational speed and power output, while also allowing the rotational speed of the driveshaft to vary with the speed of the vehicle, which is similar to a series HEV. Furthermore, during acceleration power from the ICE and the two motor/generators can be combined to achieve high output power to the driveshaft, which is similar to a parallel HEV. This topology necessitates more advanced electrical and mechanical controls, but the benefit is both increased efficiency as well as increased performance during acceleration and deceleration.
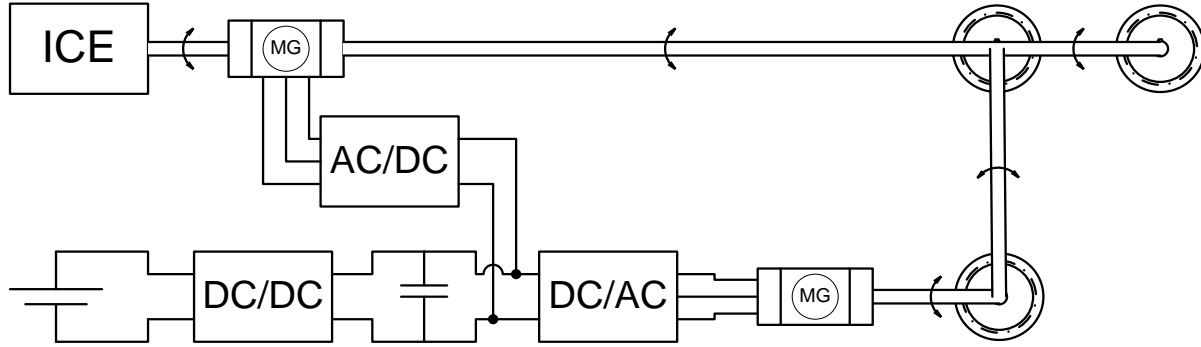
Figure 8 Series-Parallel HEV 2 Architecture

The HEV architecture shown in Figure 8 is another series-parallel configuration, similar to that of Figure 7, yet without the differential gear. This system is less efficient than the series-parallel HEV #1, yet it may have certain cost benefits. This is most similar to the parallel HEC, except that there is another motor/generator in series with the ICE. This can allow further improvement in acceleration, and can allow the ICE to charge the battery without requiring the mechanical energy to flow through the gears of the drivetrain to the other motor/generator.
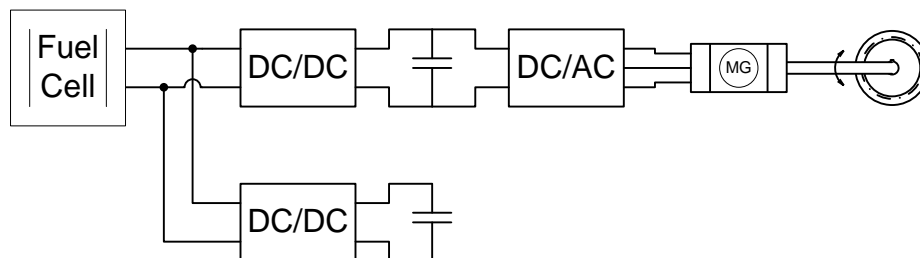
Figure 9 Fuel Cell Vehicle Architecture with Bulk Energy Storage Ultra Capacitor

The system shown in Figure 9 is a new potential architecture which could be useful in a fuel cell powered system. One significant challenge with a fuel cell vehicle is that the fuel cell is not especially suited for reacting to load transients. Because of this it is often necessary to include a large ultra capacitor on the output of the fuel cell, so as to allow the fuel cell more time to react. The downside of including a large ultracapacitor on the output of the fuel cell is that the full potential energy storage is not utilized, since the voltage on the capacitor only swings a

minimal amount. By configuring the system as shown in Figure 9, the ultracapacitor can be completely charged and discharged, allowing a reduction in the necessary capacitor size, saving size and cost.

Research Objectives: Specific Needs of the EV and HEV Industry

The needs of the hybrid-electric vehicle industry over the current technology are increased power-density, increased efficiency, and the capability for higher coolant temperature. A comprehensive roadmap for the electrical system and electronics of future electric vehicles has been created by the FreedomCAR program, which is a partnership between the U.S. Department of Energy, national laboratories, and many industrial partners. This roadmap, found in [3], not only addresses the key factors which require improvement, but it provides specific performance metrics for the electronics to achieve. Present systems generally require a lower temperature coolant than the coolant for the internal combustion engine (ICE), since the DC-DC converters cannot typically operate with coolant temperatures up to 100°C, as is typical for the coolant loop of the ICE. Often the DC-DC converter will require 70°C to 80°C coolant, which introduces a system density penalty, as the vehicle must have an auxiliary coolant loop specifically for cooling the power electronics. Also, the necessary size of the auxiliary coolant loop radiator will be large, since it is harder to reject the heat from a lower temperature coolant loop. In order to reduce the overall system cost, size, and complexity, it is ideal for the converter to be cooled by the main coolant loop, which is usually approximately 100°C. Further analysis of the potential cooling technologies, and the reasoning for the use of 100°C coolant can be found in [4] and [5].

The power density is important for system integration, as a large converter decreases the utility and efficiency of the vehicle. High efficiency is obviously important, since losses in the converter essentially reduce the effective efficiency of the system. Furthermore, increased

electrical efficiency will reduce the necessary cooling load and heat rejection on the vehicle cooling system, further increasing performance and decreasing cost. Based on the FreedomCAR roadmap, the target power density of the electric propulsion system for the year 2020 is 4 kW/L, and the target efficiency is 94%. Considering that these targets are for the DC-DC and the motor drive inverter, it is reasonable to assume that the target for the DC-DC converter should be approximately 8 kW/L, with efficiency reaching 97% between 10% and 100% load range.

Based on the work further referenced in this dissertation, specifically [14] and [20 - 24], there has been a great deal of research performed in the development of higher performance bidirectional DC-DC converters for electric vehicles. Through various implementations, there have been converters which achieve nearly 99% efficiency, and some DC-DC converters with power density exceeding 10 kW/L, which shows that the overall system goals are achievable, but will require a design which allows for the highest performance in each metric. Of particular relevance is [20], where a DC-DC converter of very similar structure to the converter presented in this Dissertation is demonstrated. This converter is similar in that it has the same soft-switching topology, but the control algorithm is much simpler, which has many detriments as described later, such as reduced efficiency and potentially dangerous operation in unexpected conditions and transients. Nevertheless, this converter presented is a good representation of the existing state-of-the-art, which demonstrates a power density of 6 kW/L and high peak efficiency.

The goal of the work presented in this Dissertation is to design a DC-DC converter capable of increasing the key performance metrics of the converter, specifically the power density, the efficiency, and the necessary cooling temperature. While the research to develop these converters doesn't necessitate any specific performance in each of the categories, the

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performance goals desired by the United States Army, who funded this work, serve as a good

benchmark to demonstrate superior performance compared to the available DC-DC converters.

Table 1 Key Performance Metrics, Threshold, Target, and Achieved Performance

Specification	Threshold	Target	Achieved
Power Density	6 kW/L 2 kW/kg	8 kW/L 4 kW/kg	8 kW/L 4.4 kW/kg
Peak Power	180 kW	--	200 kW
Average Power	150 kW	--	180 kW
Volume	--	--	25 L
Mass	--	--	45.5 kg
Output Voltage Range	580V – 640V	--	580V – 700V
Battery Voltage Range	250V – 530V	--	250V – 530V
Efficiency @ 5kW	91%	--	92%
Efficiency @ 30 kW	96%	--	97.5%
Efficiency (Peak)	--	--	98.5%
Max Coolant Temp	90ºC	100ºC	105ºC
Voltage Regulation	±3%	--	±1%
Current Regulation	±3%	--	±3%
Coolant Flow Rate	18 L/min	12.5 L/min	12.5 L/min
Pressure Drop	25 psi	--	16 psi

The goal for power density is to exceed 6 kW/L, with an ideal target of 8 kW/L. The

power density of typical industrially available DC-DC converters is approximately 4 kW/L,

which puts the performance goal at roughly double the power density of currently available DC-

DC converters. The goal for efficiency is to exceed 96%, with an ideal target of 97%. It is

difficult to specify the efficiency improvement over currently available DC-DC converters for

EVs, as it can depend on many factors, and is highly dependent on the design and operating

conditions. The main focus is to achieve efficiency high enough where there will be little

penalty for the use of a bidirectional DC-DC converter in a system. The goal for coolant

temperature is 100°C, which is a 20°C - 30°C improvement over currently available technology.

This will allow the converters to use the coolant directly from the high temperature coolant loop

of the vehicle engine.   All of the desired performance metrics as well as the achieved performance is shown in Table 1.

Technical Approach

To achieve the desired goals, significant advances must be made in multiple aspects of the DC-DC converter. The performance of the converter in the various categories is very intertwined, and the overall system improvement will depend on the improvement in each category. For example, if the efficiency is too low, the losses will be too high, which decreases the allowable coolant temperature as well as the peak power rating, which then reduces the power density. In this way, if significant gains can be made to each aspect of the converter design, the overall performance will benefit greatly. To increase the coolant temperature, it is necessary to both increase the cooling performance, and decrease the losses of the main semiconductors (insulated gate bipolar transistors, IGBT).   This is achieved through the development of a digitally controlled soft-switching DC-DC converter topology and control strategy. To increase power density, it is necessary to maximize the processed power per IGBT, which is defined by the maximum allowable losses per device, linking the efficiency to the available processed power, and thus the power density. Furthermore, it is critical to reduce the size of the passive storage components. This is achieved through a combination of advanced nanocrystalline inductor design, high density snubber capacitors, and a multiple module interleaving controller, which reduces the effective current ripple, and reduces the necessary bus filtering capacitors.

The work presented in this Dissertation illustrates the design of two different bidirectional DC-DC converters, one which uses an evaporative spray cooling approach, another

which uses high performance coldplates. Throughout the paper they are referred to as the spray cooled converter and the coldplate converter for convenience.

Dissertation Outline

The first chapter of this Dissertation is the introduction, which illustrates the utility, shortcomings, and technical approach to developing a high-density high-efficiency bidirectional DC-DC converter for hybrid-electric vehicles. The soft-switching topology and controller developed for this DC-DC converter system is given in chapter three. This soft-switching topology and control is employed in two distinctly different converters, which are described in detail in later chapters. The third chapter describes the development of high performance nanocrystalline inductors for the two DC-DC converters. The fourth chapter outlines the development of an evaporative spray cooling based bidirectional DC-DC converter, which uses custom IGBT modules to achieve very high switching frequency, and high coolant temperature. The fifth chapter outlines the development of a high performance coldplate based bidirectional DC-DC converter, which uses a coldplate structure which directly cools the IGBTs as well as the nanocrystalline inductors. The sixth chapter draws conclusions based on the findings from this research.

CHAPTER 2: SOFT-SWITCHING TOPOLOGY AND CONTROLLER

To achieve a high performance DC-DC converter which meets the current and future needs of the automotive and electric vehicle industry, a major feature of the converter is the ability to achieve soft switching on the main semiconductor devices. Soft switching is the general concept of operating a switching semiconductor device, either through circuitry or control, in a way which reduces the losses associated with the activation and deactivation of the device. The use of soft switching will allow the converter to operate more efficiently, and also may allow for higher switching frequency, which can allow for a reduction in size of the magnetics and filter capacitors. Based on the known voltage and current needs of the converter, it is readily apparent that the primary candidate for the main switching device is the IGBT. The necessary blocking voltage of the switch should exceed 1000V, and the maximum RMS current should exceed 200A per module, which precludes any standard MOSFETs from the application. For this reason the IGBT is the primary device for vehicular high power DC-DC converters and motor drive systems.

While the IGBT offers very low conduction losses and the capability to process high amounts of current, there is a significant downside which detracts from the performance in most IGBT applications, which is the switching loss. Compared to the MOSFET, the IGBT tends to transition between on and off states relatively slowly, and with a high amount of loss. For this reason, the IGBT is typically only operated with switching frequencies up to 20 kHz in a hard switched system, and often even lower, down to 5 kHz. By implementing a soft-switching behavior, the system will operate more efficiently, and was able to switch at up to 60 kHz.

Soft-Switching Overview

In literature one can find numerous soft-switching topologies which can potentially be implemented in a high power DC-DC converter. The concept of soft-switching is quite mature in the power electronics industry, with widespread use in many applications including server power supplies and point-of-load DC-DC converters, although, the use of soft-switching has not enjoyed much prominence in the high-power DC-DC converter field for automotive applications. Of particular interest for high-power DC-DC converter designs are topologies which can achieve high efficiency, don't require many additional components, and which don't insert additional passive elements in series with the very high current flow. One of the early works to analyze the operation of a topology very well suited for high-power DC-DC converters can be found in [6], which was published in 1987. One of the converters of interest is the zero voltage switching quasi square wave (ZVS QSW) converter. This topology is well suited in that it only requires the addition of two snubber capacitors in parallel with the main switching devices, and can achieve zero voltage switching at turn-on, and reduced current turn-off. Another important feature is that the topology is naturally bidirectional when synchronous switching devices are used. Further analysis of the topology, resonant behavior, and control was done by [7-10]. Later, an adaptation of the topology featuring coupled inductors was explored by [11]. The ZVS QSW converter presented in these works uses the converter in a constant frequency continuous conduction mode (CCM), which operates essentially exposes the inductor to a large constant current ripple, where the negative peak of the current must always conduct far enough below 0 A to allow the soft-switching resonant behavior to take place before the switching device is activated again. While the control is simple, there are specific drawbacks which make this

control strategy less desirable for high power bidirectional converters, specifically for HEV applications.

Advantages of constant-frequency ZVS QSW for high power bidirectional DC-DC

- Minimal additional components

- High efficiency at high power

- Naturally bidirectional if synchronous switching is used

- Easy PWM control

  o Interleaving is straightforward and easy to achieve

Drawbacks of constant-frequency ZVS QSW for high power bidirectional DC-DC

- High current ripple

  o Low efficiency at lighter load

- Loss of soft-switching at too high load

  o Likely damage will result

To increase the performance and utility of the converter, a variable frequency approach is preferred. A digitally implemented variable frequency approach to the QSW converter for VRM applications is presented in [12]. The first high power bidirectional variable frequency QSW DC-DC with interleaving, which is the topic of this dissertation, is presented in [13].

While there are many examples of electric vehicle purposed soft-switching converters in literature, there has not been a substantial use of soft-switching for industrially commercialized vehicles. While the reasons for a lack of adoption of soft-switching are probably numerous, there are key factors which have contributed to the nearly exclusive use of hard-switched converters.

- Additional hardware complexity

- o   Additional hardware cost

- Additional control complexity

  - o   Additional hardware cost

  - o   Potentially less reliable operation

- Additional development time

- Higher cost of development, including testing, debugging and verification

As would be expected, although there are many significant factors which have precluded the adoption of soft-switching schemes by industry, the main unifying factor tends to be cost, in the form of hardware cost, development time, and potential risk for converter failure. Notwithstanding, researchers continue to develop new and promising soft-switching DC-DC converters for electric vehicles, such as the new work presented in [14].

A major goal of this dissertation work, beyond the technical achievements, is to develop a DC-DC converter system which will have impact as a high performance converter which meets the future needs of electrified vehicles while having the potential to be commercially competitive with the traditional hard-switched approach.

IGBT Switching Losses

The IGBT exhibits high current handling and high voltage blocking capability, and has superior conduction losses at higher voltage applications compared to the MOSFET. The IGBT exhibits a low series resistance, yet has a series PN junction, in comparison to the MOSFET which exhibits a relatively higher series resistance, yet doesn't have a series PN junction. The result is that the MOSFET is more ideal at lower voltage applications, and the IGBT is more ideal for higher voltage applications, where the penalty of the series PN junction is not as severe. A significant difference though, is that the IGBT is a minority carrier device, whereas the

MOSFET is a majority carrier device. The result is that the IGBT exhibits slower switching, and hence, higher switching loss.

The switching losses (excluding driving losses) of the IGBT are from the product of the collector-emitter voltage and the current through the device. As is shown in Figure 10, on turn-on, the current tends to rise before the voltage falls, resulting in heating losses of the device. At turn off the IGBT current begins to fall as the voltage rises, but once the collector-emitter voltage reaches the peak, the current drop-off happens at a much slower pace. This is due to the fact that the IGBT is a minority carrier device, and once current is no longer being forced through the device, the recombination in the n- drift region occurs much slower. This period during the turn-off of the IGBT is known as the tail current. One important characteristic of the tail current is that the turn-off time will increase as the amount of current being turned-off decreases, since less minority carriers will be recombined initially. This behavior is important when designing the soft-switching circuit, as further decreased turn-off current produces diminishing returns on energy savings.
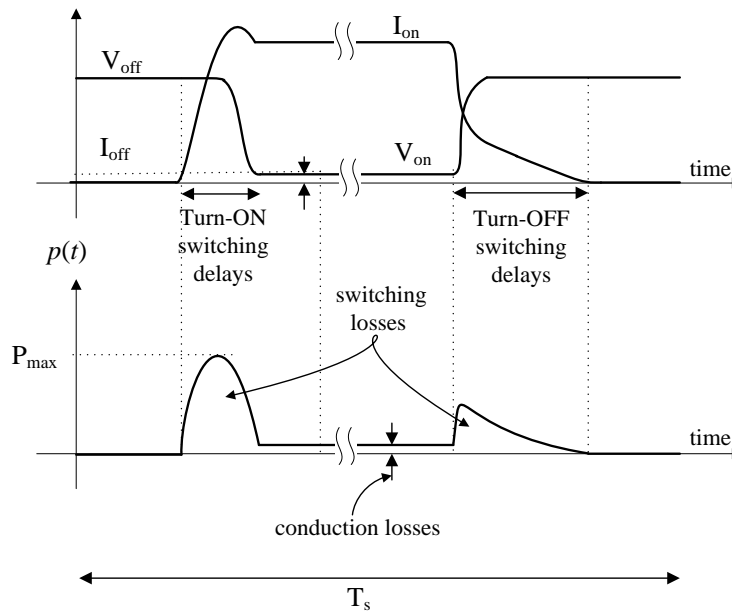
Figure 10 Hard-switched IGBT losses

The switching waveform shown in Figure 11 illustrates the IGBT in a soft-switched behavior. At turn-on, through some means the collector-emitter voltage is first reduced to 0 V before the IGBT is turned on. Once the IGBT is turned on, the current will slowly climb until it reaches the fully-on current. Since the switching losses are the product of the voltage and current across and through the device, the losses are essentially zero. This is known as zero voltage switching (ZVS), as the voltage across the IGBT is zero before the switch is enabled. At turn-off, the soft-switching behavior shown is also ZVS, where the rise rate of the voltage of the IGBT is by some means externally reduced, so as to reduce the losses due to the tail current during turn-off. The losses exhibited during turn-off are still a function of the tail current (albeit reduced) and the collector-emitter voltage. As discussed earlier, the switching time increases as the turn-off current decreases, so there is a practical limit to the amount of switching loss reduction that can be achieved through this method, as is described in [15] and [16].
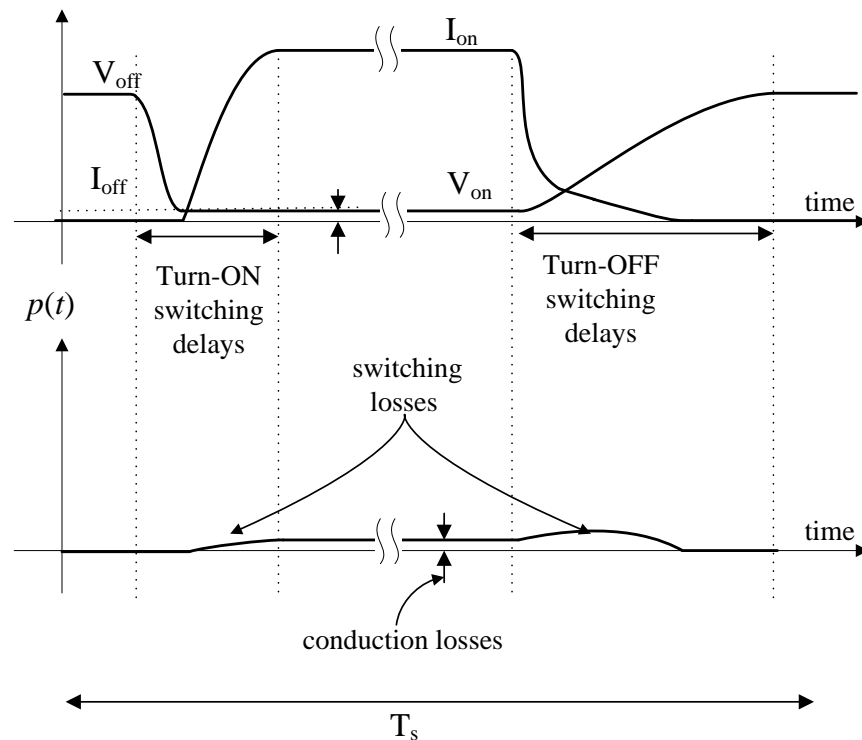
Figure 11 Soft-switched IGBT losses, ZVS turn-on, ZCS turn-off

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Topology Selection

There are numerous potential soft-switching DC-DC converter topologies which would reduce the switching losses, but each topology has pros and cons, which necessitates careful consideration for optimal design. A comparison of bidirectional topologies can be found in [17]. Some researchers have developed complicated structures which combine the DC-DC and AC-DC, such as in [18]. A bidirectional ZVT-PWM converter which could also be applicable is presented in [19]. To aid in the topology selection, a decision matrix was made, as shown in Table 2.

Table 2 Comparison of potential non-isolated DC-DC converter topologies

	QSW Const Frequency	QSW Var Frequency	ZVS Resonant Tank	ZVT-PWM Bidir	QSW W/ Aux enable switch
Bidirectional power flow	Yes	Yes	Depending on topology	Depending on topology	Yes
Soft-switched turn-on	Yes	Yes	Yes	Yes	Yes
Soft-switched turn-off	Yes (partial)	Yes (partial)	Yes	Yes (partial)	Yes (partial)
Minimal additional components	Yes	Yes	No	No	No
Reliability	Mid	High	Low	Low	High
Control complexity	Low	High	Mid	High	Mid
High peak efficiency	Yes	Yes	Yes	Yes	Yes
High low power efficiency	No	Yes	No	No	Yes
Fault tolerant	No	Yes	No	No	Yes
Power Density	High	High	Mid	Low	Mid

The constant frequency quasi square wave (QSW) soft switching converter, an example of which is shown by [20] and [21], is a good candidate, as there are minimal additional components, and it can achieve high peak efficiency. The downsides of the constant frequency

QSW converter is that the efficiency suffers at light load, due to the high current swing that is always present. Also, reliability is somewhat diminished, in that the converter must never be allowed to be loaded beyond the maximum designed output current for a given set of operating conditions. An attempt at improving the performance of the constant frequency QSW converter was presented in [22], where the converter is still operated as constant frequency, yet the controller performs frequency hopping at different discrete load levels, thus approximating variable frequency control. If the constant frequency QSW DC-DC converter was to operate at too much current, the soft-switching operation would fail, and the converter would likely fail. The topology for the QSW converter (both constant frequency and variable frequency) is shown in Figure 12. Additional approaches to the challenge are shown in [23 - 27].
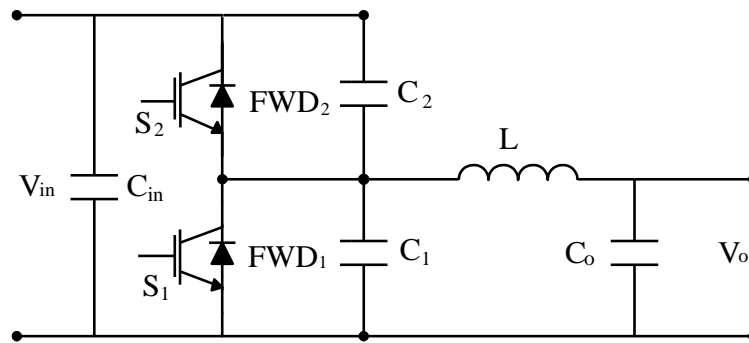
Figure 12 Quasi square wave soft switching power stage

To further improve the efficiency and reliability of the constant frequency QSW approach, a new control methodology for the QSW topology was created. The variable new frequency controller is significantly more complicated than the control necessary for the constant frequency method, yet can allow for significant improvements in performance and reliability. Since embedded digital controllers have become quite powerful and inexpensive, the higher control complexity doesn't have a significant cost or size penalty. Other topologies such as the ZVS and ZVT converters require a significant amount of additional hardware, which will reduce

power density, increase cost, and potentially decrease reliability. Based on a comprehensive comparison of potential converter topologies, it was determined that the QSW converter topology is most ideal, given that a new variable frequency controller system can be achieved reliably.

The DC-DC converter system is comprised of 8 separate DC-DC converters, which are connected through a distributed DC bus, and are controlled so as to be fully interleaved in time, so as to reduce the current ripple experienced by the bus capacitors.
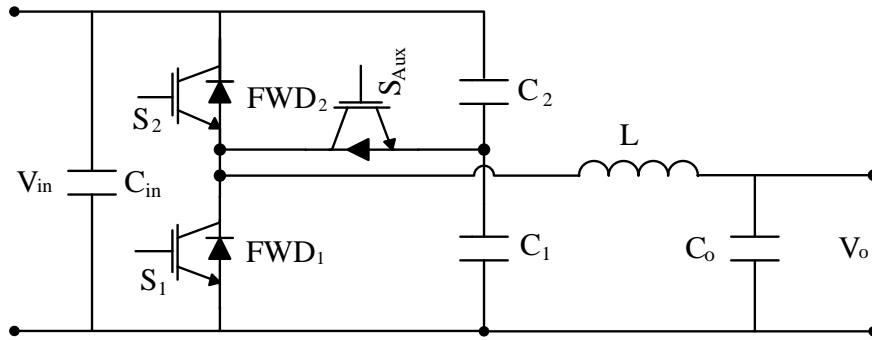
Figure 13 Quasi square wave soft switching power stage with auxiliary enable switch

One significant challenge with the proposed QSW converter is that during certain operating conditions, it may not be ideal to have the snubber capacitors connected across the IGBTs. During certain transient or startup conditions, it might be ideal for the converter to lose the soft switching operation. If the converter doesn't achieve ZVS at turn-on, all energy stored across the snubber capacitors will be discharged into the IGBT, significantly increasing the turn-on losses beyond the typical hard-switched operation of the device. Depending on the size of the snubber capacitors, how far away from ZVS the device is when it turns-on, and the thermal characteristics of the IGBT module, there is a limited number of times where a hard-switched turn-on can occur before permanent damage to the device occurs. One way to combat this issue is through the addition of an auxiliary enable switch, as shown in Figure 13. This would require

the addition of an IGBT between the snubber capacitors and the switch node of the converter. The drawbacks are increased cost, decreased density, the necessity for a custom IGBT module. Another major drawback is that there would be a reduction in efficiency, due to heating of the auxiliary IGBT, and a reduction in the quality of the soft-switching at turn-off, due to the additional resistance and inductance between the path between the snubber capacitors and the IGBTs. For these reasons, the QSW DC-DC converter with a new variable frequency control is selected.
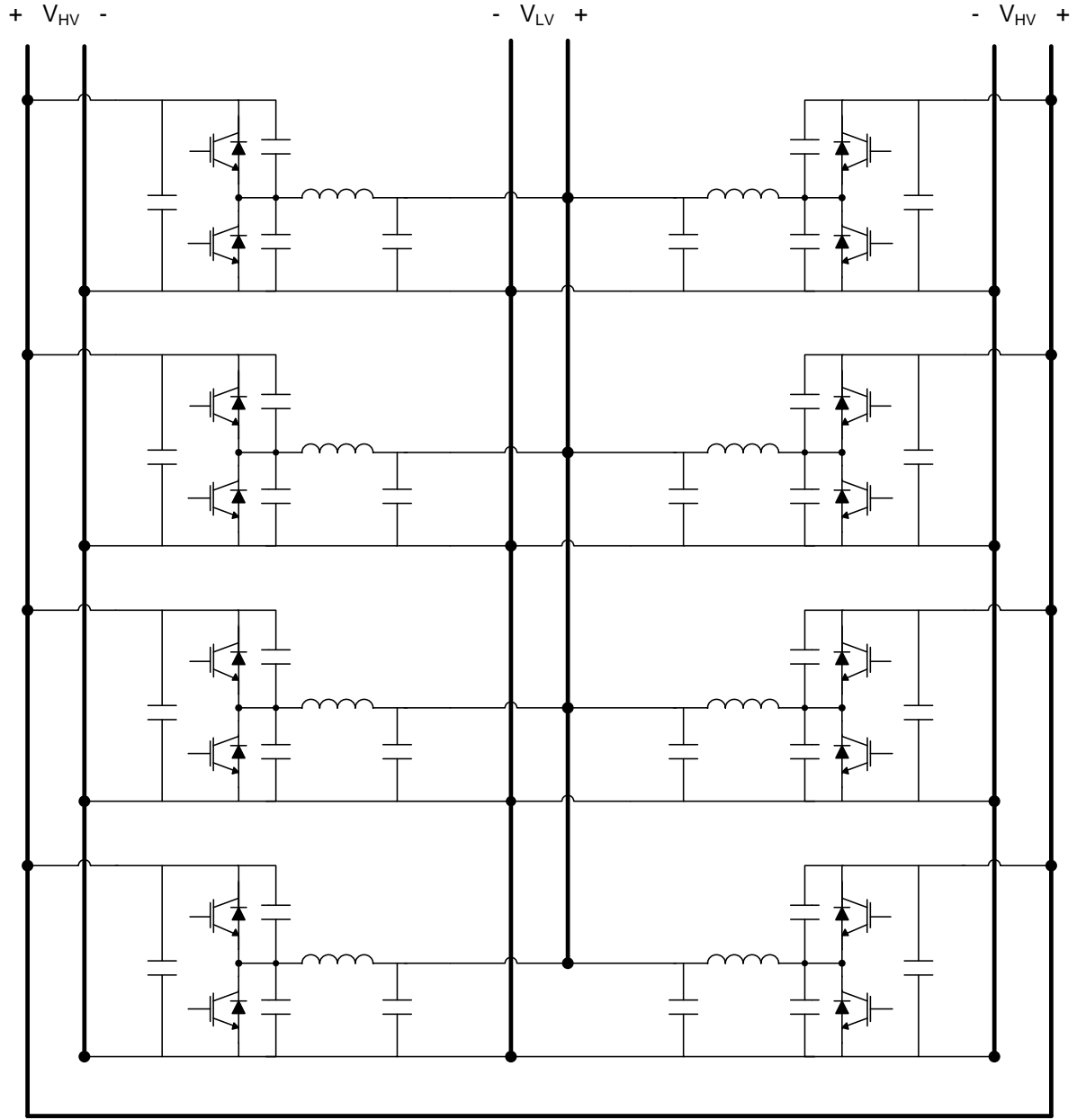
Figure 14 8-Module DC-DC with distributed bus

The modular high power DC-DC converter is a combination of multiple DC-DC converters, sharing a common DC bus. The bus capacitance is distributed between the individual DC-DC converter modules, and ideally the converters are operated in an interleaved manner to reduce the necessary current ripple handling of the bus capacitors. The multiple module converter structure used in this work is shown in Figure 14. From a major hardware standpoint,

this would be identical to a hard-switched converter system, except for the addition of the snubber capacitors, which makes this approach very relevant to the future needs of the electric vehicle industry.

Variable-Frequency Boundary Mode Quasi Square Wave

For EV applications, there are numerous potential operating modes, which necessitate a digitally controlled bidirectional converter, capable of performing many advanced function, such as described by [18], which also presents a novel integrated bidirectional DC-DC converter. The QSW converter is designed to have the current ripple of the inductor much larger than the DC output current, thus operating with the inductor current dropping below 0 A every switching cycle. The QSW converter can naturally achieve soft-switching with constant frequency control, given that the appropriate duty cycle and dead-time is observed, and that the loading doesn't exceed the limit for the given operating condition. If the average current in the inductor rises too high, the current will no longer go negative during the off time, which will cause hard-switching, and likely destruction of the converter. The converters presented in this work are digitally controlled through a CPLD executed state-machine which actively controls the points at which the IGBTs will turn on and off. In order to control the desired output power, the control variable is the peak current that the inductor current will reach before the IGBT is turned off. Based on the converter operation theory, there is a minimum amount of negative current for a given operating condition that must be achieved in order to ensure soft turn-on of the IGBT. For this reason, the controller must force a minimum amount of negative current at all times, in order to achieve soft switching. The relationship between the output power and the inductor peak currents is shown in Figure 15. The result is a converter that will operate at a variable frequency to respond to the controller peak-current commands. A constant frequency PWM based soft-

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switching bidirectional DC-DC converter was presented by Zhang, Lai, Kim, and Yu (2007) which exhibited high efficiency at full load, but is not optimal at light load. A somewhat similar bidirectional DC-DC converter was later presented by Yu and Lai (2008), which implemented frequency hopping between discrete levels to achieve higher light load efficiency, while still maintaining the relatively simple constant frequency control. The new variable frequency boundary mode QSW converter further optimizes efficiency by operating with continuously variable frequency.
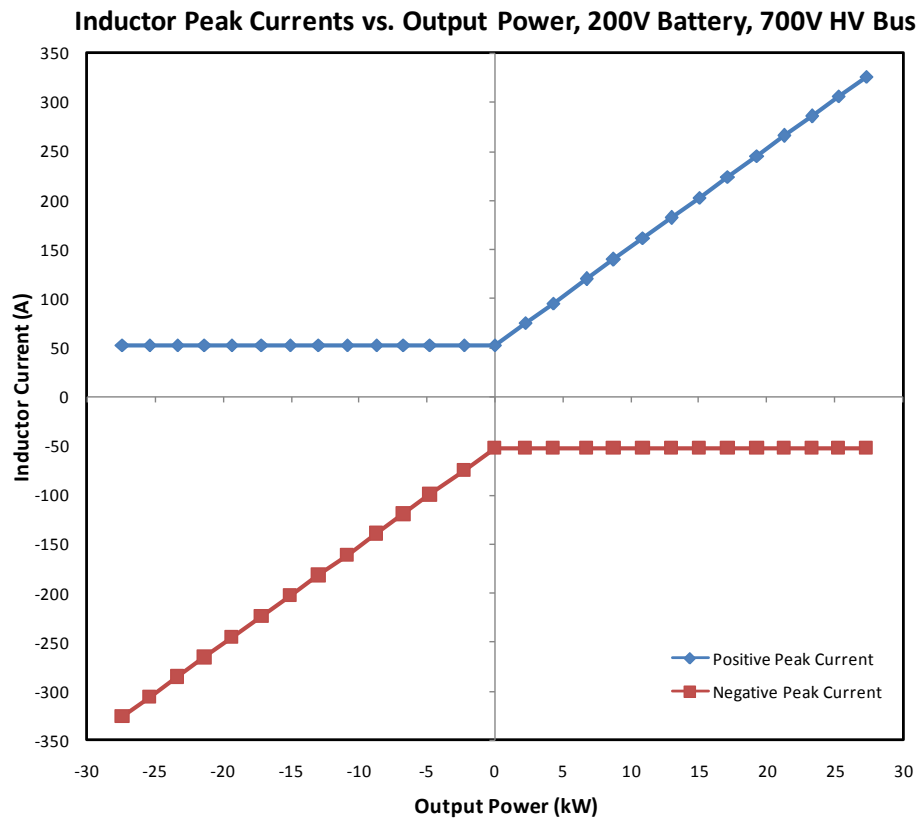
Figure 15 Inductor Peak Currents vs. Output Power

As can be seen in Figure 16, at low power operation the frequency is very high (up to 60 kHz), since the positive and negative peak currents will be nearly the same. As the power increases, the frequency will naturally decrease, since the positive current level will increase. This is advantageous, since lower switching frequency is ideal when the IGBT is processing

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higher amounts of current, since the switching losses tend to increase with higher switched current. At light load, the current ripple is much less than that of a system designed to operate at a constant frequency, which results in higher light-load efficiency.

2-Module Frequency vs. Power:
200V in 700V out
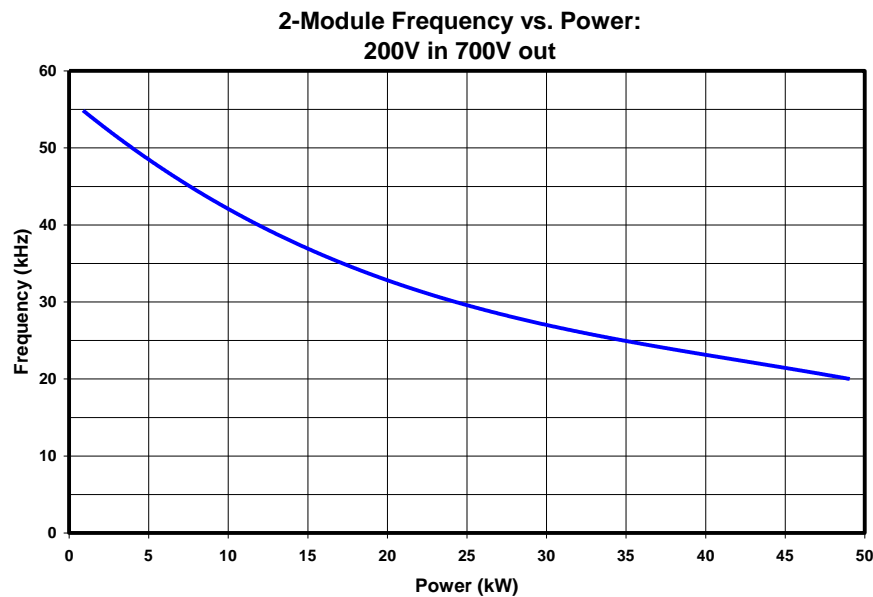
Figure 16 Switching frequency vs. output power

The proper system design will optimize the inductance and snubber capacitance to match the target power level and the characteristics of the switching devices. For example, an IGBT module known for lower switching losses and higher conduction loss would benefit from less snubber capacitance, as it will reduce the amount of circulated energy. A design using a slower IGBT with better conduction loss would benefit from higher snubber capacitance and lower switching frequency. The characterization of the switching losses at turn-off is somewhat complicated, since the IGBT will turn off slower when there is more snubber capacitance as described by [15] and [16], which indicates that there is a practical limit as to how much the turn-off losses can be reduced, depending on the specific device. Furthermore, the optimal snubber capacitor is not necessarily the value which results in the highest efficiency, since the small efficiency improvement with vary large snubber capacitance does not justify the additional

capacitor size. For each application the benefits of increased efficiency and power density must be compared.

The tradeoffs of snubber capacitance selection are similar to that of inductance selection. The optimal efficiency with respect to IGBT loss can be found with higher inductance, since this will result in low switching frequency, yet this is not optimal for overall system performance. The inductor will tend to have higher losses and higher volume as the inductance increases, which again opens the task of converter optimization to be subjective based on overall system goals. Furthermore, increased inductance decreases switching frequency, which further stresses the current ripple filtering bus capacitors, usually detracting from the system density.

The following converter operation characterizes the variable frequency control, where the positive and negative peak currents are actively controlled using analog comparators and digitally controlled analog references. For proper operation, the controller will set the negative current low enough so as to guarantee soft switching at IGBT turn-on. The positive current control will vary to control the power flow of the converter. When processing power in the opposite direction, the controller will maintain the positive current at a minimum value, and control the negative current to control the power flow. While the converter operation is bidirectional, for the purposes of this analysis, the operation is considered to be in Boost, or step-up mode, where Vout is the higher voltage DC bus, and Vin is the lower battery voltage.

Mode 1a ($t_o \leq t < t_1$)
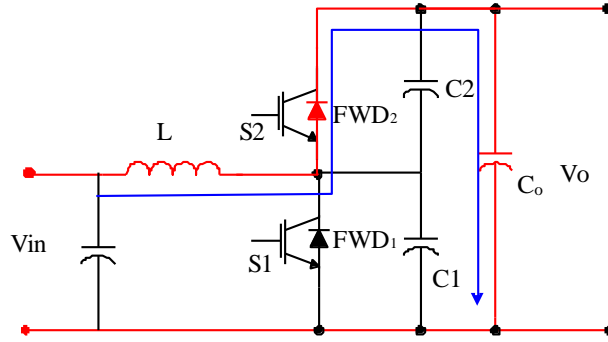
Figure 17 Mode 1a

As shown in Figure 17 Mode 1a begins with FWD$_2$ turning on at

$$i_L(t_0) = -i_{D1}(t_0)$$

(1)

The inductor during this mode will begin conducting through the anti-parallel diode 2 (FWD$_2$) which is in series with the input and output voltages. This will cause the inductor to discharge linearly into the input.

$$i_L(t) = \frac{V_{in} - V_o}{L} \cdot t + i_L(t_o)$$

(2)

This mode will end when switch S$_2$ is turned on under ZVS (Zero Voltage Switching).

Mode 1b ($t_1 \leq t < t_2$)
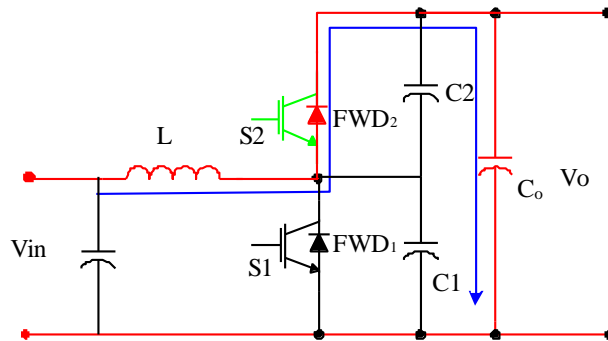
Figure 18 Mode 1b

S$_2$ and FWD$_2$ are both active, however, FWD$_2$ is the only device conducting. As with the previous mode, the inductor current is still linearly discharging into the input through FWD$_2$. This mode ends when the inductor current goes to zero. Thus, FWD$_2$ will turn off with ZCS (Zero Current Switching) and S$_2$ will begin conducting.

Mode 2 (t$_2$ ≤ t < t$_3$)
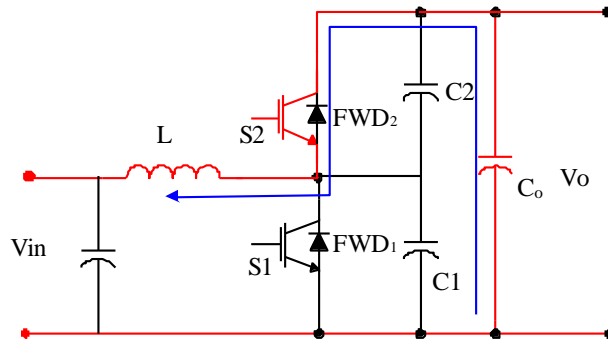
Figure 19 Mode 2

Mode 2 starts when the inductor current reached zero and S$_2$ starts conducting. This mode will end when the inductor current reaches the commanded current and S$_2$ is turned off. This maximum commanded current is:

$$i_L(t_3) = i_{max}$$

(3)

By controlling the switches by peak-current, the converter is naturally variable frequency, with the frequency decreasing with increased power.

Mode 3 (t₃ ≤ t < t₄)
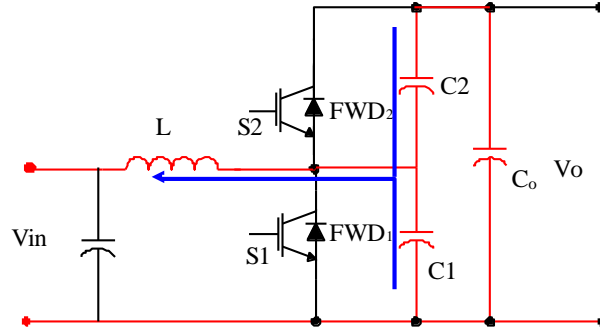
Figure 20 Mode 3

Mode 3 is the first of two resonant modes that the converter goes through to enable ZCS switching for the main switching devices. During this mode, all devices are off. The inductor current will resonate with the snubber capacitor's voltage; charging C_2 and discharging C_1. The capacitor C_1 will discharge down to zero, at which point FWD_1 will conduct with ZVS starting the next mode.

$$\omega_0 = \frac{1}{\sqrt{L \cdot (C_1 + C_2)}}$$

(4)

$$V_{C1}(t) = -\frac{i_{max}}{\omega_0(C_1 + C_2)} \cdot \sin(\omega_0 \cdot t) + (V_{in} - V_o) \cdot \cos(\omega_0 \cdot t) + V_o$$

(5)

$$V_{C2}(t) = V_{in} - V_{C1}(t)$$

(6)

$$i_L(t) = i_{max} \cdot \cos(\omega_0 \cdot t) + \omega_0 \cdot (V_{in} - V_o) \cdot (C_1 + C_2) \cdot \sin(\omega_0 \cdot t)$$

(7)

$$i_L(t_4) = i_{D2on}$$

(8)

Mode 4a (t₄ ≤ t < t₅)
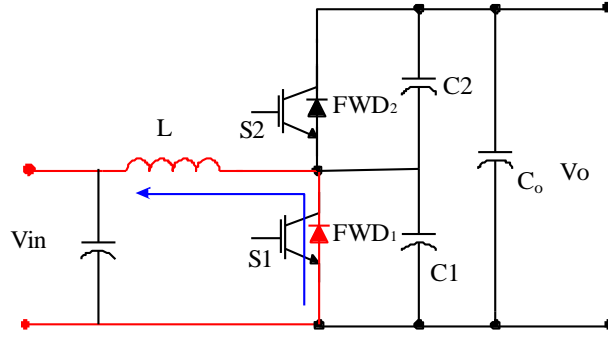
Figure 21 Mode 4a

Mode 4a begins with FWD_1 turning ON. The inductor current will discharge linearly due to the output voltage applied across the inductor.

$$i_L(t) = \frac{-V_o}{L} \cdot t + i_L(t_4)$$

(9)

This mode will end when the active switch S_2 turns on under ZVS.

Mode 4b (t₅ ≤ t < t₆)
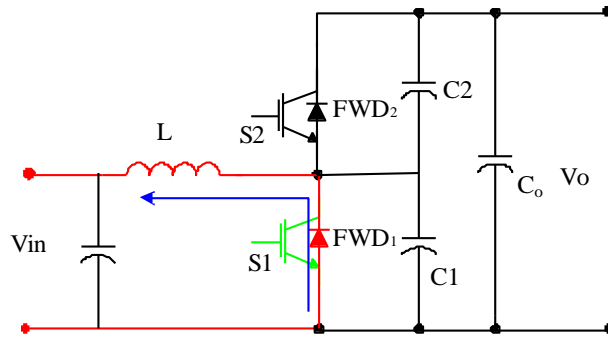
Figure 22 Mode 4b

Mode 4b starts when S_1 is turned ON under ZVS. In this mode both S_1 and FWD_1 are on however, only FWD_1 is conducting. This mode ends when the inductor current reaches zero and the FWD_1 will turn off with ZCS.

Mode 5 ($t_6 \le t < t_7$)
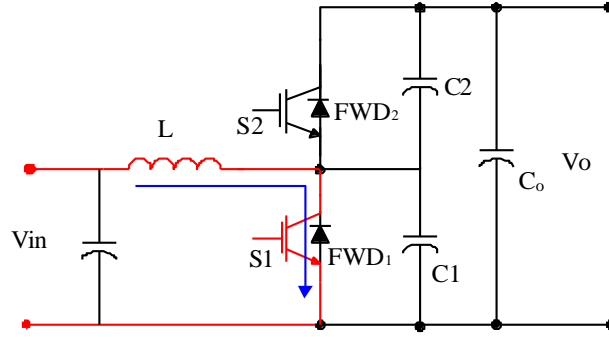
Figure 23 Mode 5

Mode 5 begins when the FWD$_1$ turns off under ZCS and S$_1$ still on. This mode will end when the inductor current reaches the negative commanded current and S$_1$ is turned off. The negative commanded current must be greater (magnitude) than the minimum current necessary to achieve soft-switching, i$_{soft\_min}$. This negative commanded current is:

$$i_L(t_7) = -i_{min} \tag{10}$$

The reason for this negative commanded current is to insure that ZVS can be achieved on the switching devices S$_1$ and S$_2$.

Mode 6 ($t_7 \le t < t_8, t_o, T_s$)
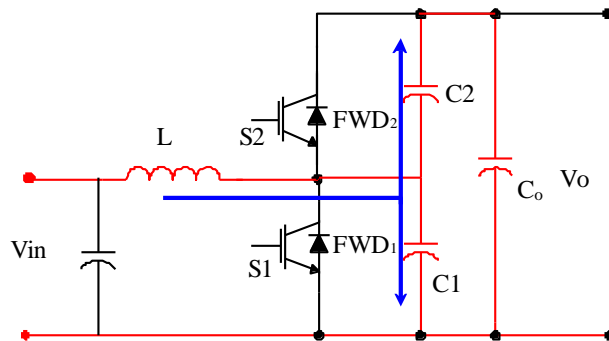
Figure 24 Mode 6

Mode 6 begins when S_1 is turned off. This will also begin the last resonant mode. This mode is similar to that of Mode 3 with the inductor current resonating with the capacitors C_1 and C_2. However, during this mode the inductor current will resonant with the capacitor's voltage charging C_1 and discharging C_2.

$$V_{C1}(t) = (\frac{i_{min}}{\omega_0(C_1 + C_2)})\sin(\omega_0 \cdot t) - V_o \cdot \cos(\omega_0 \cdot t) + V_o$$
(11)

$$V_{C2}(t) = V_{in} - V_{C1}(t)$$
(12)

$$i_L(t) = (-i_{min}) \cdot \cos(\omega_0 \cdot t) - V_o \cdot \omega_0 \cdot (C_1 + C_2) \cdot \sin(\omega_0 \cdot t)$$
(13)

At the end of this interval, V_{C2} will approach zero, and FWD_2 will turn ON under ZVS. The end of this mode's current is:

$$i_L(t_o) = -i_{D1on}$$
(14)
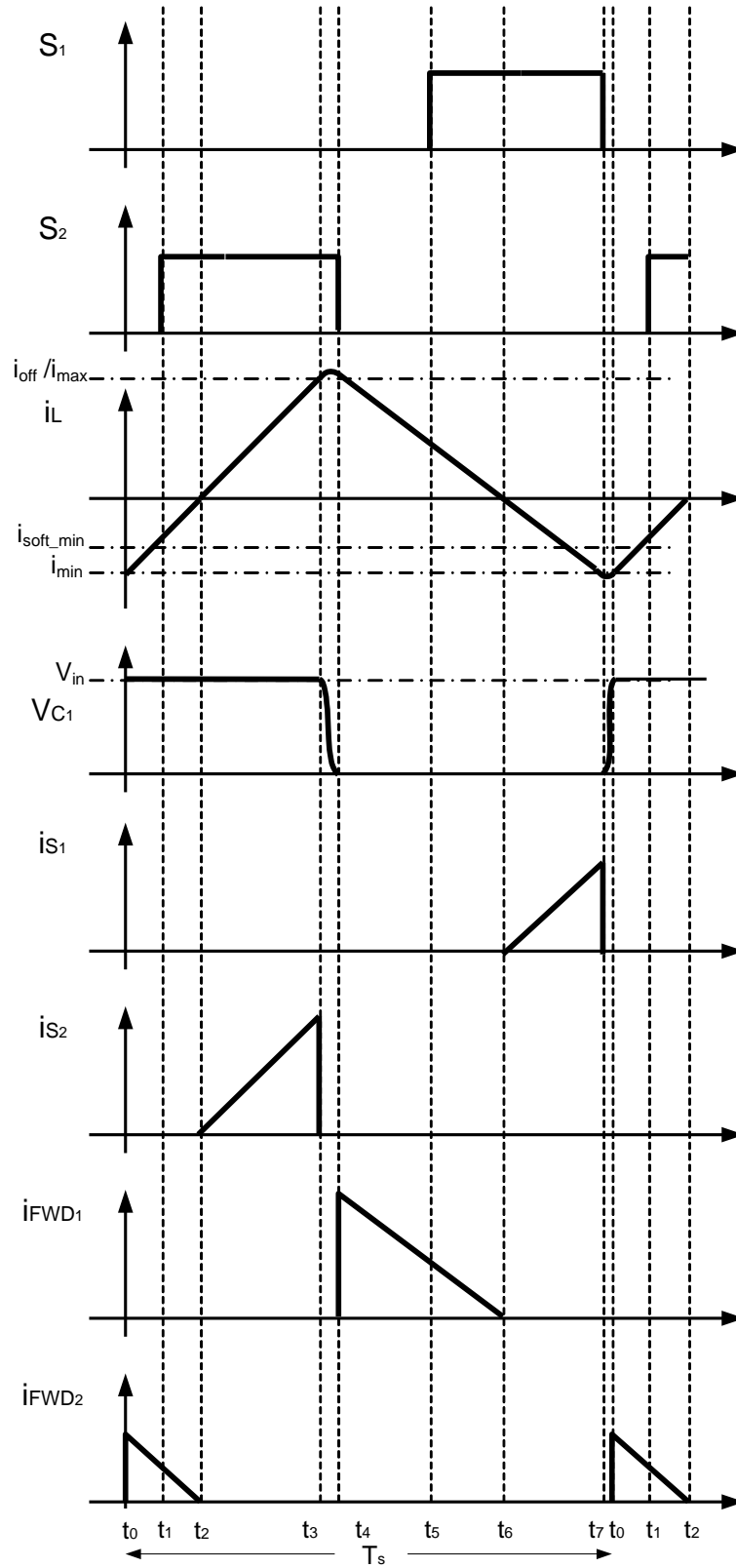
Figure 25 Switching Waveforms – (Low power operation for clarity)

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Soft Turn-On Detection

Unlike a traditional converter, in this topology, if hard switching occurs, there is a great possibility for damage to the IGBT, as the large snubber capacitors in parallel with the IGBTs will immediately discharge into the IGBT, thus having a very large current spike. For this converter, the inductance in the path from the IGBT to the snubber capacitors is very low, and the snubber capacitors have low ESR and ESL. The specific operating condition where the hard-switch event occurs will dictate how the IGBT is affected, and how often such an event can occur. Ultimately an IGBT will fail due to heating during the hard-switched events, including chip-wide heating from multiple less severe events, or possible from excessive current in a single severe event. In order to prevent this, there must be protection logic and hardware which only allow for hard-switched events to occur occasionally and when necessary for the continued operation of the converter.

The primary situation which must be protected against is to turn-on the IGBT with voltage across it, thus not achieving ZVS. To prevent this, comparator hardware is added, which compares the voltage across the IGBT to 0 V. Based on the operation of the QSW converter, the body diode of the IGBT should be conducting before the IGBT is enabled. When the body diode is conducting, the voltage from collector to emitter will be negative, due to the voltage drop of the diode, typically greater than -1 V. The comparator will indicate to the real-time controller implemented in the CPLD that the IGBT is not ready to soft-switch. Based on that input, the CPLD controller will wait longer until the soft turn-on detection indicates that it is safe to switch.
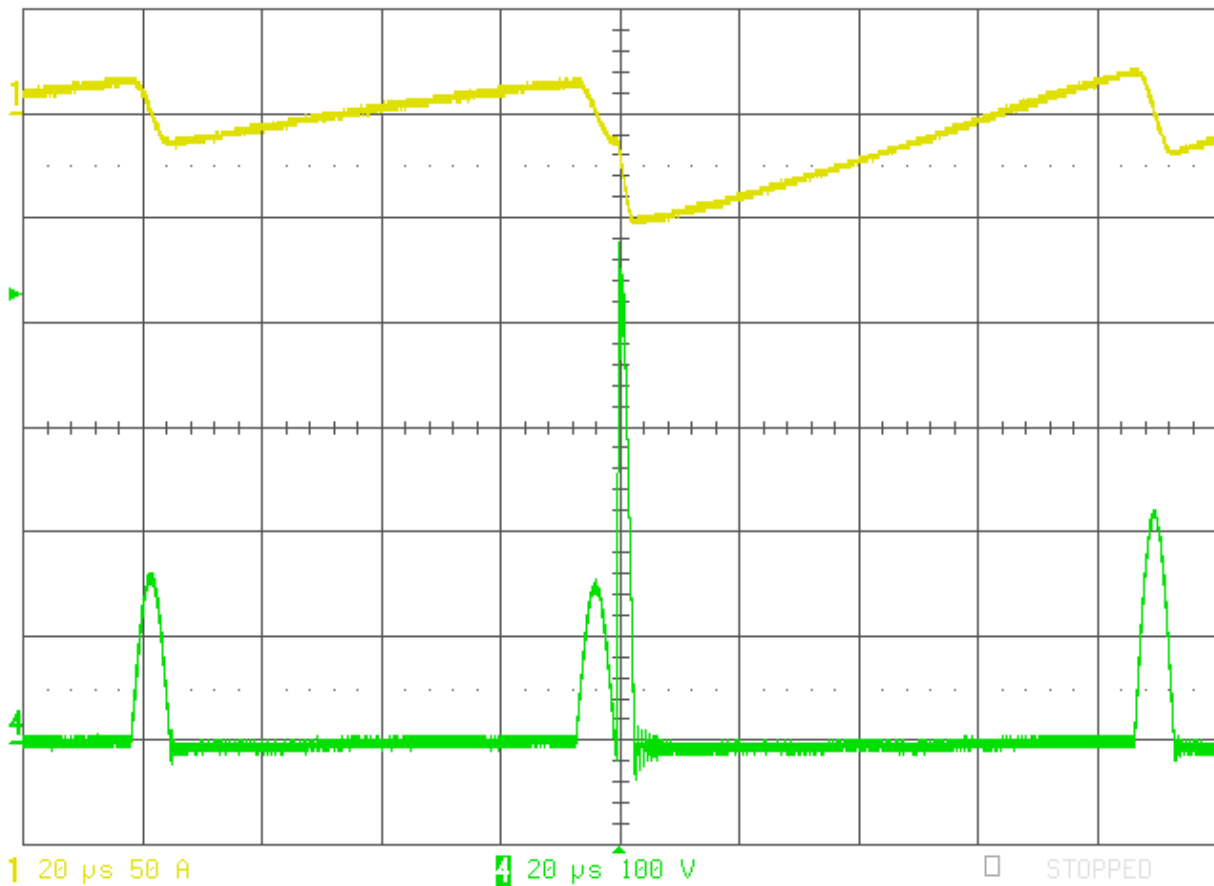
Figure 26 A hard switching event, showing high dv/dt on the switch node (signal #4)

Occasionally it may be desirable to enable a hard-switched turn-on in the system, as long as it will not cause damage to the IGBT. One condition where this is necessary is during initial startup, where the snubber capacitors have some voltage across them. Another case might be where there is a severe transient on the system and the input and output voltage changes quickly, causing the existing negative current setpoint to be too low, until the controller can recover. As long as the pulsed energy ratings well exceed the energy stored in the snubber capacitors, it can be safe to allow for a certain number of hard-switched events. The controller will count the number of hard-switch conditions, and disallow further hard switching for an appropriate amount of time, allowing the IGBT to thermally recover.

Variable Frequency Control

The variable frequency control is achieved through real-time peak current mode control, implemented in a programmable logic device, such as a complex programmable logic device (CPLD) or field programmable logic array (FPGA). The controller implements cycle-by-cycle control through a state machine, which relies on the peak current detection and soft-switching enable signals from the hardware. The peak current levels are commanded by a digital signal processor (DSP), which commands an analog compare setpoint to a digital-to-analog converter (DAC), which creates an analog voltage representing a specific current level for the IGBT to turn off. The current through the inductor is sensed and conditioned, and processed by the high-speed comparator, which communicates the necessity to turn off the IGBT when the current exceeds the commanded level. Based on this operation, the converter is continuously varying in frequency, where the currently existing operating conditions will dictate the switching frequency at any given moment.

CPLD Controller Operation

The CPLD performs the functions which require strict timing and real-time control, allowing the DSP to perform the more advanced control functions. The main tasks of the programmable logic device are to properly implement the pulse width modulation (PWM) with appropriate dead-time for each IGBT in the converter. A secondary task for the CPLD is to implement multiple levels of protection, to assure that the converter is controlled safely, and damage from unexpected conditions is avoided. Also, in order to achieve interleaved operation, the converter system is organized in a master/slave configuration, where the operation of one converter is a source of timing information for the other converters, allowing all of the converters

to delay themselves appropriately, and reduce the current ripple experienced by the bus capacitors.

Driving Logic

The CPLD's most advanced and primary function is the driver logic. The driver function accepts the signals from the upper and lower inductor current comparators, the current polarity feedback signals, the 0A detection signals, and the run command and mode select from the DSP. The driver will cycle through 4 states, which corresponds to each IGBT on-state as well as the dead-time between the switching. The following graphic illustrates the way in the state machines cycles through the 4 states.

MASTER State Machine

STATE 1: High side IGBT is ON

→ STATE 2 @ [(IcompL && MinOnDelay) or MaxOnDelay]

STATE 2: Resonant time (IGBTs OFF)

→ STATE 3 @ [(Q2IpolarityFeedback && MinDeadtime) or MaxDeadtime]

STATE 3: Low side IGBT is ON

→ STATE 4 @ [(IcompH && MinOnDelay) or MaxOnDelay]

STATE 4: Resonant time (IGBTs OFF)

→ STATE 1 @ [(Q2IpolarityFeedback && MinDeadtime) or MaxDeadtime]

SLAVE State Machine

STATE 1: High side IGBT is ON

→ STATE 2 @ [((InterleavePulse or IcompL) && IcompMin) or MaxOnDelay]

STATE 2: Resonant time (IGBTs OFF)

→ STATE 3 @ [(Q2IpolarityFeedback && MinDeadtime) or MaxDeadtime]

STATE 3: Low side IGBT is ON

→ STATE 4 @ [((InterleavePulse or IcompH) && IcompMin) or MaxOnDelay]

STATE 4: Resonant time (IGBTs OFF)

→ STATE 1 @ [(Q2IpolarityFeedback && MinDeadtime) or MaxDeadtime]

Protection timers

In the CPLD there are implemented timing functions which count the amount of time that has passed after a critical event. With the use of the independent timers, the driving logic can determine when the following timing events have occurred: Minimum On-Time, Maximum On - Time, Minimum Dead-Time, and Maximum Dead-Time. These time counters are not strictly necessary to implement the control strategy, yet they serve to increase the reliability of the system, in that they won't allow the converter to operate drastically beyond the nominal behavior.

Snubber Capacitor Fault

Another function which can be implemented in the CPLD is a function to look at the rise time for the switch node during resonant times. If this time is too short, it indicates that there is a problem with the resonant operation of the converter, which indicates a fault condition, most likely due to a reduction or loss of snubber capacitance. When this is detected, the CPLD will inform the DSP, which decides how to handle the fault. It is possible that the resonant timing is different during certain startup conditions, which is why the DSP might ignore the fault under these conditions.

Slave Driving Logic

The slave driving logic is similar to the master driving logic, except the switching events can be triggered by either the current comparators or the interleaving pulses which come from the DSP (which was calculated from the signal communicated by the master DSP). The slave DSP will generate peak current commands slightly higher than the current command used by the master DSP, so as to allow the slave DC-DC converter to effectively "drop back" into an interleaved position, by operating at a slightly lower frequency until the interleaving synchronization pulses become the primary signal to trigger the IGBT to turn off.

Current polarity feedback

Figure 27 shows the current polarity feedback (CPF) and IGBT gate signals. It can be seen that the gate signals go high after the CPF signals have come high which means the respective diode is conducting and it is safe for the respective IGBT to turn on under zero-voltage switching (ZVS).
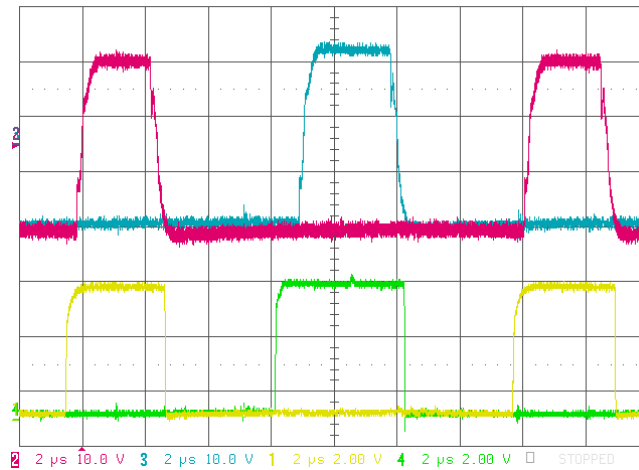
Figure 27 Gate high (#2), Gate low (#3), CPF-high (#1), CPF-low (#4)

In Figure 28 the CPF and gate signals are shown, but with the inductor current and switch node voltage. The CPF-high signal stays high while the switch node voltage is equal to the DC

bus voltage when the high-side diode or IGBT is conducting. The same is true for the CPF-low signal, when the switch node voltage is zero and the low-side- diode or IGBT is carrying the current. Only during the transitions of the switch node voltage (resonant mode) the CPF signals are not active. These signals are processed in the CPLD state machine, as a manner of protection and assurance that the IGBT is always turned on under a soft-switching condition.
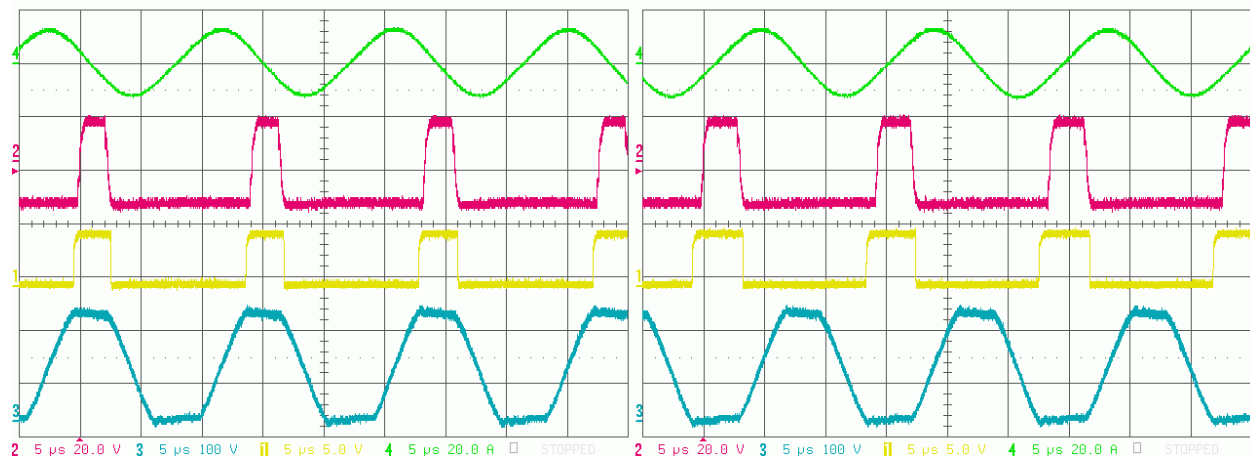
Figure 28 Inductor current (#4), Switch node voltage (#3); Gate high (#2 Left), CPF-high (#1 Left); Gate low (#2 Right), CPF-low (#1 Right)

Interleaving

Interleaving occurs when the inductor current through each DC-DC converter is shifted in phase, so as to balance the current ripple experienced by the filtering bus capacitors. Interleaving increases the effective switching frequency the bus capacitors must filter by the number of DC-DC converter modules, and also reduces the amplitude of the ripple current, as converter modules will tend to cancel out each other's current. For an 8 module system, each successive converter should be delayed in time by 45 degrees, with the ideal physical arrangement of converters in a way to place converters which are 180 degrees out of phase near each other. Two DC-DC converter modules 180 degrees out of phase are shown in Figure 29.

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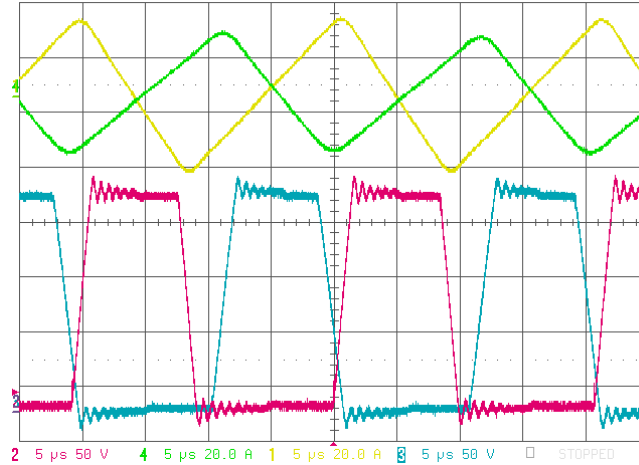
Figure 29 Interleaving of two converters (steady state); Master: Inductor current (#1), Switch node (#2); Slave: Inductor current (#4), Switch node (#3)

Since the system parameters, such as inductance and snubber capacitance, can vary significantly between each DC-DC converter module, the interleaving scheme must be tolerant of the potentially large difference between each module. An example of a large difference between the modules is also apparent in Figure 29. To achieve interleaving, the converters are in a master/slave configuration, where the master converter is free-running, and the other modules receive a synchronizing pulse, which they try to follow when possible. The synchronizing pulse generated by the master transitions low with the turn-off of its low-side IGBT and comes back high with the turn-off of its high-side IGBT. Doing that, the slave stage can capture the current switching frequency as well as the turn-off point of both IGBTs of the master stage. Because it is a variable switching frequency system, for every switching cycle the DSP controller has to calculate two interleaving pulses for its turn-off of both the low-side- and high-side IGBT when it is interleaved in steady state, as shown in Figure 30.

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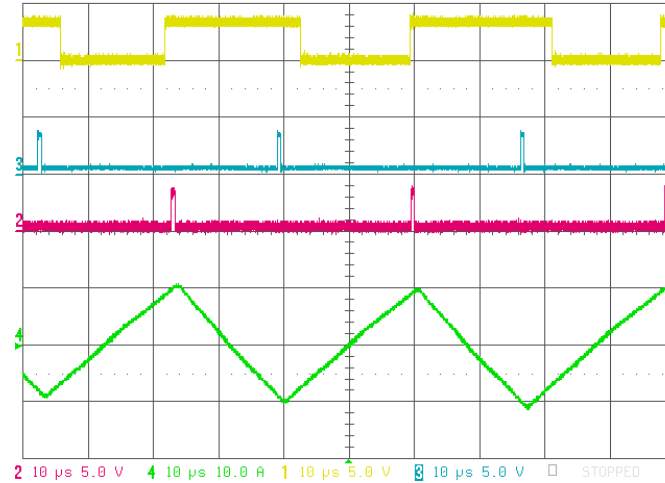
Figure 30 Signals for interleaving: synchronizing pulse (#1), negative and positive interleaving pulses (#3, #2), slave inductor current (#4)

If the generated interleaving pulses are too far shifted for normal operation, the logic operates the converter as a master stage until interleaving is acquired again. To aid in achieving interleaved operation, the master module also communicates the controller setpoints to the slave module controllers. The slave controllers use the master controller's current command to set the slave current command slightly higher than the master. The result is a slave module that accidentally falls out of interleaved operation will naturally push more power, reducing the operating frequency until the slave module falls back into the proper interleaved position, usually within a few switching cycles. The only drawback of this interleaving method is that the peak currents of the power stages have different levels depending on the tolerance of the inductors, but this cannot be avoided. The power stage with the highest inductance will have the lowest peak currents and therefore also lower thermal stresses on the IGBTs and diodes due to less RMS current. Startup of a slave module at various positions in the operation of the master DC-DC converter module is shown in Figure 31. Depending on the initial point where the slave module

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activates, the slave module will operate with higher peak current levels, until the module falls

back into the interleaved position.
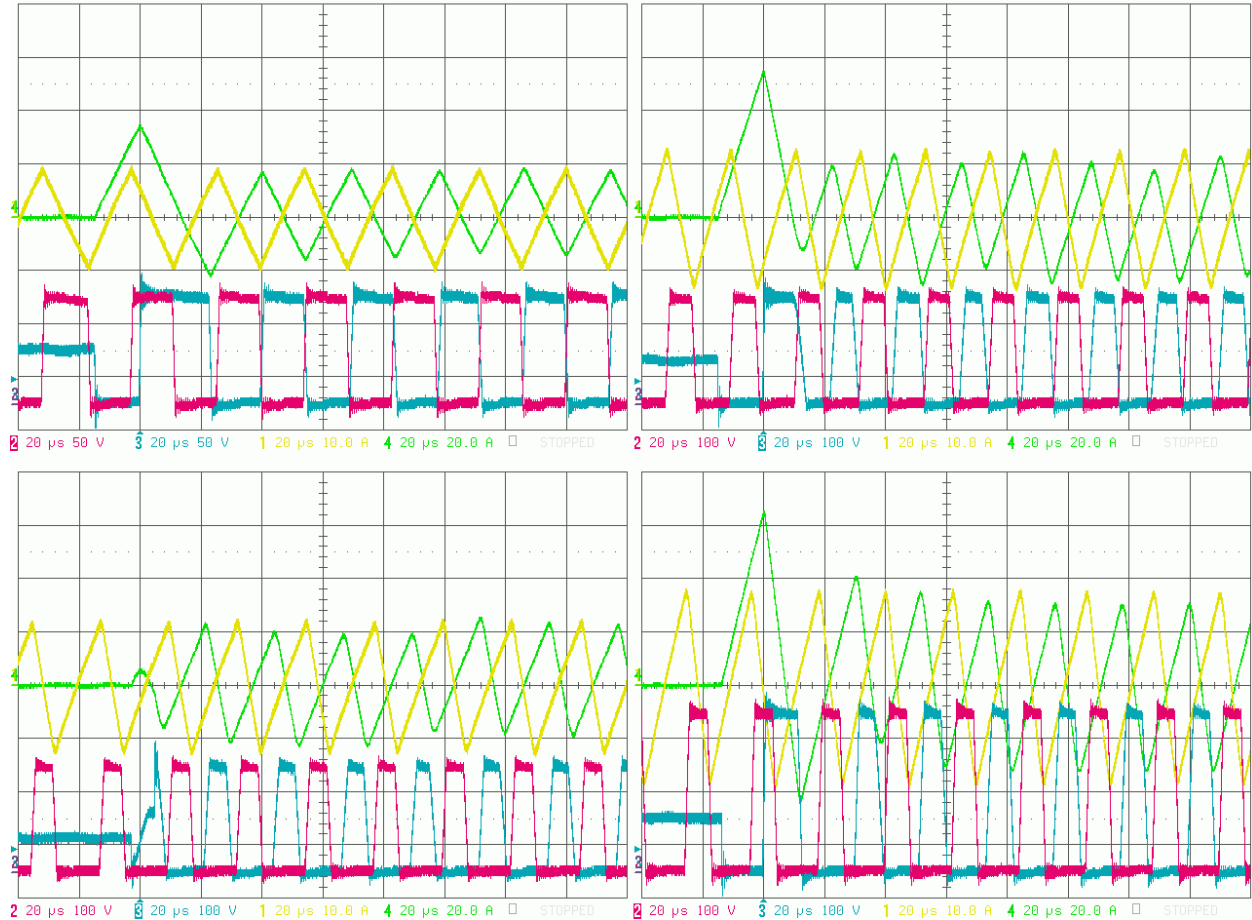
Figure 31 Start of interleaving: Master: Inductor current (#1), Switch node (#2); Slave: Inductor

current (#4), Switch node (#3)

Digital Controller Design

The digital controller is the key to the stable and optimal operation of both the DC-DC

converter and the entire HEV system. The digital controller is implemented in the DSP of the

converter, which controls the cycle-by-cycle control operations performed by the CPLD. There

are many potential system configurations, and subsequently, there are numerous potential

operating conditions. The goal was to develop a universal digital controller structure, which can

accommodate all of the conceivable EV and HEV system structures. The following figures illustrate the potential operating conditions, which were discussed in Chapter 1.
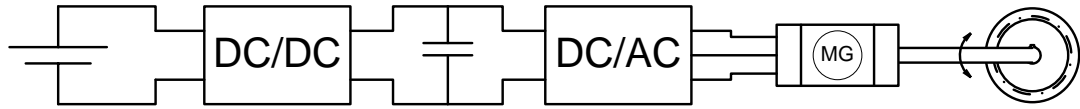
Figure 32 Electric Vehicle Architecture with DC-DC Converter
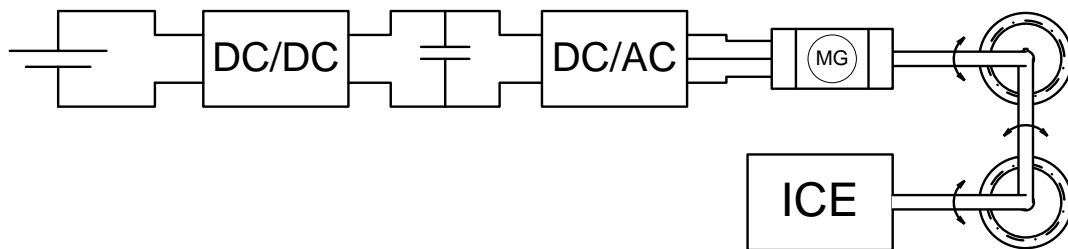
Figure 33 Parallel HEV Architecture
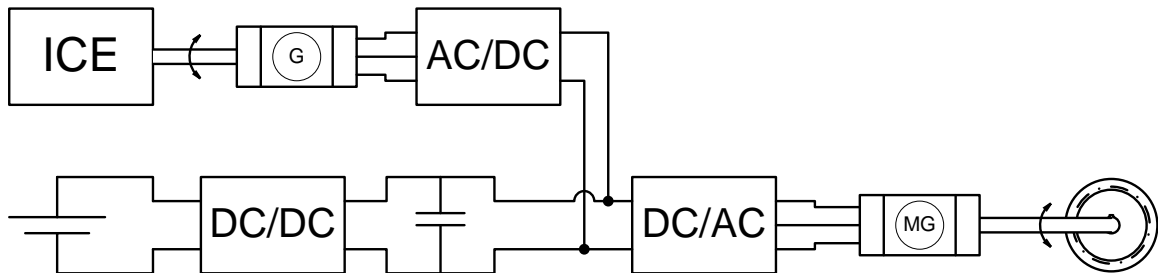
Figure 34 Series HEV 1 Architecture
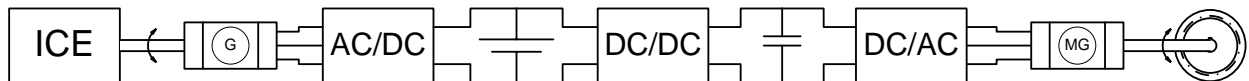
Figure 35 Series HEV 2 Architecture

Figure 36 Series-Parallel HEV 1 Architecture
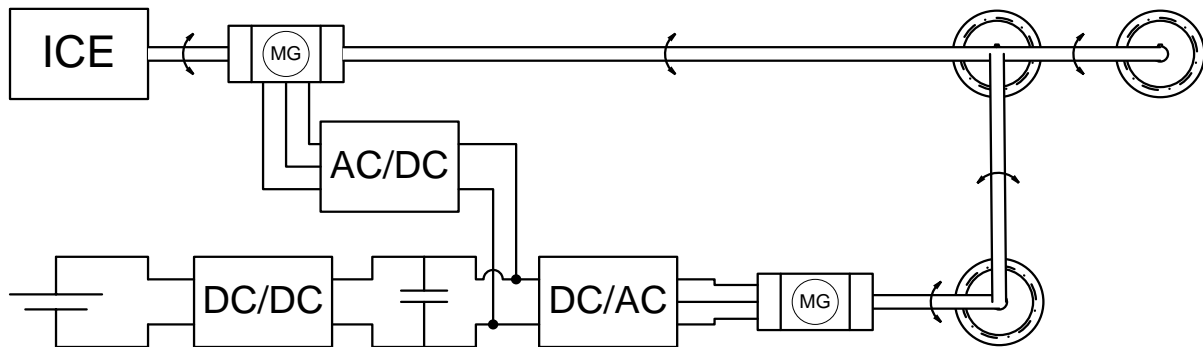
Figure 37 Series-Parallel HEV 2 Architecture

To allow the converter system to be very versatile and allow seamless integration with many system architectures, it is critical that the digital controller structure be robust enough to accommodate many operational conditions, while also minimizing the necessary customization depending on the application. To this goal, a digital controller structure was developed, as shown in Figure 38, which can seamlessly transition between numerous operating conditions and scenarios. The controller is a cascaded structure of multiple key subsystem controllers, including battery current regulation (BCR), output voltage regulation (OVR), and input voltage regulation (IVR).
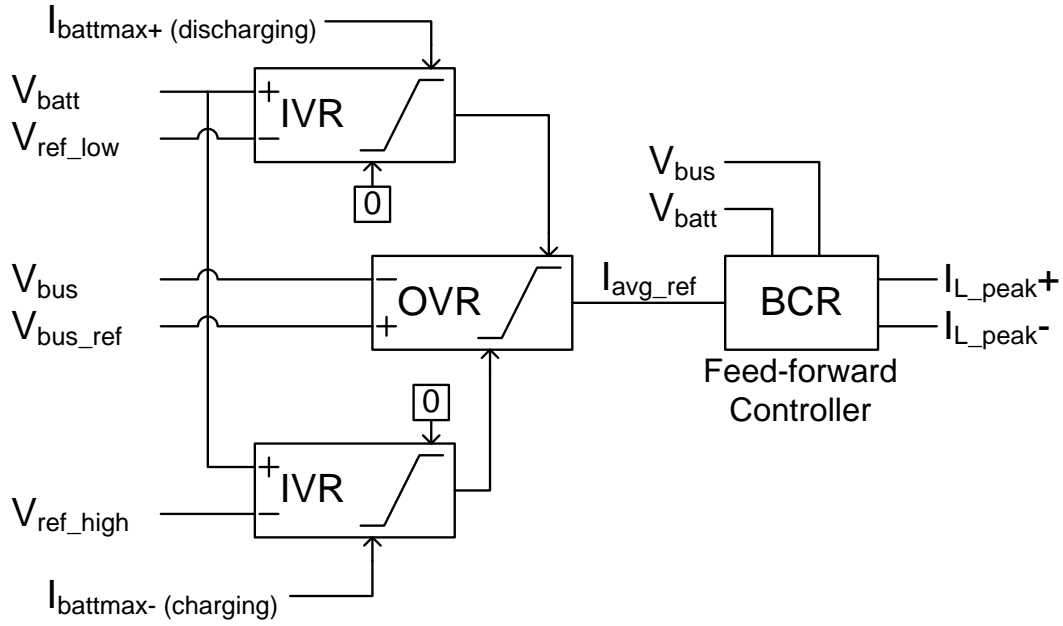
Figure 38 Bi-directional digital controller structure

Battery Current Regulation

The BCR loop is a feed-forward controller, meaning that it is essentially open-loop. Based on the static system parameters and dynamic operating conditions, including input and output voltage, inductance, and snubber capacitance, it is possible to generate a multidimensional equation or look-up table, where the necessary peak currents can be determined from a desired average current. The accuracy of the BCR will depend on the precision and accuracy of the multidimensional equation, the accuracy of system parameter measurement, and the change in inductance and snubber capacitance over time and temperature. Even though the BCR loop is not closed, this will only have an effect on the regulation accuracy of output current, which is typically not a system critical value, unlike voltage. Typically, a current regulation mode would be where the converter is operating at a maximum system current for protection, such as the maximum charge or discharge current of the battery. This protection value is not critical, i.e. a battery will not be fine when charging with 100 A, but be damaged when charging with 103 A.

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Furthermore, the BCR controller can be calibrated in-system, decreasing the error significantly, potentially less than 3% error.

Output Voltage Regulation

The output voltage regulation (OVR) controller is a digitally implemented PID controller. One key aspect of the digital OVR controller is that the controller output must be continuously limited, to prevent transient conditions of the controller from commanding higher peak-currents than the system is designed for. Furthermore, as can be seen from the system controller structure in Figure 38, the output limits of the OVR controller are active control points for the input voltage regulation (IVR) controller loops, which necessitates that the manner in which the OVR loop is output limited is important to the overall system performance. In the classically known PID controller, as shown in Figure 39, the outputs from the proportional, integral, and derivative controllers are summed to achieve the control output. If the output of the controller must be limited to specific values, as is the case for the OVR loop, there is a final output limiting function. This limiting function will of course serve the purpose of limiting the output value, but it will not limit the output of the integral controller, which could be further increasing outside of the limited bounds of the controller. Once the error signal reverses, to correct the overshoot, if the integrator was well saturated higher than the commanded control signal, significant instability can occur. This is a problem exhibited in many controllers, yet in most cases, the controller is not expected to routinely operate in a saturated manner as a desired function, so the effect is not often experienced.
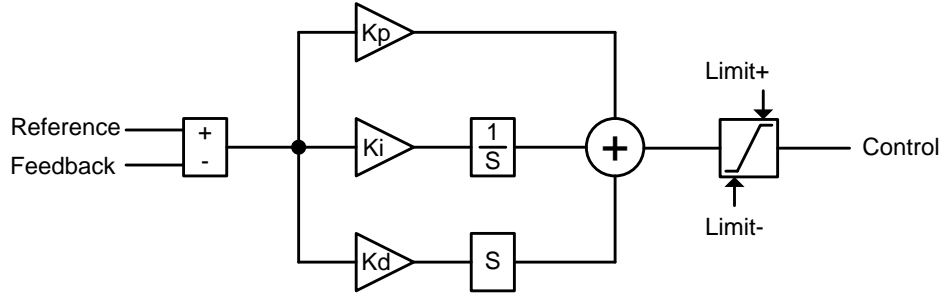
Figure 39 Traditional PID structure with discontinuous output limiting

There are many ways to prevent the integrator from saturating, as are presented in [28 - 31], but these solutions often are intended to be used with a static saturation value, and are not optimal when the converter is actively modulating the saturation limits as a method of control. To combat the controller saturation issues, a modified PID controller structure was derived, which implements an integrator as the final block before the control output. This single integrator block can then be easily limited to the desired upper and lower limit values. In this case, if the controller is saturated, the output integrator will saturate to the upper or lower limit, thus allowing the controller to instantly recover when the error signal reverses, or the upper limit is changed. To achieve this, a derivative term is distributed to each of the P, I, and D controllers, thus cancelling the dynamic effect of the final integrator. This new PID structure is shown in Figure 40.
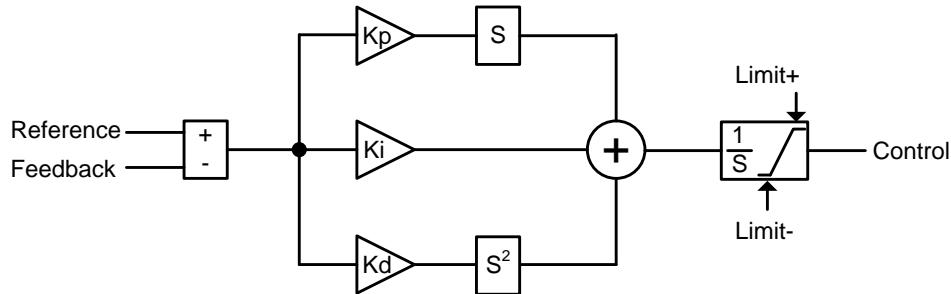
Figure 40 Modified PID structure with continuous output limiting

A PI controller features a pole at the origin, and a zero of which the placement is determined by ki/kp. Often in power electronics converters, a Type II controller is implemented, which is similar to the PI, except it has an additional pole placed at a frequency roughly 1/4 of the switching frequency, which is intended to limit the controller reaction to high frequency disturbance, primarily from the output voltage ripple. When implementing the OVR loop, the output from the digital controller feeds the feed-forward BCR loop, which generates analog peak-current comparison levels. The output of the digital-to-analog converter which generates the peak-current references is ultimately filtered with an analog RC circuit, in order to filter noise on the signal. This RC filter represents a final controller pole, which proves the digitally implemented PI controller to be equivalent to the Type II controller. The PID controller consists of a pole at the origin and two zeros, and with prudent addition of analog filter circuitry, the digital PID controller can be compared to the Type III controller, which has an additional two pole pair at higher frequency. The factorization of the PI and PID controllers and the zero locations are shown in the following equations. To transition between a Type II or III controller and the PID controller, the zero frequencies are expressed in terms of the PID gains. The pole locations (beside the common pole at DC) of the Type II and Type III controllers are implemented by analog filtering in the peak-current reference generated by the digital-to-analog converter.

$$G_{PI}(s) = k_p + \frac{k_i}{s} = \frac{k_p\left(s + \frac{k_i}{k_p}\right)}{s}$$

(15)

$$f_{zero} = \frac{1}{2\pi} \cdot \frac{k_i}{k_p}$$

(16)

$$G_{PID}(s) = k_p + \frac{k_i}{s} + k_d \cdot s = \frac{k_d s^2 + k_p s + k_i}{s}$$

(17)

$$G_{PID}(s) = \frac{k_d\left[s + \left(\dfrac{k_p - \sqrt{k_p^2 - 4k_d \cdot k_i}}{2k_d} \right) \right] \cdot \left[s + \left(\dfrac{k_p + \sqrt{k_p^2 - 4k_d \cdot k_i}}{2k_d} \right) \right]}{s}$$ (18)

$$f_{zero1} = \frac{1}{2\pi} \cdot \frac{k_p - \sqrt{k_p^2 - 4k_d \cdot k_i}}{2k_d}$$ (19)

$$f_{zero2} = \frac{1}{2\pi} \cdot \frac{k_p + \sqrt{k_p^2 - 4k_d \cdot k_i}}{2k_d}$$ (20)

The digital implementation of the PID with continuous output limiting is shown in Figure 41. The first and second derivatives are calculated to feed the proportional and differential controllers. The final output integrator is implemented in a 1st order integrator, which simply delays the output, and adds the output from the controllers to the last integrator value. This integrator is the most basic, and therefore, has the highest degree of loss. If desired, the integrator order can be increased, to increase the fidelity of the controller, although, experimental testing has found the 1st order integrator to be reasonably adequate.
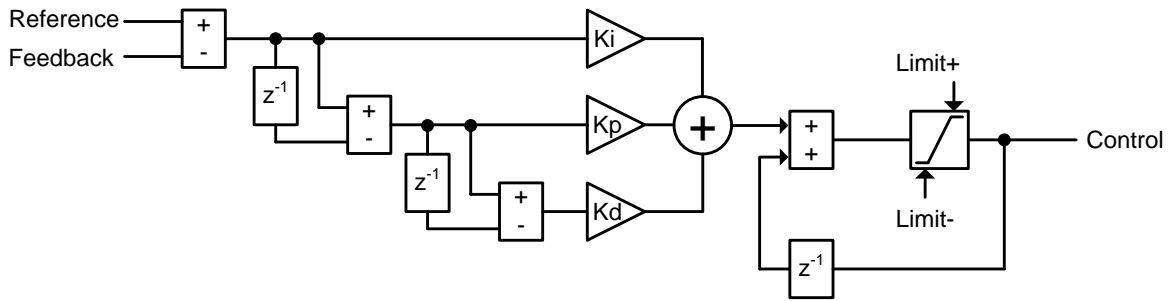
Figure 41 Digital PID implementation with continuous output limiting

Input Voltage Regulation

During the normal course of operation, the voltage of the drive battery will not be expressly controlled by the DC-DC converter, since the controller can only control one system parameter at a time, either output voltage, input voltage, and input current. Usually output voltage and input current are primary control parameters, but the battery voltage must remain within the safe operational region. A case where is important is when the battery is already mostly discharged and the vehicle is asked to accelerate. With the increased load current, the battery voltage will naturally drop, possibly below the specified minimum safe voltage. In this case the battery voltage will be below V_{ref_low}, causing the IVR controller to reduce the discharging current to a level which maintains that minimum battery voltage. A similar case is when regenerative braking is engaged with a full battery, to prevent overcharge and potential damage to the battery, the other IVR controller will limit the battery charging current, to not allow the voltage to exceed a safe limit. The IVR controllers are implemented as digital PID controllers, similarly to the OVR controller.

Controller Verification

In voltage regulation mode, the digital controller is responsible for controlling the peak currents of the inductor so as to keep the high voltage bus at the reference set point. When there are load transients, the converter will have overshoot or undershoot, of which the controller must quickly change the peak-current commands to bring the voltage back to the reference point. The most dangerous condition is when the converter is operating at full power, and the load is removed, which will cause the output voltage to quickly rise. In order to prevent the over-voltage fault, the controller must be fast enough to keep the bus voltage in a normal range. A simulation was made of the digital controller which is being implemented in the DSP as well as

the converter. To test different controller responses, the simulation switches between light load and heavy load so as to see the potential overshoot and undershoot of the designed controller. The simulation in Figure 42 showed that the expected controller values operate well, with the peak overshoot around 50V when the converter is transitioned from full load to no load. This should be acceptable, especially considering that the load should not change nearly as quickly, since the bus load will be loaded by the motor controller, which will not be able to change modes very quickly.

During testing, the controller parameters are set as variables which are passed from the interface, which is very useful for testing the controller. This is also useful for when the converter is powering the motor controller, which most likely will have high input capacitance. In this case the dynamic behavior of the system will change, and it will be necessary to change the controller characteristics in order to keep the system stable. The interface will have the controller parameters as an available option, so the system will be very versatile, as the controller can easily be tuned for different configurations.

400V
200V
0V
□ V(ZCONTROL)
100V
0V
-100V
□ V(ERROR)
400A
0A
-400A
□ I(L)
800V
700V
SEL>>
600V
0s   1ms   2ms   3ms   4ms   5ms   6ms   7ms   8ms   9ms   10ms   11ms   12ms
□ V(HIGH)
Time
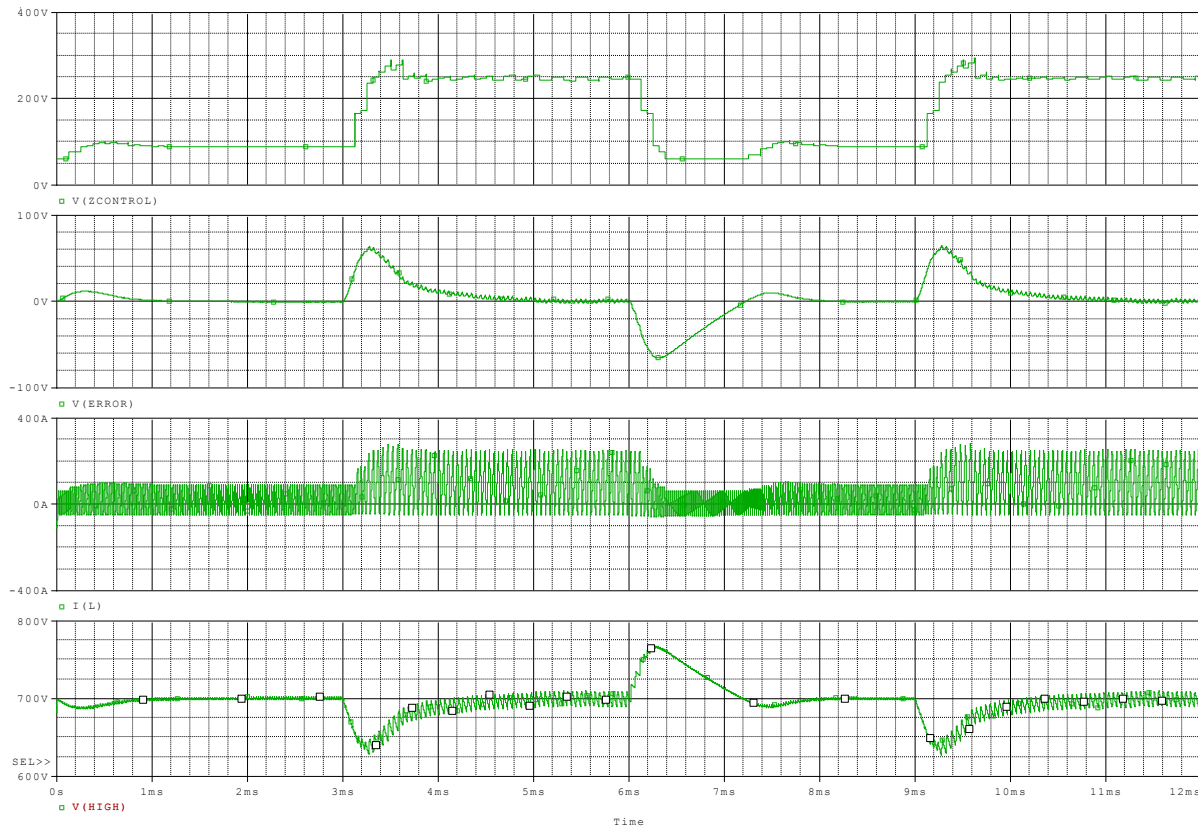
Figure 42 Simulation of the digital controller under transient conditions (current control signal,

controller error signal, inductor current, output voltage)

Another feature of the controller is safety, which means that the converter should be able
to operate safely under all conditions, even when unexpected conditions occur. One such
condition is a surge of output power, such as if the motor controller was to malfunction. Since
the controller directly controls the peak currents of the inductor, the system is safe from damage
even if the bus is suddenly shorted. The peak current will not exceed the pre-determined
maximum value, so the voltage will naturally drop under the heavy load, until the system detects
the under voltage fault condition, and shuts down the converter. A simulation of this condition is
simulated in Figure 43. If there was a short on the bus, the converter would shut off, but if the
battery is connected, it will push current through the body diodes of the upper IGBT, and could

possibly damage the unit. It is necessary that the batteries have a mechanical cutoff such as a contactor or fuse to prevent such situations.
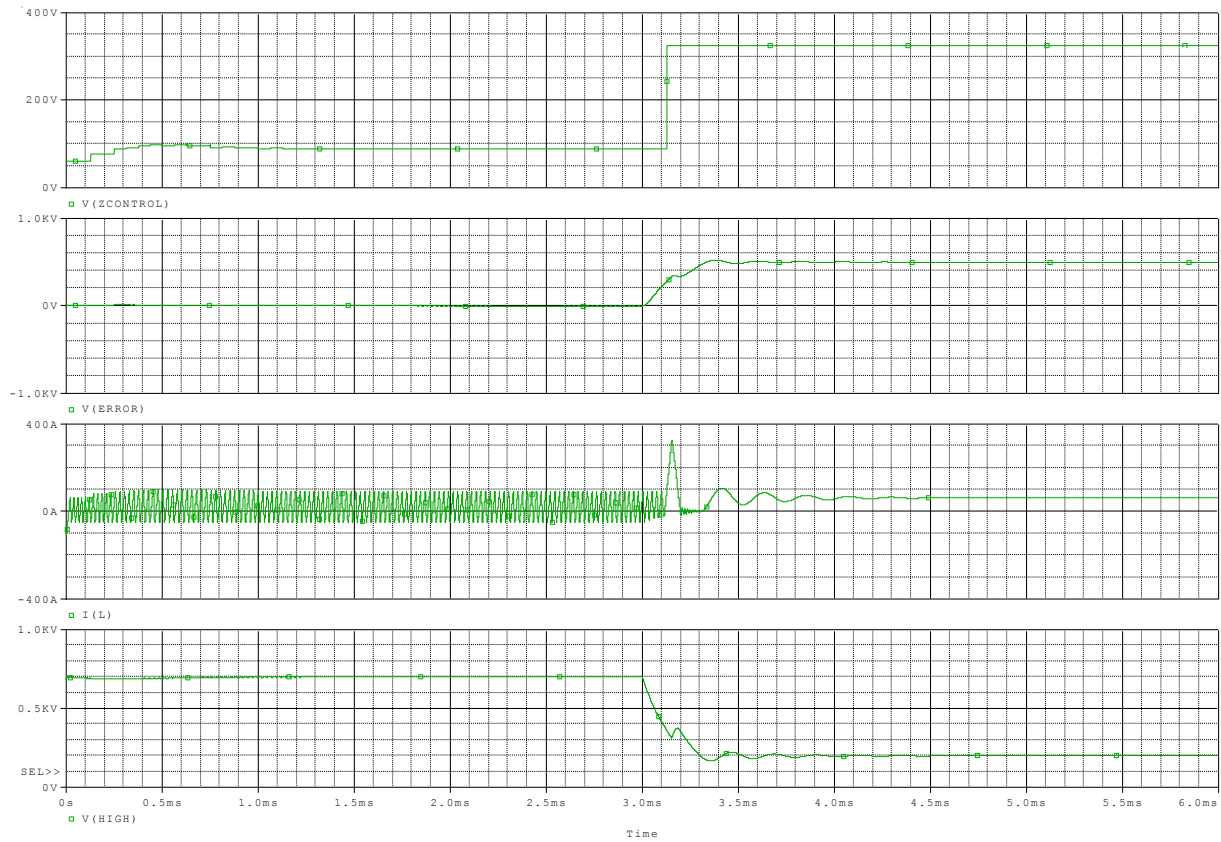
Figure 43 Simulation of the converter with a short circuit condition (current control signal, controller error signal, inductor current, output voltage)

Output Capacitor Emulation for Fuel Cell

The proposed converter system has many unique and advanced characteristics, including high density, high efficiency at low power, and fast transient response due to the boundary mode operation. These characteristics can allow the converter to serve other useful functions for electric vehicles. One such function is the ability for the converter to increase the density of fuel-cell vehicle drive systems, by increasing the utilization factor of the ultracapacitors used to buffer the energy drawn from the fuel cell. Increasing the utilization factor of the ultracapacitors effectively increases the density of the capacitors, reducing the necessary ultracapacitor size for

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the same performance. Examples of the use of a ultracapacitor to buffer the load transients to the fuel cell are shown in [32] and [33].

The fuel cell power source is traditionally considered a slow transient device, in comparison to a traction battery. Where a battery can quickly supply transient current, the fuel cell is not well suited for transient behavior. In a fuel cell powered electric vehicle, the system must be able to respond quickly to power demands, which is why ultracapacitors are commonly used in conjunction with fuel cell systems, since the ultracapacitor can deliver transient energy, while allowing the fuel cell to power the system in a steady manner. A major drawback of ultracapacitors in comparison to electrochemical batteries is that the energy stored in a capacitor is distributed over the entire operating voltage of the capacitor, whereas a battery has a specific voltage range which corresponds to the charge level. Since the fuel cell must operate within a small voltage range, the usefulness of an ultracapacitor in parallel is severely limited. The proposed concept is to use the DC-DC converter to interface between the fuel cell output and an ultracapacitor. In this way, the ultracapacitor voltage is decoupled from the fuel cell voltage. The ultracapacitor will be able to swing between the maximum rated voltage and a very low voltage, yielding a utilization factor of nearly 100%. The structure of the proposed concept is shown in Figure 44.
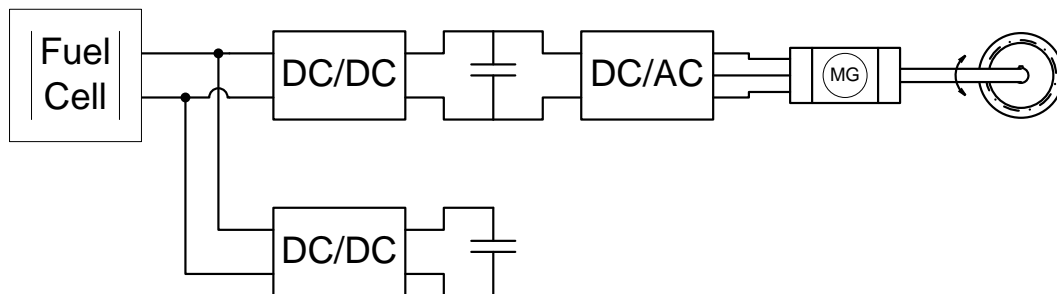
Figure 44 Fuel-cell output capacitor emulation system structure

To achieve this goal, a controller structure has been developed, which is able to simulate a much larger capacitance value at the output of the fuel cell, with the knowledge that the simulated capacitor will not be effective if the transient operation causes the fuel cell voltage to swing beyond the designed limits. For example, since the actual ultracapacitor has a specific energy available for storage, if the transient energy exceeds the energy capacity of the ultracapacitor, it will no longer be able to assist the fuel cell in transient response.

The developed controller structure operates by sensing and calculating the derivative of the fuel cell voltage, and calculating what the corresponding current from the simulated capacitor would be based on the virtual capacitance. The controller implements OVR control loops to limit the ultracapacitor from being overcharged when absorbing energy, or discharging below the desired voltage when delivering energy. There is another slower OVR loop which works to keep the ultracapacitor charged in a steady state to some point, usually representing the capacitor being charged with half of the total allowable energy, so that the system is ready to absorb or deliver an equal amount of transient energy. The devised controller structure is shown in Figure 45.
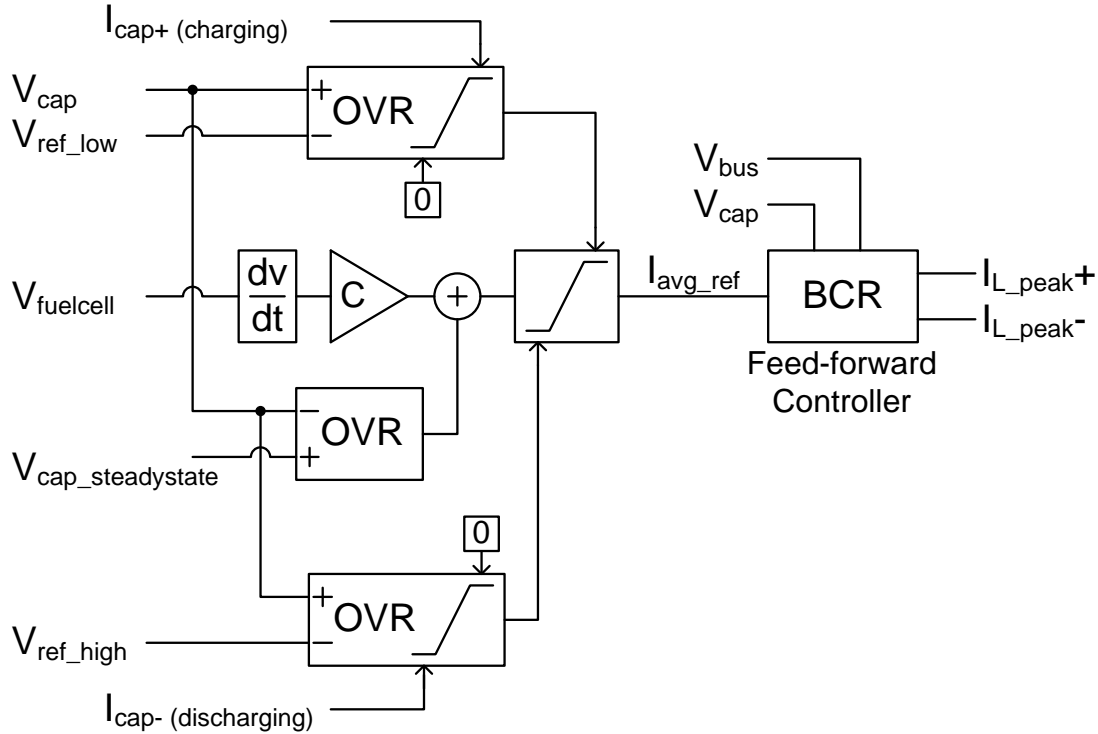
Figure 45 Fuel-cell bus capacitor emulation digital controller structure

To design the bus capacitor emulation system, there are certain parameters which must be set to specify the behavior of the system. The critical parameters are the allowable voltage swing on the ultracapacitor, the allowable voltage swing on the fuel cell, the capacitance of the ultracapacitor, and the desired virtual capacitance. With these critical parameters, the desired system can be designed, with the action of leaving one parameter as an independent variable during the design process. For example, if the expected transient energy is known, as well as the allowable ultracapacitor voltage swing, and the allowable voltage swing on the fuel cell, the desired virtual capacitance can be calculated. The applicable design and system equations are shown below, with the consideration that the ultracapacitor will be naturally charged to a voltage representing 50% of the available storage energy, making the system equally prepared to charge or discharge the fuel cell bus. The system could also be designed to anticipate high regenerative transients, such as during regenerative braking, since the fuel cell cannot absorb energy.

$$\Delta V_{FuelCell} = Alowable \ voltage \ swing \tag{21}$$

$$V_{FC\_SS} = Steady \ state \ fuel \ cell \ voltage \tag{22}$$

$$\Delta E_{UltraCap} = \tfrac{1}{2} C_{UltraCap}(V_{refHigh}{}^2 - V_{refLow}{}^2) \tag{23}$$

$$\Delta E_{FuelCell} = \tfrac{1}{2} C_{Virtual}\left[(V_{FC\_SS} + \Delta V_{FuelCell}(1-\tfrac{1}{\sqrt{2}}))^2 - (V_{FC\_SS} - \Delta V_{FuelCell}\tfrac{1}{\sqrt{2}})^2\right] \tag{24}$$

$$\Delta E_{UltraCap} = \Delta E_{FuelCell} \tag{25}$$

$$C_{Virtual} = \frac{C_{UltraCap}(V_{refHigh}{}^2 - V_{refLow}{}^2)}{2V_{FC\_SS} \cdot \Delta V_{FuelCell} + \Delta V_{FuelCell}{}^2(1-\tfrac{1}{\sqrt{2}})} \tag{26}$$

CHAPTER 3: HIGH DENSITY INDUCTOR DESIGN

A significant characteristic of the proposed DC-DC converter is the very high current ripple in the inductor. The traditional CCM DC-DC converter utilizes an inductor with relatively large inductance, which will conduct a DC current with a small AC current ripple. The converter presented in this dissertation requires an inductor which can operate with an AC current ripple much exceeding the average DC current. The benefit of this design is the ability to use an inductor with much lower inductance compared to the traditional CCM converter, but this is only beneficial if an inductor can be designed to perform well with such high current ripple. Since the current ripple experienced by the inductor greatly exceeds the average current through the inductor, it is critical that the inductor has very low AC core losses in addition to low copper loss.

In the course of this work, two converter prototypes were developed, which had differing inductor needs. The evaporative spray cooling converter required lower inductance, higher peak current, and higher frequency operation. The cold-plate cooled converter required higher inductance, lower peak current, and lower frequency operation. To satisfy the needs of the converters, tape-wound nanocrystalline inductors were designed, which features 18 μm thick magnetic material, which is wound around a former to make the shape, and epoxy fused. The designed core exhibits low magnetostriction due to the core material (Hitachi FT-3M FINEMET), which corresponds to low AC losses. Furthermore, since an air gap is required in the core to achieve the proper inductance, the very thin core material significantly reduces the gap losses from eddy-currents in the material. To further reduce losses, the gap in the core is distributed between multiple gaps, which reduces the flux fringing at the gaps, reducing gap losses. Due to the high current ripple, copper loss is reduced by using copper foil conductors. The inductor was designed with cooperation of theoretical analysis and finite element analysis (FEA), so as to

completely optimize the efficiency and density. A methodology for high power nanocrystalline inductor design was presented by [34]. To cool the inductors, they are pressed between two liquid cooled coldplates and potted with a thermally conductive epoxy. The copper foil leads of the inductors are routed to the appropriate busbar connections on the DC-DC converters.

Table 3 Nanocrystalline Inductor Specifications

Inductor Rev #	1	2
Material	FT-3M	FT-3M
Inductance	20 uH	32 uH
Core Effective Area	12.3 cm^2	12.3 cm^2
Magnetic Length	18.5 cm	16.1 cm
Saturation Flux	1.2 T	1.2 T
Number of Winding Turns	6	7
Saturation Current	431 A	331 A
Conductor Width	5.08 cm	3.55 cm
Conductor Thickness	0.813 mm	0.813 mm
Core Mass	1.75 kg	1.54 kg
Number of Gaps	6	4
Gap Thickness	0.5 mm	0.63 mm
Maximum Temperature	200ºC	200ºC

Core Material Selection

It is clear that the inductor core material should have certain characteristics to achieve an optimal design. Due to the required high density, the inductor core material should have a high magnetic field saturation level and high permeability, which will reduce the number of conductor turns on the core necessary for a given inductance. The core material must also have exceptionally low AC loss, since the AC magnetic flux swing is very high in comparison to the DC field. Furthermore, the inductor will be subjected to high temperature, exceeding 180ºC. Through a survey of the numerous potential core materials, it is immediately apparent that most inductor core materials are not suitable for this application, either due to the inability to operate at high temperatures over 100ºC, or they saturate at a low flux density (less than 0.8 T). As can be

seen in Table 4, the nanocrystalline core material has characteristics which excel in each category.

Specifically, the nanocrystalline material has the lowest loss, high saturation field, high curie

temperature, and the thinnest material of all of the wound cores. From this comparison, it is very

clear that the nanocrystalline material is well suited for this application, with some provisions. A

comparison of core materials for similar high flux swing inductors is presented in [35]. The data

shown in Table 4 shows the physical properties of the core materials, but, additional

considerations must be made for the practical applications. One major consideration is the effect

of the air gaps on the performance of the core. If core geometry is not carefully designed, the

additional losses from fringing at the gaps can easily increase the AC losses of the inductor by a

factor of 2 to 3 times, which would be disastrous in this application, where AC losses grossly

dominate.

Table 4 Comparison of applicable core materials

Material	Thickness (μm)	B (T)	μ @ 100 kHz	P_{loss} @ 0.2T (kW/m$_2$)	T_{curie} (ºC)
Nanocrystalline 3M	18	1.23	16	300	570
Fe Amorphous	25	1.56	5	2200	415
Co Amorphous	20	0.60	10	460	210
Mn-Zn Ferrite	N/A	0.49	2.4	680	200
80% Ni Permalloy	25	0.74	5	1000	460

To properly design and optimize the inductor, it is critical to understand the various

components of the inductor loss. The inductor losses are distributed between conductor and core

losses, with each type of loss having further subcategories. Core loss occurs during each change

in magnetic field, where there is hysteresis on the B-H curve, meaning that there is residual

magnetism as the flux is reduced, and energy is lost in the process of returning the magnetism of

the material to zero. The core loss has many causes, reaching from energy loss on a molecular

level, to mechanical heat generation from the physical expansion and contraction of the material, known as magnetostriction. The copper loss has two main components, AC and DC losses. DC loss is simply the DC resistance multiplied by the DC component of the current squared. The AC losses are significantly more complicated due to the various effects of high-frequency current on the behavior of the conductors, due to skin loss, eddy currents, and the proximity effects. Furthermore, there is also an important loss to consider, known as gap loss and fringing loss. Fringing is the tendency for the magnetic field to stray from the core area magnetic path at the air gap. At larger air gaps, and with higher AC flux, the losses stemming from the gap flux fringing become more critical. The fringing field induces eddy currents in any electrically conductive material it contacts, which includes the copper conductors of the inductor, as well as the core material itself.

For illustrative purposes, the inductor design is simulated in Figure 46. As can be seen, the fringing flux induces projects from the gap, and induces heating in the copper conductors. Furthermore, the fringing flux tends to re-enter the core material from the other side of the gap at a right angle, thus inducing eddy currents in the wound planar material of the core. The eddy currents in the core material induce heating, which is known as gap loss. This problem is much more severe for such a laminated core in comparison with ferrite cores, which are constructed of a homogeneous ceramic material with relatively low conductivity. The thickness of the tape wound nanocrystalline material is important to reduce the effect of gap loss, as a thinner material will have higher resistance, and will exhibit lower eddy currents. Considering all of the causes for loss in the inductor, it is clear that the nanocrystalline core material is optimal for this application.
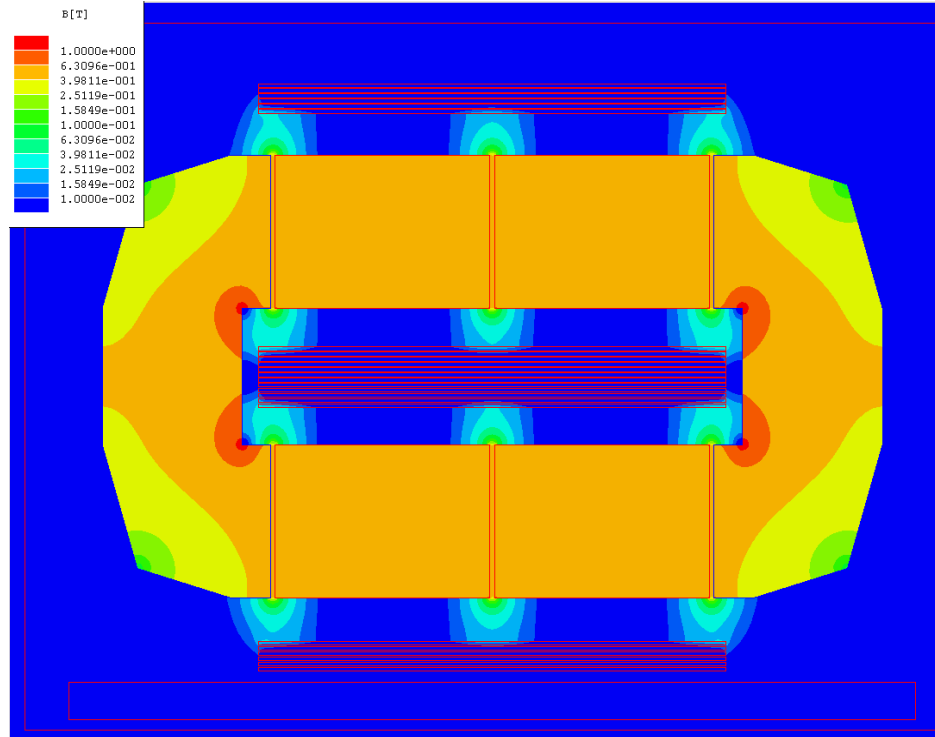
Figure 46 FEA Simulation of Inductor Flux and Gap Fringing

Current Ripple vs. Output Power

One important characteristic of the variable frequency boundary mode DC-DC converter is the relatively high AC ripple current experienced by the inductor, and the variable frequency operation, which operates the converter at higher frequency to correspond with lower output power. This soft-switching operation, while ideal for the efficiency of the IGBT, make the inductor design more difficult, and increases the necessary analysis for proper design. Since AC inductor losses are related to the switching frequency in addition to the amplitude of the AC current swing, the design of the inductor for the "worst case" is not necessarily straight forward. While the low power operation will significantly reduce the amplitude of the current ripple, the higher frequency operation will directly increase the inductor losses, potentially completely mitigating the loss benefits of lower ripple current. For this reason, it is important to properly model the operation of the inductors over the entire power range, which is related to the

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switching frequency. To reiterate upon the operating conditions of the inductor, the peak currents of the inductor for the 20uH inductor versus output power are shown in Figure 47. As can be seen, with zero output power, the converter operates with the lowest peak currents, which dictates higher switching frequency. A plot of switching frequency can be seen in Figure 48, where the full load frequency approaches 20 kHz, and the no-load switching frequency exceeds 55 kHz.
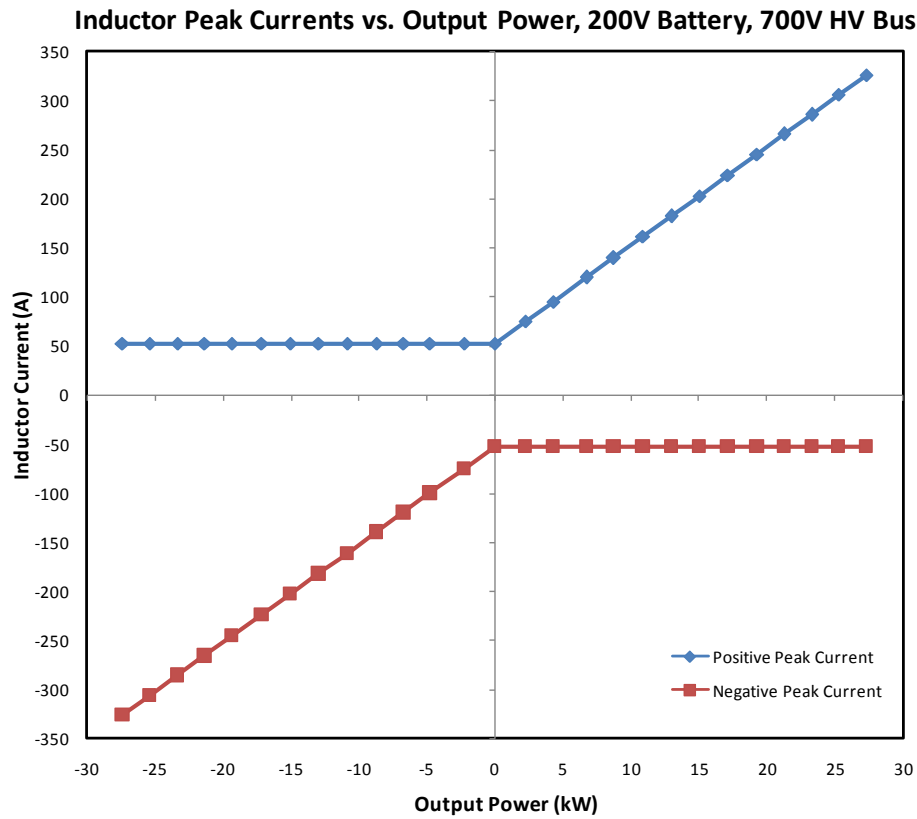
Figure 47 Inductor Peak Currents vs. Output Power
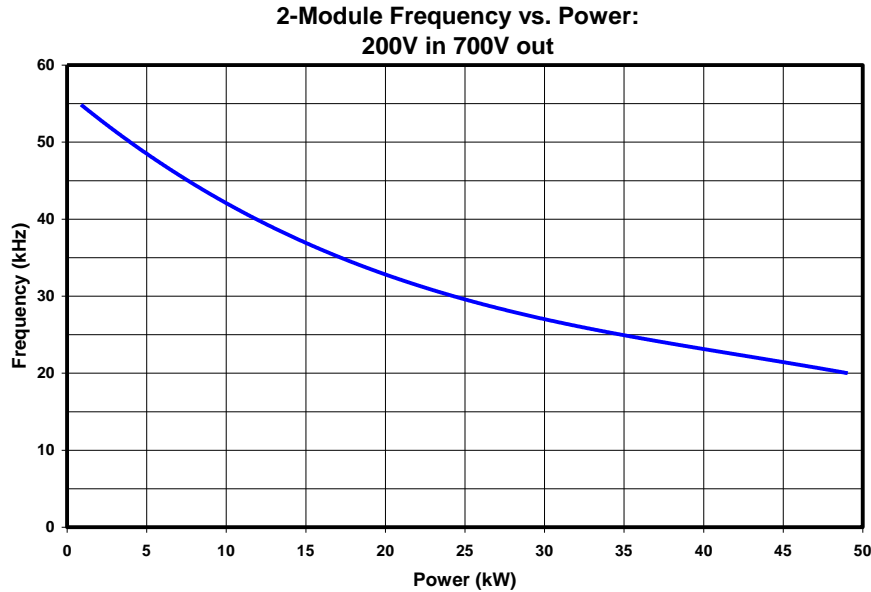
Figure 48 Switching frequency vs. output power, 2-module DC-DC

Since the losses of the inductor are dependent on the DC current, the AC current ripple, and the switching frequency, the "worst case" operating condition is not immediately clear, requiring the development and analysis of the losses across the entire operational range. An analytical model to determine the losses in magnetic components is presented in [36]. To achieve this, the inductor has been mathematically modeled and simulated, so as to assure that the design is optimal. As will be shown later in this chapter, the worst case operating condition did prove to be the full power condition, which is shown in Figure 49. Although the worst loss condition is at full power, it is still important to analyze the operation across the load range, so as to optimize overall efficiency. The calculated plot of inductor peak current and AC flux density swing is shown in Figure 50.
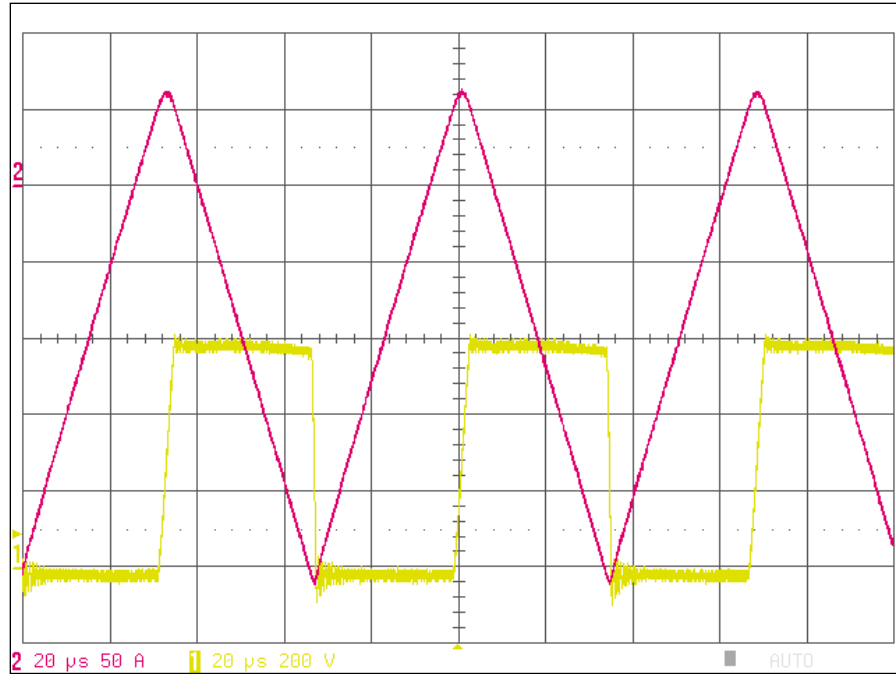
Figure 49: Inductor #2, 32 uH measurement, 600V to 300V, 28kW (#1 switch node voltage, #2 inductor current)
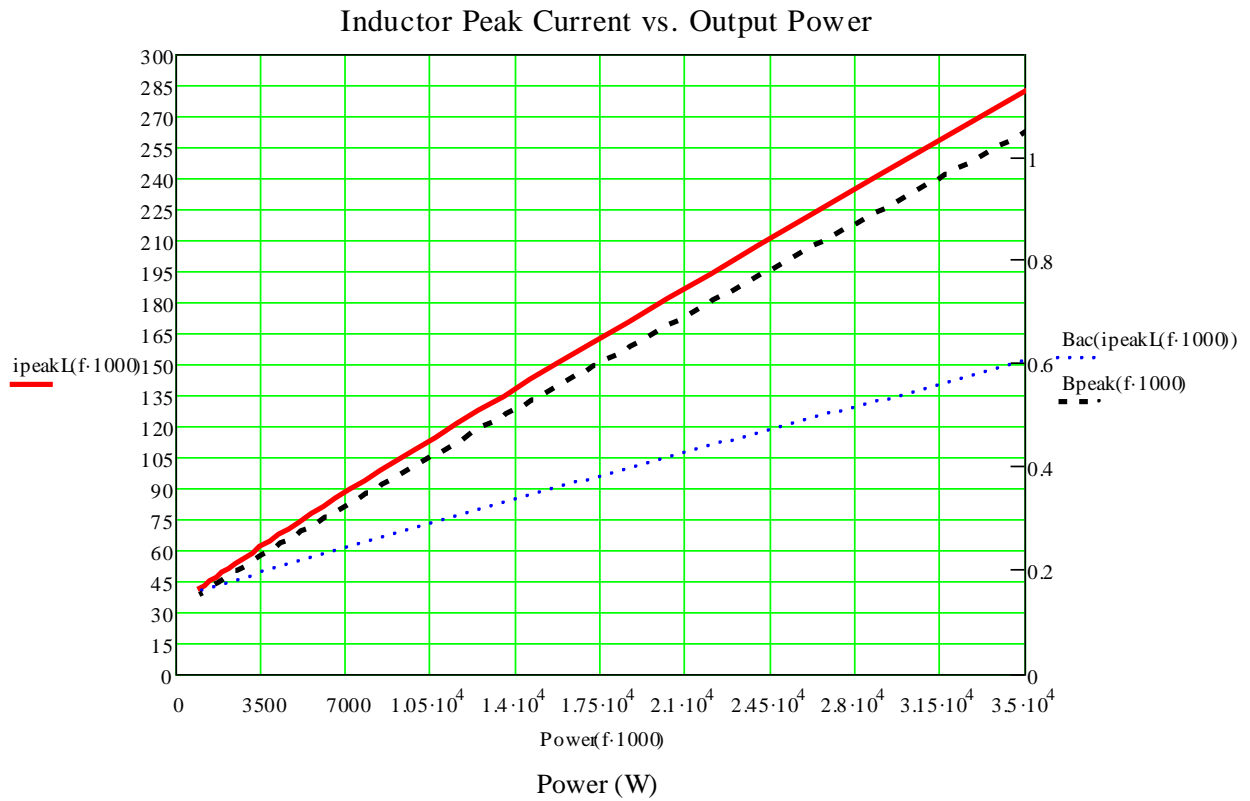
Figure 50 32uH inductor peak current and AC flux density vs. output power

Nanocrystalline Core Design

The inductor design process is iterative, where the core and winding geometry is first optimized through analytical means, and then once a seemingly optimal design is achieved through analysis, finite element analysis (FEA) simulations are performed to further refine the design. If one were designing an inductor which had a lower permeability, and no air gaps, the losses of the inductor would be more straightforward to determine through analytical methods. Due to the high level of complexity of the design, it is exceedingly difficult to model the losses associated with the fringing at the gaps, which is why the 2D FEA is important to finalize the design.

One important key characteristic of the design is the use of distributed gaps, which allow the inductance to be precisely achieved, in a way which has high temperature stability, and will not significantly increase the losses of the inductor. All magnetic materials will have a variation in permeability across a temperature range, which can significantly change the inductance of the design, unless the dominating reluctance comes from air gaps, which will not have a variation due to temperature. Furthermore, as described earlier, larger air gaps will lead to higher losses, due to the fringing and gap losses. To combat this, many smaller air gaps are desired. The overall analysis of the inductor design is performed with a mathematical software package, and a 2D FEA simulation tool.

Core Loss Calculation

The basis for core loss calculation is an equation specific to the core material, which has been determined by the manufacturer of the core material. This equation, shown as number 27, is empirical in nature as provided by the manufacturer. A characterization of the losses in nanocrystalline magnetics is presented in [37]. There are numerous factors which contribute to

the loss characteristics of a core material, including the process in which the tape wound core is epoxy bonded. To use this equation, one must know the mass of the core, the oscillation frequency, and the AC amplitude of the flux swing. These values have been analytically calculated in the developed "Nanocrystalline inductor calculator", which can be found in the appendix.

$$P_{loss\_core} = mass \cdot 1.79 f^{1.51} \cdot Bac^{1.74}$$

(27)

Due to the complex operation of the DC-DC converter, the inductor calculator developed is correspondingly complex. Since the current waveform as well as switching frequency depends on many system parameters, the calculator must be able to sweep the output power for a given set of conditions, and calculate the accompanying system information for each of the desired conditions. To calculate core loss many calculation steps are taken, which are described below.

1. Input all required system information and desired configuration

    a. operating parameters, including voltages, snubber capacitors.

    b. Input desired inductance and number of copper turns.

    c. Input core material specifications, specifically saturation flux density

    d. Input copper foil width (used to generate some core geometry)

    e. Input major core geometry, including wound dimensions, winding window dimensions, number of desired gaps, and the material stacking density when the core is epoxy fused

2. The corresponding core specifications are calculated, including:

    a. Effective core area, A_e

    b. Magnetic length

    c. Core mass, based on density of material, effective area, and magnetic length)

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d. The desired A_L value, based on the desired N and inductance

e. Saturation current, based on A_e, N, B_{max}, and inductance

3. Positive and negative peak current vs. frequency calculation is performed using resonant equations of the soft-switching topology.

a. B_{ac} is calculated based on the calculated peak currents

4. Core power loss vs. frequency is calculated using the empirical loss equation for the material.

a. Core loss vs. output power is graphed using output power vs. frequency and core loss vs. frequency equations.

Distributed Gap Design and Modeling

The theoretical estimation of core losses has some assumptions, a major one being that the effective gapping is fully distributed, meaning that there are no core losses associated with fringing and gap loss. In reality, there can only be a limited number of air gaps, with the tradeoff being between manufacturing difficulty and performance. To quantify the necessary number of gaps, a fringing ratio calculation was performed, as shown in equation 29, which compares the geometry of the core area to the gap distance. As a rule of thumb, the core manufacturer recommends that the calculated fringing factor stay below 5-6%, which is a nominal tradeoff between manufacturing complexity and additional gap losses. The number of gaps can then be selected so as to result in a sufficiently low fringing factor. When calculating the necessary gap, if the effect of fringing is not considered, it can be found with equation 28. When considering the fringing factor, the recursive equation 30 could be directly solved, or the result from equation 28 could be used as a close estimation to reduce mathematical complexity.

$$gap = \frac{\left(\mu_0 \cdot N^2\right)\left(\dim a\right)\left(\dim d\right)}{L} - \frac{maglength}{\mu_r} \tag{28}$$

$$F_{fring} = \frac{\left(\dim a + \frac{gap}{cuts}\right)\left(\dim d + \frac{gap}{cuts}\right)}{\dim a \cdot \dim d} \tag{29}$$

$$gap_{fringing} = \frac{\left(\mu_0 \cdot N^2\right)\left(\dim a + \frac{gap}{cuts}\right)\left(\dim d + \frac{gap}{cuts}\right)}{\dim a \cdot \dim d} - \frac{maglength}{\mu_r} \tag{30}$$

The calculation of output power versus frequency depends on the input voltage, output voltage, snubber capacitance, and inductance. Since the converter is peak-current mode controlled, on the operation of the resonant periods in addition to the linear on and off periods of the operation decides the switching frequency. To determine the output power to frequency relationship, the converter operation equations are solved to find period, and the inductor current in each mode is integrated, to determine the energy processed in that period, which yields a power to correspond to the calculated period. The output power versus frequency for both the 20 uH and 32 uH inductors can be seen in Figure 51 and Figure 52. The core and copper losses (copper loss to be discussed in a later section) can be seen in Figure 53 and Figure 54.

Output Power vs. Frequency @ 200V
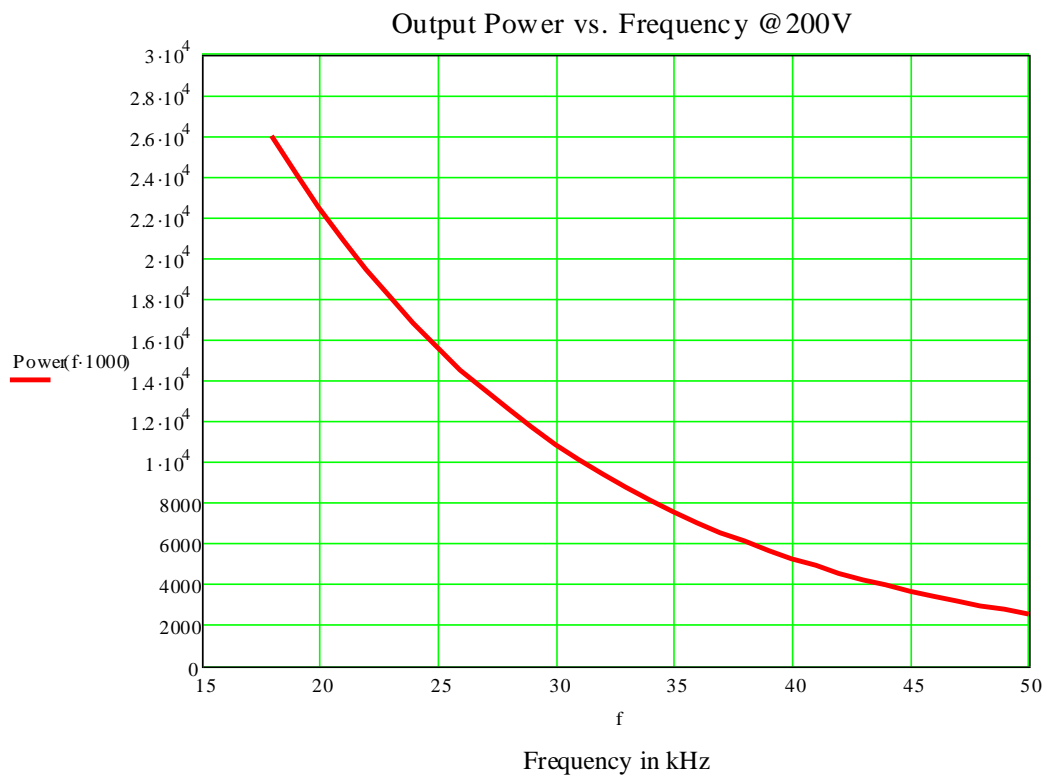
Figure 51 20uH Inductor output power vs. frequency @200V - 700V

Output Power vs. Frequency
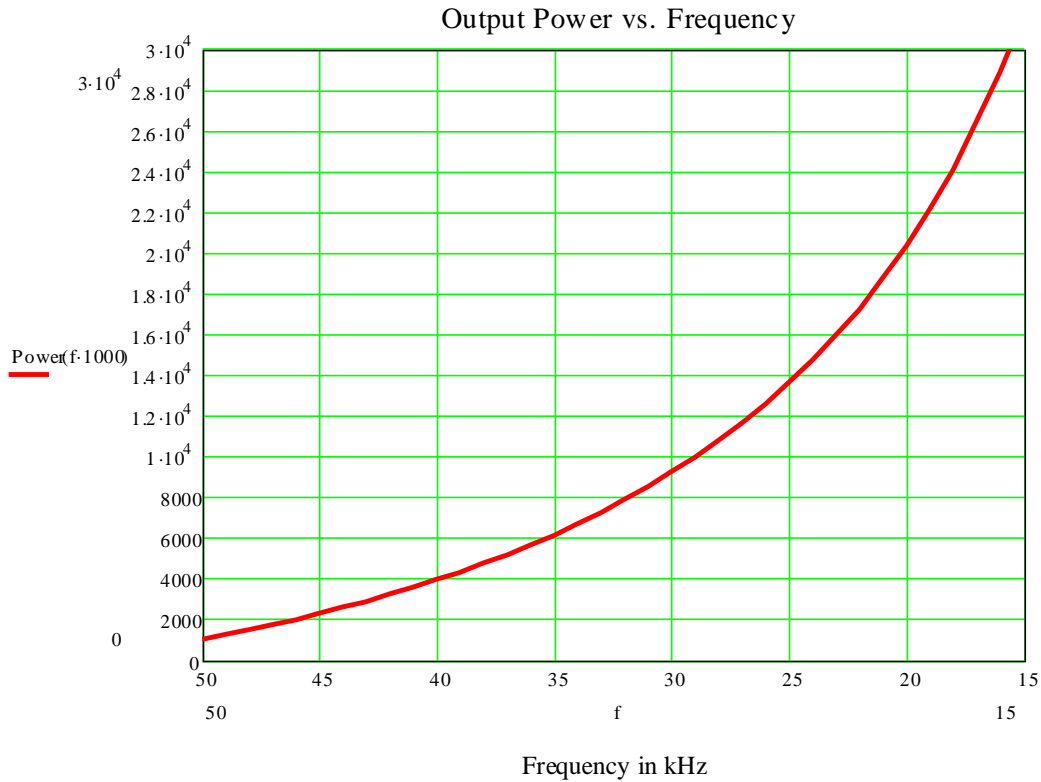
Figure 52 32uH Inductor output power versus frequency @ 300V - 600V

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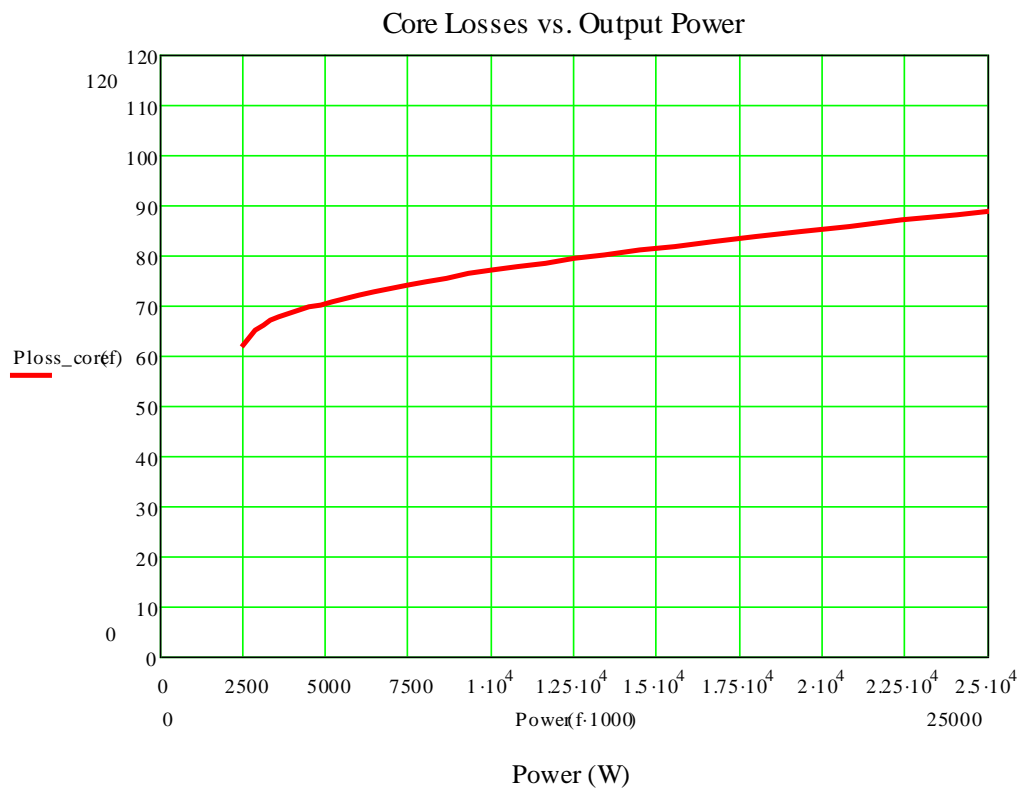
Figure 53 Calculated 20uH inductor losses vs. output power
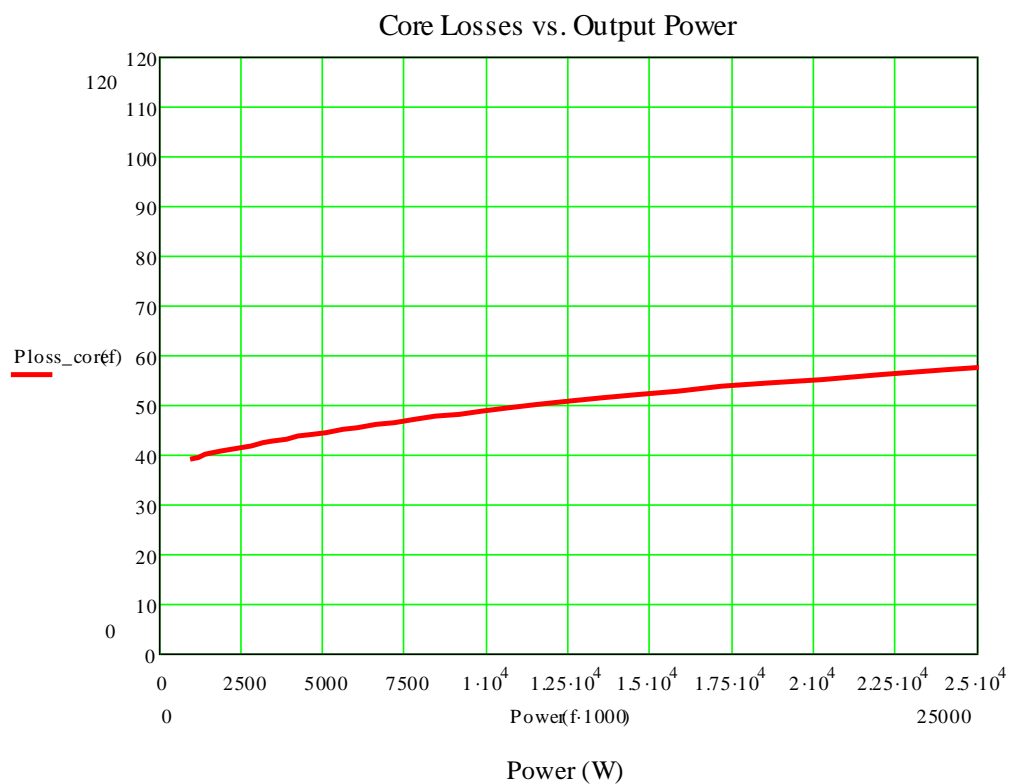
Figure 54 32uH Calculated inductor losses vs. output power

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Once the core design has been reasonably optimized, the corresponding inductor design can be simulated using 2D FEA software, allowing verification of the core design, visualization of the gap fringing, and calculation of copper losses during the winding optimization stage. The simulation results at full power can be seen in Figure 55 and Figure 56. The simulation is only of the AC flux, since the DC offset will have little effect on losses, given that the inductor is operated within the linear B-H curve. Furthermore, the FEA simulation can only simulate a single frequency at a time. To determine the losses associated with the non-sinusoidal current waveform, the calculator performs Fourier analysis to find the first 6 harmonics, of which simulation of the first 3 is reasonably sufficient. The FEA simulation must be executed with the current and frequency of the waveform harmonics, allowing the determination of the effects of higher frequency components on the design. The total copper losses are the sum of the individual harmonics, in addition to the DC current loss. It can be seen from the simulations that the gap fringing does extend to the copper conductors, but, the flux strength at the point where it interacts with the foil conductors is minimal, generally less than 0.04 T.
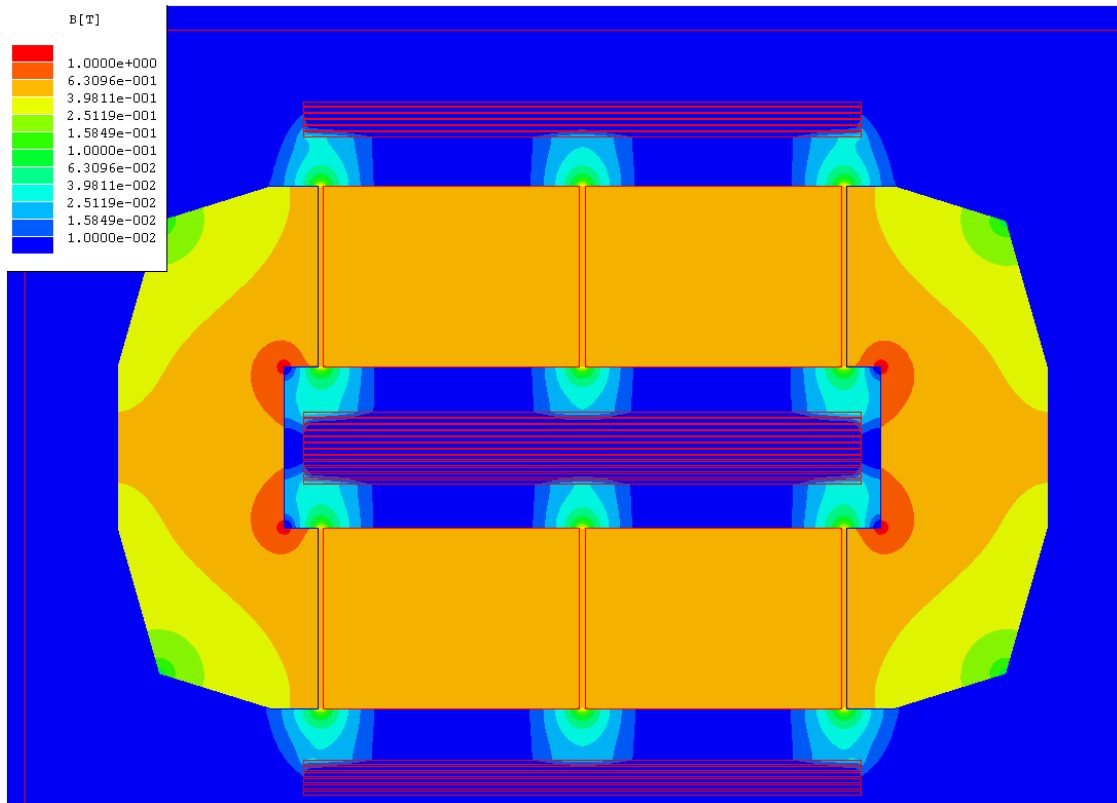
Figure 55 Simulation of the 20uH distributed gap inductor at 20kW
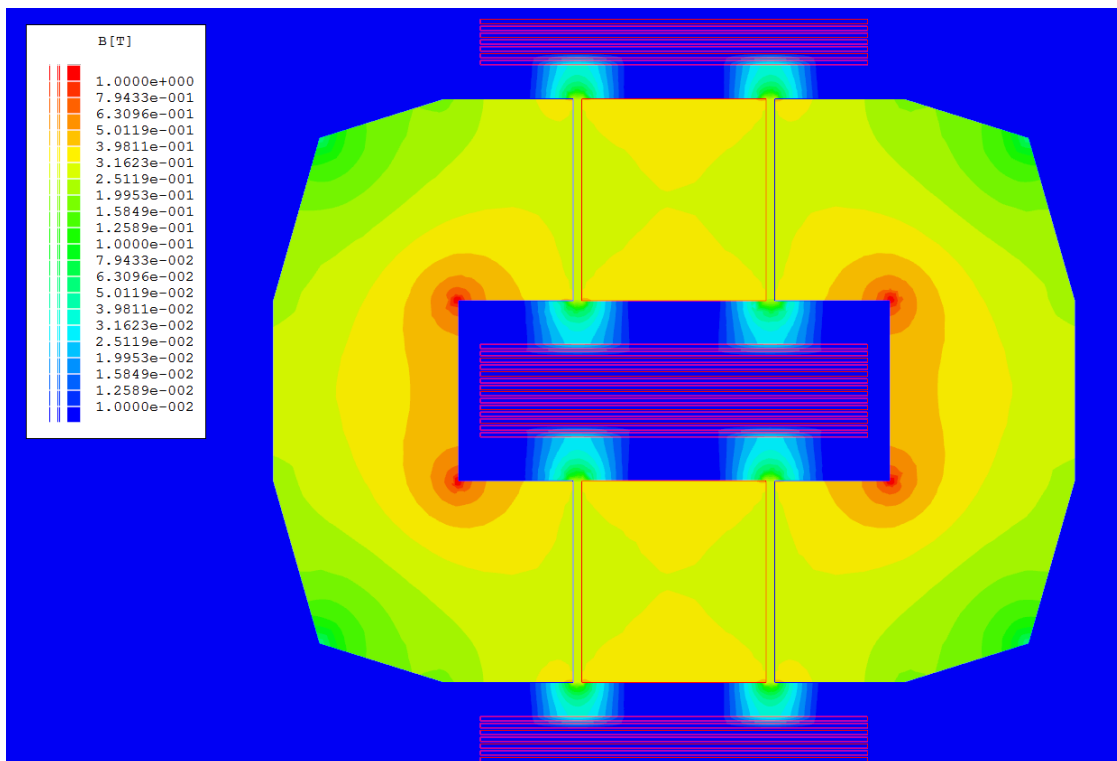
Figure 56 Simulation of the 32uH distributed gap inductor at 20 kW

As can be seen from the simulated results, the second design iteration of 32 uH is significantly smaller than the 20 uH design. It is apparent, though, that the 32 uH design utilizes only 4 gaps, whereas the 20 uH inductor uses 6 distributed gaps. The fringing flux in the 32 uH design is greater, as shown by higher intensity flux contacting the windings. While this does result in higher gap losses, it was revealed that the gap losses were ultimately similar, one reason being that there are simply less gaps, and also that the 20 uH inductor operates at higher frequency, which increases the effect of the gap flux on the windings. The final dimensions of the 32 uH inductor can be seen in Figure 57 and Figure 58. The core is coated with an electrically isolating epoxy as a post-process, which is shown by the blue coating on the inductor.
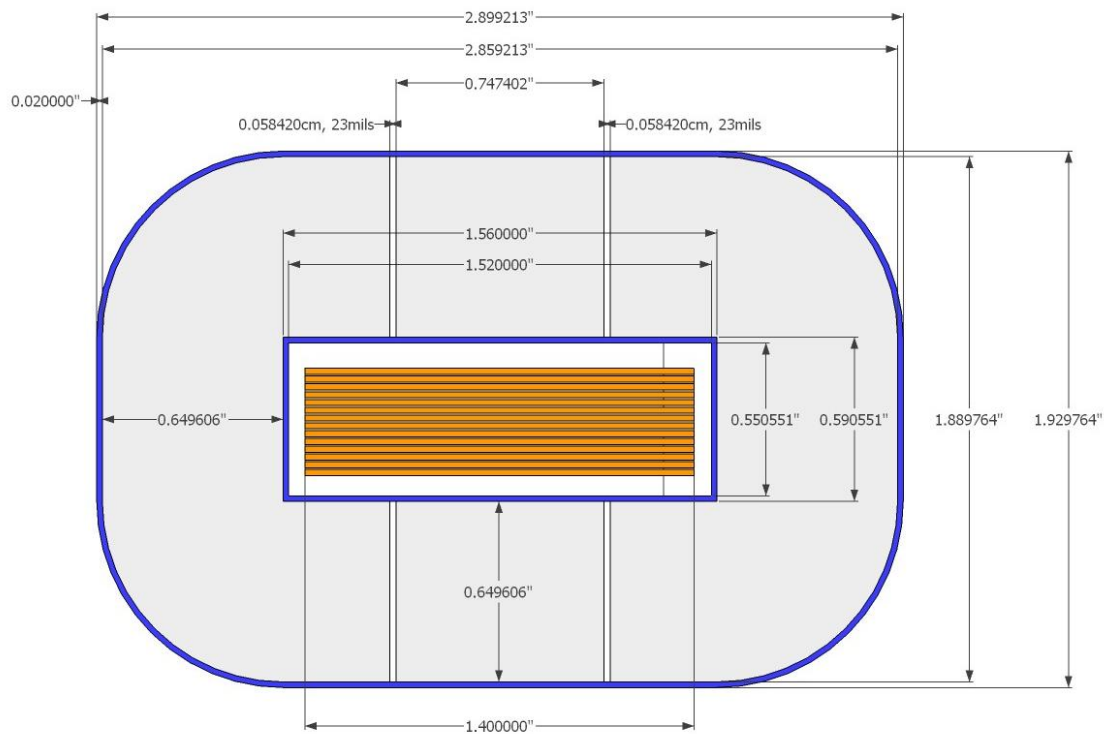
Figure 57 32uH Nanocrystalline inductor design
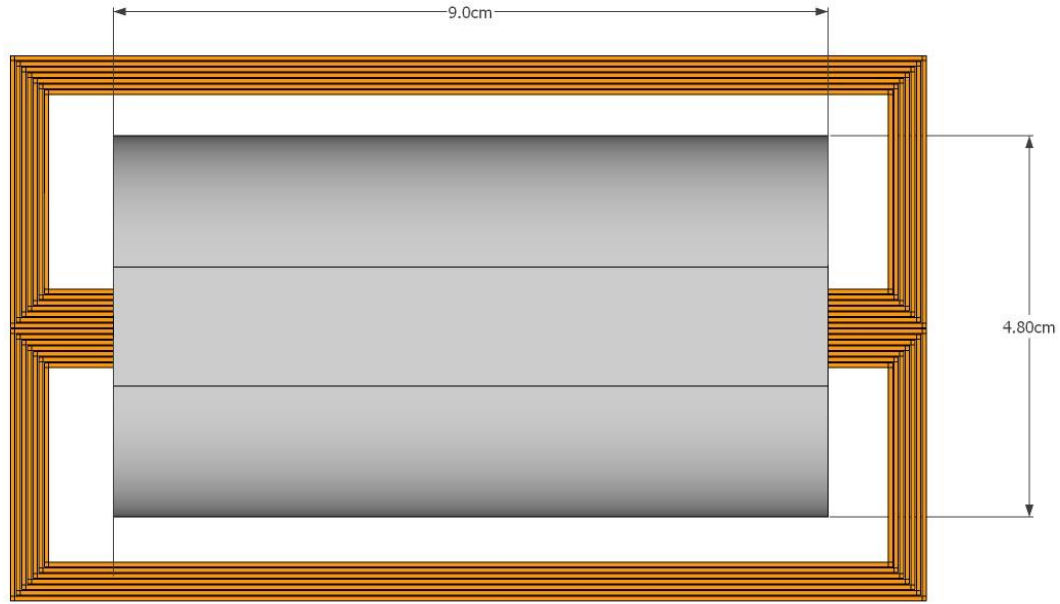
Figure 58 Side view of 32uH inductor

The prototype 20uH inductor featured 6 gaps, which each must be separated by a gap filling material, and epoxy fused to create a single core. The gap material should be dimensionally stable at high temperature, and the epoxy should be thermally conductive, to allow heat generated in the inner core pieces to conduct through the gaps. A fiberglass gap material was used, to stabilize the gaps, and epoxy with thermal conductivity exceeding 1W/m°C . To protect the insulation on the copper foil conductors from becoming damaged by the metallic nanocrystalline material, the 20 uH inductor was wrapped with high temperature polyimide tape. The 20 uH core is shown in Figure 59.
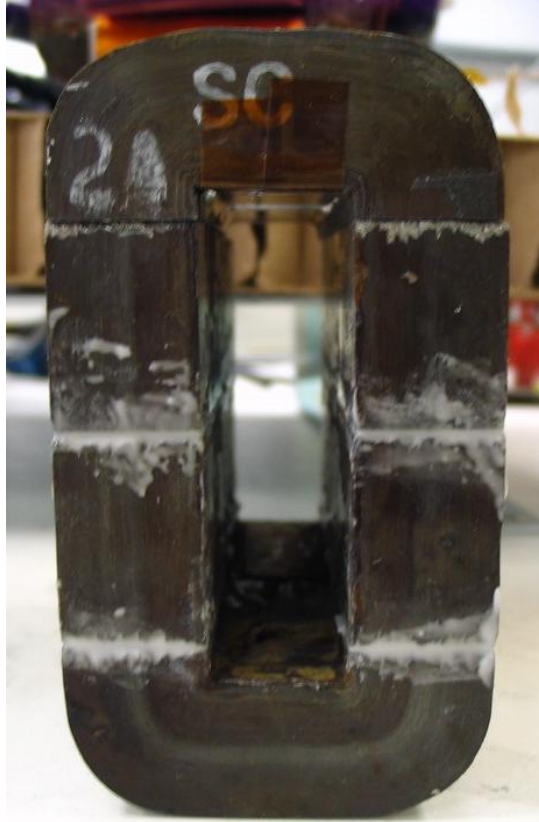
Figure 59 20uH distributed gap core w/ gaps fixed using thermal epoxy

Figure 60 32 uH nanocrystalline inductor core

The second design iteration resulted in the development of the 32 uH inductor core, as can be seen in Figure 60. This core features 4 gaps, and has a smaller winding window, increasing density, and decreasing core losses. While it is sometimes counterintuitive, the smaller inductor core is potentially more efficient, since there is less core material to create loss. When comparing the 32 uH design to the 20 uH design, the effective core area is identical, but since smaller copper foil could be used due to lower peak current, the core width could be significantly reduced. Instead of using high temperature polyimide tape to insulate the core as in the 20 uH design, the 32 uH inductor was epoxy coated as a post-process. For detailed information on the core designs, calculations, and simulations, refer to the Appendix.

Copper Foil Winding Design and Optimization

The inductor cores are designed to utilize copper foil conductors, which are well suited for this application, where low AC resistance is required, due to the high amplitude of the AC current in the inductor. The copper foil conductors are the least susceptible to losses due to the skin effect and the proximity effect. The skin effect is the tendency for AC current to crowd onto the outer surface of the conductor, thereby increasing the effective resistance of the conductor. By using copper foil conductors, the largely wasted inner core of a round wire conductor is removed, thus increasing the density and performance of the design. The proximity effect is similar in nature, but it is the tendency for current within groups of electrically isolated conductors to crowd onto the outer regions of the group. In this case, each conductor still will carry the full current, but the current density will increase at portions of the conductor area which are nearer to the outside of the conductor group. The proximity effect is typically less known to inductor designers, and is often overlooked in loss calculations, especially when the application is for low AC current and lower density, where the conductors are more spaced out from each

other. In this case, since the AC current ripple is so much larger than the DC current, the proximity effect plays a major role in the overall inductor losses. The prevailing losses in the conductors are the simple i^2r losses from the DC current, the AC current losses due to skin effect and proximity effect, and the gap losses, caused by the fringe AC flux escaping from the inductor core air gap. As discussed earlier in this chapter, as the AC flux travels within the air gap, there is a tendency for the AC flux to inducing heating in the copper conductor. A new winding concept for reduced AC resistance is presented in [38], where the copper which is exposed to the gap fringing is shaped to more evenly disperse the effect of the AC flux across multiple conductors. While this approach seems to have promise, in this case it is not feasible to construct, considering the complexity of the copper foil geometry.

The design of the winding for the inductor has many variables, and is exceedingly difficult to estimate the conductor losses, especially when there is potential gap loss. Nevertheless, by performing a high-fidelity analysis a nearly-optimal design can be achieved, which can then be finalized iteratively utilizing FEA software. The simulations allow the performance of the inductor to be visualized, allowing optimization through sequential changes of certain parameters. The simulation, in addition to being able to visualize the flux density, and the current density in the inductor, allows for the mathematical integration of the 2D conductor surface resulting in a quantifiable amount of power loss. Early in the design process, the inductor was modeled with the copper foil winding only around one side of the core, so as to allow the inductor core to have better thermal impedance to the cooling plate. From simulation it was observed that the severity of the gap loss and the proximity effect is dominating in that design for varying reasons. The reasons for increased proximity effect are obvious, in that a larger group of conductors will have a more substantial effect. It was also observed that the gap

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loss at the conductor edges inside the winding window was also very high, as can be seen in Figure 61. It is apparent that the flux density is higher in the upper core material than the lower, and that there is significant flux bridging from each gap at the ends to the corresponding gap on the other side. This is since the bottom inductor leg doesn't have a winding which is forcing the flux to travel equally through the top and bottom pieces, thus reducing the tendency for the gap fringing flux to try to find another path back into the other side of the core. Because of this behavior, as the flux passes through the edges of the inner copper foil it induces higher losses. The general structure of the final design was the solution to mitigating the gap loss and proximity effect, where there are two separate copper foil windings, which are paralleled at the terminals of the converter. Due to the reduction in gap fringing, the effective gap length is increased, thus reducing the inductance. This reduction must be taken into account when selecting the gap sizes, with the preferred method being to build an initial prototype without permanently fixed gaps, so as to experiment until the proper gap is determined.
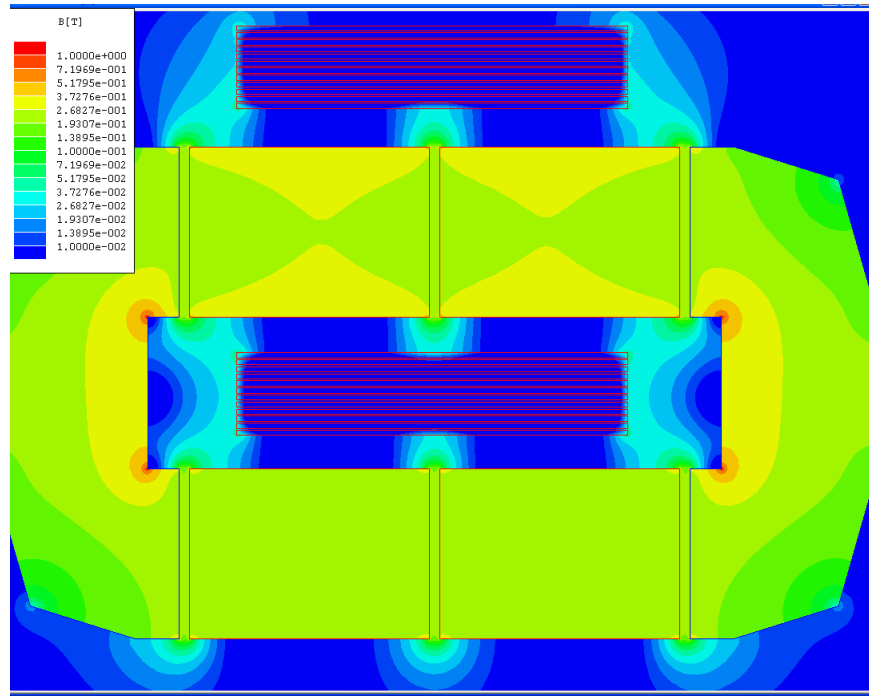
Figure 61 Simulated gap loss in early inductor design, leading to split winding design

Conductor Loss Estimation

The same calculation tool developed for core design optimization has the ability to estimate conductor losses including DC loss, higher AC losses from the skin effect, higher AC losses from the proximity effect, as well as consideration for an increase in the copper resistance due to higher temperature. The AC losses are calculated using Dowell's method, illustrated in [36]. Although this calculation is very detailed, there is still a significant amount of error, which can only be truly determined through FEA simulation, and ultimately through prototyping. The core loss calculation process is as follows, for more detailed information consult the calculator in the Appendix.

1. Input all additional required system information and desired configuration, beyond what is already used from the core loss calculator

    a. Number of paralleled conductors

    b. Copper width

    c. Copper thickness

    d. Thickness of polyimide insulating tape

2. The corresponding winding geometry specifications are generated

    a. Window fill factor is calculated (including tape)

    b. Window fill density is calculated (copper vs window)

    c. Number of copper layers calculated, ml

3. Generate functions calculating design factors

    a. Generate skin depth vs. frequency function, equation 31

$$depth_{skin}(f) = \sqrt{2 \cdot \frac{\rho}{2\pi \cdot f \cdot \mu \cdot \mu_0}} \tag{31}$$

b. Generate ξ vs. frequency function, equation 32

$$\xi(f) = \frac{h^2}{(h + tape) \cdot depth_{skin}(f)}$$
(32)

c. Generate the AC to DC resistance ratio vs. frequency function, equation 33

$$F_r(f) = \frac{\xi(f)}{2} \left[\left(\frac{\sinh(\xi(f)) + \sin(\xi(f))}{\cosh(\xi(f)) - \cos(\xi(f))} \right) + (2ml - 1)^2 \cdot \left(\frac{\sinh(\xi(f)) - \sin(\xi(f))}{\cosh(\xi(f)) + \cos(\xi(f))} \right) \right]$$
(33)

d. Calculate the 25°C DC resistance based on conductor area, length, conductivity, and number of parallel conductors

e. Generate the DC resistance vs. temperature function, based on empirical copper design equations

4. Copper power loss vs. frequency is calculated using RMS current Fourier expansion of current waveform.

a. DC loss is calculated using RMS current vs. frequency function and temperature normalized DC resistance function

b. AC loss for each harmonic of the inductor current for a given switching frequency is calculated and summed, using the AC resistance vs. frequency function

c. Total losses are calculated by summing all DC and AC losses

The conductor loss calculator generates a plot of losses versus frequency, which can also be used with the output power vs. frequency function to plot losses versus output power. As can be seen from the loss plot for the 20 uH inductor in and the 32 uH inductor in , even though there is a slight increase in copper loss for the 32 uH inductor, the reduction in core losses results in an inductor with similar light-load losses, but with 35 W less loss at higher power. Another way of visualizing the performance is by plotting the efficiency of the inductor, as shown in Figure 64.

Inductor Losses vs. Output Power

Ploss_copper(f·kHz)

Ploss_core(f)

Ploss_total(f)

Power(f·1000)
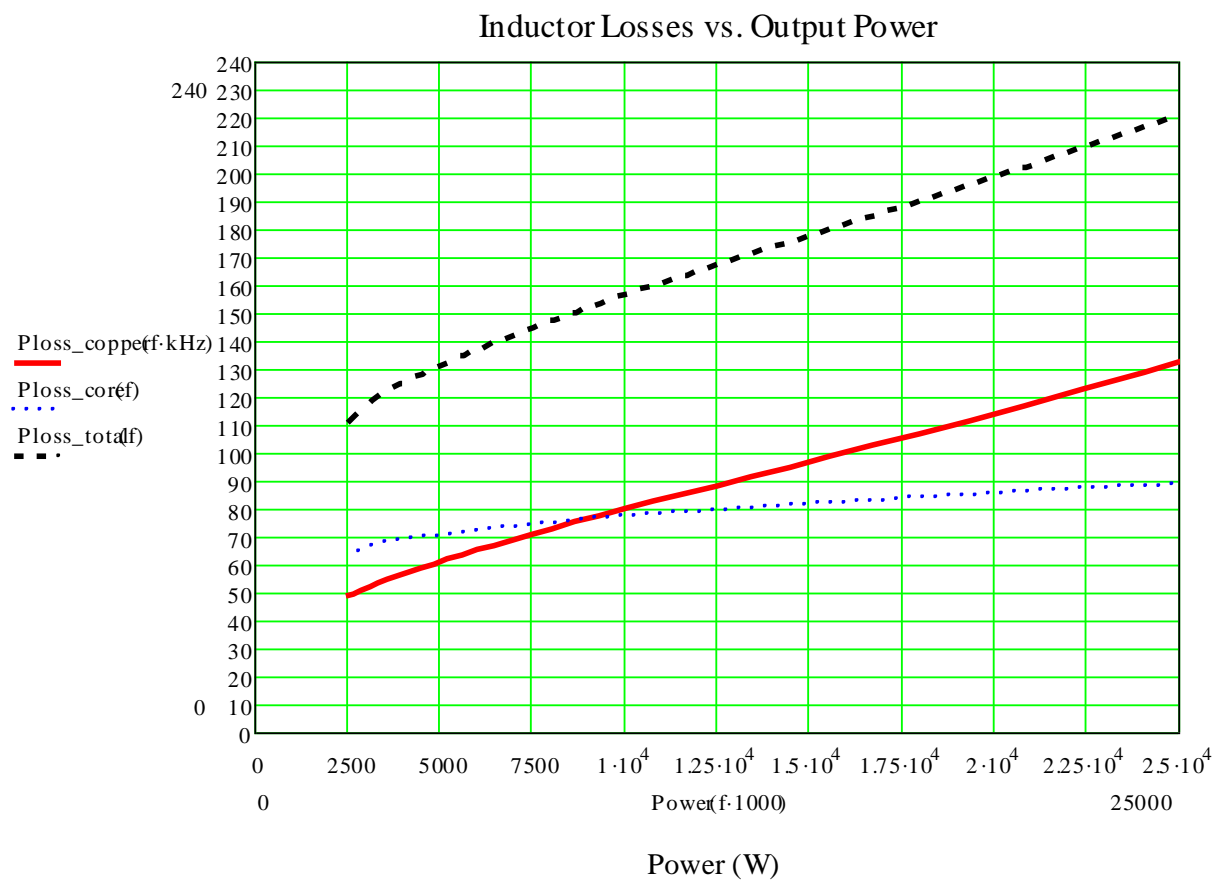
Power (W)

Figure 62 20 uH inductor total losses vs. output power

Inductor Losses vs. Output Power
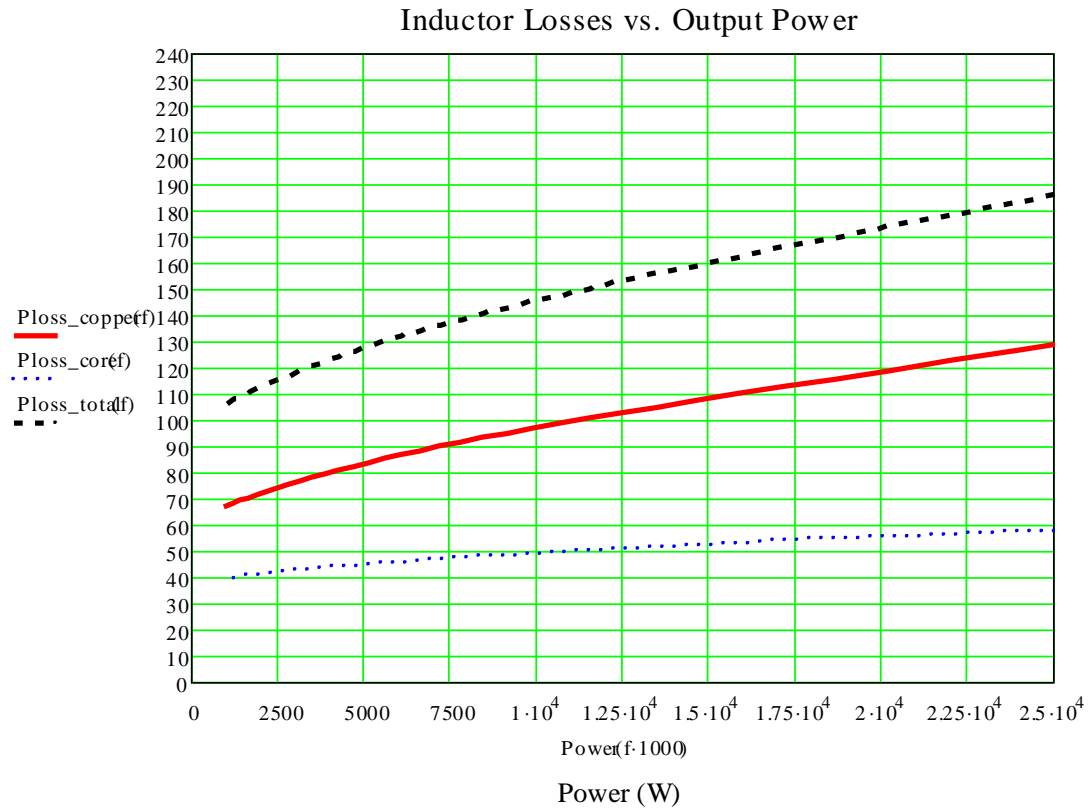
Figure 63 32 uH inductor total losses vs. output power

Inductor Efficiency vs. Output Power
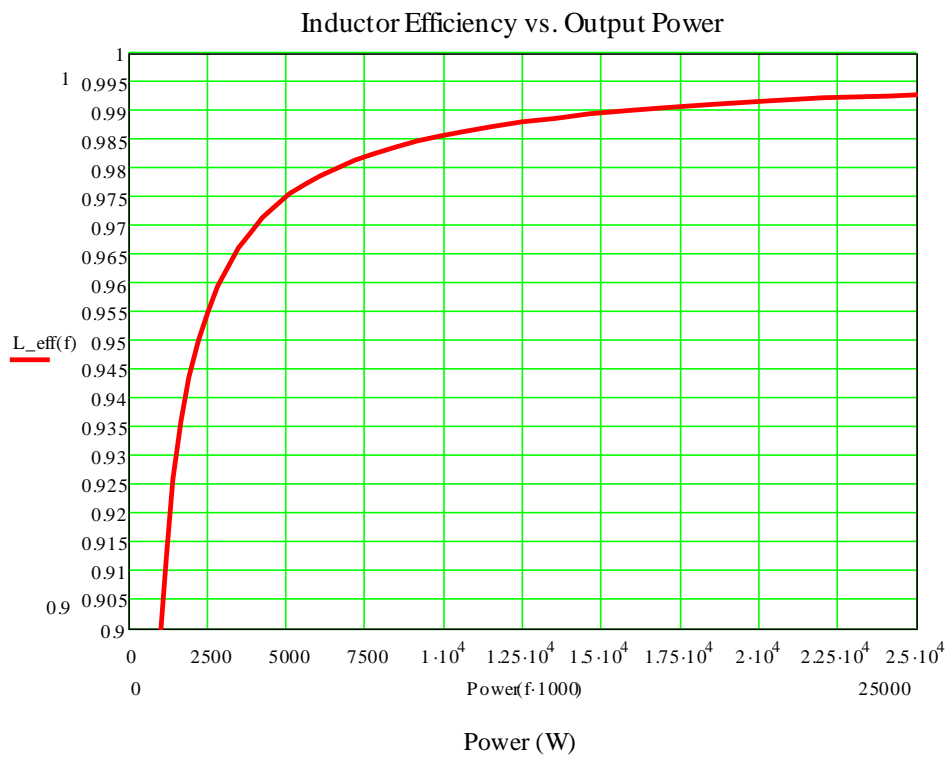
Figure 64 32uH inductor efficiency vs. output power

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FEA Simulation of Conductor Loss

Once the inductor design has been relatively optimized using the inductor calculator, the next step is to perform further analysis and optimization using FEA software. The core geometry is setup as a high permeability homogeneous material, although this is not actually true of the nanocrystalline material. Since the primary purpose of the FEA simulation is to optimize the core geometry and the copper losses, the additional information available through trying to more accurately model the many layers of the nanocrystalline material wouldn't be worth the significant effort. The individual copper conductors must be designed to the specification, with a reasonable air gap in-between each conductor, representing the insulating tape and spacing. Once the conductors are established, the current sources must be established. Since the inductor has 6 or 7 turns of the winding foil, with the winding actually being two conductors in parallel, a specific current source should be established which shares the current between each corresponding winding, this allows the simulation to identify, if need be, that there may be unequal current flow between the two winding strips.
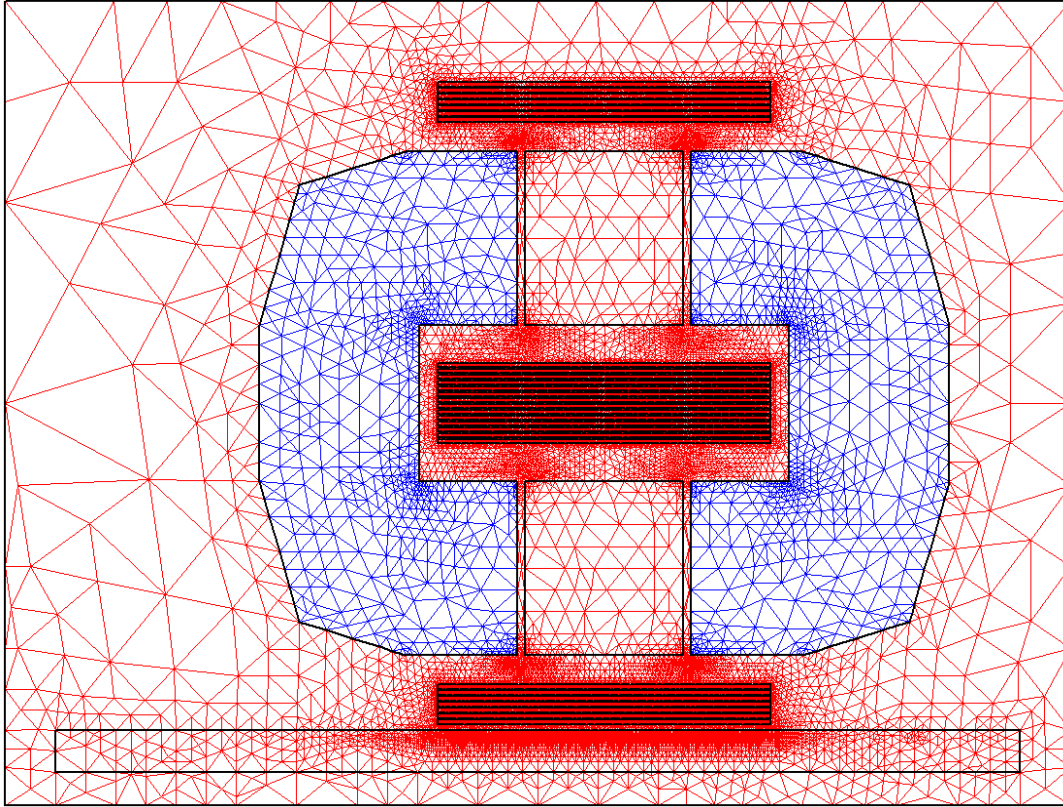
Figure 65 Manually generated mesh for inductor FEA simulation

To set up the structure for simulation, a nodal mesh must be generated. This mesh establishes the points which should be analyzed. In regions which are expected to have more variation in data per unit area it is desired to have a more fine pitched mesh, allowing more accurate data. By limiting the mesh resolution in less critical or active regions of the core, the complexity and processing time of the simulation is greatly reduced. The simulation is executed with the current source operating at a specific frequency with a specific AC current. The operating conditions are available from the inductor design calculator, which provides a breakdown of the frequency and current level for the higher frequency harmonics of the current waveform. In this way, the simulation can be run for each of the more critical harmonics, the sum of which resulting in a more accurate loss estimation.

The current crowding due to the proximity effect can be seen in Figure 66. Even with the use of copper foil with a skin depth exceeding the thickness of the foil, there is still a severe crowding effect, showing the prevalence and importance of the proximity effect greatly exceeds that of the skin effect in this case. The severity of the effect depends on many factors, including the copper width, thickness, and the spacing between the conductors. In this way the FEA simulation can help to optimize the design, as various configurations can be analyzed and tested.
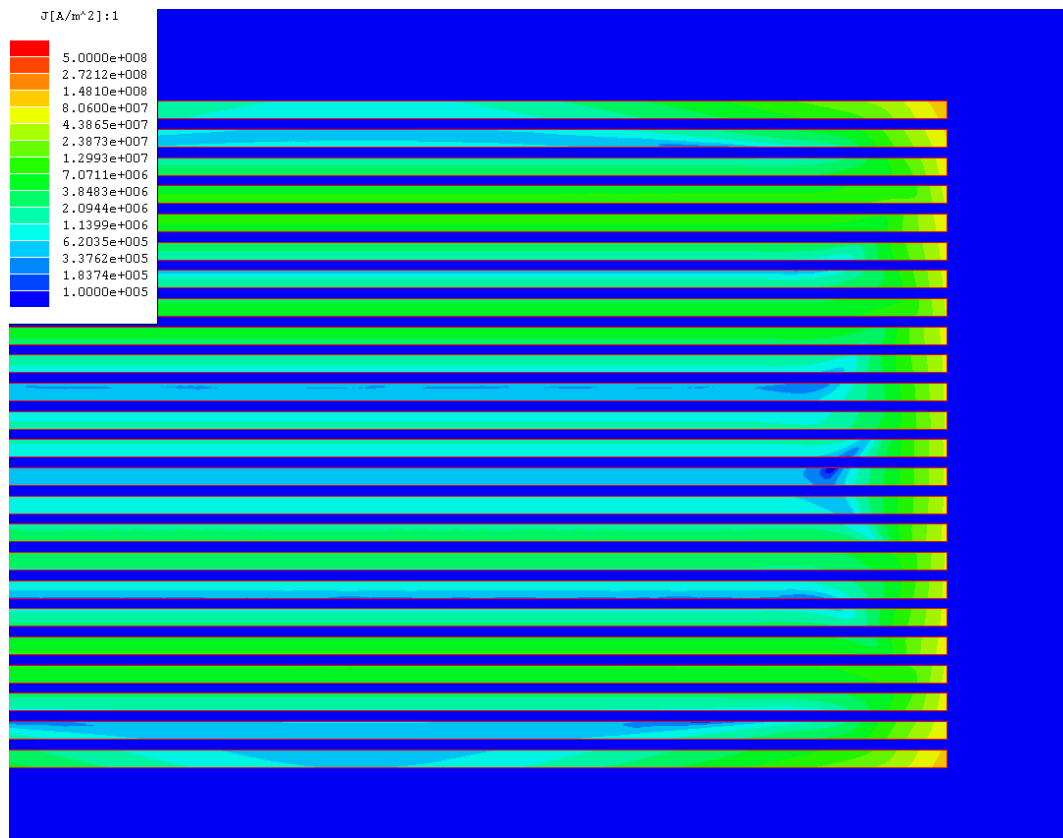
Figure 66 Simulation showing crowding from proximity effect
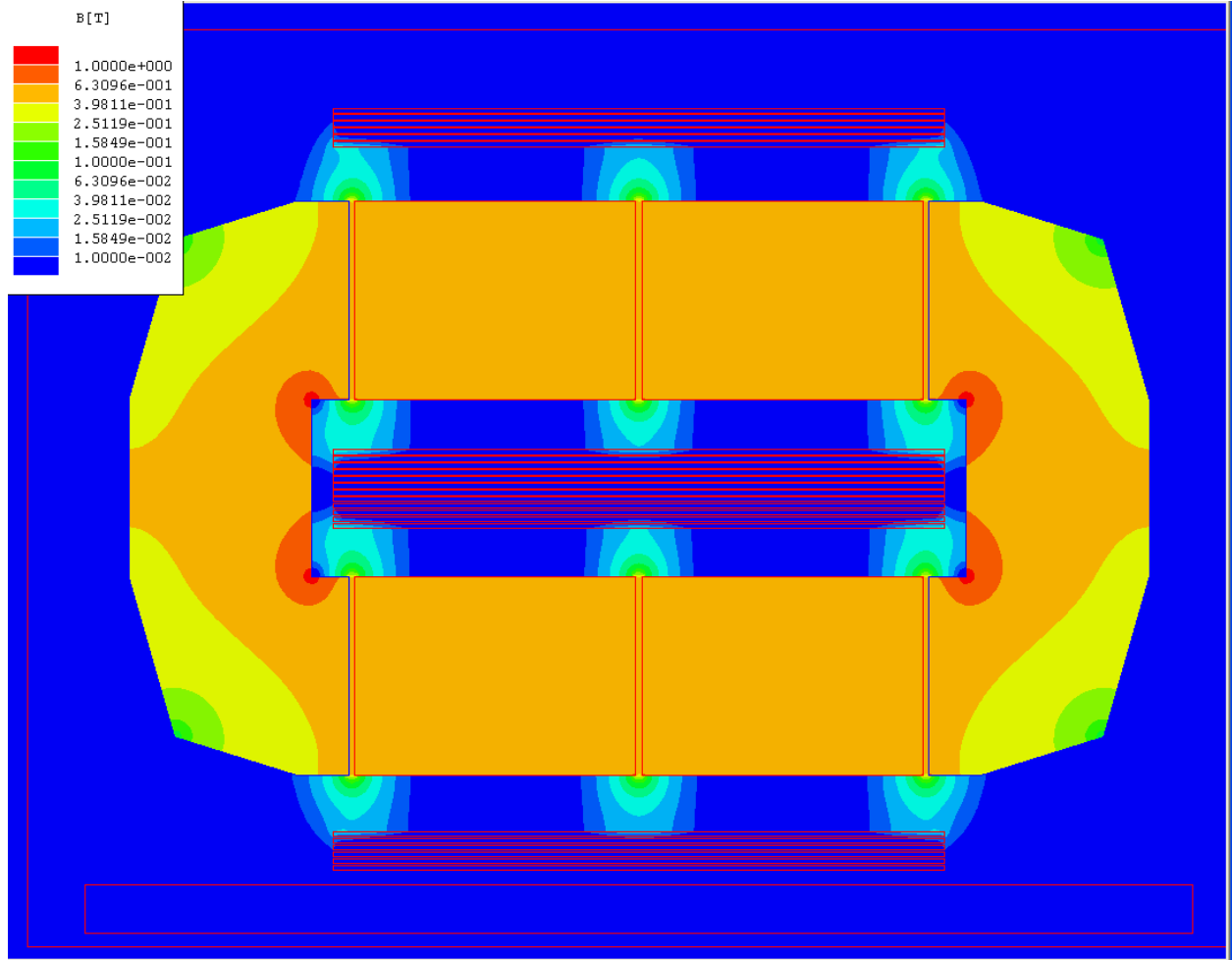
Figure 67 Simulation of the 20uH distributed gap inductor at full power

Besides the core design, the winding structure is very important for the optimization of the losses. By using the simulation of the inductor, different copper foil winding structures were analyzed to determine the ideal solution. It was found that the structure shown in Figure 67 was the most ideal, as the simulated copper losses were the least. It should be noted that with a high-density design, the crowding effect becomes a leading source of copper loss. This is similar to the skin effect, in that the current density will increase around the edges of a copper foil group at higher frequencies. For this reason, the optimal design is not simply to use the thickest foil that can fit in the window. Furthermore, the existence of the multiple gaps serves to induce losses in the copper that is near the gap. The losses can be minimized by evaluating the tradeoff between

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copper thickness and distance from the gaps. The simulation for the 32 uH inductor is shown in Figure 68. As can be seen, with fewer gaps which are wider, the fringing of the 32 uH inductor is slightly greater, but the effect may not necessarily be much worse than the 20 uH inductor, since there are fewer gaps to create loss.
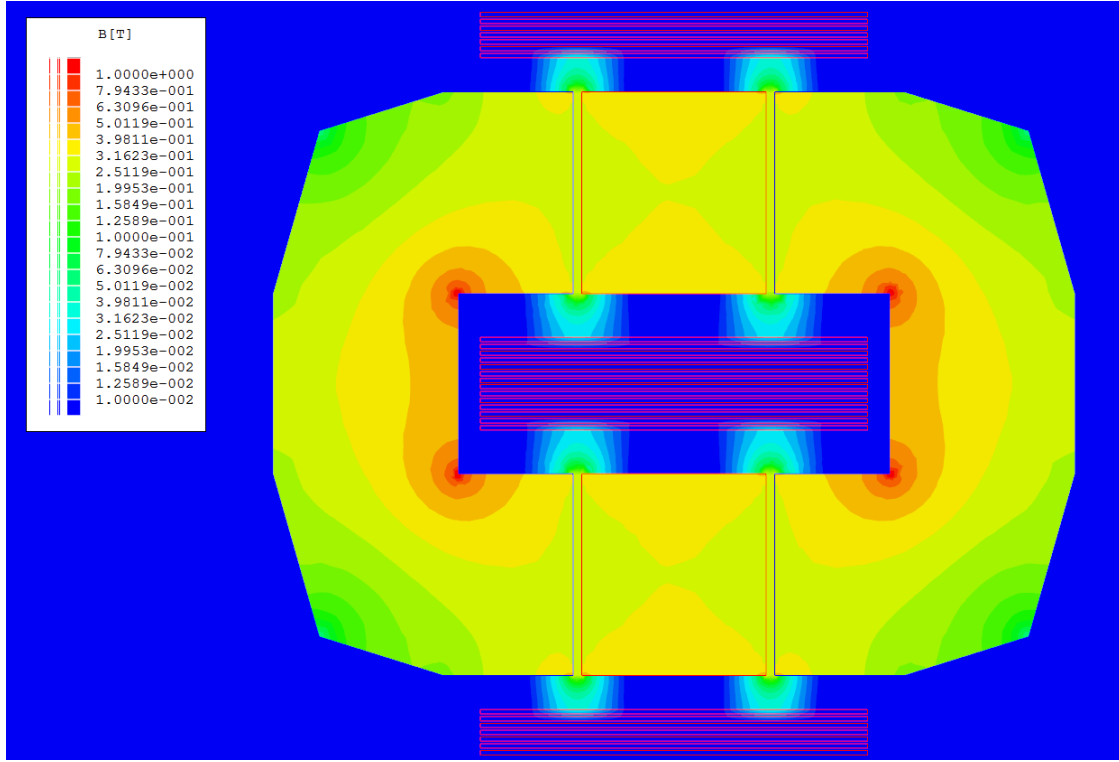
Figure 68 Simulation of the 32uH distributed gap inductor at 20 kW

During the course of FEA simulation and optimization, variations of the design generated in the inductor calculator were tried, so as to obtain the most optimal design. To determine the copper losses, the analysis tool was used to integrate the power loss over the surface of the conductors, yielding a result in terms of power per meter. Since the inductor design is relatively uniform along the length, the generated W/m loss value can be multiplied by the length of the inductor to determine the expected AC copper losses. The results from iterative optimization of the inductor designs are shown in Table 5 for the 20 uH inductor, and Table 6 for the 32 uH inductor. For the 20 uH inductor, during the optimization process, it was determined that

splitting the windings across each side of the inductor had the benefit of reducing the copper loss from fringing, as well as reducing the necessary air gap, which further decreases losses. The optimal design was found to use two 2" wide copper foil conductors, each 0.016" thick, with a minimum spacing of 0.18" between the outer windings and the core. For the 32 uH inductor, the simulations #4, #6, and #7 have similar loss characteristics, and although #6 was found to have slightly higher loss than the others, it was ultimately selected for the design. There are multiple reasons for this, one reason is that the wider core window will allow more flexibility for experimental optimization; another reason is that although the simulations seem to be high fidelity, when comparing two designs which are essentially equal in loss, having lower DC resistance might turn out to be more optimal over a wide operating range. Also, the wider conductor will be more efficient outside of the core, in the wiring which connects to the converter. After final design and production of the core, it was later determined that 1.375" copper strips would be easier to fit in the winding window, due to unexpected additional epoxy thickness in the core window. Based on the simulation, it was clear that there would be minimal tradeoff to utilize the slightly thinner copper foil, as it is in-between simulations #6 and #7.

Table 5 Simulation results for 20 uH inductor, 2 x 175A @ 20 kHz

Simulation	Note	Copper Width (in)	Copper Thickness (mils)	Core to Winding Space (in)	AC Copper Loss (W)
#1	Single side winding	1.5	2 x 20	0.18	143.5
#2	Single side winding	1.5	4 x 10	0.18	162.8
#3	Single side winding	2	2 x 20	0.18	140.3
#4	Single side winding	2	2 x 16	0.18	120.8
#5	Single side winding	1.75	2 x 16	0.18	134.3
#6	#4 w/ Al coldplate 0.125" from core	2	2 x 16	0.18	120.8 + 27.5 in Al
#7	**Dual side winding**	**2**	**2 x 16**	**0.18**	**103**
#8	Dual side winding	2	2 x 16	0.11	122

Table 6 Simulation results for 32 uH inductor, 2 x 96A @ 17 kHz, 7 turns

Simulation	Note	Copper Width (in)	Copper Thickness (mils)	17 kHz AC Copper Loss (W)	Total Copper Loss (W)
#1	8 Turns, 6 gaps, from 20 uH core	2	16	62	75
#2	7 Turns, 4 gaps, core too wide for structure	1.75	16	54.8	68
#3	6 Turns, , 4 gaps, Core loss too high	1.5	16	35.3	54.5
#4	7 Turns, 4 gaps	1.25	14	48	72
#5	7 Turns, 4 gaps	1.25	20	67.6	89
#6	**7 Turns, 4 gaps, selected for comparable losses to #7, optimal core width, and lower DC resistance**	**1.5**	**16**	**52.7**	**75**
#7	7 Turns, 4 gaps	1.25	16	50.5	72

Thermal Management

One critical point of the inductor design and analysis is the verification that the inductor will be adequately cooled, so as to prevent long-term fatigue and eventual failure. The inductor design calculator developed also utilizes the known losses versus output power to develop a plot of inductor temperature versus output power. The inductor is cooled from the top and bottom by liquid coldplates, which will cool the inductors immersed in an thermally conductive epoxy with coolant up to 100 ºC. Since the inductors will be cooled by relatively high temperature coolant, it is important to verify that the inductor cores will be adequately cooled, with a maximum desired temperature of 200 ºC. A major advantage of the nanocrystalline material is the ability to operate safely at 200 ºC, which relaxes the necessary cooling requirements, allowing the system to achieve high density without the need for complex inductor cooling systems.

The inductor temperature is calculated by finding the temperature gradient from the two coldplates (top and bottom) to the inductor cores. The structure is designed to use two 12 inches long coldplates to cool 4 inductors, which means that each coldplate must support half of the thermal load of 4 inductors. The other critical assumption is the effective distance between the core and the coldplate where the epoxy will resist heat flow. Based on the geometry of the windings, the distance of the core from the coldplate is 1.25 cm. By using the thermal impedance of the coldplates and the calculated impedance from the core to the coldplate, a function was created, solving for ΔT as a function of switching frequency. One important note is that the effect of the copper windings was not considered for this analysis, which will actually improve the performance, but would require more complex modeling and simulation to accurately represent. Based on the winding structure, the copper windings actually serve as a channel for heat near the center of the core to conduct to the coldplate. Since this will benefit the

performance, the mentality is that if the theoretical analysis is acceptable without the additional cooling effects of the copper windings, the performance in the real system will also be acceptable. The plots for temperature versus output power for the 20 uH and 32 uH inductors can be found in Figure 69 and Figure 70. As can be seen from the plots, the estimated inductor temperatures are less than 180 ºC at the full steady-state power of 20 kW, with the 20 uH inductor temperature approximately 15 ºC lower in temperature at 20 kW. The better thermal performance of the 20 uH inductor is due to the larger exposed core area, allowing the similar losses to have a larger cross-section of thermally conductive epoxy area to flow through, resulting in a lower thermal impedance. Although it would seem that the 32 uH inductor is less optimal, the desire for high density exceeds that of lower temperature.
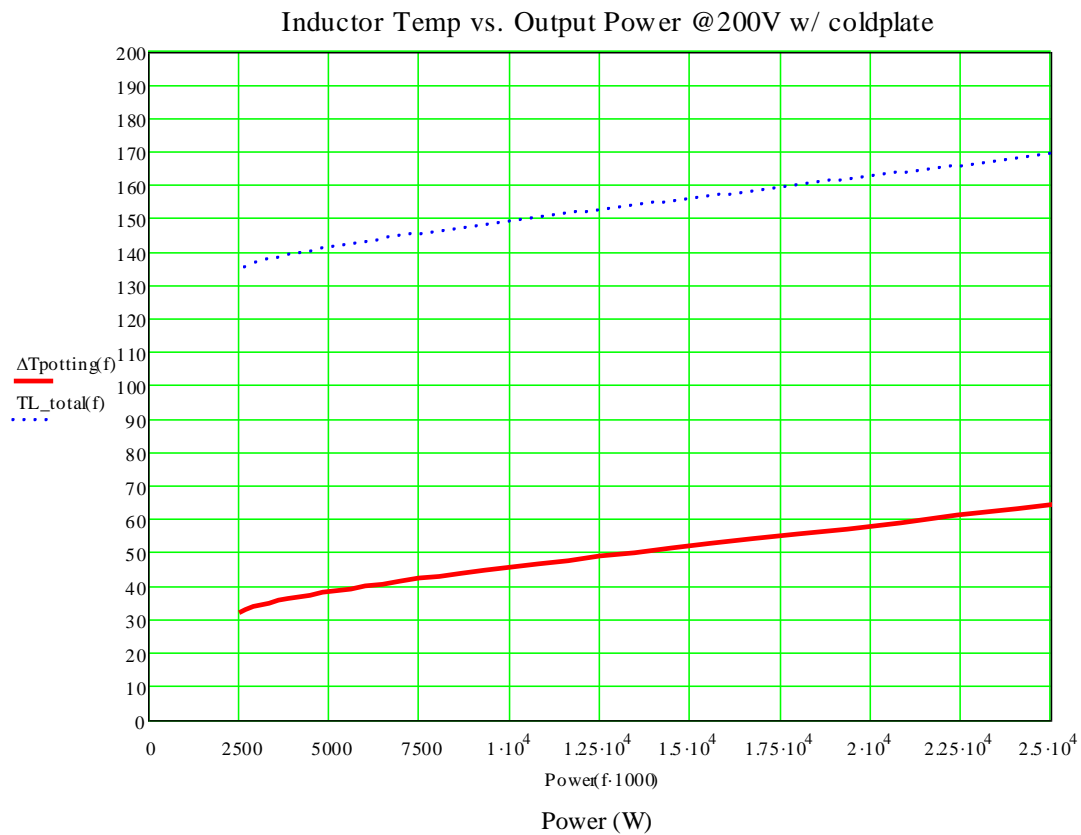
Figure 69 Plot of 20 uH inductor temperature versus output power

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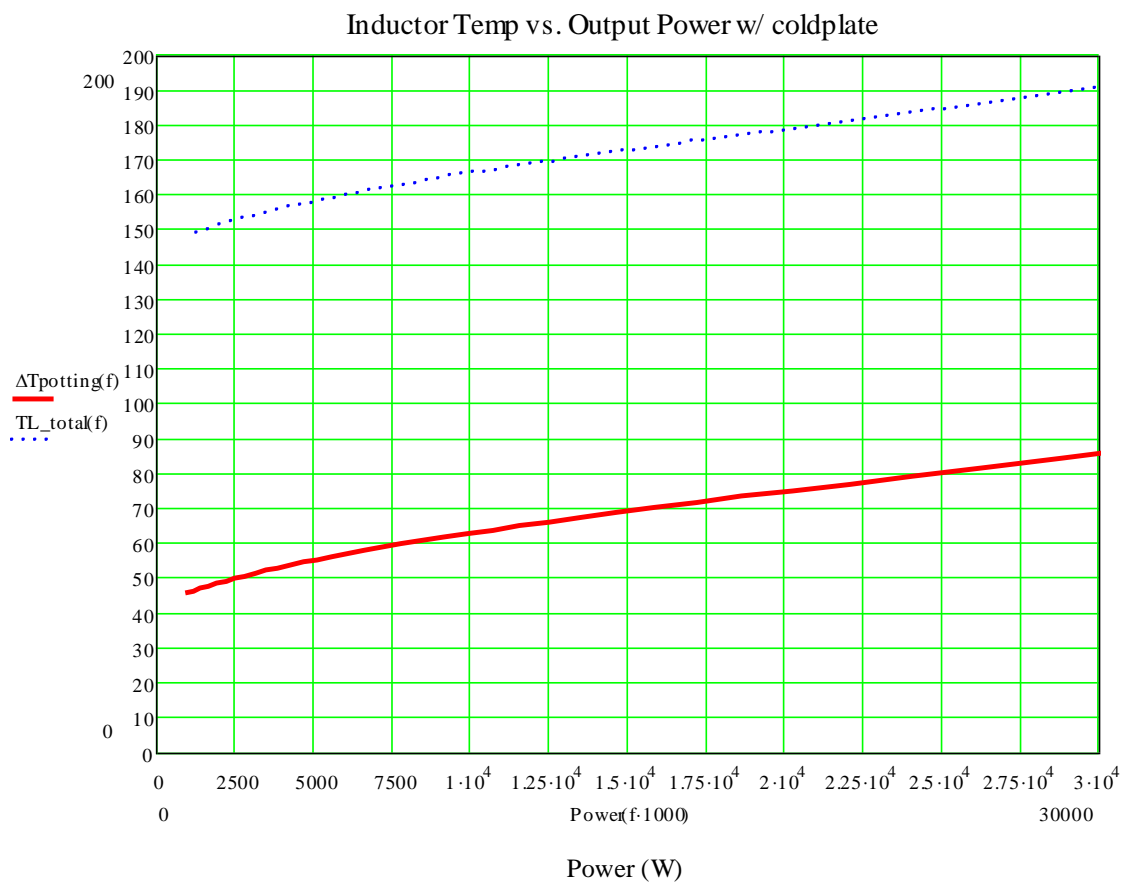
Figure 70 Plot of 32 uH inductor temperature vs. output power

Nanocrystalline Inductor Experimental Results

The inductor cores were manufactured to the specifications provided by a tape-wound core manufacturer, using Finemet FT-3M nanocrystalline material. After the material is wound around a former to create the core, the material is vacuum bonded with an epoxy, resulting in a solid core with a material fill factor of 83%. The cores are then cut to create the gaps, and polished to be sure that the gap surfaces are uniform. The gaps are then shimmed with fiberglass gapping material, and epoxy fused, to create a single core with distributed gaps. As a final process, the inductors are epoxy coated (only the 32 uH was coated) to reduce the risk of shorting from the windings to the core.

The inductors were wound to specification with polyimide cuffed copper foil, with careful care taken not to scratch the thin insulation on the windings. The ends of the copper foil are stripped of tape, tinned with solder, and the two parallel windings are soldered together, then a mounting hole is drilled in the copper. The prototype inductors could then be tested for performance. The prototype 20 uH inductor is shown in Figure 71.

Figure 71 Prototype 20 uH inductor
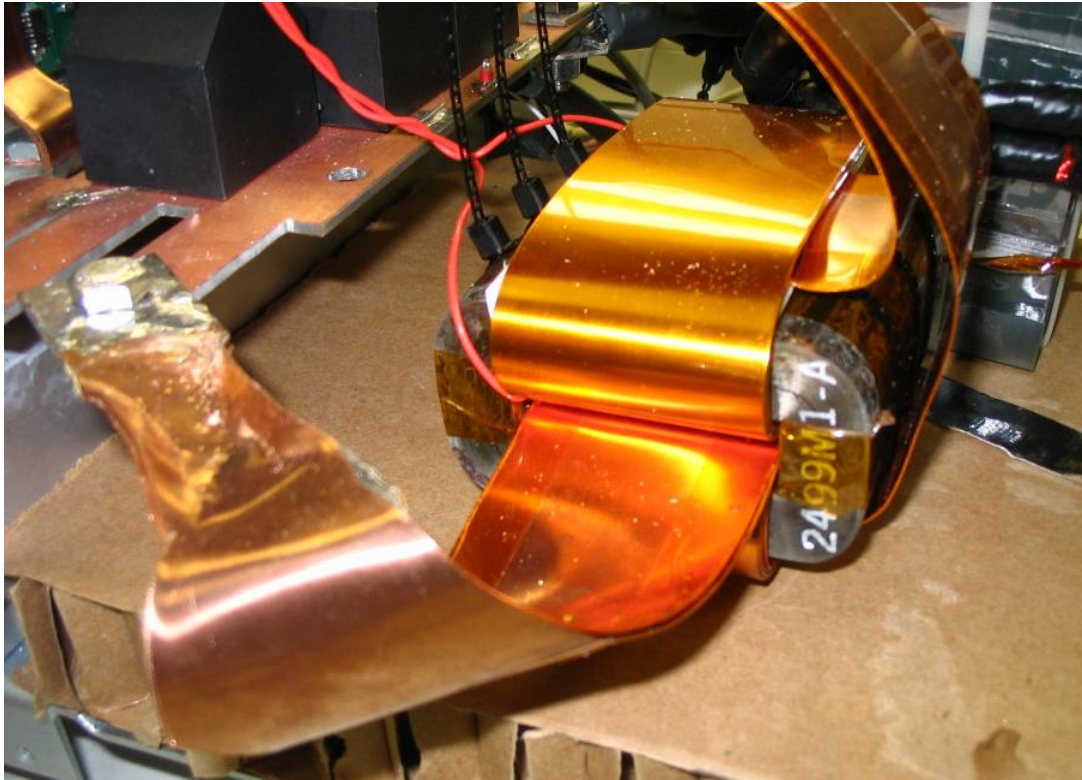
Figure 72 Prototype 20 uH nanocrystalline inductor during testing

The 20 uH inductor was first tested at 9 kW with light air cooling to first verify performance before potting the inductors with epoxy and using liquid cooling, as is shown in Figure 72. The core was found to heat up to 60 °C, which although there is nothing quantifiable to confirm that this temperature corresponds to expected performance, it empirically suggests that the design is generating a reasonable amount of loss. A thermal image of the inductor being tested with air cooling is shown in Figure 74. It can be seen that the hottest part of the inductor is the inner core, where the copper foil is blocking airflow, preventing heat from escaping. The operation of the inductor was as expected and further testing with liquid cooling was warranted.

The improved 32 uH inductor was similarly assembled to the designed specifications. The core was tested, and was found to have reasonable losses, and it exhibited good electrical performance. In a similar manner to the 20 uH inductor, the 32 uH inductor was tested at 10 kW

with forced air cooling, to judge the performance of the core and the design. The air cooled thermal test showed the design to operate as expected, with the maximum temperature of the core approximately 55 ℃, which can be seen in Figure 75. In order to verify the production tolerance, the inductance of each core was measured, and was found to have a variation of +- 2.5%, which is acceptable. This new inductor design is 32uH, has a saturation current of approximately 325A, and a volume of 500 cm^3. This has resulted in a 25% reduction in volume from the 20 uH inductor, an increased power handling capability, and comparable efficiency. The prototype 32 uH inductor can be seen in Figure 73.
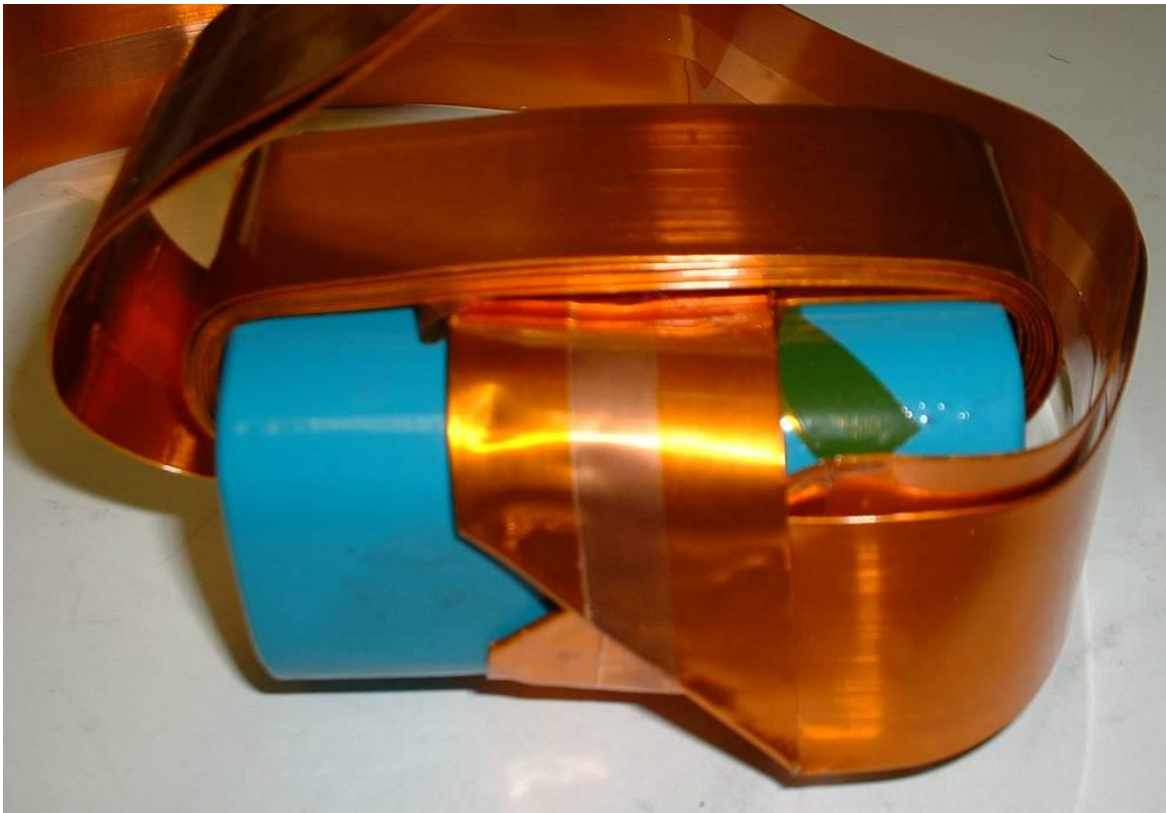
Figure 73: Prototype 32 uH Inductor
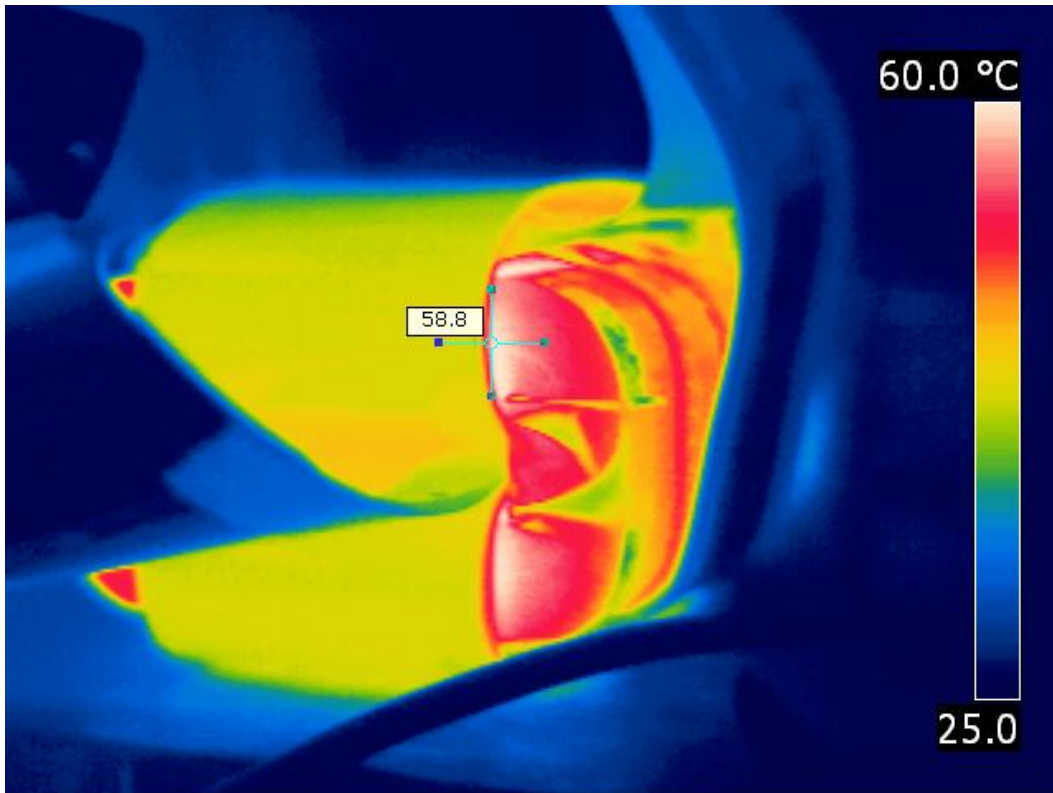
Figure 74 Thermal picture of open air cooled 20 uH inductor at 8.5kW

Figure 75 Thermal picture of open air cooled 32 uH inductor at 10 kW
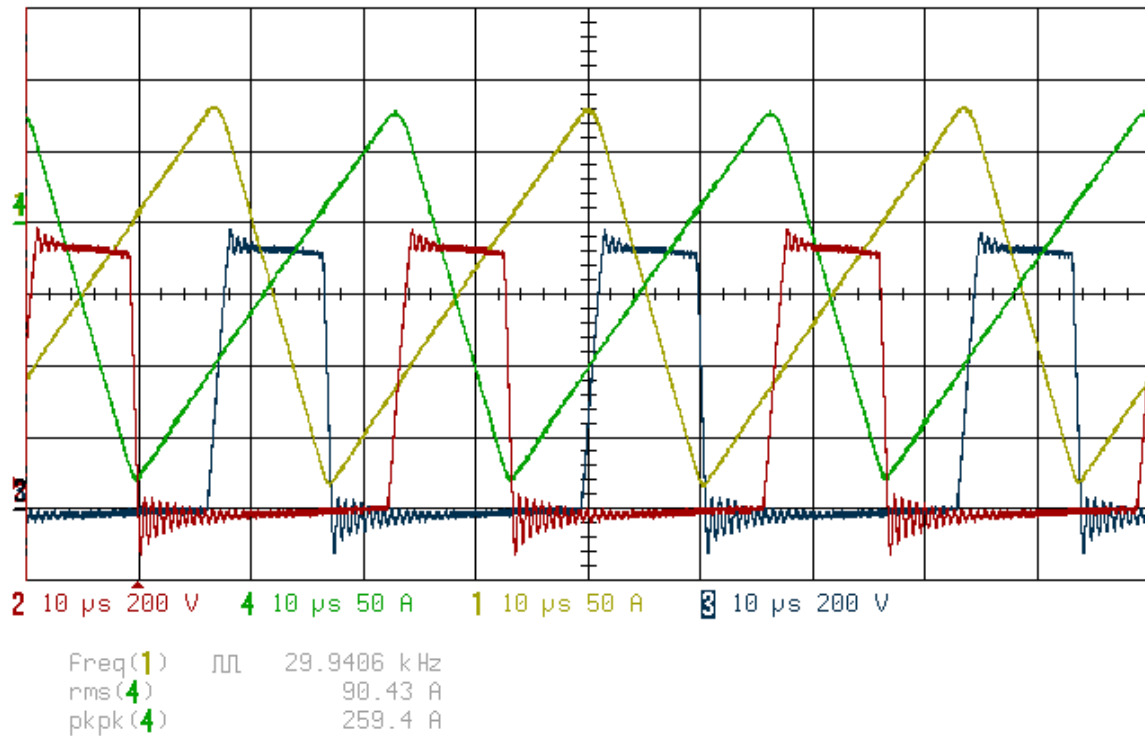
Figure 76 20 kW (10 kW / Inductor) Thermal Test Condition (#1 inductor current A, #2 switch node voltage B, #3 switch node voltage A, #4 inductor current B)

To verify the thermal performance of the inductors in the potting material, the 20 uH inductors were potted in-between the liquid coldplates, and the converter was operated at 20 kW, as the waveform shows in Figure 76. To test the inductor temperature, a thermocouple was embedded in the inside of the core before potting, which allows the measurement of the inductor temperature with the liquid cooling. The results, as shown in Figure 77, showed the temperature rise at the inside of the core. The final temperature rise is approximately 60°C at 70% heat load. Based on the experimentally verified thermal performance, the steady-state inductor temperature is under 185°C with 100°C coolant, which is within the design specs of 200°C. It should also be noted that the thermal capacity of the system is very high, as it took over 1 hour for the inductors to reach steady-state. Due to the long time constants, there is no worry that the inductors will not be able to thermally manage transient conditions of higher power, since this will have little effect

on the core temperature. The inductor designs were found to operate as expected, allowing the

converters to achieve high efficiency and power-density.

Inductor Temperature @ 10kW (70% heat load)
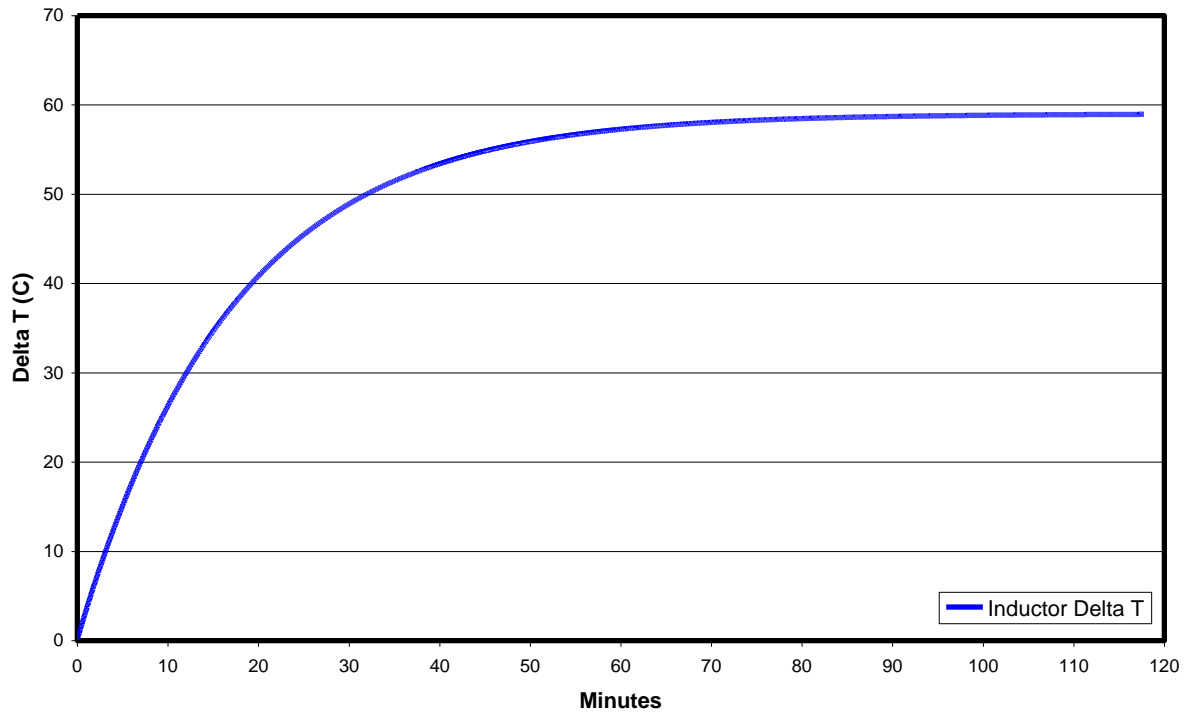
Figure 77 Temperature Rise of 20 uH Inductor @ 0.8 GPM, 12 PSI

CHAPTER 4: EVAPORATIVE SPRAY COOLING DC-DC CONVERTER DESIGN

Two fundamentally different DC-DC converters were developed to evaluate the proposed DC-DC converter system. The first prototype utilized a new evaporative spray cooling approach for cooling the IGBTs of the converter, whereas the second prototype utilized more traditional liquid pin-fin coldplates. The spray cooled converter utilizes specially designed IGBT modules and evaporative spray cooling nozzle arrays, which necessitate a radical converter structure design to optimize efficiency and power density. The design of the evaporative spray cooling converter and experimental results is addressed in this chapter.

Evaporative Spray Cooling

A major goal of this work is to develop a converter which can achieve high power density while using 100°C coolant. To achieve operation at high coolant temperatures, evaporative spray cooling is used opposed to other more traditional coldplate cooling methods. When performing the thermal analysis of a coldplate based system, it is apparent that the thermal impedance from the coolant to the direct bond copper (DBC) ceramic substrate of the IGBT module constitutes a significant portion of the total thermal impedance from coolant to the device junction. Instead of using a liquid coldplate, the baseplate of the IGBT module was windowed to allow for evaporative spray cooling (ESC). The concept of spray cooling is that the coolant will undergo phase change at the surface of the DBC of the IGBT module. Instead of cooling the device by slightly raising the temperature of the cooling liquid, the spray cooled device expells energy through the phase change process, which extracts a high amount of energy. As thoroughly described in [39] and [40], the spray cooling interface has a very low themal impedance above the 107°C boiling temperature of the cooling medium, 50/50 ethylene glycol

water (EGW). The spray cooling technique effectivly limits the surface temperature of the DBC to a few degrees higher than the boiling point of the cooling medium. To achieve this goal, custom IGBT modules must be designed, which have sealed windows in the baseplate, allowing the coolant to boil directly on the surface of the DBC, as shown in Figure 78.
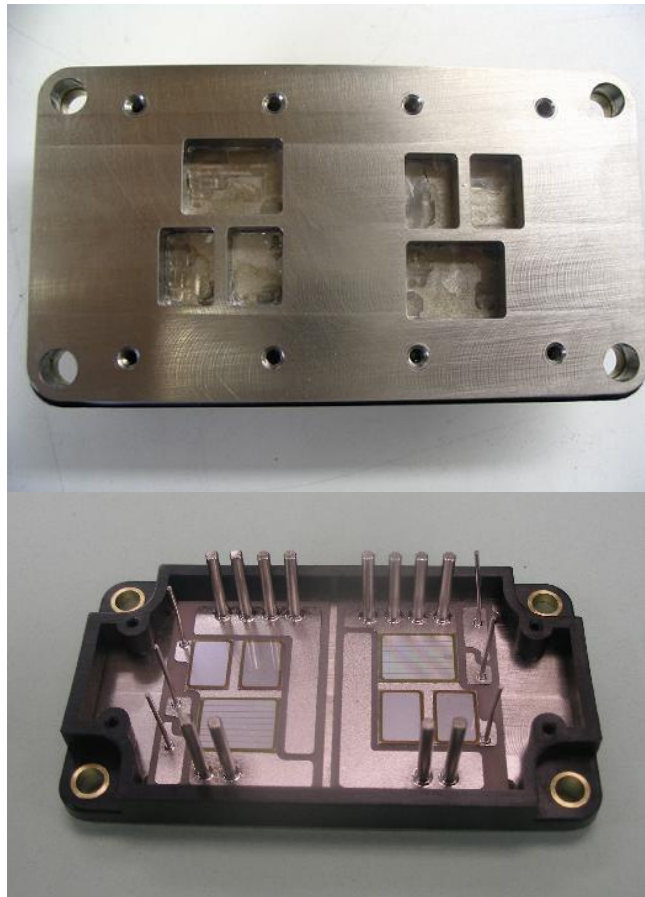
Figure 78 Custom IGBT with windows for spray cooling

The specific goals of this work was not to develop or optmize the spray cooling approach, as this is a very different field than that of the power electronics topology, control, and system design work presented in this dissertation. The ESC is used as a tool to enable high power-density, which is utilized in full effect to achieve a converter which exhbits very high performance in all metrics, including high coolant temperature operation. In consideration of the benefits of ESC, there are some specific challenges which must be addressed when

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implememnting the cooling method for vehicular applications. The ESC design assumes that the outlet pressure of the ESC nozzle array is atmospheric pressure, which will result in 50/50 ethylene glycol - water (EGW) mixture boiling at 107 ºC. Due to the extreemly low thermal impedance at the phase change interface, it can be considered that the DCB baseplate is "locked in" at a temperture just above 107 ºC, allowing the temperature differntial between the IGBT die and the coolant system to be distributed as a gradiant through the various bonding layers of the IGBT module. The goal is to achieve a maximum die temperture less than 140 ºC, as this will result in good long-term reliability for the IGBT die, which is rated for a maximum temperature of 150 ºC. In order to mainain the designed specifications, it is crital that the exhaust pressure remain at atmospheric pressure, otherwise, the boiling temperature of the 50/50 EGW will quickly rise to a level which will damage the IGBT.

To complement the numerous advantages of ESC, there are some specific drawbacks. Currently, vehicle cooling systems utilize the increased boiling temperature of coolant at higher pressure as a tool to prevent boiling in the system, which is fundamentally opposite from the goal of ESC. An increase in coolant pressure of 12 psi will increase the boiling temperature of 50/50 EGW to 126 ºC, with a coolant pressure of 24 psi raising the boiling temperature to 138 ºC. It is apparent that there is no tolerance in the deisgn for higher coolant exhaust pressure, which presents the challenge that coolant systems intending to use ESC must be carefully designed to ensure that the exhaust pressure is atmospheric.

The baseplate of the module is designed with open windowes beneath the semiconductor dies, which allows for direct evaporative spray cooling. The accompanying evaporative spray cooling nozzle assembly was developed in cooperation with Rini Corporation, and is shown in Figure 79. Further explaination of the evaoprative spray cooling has been explained by Mertens,

et. al. (2007). Unlike traditional coldplate approaches, the effective thermal impedance between the coolant and the IGBT die is non-linear, depending on the heat flux. This is since the coolant will boil at 107 ℃, no matter what the coolant temperature is, so in some cases, the thermal impedance of the cooling approach might seem high, yet, with higher coolant temperature, the effective thermal impedance will decrease, resulting in similar IGBT die temperatures. This is in contrast to liquid coldplates, where the impedance between the coolant and the IGBT die is relativly constant, resulting in double the ΔT when the power dissipation doubles. As can be seen from Figure 80, roughly doubling the power dissipation only increased the ΔT between the cooland and the IGBT by 60%.

Even with the lower thermal impedance spray cooling technique, the losses still must remain low to maintain IGBT operating temperatures below the nominal operating temperature, which is why the soft-switching topology is still critical.

Figure 79 Evaporative Spray Cooling Nozzle Assembly

**2-Module IGBT Temperature Rise vs. Output Power
w/ 95°C Coolant**
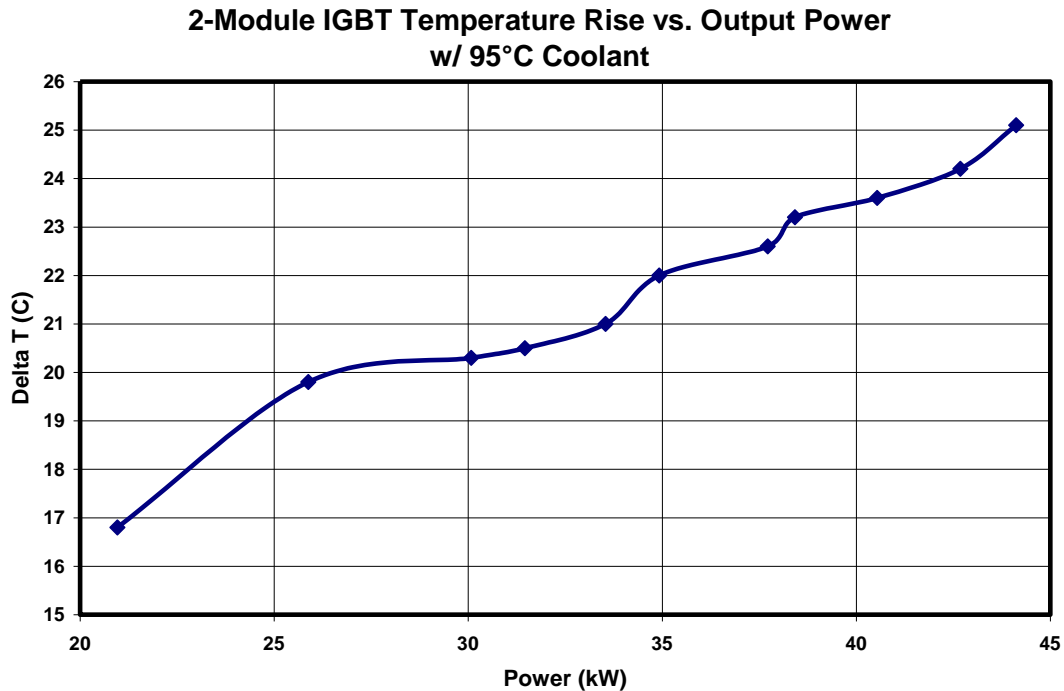
Figure 80 IGBT die temperature rise vs. output power

Custom ESC IGBT Module Design

In order to achieve high power-density with high coolant temperatures, there are two ways to improve performance. The first way is to simply decrease the IGBT losses, which will then decrease the necessary cooling power, and decrease the overall temperature of the device. The second improvement is to utilize a better cooling method with lower thermal impedance, which can cool the device at higher coolant temperatures. In order to achieve this, a new device package was designed in cooperation with Powerex. The new device was designed with both goals in mind. The semiconductor configuration is in a manner to decrease parasitic elements of the package. The package also features a special base plate which has windows cut-out under the semiconductors, which will allow the use of evaporative spray cooling. The configuration of the semiconductors is shown in Figure 81. Advantages of the new packaging approach include:

- Lower parasitic inductance

- Lower voltage overshoot

- Ultra-fast switching transients

- Improved efficiency

- Lower EMI

- Direct solder pins, including dedicated collector-emitter sense pins

- Higher silicon density

- Spray cooling w/ lower thermal impedance

The module configuration is a single switching leg, with two NFH series fast 200A IGBT dies, and each IGBT has two 100A ultra-fast antiparallel diodes. The module uses high-current direct-solder pins for both the power and control connections, which serves to reduce the paracitic inductance in the path between the snubber capacitors and the IGBT dies, helping to further reduce switching losses. The module assembly process is similar to that of traditional IGBT modules, except there are no bond wires betwen the power and signal connections and the device conduction paths, serving to reduce paracitic inductance and increase efficiency, especially at high switching frequency. The module is configured with two IGBT/diode pairs to create a single phase leg, where each IGBT/diode pair is bonded to a single DBC ceramic plate. Each DBC plate is solder bonded to the special baseplate, which is windowed to allow for evaporative spray cooling. Each baseplate has threaded mouning holes, which will allow the ESC cooling nozzle array to attach.
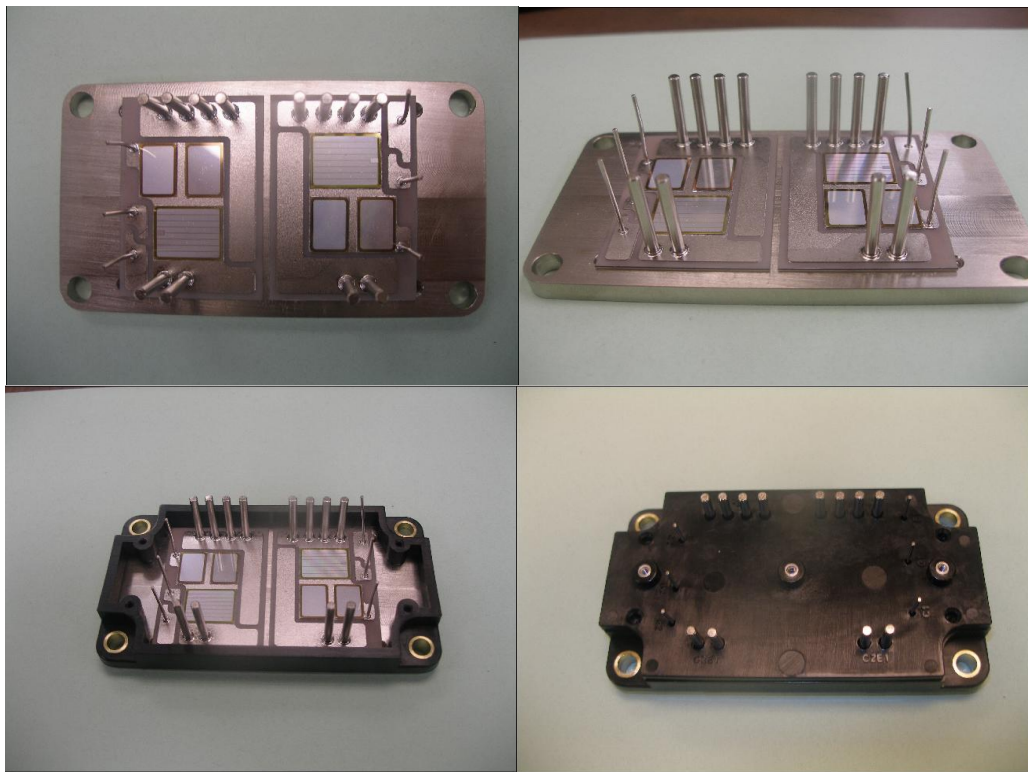
Figure 81 Custom Packaged IGBT Module
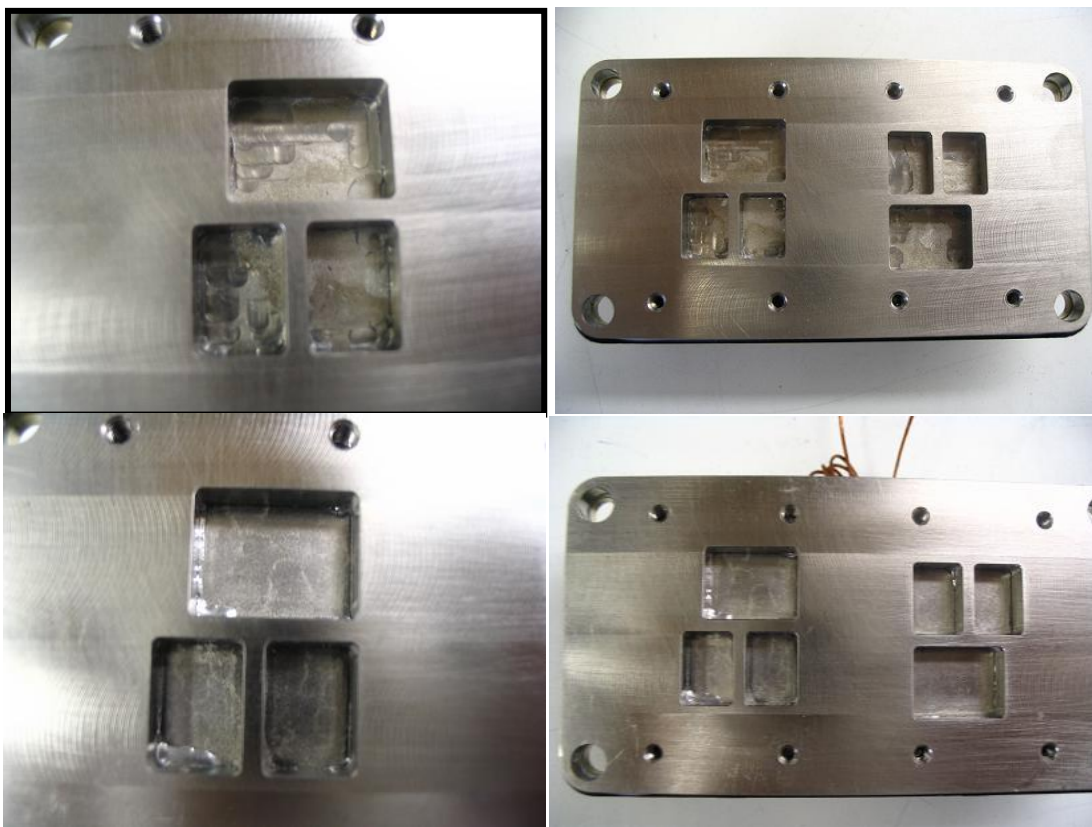
Figure 82 Windowed Baseplate for Custom Modules

Before testing with the custom IGBTs, an off-the-shelf IGBT from the same Powerex NFH series was tested using a forced air cooling heat sink was used in order to make sure that the basic converter operation is as expected, and that all the other components can handle the current stresses (input & output capacitors, snubber capacitors). To verify the thermal performance of the off-the-shelf IGBT module with air cooling, the measurements in Table 7 were performed by operating the device in the linear region to dissipate power, and measure the base plate temperature. It is apparent that the air-cooled testing prototype can only dissipate enough power to operate at approximately 12 kW of power per module. To prove the need for ESC, a test was performed to determine the maximum performance of the off-the-shelf NFH IGBT using available liquid cooling technology. The IGBT module was tested using the off-the-shelf IGBT CM150DU-24NFH with an attached micro-channel water cooled coldplate as shown in Figure 83. The thermal resistance of that setup was determined (Table 8) and then compared to the setup with the forced air cooling. The result was that the liquid cooled IGBT could potentially process approximately 16.5kW maximum using the off-the-shelf IGBT and the cooling with the cold plate. This test proves the necessity to investigate a higher performance cooling methods.

Table 7 Thermal Measurements for off-the-shelf IGBT with Forced Air cooling and Heat Sink

V IGBT (V)	I IGBT (A)	P IGBT (W)	T Diode high (°C)	T IGBT high (°C)	T Diode low (°C)	T IGBT low (°C)	T ambient (°C)	R_{th} HS
15.2	2.32	35.3	28.9	29.1	30.2	31.1	25.4	0.16
23.2	3.44	79.8	32.7	33	35.3	37.2	26	0.14
26	4.6	119.6	37.2	38	41.4	44.8	26.5	0.15
28.3	5.57	157.6	42	43.1	48	52.6	27.4	0.16
30.5	6.22	189.7	45.4	46.8	51.8	58.2	27.7	0.16
33	7.1	234.3	50.1	52	57.9	66.3	28.3	0.16
35	8	280	54.7	56.6	63.7	73.3	29	0.16
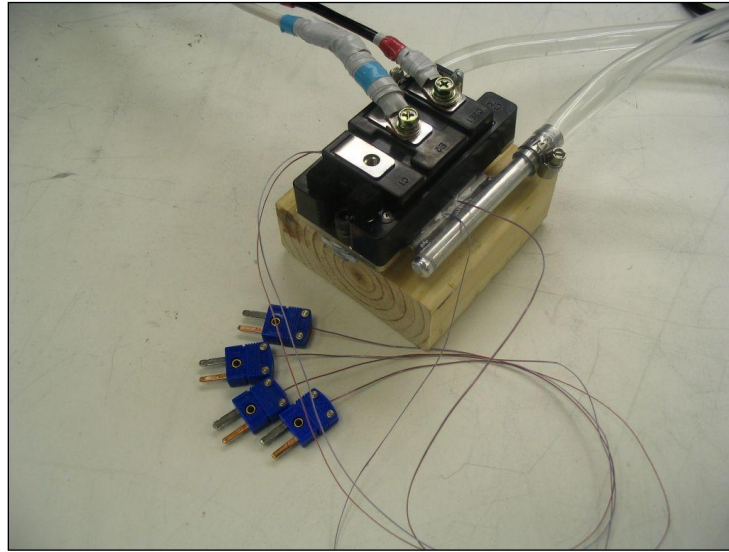
Figure 83 Setup of IGBT and Micro-channels Cold Plate

Table 8 Thermal Measurements for off-the-shelf IGBT with Micro-Channel Water Cooling

P IGBT (W)	T Diode high (°C)	T IGBT high (°C)	T Diode low (°C)	T IGBT low (°C)	T ambient (°C)	R_{th} HS
80	26.6	27.2	33.2	32.8	24	0.11
161	30.1	31.1	42	43.3	24	0.12
234	33.5	34.8	49.3	52.7	24	0.12

After the method of thermal impedance estimation was verified, the custom water-cooled nozzles (none-spray) with custom IGBT (see Figure 84) were tested. The value for the thermal resistance of the device as designed was confirmed in this measurement. So in terms of thermal performance the converter setup using the custom IGBT's with the water cooling should be able to reach 20kW.
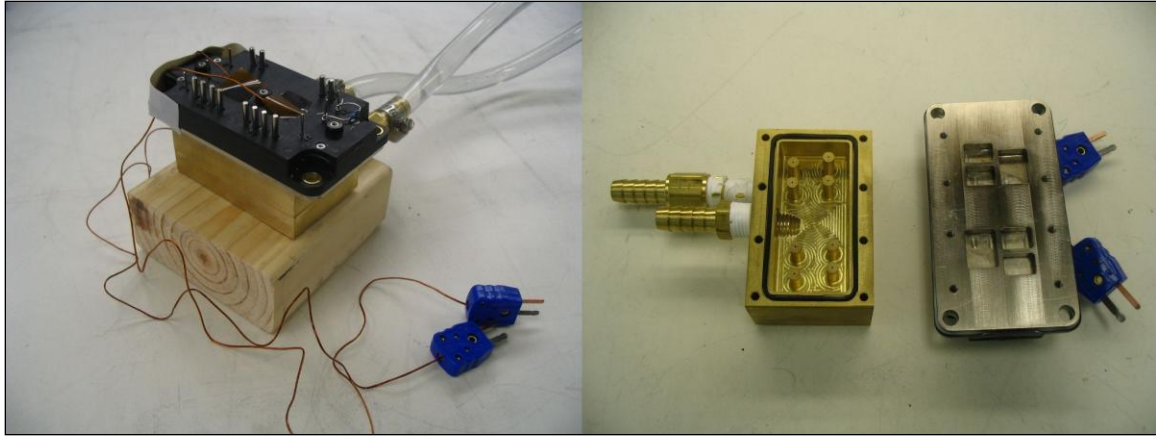
Figure 84 Water cooling & custom IGBT

Figure 85 shows the case temperature of an attached component with different heat fluxes using a water temperature of 25°C.
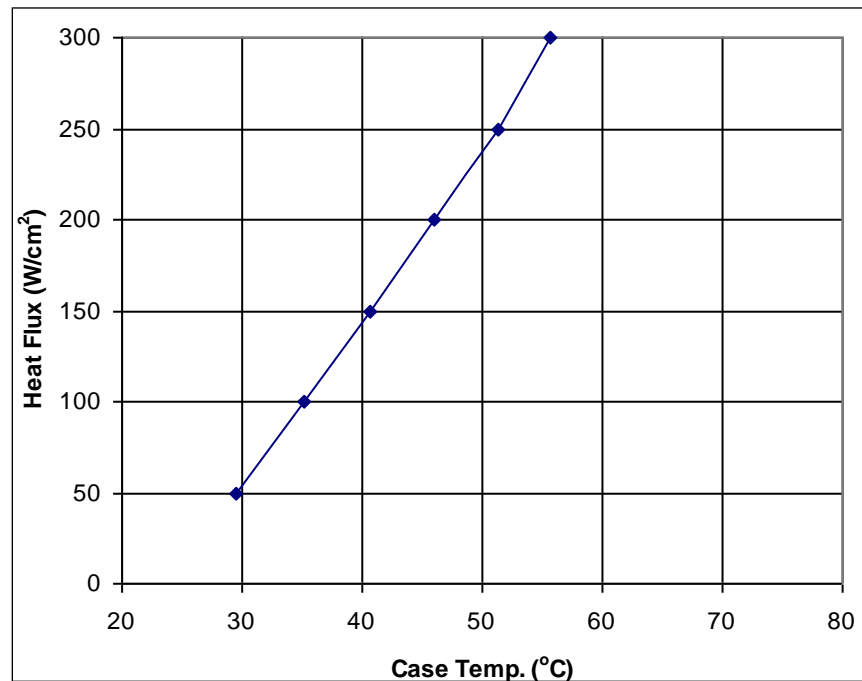
Figure 85 Performance of the water-cooling setup with 25ºC coolant

The custom IGBT package also has 2 thermocouples where each of them is sitting in the middle of the IGBT- and the 2 diodes dies. But in any mode of operation of the converter either

the IGBT or the diodes will contribute to the temperature increase, for example in boost mode it will be the low-side IGBT and the high-side diodes. When the custom IGBT's are operated in the converter, the temperature readings of the thermocouples give a rough idea about the actual die temperatures of both the IGBT and the diodes, but not the actual die temperature. It can be seen from Figure 86 how much less the temperature readings of the thermocouples will be compared to the junction temperature for different heat fluxes. For example, when the converter is operated with an estimated heat flux of the IGBT of 200W/cm^2 and it is expected to operate the junction below 125°C then the thermocouple's reading should be less than around 115°C (10°C less) in order to ensure safe operation of the converter.
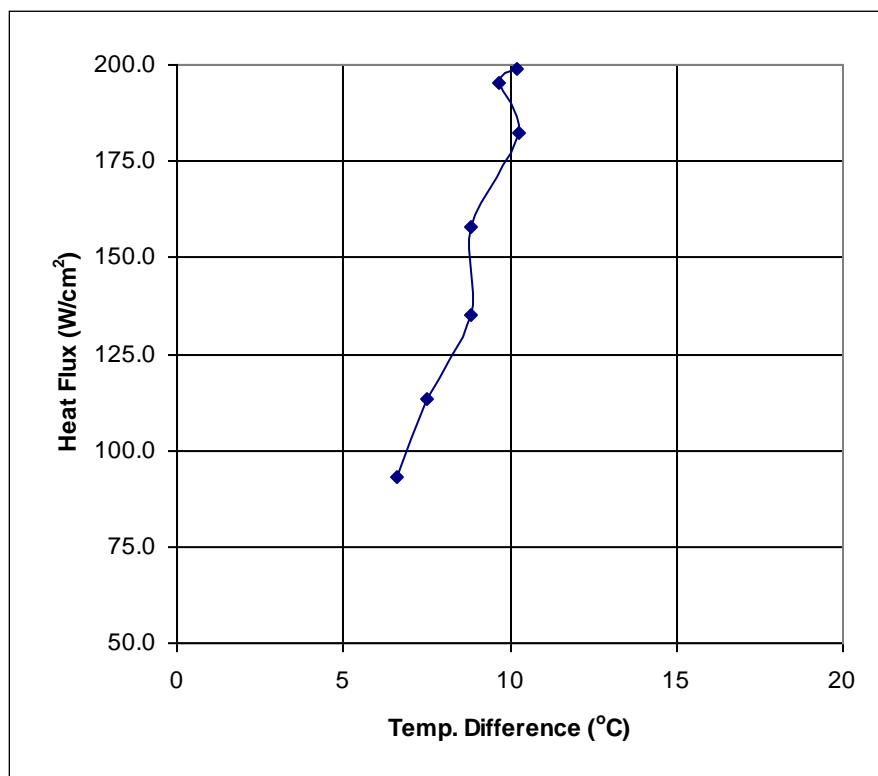
Figure 86 Estimates on the performance of the thermocouples in the custom IGBT

The expected heat loads are shown in Figure 87. The only substantially high heat flux is the 250 W/cm^2 load on one of the IGBT's during boost mode. With the various devices experiencing different heat fluxes, the possibility of using different nozzle designs was explored. The differences between the nozzle designs consisted of only minor variations in geometric features which yield different flow rates of spray liquid for the same ΔP. Hence, low flow rates of liquid can be used in the lower flux devices while the higher flux IGBT gets more liquid. This gives an economical use of the liquid supplied to the module, with more liquid going where it's needed and less liquid where there can afford to be less.

q"= 150   q"= 120

q"= 250 W/cm^2 q"= 100
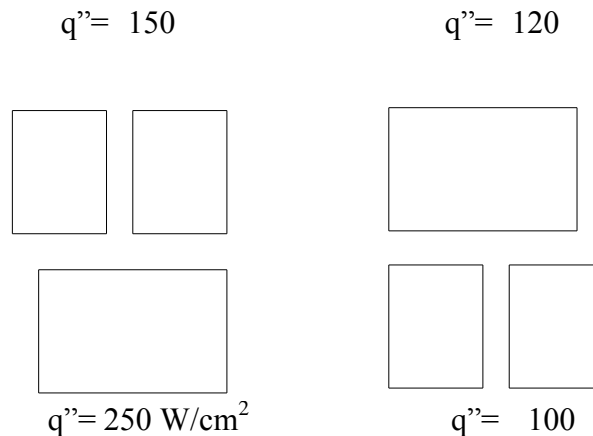
Figure 87 Heat fluxes (W/ cm^2) used during design of spray cooling module

In cooling the power electronics, a key consideration is the thermal budget that is available for heat transfer. This is diagramed in the thermal budget diagram in Figure 88. Any means of boiling heat transfer must work within the gap between the liquid's saturation (boiling) temperature and the junction temperature of the chips. However, due to the thermal resistance of the chips, the ΔT through the chips increases quickly with heat flux. This results in most of the ΔT between the 135 ^{o}C junction temperature and the boiling temperature of the liquid being due to thermal conduction through the devices and only a portion due to spray cooling. The ambient air condition of 50 ^{o}C represents the maximum ambient temperature that a vehicle is likely to

encounter, although this is not of consequence of the ESC development, as the vehicular cooling system is responsible for supplying the 100°C coolant however the designer sees fit.

$q"_{IGBT}= 225$ W/cm^2
$T_{junction}= 135$ °C

ΔT internal to IGBTs

$T_{case}= 115$ °C

$T_{sat}= 107$ °C

$q"_{IGBT}= 150$ W/cm^2
$T_{junction}= 125$ °C

ΔT internal to IGBTs

$T_{case}= 112$ °C

ΔT of spray cooling

$T_{sat}= 107$ °C

ΔT of spray cooling

ΔT for heat rejection to ambient air

ΔT for heat rejection to ambient air

$T_{air}= 50$ °C

$T_{air}= 50$ °C
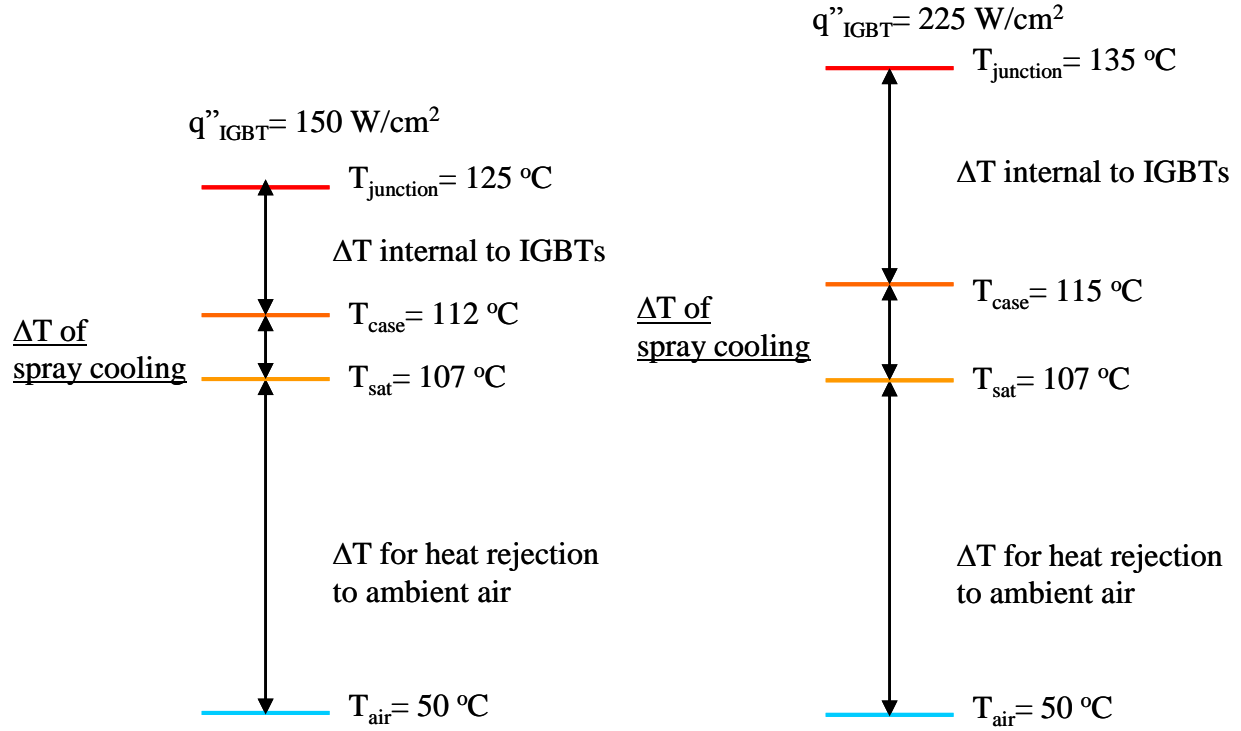
Figure 88 Thermal budget for spray cooling of vehicle power electronics

Experimental Topology Testing and Verification

To achieve initial verification of the control methodology and the topology, high-power testing was done in boost mode using the setup as shown in Figure 89 and a custom IGBT with water cooling. The tests were run with 200V input voltage and an output voltage 700V. The results can be seen in Table 9 and are graphed in Figure 90. With 200V input voltage the converter was tested the converter up to an output power level of about 17.3kW. The switching waveforms under that condition are displayed in Figure 91.

When testing it was desirable to be able to measure the current through the IGBT, in a goal of visualizing the soft-switching behavior, as well as to attempt to estimate the losses of

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each switching device. In order to do this a current probe needed to be clamped into the current path of the custom IGBT. In doing so the snubber capacitors were moved further away from the IGBT's which increased the inductance and therefore increased switching losses. The additional ringing due to that extra inductance significantly increased the turn-off losses, as can be see in Figure 91, where the first spike in the waveform is the instantaneous power. The next step was to place the snubber capacitors closer to the switch node in order to create a more optimal design and record the new efficiency. Once the new efficiency was recorded and compared to that of the previous efficiency, a more accurate idea of the power loss in the custom IGBT and a more accurate heat flux was achieved.
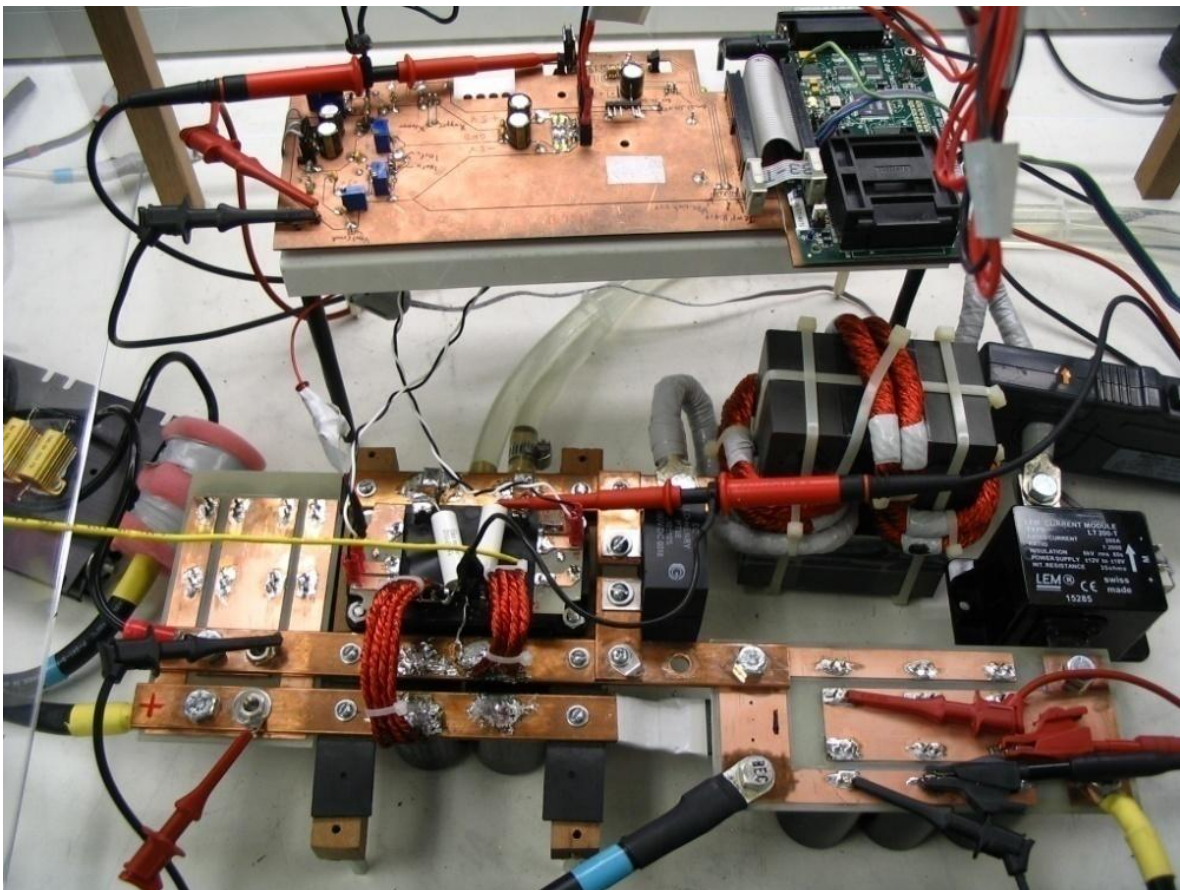
Figure 89 Initial high-power testing setup w/ custom IGBT's and wires for IGBT current sense

Table 9 Initial efficiency measurements with parasitic current sense wires

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (kW)	Pout (kW)	Efficiency (%)
199.2	10.67	726.2	2.67	2.1255	1.939	91.2
199.1	14.8	704	3.9	2.9467	2.7456	93.2
199	19.47	701	5.18	3.8745	3.6312	93.7
199.6	28.5	697.3	7.76	5.6886	5.411	95.1
199.4	38.4	702	10.43	7.657	7.3219	95.6
199.3	47.93	701.8	13.03	9.5524	9.1445	95.7
199.5	57.25	700.6	15.61	11.421	10.936	95.8
199.3	67.3	702.3	18.26	13.413	12.824	95.6
199.3	76.55	701	20.76	15.256	14.553	95.4
199.6	86.7	701	23.41	17.305	16.41	94.8
199.7	91.8	702	24.74	18.333	17.368	94.7
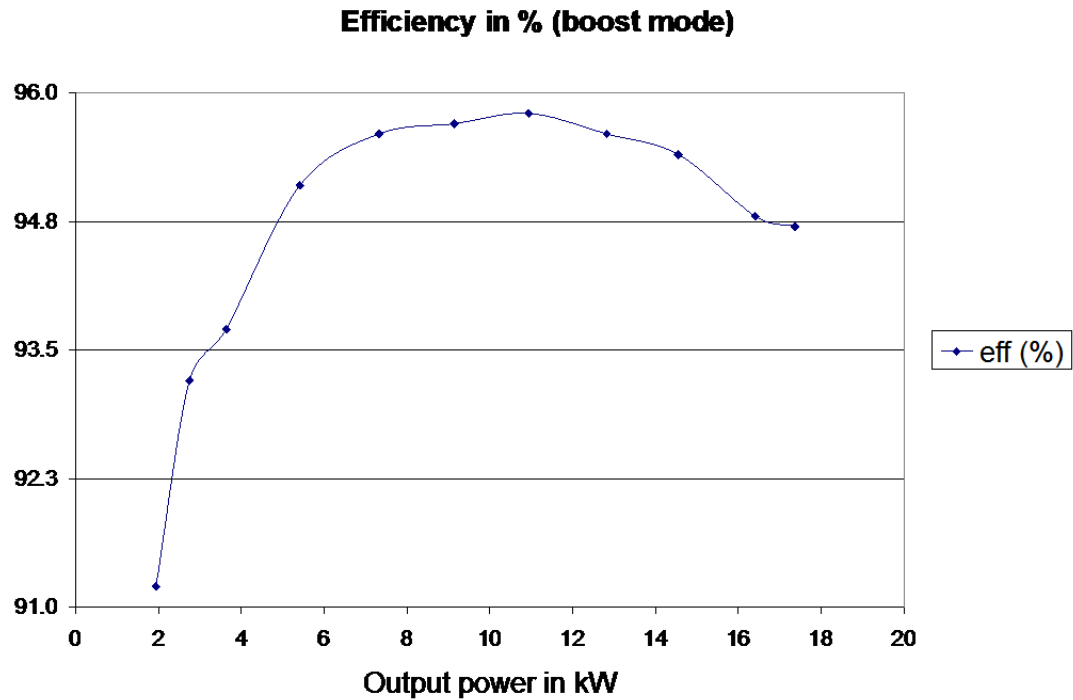
Figure 90: Efficiency of initial testing with custom IGBT module
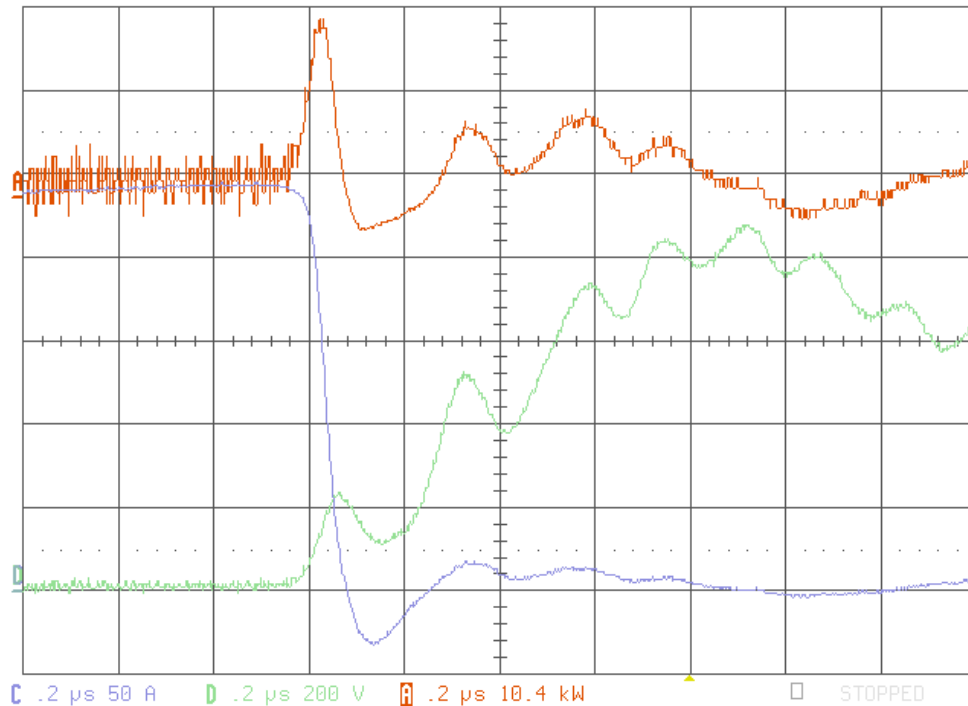
Figure 91 Switching waveforms: switch node (#D), low-side IGBT current (#C), instantaneous power

(#A) @ 200V & 17.3kW

In Figure 91 the orange waveform (#A) is the instantaneous power that is being dissipated by the custom IGBT. In order to determine the losses in the IGBT, the current and voltage across the device must be measured before the snubber capacitors. Fundamentally, there is a problem with trying to measure the switching losses in this soft switching topology. Since we must measure the current before the snubber capacitors, we must add in some distance with wires between the snubbers and the IGBT for current sensing. By adding longer wires between the snubber and the IGBT, we have also added parasitic inductance in the loop, which will result in higher switching losses. The first spike that is seen represents the turn-off loss, and is probably worse than expected due to the increase in inductance from current sensing. The turn-off losses will be reduced when the snubber capacitors are placed closer to the switch node on the custom IGBT and the connection leads from the emitter of the custom IGBT to the bus bar

are shortened, as shown in Figure 92. Also, the ringing on the switch node that is seen will be reduced for the same reason. By decreasing losses and increasing efficiency, more accurate heat flux and efficiency measurements are available, but without the ability to visualize the switching behavior.
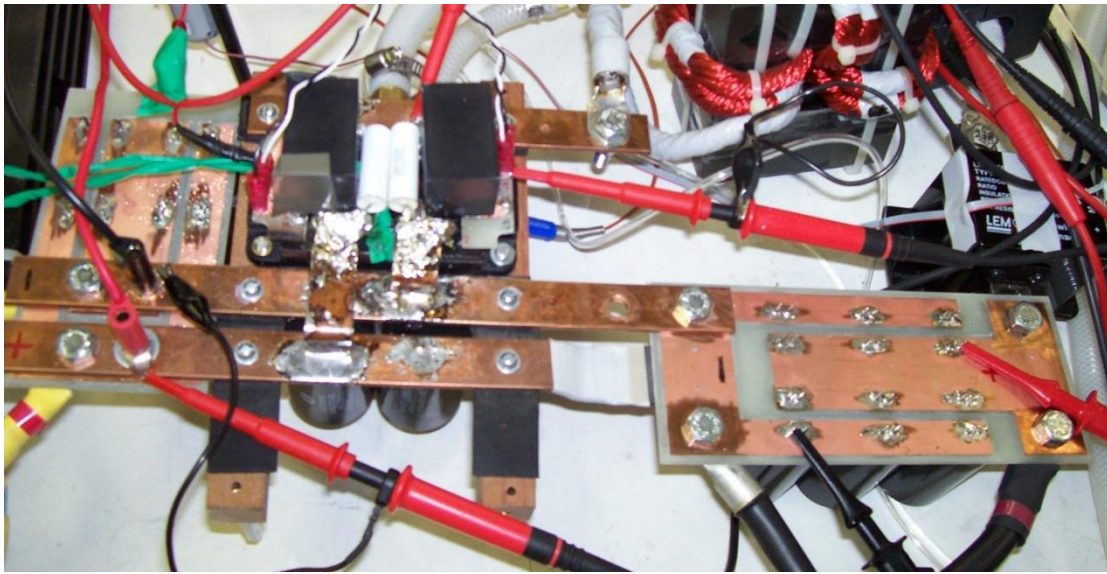
Figure 92 Prototype #2 w/ Snubber Capacitors Directly on IGBT

Efficiency of Boost (200V-700V)
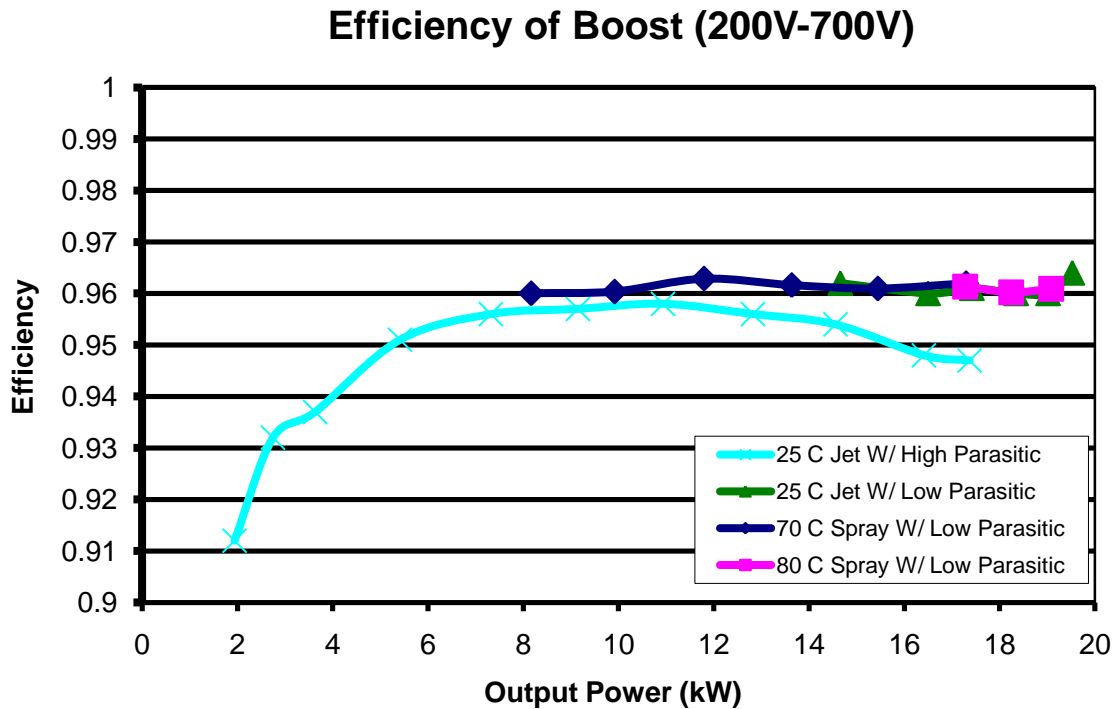
Figure 93 Efficiency Comparison of Single Boost DC-DC Converter

As expected, the efficiency was found to be greater once the parasitic elements of the current sensing loop were removed from the snubber capacitor circuit, as can be seen in Figure 93. The peak efficiency exceeds 96%, with is an increase of over 1% at higher power. Ideally, the snubber capacitor would connect directly across the IGBT die, but since there is necessary distance for leads and connections, it is impossible to have the completely ideal case. The final prototype will be designed to use new custom snubber capacitors, which are flat silvered mica foil capacitors. The new capacitors should have even lower parasitic elements, allowing the efficiency to be even greater. The switching waveforms of the prototype with high parasitic snubber inductance and lower parasitic snubber inductance can be seen in Figure 94 and Figure 95. It is very apparent that the reduced inductance in the snubber circuit has a major effect on the ringing in the system.
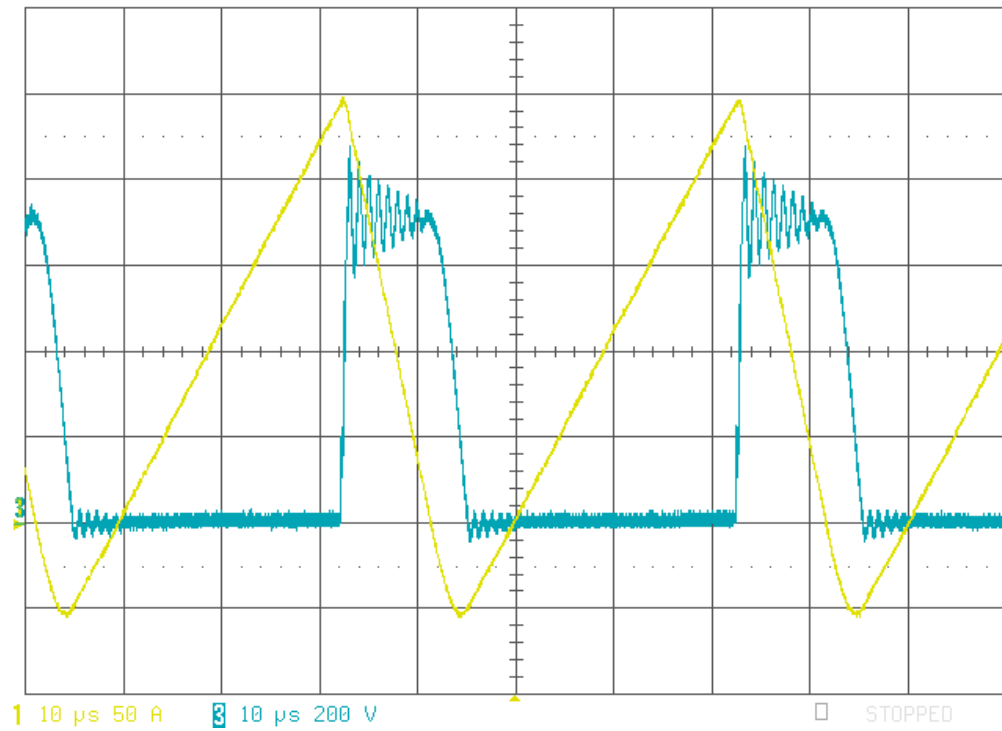
Figure 94 Inductor current waveform (1) and IGBT switch node (3) w/ parasitic wire connections
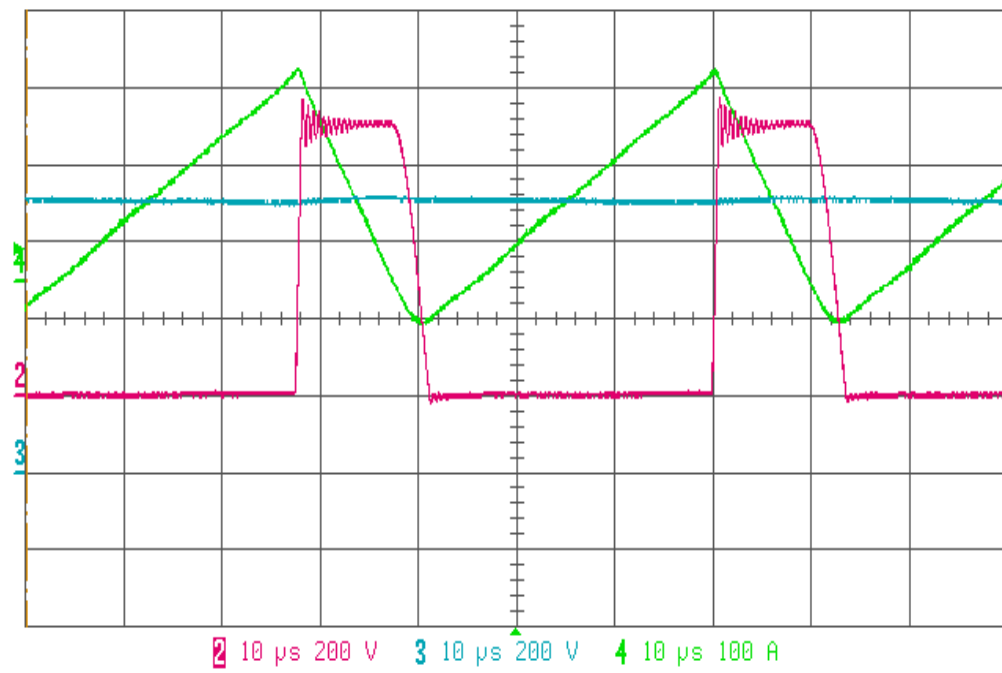
Figure 95 Inductor current waveform (4) and IGBT switch node (2) w/ snubber directly on IGBT

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Comparing the waveforms between the higher and lower snubber parasitic inductance prototypes show that the parasitic ringing has been greatly reduced, which is why there is an increase in efficiency. It is expected that the efficiency will increase even more when the custom snubber capacitors are used, since they have very low parasitic inductance, as well as low equivalent series resistance (ESR).

Low efficiency is very critical for this design, as efficiency directly correlates to generated heat which must be dealt with. Based on the initial efficiency results, it is clear that the converter will meet the objective efficiency of 96%, with the potential for even higher efficiency as the design is refined. Since such high cooling temperature is required for this converter, the design will be pushing the limits of the system as we approach full power. It is estimated that every .1% increase in efficiency could result in a reduction in the IGBT die temperature by up to 0.75 °C, which is very important when we are pushing the devices so close to the limit of 150 °C.

Silvered Mica Snubber Capacitors

The snubber capacitor is critical to the soft-switching operation of the converter. The performance of the converter is highly dependent on the characteristics of the snubber capacitors, including the series parasitic inductance and resistance, the linearity of the capacitance over a wide temperature range, and the long-term reliability of the capacitor. Commonly, snubber capacitor for EV applications are comprised of polypropylene or other similar film dielectrics, which are valued for their high current handling capability, low parasitic inductance and resistance, and relatively high density. The limitation for these capacitors is the allowable operating temperature, which is typically limited to 105ºC. In this application, since the cooling liquid can already exceed 100ºC, it is not feasible to use traditional film snubber capacitors,

considering the expected self-heating of the device will raise the temperature well over 120ºC. Another issue is the tolerance and linearity of the capacitance between devices and across wide temperature variations. Since the soft-switching scheme depends highly on the resonant behavior of the converter, the controller is designed to operate with capacitors that are within a reasonable tolerance, and thus, any capacitor solution should ideally be within about 10% of the nominal capacitance value across temperature and manufacturing variations.

The solution to the need for high reliability snubber capacitors exhibiting very high performance was solved by using specialized silvered mica capacitors. The capacitors were developed to optimize high-temperature performance, as well as to minimize the series parasitic inductance and capacitance. Unlike cylindrically wound film capacitors, the custom snubber capacitors are assembled as a parallel plate capacitor, with alternating copper foil conductors and silvered mica dielectric. The entire assembly can be fine-tuned for capacitance, as the amount of capacitance can be easily modified by adding or removing capacitor layers before the conductors are solder fused. The silvered mica capacitors can withstand operation at well over 150ºC, and exhibit very linear capacitance over the wide expected operation temperature range from -40ºC to 150ºC. Furthermore, the overall efficiency benefits from the use of very low loss snubber capacitors, whose high performance also serves to further decrease the IGBT switching loss in comparison to capacitors with higher parasitic inductance and resistance. The structure of the snubber capacitor is shown in Figure 96.
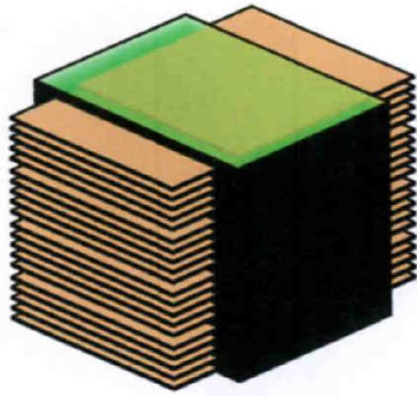
Figure 96 Custom Silvered Mica Snubber Capacitor

The capacitors must have very good temperature tolerance, meaning that the capacitance must not vary at high temperature, since the capacitance value is critical for proper soft switching operation. The capacitors also must be capable of operating at high temperature without damage, since the capacitors will self heat from the current ripple, and their temperature will rise even higher than the already high ambient temperature of the converter. In the second prototype, we use Electronic Concepts low inductance polypropylene snubber capacitors. These capacitors are acceptable for testing at normal ambient temperature, but they are not capable of operating above 105°C. Considering that the leads are directly connected to the leads of the IGBT module, and the IGBT die will be operating up to 135°C or more, the snubber capacitor may go to very high temperatures (150°C), which would be detrimental for most available snubber capacitors.
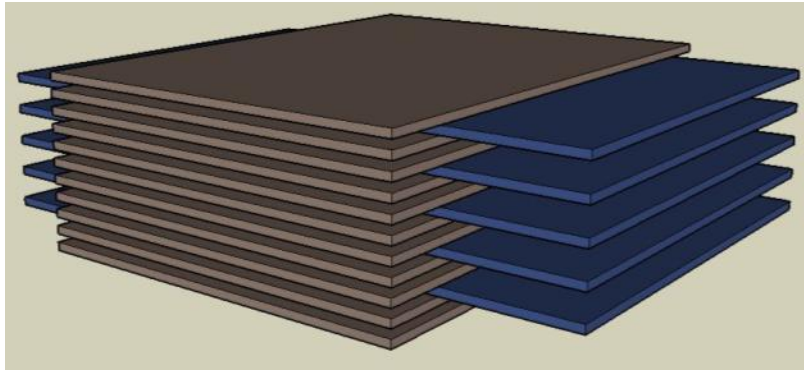
Figure 97 Construction of Custom Capacitors
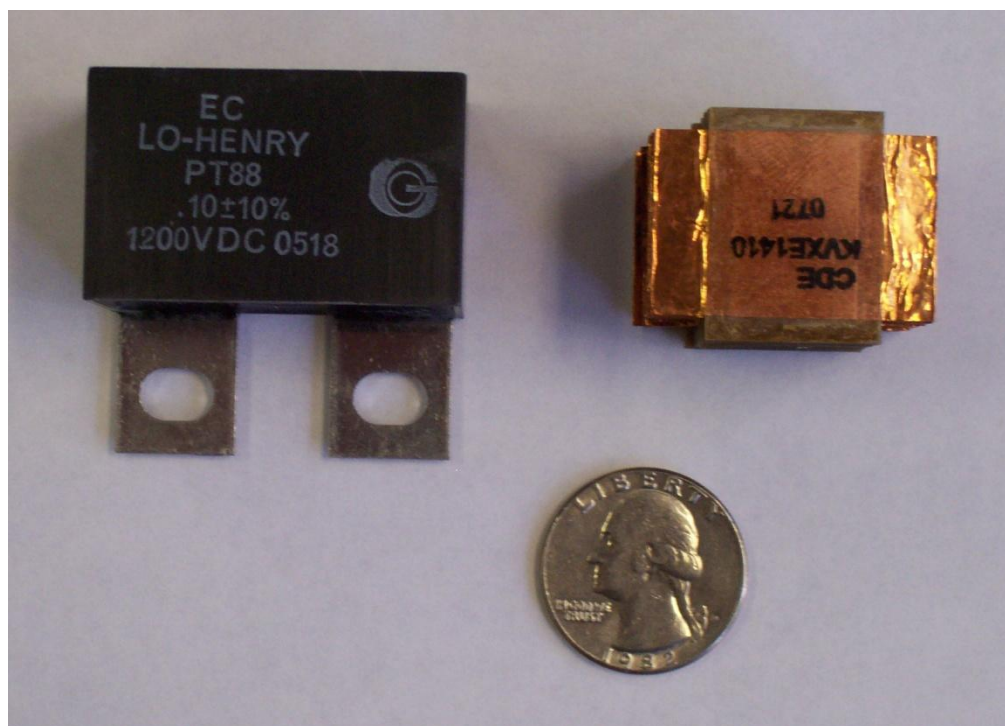
Figure 98 Top view of the Custom Snubber Capacitors vs. off-the-shelf Snubber

For the capacitor design, the individual custom silvered mica capacitors were designed to fit between the power pins of the IGBT module. These capacitors, which were manufactured to specification by CED, are constructed using silver impregnated mica, which will allow for very high operating temperatures as well as high ripple current. Many capacitor types are capable of high operating temperature, such as ceramic, but the problem is that the capacitance is not very

linear with temperature. For this application, the proper soft switching resonance requires the snubber capacitance to remain constant over the entire operating range. The silvered-mica capacitors remain very linear across the operating temperature range.

The current ripple that the capacitor experiences is very high which necessitates a capacitor that has a low equivalent series resistance (ESR). While the exact value of the new custom capacitor's ESR is currently unknown since it is difficult to measure with such a low ESR device, it is expected to be very low, since the construction of the capacitor is actually many layers of copper foil and the mica dielectric. With the equivalent of many capacitors in parallel, each of them with a high surface area, the low ESR is expected to increase efficiency slightly, as well as increase the reliability of the converter. Each of the delivered capacitors are 5nF, which when stacked in parallel, allow the design of the exact desired snubber capacitance in 5nF increments. The initial design is to use two 100nF capacitors as the snubbers, future work will be to vary the capacitance and observe the effects. The old and new snubbers are shown in Figure 98 and Figure 99.
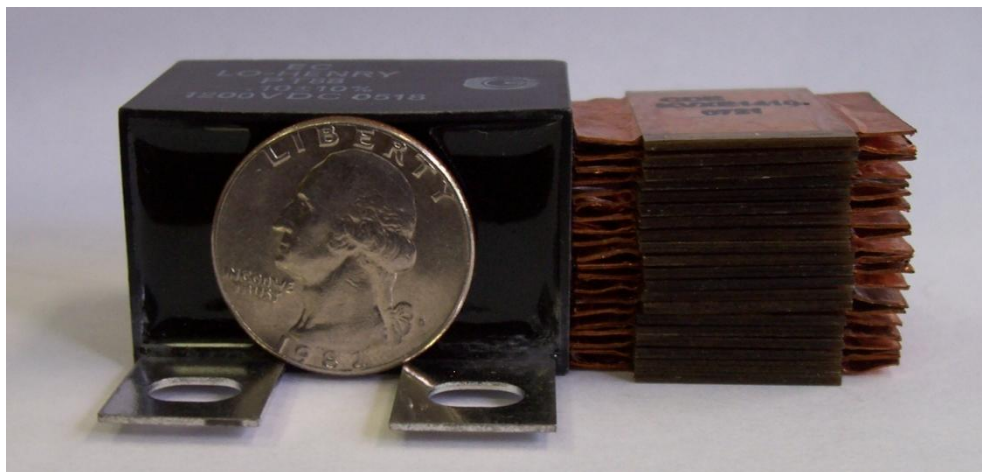
Figure 99 Side View of the Custom Snubber Capacitors vs. off-the-shelf Snubber

Power PCB Design and DC-DC Converter Structure

The power PCB, was designed to accomplish two main goals, provide the capability for high power operation, and configure the devices in such a way that optimizes power density. The power PCB houses a single IGBT module, the snubber capacitors, an input and output capacitor, and the connections to the driver and controller boards. The power PCB also has slots for copper busbar to pass through the module, to allow for paralleling of multiple modules. The design of the power PCB occurred simultaneously with the design of the overall converter structure, which was performed using 3D modeling software. The power PCB schematic is shown in Figure 100.
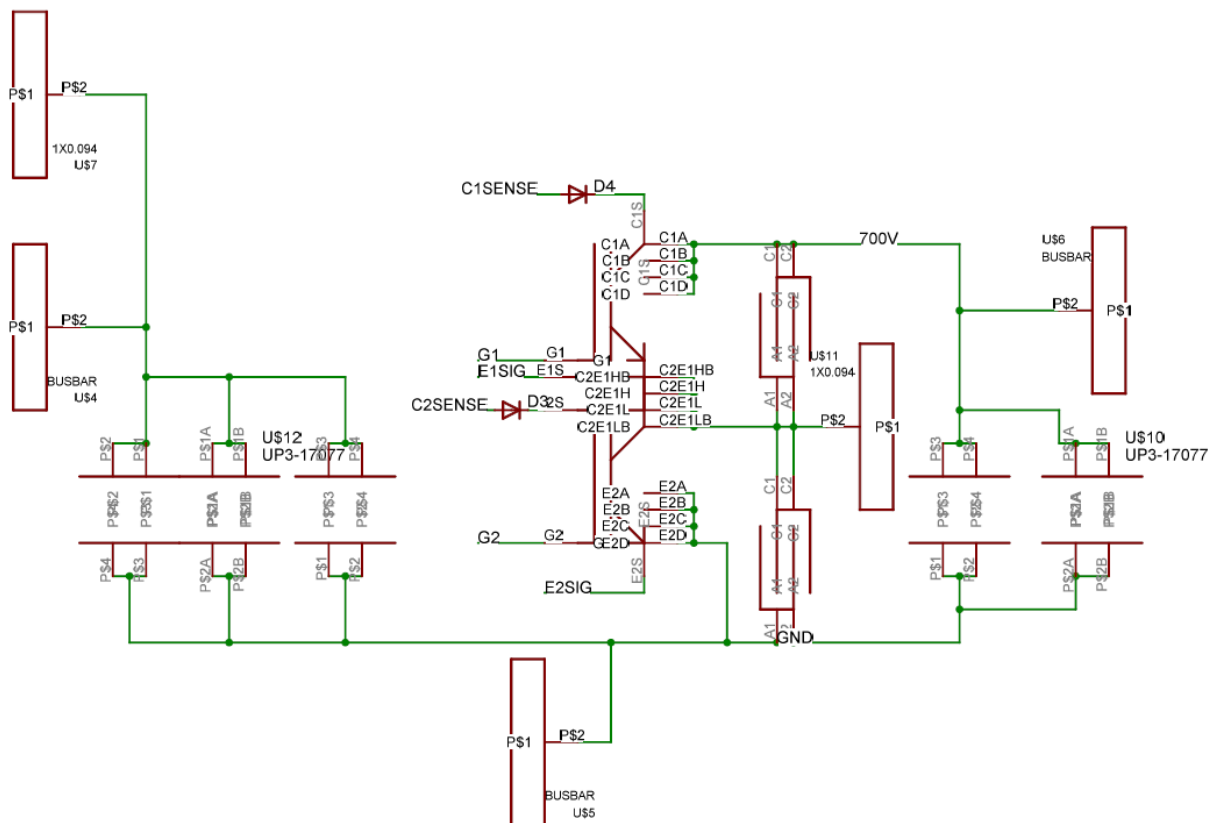
Figure 100 Power Board Schematic

The power PCB boards are constructed with 6oz copper boards, which will be able to accommodate the high current levels. The power board integrates one high side capacitor and one low side capacitor. The bus bar configuration has been designed to allow for the easy parallel connection of the 8 modules.
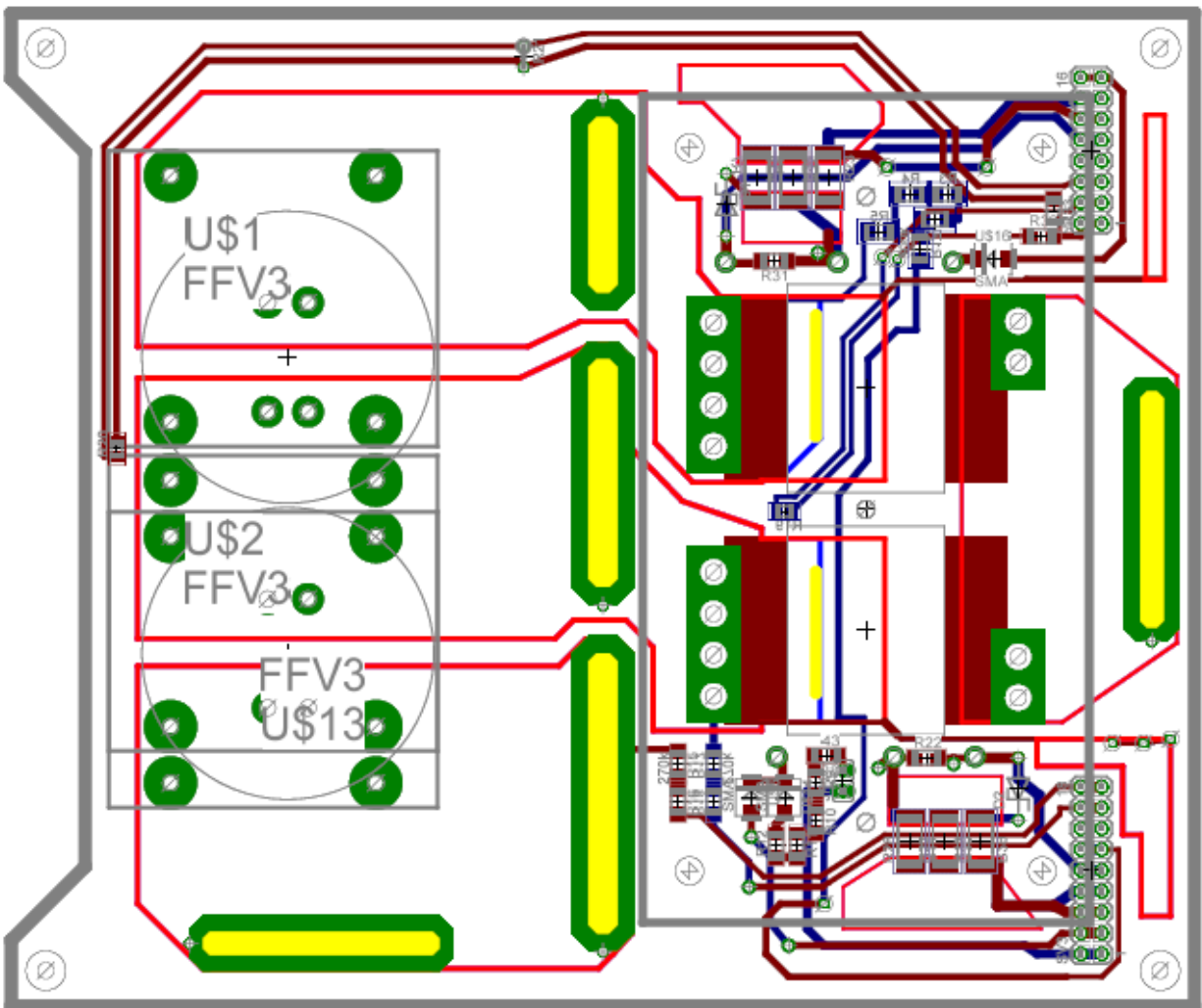
Figure 101 Power Board Layout (without controller board connections for clarity)

To save space, the gate drive resistors were implemented as surface mount components, which use a copper pour area to dissipate waste heat. The signal portions of the board are behind ground and 700V sections of copper pour which will help to eliminate switching noise from the converter from interfering with proper operation. The west end of the board was notched inward

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to make space for communication wires, which will be able to pass within the overall outline of the board, thus reducing the overall size of the converter enclosure.

The PCB was designed so as to have the switch node bus-bar pass by a Hall Effect sensor on the driver board. The negative space under the filter capacitors (next to the spray cooler and IGBT), is then filled with the cooler and IGBT module from the other module in the 2-module pair. In this way, the overall volume is almost completely occupied, maximizing power density.

The bus bar connection is designed to easily parallel multiple modules, while minimizing the total system volume. Multiple converters can be stacked vertically, which allows for a short connection between the converters, thus helping to minimize the necessary capacitance, and capitalize on interleaved operation. The final converter will be a 2X2X2 stack of converters, resulting in a very small high power density converter. By properly selecting which converters are controlled in the interleaving pattern, we can maximize the performance, and minimize losses due to ringing and the skin effect of the bus bar. Logically, it makes sense to parallel closely converters which are complements in terms of the interleaved operation. Then those two converters should be paralleled with the converter pairs which are 90 degrees out of phase from that. This will allow for a near-DC current in the main bus bar, which will help to reduce the necessary size of the bus bars and the overall system.

The driver board will connect to the power board in a similar fashion where the bias power supplies occupy the space to the outside of the snubber capacitors. The design will allow for the switch node bus bar to pass by the current sense IC. The controller board will mount perpendicular to the driver board, thus filling out the space above the snubber capacitors. The 3D model of the converter design is shown in Figure 102, Figure 103 and Figure 104. A single assembled model is shown in Figure 105, and 4 modules assembled is shown in Figure 106.
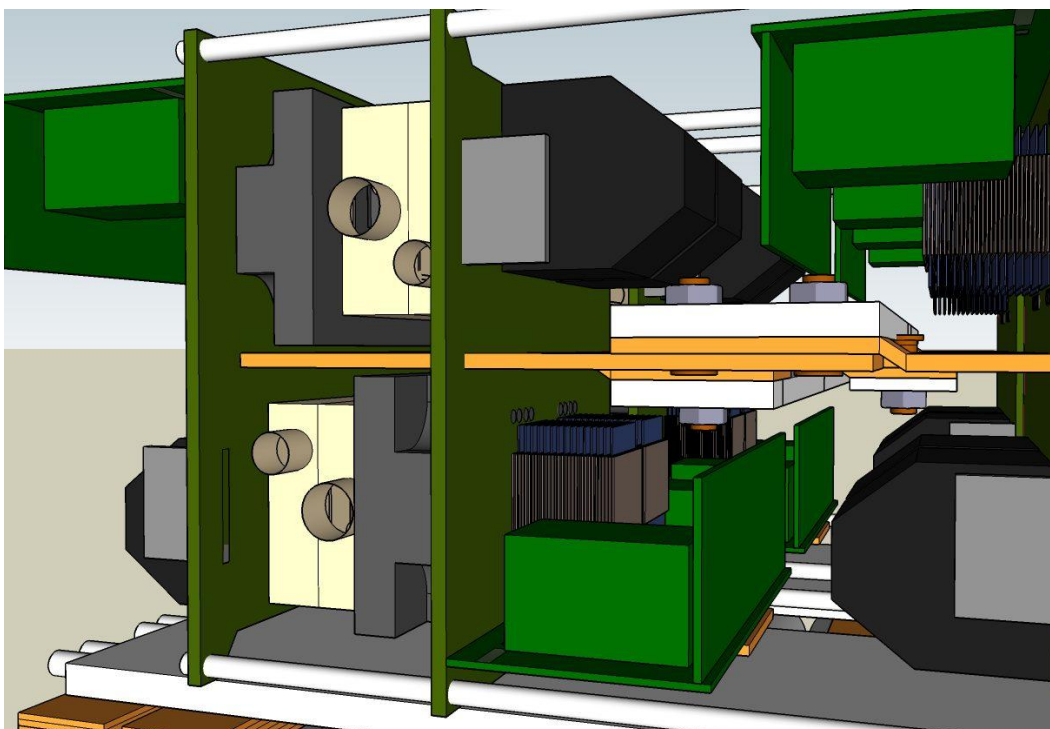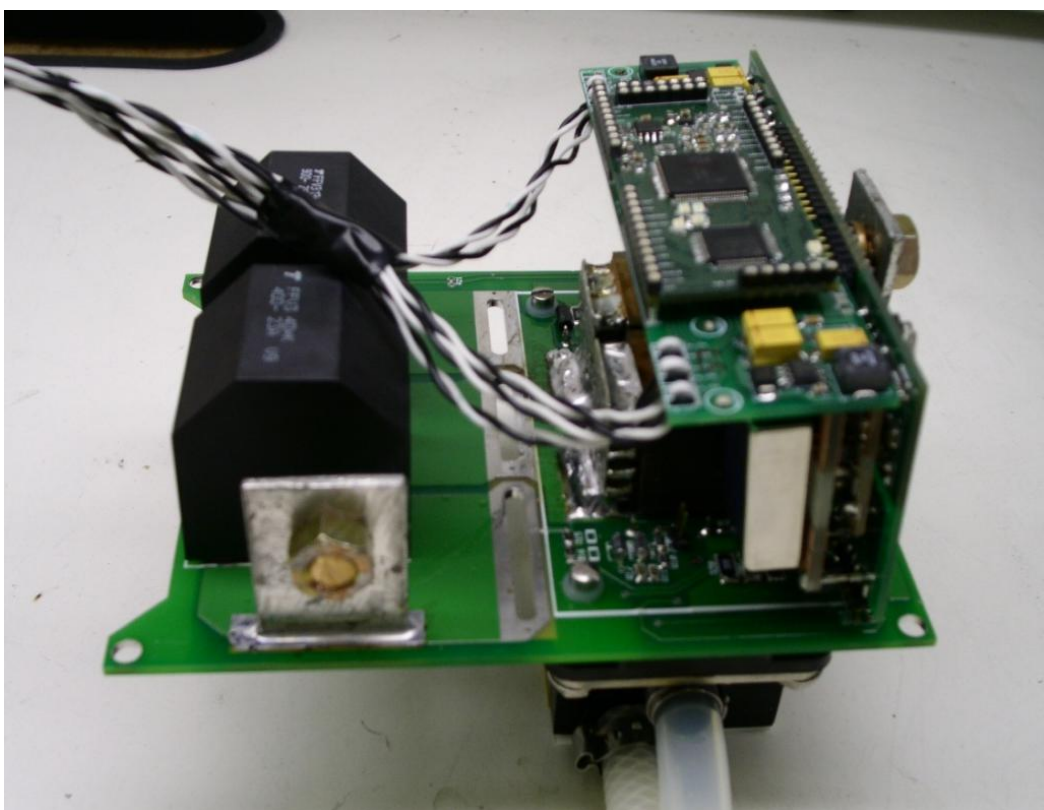
Figure 102 3D Model Profile
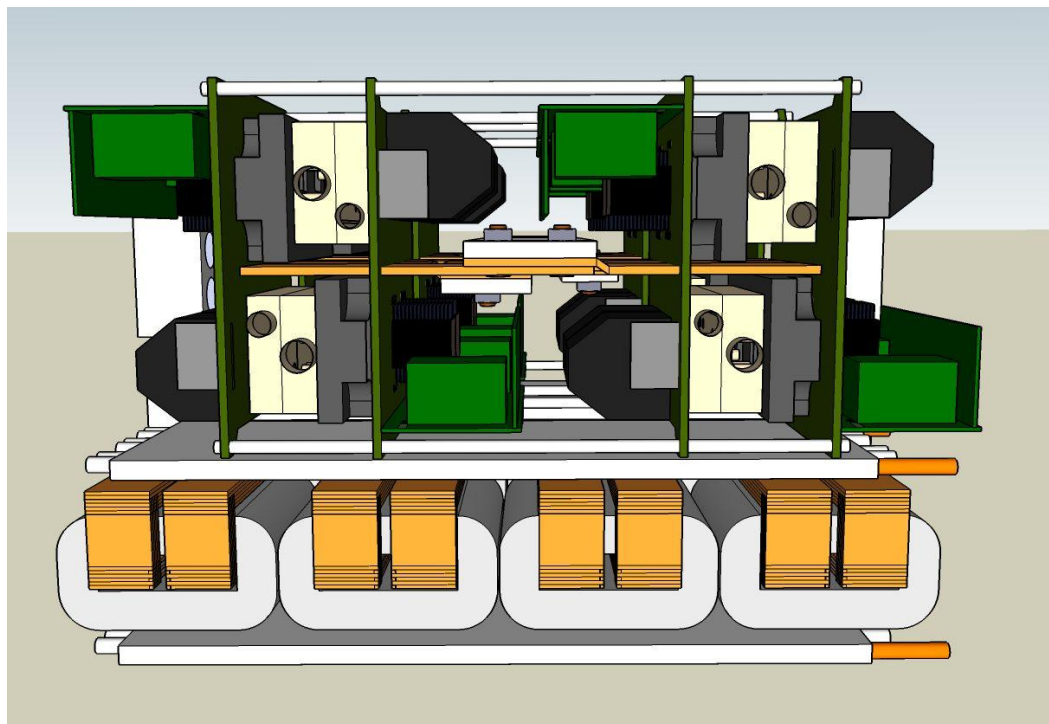
Figure 103 3D Model Side

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Figure 104 2-Module Assembly

Figure 105 Assembled power PCB module with driver and controller boards
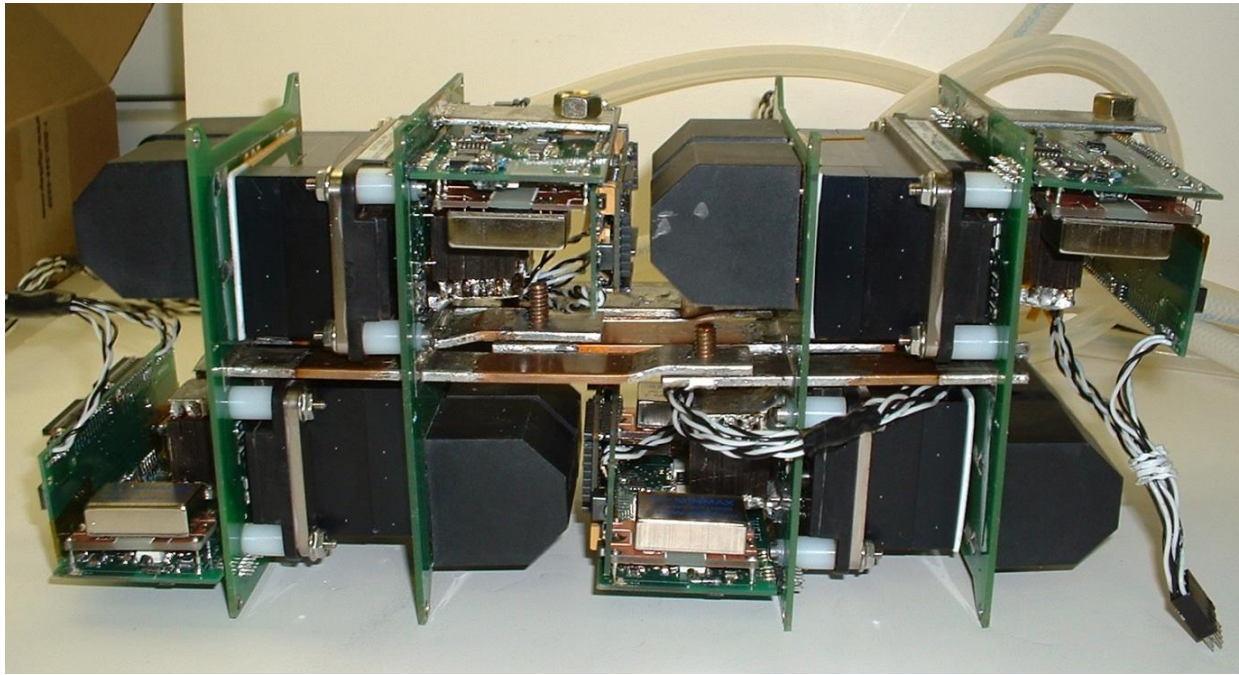
Figure 106 Assembled 4-module prototype

Simulation of Interleaved Converters w/ Parasitic Elements

The total input and output capacitance of the converters can be substantially reduced through the use of interleaved operation. Since the average current is nearly DC after the current from 8 modules is properly interleaved, the ripple current that each capacitor must filter is significantly less than that of a single module, allowing the use of less capacitors, and increasing power density. The parasitic inductance and capacitance of the bus bar connections will decrease the effectiveness of the distributed capacitance. This is because the current ripple will hit the nearer capacitor before the other distributed capacitors can help to filter the current ripple. The parasitic elements are especially critical for the high side capacitors, since the current quickly changes as the high side diode begins to conduct. The ringing on the capacitor can result in very high RMS currents. It is necessary to model the connections between the converters, so that the effect of the connections as well as the parasitic elements of the capacitors and traces can be evaluated.

The simulations were created to simulate the full bus bar setup of the 8 interleaved converters. From this the RMS currents of the capacitors have been evaluated to determine the necessary capacitors. This simulation also allows for estimation of ripple in the output voltage.

The simulations revealed that the maximum ripple current for the high voltage bus capacitor is 13 Arms, and the ripple current for the low voltage is only 1.5 Arms. It was determined that a single polypropylene capacitor can be used on the input and output side of each converter module, which will help to reduce the overall size of the system, and increase the power density. The SPICE simulation and results for the high voltage input capacitors are shown in Figure 107 and Figure 108. The simulation and results for the low voltage input capacitors are shown in Figure 109 and Figure 110.
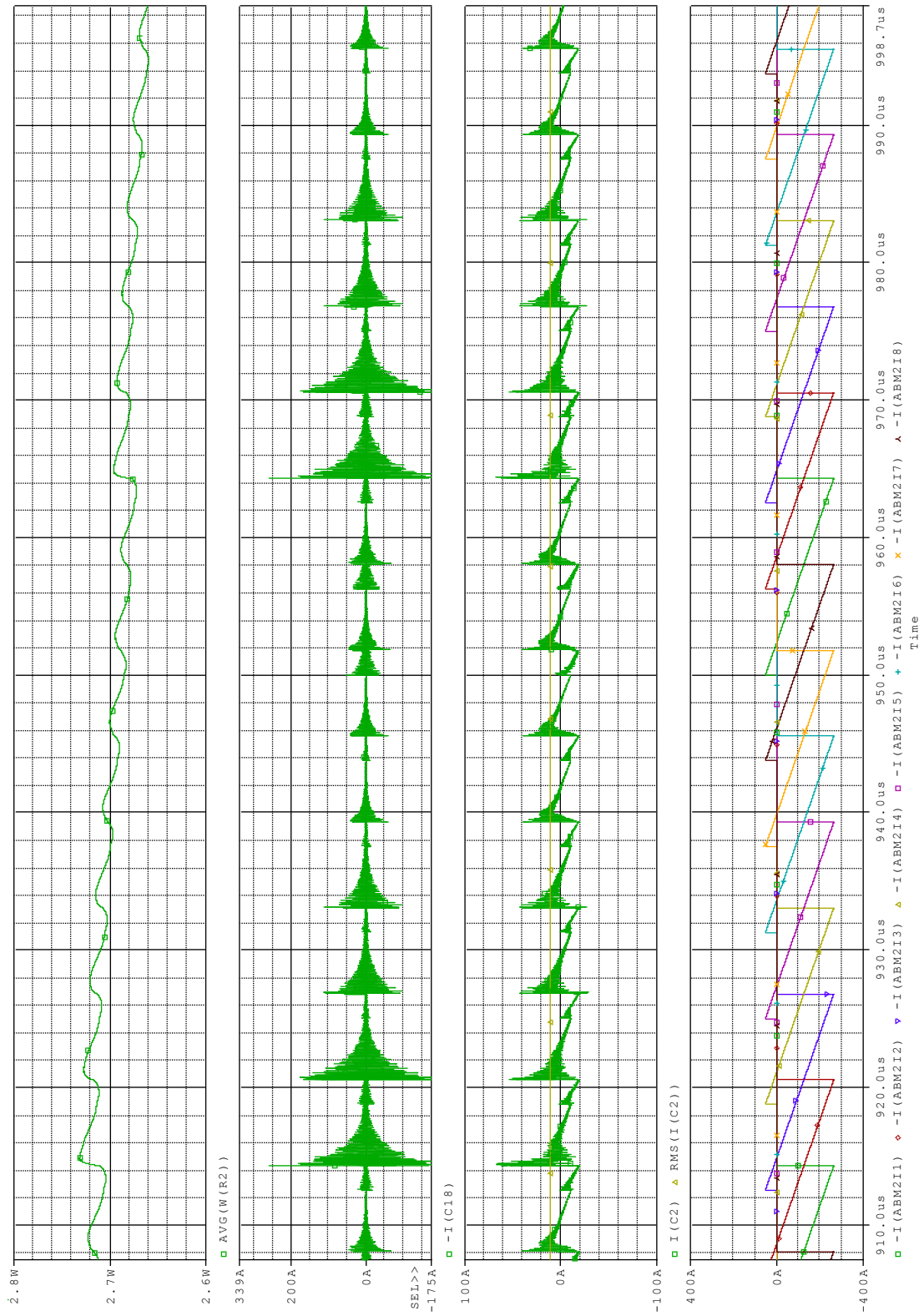
Figure 107 HV bus capacitor simulation
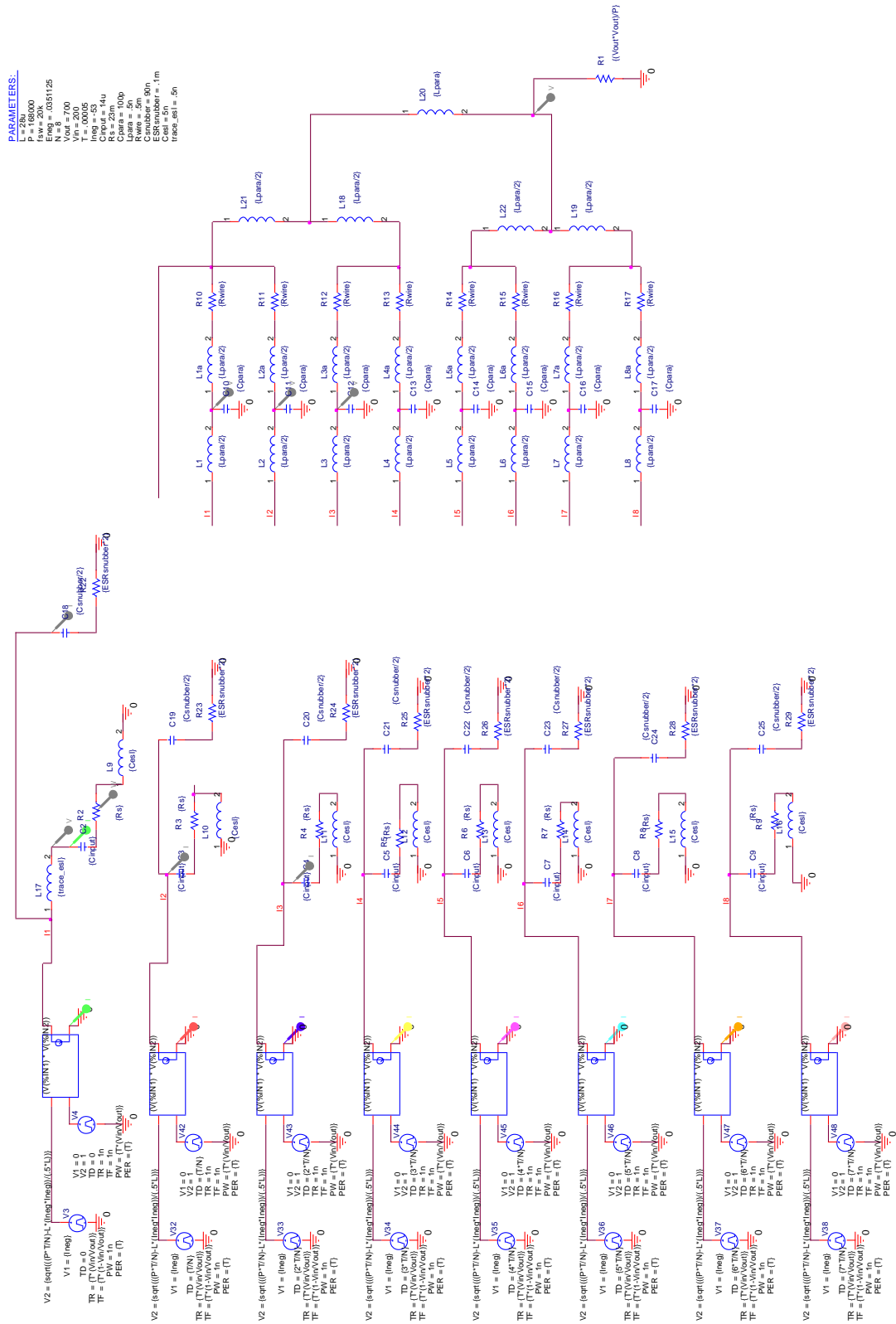
Figure 108 HV bus capacitor simulation results

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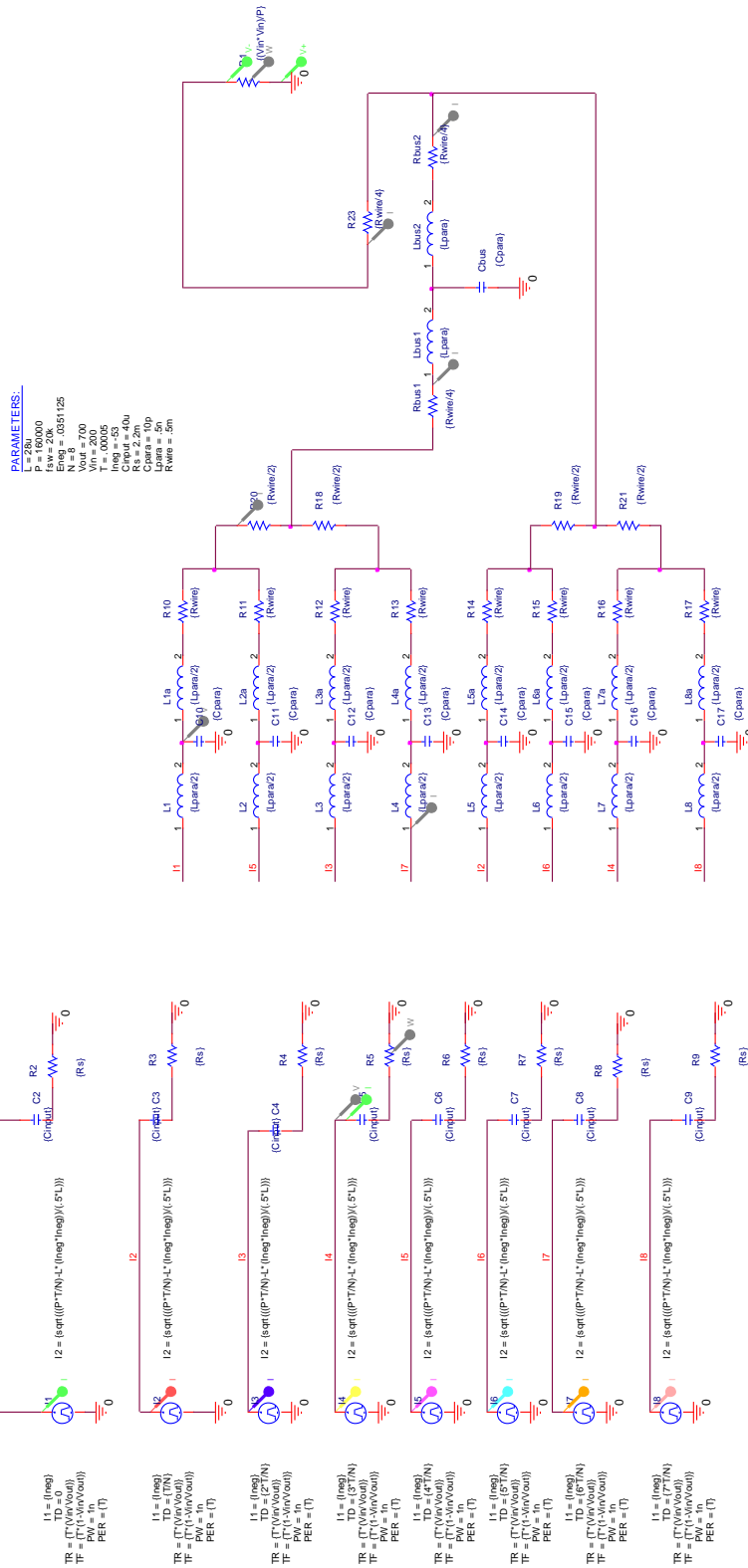
Figure 109 LV bus capacitor simulation

PARAMETERS:
L = 28u
P = 160000
fsw = 20k
Eneg = 20k
N = 8
Vout = 700
Vin = 200
T = .00005
Ineg = -53
Cinput = 40u
Rs = 2.2m
Cpara = 10p
Lpara = 5n
Rwire = .5m

R23 (Rwire/4)
Rbus2 (Rwire/4)
Lbus2 (Lpara)
Cbus (Cpara)
Lbus1 (Lpara)
Rbus1 (Rwire/4)

R20 (Rwire/2)
R18 (Rwire/2)
R19 (Rwire/2)
R21 (Rwire/2)

R10 (Rwire)
R11 (Rwire)
R12 (Rwire)
R13 (Rwire)
R14 (Rwire)
R15 (Rwire)
R16 (Rwire)
R17 (Rwire)

L1a (Lpara/2)
L2a (Lpara/2)
L3a (Lpara/2)
L4a (Lpara/2)
L5a (Lpara/2)
L6a (Lpara/2)
L7a (Lpara/2)
L8a (Lpara/2)

C10 (Cpara)
C11 (Cpara)
C12 (Cpara)
C13 (Cpara)
C14 (Cpara)
C15 (Cpara)
C16 (Cpara)
C17 (Cpara)

L1 (Lpara/2)
L2 (Lpara/2)
L3 (Lpara/2)
L4 (Lpara/2)
L5 (Lpara/2)
L6 (Lpara/2)
L7 (Lpara/2)
L8 (Lpara/2)

V(Vin*Vin/P)
V+

R2 (Rs) C2 (Cinput)
R3 (Rs) C3 (Cinput)
R4 (Rs) C4 (Cinput)
R5 (Rs) C5 (Cinput)
R6 (Rs) C6 (Cinput)
R7 (Rs) C7 (Cinput)
R8 (Rs) C8 (Cinput)
R9 (Rs) C9 (Cinput)

I1 = (Ineg)
TD = 0
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (2*T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (3*T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (4*T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (5*T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (6*T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I1 = (Ineg)
TD = (7*T/N)
TR = (T*(Vin/Vout))
TF = (T*(1-Vin/Vout))
PW = 1n
PER = (T)

I2 = (sqrt((P*T/N)-L*(Ineg*Ineg))/(.5*L)))

Figure 110 LV bus capacitor simulation results

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Integrated Controllers/Drivers

The IGBT controller and driver board is designed to interface with the power PCB, and utilize the available space in the converter to increase density. As can be seen from Figure 111, the bias power supplies stick out into the space above the gate drive resistors on the power PCB, and there is empty space in the middle for the snubber capacitors of the power PCB. The driver PCB uses fully isolated bias power supplies and opto-isolated gate drivers to provide +- 15 V driving logic to the IGBT modules. The center of the back of the driver board has an open loop hall effect sensor, which allows the sensing of the inductor current in the switch node busbar.
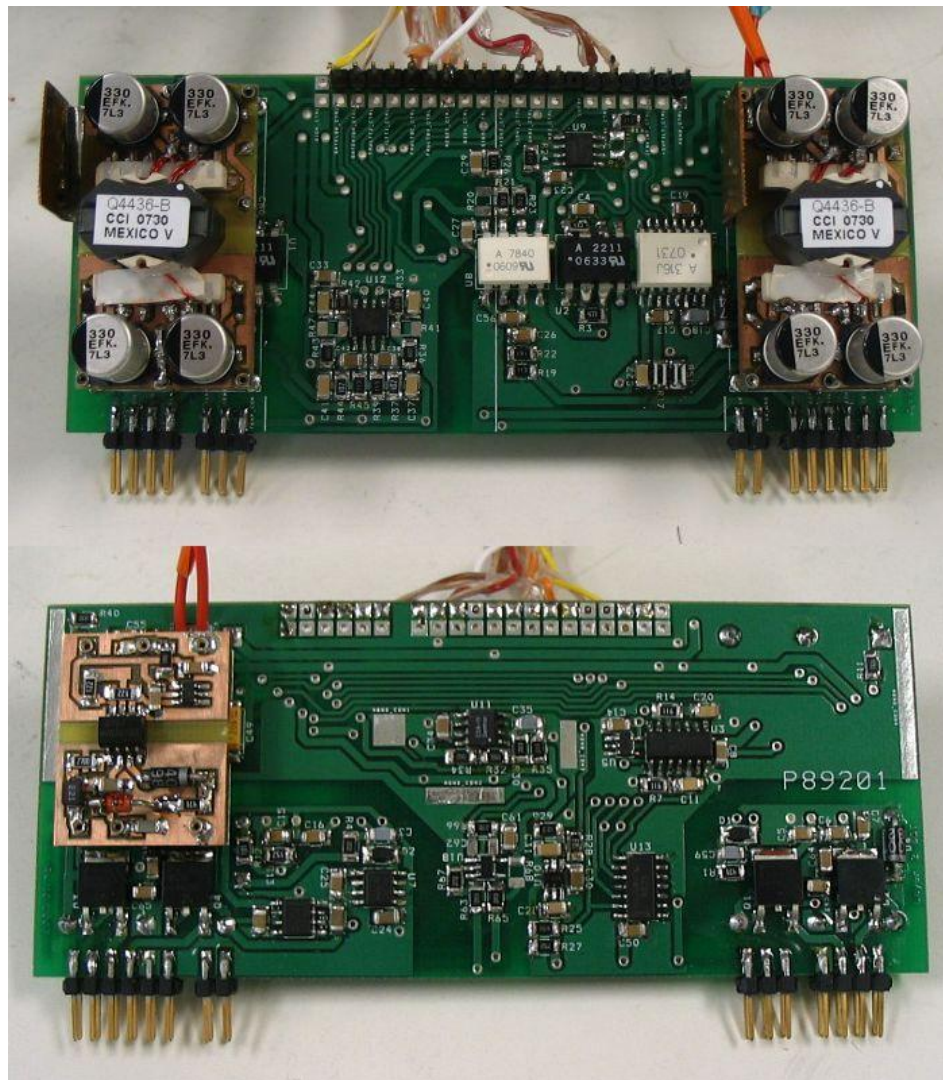

Figure 111 Populated IGBT driver board (Top & Bottom)

Experimental Results

To test the modular converter, a 2-module demonstration prototype was constructed. The converter utilized 100°C liquid cooling for the IGBT modules as well as the nanocrystalline inductors. The DC-DC converter modules were designed in a way which allows the converters to share common copper bus bars for the High Voltage bus, the battery bus, and ground connections. The converters fit together to maximize the power density as well as to minimize the current ripple experienced by the filter capacitors. In this prototype, each IGBT module has its own coolant lines, which are paralleled by the cooling unit.
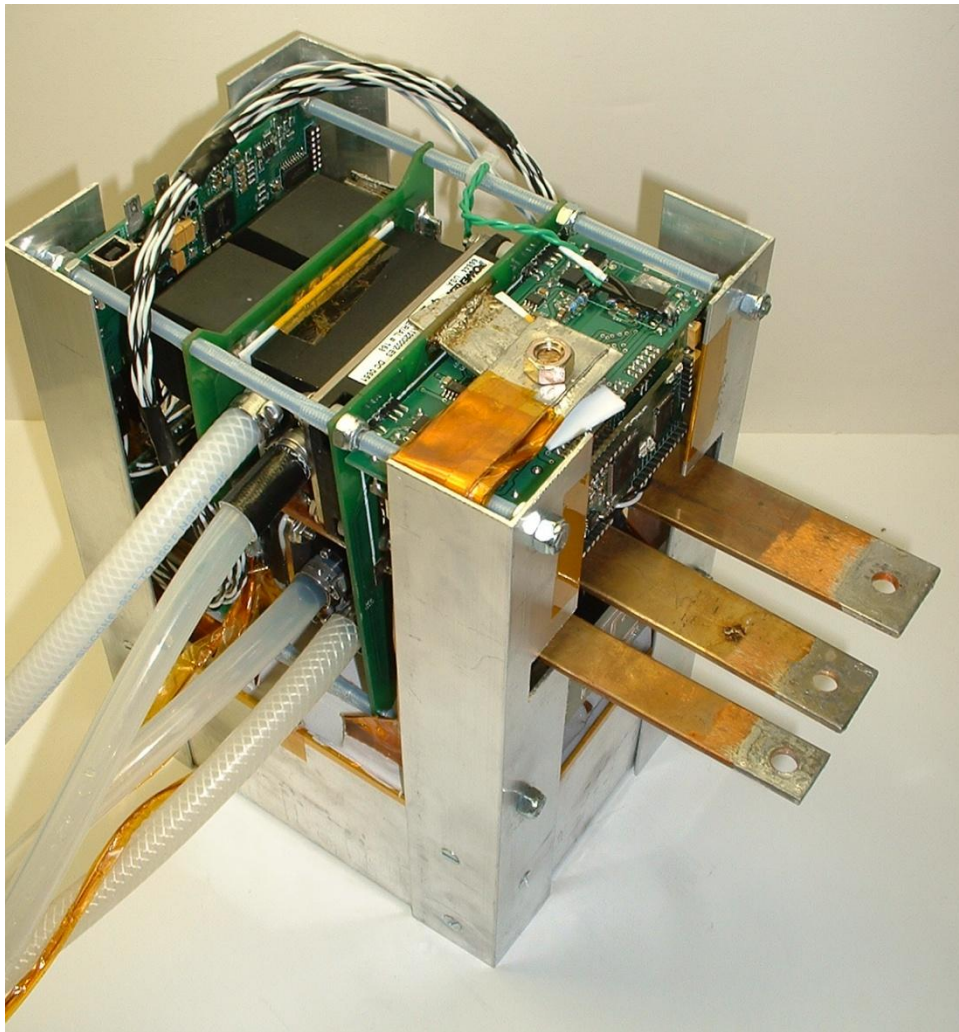

Figure 112 2-Module 50 kW Prototype

The 2-module prototype is contained in an aluminum enclosure, which has a sheet metal outer skin. To further increase system power, more 2-module pairs can be easily paralleled. The system uses a master communication board to handle communication between the converter modules and the vehicle. Since the modules use CAN communication to perform control functions, it is desirable to separate this CAN bus from the vehicle CAN bus. The communication board has an external CAN interface as well as a USB interface for bench top testing with communication to a PC with a controlling software interface. The completed converter can be seen in Figure 112. The specifications of the 2-module DC-DC converter prototype are shown in Table 10.

**Table 10 2-Module ESC DC-DC Converter Specifications**

Input Voltage	200V – 350V
Output Voltage	650 V – 800V
Output Power	50 kW
Inductance (each module)	20 uH
Inductor Saturation Current	400 A
Snubber Capacitance (per IGBT)	100 nF
Output Capacitance (400V)	80 uF
Input Capacitance (900V)	26 uF
IGBT Module Current Rating	200 A
Freewheeling Diode Current Rating	2 X 100A
Peak Efficiency	97%
Operating Frequency (low – high power)	60 kHz –18 kHz
Maximum Coolant Temperature	100°C
Coolant Flow Rate	1.9 L/min
Coolant Pressure (50/50 EGW)	40 psi
Converter Volume	6 L

The spray cooling set up was delivered from RTI complete with temperature regulation and measurements, pressure adjustments and measurements, and water level indicators. The spray cooling system was attached to the spray cooling nozzles and fixed to the custom IGBTs. This testing set up can be seen in Figure 113 and Figure 114.
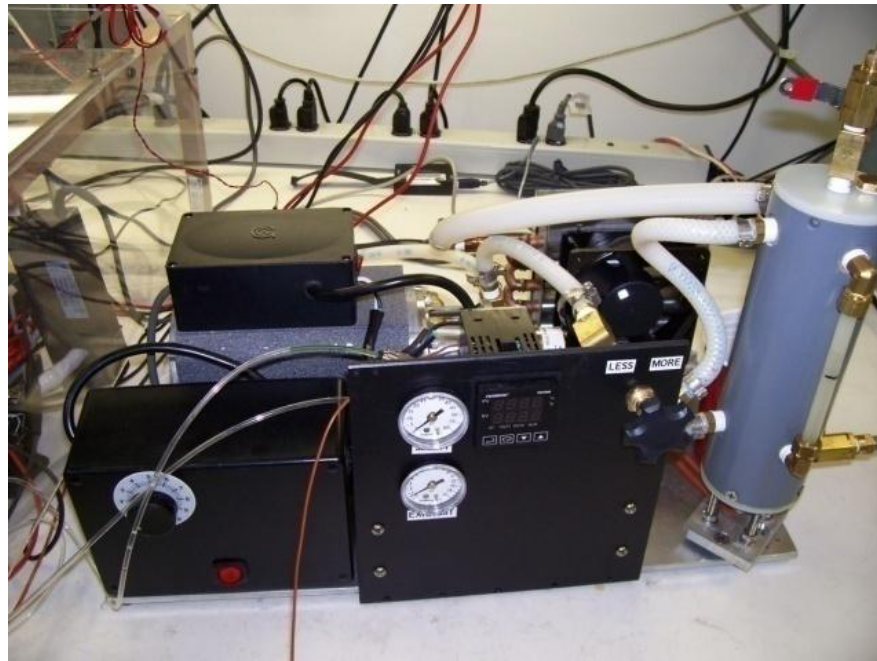
Figure 113 Cooling system used to run evaporative spray cooling modules
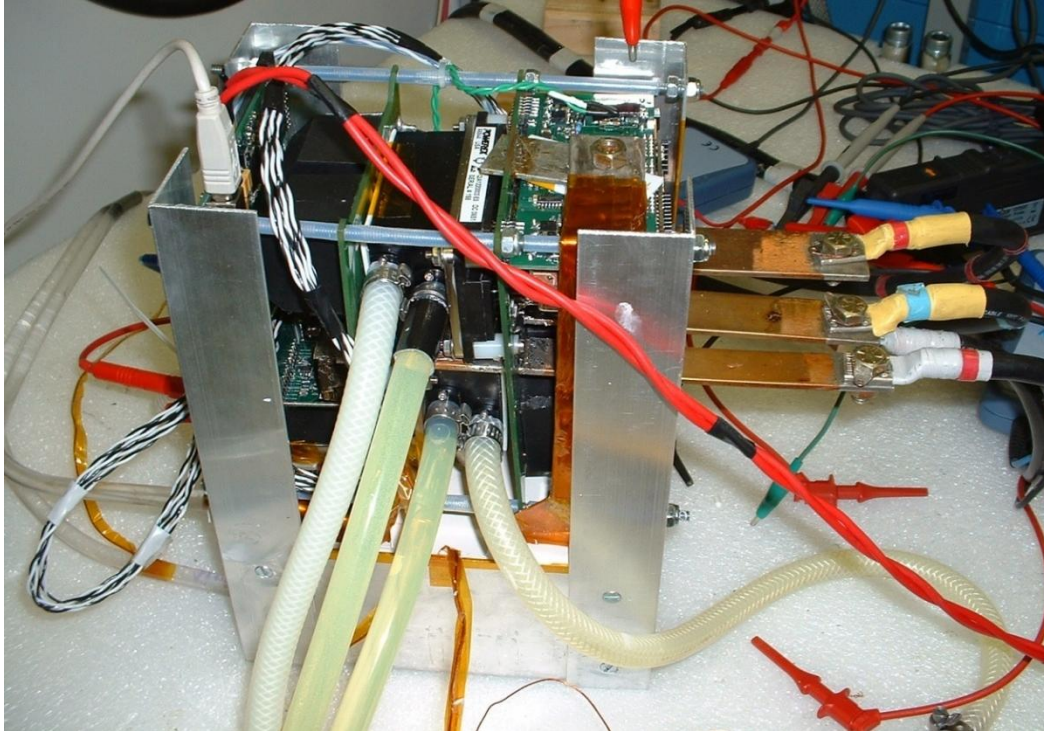
Figure 114 2-Module ESC DC-DC converter in-testing

Evaporative Spray Cooling Results

The evaporative spray cooled IGBT's have been shown capable of achieving high heat flux, which allows the devices to be cooled with 100°C coolant. The modules were tested to over 22 kW each at 200V to 700V operation, which puts the most stress on the IGBT. Figure 115 shows the temperature rise of the IGBT above the coolant temperature versus the output power, as reported by the thermocouple integrated into the module. This temperature reading is not completely accurate, as the thermocouple is placed next to the IGBT die. The actual die temperature is higher than the thermocouple reading, but it is unknown by how much. The estimate is that the actual die temperature is approximately 40% higher than the thermocouple reading, which keeps the IGBT below the designed limit of 140 °C. The design goal was for the IGBT ΔT to be less than 40 °C, which the experimental data supports. The die is designed to

operate at 150 °C, but for long-term reliability, lower temperature is better. It is good to have the additional ΔT overhead, as this will allow for handling of transients.

IGBT Delta T VS Output Power
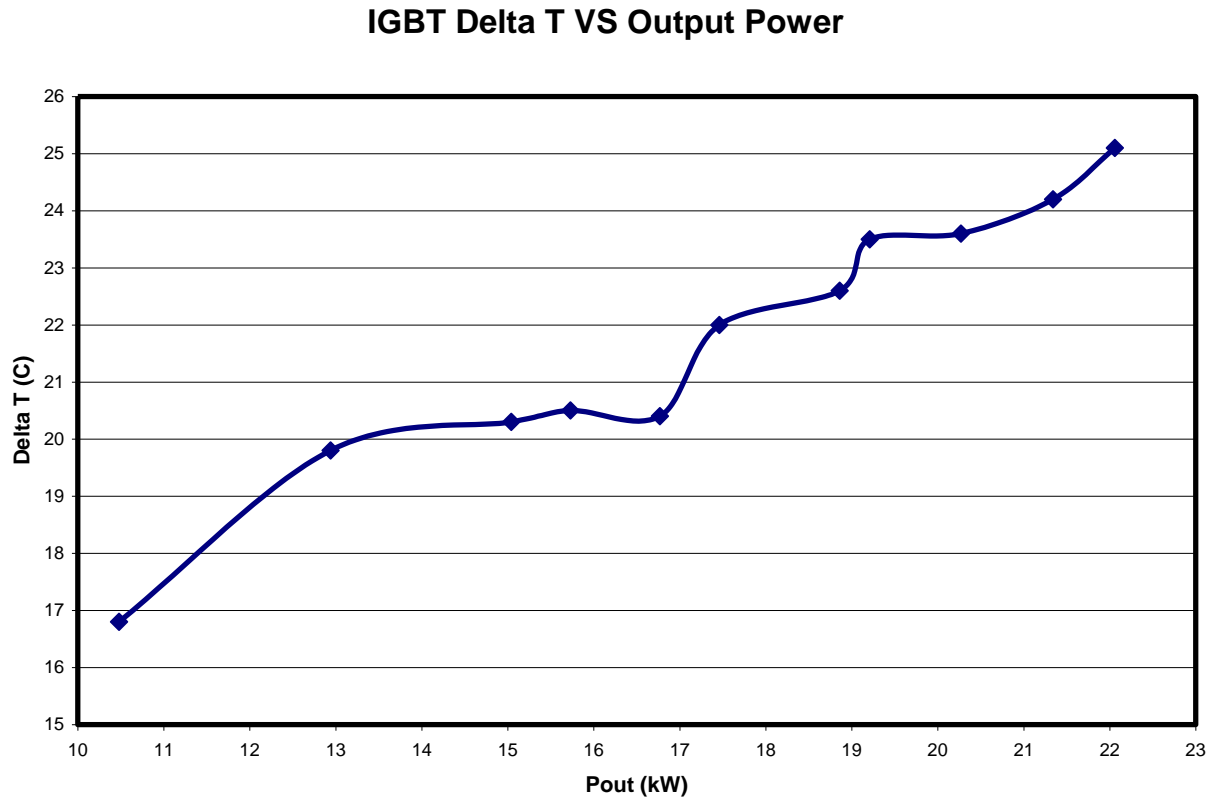
Figure 115 Experimental IGBT Temperature Rise @ 95°C Coolant

Final Converter Efficiency

The two-module converter was tested for overall efficiency at the 200V to 700V case, which is the most stressful for the converter, and yields the lowest efficiency. The efficiency was measured using calibrated resistor load banks, and calibrated Hall Effect current meters. Efficiency is always difficult to measure accurately, especially for high-power converters. A great amount of effort was put into accurate efficiency measurement, yielding results that are believed to be within (+0.25%, -0.5%) accuracy. The efficiency curve is shown in Figure 116.
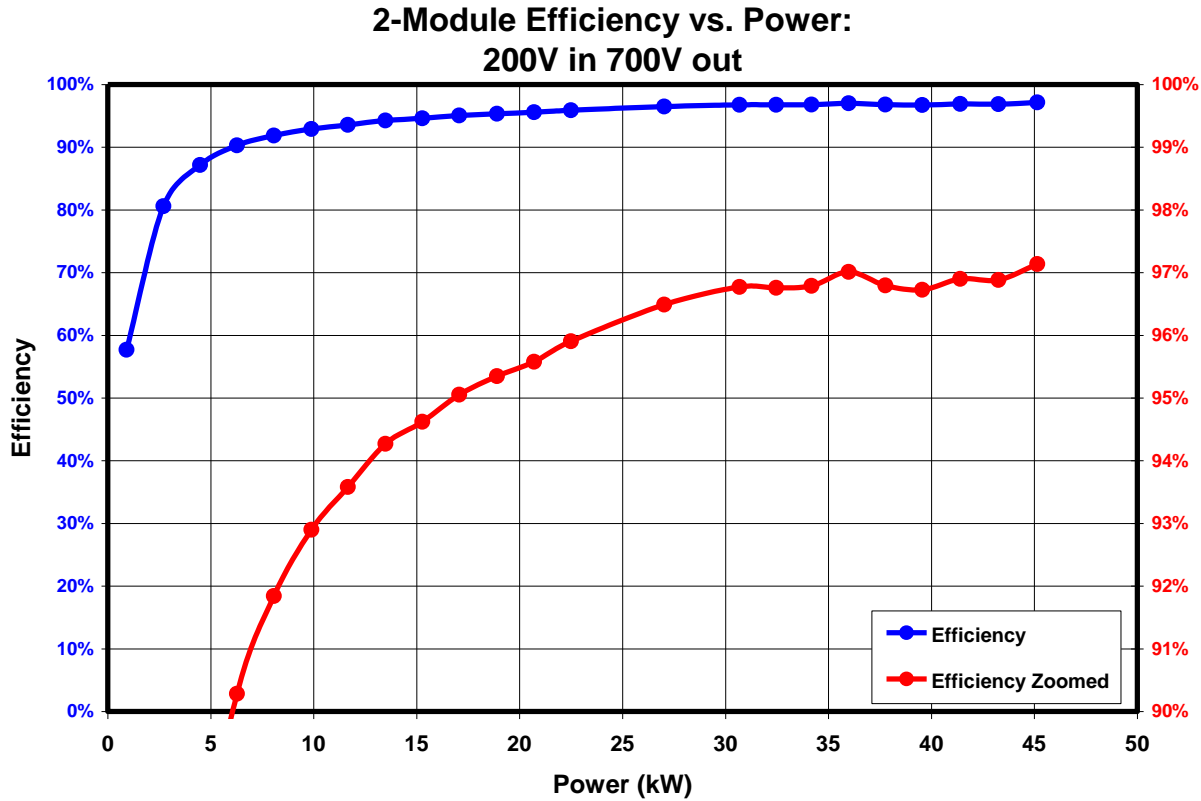
Figure 116 Final experimental efficiency of 2-module ESC DC-DC converter

In order to achieve an even flatter efficiency curve, it is possible to employ a concept known as phase scheduling, where certain modules are deactivated when operating at lower power. Although this has not been implemented on this prototype, a highly modular system is very well suited for such an approach. This improvement is later implemented in the DC-DC converter documented in Chapter 6, which can yield a converter with an extremely flat and high efficiency curve across the entire power range. This is especially desirable for automotive applications, where the converter could potentially operate at light load for long periods of time.

Final Power Density

The two-converter prototype has a volume of 6.537 L. Depending on the operating voltages, the maximum power changes, with the converter being able to process more power at higher input voltages. During testing the converter was operated at 22.5 kW / module

at 200V to 700V, which yields a power density of 6.88 kW/L as a worst case. If the converter is operated at higher input voltage, higher power can be achieved, yielding higher power density exceeding 8 kW/L (50 kW = 7.64 kW/L @ 250V, 55 kW = 8.4 kW/L @ 300 V).

The mass of the converter is approximately 11 kg, yielding a mass power density of 4.1 kW/kg at 45 kW (200 Vin), and 5 kW/kg at 55 kW (300Vin). Some mass could be trimmed by adding lighter dense foam to larger areas of the inductor tray which are occupied by potting material, but this would only have a small effect. Most of the mass of the unit is in the critical components which cannot be reduced in weight, meaning that mass power density probably cannot be increased much above 5 – 6 kW/kg.

CHAPTER 5: COLDPLATE BASED COOLING DC-DC CONVERTER DESIGN

Although the design of the evaporative spray cooled DC-DC converter was successful, there are certain practical concerns which reduce the applicability of the converter to the hybrid-electric vehicle industry, specifically the stringent requirement for the coolant exhaust to be at atmospheric pressure. Since almost all current vehicle coolant systems intentionally operate at higher pressure to prevent boiling, significant changes to the cooling systems and the other devices in the coolant loop would be necessary to make evaporative spray cooling applicable, making the ESC DC-DC converter a more long-term solution. The DC-DC converter presented in this chapter is intended to evaluate the potential performance of the variable frequency soft-switching bidirectional DC-DC converter system design while using commercially available IGBT modules, and traditional liquid coldplates, which have no specific requirement for coolant exhaust pressure.

The converter was designed with similar specifications and goals as the ESC DC-DC converter, namely, 200 kW total power capability, 100 ℃ coolant operation, efficiency greater than 96%, and the capability for long-term reliability. The converter uses 8 IGBT modules, with the converter housing two 4-module 100 kW DC-DC converters. Each 4-module converter has a custom designed coldplate assembly, which houses four 32 uH nanocrystalline inductors, and also cools the IGBT modules. The converter features custom designed high temperature film snubber capacitors, heavy copper power PCBs, and a system design which maximizes density and efficiency.

IGBT Selection

Since the high-frequency packaging which was designed for the ESC DC-DC converter is not available for this design, the inductance in the path between the IGBT devices and the snubber capacitors is significantly higher, necessitating that the converter be designed for lower frequency operation, to mitigate this effect. In the ESC converter design, it was desired that the converter not operate at a switching frequency below 20 kHz, so as to prevent audible noise from the converter switching. In this case that design parameter was removed, with the hope that the audible noise is not very significant. The IGBT modules available were examined, and immediately two potential modules were identified as candidates, specifically based on the electrical performance ratings, as well as the very thin form factor, which is ideal for this design.

After extensive testing of a Powerex (CM300DX-24A) and an Infineon (FF300R12ME4) IGBT modules it was decided to use the Infineon part based on 3 major factors:

1. Higher efficiency

2. Cooler die operation

3. Higher maximum die temperature (175 ºC vs. 150 ºC)

Efficiency was compared in buck mode from 600V to both 300V and 450V with the same setup including inductor and power board. As can be seen from Figure 117 the Infineon IGBT performed better than the Powerex IGBT over the whole load range for both output voltages. The following section documents the process by which this data was obtained, and the IGBT module selection was performed.

600Vin Efficiency: Powerex vs Infineon
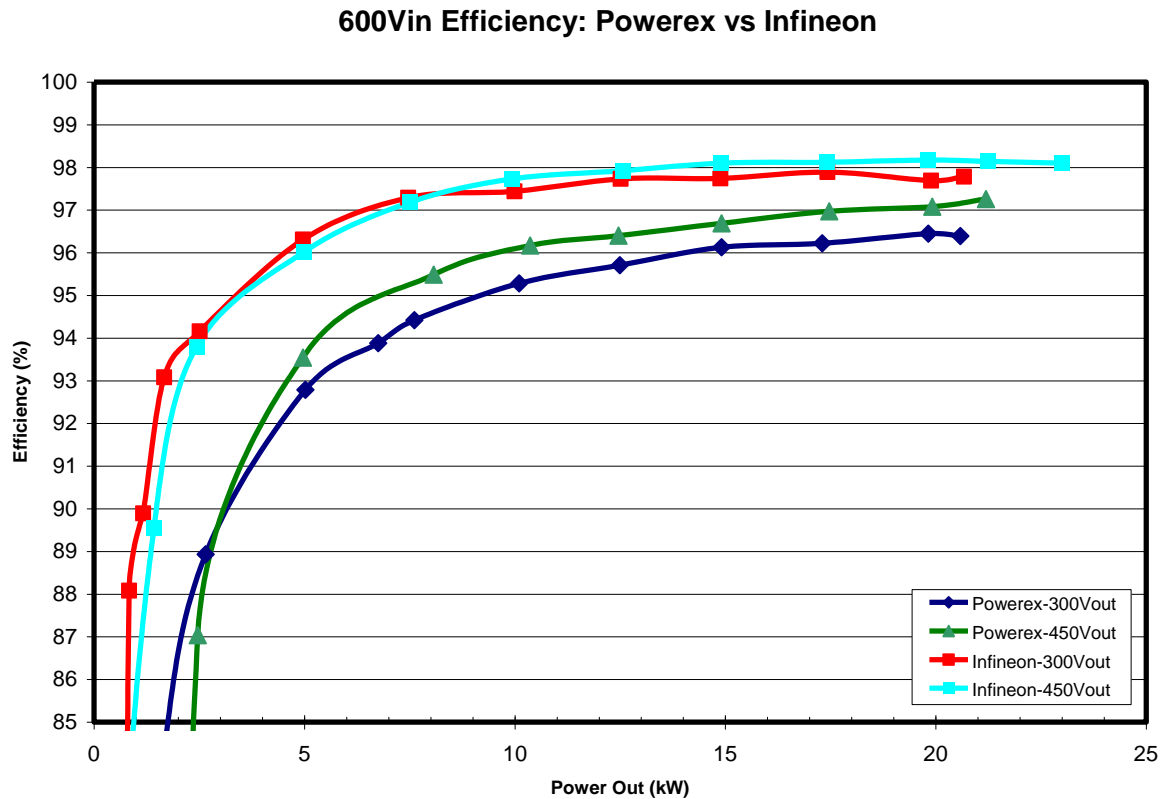
Figure 117 IGBT efficiency comparison: Powerex CM300DX-24A and Infineon FF300R12ME4

For help in analyzing the operation of the IGBT modules, a special prototype was built with an open window directly above the IGBT which enables the use of a thermal camera to directly see the IGBT and diode dies temperature once the lid is removed from the IGBT case. It is extremely helpful seeing how close the die's temperature is to the maximum operating temperature while the converter is running. Therefore long-term reliability of the system can be estimated. This prototype was tested close to full power in buck mode, efficiency measurements were taken and thermal images were captured. The layout of this prototype is shown below in Figure 118. Figure 119 shows the testing setup for power prototype 2 with water-cooling using off-the-shelf cold plates. It can be seen that the lid of the IGBT module is removed and the thermal camera is pointed directly at the IGBT module.
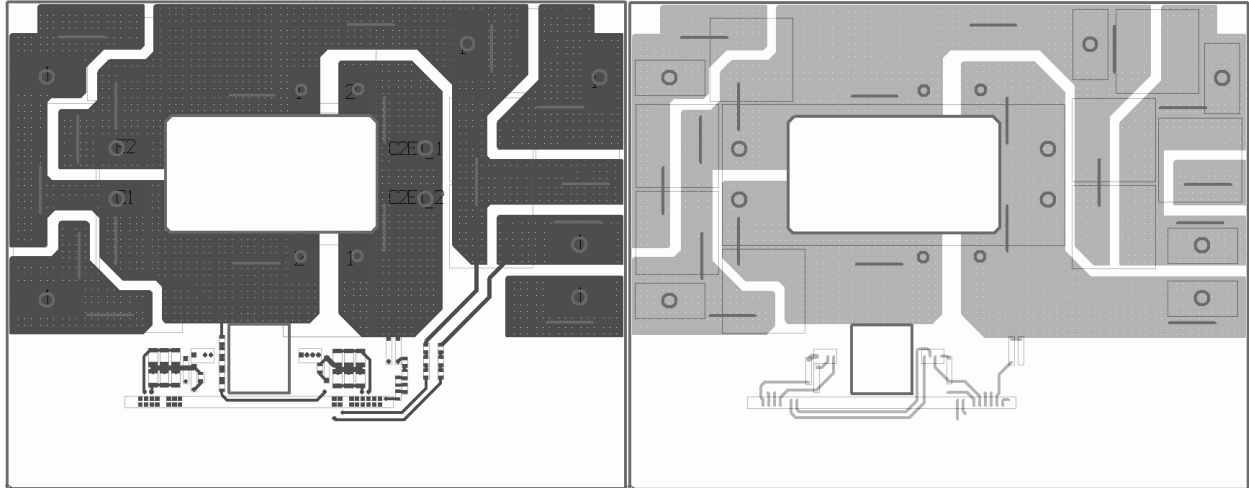
Figure 118 Layout of Power Prototype 2 (left: top layer, right: bottom layer)

Figure 119 Testing setup of open window testing prototype

The Powerex CM300DX-24A IGBT was tested with 70°C cooling temperature and reached a die temperature of approximately 111°C at 21kW output power. The thermal image in

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Figure 120 shows the 2 IGBT dies on the left and the 2 diode dies on the right. The actual die temperature is close to initial estimations based on the total losses in the IGBT. Even though the IGBT was running fine at the testing conditions, it will come very close to the maximum rated junction temperature of 150°C when the cooling is 100°C. Compared to the Powerex IGBT, the Infineon FF300R12ME4 IGBT operation was cooler at the same power level and higher cooling temperature, as shown in Figure 157. The reasons for the lower temperature operation on the Infineon IGBT are multiple. One reason is that the device simply has lower losses in the IGBT than the Powerex device, since it is a newer generation device. The Infineon device has a better distribution of the losses across the cooling baseplate, since it has three 100 A IGBT and diode dies, compared to two 150 A devices in the Powerex device, which are concentrated in a much smaller area within the package. Additionally, the thermal images for the Infineon are probably not be completely accurate because the gel covering the dies seems to disturb the temperature readings because of its unknown emissivity, but it still operates cooler without a doubt. In addition, the Infineon IGBT is rated for a maximum junction temperature up to 175°C and a continuous operation at 150°C whereas those 2 ratings for the Powerex IGBT are 25°C lower. This fact gives more headroom for extended high-temperature operation of the Infineon IGBT and added reliability of the converter.
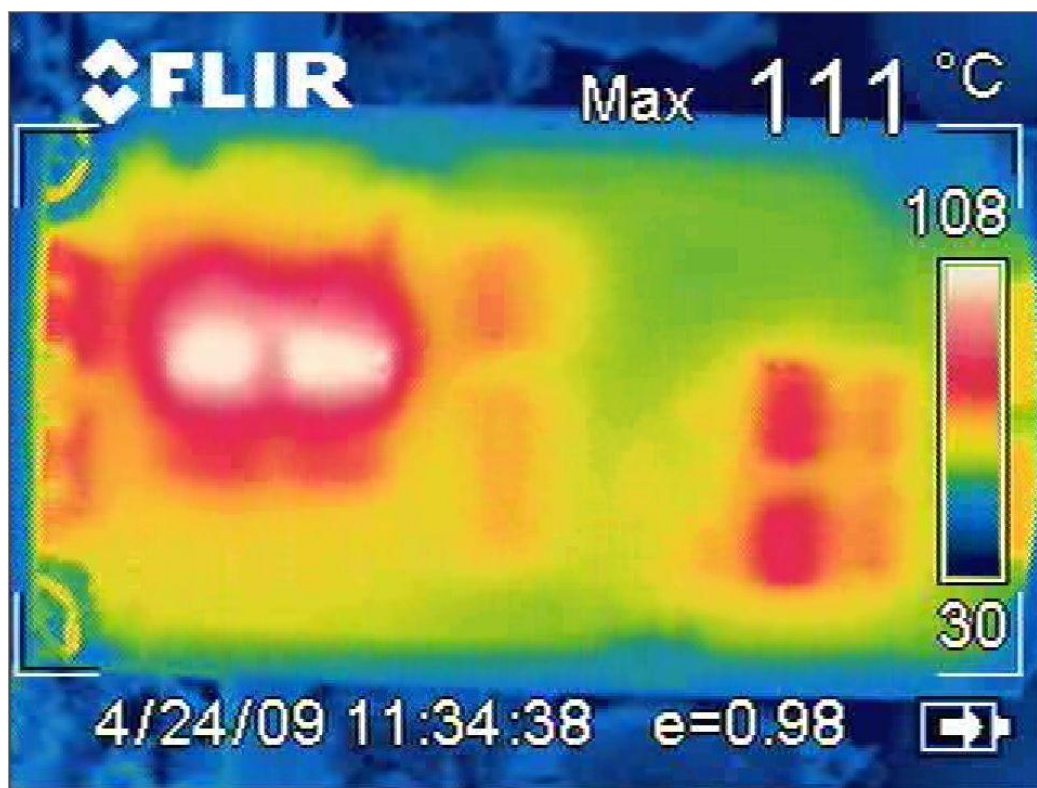
Figure 120 Thermal image of Powerex CM300DX-24A IGBT @ 21kW and 70°C cooling
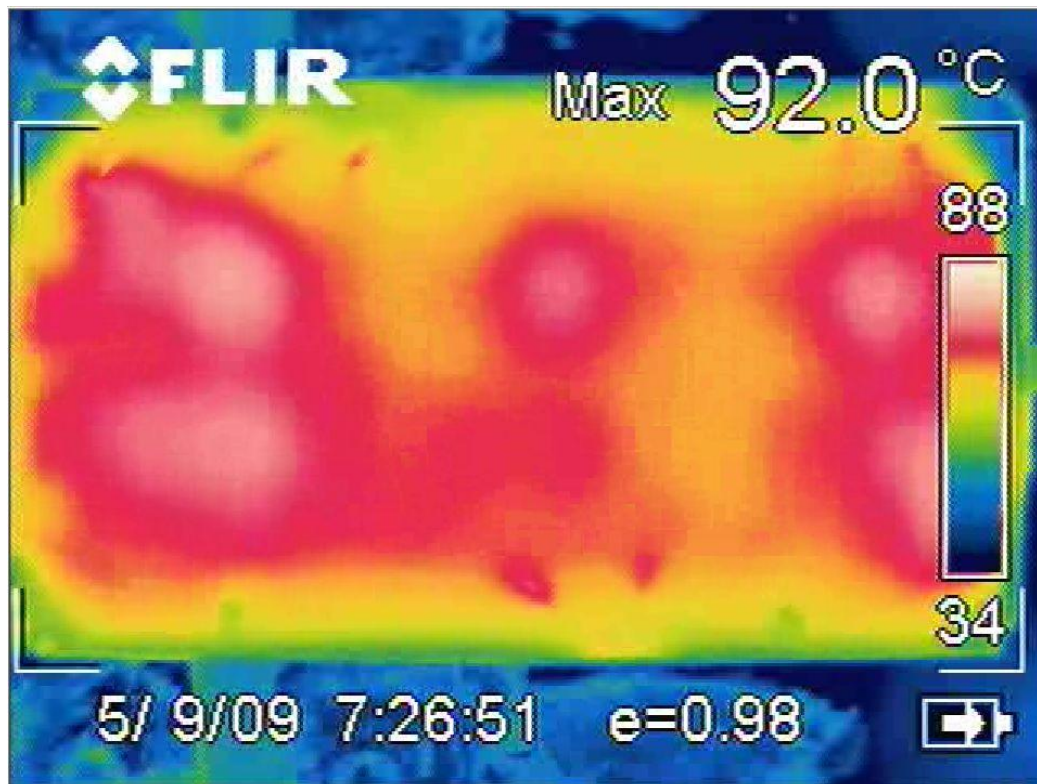

Figure 121 Thermal image Infineon FF300R12ME4 IGBT @ 21kW and 85°C cooling

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The main switching waveforms of the open window prototype were recorded. Figure 122 shows the inductor current, low and high-side gate signals as well as the switch node at 20.6kW output power in buck mode running with approximately 80°C coolant temperature. The special layout to leave room for the window to look at the IGBT directly added some additional inductance in the power path between the IGBTs and the snubber capacitors, which introduced some additional ringing of the switch node, meaning that the final converter will be even more efficient that what was found with this prototype,
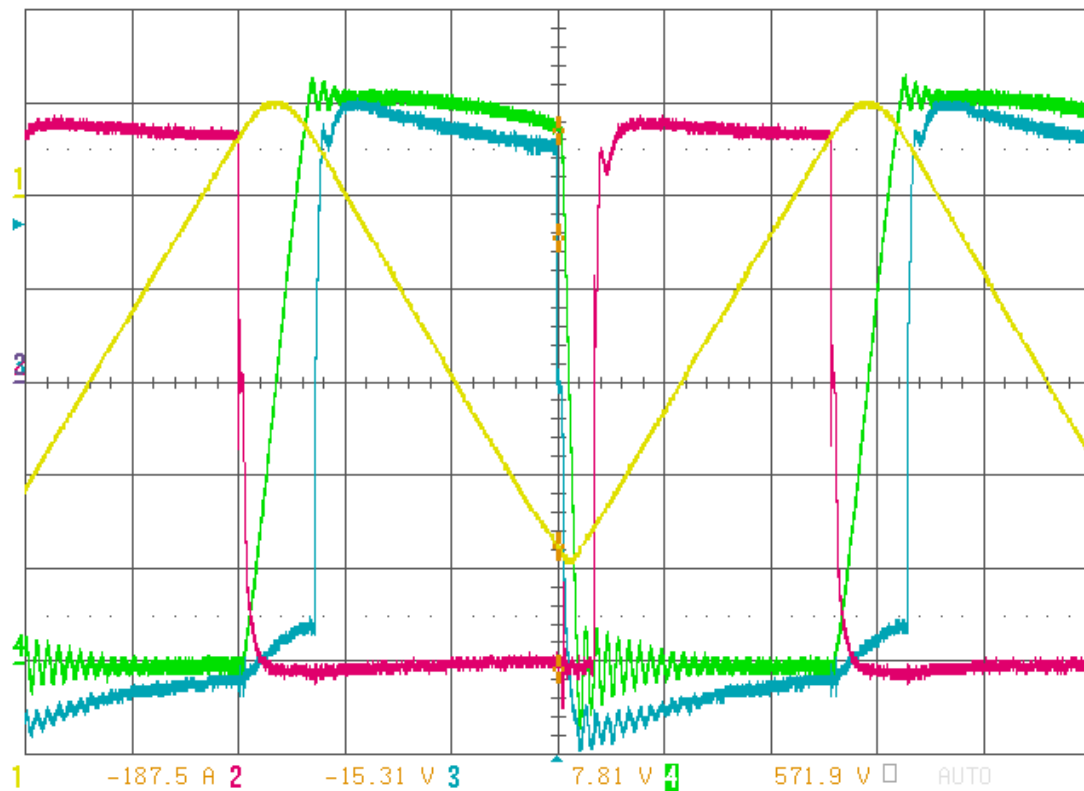
Figure 122 Switching waveforms, 20.6kW, buck mode (#1 inductor current, #2 low-side gate signal, # 3 high-side gate signal, #4 switch node)

The IGBT selection is critical for achieving high efficiency as well as high reliability. To ensure reliability, it is critical that the IGBT die temperature stay within a safe value. Since efficiency directly affects the IGBT temperature, achieving soft switching is the first step to

achieving this goal. The efficiency testing has given positive results, with the peak efficiency over 97% for the Powerex device, and over 98% for the Infineon device. It is also expected for this efficiency to slightly increase as the design is further optimized, and the layout is more optimal. Due to the unknown emissivity of the Infineon IGBT, it was difficult to accurately determine the die temperature, but, it is apparent from the efficiency data that the Infineon device is significantly more efficient than the Powerex device, which can serve as a reference for expected performance. As can be seen from Figure 123, the Powerex IGBT module has a ΔT of approximately 40 ℃ at full power, which indicates that the Powerex module would be applicable to the converter, yet, as the efficiency is nearly 1 % lower than the Infineon device, it is expected that the Infineon device will result in even lower temperatures, which was supported by the thermal imagery.

Temperature Rise of IGBT (Buck Mode 600V - 300V)
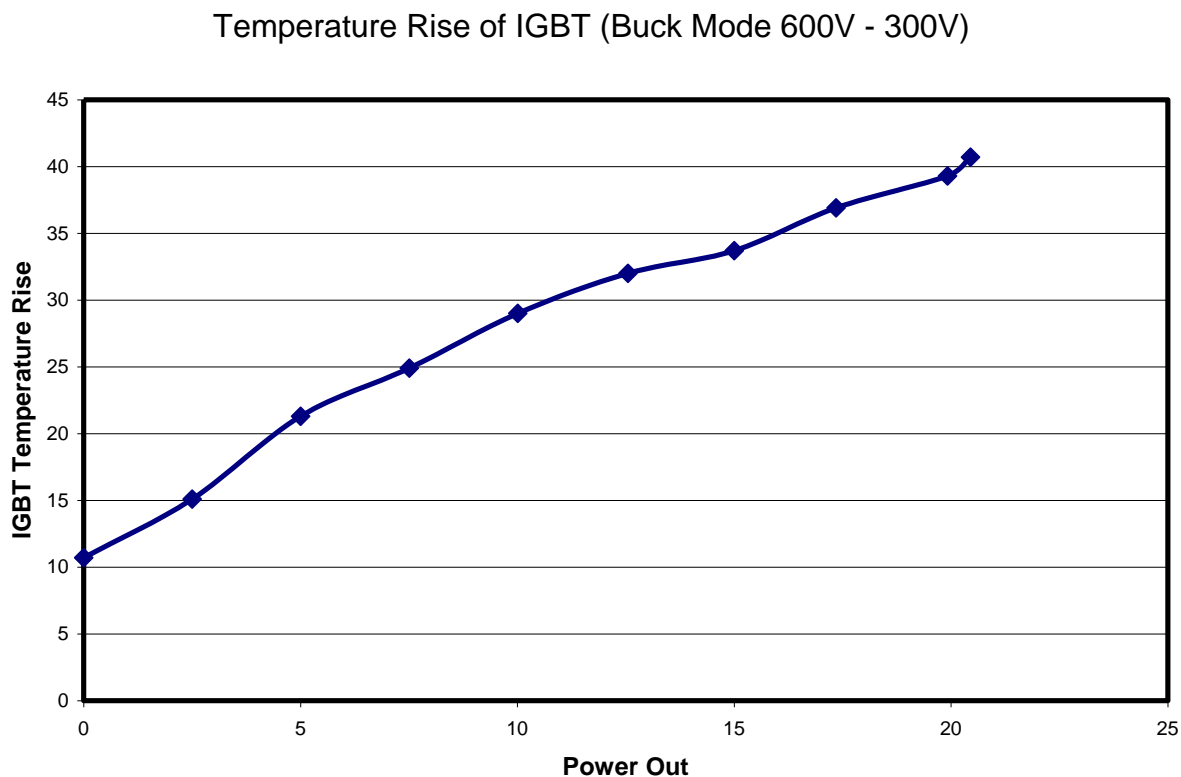
Figure 123 Temperature rise of Powerex CM300DX-24A IGBT die (80C coolant)

Another important efficiency goal is to achieve high efficiency at light load. Specifically, the goal was established for the 8-module DC-DC converter to exceed 92% efficiency at 5 kW, which represents only 2.5% load. Achieving such high efficiency at such light load is a major feat, which has significant benefits to the HEV field, as the majority of the time the converter is running it is operating at light load. A converter which achieves high peak efficiency but has low light load efficiency is not particularly useful to modern electric vehicles, which are constantly operating in transient modes and low power modes. In order to achieve the specified efficiency for the entire system, we will have to disable modules at lower power. Based on the initial efficiency data, the converter will be able to operate with light-load efficiency high enough so as to always allow two modules to run, so as to reduce the complexity of the phase scheduling scheme.

High Temperature Film Snubber Capacitors

Before a custom film capacitor snubber could be designed, it was important to determine the ideal snubber capacitance. More efficiency testing was done to determine the right snubber capacitance value for the Infineon IGBT. A total snubber capacitance of 400nF (200nF per IGBT) was compared to 300nF (150nF per IGBT). The light blue and red curve in Figure 124 were obtained by using the minimum negative turn-off current which is just enough to allow for zero-voltage turn-on and is different depending on the snubber capacitance value. On average, the 400nF setup gives a slight benefit over the 300nF setup. But this small efficiency gain is not enough to justify the increased RMS-currents in the system and larger physical size of the snubber capacitors, especially because the maximum efficiency numbers are already in the target range of 97 to 98%.

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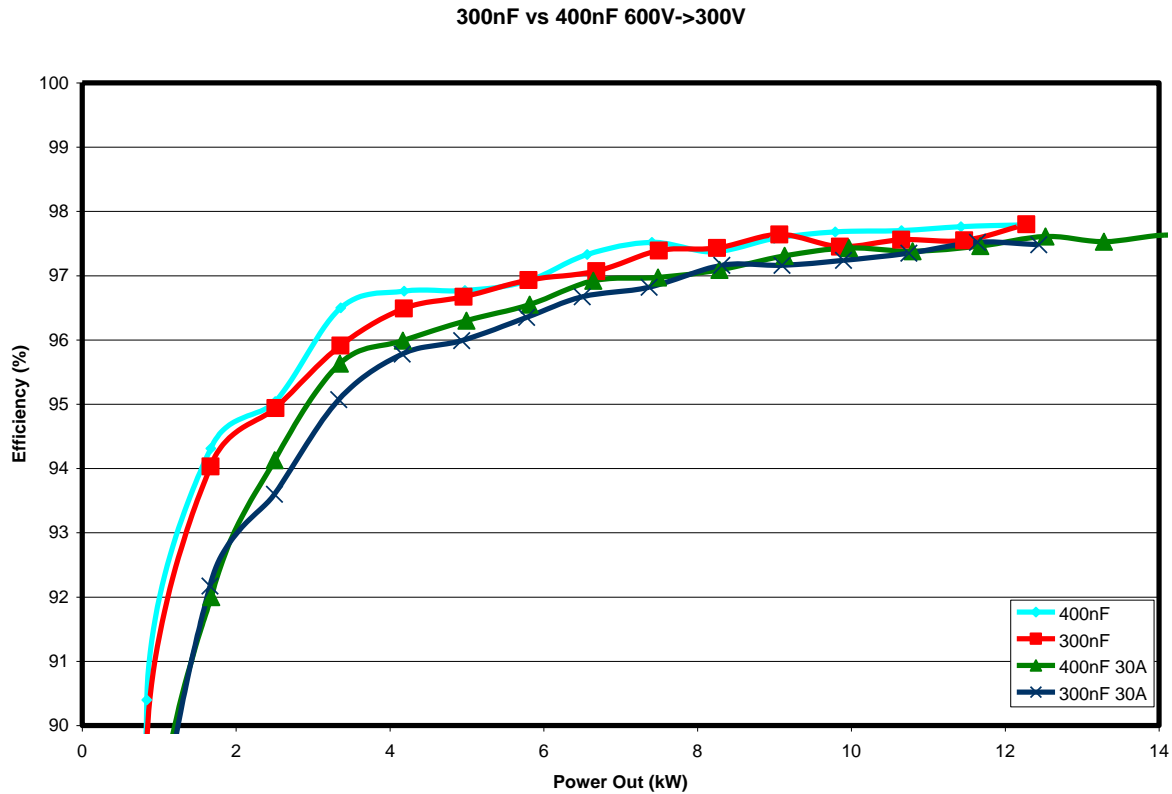
Figure 124 Efficiency comparison for different snubber capacitance values and turn-off currents

Additionally a test was done with a higher static turn-off current of 30A for both cases. It can be seen that the efficiency difference between the minimum and 30A turn-off current for both snubber capacitance values is more significant than the difference between the 2 snubber capacitance values at the same turn-off current. Therefore it can be concluded that in the final stage of the project the system efficiency can be optimized by fine-tuning the negative turn-off current to a minimum value just big enough to keep the converter running safely with zero-voltage turn-on of the IGBTs. Based on collaboration with the capacitor manufacturer, a snubber capacitance value of 160nF per IGBT was chosen as a good compromise between efficiency and physical size.

The snubber capacitor is critical to implement the variable-frequency soft switching topology. For maximum efficiency, the snubber capacitor should be designed for low equivalent

series resistance (ESR) and equivalent series inductance (ESL). This performance is available with standard polypropylene snubber capacitors, but polypropylene is not stable over 105°C, which would not be reliable for long term use, since the coolant temperature is 100°C, and there will be some self-heating of the capacitors. For the ESC DC-DC converter prototype, special silvered mica capacitors were developed, which performed very well, but were costly due to the high cost of mica. For this converter, in keeping with the theme of using commercially available components, the goal was to use capacitors which are commercially viable in addition to offering high performance. Polyester capacitors are available with 125°C ratings, but they have higher dissipation factor, and would not be suitable for the current stress. To solve this problem, collaboration with a film capacitor manufacturer Aerovox was initiated. With the goal of achieving performance close to polypropylene with 125°C working temperature, Aerovox was able to design a proprietary structured capacitor which utilized a hybridization of materials, allowing the capacitors to have low ESR, high current handling capability, and higher operating temperature. The full power current ripple was simulated, as shown in Figure 126 and Figure 127, and it was determined that the RMS current rating of the capacitor should be greater than 20 Arms at 15 kHz for safety. Based on analysis and testing, it was determined that the proprietary capacitor design achieves the desired performance.
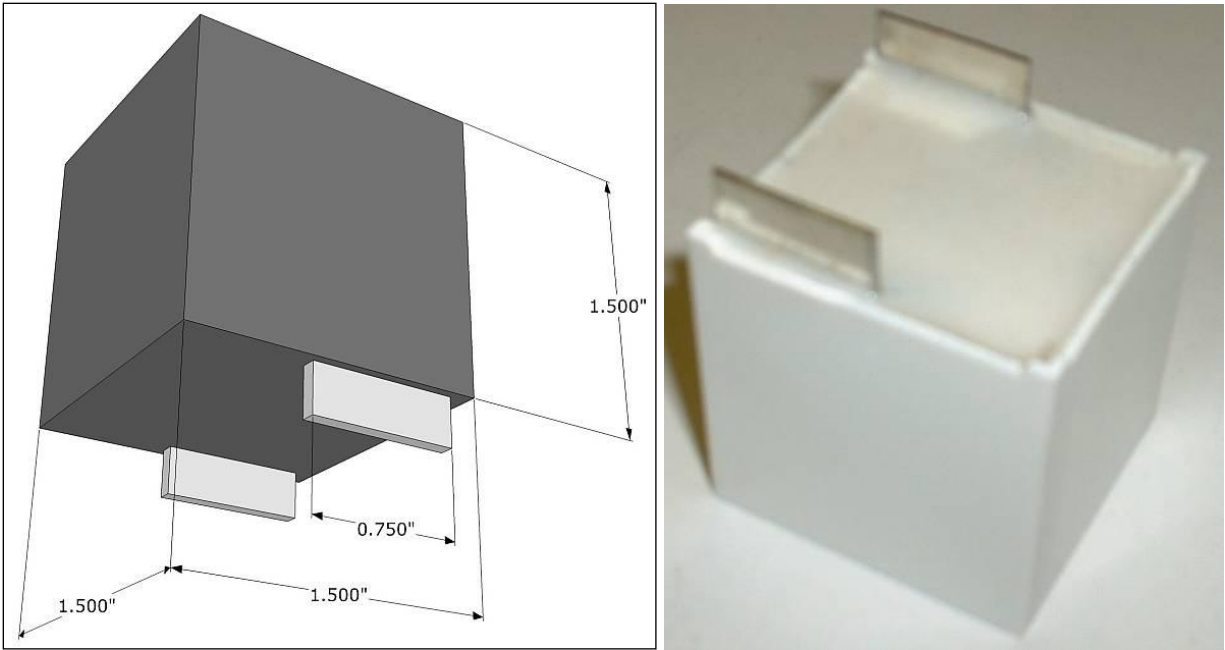
Figure 125 Prototype film snubber capacitor

Capacitor dimensions:
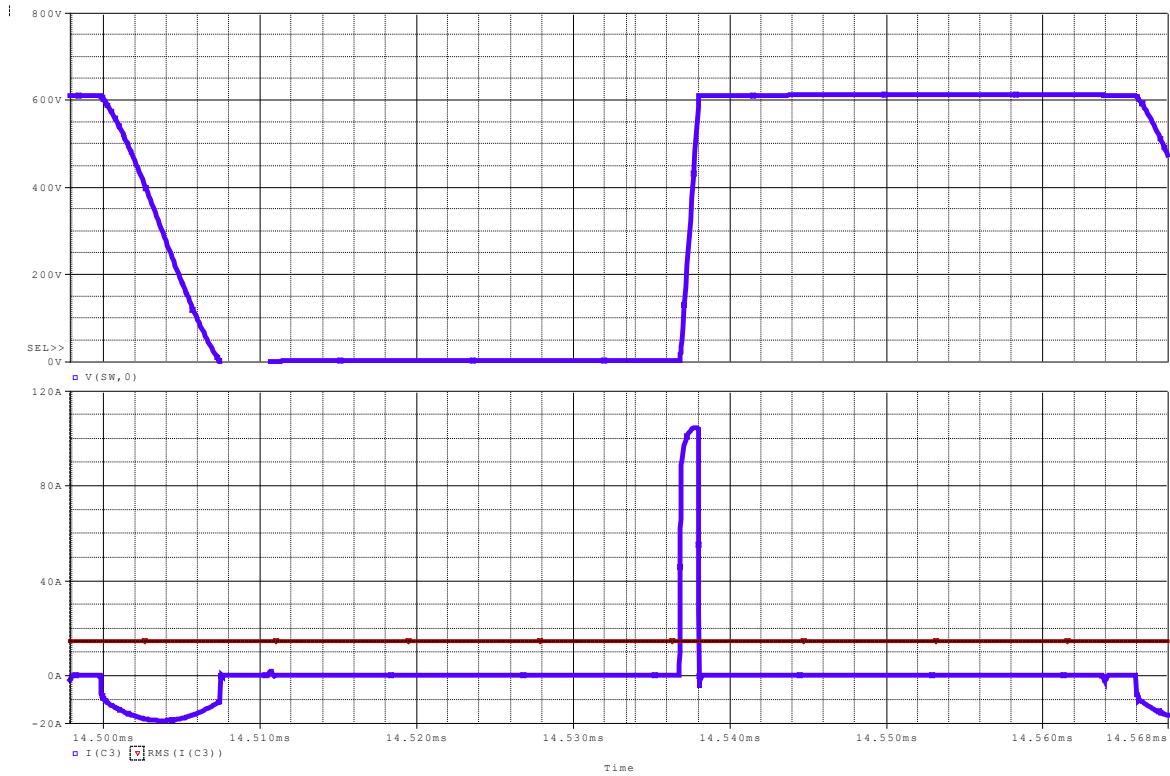
Length: 1.5"

Height: 1.5"

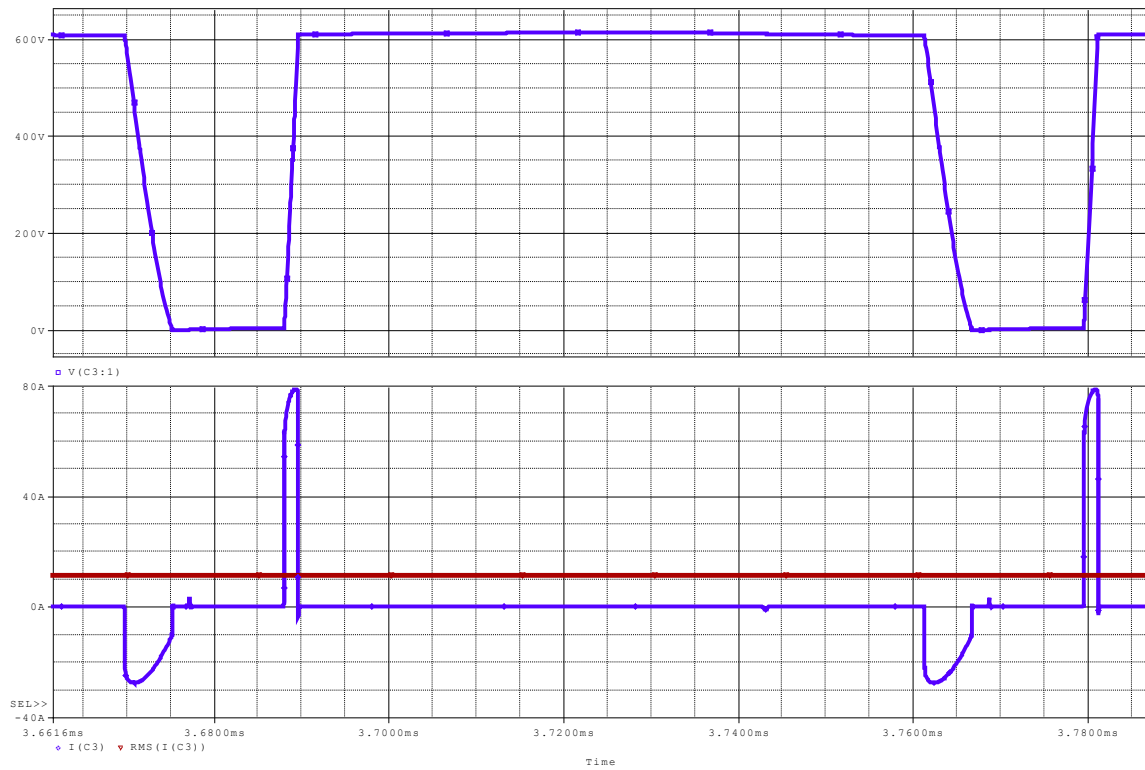Width: 1.5"

Specifications:

Capacitance = 200 nF

Operational current > 20 Arms

VDC rating: 1200V

Temperature rating: 125°C (working), 100°C (ambient)

Figure 126 Snubber capacitor waveform 1 (15 kHz, 14.6 Arms)

Figure 127 Snubber capacitor waveform 2 (12 Arms, 11khz)

The snubber capacitor is critical in this design, since the soft-switching operation is dependent on the snubber capacitor having low ESR, low inductance, and high reliability. The capacitors are specially designed to offer performance similar to polypropylene capacitors, with a higher operating temperature of 125ºC. During testing the capacitors were found to operate very well; they exhibit low loss, and stay relatively cool. Also, the tolerance between the capacitors was within 2%, which is acceptable. Experimental results have shown that the temperature rise of the capacitor is low, and that the long-term reliability will be on-par with traditional polypropylene capacitors. The snubber capacitor has been slightly modified to fit on our currently existing power board (see Figure 128). Thermal testing results show that it performed very well.

To test the capacitor, the converter was operated in buck mode from 600V to 300V with no load and with about 20% of the full load. Full load doesn't necessarily have to be tested, since the RMS current through the snubber capacitor is approximately constant from no load to full load because of the soft-switching, variable frequency converter. The reason is that the snubber capacitor ripple current increases, but the switching frequency decreases with increased power, leading to an almost flat RMS current curve over the full power range. The steady-state temperature of the snubber capacitor was about 39 °C (see Figure 129), which is 15°C above ambient, which should keep the capacitor under 120 °C with high temperature cooling.

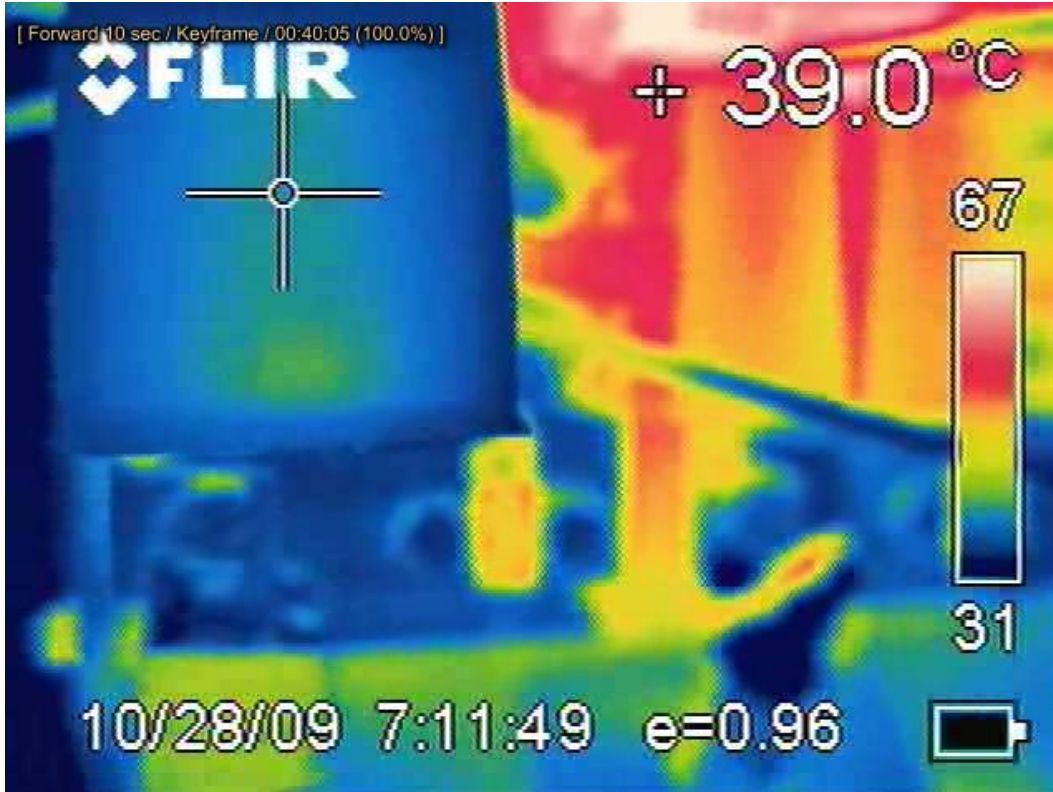**Figure 128 Test setup to evaluate new snubber capacitor**

Figure 129 Snubber capacitor thermal testing, 25 ºC ambient

In addition to the experimental testing with the converter, the capacitor manufacturer also completed tests with a batch of the newly developed capacitor. Measured parameters were the capacitance, DC breakdown voltage, and dissipation factor both at room temperature and 125°C. The absolute capacitance is 160nF and only drops by a maximum of 4% at 125°C. The DC breakdown voltage is in the range of 7.9kV at room temperature and around 5.7kV at 125°C which leaves a very large dielectric safety margin indicating a long life at 125°C operation. The dissipation factor has an average value of 0.018% at 120Hz and 0.034% at 1kHz. Furthermore, the capacitors were tested for capacitance and dissipation factor at room temperature, heated to 125°C for 2 hours, and then cooled back down to room temperature and re-measured. The results demonstrate that there is no detectable permanent change to the capacitor's electrical properties as a result of 100°C temperature swings. The snubber capacitors were tested substantially in the final 200 kW DC-DC converter, and were found to perform flawlessly.

Power PCB Design

The design and layout of the 100 kW 4-module power board is important for the overall performance and density of the converter. Since so much power will be processed in a single PCB, it is critical that the current paths in the PCB are properly designed for the expected operating conditions. The board is a 4-layer FR4 PCB, with 6oz (0.21 mm) copper on all layers, and 2 oz (0.07 mm) of additional plating on the outer layers. This results in an overall board stackup of 8/6/6/8oz copper, with the total board thickness being 0.125 inches. The additional 2oz of plating is to plate the many vias needed to pass current between layers. The power PCB must assume the role of a laminated bus bar in some respects, while also allowing the layout of the sensing and driving circuitry. The output and input capacitors are AVX FF3 polypropylene capacitors. There are four 13 uF 900 V capacitors for the high voltage bus, and five 20 uF 700 V

capacitors for the lower voltage bus. The PCB is designed in a way which allows the low voltage bus to connect to the board on either side, depending on how the bus capacitors are populated. This allows the two 100 kW converters to be placed in the same enclosure, with the power connections entering from the center on the same side. The schematics, layout, and pictures of the power board can be seen in Figure 130 to Figure 135. The power PCB was initially tested with only 2 IGBT modules to verify operation. The initial testing setup is shown in Figure 136 which is using all of the final components including the Infineon IGBT FF300R12ME4, the power inductor, the snubber capacitors, the cold plate setup and the controller boards.
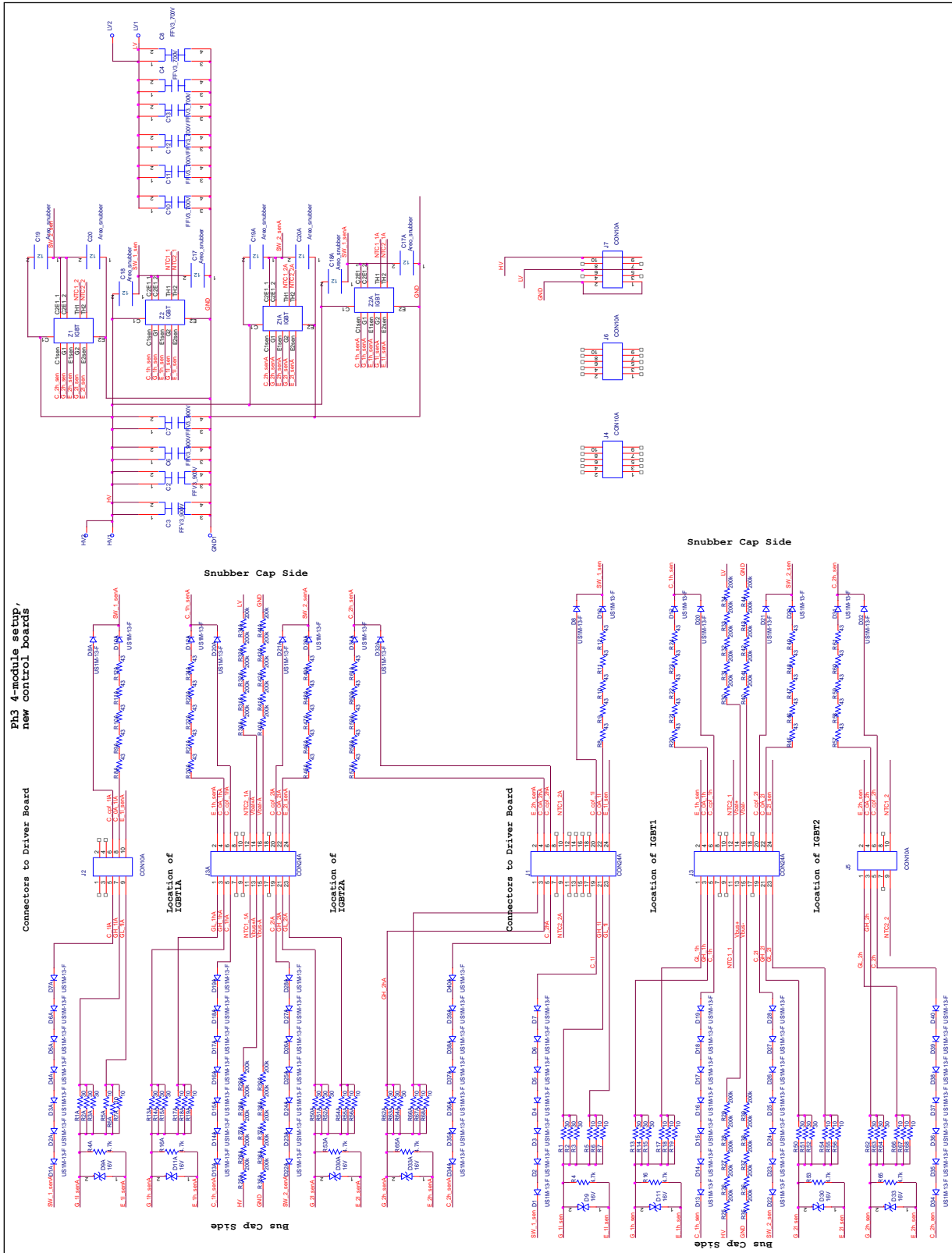
Figure 130 Schematics of new power board

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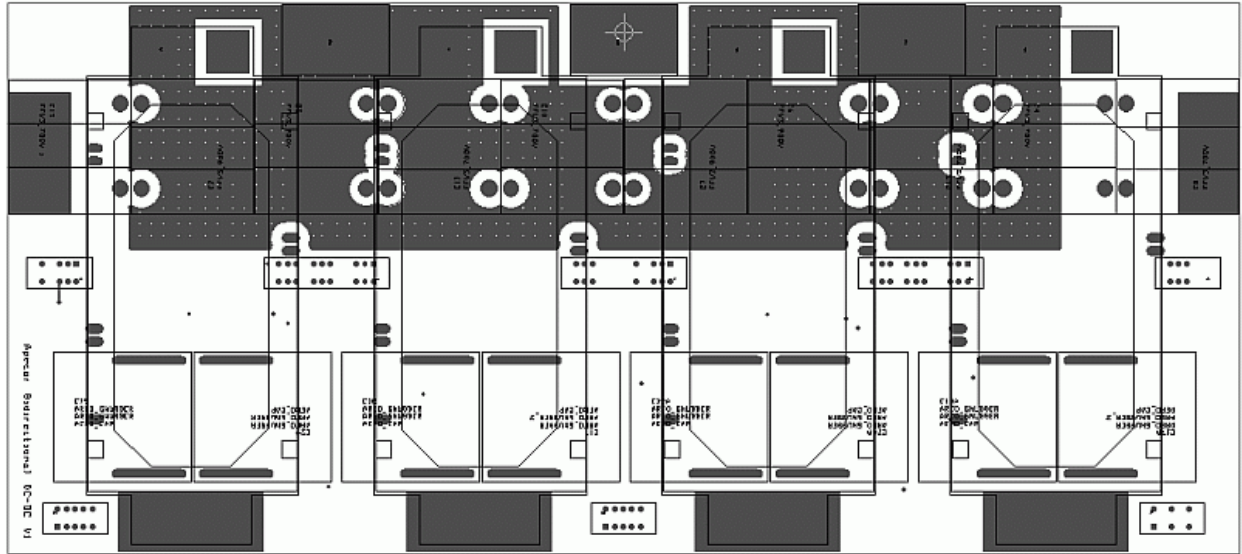
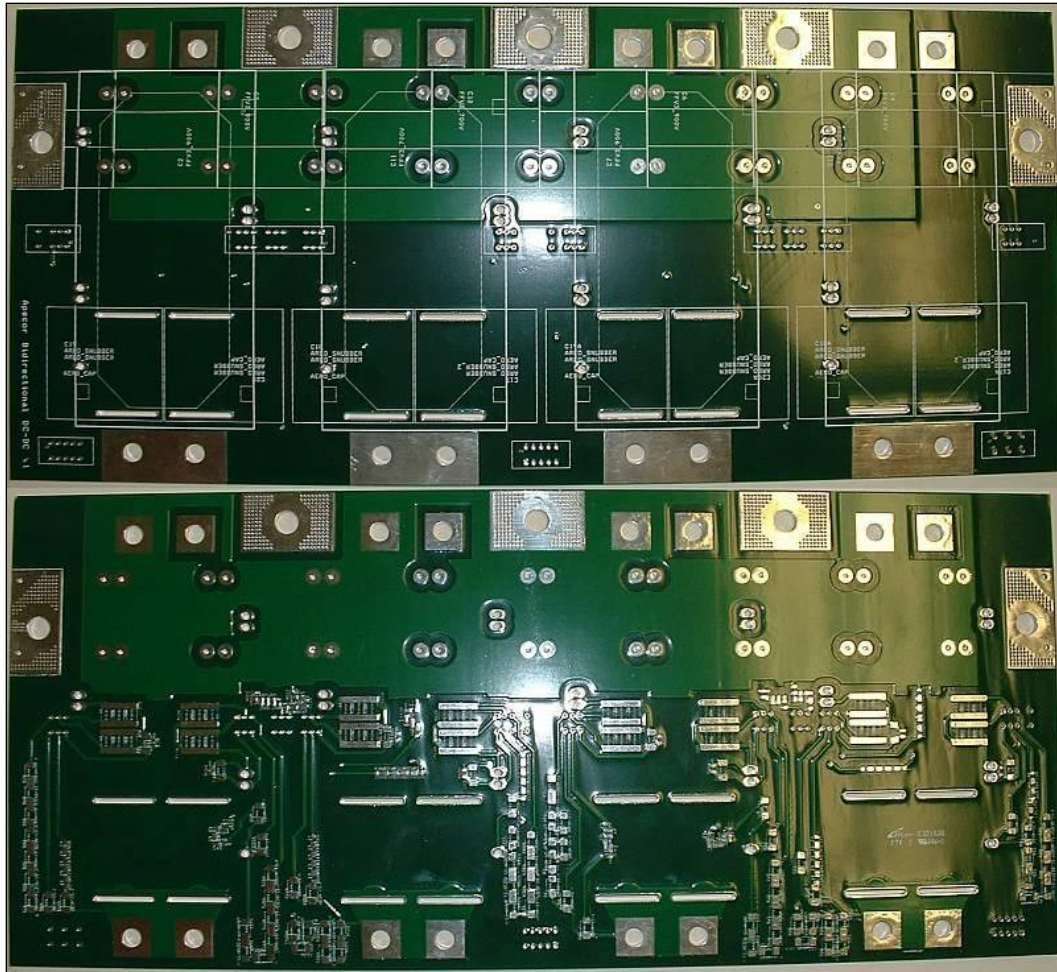**Figure 131 Top layout and components of new power board**
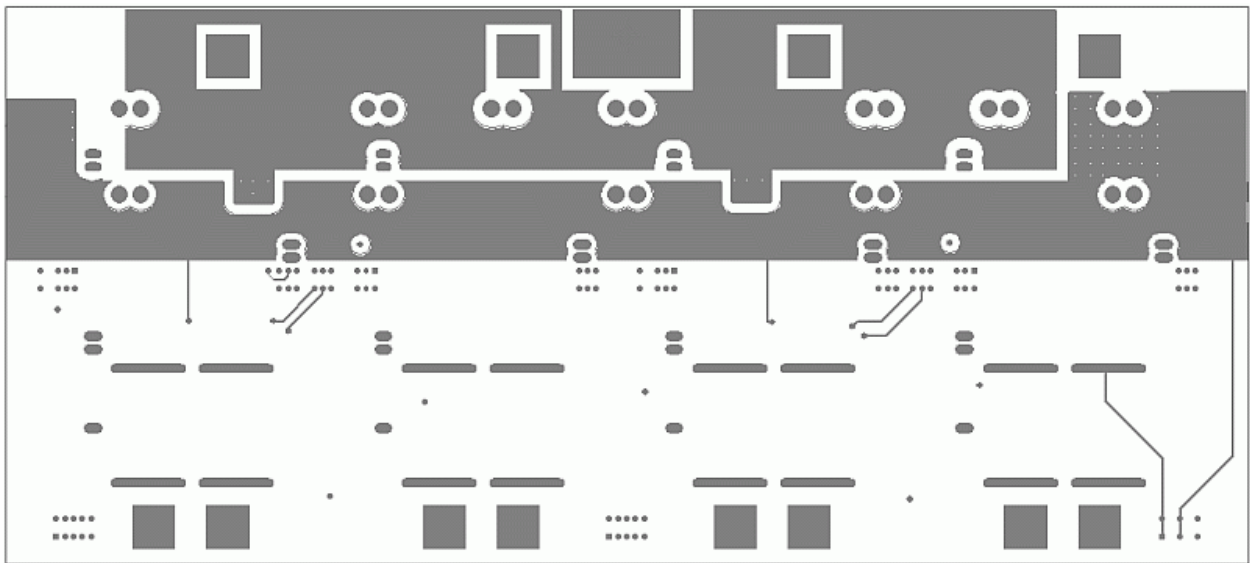
Figure 132 Inner 1 layout of new power board
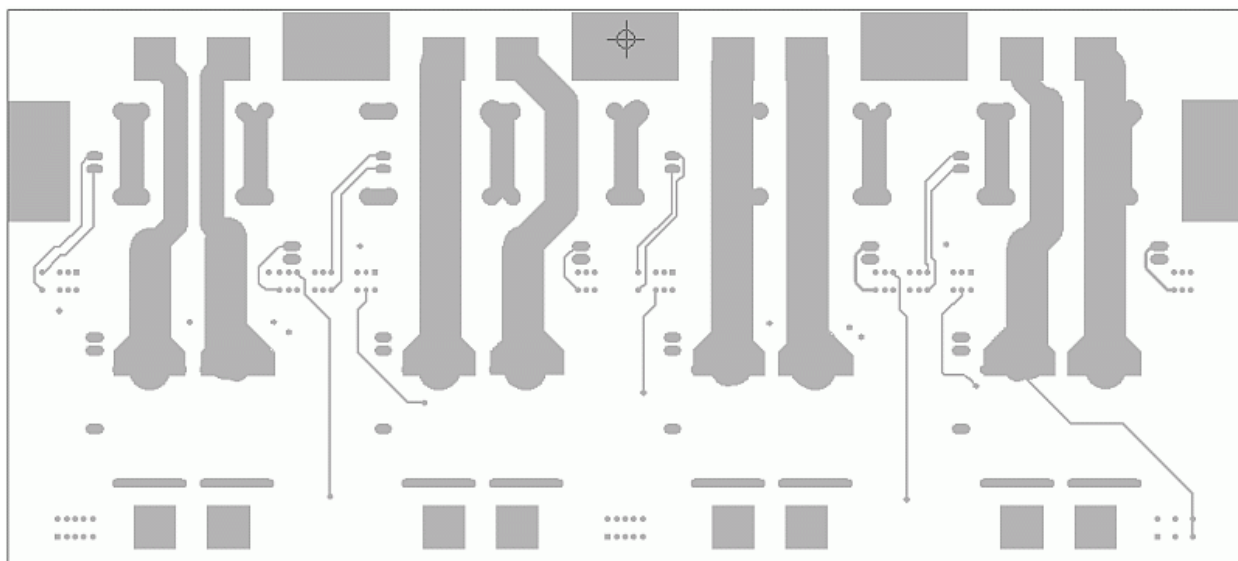
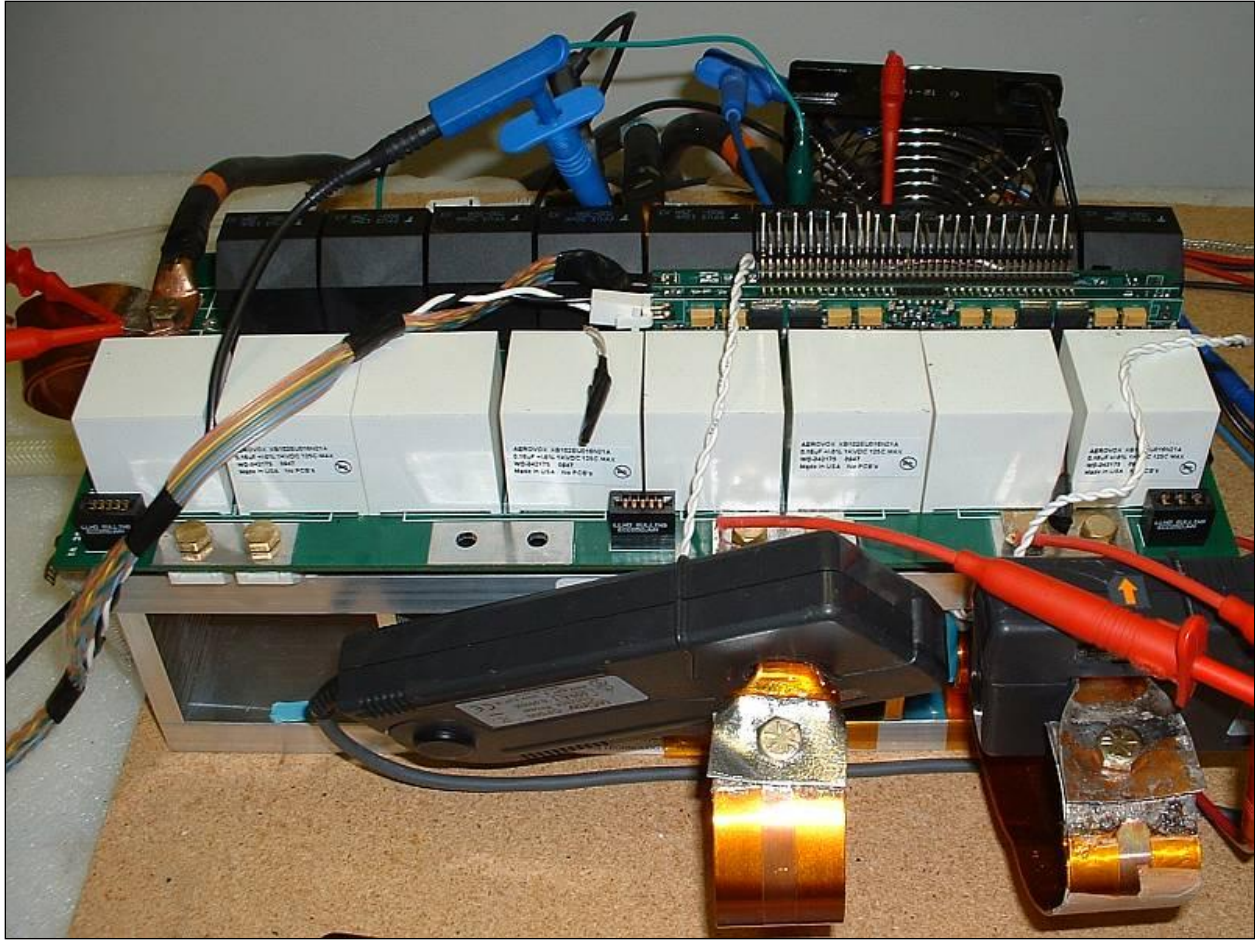**Figure 133 Inner 2 layout of new power board**
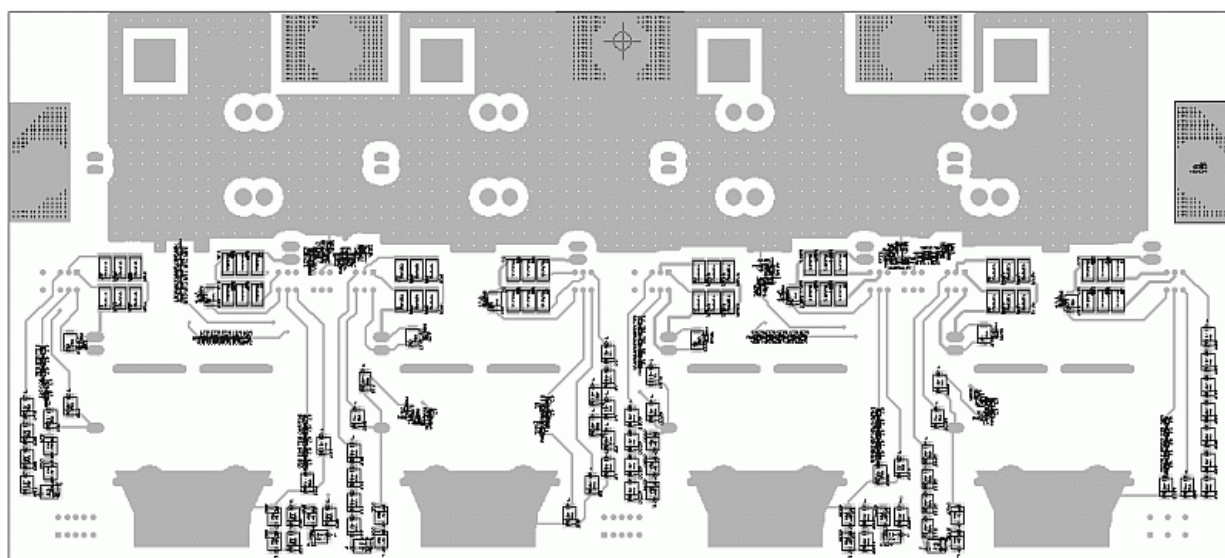
**Figure 134 Bottom layout and components of new power board**

Figure 135 100 kW 4-module off-the-shelf power PCB (top and bottom side)

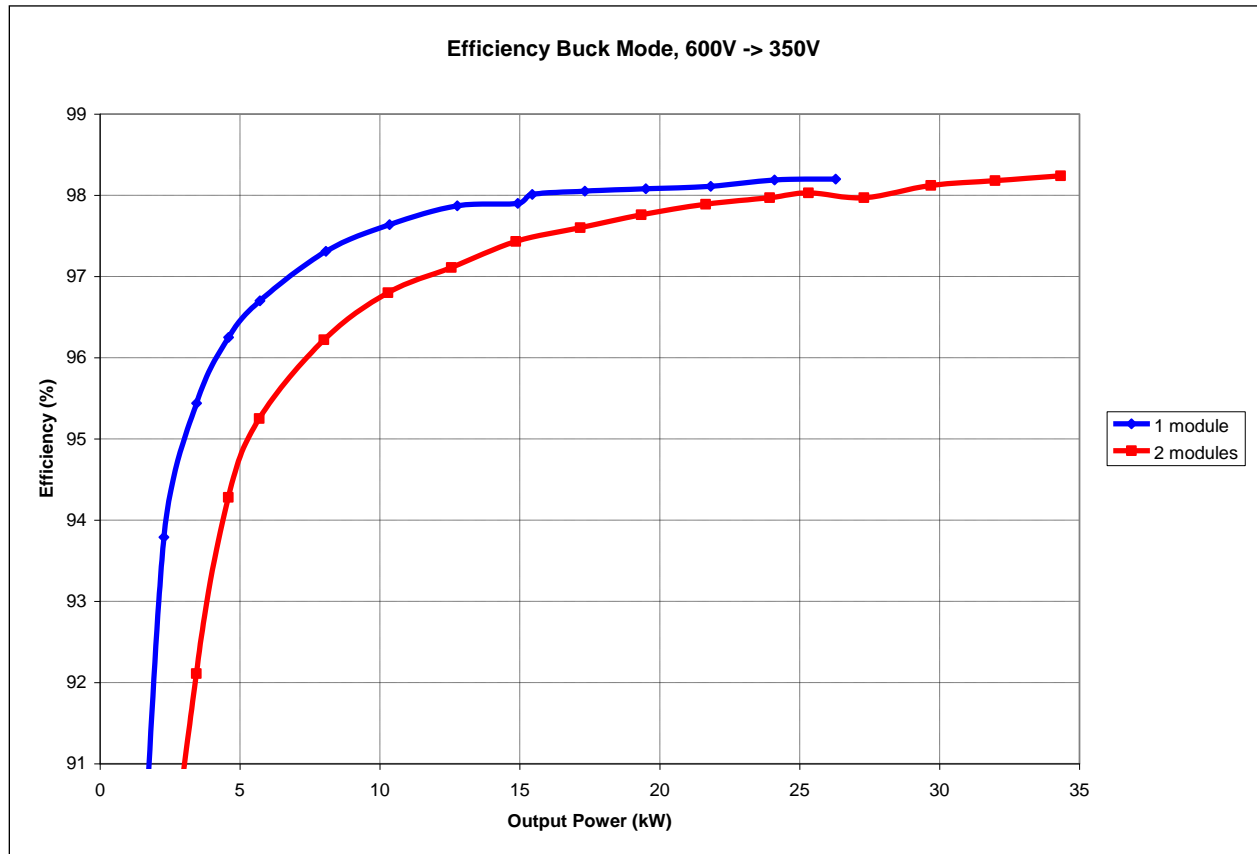**Figure 136 Initial power PCB testing setup**

In the power testing setup in Figure 136, the 2 power stages on the right are fully assembled with the inductors placed in their respective place inside the cold plate. The IGBTs (not visible) are mounted between the cold plate and power board. The (white) snubber capacitors are placed in one row on the front side, the battery and bus capacitors (black) can be seen in the back. The driver-control assembly is placed in the middle between the 2 capacitor rows. The communication board (not shown) will be placed in front of the snubber capacitor row. The power connections are made on the back and the left side of the board. Additionally, extra conductor pieces have been added to the inductor wires to allow for oscilloscope measurement.

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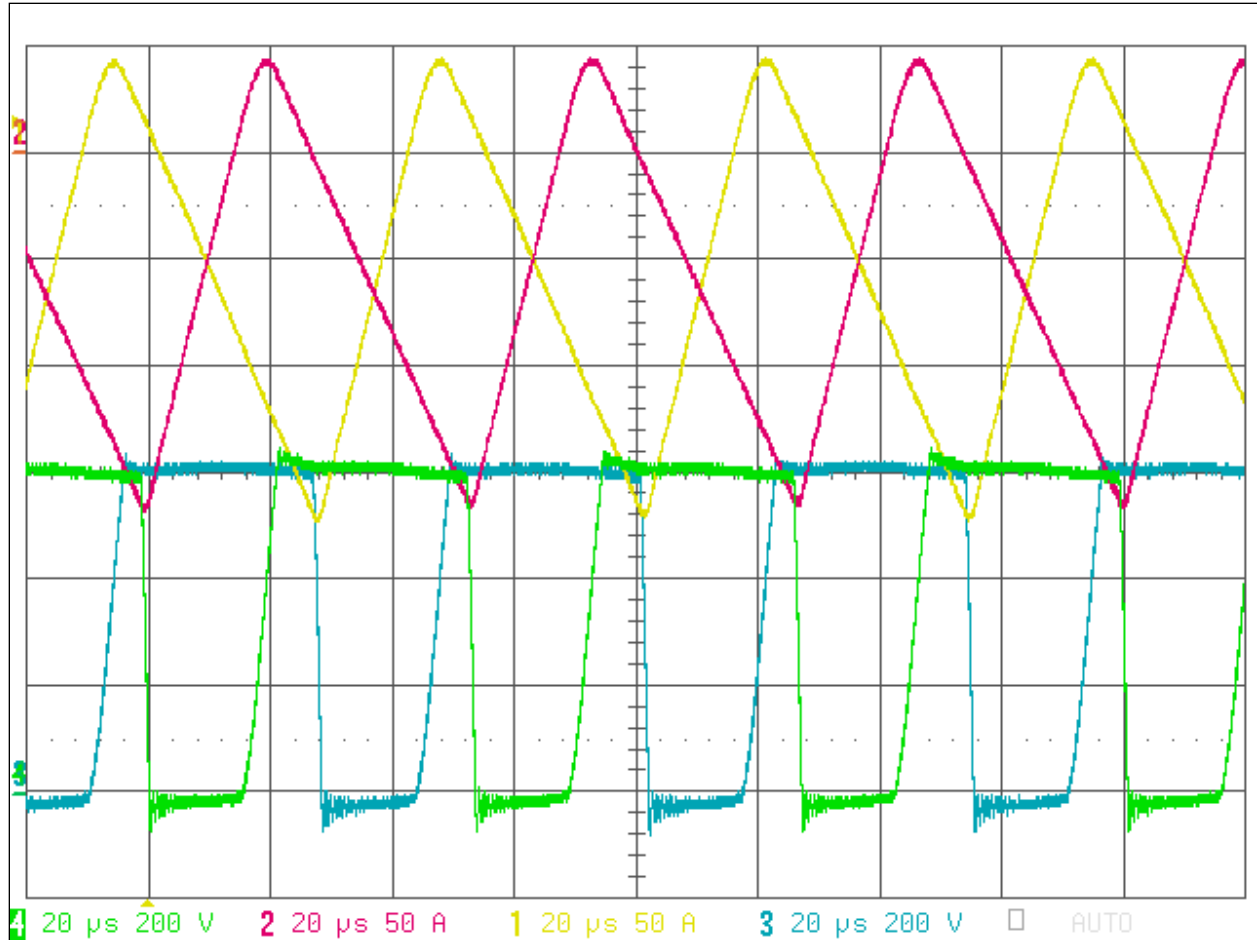
Figure 137 Switching waveforms, Buck mode, 2 interleaved stages, 600V to 370V, 46kW

(#1,2: inductor current; #3,4: switch node voltage)

For initial testing, the water cooler was connected to the system and 2 interleaved power stages were operated with up to 52kW, 1 stage was running with up to 26kW which is already above the final requirements for one stage. Respective switching waveforms have been recorded at 46kW power and they can be seen in Figure 137. Furthermore efficiency measurements using a calibrated efficiency measurement setup were captured for a single and both power stages running, and the efficiency is very good and within the expected range, in some conditions exceeding 98%, as shown in Figure 138.

Figure 138 Efficiency of initial power PCB testing

Custom Pin-Fin Liquid Coldplate

The DC-DC converter features 8 IGBT modules, which are mounted on liquid cooled pin-fin type coldplates. The coldplate assembly is actually two coldplates, which are joined by aluminum dividers, which create channels for the inductors to be mounted within, allowing the top coldplate to cool the IGBTs as well as the inductors, and the bottom coldplate cools only the inductors. To assure good thermal performance, as well as mechanical stability, the inductors are potted with a thermally conductive epoxy. Each inductor wire is pre-fitted to the power PCB, as well as the front panel connector, to make sure that after potting, the entire assembly will fit properly. The designed 4-module coldplate is shown in Figure 139.

Figure 139 Coldplate Assembly

The IGBT modules are manufactured by Infineon, part number FF300R12ME4. The IGBTs are rated for 300A and 1200V, with a maximum die temperature of 175°C. The modules are screwed to the coldplate, and have a thermal paste to decrease the thermal impedance between the IGBT and the coldplate surface. To decrease the thermal impedance, a fairly high performance thermal paste, Keratherm KP93, is applied in a very thin layer, so as to even out the surface roughness between the coldplate and the baseplate, without adding additional thermal insulation.
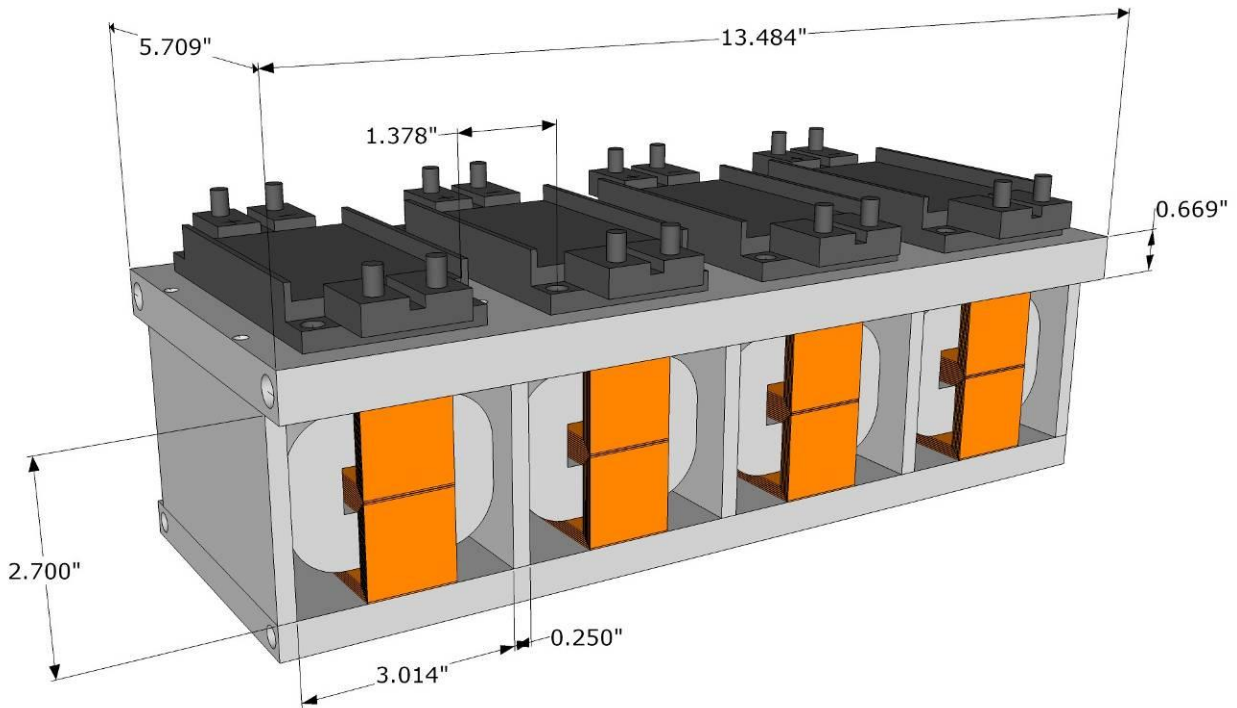
**Figure 140 3D Model of Coldplate Assembly w/ IGBT Modules and Inductors**

The converter is designed to use two 4-IGBT module converters to achieve the target power level of 200kW. Each 100kW module has a single coldplate assembly, which cools the 4 IGBT modules, as well as the accompanying inductors. The upper IGBT coldplates use pin-fin cooling channels, which have been designed to have high cooling performance with minimal flow rate and pressure drop. The bottom coldplate is intended to assist in cooling the inductors, which will be encapsulated in potting material. The bottom coldplate features cooling channels, which make 2 passes across the length of the coldplate. Since the necessary cooling power of the bottom coldplate is considerably less than that of the top coldplate, this design is chosen to reduce pressure drop in the system, allowing the coolant to flow much more freely.

The coldplate design was created to match the mounting requirements of the IGBT modules, the power PCB, and the width of the inductor cores. The vertical aluminum plates also serve to conduct heat from the sides of the inductor cores to the liquid coldplates. The thermal

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analysis for the cooling of the inductors was performed in the nanocrystalline inductor calculator, found in the Appendix. As shown in Figure 141, the dimensions of the coldplate assembly were generated, in addition to the development of the 3D model. Once the dimensions of the coldplate were determined, the design was delivered to a coldplate manufacturing company, MaxQ technologies. The manufacturer produced the custom coldplate to use their proprietary pin-fin cooling interface, which exhibits good thermal performance with low pressure drop. The pressure drop and thermal impedance of the top coldplate is shown in Figure 142.
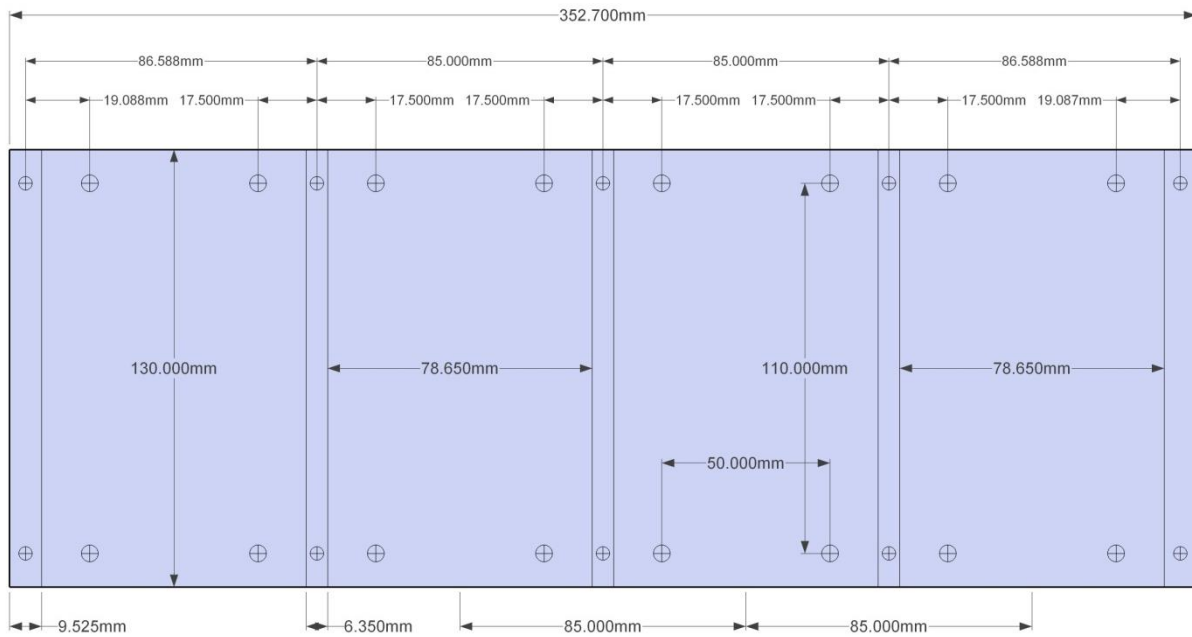
Figure 141 Coldplate Dimensions
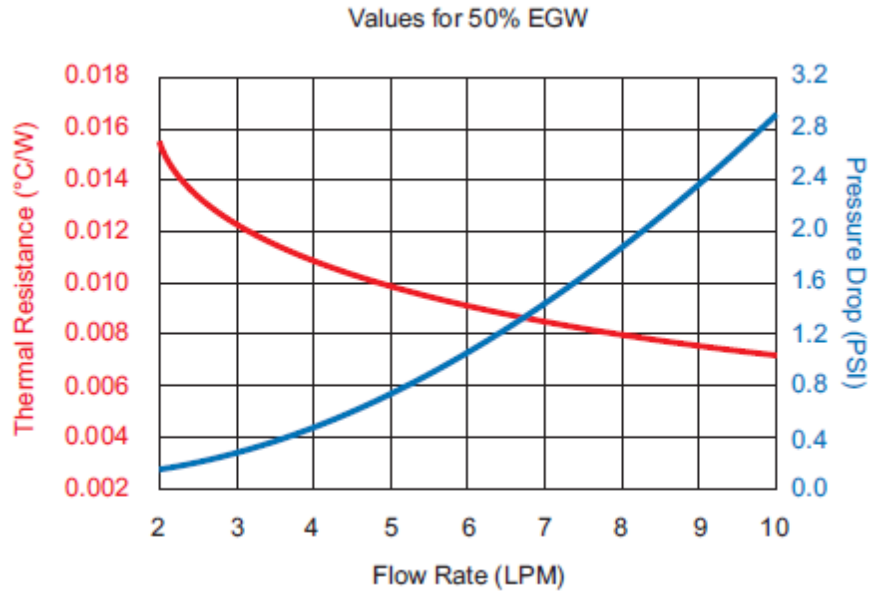
**Figure 142 Expected Performance of IGBT Coldplate**

The converter is assembled into the sealed aluminum enclosure, starting with the coldplate assembly, then the IGBT modules, mounting the power PCB, then by inserting the driver/controller boards into the card-edge connectors. The coolant hoses and fittings are connected throughout the process, as the enclosure is fairly cramped, and the hoses would be in the way of tools if they were assembled first. The assembly process can be seen in the following figures.

Integrated Controllers/Drivers

The structure of the power PCB was designed in such a way that the driver and controller boards interface through card edge connectors, which allows for the easy removal of the controllers during debugging and testing. The controller/driver module is actually a sandwich of 3 PCBs, which mate together, to make a single module which controls two IGBT modules. Unlike the ESC DC-DC converter prototype, which had a single controller module per IGBT, it was apparent that the overall reliability would increase by only having to manage the

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communication and interleaving between four controller modules opposed to eight. The master controller and communication PCB spans the length of the prototype, coordinating the behavior of the individual DC-DC converter controllers through an internal CAN bus, and communicating with the vehicle master controller or the USB PC control interface.

The controller modules integrate the isolated bias power supply circuits, the driver circuitry, and the digital controllers, which is implemented with a DSP and CPLD. The master communication and control board also features a capacitor precharge circuit, which charges the high voltage bus capacitor to 50 V greater than the battery input voltage before the converter is activated, as described in Chapter 3, this is necessary to allow the converter to begin the soft-switching resonant operation. The communication and master controller board is shown in Figure 143. The exploded view of the controller module is shown in Figure 144, with the assembled controller module shown in Figure 145.
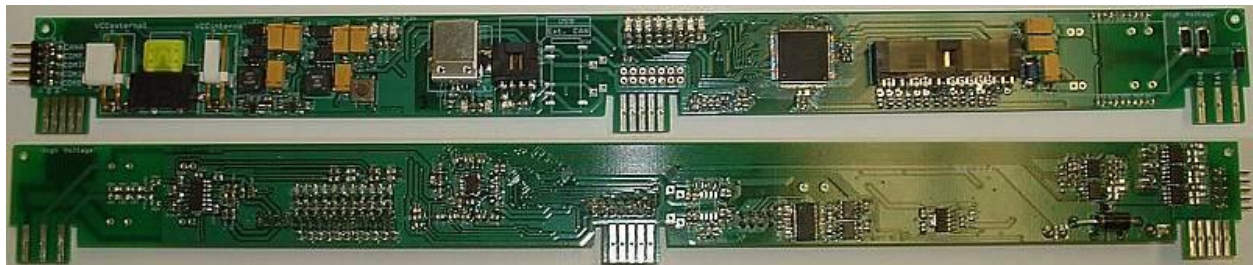
**Figure 143 Picture of communication board (top and bottom side)**
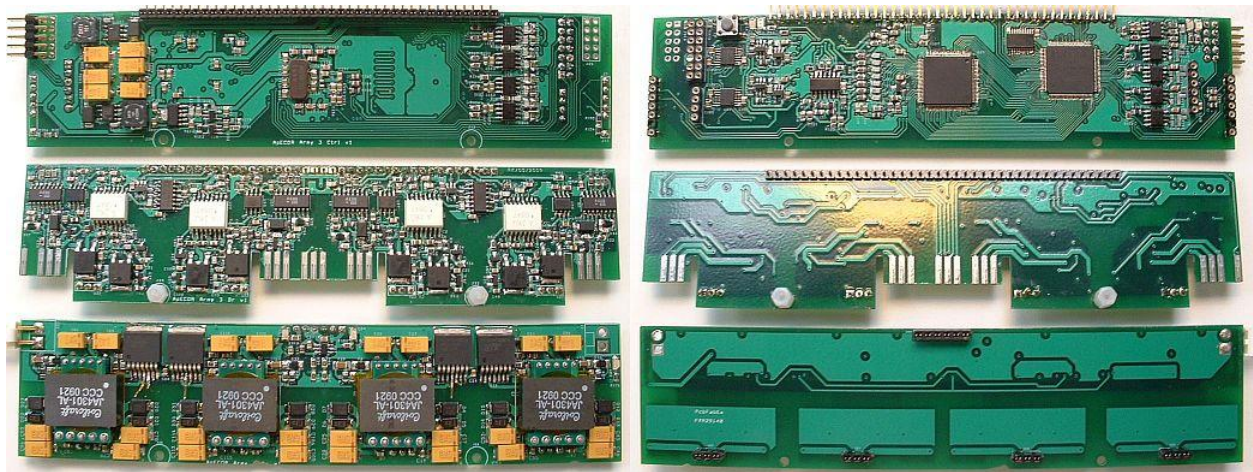
Figure 144 Picture of the boards with components (left: top side, right: bottom side, top: control board, middle: driver board, bottom: isolated power supply board)

Figure 145 Picture of full assembly (front: isolated power supply board, middle: driver board, back: control board)

8-Module 200 kW DC-DC Converter 3D Design and Assembly

During the course of the development of the 200 kW prototype, a 3D model was concurrently designed and maintained, so as to be sure that the design is optimal in terms of density, and that all of the components will fit together properly, as shown in Figure 146. Once the 3D model of the converter was complete, an aluminum enclosure was developed as a structural enclosure, as well as to act as a thermal heatsink at the top of the converter, serving to cool the capacitors and controller modules. The aluminum enclosure dimensions were sent to a sheet metal manufacturer to produce.
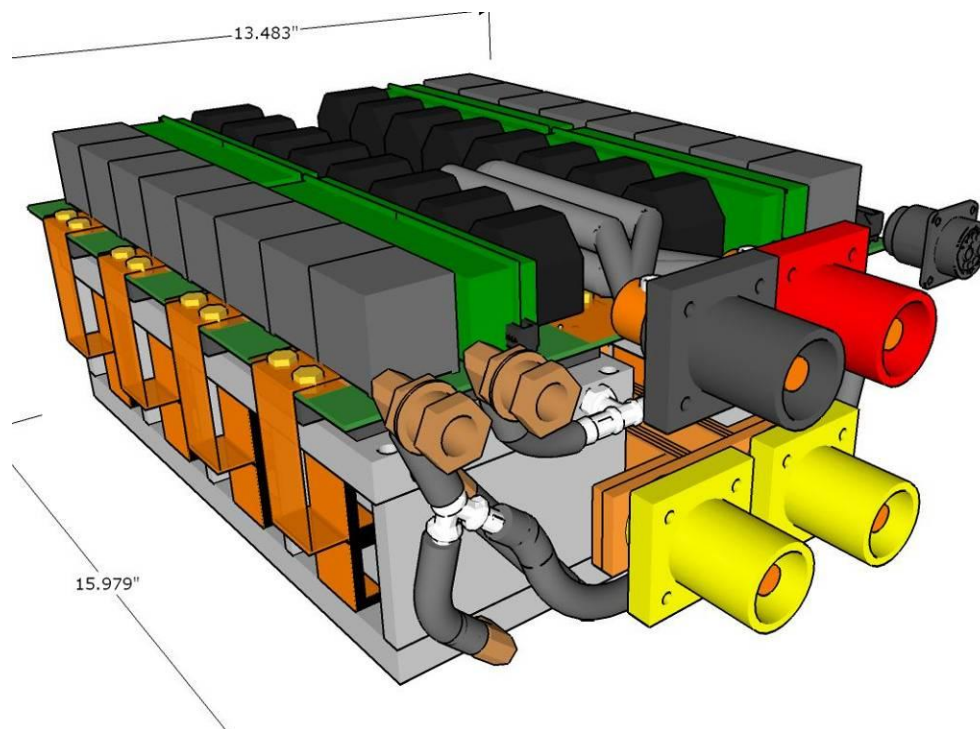
**Figure 146 3D Model of Assembly**

Connectors

The converter is to be enclosed with a custom sealed aluminum case, and will use sealed connectors for the power, signal, and coolant fittings. For the signal connector, there are a good number of choices available, of which a mixed power/signal connector from Tyco was selected.

This connector is sealed, rugged, and has connections for the 12V/24V auxiliary power as well as the CAN controller interface.

To accommodate the high power connections, the high-voltage connectors should be rated at over 350A, while the battery connection should be rated at over 700A. At this current level, it is difficult to find connectors meeting the requirements which are reasonable in size and cost. The connectors should also be rated for harsh environment operation, and capable of proper voltage isolation. After a good deal of searching, single pole connectors used in the marine industry were selected. These connectors would typically be used to power a large boat when docked on shore. The 400A conductors are solid brass, which offers very good weather resistance. The housing is a solid nylon plastic, which will offer good environmental resistance as well as voltage isolation. The voltage rating of the connectors is 600 VAC, which would have a sinusoidal peak voltage of 850V, satisfying the voltage isolation requirements. To handle the higher currents of the 300V input, two connectors are paralleled internally. Since the direction of the current through the ground for the high voltage and the battery connections are in opposite directions, it is ideal to have a single point ground connection, requiring the two power grounds to be paralleled before entering the converter, reducing loss and the need for additional power connectors.
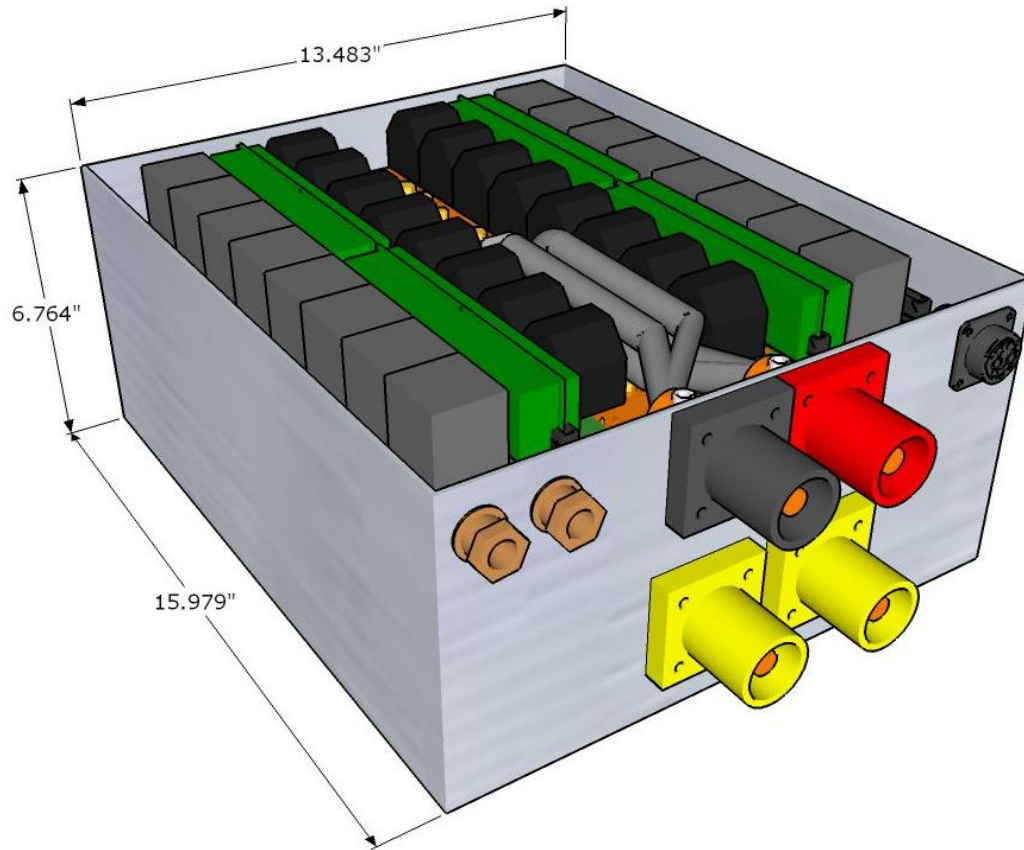
**Figure 147 Converter 3D model with enclosure and connectors**

High Current Internal Cabling

For the internal connections from the high-current connectors to the power PCB, flexible high-current cables are needed. Each connector will connect to 2 flexible 1/0 AWG wires, which will distribute power to each of the power PCBs. Although 1/0 wire is rated to accommodate over 240A, which is more than the 175A needed, the connection lugs are often not able to handle the required current, due to the additional interface between the copper strands and the lug. To combat this problem, the design will use custom fusion lugs, which are actually manufactured to press the copper strands of the wire into a lug shape, thus eliminating the downfalls of traditional terminations. The original design had two 90 degree bends, but after working with the manufacturer, it was determined that the additional cost for custom tooling wasn't worth the benefit. As such, the new design is to have a single 60 degree bend, and use the flexibility of the cable to accommodate for the bend to route the cable horizontally. This is shown in Figure 149.

The power cables feed directly into the ground and high-voltage connectors, where they are clasped with large set screws.
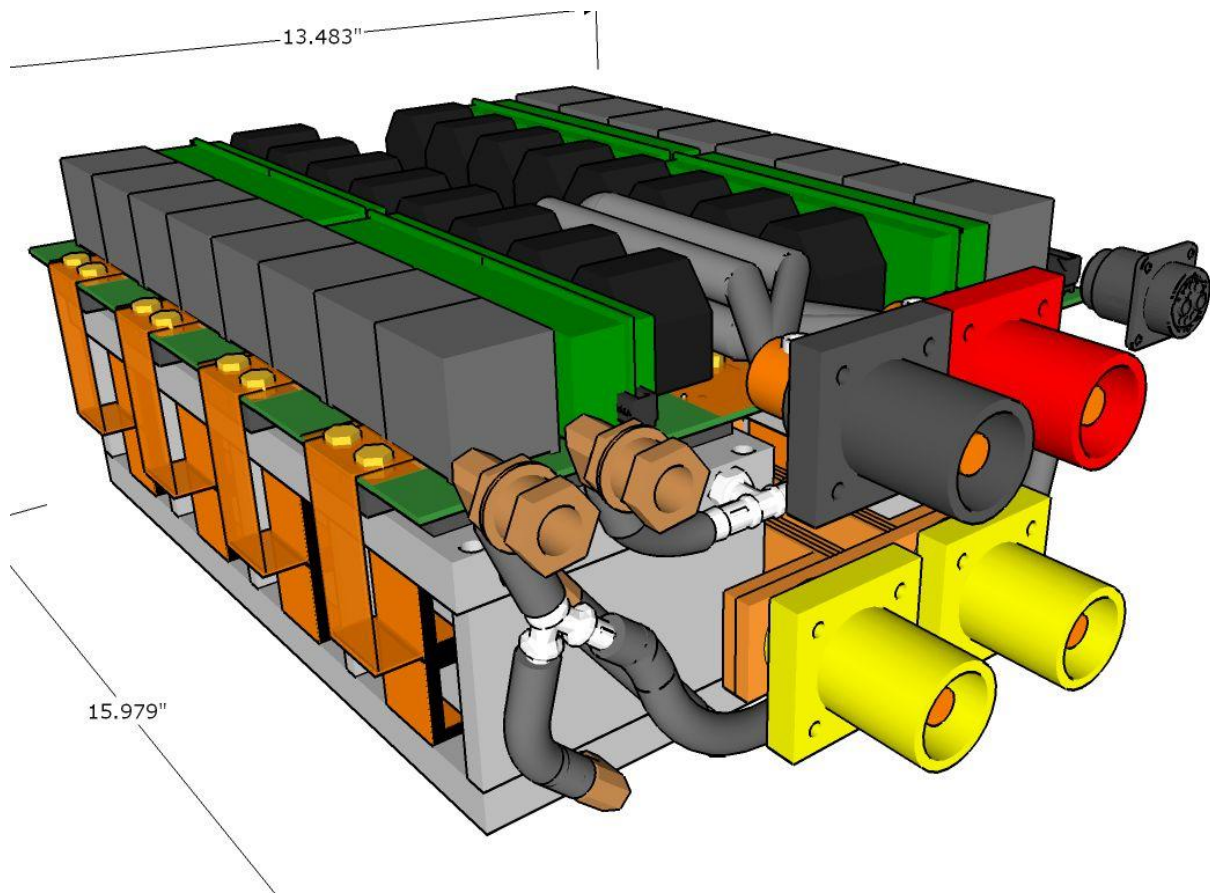

Figure 148 Cooling and Connector Assembly
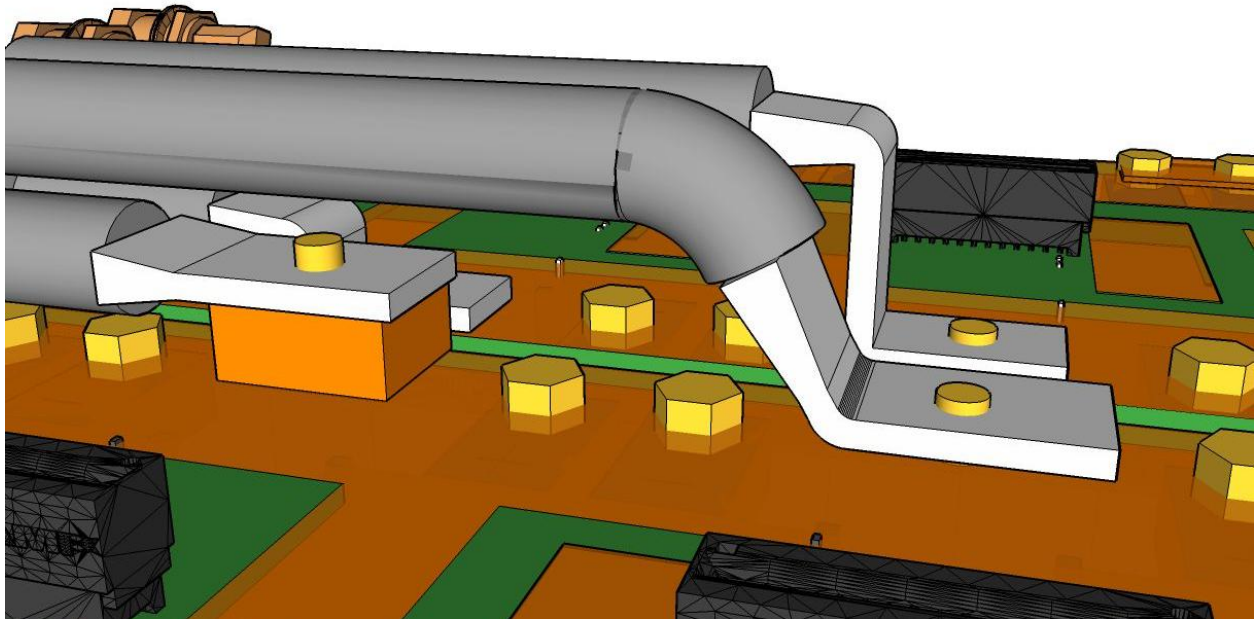
Figure 149 Fusion lug power cables (60º bend in front, abandoned 90º design in back)

As can be seen in Figure 148, the inductor wires which connect to the battery input voltage are run in parallel on the inside of the coldplate assemblies, and joined together at a single point at the input connector. This structure allows the interleaved current to substantially cancel before the filter capacitors are required to filter the current ripple, significantly reducing the voltage ripple at the input, and increasing efficiency.

Prototype Converter Assembly

This section documents the final assembly of the 200 kW DC-DC converter prototype. The first components to be inserted into the case are the coldplate assemblies, which house the epoxy potted nanocrystalline inductors, as can be seen in Figure 150. The copper foil inductor connections are then mounted to the copper mounting plate on the battery bus connectors.
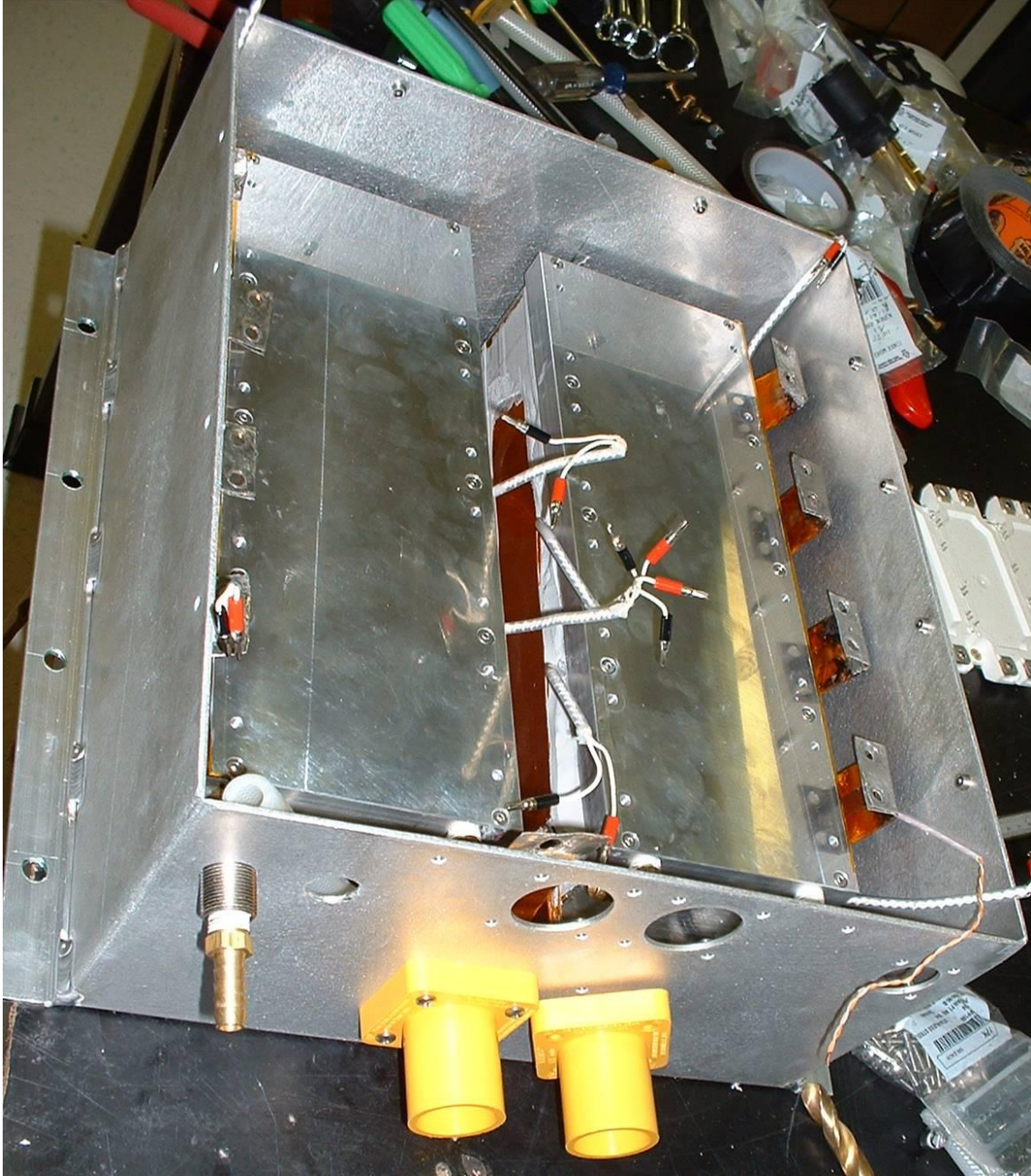
**Figure 150 Enclosure with potted coldplates and inductors**

Once the coldplate assemblies are mounted, the IGBT modules are screwed to the coldplates with a thin layer of thermal grease to improve the thermal connection between the modules and the coldplates, as shown in Figure 151.

**Figure 151 IGBT modules mounted to coldplate assemblies**

The power PCBs are mounted to the IGBT modules, with the power connections to the inductors and the connectors being fixed with brass nuts and bolts, so as to allow for later removal, as is shown in Figure 152.
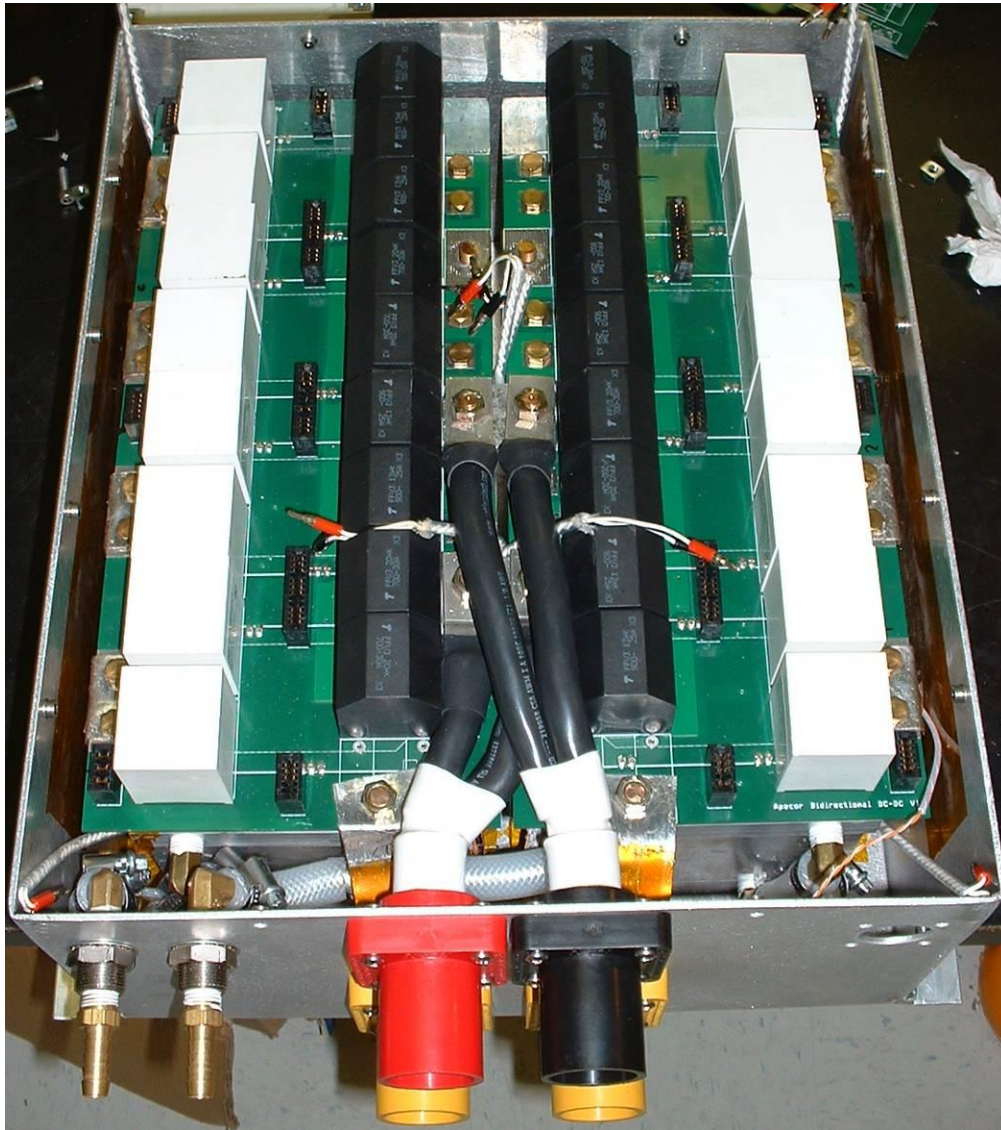

Figure 152 Power PCBs and cabling mounted

Once the power PCBs are mounted, the controller modules can be inserted, and the communication cables are connected, as shown in Figure 153. At this point the converter is ready to be tested to make sure that the system is working properly. Once all of the major components are tested, the controller modules can be covered with aluminum housings, which serve the purpose of creating a thermal path from the heat generating components of the controller modules and the top lid of the enclosure, as well as reducing the effect of noise and EMI on the performance of the controller modules. The aluminum controller module channels are shown in Figure 154, with the addition of thermally conductive gap pads in Figure 155.
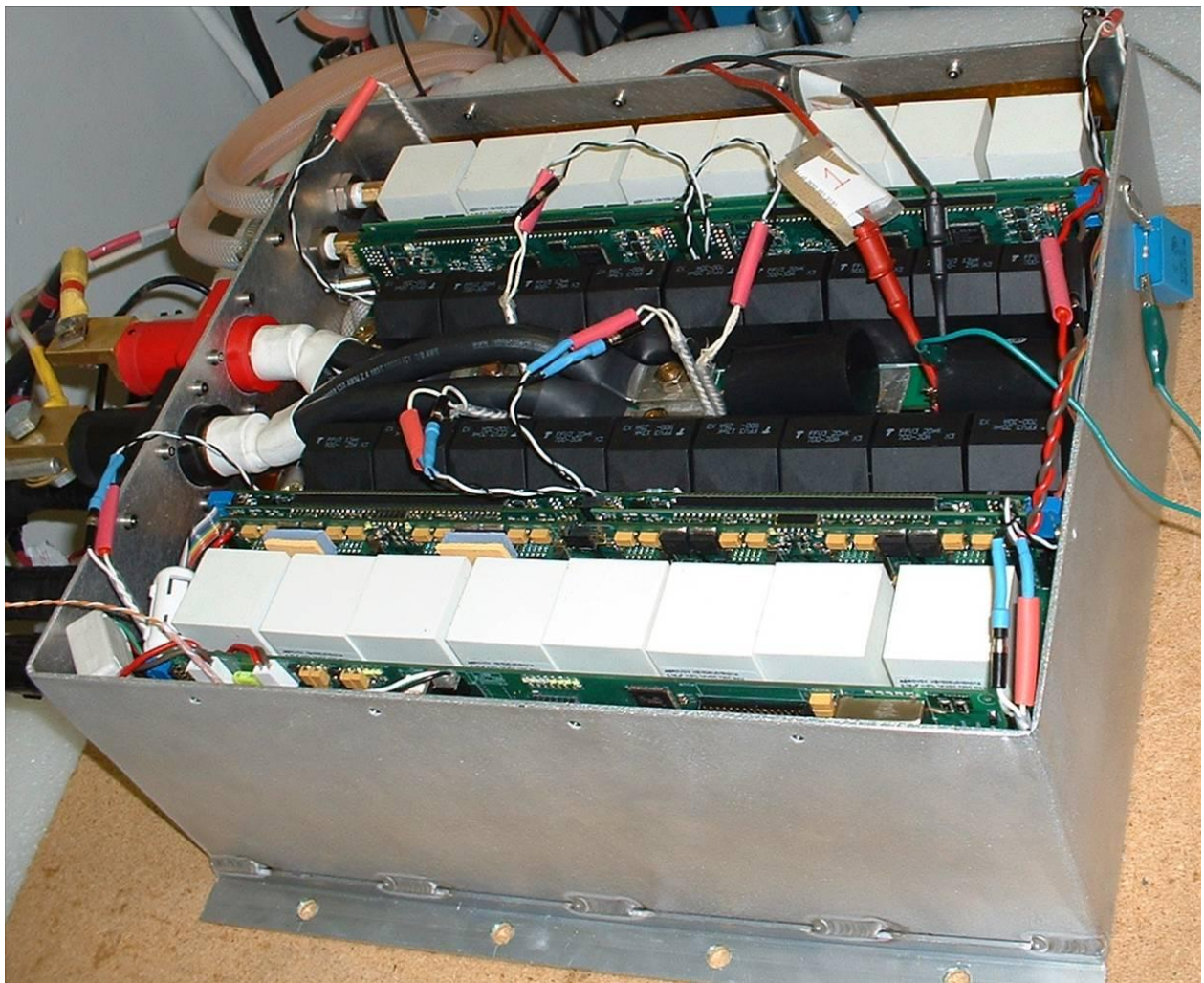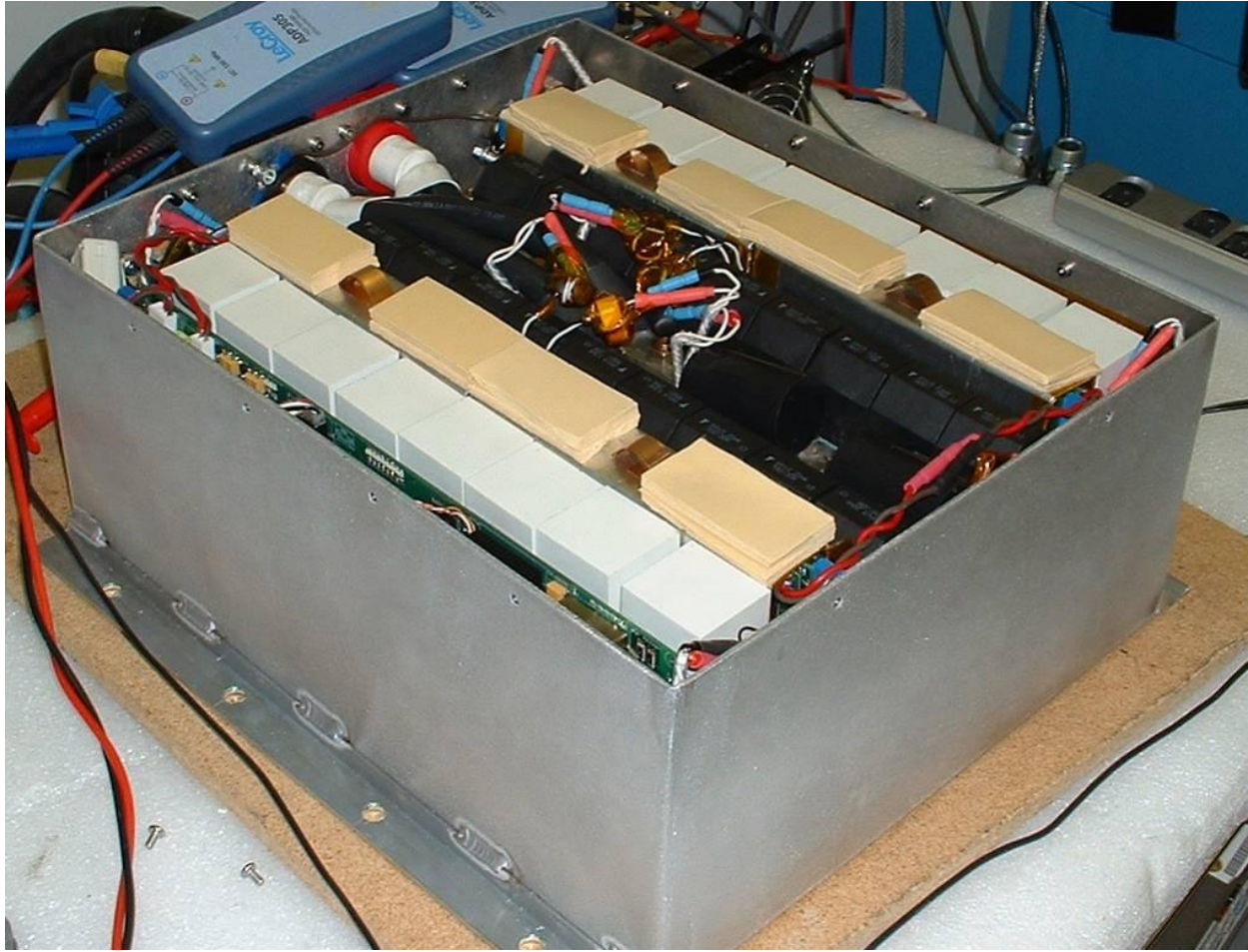

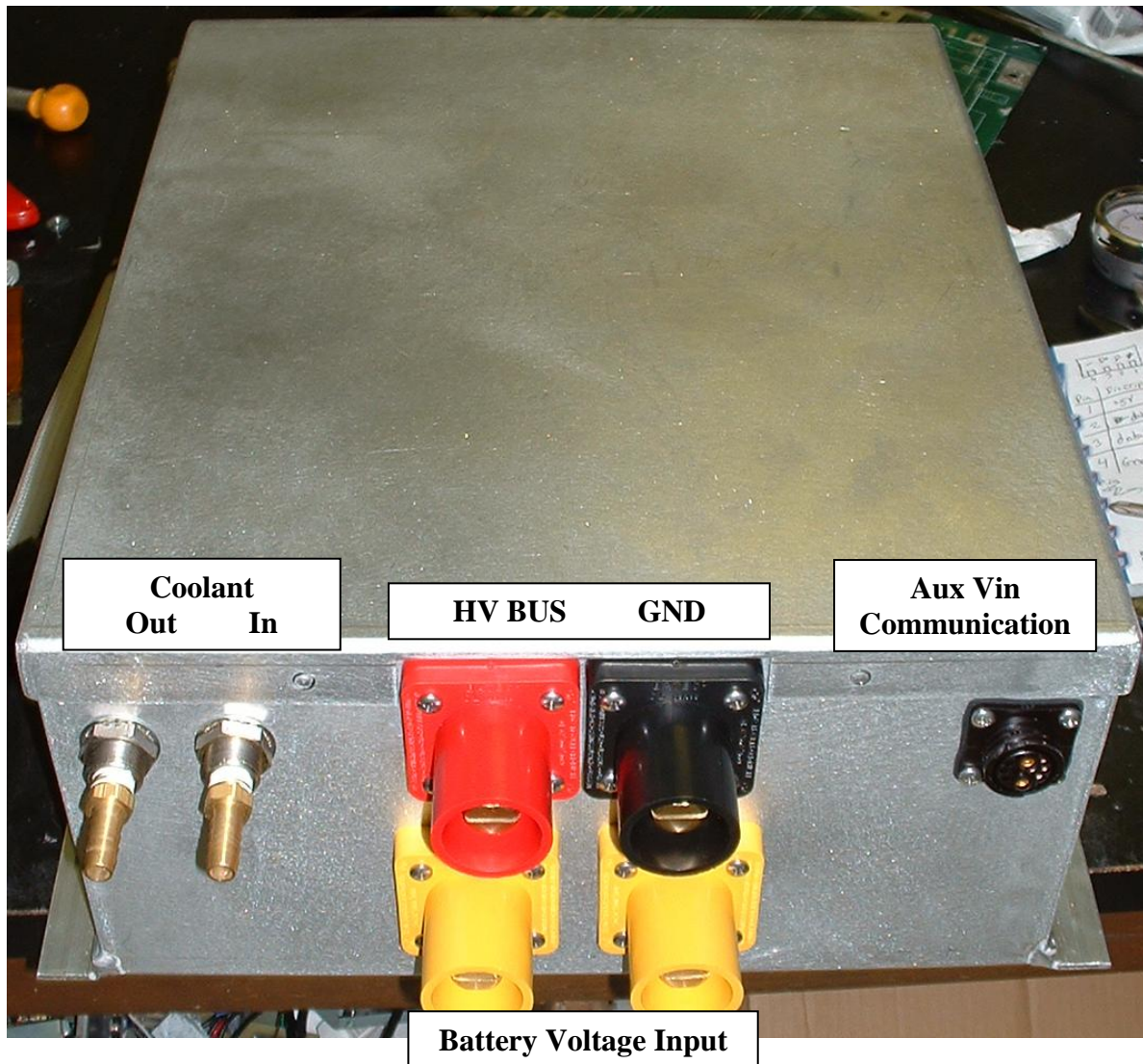**Figure 153 Assembled DC-DC Converter in Testbed**
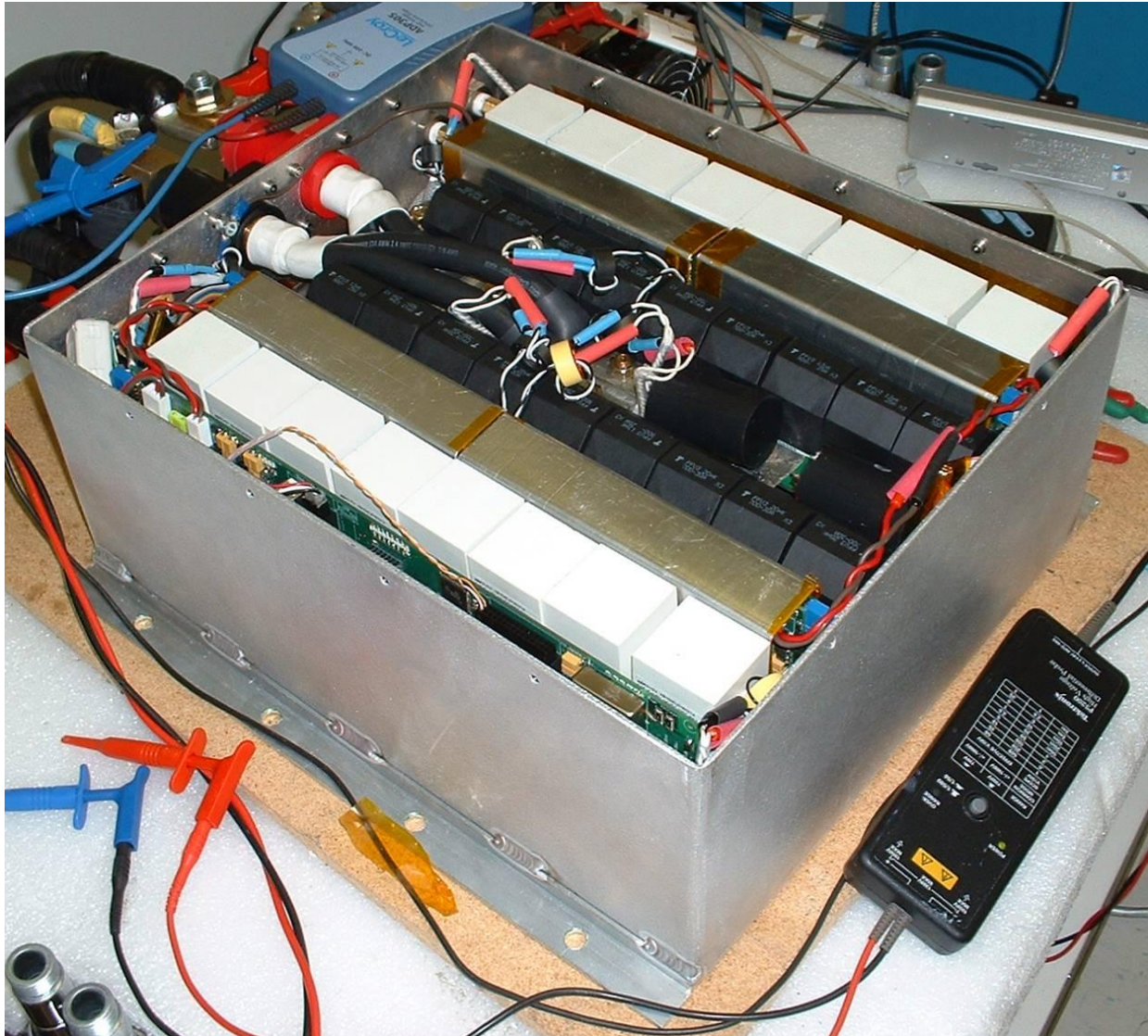
Figure 154 DC-DC Converter w/ Aluminum Channels for Cooling and EMI Suppression

Figure 155 DC-DC Converter w/ Thermal Gap Pads and Copper Grounding Springs to Lid

The completely assembled 200 kW DC-DC converter prototype is shown in Figure 156. The converter is designed for the harsh vehicular environment, and is completely sealed from moisture and sand. The power, coolant, and communication connections as shown are the only connections to the converter. The communication connector also houses the necessary auxiliary 12 V or 24 V input to power the controllers, as well as additional USB communication signals, for control from the PC during testing.

Figure 156 Fully Assembled DC-DC Converter

Experimental Results

The 200 kW 8-module prototype was operated under many conditions, including full power with high temperature coolant. The converter demonstrated performance exceeding expectations, with the average peak efficiency exceeding 98%, with some cases regularly achieving 98.5% efficient.

Thermal Performance
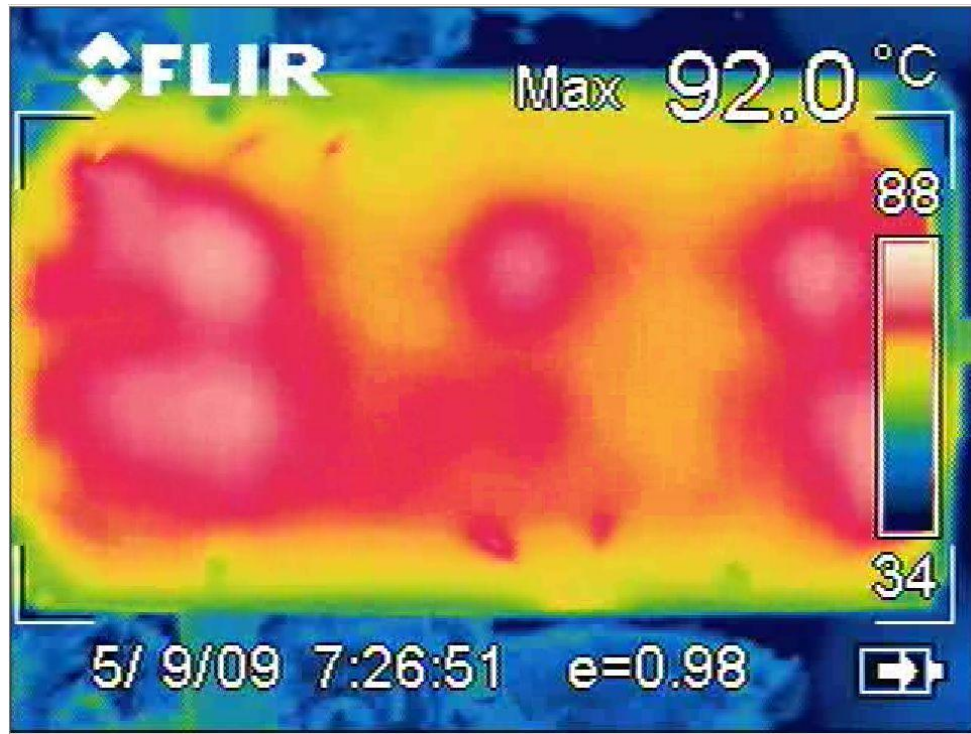
Figure 157 Thermal image Infineon IGBT @ 21kW and 85°C cooling

It is very difficult to determine the die temperature of the IGBT while in-system, since even the internal thermistors give a value which is somewhere in-between the baseplate temperature and the die temperature. Early in the project we were able to develop a testing setup, where a thermal camera could directly view the IGBT dies. Although the emissivity of the IGBT potting gel is unknown, it was estimated that the temperature rise was very low, approximately 25ºC, which means that there is no problem with running 105ºC coolant, with a very long expected IGBT life.

Operational Waveforms

The converter was tested to verify that the interleaving was occurring properly, in that each of the 8 converter modules should be shifted in phase by 45º from each other. This

operation was confirmed to operate very well, even considering the variation in inductance and snubbber capacitance between modules. As can be seen in Figure 158m the modules are well interleaved, and it can be seen that there is significant difference between the inductance of each module. It was later discovered that the inductors which are reaching higher peak current have lower inductance since they were the closest to the single-point battery input connection. The result is that the inductors with longer foil wires have higher overall inductance, from the self-inductance of the foil leads. This is why it can be seen from the waveform that the modules seem to vary sequentially to have increased inductance, and thus, lower peak current.
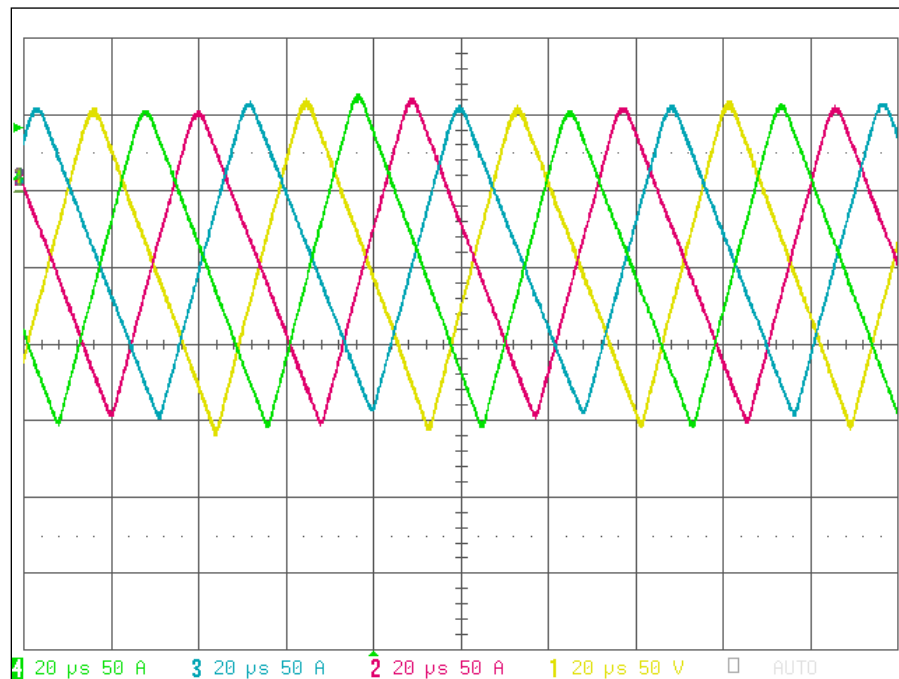
Figure 158 4 stages, 4 inductor current measurements, 600V to 350V, 62kW

The same test condition of Figure 158 is shown in Figure 159, with the switch node voltage of two of the modules shown, proving the soft-switching behavior.
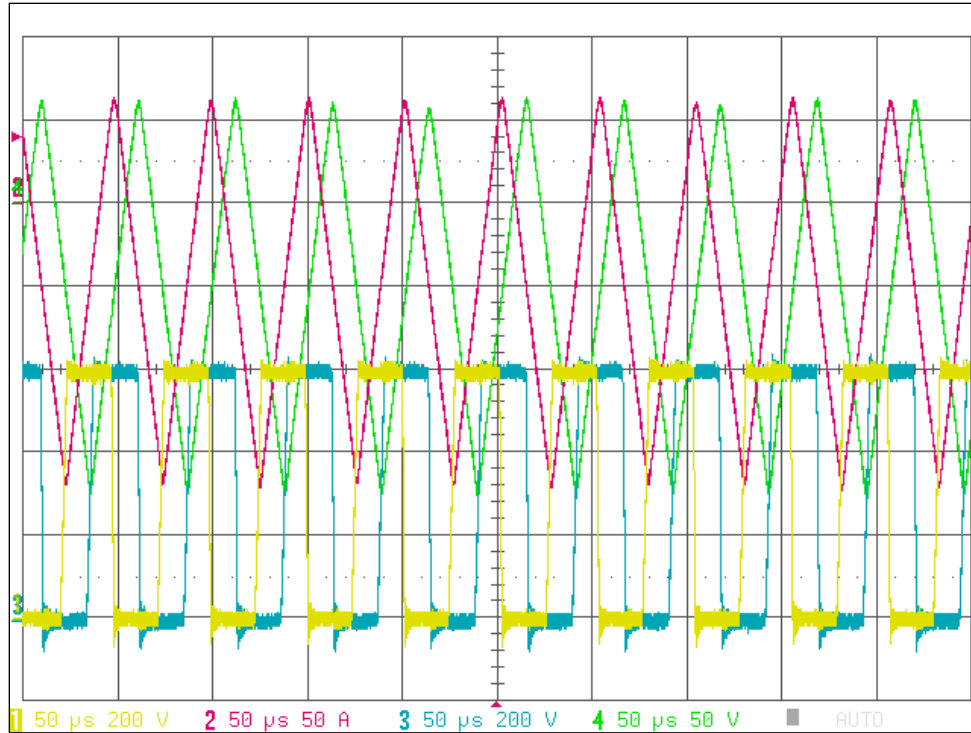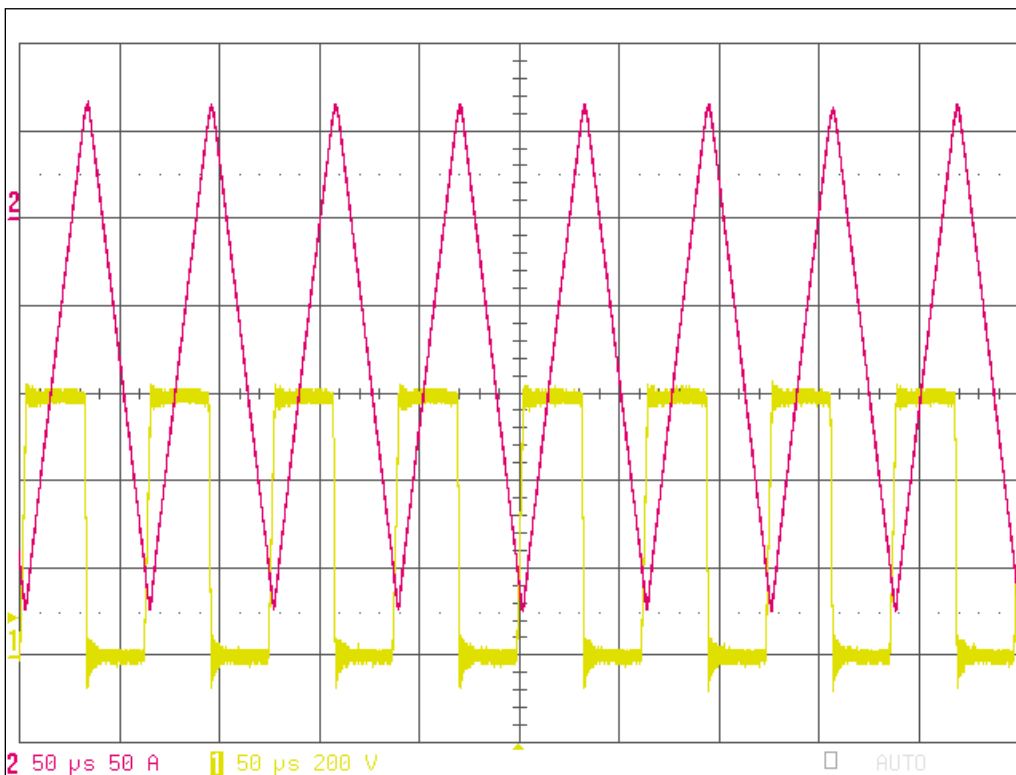
Figure 159 4 stages, 1st and 3rd stage: switch node voltage, 2nd and 4th stage: inductor current,

600V to 300V, 62kW

To test the power handling capability of the converter, a single module was operated to 28 kW, well exceeding the designed full power rating of 22.5 kW. This suggests that the converter will be robust, and will be able to handle output power transients well higher than the steady-state maximum power, probably exceeding 225 kW. This was not tested though, due to lack of a DC source powerful enough. During testing, single modules of the converter were operated up to 30 kW successfully, without any indication that the limits of the converter were being reached. Later work will be to determine the physical limits of the converter, as the converter was never tested to a point where a power component failed. The waveform in Figure 161 shows two modules operating at the full power of 46 kW. The converters operate as expected, with interleaving and soft-switching behaving very stable.
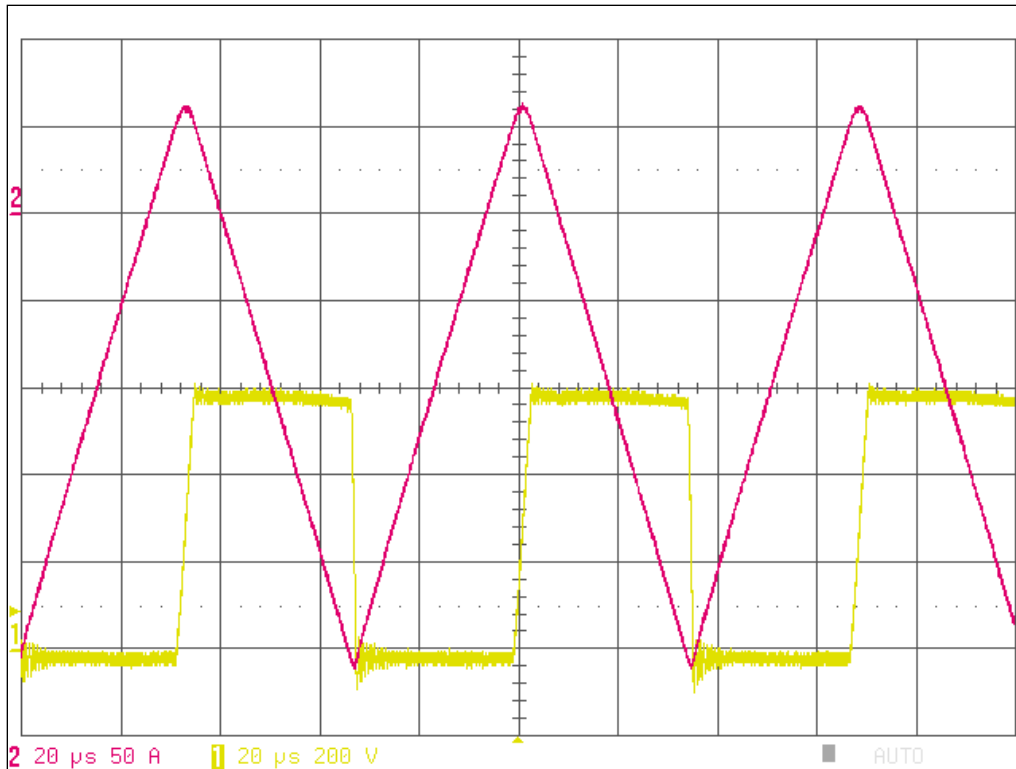
Figure 160 1 stage, switch node and inductor current measurement, 600V to 300V, 28kW

Figure 161 2 stages, 1st stage: switch node voltage, 2nd stage: inductor current, 600V to 300V, 46kW

Performance Metric Comparisons

The bidirectional DC-DC converter was tested under many conditions to verify performance. The performance was found to exceed the specified targets in most cases. The converter performance specifications are listed in Table 11.

The power density is approximately 8 kW/L, which is slightly less than the target of 8.5 kW/L. This value depends on the maximum power rating, and the volume of the converter. In our case, it is difficult to measure power levels above 200 kW, due to the testing capabilities, yet, the converter has been able to run 4 IGBT modules at over 100 kW, and it is strongly suspected that the overall peak power capability is higher than the listed 200 kW.

Table 11 Converter Specifications

Specification	Threshold	Target	Achieved
Power Density	6 kW/L 2 kW/kg	8.5 kW/L 4 kW/kg	8 kW/L 4.4 kW/kg
Peak Power	180 kW	--	200 kW
Average Power	150 kW	--	180 kW
Volume	--	--	25 L
Mass	--	--	45.5 kg
Output Voltage Range	580V – 640V	--	580V – 700V
Battery Voltage Range	250V – 530V	--	250V – 530V
Efficiency @ 5kW	91%	--	92%
Efficiency @ 30 kW	96%	--	97.5%
Efficiency (Peak)	--	--	98.5%
Max Coolant Temp	90ºC	100ºC	105ºC
Voltage Regulation	±3%	--	±1%
Current Regulation	±3%	--	±3%
Coolant Flow Rate	18 L/min	12.5 L/min	12.5 L/min
Pressure Drop	25 psi	--	16 psi

Efficiency Results

The efficiency of the converter is very high, with the peak efficiency exceeding 98%. By implementing phase scheduling, the converter's average efficiency also remains very high, since the converter can automatically disable power stages in steps of 2, allowing the converter to drop down to only 2 operating stages at light load, but quickly add more stages as power demands increase. The only downside of phase scheduling is that the transient response will suffer for "hard" switched loads, like resistor banks, where the power requirements will instantaneously change. Since there is a delay in the activation of further stages, the converter may not be able to support the load for a short period of time. In the actual vehicle application though, there are no such transients, as there are significant time constants associated with the motor drive system. With phase scheduling enabled, the suggested maximum current slew rate for the bus voltage is 1000 A/sec. Depending on the needs of the system, the maximum current slew rate can also be optimized, with the tradeoff being between efficiency and transient response. Figure 162 shows the phase scheduled efficiency of the converter in buck mode, while Figure 163 shows the phase scheduled efficiency in boost mode.
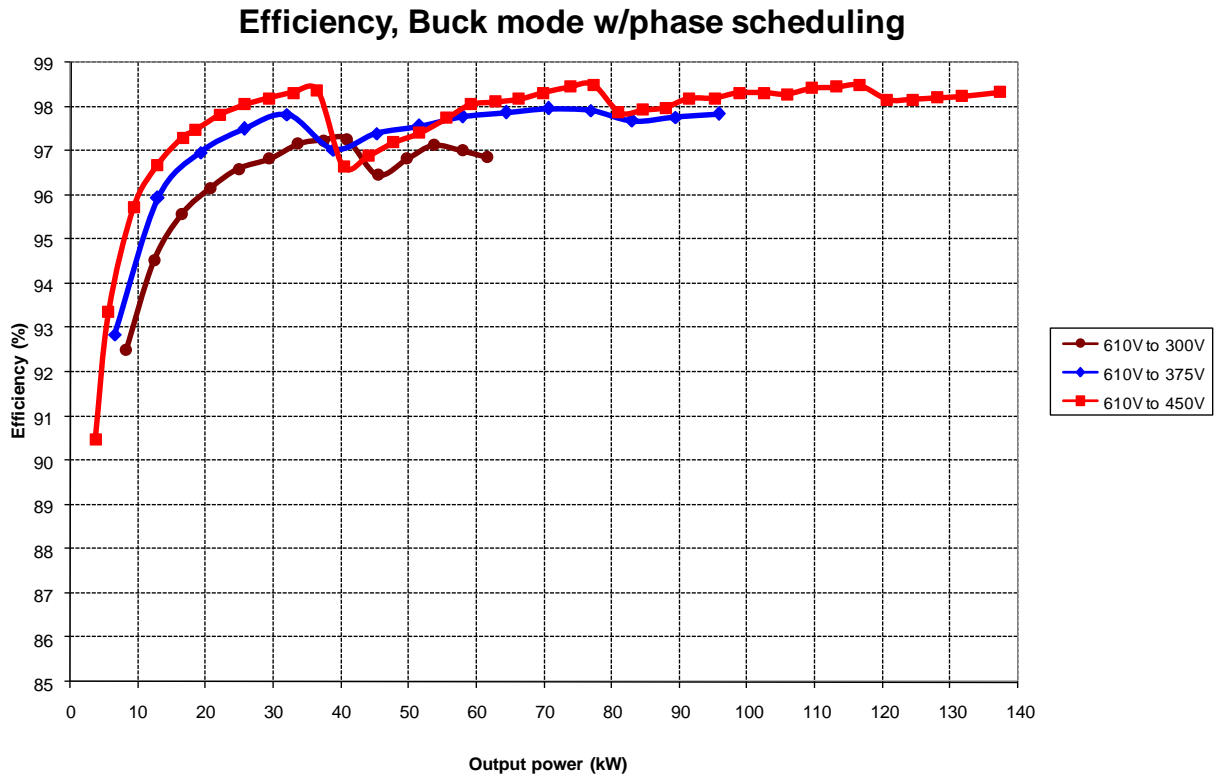
Efficiency, Buck mode w/phase scheduling

Figure 162 8-Module DC-DC converter buck mode efficiency

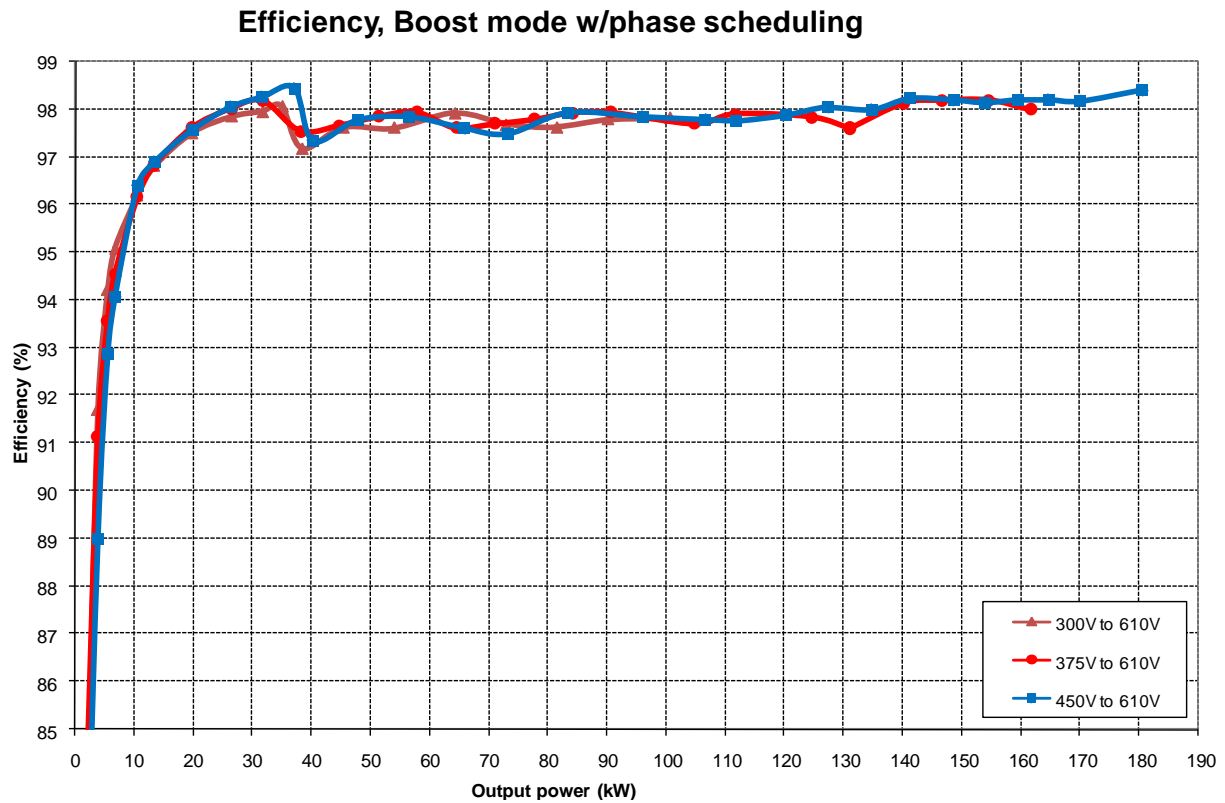**Efficiency, Boost mode w/phase scheduling**

Figure 163 8-Module DC-DC converter boost mode efficiency

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Another specification to notice is the pressure drop of the coolant loop. The achieved value of 16 psi, while less than the 25 psi threshold, is still greater than what was expected based on the design. In the testing of the 4-module prototype, the pressure drop was approximately 6 psi, and in the 8-module prototype, there are two coldplates in parallel, which should result in a similar pressure drop, with increased flow rate. Due to the additional plumbing necessary to connect the coldplates in parallel, it is apparent that the overall pressure drop of the converter has increased. In future designs, a lower impedance coolant path inside the converter will probably yield a more favorable pressure drop.

The final efficiency sweep of the converter in buck mode, across various operating conditions and number of active phases is shown in Figure 164. The benefit of phase scheduling is apparent when comparing the efficiency of only two modules running versus all eight.
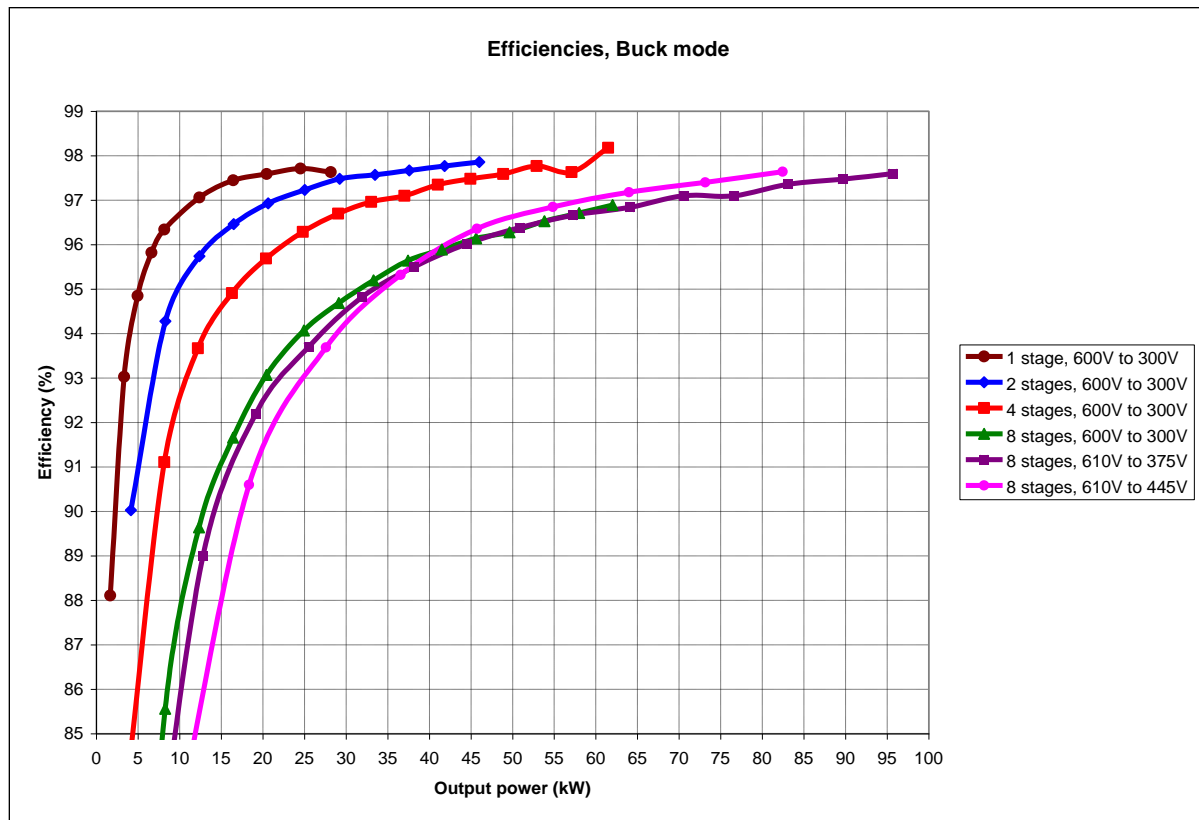
Figure 164: 8-Module converter efficiencies at different conditions in buck mode

CHAPTER 6: CONCLUSIONS

The goal of this work was to investigate and create technology which will allow high power DC-DC converters to operate with higher power-density, higher efficiency, and at higher coolant temperature. Through advancements in many areas of power electronics design, these goals have been achieved. The first building block of this achievement is the use of a boundary mode interleaved variable-frequency bidirectional soft-switching DC-DC converter topology, which significantly reduces the switching losses of the device, thus allowing higher switching frequencies. Higher switching frequency then enables reduced necessary passive energy storage in the inductors and capacitors, which serves to reduce the converter size, and increase power density.

The second building block is a new digital controller scheme, which enables multiple modules to operate between different modes seamlessly with variable frequency soft switching while also achieving interleaved operation, which increases the effective ripple frequency to the filter capacitors, thus further increasing power density. The digital controller also allows flexibility, so that the converter can easily be adapted to different systems without significant redesign.

The third building block is the use of advanced cooling technology to allow higher coolant temperature. Custom IGBT modules were designed which have windowed openings allowing for evaporative spray cooling directly on the DBC under the semiconductor devices, thus reducing the thermal impedance of the cooling, and increasing the maximum allowable coolant temperature. The spray cooled IGBTs are capable of operating at full power with 100°C

coolant, which can unlock the potential for the converter to be cooled directly from the main vehicle coolant loop.

The last major building block is the development of a high density nanocrystalline inductor structure, which is capable at operating up to 200°C, while achieving high density and low loss. By utilizing these new high temperature and high density inductors, the method of cooling becomes less critical, which allows for higher power density and reliability.

The experimental prototypes have achieved high power density, high efficiency, and high temperature operation. Results with the off-the-shelf IGBT prototype has also shown that the culmination of variable frequency soft switching and the nanocrystalline inductor still can deliver very high performance, which leads to the possibility of pursuing a design which doesn't utilize spray cooling and custom IGBT modules, but is still capable of high performance. The spray cooled custom IGBT is the key for very high performance, with the potential for well over 10 kW/L, but the use of evaporative spray cooling presents challenges to the design of the vehicle cooling system. Future vehicles can be designed with the ESC electronics in mind, to allow the design to see mainstream applications.

Even though the goal of this project was to assess performance potential, it is still important to assess potential for future industry adoption. Based on the results of this work, it is apparent that most technologies implemented in this converter are relatively close to being ready for practical use. The only technology which will require more significant development time and investigation is the spray cooled IGBT. Use of evaporative spray cooled power converters in real world systems must be further analyzed to assess the potential risks of non-optimal operating conditions.

Based on the results of this effort, it is believed that the best course of action would be to decouple the spray cooling research from the soft-switching converter research. The soft-switching technology that was designed has the ability to increase the performance of the converter, without regard to the method of cooling for the IGBT, as was demonstrated by the traditional coldplate prototype. Similarly, a spray-cooled IGBT module can potentially increase the performance of a traditional hard-switched converter. Furthermore, the new digitally controlled soft switching approach, and the high density inductor design will be able to increase the performance of a converter with any method of cooling.

Future Research

Future research in this field will be to further optimize the converter components and system design, using the base technology developed in this dissertation. Based on the outstanding performance of the 8-module 200 kW DC-DC converter, it is anticipated that future work will readily achieve power density exceeding 10 kW/L, with the potential to exceed 14 kW/L with further long-term optimization. Furthermore, this technology can be applied to other converter topologies, including the bidirectional buck-boost converter and potentially a bidirectional coupled-inductor boost converter. The operation of the buck-boost converter is fundamentally similar to the presented boost converter, but there will be necessary analysis and design for the additional IGBT voltage stress. The advantage of the buck-boost converter would be the ability to convert power between widely varying input and output voltages, whereas the presented converter topology requires a minimum voltage difference between the battery voltage and the high-voltage bus. A potential disadvantage of the buck-boost converter is generally lower efficiency, and the potential for complication due to the effective negative output voltage of the converter.

Another potential research focus is to design a soft-switching boundary mode control structure for a coupled inductor topology. The coupled inductor buck and boost converter has been shown to increase the density and efficiency of hard-switched converters, due to the decreased magnetics size and decreased current ripple. The magnetic structure presented in this work is an inductor featuring two isolated parallel windings, with a coupling factor of approximately 0.66. This structure closely mimics that of a coupled inductor design, where the coupled inductor is essentially a transformer with considerable leakage inductance on each winding. If this control structure can be adapted for use as a coupled inductor converter, there is the potential to achieve significantly higher power density while still maintaining high efficiency.

APPENDIX A: NANOCRYSTALLINE INDUCTOR CALCULATOR

Nanocrystalline inductor calculator for Boost Mode

$Vin := 300$ in volts $Ls := 32$

$V_o := 600$

$Npri := 7$

$ineg := 30$ $C_1 := 160 \cdot 10^{-9}$ $C_2 := 160 \cdot 10^{-9}$

$k := 1.5 \quad \dfrac{W}{m \cdot C}$ 7 btu in/F hr ft^2 = 1 W/mK   of potitng material

$Bmax := 1.23$ in tesla

$Temp := 150$ in C   temperature of wire

$Tamb := 55$ in C

$Tcold := 100$ C

$width := 1.4$ copper width in inches

$thickness := .016$

$tape := .006$

Core dimensions in cm
$dima := 1.65$ 1.65
$dimb := 1.5$
$dimc := (width) \cdot 2.54 + .4$ $dimc = 3.956$
$dimd := 9$
$dime := dimb + 2 \cdot dima$ $dime = 4.8$
$dimf := dimc + 2 \cdot dima$ $dimf = 7.256$

number of strips in parallel

$paralelled := 2$

$cuts := 4$

Shape
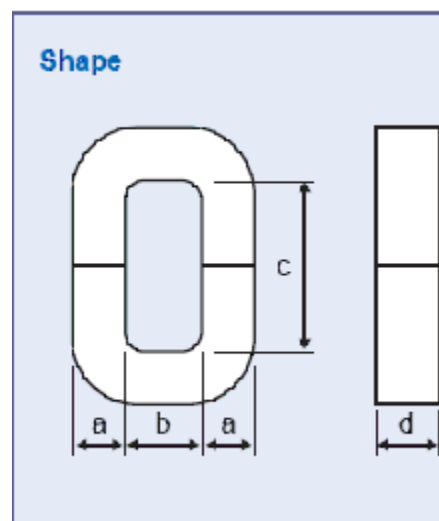
$$SA := 2 \cdot \text{dimf} \cdot (\text{dimb} + \text{dimd}) + 2 \cdot (\text{dimb} + \text{dimd}) \cdot (\text{dimb} + \text{dime}) + 2 \text{dimf} \cdot (\text{dimb} + \text{dime})$$

$SA = 376.1016$ in cm^2

$\text{maglen} := 2 \cdot \text{dimc} + 2 \cdot \text{dimb} + \pi \cdot \text{dima}$

Kstacking := .83

$\text{maglen} = 16.0956$ in cm

$Ae := 100 \text{dima} \cdot \text{dimd} \cdot \text{Kstacking}$

$Ae = 1.2326 \times 10^3$ in mm

$$\text{mass} := \left[\frac{1.8}{1203.5192} (Ae \cdot \text{maglen} \cdot 10) \right]$$

$\text{mass} = 1.5454$ in kg

$$Al := \frac{Ls}{\text{Npri}^2} \qquad Al = 0.6531$$

$$\text{isat} := \frac{Ae \cdot \text{Npri} \cdot \text{Bmax}}{Ls}$$

$\text{isat} = 331.633$ in Amps

$f := 10, 11 .. 50$

calculation of proximety effect:

width = 1.4

thickness = 0.016

$window := \dfrac{dimc}{2.54}$ width of winding window $window = 1.5575$ in inches

paralelled = 2

$stacked := Npri$ number of turns stacked $stacked = 7$

$wirelength := Npri \cdot \dfrac{2dimd + 2\cdot\pi\cdot dima}{100}$ $wirelength = 1.9857$ meters

$copperlength := wirelength \cdot paralelled$ copperlength = 3.9714   in meters

$windowheight := \dfrac{dimb}{2.54}$ $windowheight = 0.5906$

N1 := 1   number of groups   leave as 1

ml:= paralelled·stacked $ml = 14$ number of layes of copper

$a := width \cdot \dfrac{25.4}{1000}$ $a = 0.0356$

$b := window \cdot \dfrac{25.4}{1000}$ $b = 0.0396$

$h := thickness \cdot \dfrac{25.4}{1000}$ $h1 := h + tape \cdot \dfrac{25.4}{1000}$

$windowfill := (thickness + tape) \cdot \dfrac{ml}{windowheight}$ $windowfill = 0.5215$

$windowdensity := (thickness) \cdot \dfrac{ml}{windowheight}$ $windowdensity = 0.3793$

$\mu0 := 4\cdot\pi\cdot 10^{-7}$ in H/m $\mu copper := 1.25$

$\rho := 1.7 \cdot 10^{-8}$ in ohm meters

$\eta := N1 \cdot \dfrac{a}{b}$ $\eta = 0.8989$

$depth(freq) := \sqrt{2 \cdot \dfrac{\rho}{2\cdot\pi\cdot freq \cdot \mu copper \cdot \mu0}}$

$depth(60000) = 2.3961 \times 10^{-4}$

$depth\_mil(freq) := depth(freq)\cdot 39370$

$depth\_mil(17000) = 17.7227$

$\omega(f) := 2\pi f \cdot 1000$ in khz

$$\alpha(f) := \sqrt{\frac{h}{h}} \sqrt{\frac{i \cdot \omega(f) \cdot \mu 0 \cdot \mu copper \cdot \eta}{\rho}}$$

$\alpha(60) = 3.9568 \times 10^3 + 3.9568i \times 10^3$ f in khz

$$M(f) := \alpha(f) \cdot \frac{h^2}{h} \cdot \coth(\alpha(f) \cdot h)$$

$M(60) = 1.4754 + 1.4932i$ f in khz

$$D(f) := 2 \cdot \alpha(f) \cdot \left(\frac{h^2}{h}\right) \cdot \tanh\left(\alpha(f) \cdot \frac{h}{2}\right)$$

$D(60) = 1.7554 + 4.2668i$

$h = 4.064 \times 10^{-4}$

$$Fr(f) := Re(M(f)) + \left[\left(ml^2 - 1\right) \cdot \frac{Re(D(f))}{3}\right]$$

$Fr(17) = 12.429$ f in khz

$$Rdc\_1 := \rho \cdot \frac{wirelength}{width \cdot thickness \cdot .0006451}$$

$Rdc\_1 = 2.3359 \times 10^{-3}$

$$Rdc := \frac{Rdc\_1}{paralelled}$$

$Rdc = 1.1679 \times 10^{-3}$

$$Rtemp(Temp) := Rdc \cdot [1 + .0038666(Temp - 25)]$$

$$Tmul(Temp) := 1 + .0038666(Temp - 25)$$

$Rtemp(150) = 1.7324 \times 10^{-3}$

$Tmul(150) = 1.4833$

Alternate dowell estimation

$$\xi(f) := \left(\frac{h^2}{h1 \cdot depth(f)}\right)$$

$\xi(17000) = 0.6566$

$$Fr2(f) := \left(\frac{\xi(f)}{2}\right) \cdot \left[\left(\frac{\sinh(\xi(f)) + \sin(\xi(f))}{\cosh(\xi(f)) - \cos(\xi(f))}\right) + (2 \cdot ml - 1)^2 \cdot \frac{\sinh(\xi(f)) - \sin(\xi(f))}{\cosh(\xi(f)) + \cos(\xi(f))}\right]$$

$Fr2(17000) = 12.2066$

calculate core and copper losses

$$\omega_o := \frac{1}{\sqrt{Ls \cdot 10^{-6} \cdot (C_1 + C_2)}} \qquad \omega_o = 3.125 \times 10^5$$

$$A_1 := V_o - Vin \qquad B_1 := \frac{-ineg}{\omega_o \cdot (C_1 + C_2)}$$

$$i_{L5}(t) := -(V_o - Vin)(C_1 + C_2)\omega_o \cdot \sin(\omega_o \cdot t) + -ineg \cdot \cos[\omega_o \cdot (t)]$$

$$i_{L5}(.000003) = -41.9366$$

$$V_{c1.mode5}(t) := Vin + (V_o - Vin) \cdot \cos[\omega_o \cdot (t)] + \frac{-ineg}{\omega_o \cdot (C_1 + C_2)} \cdot \sin[\omega_o \cdot (t)]$$

$$ttest := 0$$

Given

$$Vin = V_{c1.mode5}(ttest)$$

$$tneg := Find(ttest) \qquad tneg = 2.5133 \times 10^{-6}$$

$$imin := i_{L5}(tneg) \qquad imin = -42.4264$$

$$a_1 := \frac{-B_1}{6} \qquad b_1 := \frac{-A_1}{2} \qquad c_1 := B_1 \qquad d_1 := V_o$$

$$p_1(x) := \frac{-B_1}{6} \cdot x^3 - \frac{A_1}{2} \cdot x^2 + B_1 \cdot x + V_o$$

$$v := p_1(x) \text{ coeffs }, x \rightarrow \begin{pmatrix} 600 \\ -300 \\ -150 \\ 50 \end{pmatrix}$$

$$r_1 := \text{polyroots}(v)$$

$$r_1 = \begin{pmatrix} -2.2015 \\ 1.4549 \\ 3.7466 \end{pmatrix}$$

$$m_1 := \begin{vmatrix} r_{1_0} & \text{if } (r_{1_0} > 0) \wedge [(r_{1_0} < r_{1_1}) \vee (r_{1_1} < 0)] \wedge [(r_{1_0} < r_{1_2}) \vee (r_{1_2} < 0)] \\ r_{1_1} & \text{if } (r_{1_1} > 0) \wedge [(r_{1_1} < r_{1_0}) \vee (r_{1_0} < 0)] \wedge [(r_{1_1} < r_{1_2}) \vee (r_{1_2} < 0)] \\ r_{1_2} & \text{if } (r_{1_2} > 0) \wedge [(r_{1_2} < r_{1_0}) \vee (r_{1_0} < 0)] \wedge [(r_{1_2} < r_{1_1}) \vee (r_{1_1} < 0)] \\ 0 & \text{otherwise} \end{vmatrix}$$
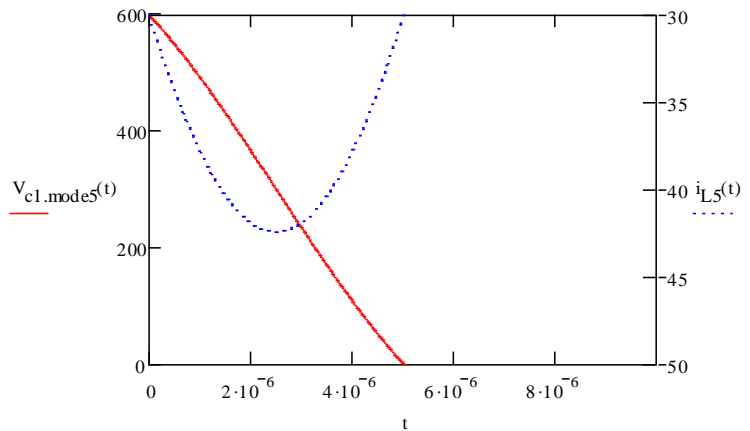
$$m_1 = 1.4549$$

$$t_{res} := \frac{m_1}{\omega_o} \qquad t_4 := \frac{-ineg \cdot \left(Ls \cdot 10^{-6}\right)}{Vin - V_o} \qquad t_6 := \frac{-i_{L5}\left(t_{res}\right) \cdot \left(Ls \cdot 10^{-6}\right)}{Vin}$$

$$t_{res} = 4.6557 \times 10^{-6} \qquad t_4 = 3.2 \times 10^{-6} \qquad t_6 = 3.5486 \times 10^{-6}$$

$$T_{ss}(f) := \frac{1}{f} - t_4 - t_{res} - t_6$$

$$ipeakL(f) := \frac{T_{ss}(f) \cdot Vin \cdot \left(V_o - Vin\right)}{Ls \cdot 10^{-6} \cdot V_o}$$

$$ipeakL(14000) = 281.364$$

$$t_1(f) := \frac{\left(ipeakL(f) - i_{L5}\left(t_{res}\right)\right) \cdot Ls \cdot 10^{-6}}{Vin} \qquad t_2(f) := \frac{\left(-ineg - ipeakL(f)\right) \cdot Ls \cdot 10^{-6}}{Vin - V_o}$$

$$t_1(20000) = 2.2846 \times 10^{-5} \qquad t_2(20000) = 2.2498 \times 10^{-5}$$

Integrating Current to be used in calculating input power

$$I_{1int}(f) := \int_0^{t_1(f)} \frac{Vin \cdot t}{Ls \cdot 10^{-6}} + i_{L5}\left(t_{res}\right) dt \qquad I_{2int}(f) := \int_0^{t_2(f)} \frac{Vin - V_o}{Ls \cdot 10^{-6}} \cdot t + ipeakL(f) dt$$

$$I_{1int}(20000) = 1.6866 \times 10^{-3} \qquad I_{2int}(20000) = 1.6977 \times 10^{-3}$$

$$I_{tot}(f) := \left(I_{1int}(f) + I_{2int}(f)\right) \cdot f \qquad I_{tot}(20000) = 67.686$$

$$Power(f) := Vin \cdot I_{tot}(f) \qquad Power(17000) = 2.6332 \times 10^4$$

Calculating the approximated fourier series expansion to be used to determine additonal loss

$$\text{Gain}(f) := \frac{\text{ipeakL}(f) - i_{L5}(t_{res})}{2} \qquad\qquad \text{DC}(f) := \frac{\text{ipeakL}(f) + i_{L5}(t_{res})}{2}$$

$$\text{Fourier}_{series}(n,t,f) := \frac{(-1)^{\frac{n-1}{2}}}{n^2} \cdot \frac{8 \cdot \text{Gain}(f)}{\pi^2} \cdot \sin(n \cdot \pi \cdot t \cdot) \qquad\qquad \text{FOR N} = 1,3,5,...$$

This is in radians

$$\text{Fourier}_{gain}(n,f) := \frac{(-1)^{\frac{n-1}{2}}}{n^2} \cdot \frac{8 \cdot \text{Gain}}{\pi^2} \qquad\qquad \text{Fourier}_{rad}(n,f) := n \cdot \pi \cdot 2 \cdot f$$

$$\text{Fourier}_{gain1}(f) := \text{Fourier}_{gain}(1,f) \qquad\qquad \text{Fourier}_{rad1}(f) := \text{Fourier}_{rad}(1,f)$$

$$\text{Fourier}_{gain3}(f) := \text{Fourier}_{gain}(3,f) \qquad\qquad \text{Fourier}_{rad3}(f) := \text{Fourier}_{rad}(3,f)$$

$$B_{test}(t,f) := \left(\text{Fourier}_{series}(1,t,f) + \text{Fourier}_{series}(3,t,f)\right) + \text{DC}(f)$$

$$f_x(t,n,f) := \begin{vmatrix} \dfrac{\text{Vin}}{\text{Ls} \cdot 10^{-6}} \cdot \left(t - \dfrac{n}{f}\right) + i_{L5}(t_{res}) & \text{if } \left[t < \left(t_1(f) + \dfrac{n}{f}\right)\right] \wedge \left[t \geq \left(0 + \dfrac{n}{f}\right)\right] \\[4mm] \dfrac{\text{Vin} - V_o}{\text{Ls} \cdot 10^{-6}} \cdot \left[\left(t - t_1(f)\right) - \dfrac{n}{f}\right] + \text{ipeakL}(f) & \text{if } \left[t \geq \left(t_1(f) + \dfrac{n}{f}\right)\right] \wedge \left[t \leq \left(t_2(f) + t_1(f) + \dfrac{n}{f}\right)\right] \\[4mm] 0 & \text{otherwise} \end{vmatrix}$$

$$F_x(t,f) := \sum_{n=0}^{9} f_x(t,n,) \qquad\qquad \text{Close to actual wave forms}$$

$$z_1 :=$$

$$\text{Fourier}_{\text{gain}}\left(z_1, 20 \cdot 10^3\right) = \begin{pmatrix} 86.806 \\ -9.6451 \\ 3.4722 \\ -1.7716 \\ 1.0717 \\ -0.7174 \end{pmatrix}$$
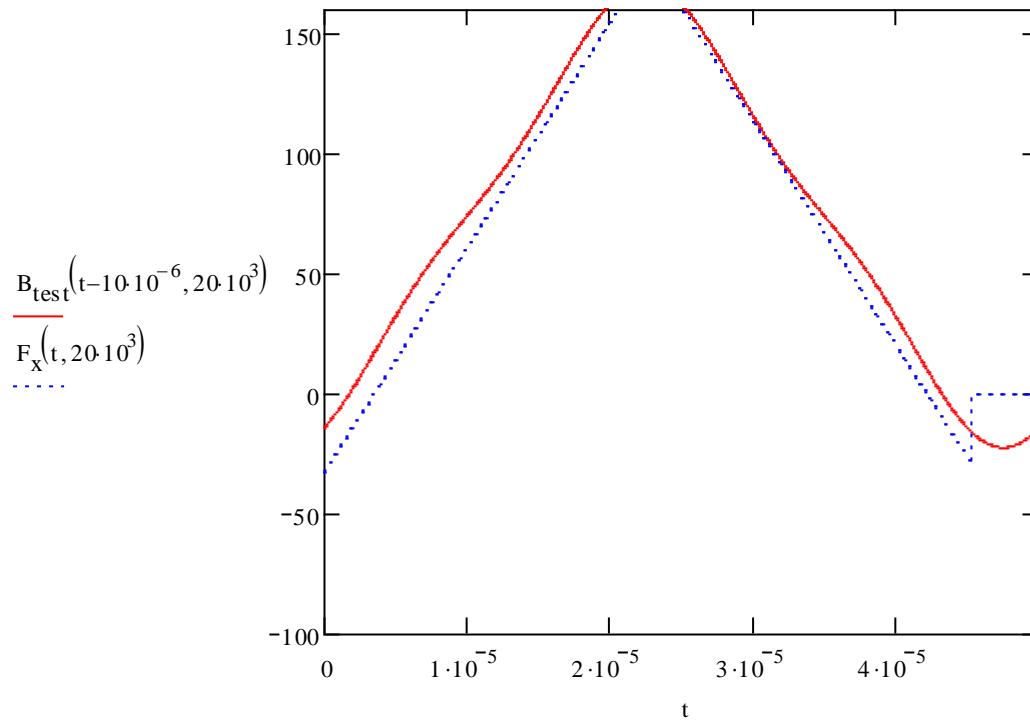
amplitude A pk

$$\text{Fourier}_{\text{rad}}\left(z_1, 20 \cdot 10^3\right) \cdot \frac{1}{10^3 \cdot 2 \cdot \pi} = \begin{pmatrix} 20 \\ 60 \\ 100 \\ 140 \\ 180 \\ 220 \end{pmatrix}$$

frequency khz

$$\text{DC}\left(20 \cdot 10^3\right) = 73.8249$$

DC bias A

The plot legend:

$$B_{test}\left(t - 10 \cdot 10^{-6}, 20 \cdot 10^{3}\right)$$

(red solid line)

$$F_{x}\left(t, 20 \cdot 10^{3}\right)$$

(blue dotted line)

$$Bpeak(f) := \frac{Ls \cdot (ipeakL(f))}{Npri \cdot Ae}$$

$$Bpeak(20000) = 0.671$$

$$Bneg := \frac{Ls \cdot imin}{Npri \cdot Ae}$$

$$Bneg = -0.1574$$

$$Bat(ineg) := \frac{Ls \cdot ineg}{Npri \cdot Ae}$$

$$Bat(89) = 0.3301$$

$$Bac(ipeak) := \frac{-Bneg + \frac{Ls \cdot ipea}{Npri \cdot Ae}}{2}$$

$$Bac(ipeakL(17000)) = 0.4909$$

$$Ploss\_core(f) := mass \cdot \left(1.79 f^{1.51} \cdot Bac(ipeakL(f \cdot 1000))^{1.74}\right)$$

$$ipeakL(17000) = 222.2779 \qquad Bpeak(17000) = 0.8244$$

$$Ploss\_core(17) = 57.8324$$

Integrating Current to be used in calculating rms current

$$I_{1sq}(f) := \int_0^{t_1(f)} \left[\left(\frac{Vin \cdot t}{Ls \cdot 10^{-6}} + i_{L5}(t_{res})\right)^2\right] dt \qquad I_{2sq}(f) := \int_0^{t_2(f)} \left[\left(\frac{Vin - V_o}{Ls \cdot 10^{-6}} \cdot t + ipeakL(f)\right.\right.$$

$$I_{1int}(20000) = 1.6866 \times 10^{-3} \qquad\qquad I_{2int}(20000) = 1.6977 \times 10^{-3}$$

$$I_{rms}(f) := \sqrt{\left(I_{1sq}(f) + I_{2sq}(f)\right) \cdot f}$$

$$irms(f) := I_{rms}(f) \qquad\qquad irms\left(20 \times 10^3\right) = 92.0178$$

$$Ploss\_copper2(f, z) := \left(\frac{Fourier_{gain}(2z + 1, f)}{\sqrt{2}}\right)^2 \cdot Rtemp(Temp) \cdot Fr\left[\frac{f \cdot (2 \cdot z + 1)}{1000}\right]$$

$$Ploss\_copper(f) := Ploss\_copper2(f \cdot 1000, 0) + Rtemp(Temp) \cdot DC(f \cdot 1000)^2$$

$$Ploss\_copper(17) = 130.9554$$

$$Ploss\_total(f) := Ploss\_copper(f) + Ploss\_core(f)$$

$$Ploss\_total(17) = 188.7877$$

$$deltaT(f) := \left(\frac{\frac{1}{\sqrt{10}} \cdot Ploss\_total(f) \cdot 1000}{SA}\right)^{\cdot} \qquad \text{in C and kHz}$$

$$Rtemp(Temp) = 1.7324 \times 10^{-3}$$

$$L\_eff(f) := 1 - \frac{Ploss\_total(f)}{Power(f \cdot 1000)} \qquad\qquad L\_eff(30) = 0.9845$$

temperature rise with cold plates

4 inductors per cp-15-12" cold plate top and bottom

$\text{Lcold} := 13.5$ inches

$\text{Wcold} := 4.5$ inches

$\text{thickness\_potting} := .5$ inches

$k = 1.5$ $\dfrac{W}{m \cdot C}$

$\text{Tcold} = 100$ C

$\text{Tplate(ploss)} := .011 \cdot \text{ploss} + \text{Tcold}$ $\text{Tplate}(1000) = 111$

$d := \text{thickness\_potting} \cdot .0254$ $d = 0.0127$ m

$\text{Acold} := \dfrac{\text{Lcold} \cdot \text{Wcold}}{1550.0031}$ $\text{Acold} = 0.0392$ m^2

$\Delta T\_\text{Potting(loss)} := \left(\dfrac{\text{loss} \cdot d}{k \cdot \text{Acold}} \right)$ $\Delta T\_\text{Potting}(1000) = 216.0224$

$\Delta \text{Tpotting(f)} := \Delta T\_\text{Potting}\left(4 \cdot \dfrac{\text{Ploss\_total(f)}}{2} \right)$

$\text{TL\_total(f)} := \text{Tplate}\left(4 \cdot \dfrac{\text{Ploss\_total(f)}}{2} \right) + \Delta \text{Tpotting(f)}$ $\text{TL\_total}(60) = 141.2618$

Estimate Gap   total gap (cm) = (.4pi * N^2*Ae(cm^2)*10^-8)/L

$$gap := \frac{10\left(10^{-8}\cdot.8\cdot\pi\cdot Npri^2\cdot dima\cdot dimd\right)}{2\cdot Ls\cdot 10^{-6}}$$

<mark>gap = 2.8575</mark>   gap in mm

cuts = 4

maglen = 16.0956   in cm

$ur := 10000$

$$Fring := \left[\frac{\left(dima\cdot 10 + \dfrac{gap}{cuts}\right)\cdot\left(dimd\cdot 10 + \dfrac{gap}{cuts}\right)}{dima\cdot dimd\cdot 100}\right]$$

Fring = 1.0516

extragap := .06   in mm

$$Lexp := \frac{10\left(10^{-9}\cdot 4\cdot\pi\cdot Npri^2\cdot dima\cdot dimd\right)\cdot Fring}{\left(extragap + gap + \dfrac{maglen\cdot 10}{ur}\right)\cdot 10^{-6}}$$

Lexp = 32.7776

$\mu 0 = 1.2566\times 10^{-6}$

$$Lnew := \frac{10^6\left(\mu 0\cdot\dfrac{dima\cdot dimd\cdot 100}{10^6}\cdot Npri^2\right)\cdot Fring}{\dfrac{extragap+gap}{1000}}$$

Lnew = 32.9584   in uH

$$gap\_fringe := \left[\frac{10^6\left(\mu 0\cdot\dfrac{dima\cdot dimd\cdot 100}{10^6}\cdot Npri^2\right)\cdot Fring}{\dfrac{Ls}{1000}}\right] - maglen\cdot\dfrac{10}{ur}$$

gap_fringe = 2.9888   in mm

$$spacer := \frac{gap\_fringe}{cuts}$$ $spacer\_mil := spacer\cdot 39.37$

<mark>spacer = 0.7472</mark>   in mm

<mark>spacer_mil = 29.4168</mark> n mils

Inductor Design Report

$Vin = 300$

$V_o = 600$

$Ls = 32$ uH

$C_1 = 1.6 \times 10^{-7}$ F

$C_2 = 1.6 \times 10^{-7}$ F

$isat = 331.633$

$Npri = 7$

$cuts = 4$

$Fring = 1.0516$

$gap\_fringe = 2.9888$ in mm

$spacer = 0.7472$ in mm

$spacer\_mil = 29.4168$ in mils

$spacer\_corrected\_mil := \dfrac{spacer\_mil}{1.18}$

$spacer\_corrected\_mil = 24.9295$

Copper specs

$width = 1.4$

$thickness = 0.016$

$paralelled = 2$ number of strips in parallel

$spacer\_corrected\_mm := spacer\_corrected\_mil \cdot .0254$
$spacer\_corrected\_mm = 0.6332$

$Rtemp(Temp) = 1.7324 \times 10^{-3}$ Rdc $\quad Temp = 150$

$windowfill = 0.5215$

Loss Analysis

$ftest := 17 \cdot 10^3$

$Power(ftest) = 2.6332 \times 10^4$

$Ploss\_copper2(ftest, 0) = 115.4827$

$Ploss\_copper2(ftest, 1) = 10.2034$

$Ploss\_copper2(ftest, 2) = 2.8352$

$Ploss\_core\left(\dfrac{ftest}{1000}\right) = 57.8324$

$Ploss\_total\left(\dfrac{ftest}{1000}\right) = 188.7877$

$Rtemp(Temp) DC(ftest)^2 = 15.4727$

$Fr\left(\dfrac{ftest}{1000}\right) = 12.429$

$Rtemp(150) = 1.7324 \times 10^{-3}$

$Bac(ipeakL(ftest)) = 0.4909$

Current Harmonic Content

estimated based on dowell's method

$Fourier_{gain}(z_1, ftest) = \begin{pmatrix} 103.5687 \\ -11.5076 \\ 4.1427 \\ -2.1136 \\ 1.2786 \\ -0.8559 \end{pmatrix}$ amplitude A pk

$Fourier_{rad}(z_1, ftest) \cdot \dfrac{1}{10^3 \cdot 2 \cdot \pi} = \begin{pmatrix} 17 \\ 51 \\ 85 \\ 119 \\ 153 \\ 187 \end{pmatrix}$ frequency khz

$DC(ftest) = 94.5051$ DC bias A

Shape
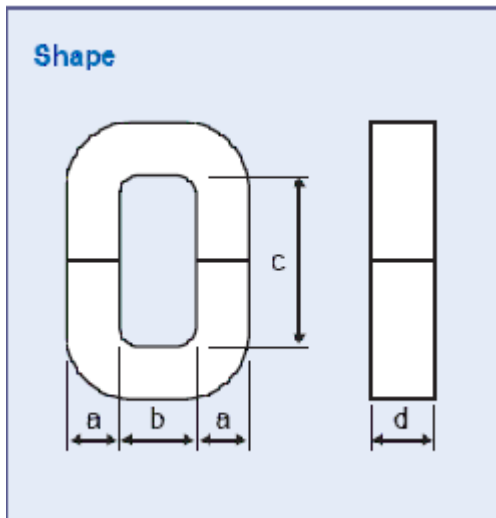
Core dimensions in cm

$dima = 1.65$ $dimd = 9$
$dimb = 1.5$ $dime = 4.8$
$dimc = 3.956$ $dimf = 7.256$

$dimc + 2 \cdot dima = 7.256$

$dimb + 2 \cdot dima = 4.8$

Inductor Losses vs. Output Power

Core Losses vs. Output Power

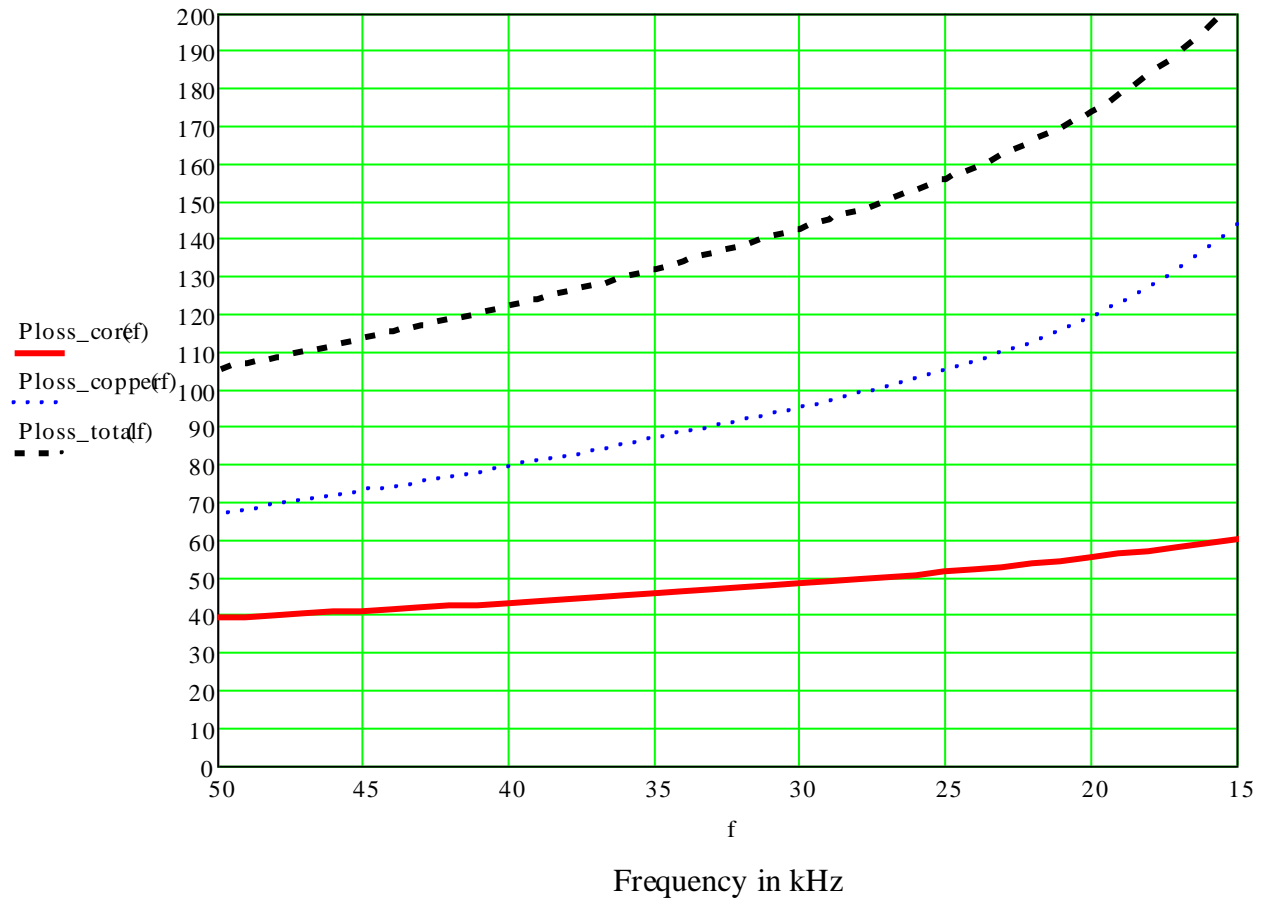Ploss_core(f)
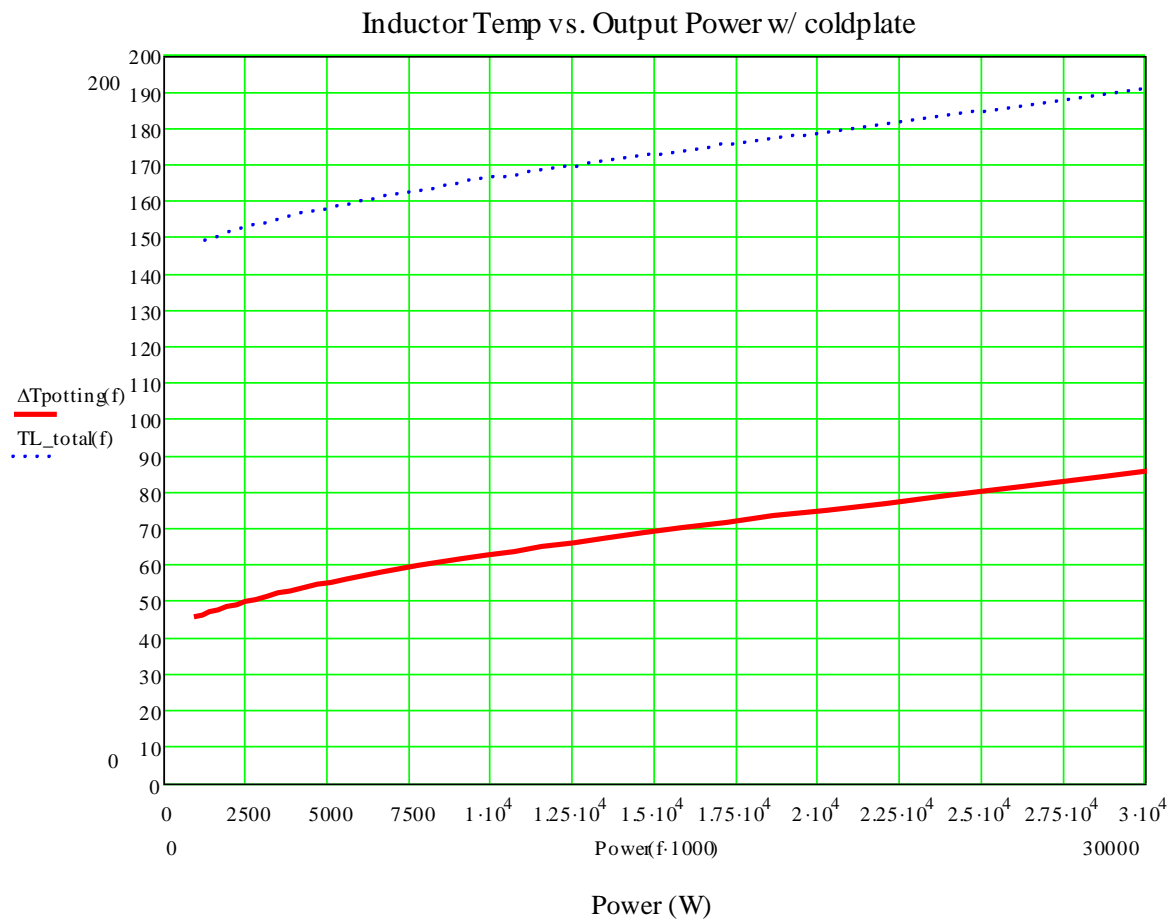
Power(f·1000)

Power (W)

Inductor Peak Current vs. Output Power
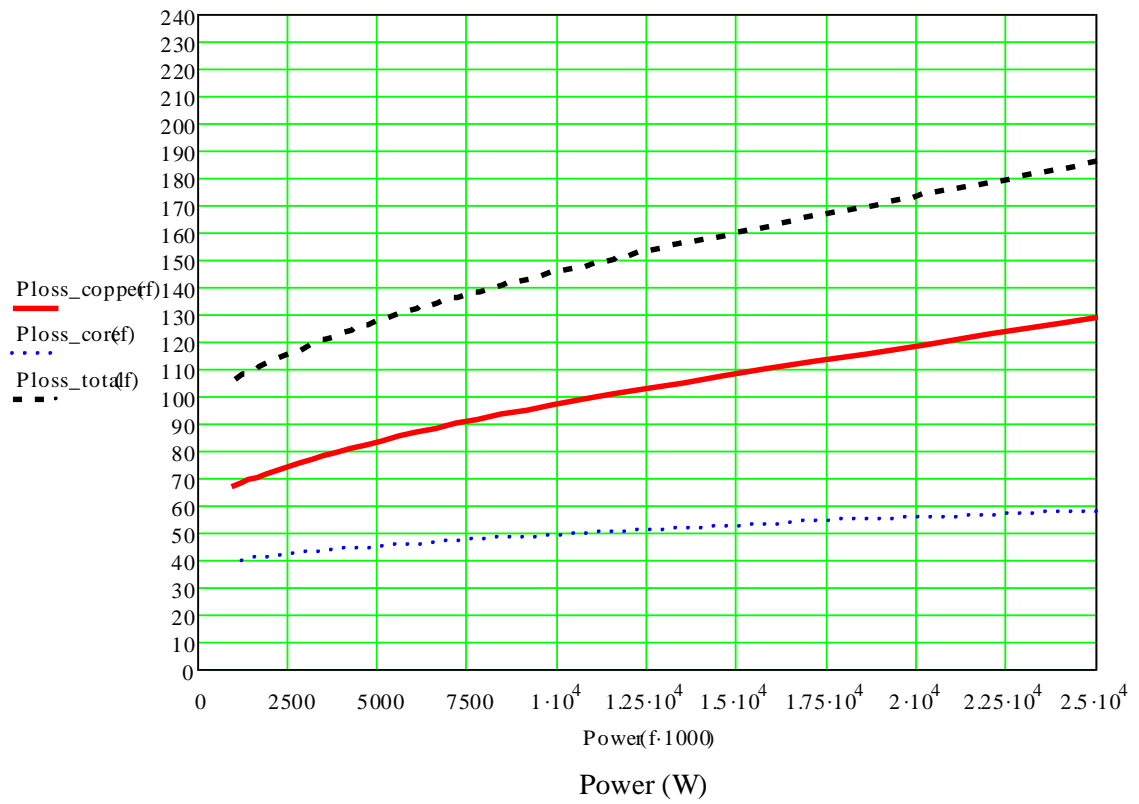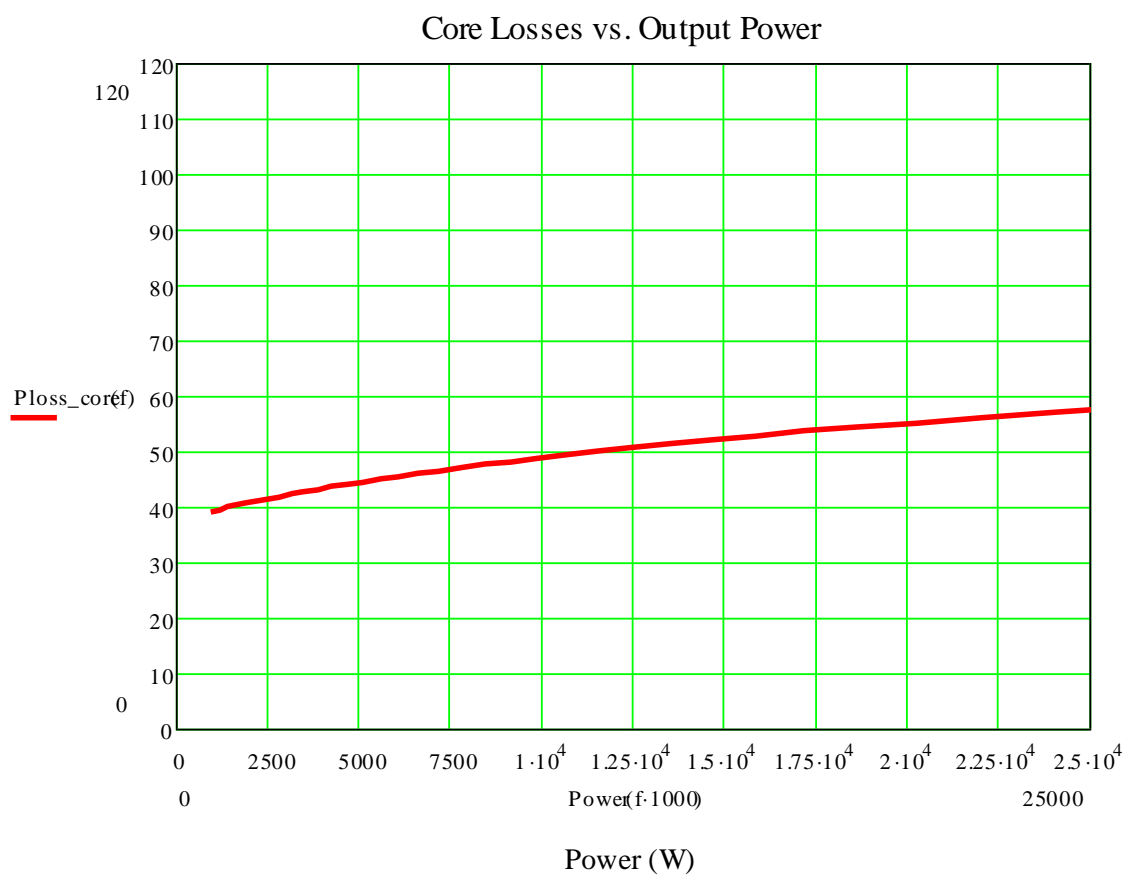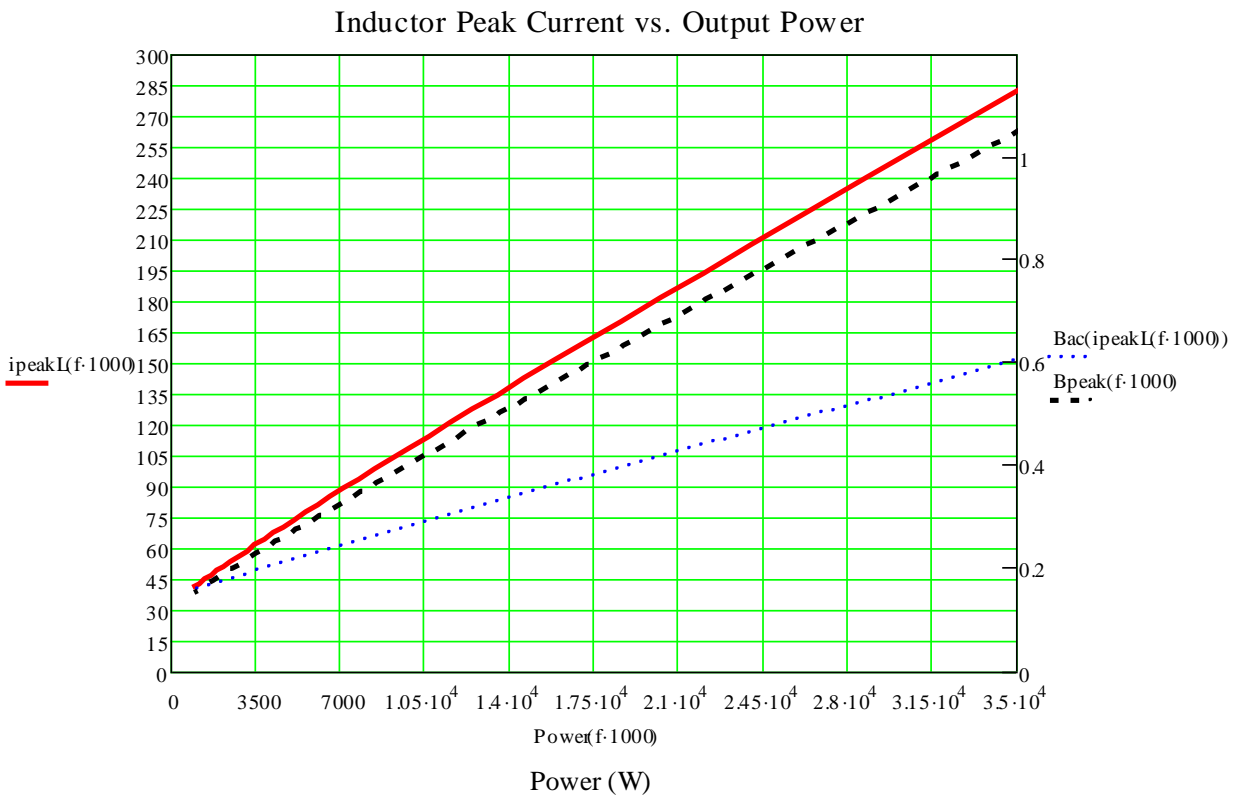
Inductor Losses vs. Frequency

Frequency in kHz

Output Power vs. Frequency

Frequency in kHz

Inductor Efficiency vs. Output Power

L_eff(f)

Power(f·1000)
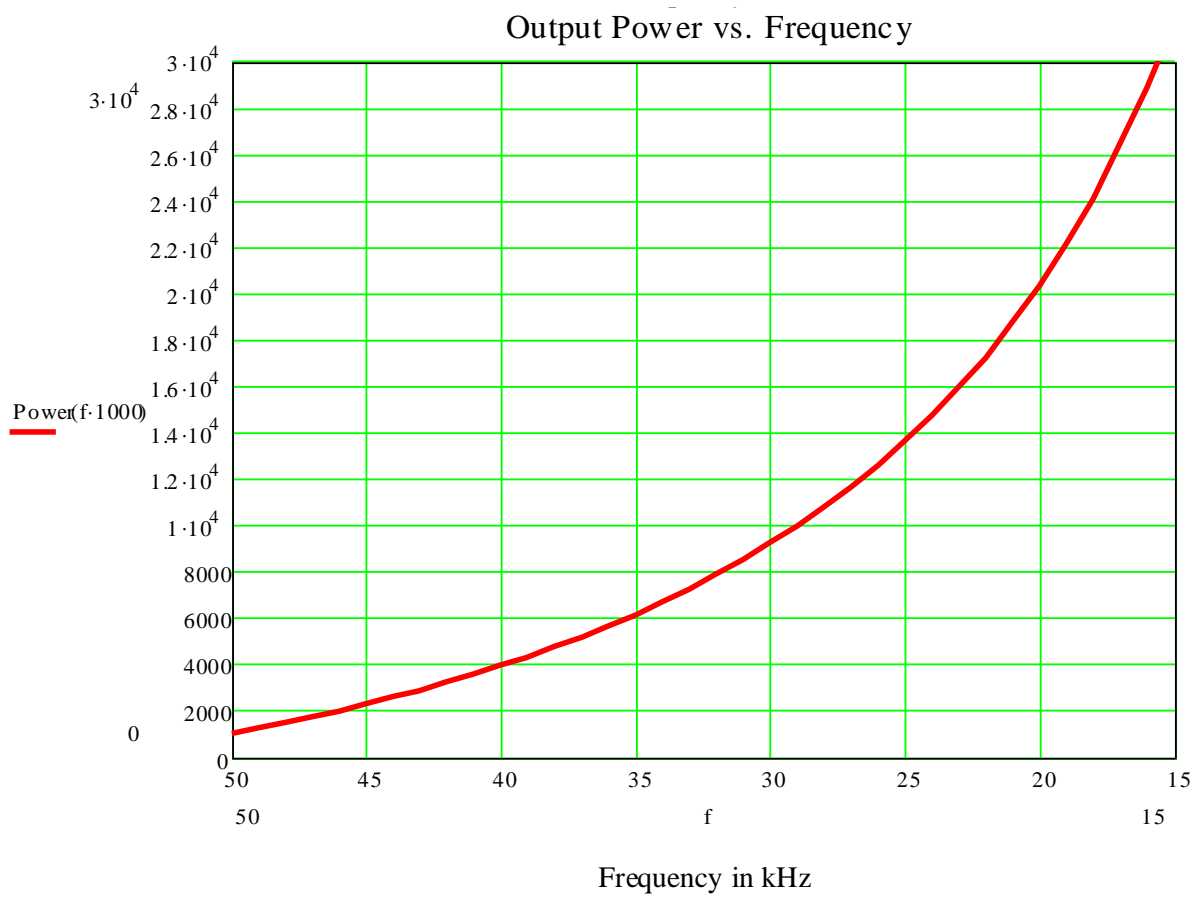
Power (W)

Inductor Temp vs. Output Power w/ coldplate
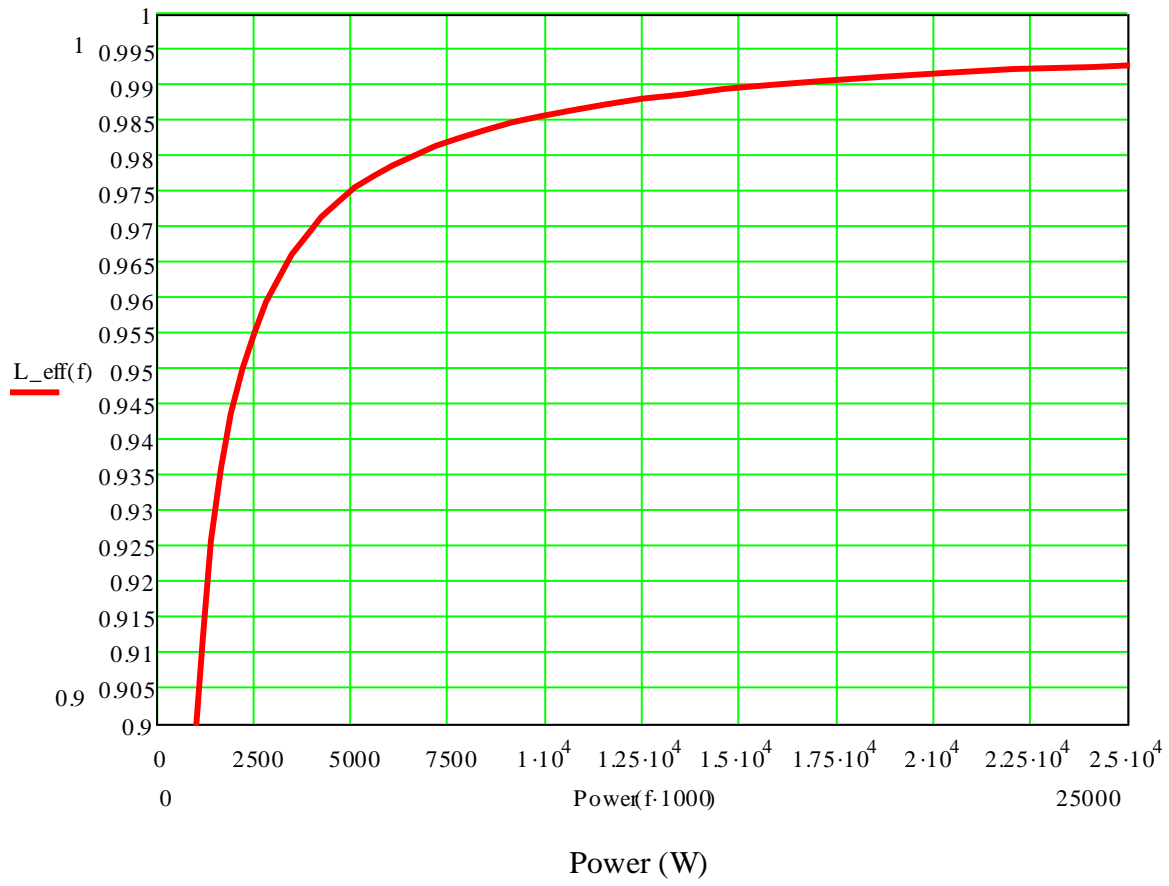
Power (W)

Inductor Temp vs. Output Power @200V in air
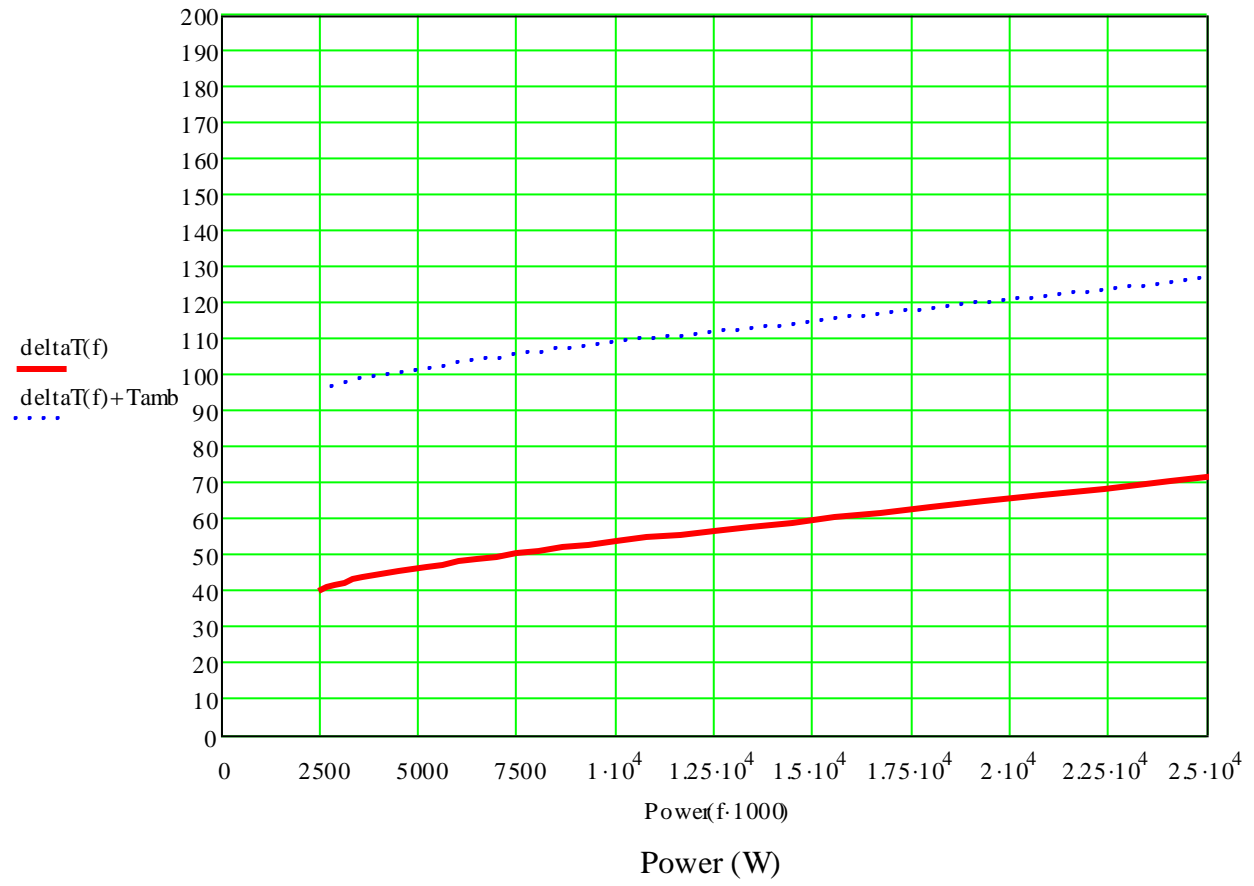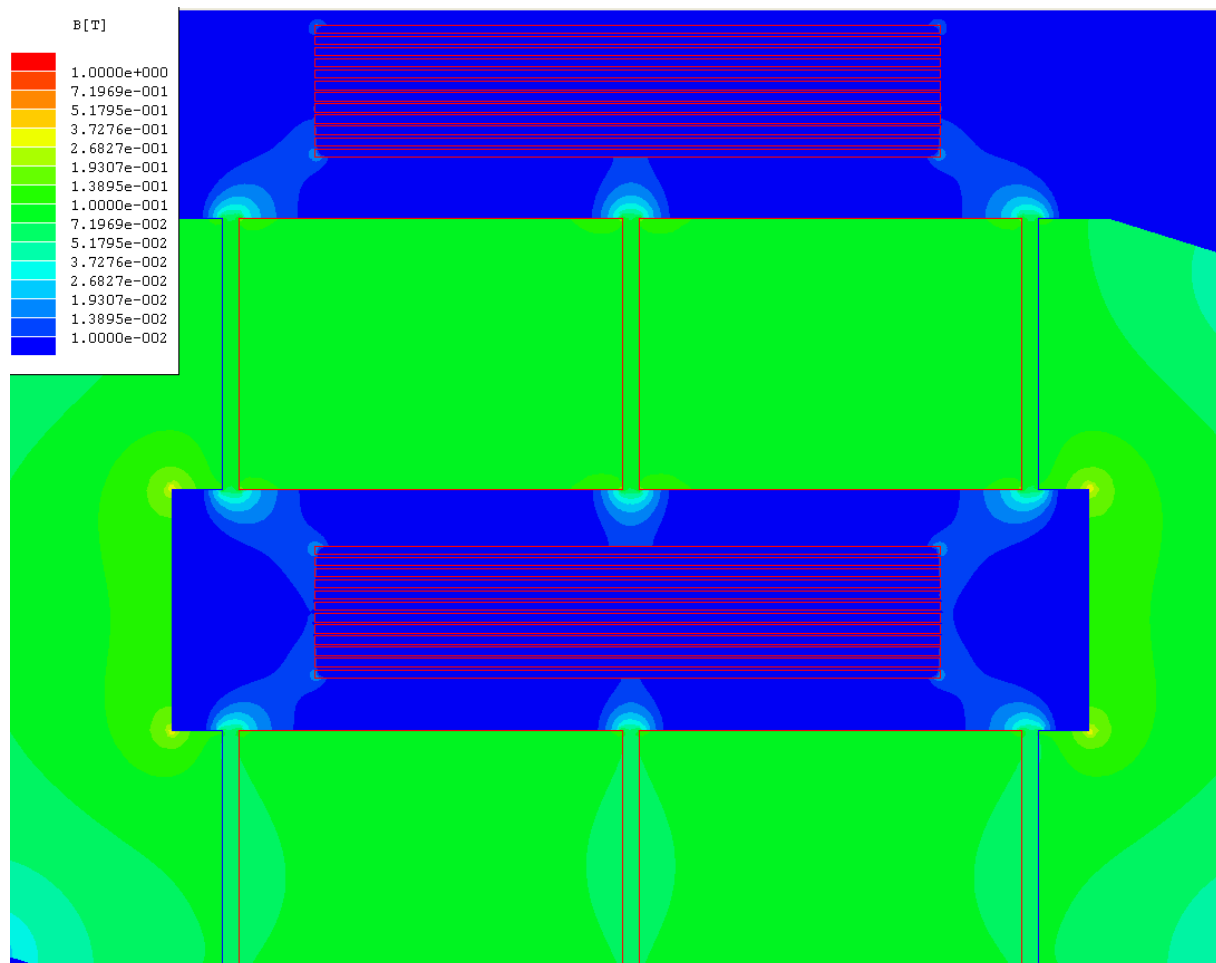
APPENDIX B: INDUCTOR FINITE ELEMENT ANALYSIS RESULTS

Case 1:
w/ 2" wide 10mil foil X4
inner: 166.77
outer: 141.7
total: 308.47
losses= 37W
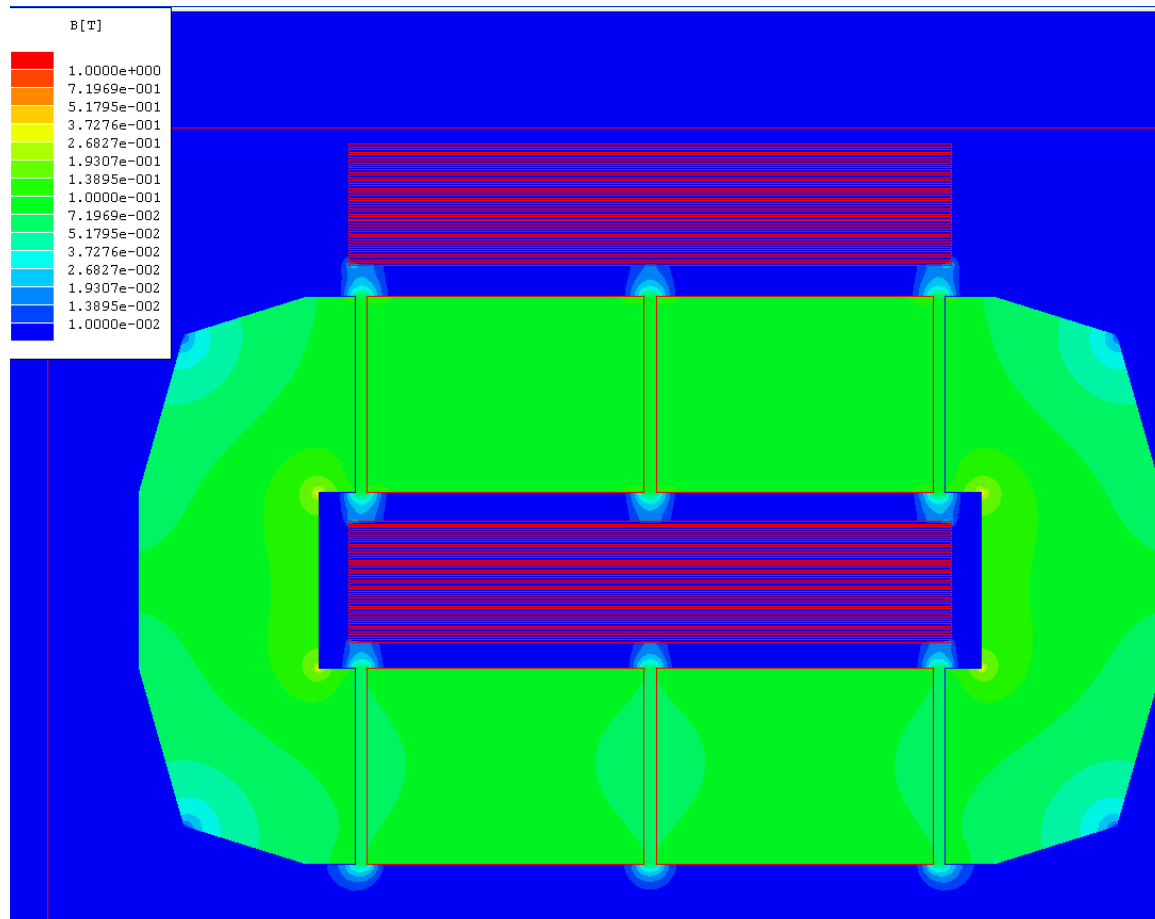
Case 2:
2x20milx1.5"
55khz
Inner: 124.35
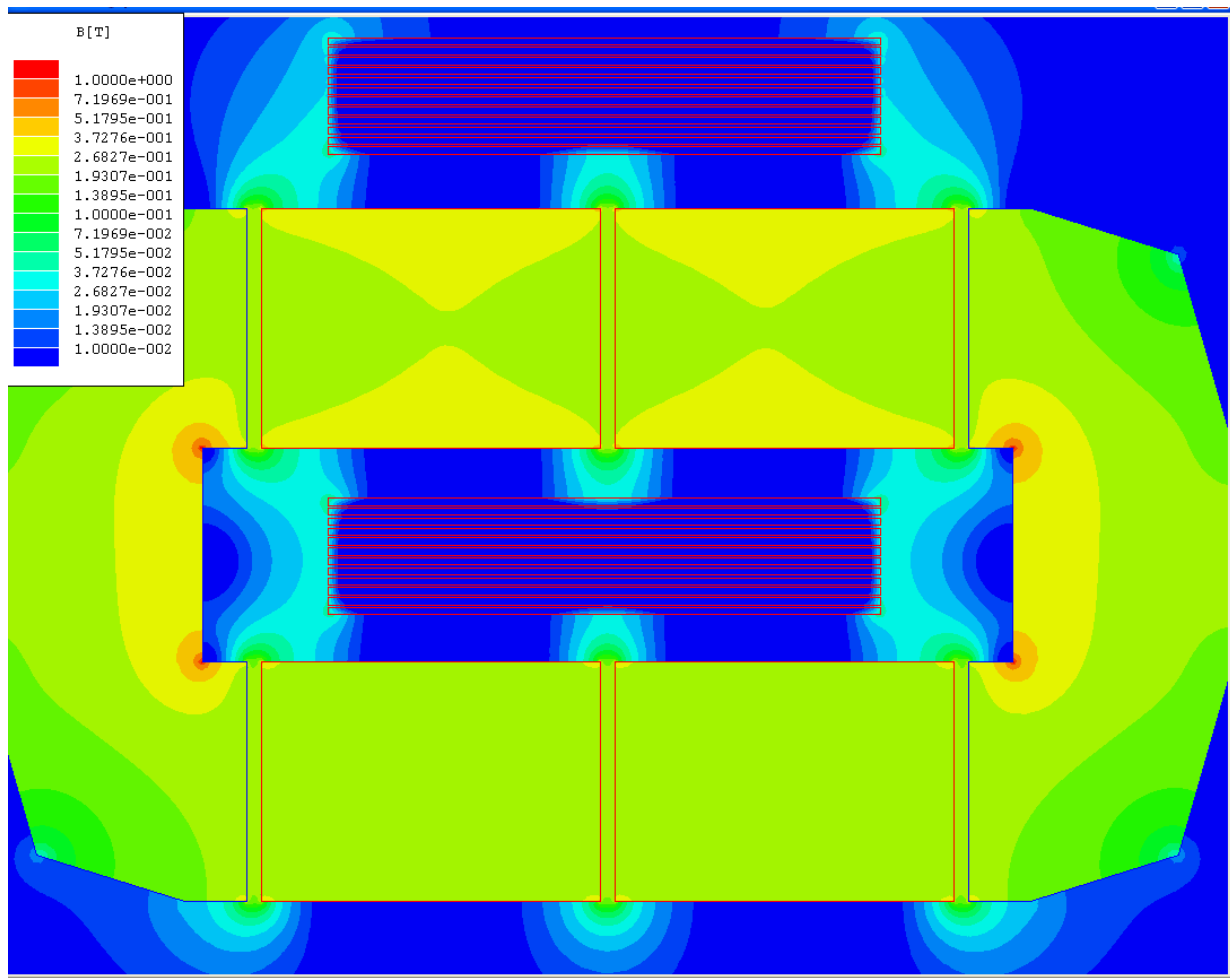**Outer: 110.6**

Total: 235
Losses:28.2W

Case 2: With 175A peak ripple, 20khz

Inner: 634   #1
Outer: 562
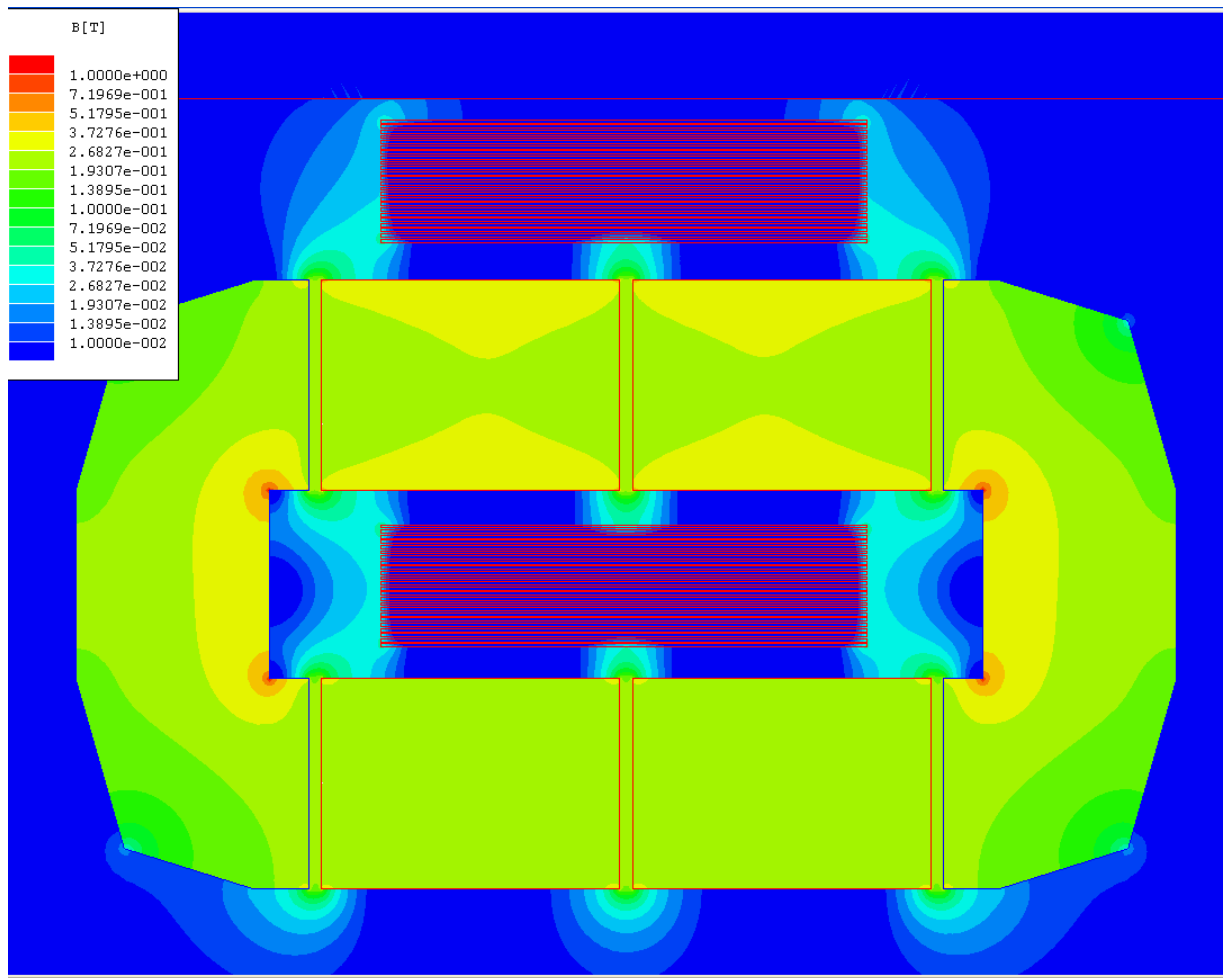
Total:1196 W/m
Losses: 143.5 W

Case 3: 175A 20khz, with 4x10milx1.5"

Inner: 722.6
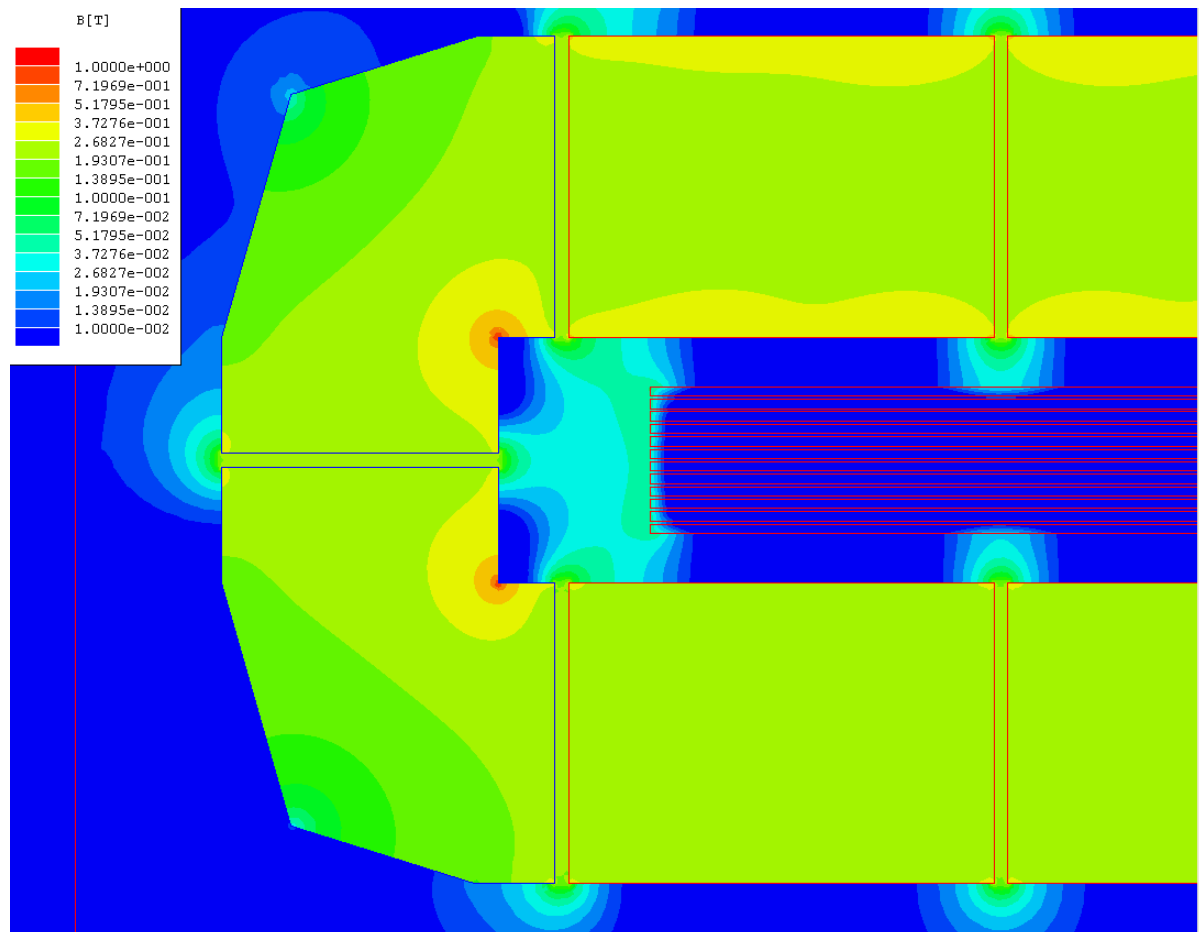**Outer: 634**

Total: 1356

Losses: 162.8

Case 4: 2x20mil 175Apeak 20khz

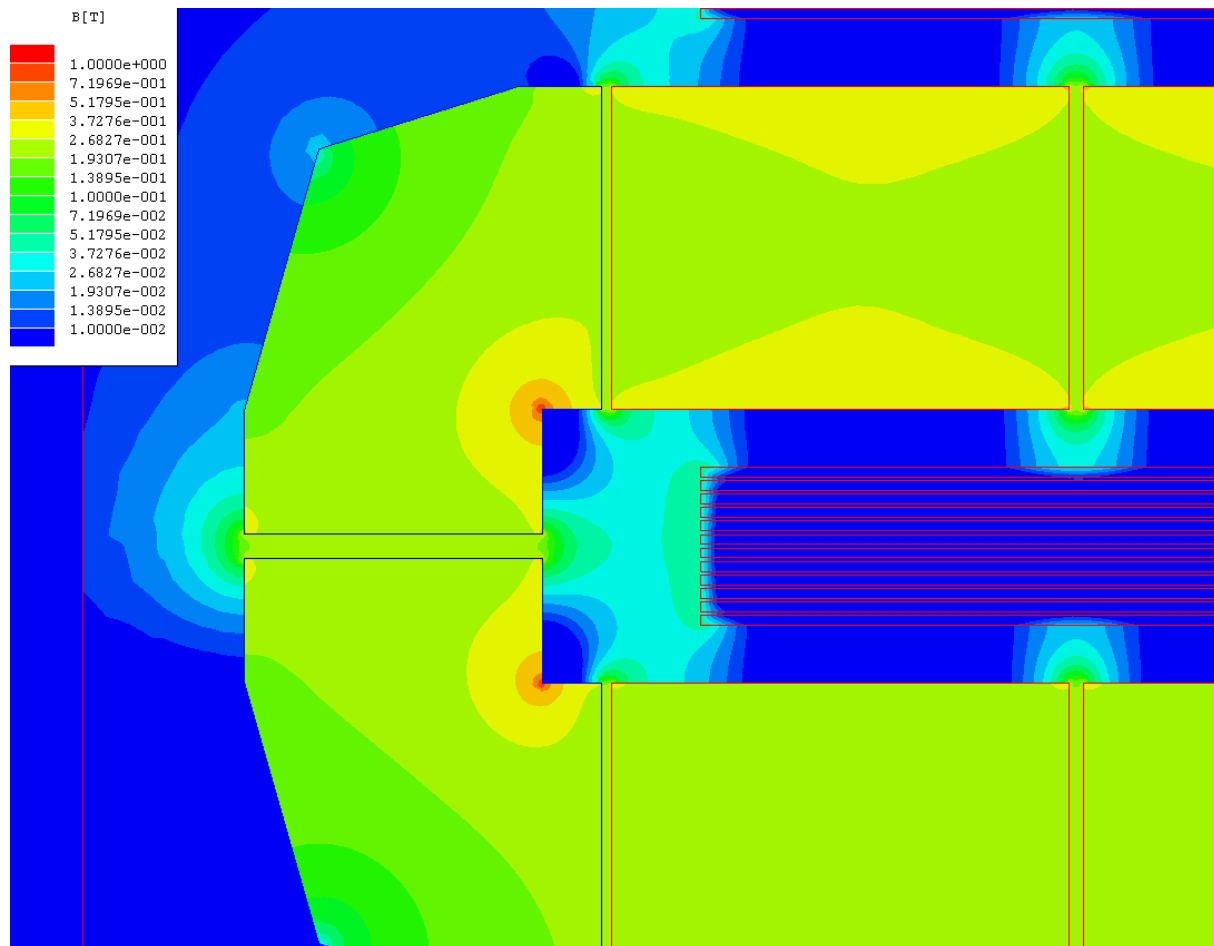**Inner:722 W/m**

Outer: 574.28 W/m

Losses: 155.6W

Case 5: 2x20mil 175Apeak 20khz .05" side gap, .02" left gaps

Inner:699.6W/m

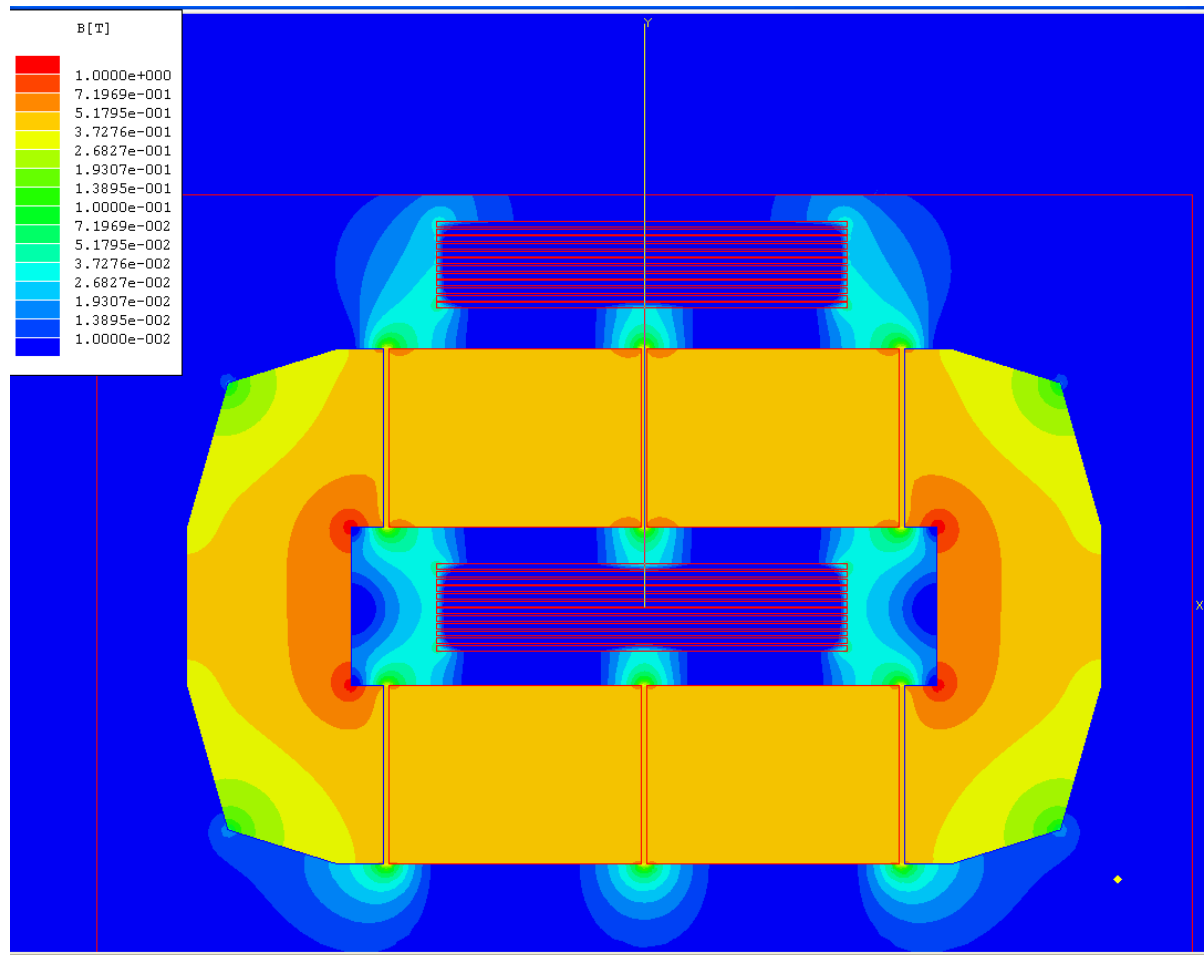**Outer: 582.16**

Losses: 153.8 W

Case 6: With 6 gap modified core, 2x20milx1.5"

175Apeak, 20khz
Inner: 636 W/m
Outer: 565.9 W/m
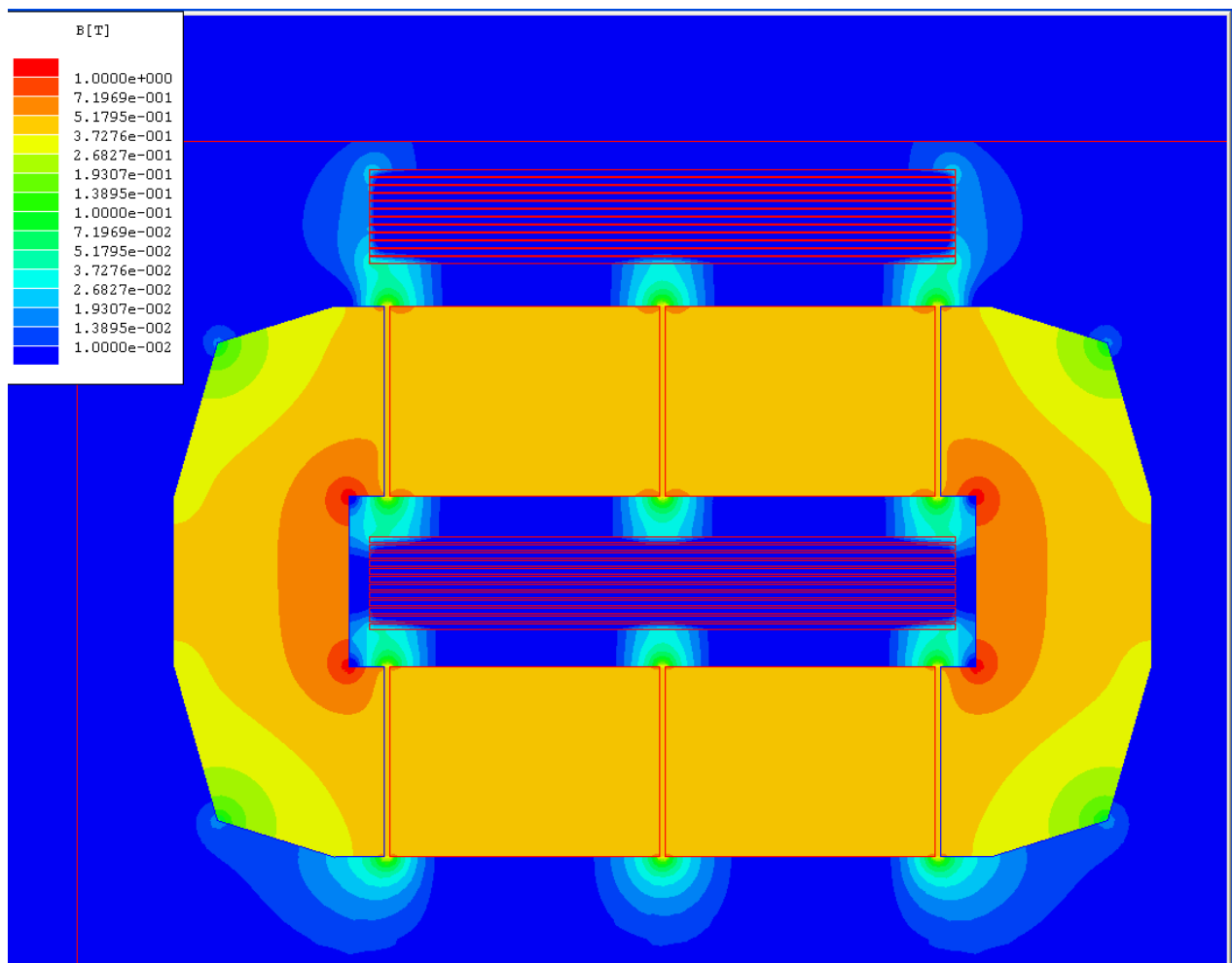**Losses: @ .12m = 144.3W**

Case 7: 2x20milx2"   Table Case #3

175Apeak 20khz

Inner: 615 W/m

Outer: 554.3 W/m

Losses: 140.3 W @ .12m

Case 8: 2x16milx2"   Table Case#4

175Apeak 20khz

Inner: 508.5

Outer: 498 W/m

Losses: 120.8W @ .12m
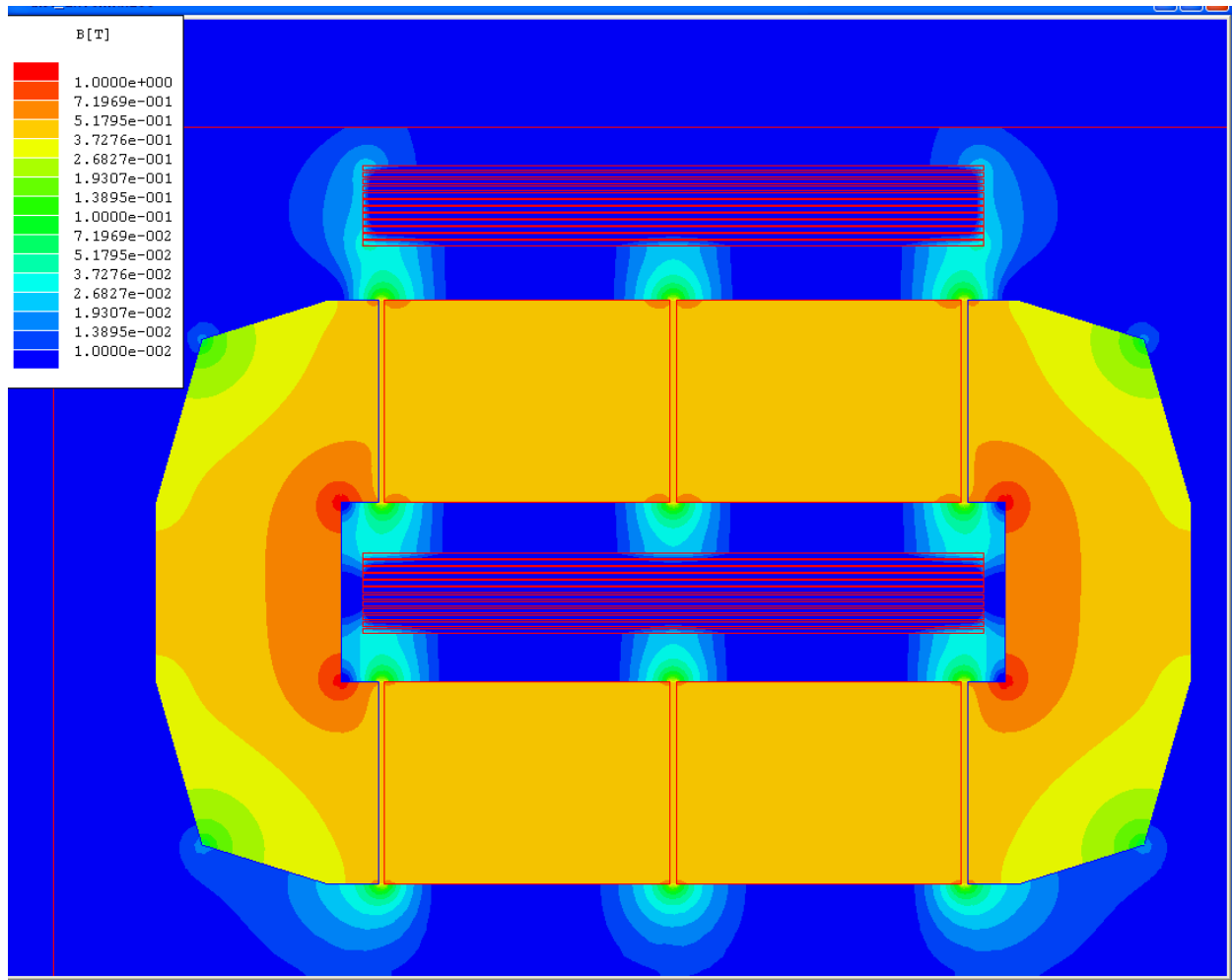
Case 9: 2x16milx1.5"
175A 20khz

Inner: 618.26
Outer: 554.6 W/m
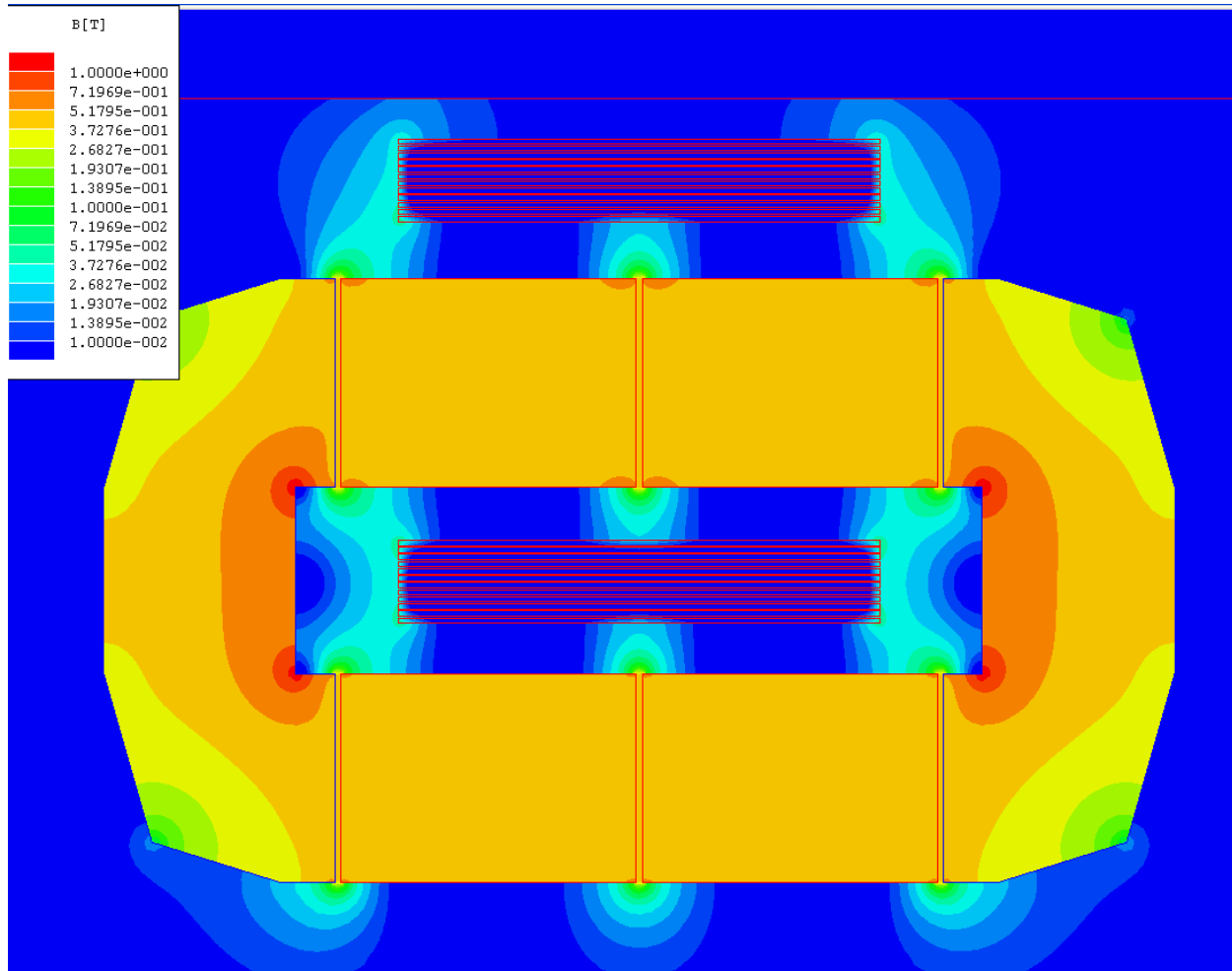
Case 10: 2x16milx1.75"   Table Case#5

175A 20khz

Inner: 580

Outer: 539 W/m

Case 11: 2x16milx2"

175A 20khz

w/AL coldplate 43mil away

coldplate loss:485.3 W/m
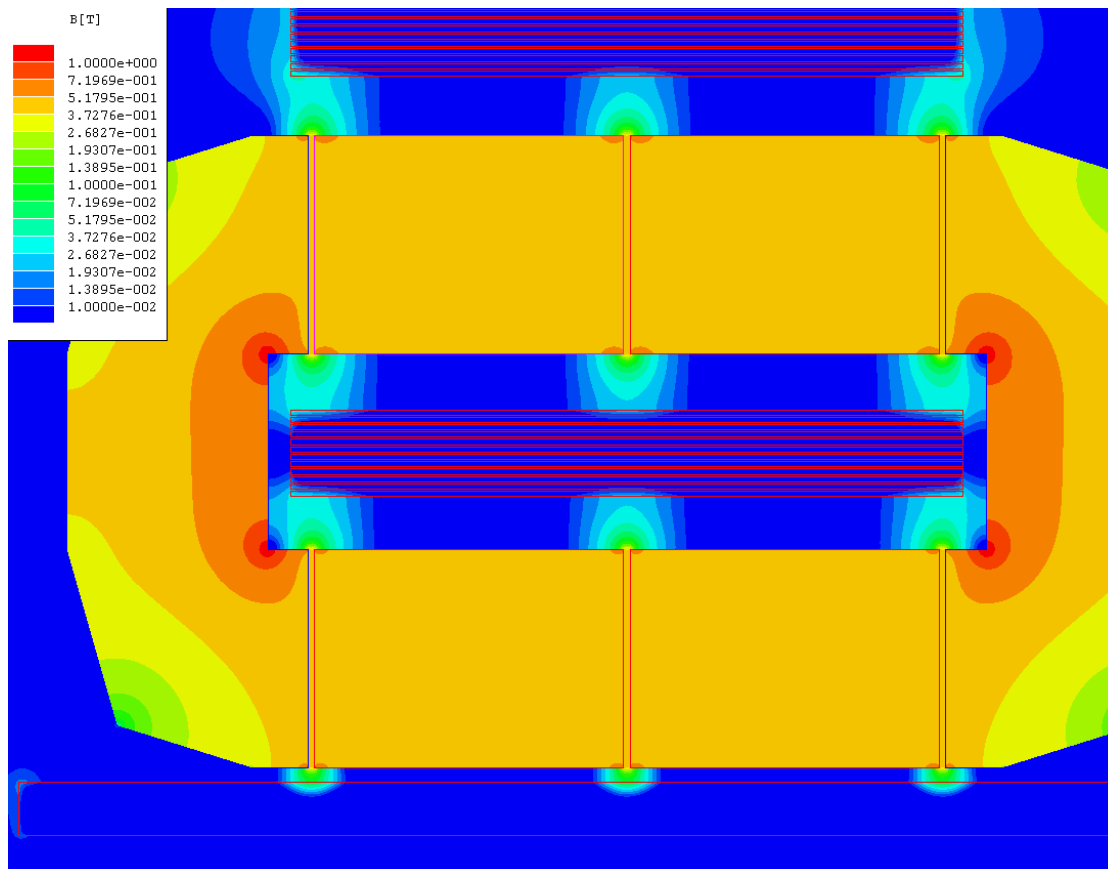
Case 12: 2x16milx2"

175A 20khz

w/AL coldplate 83mil away

coldplate loss:307 W/m
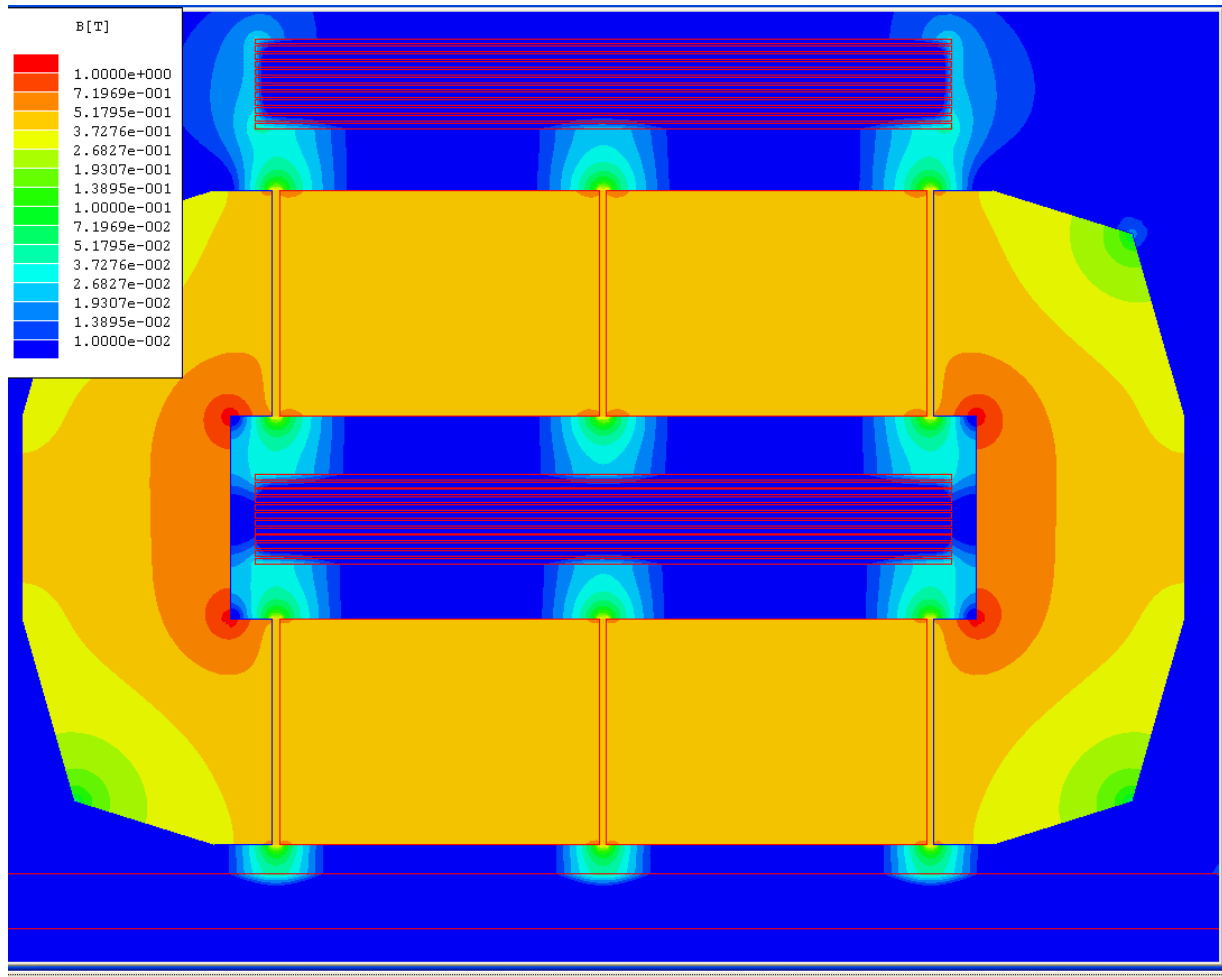
Case 13: 2x16milx2"

175A 20khz

w/AL coldplate 123mil away

coldplate loss:229W/m
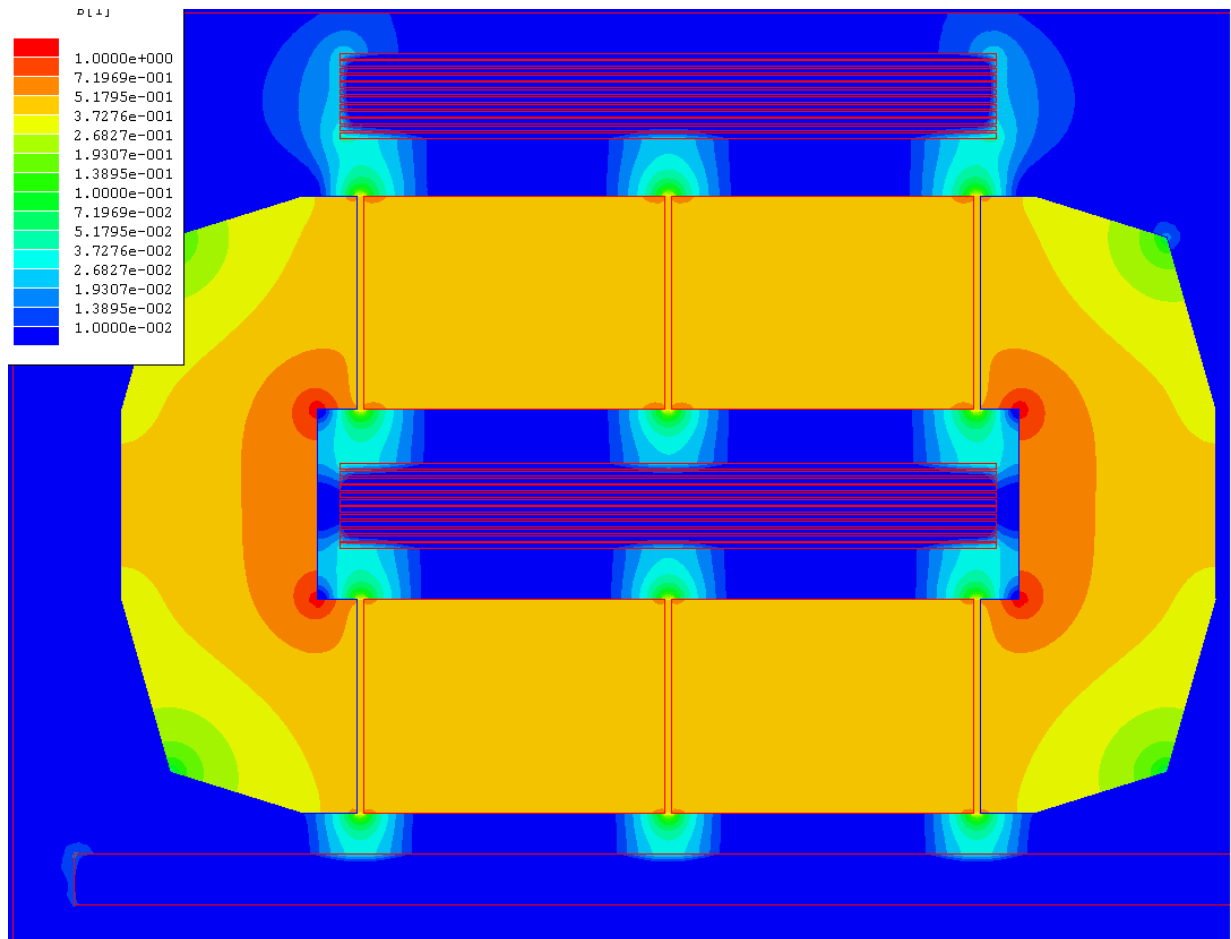
Case 14: 2x16milx2" Table Case#7

175A 20khz

Split outer, distance = .18

Inner: 507

Outer: 351 W/m

Losses: 103 W @.12m
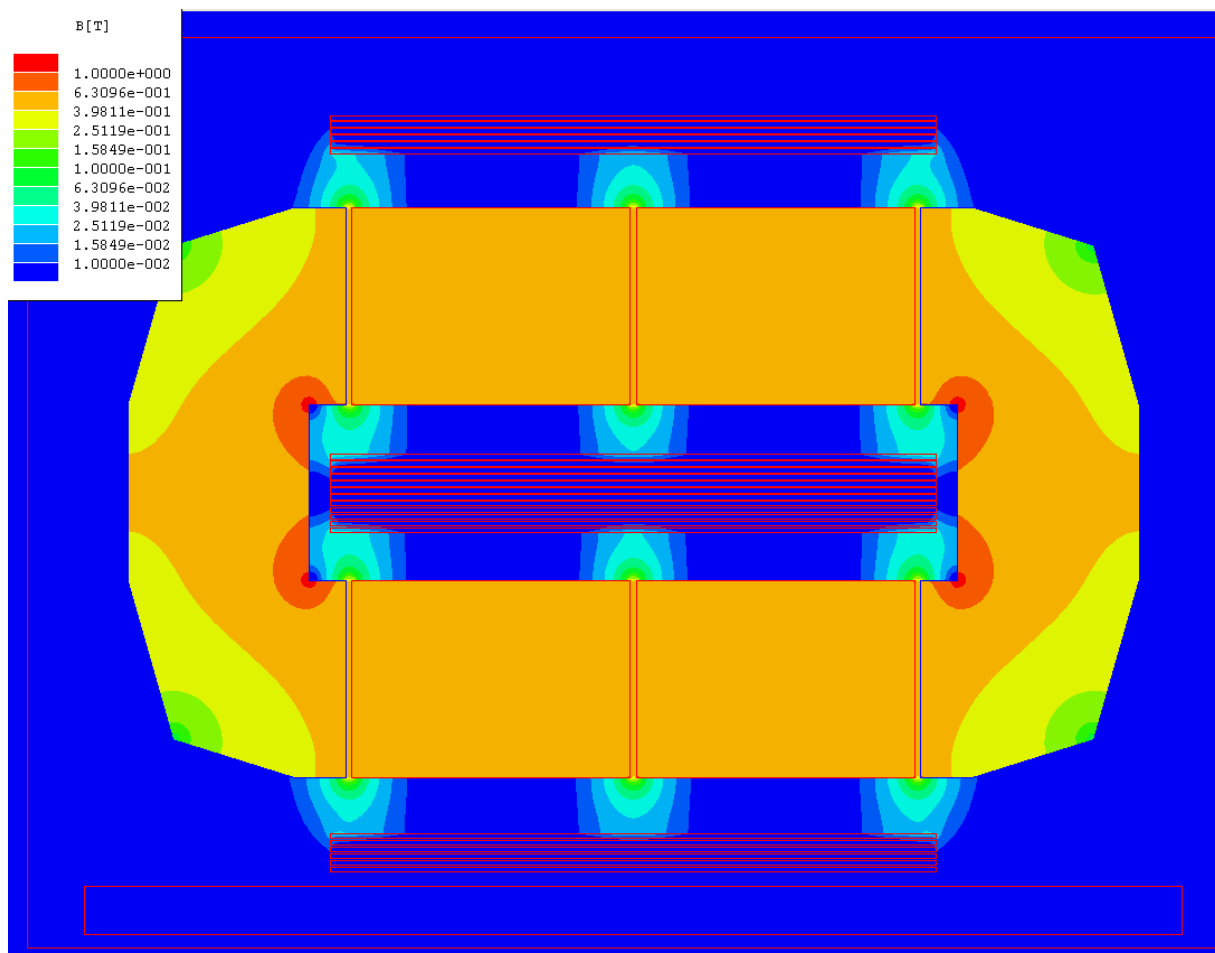
Case 15: 2x16milx2" Table Case#8

175A 20khz

Split outer, distance = .11

Inner: 507

Outer: 510 W/m
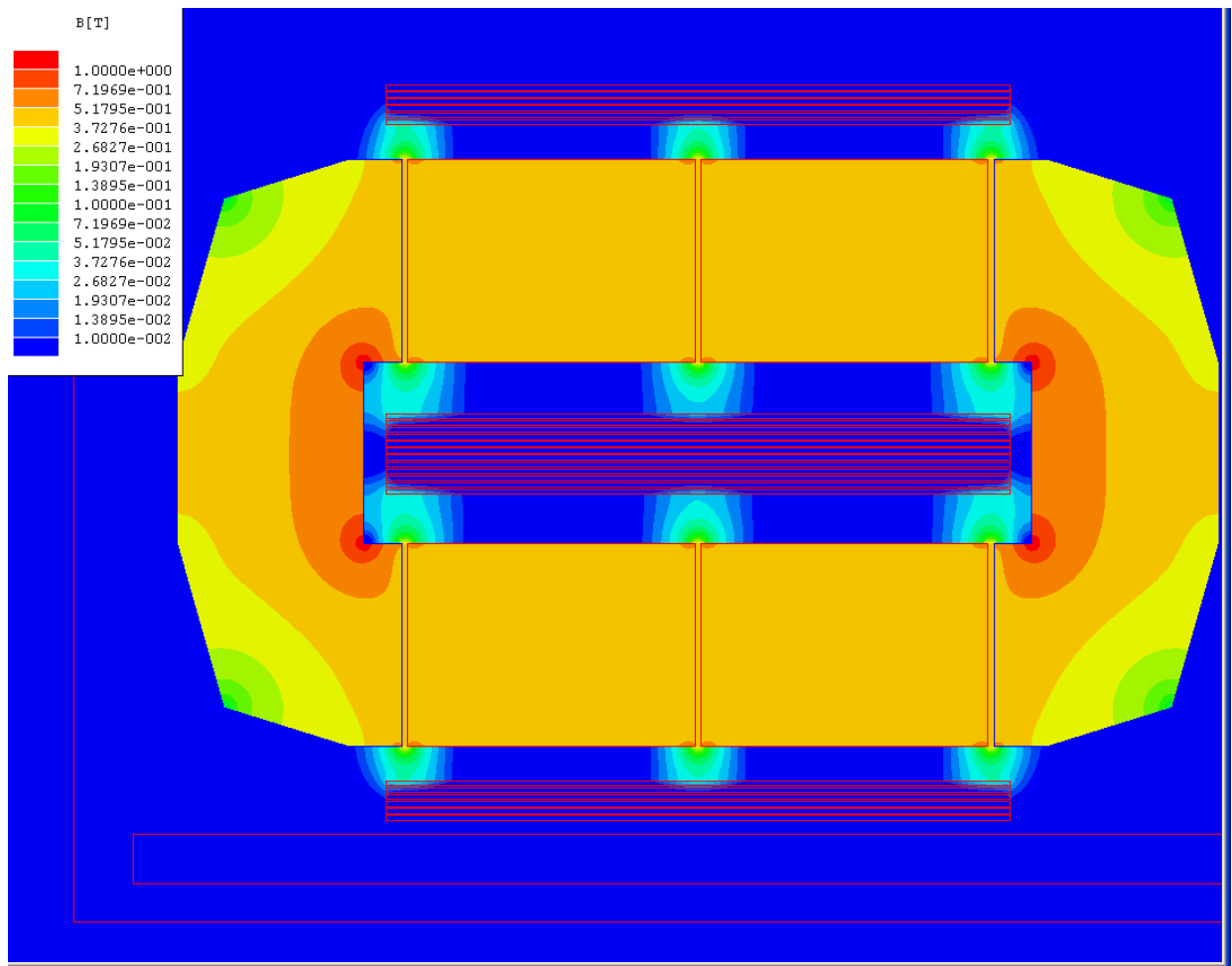
Case 16:

2x16milx2"

175A 20khz

Split outer, distance = .18

With copper thermal relief

Inner: 507.3 W/m

Outer: 198 W/m

Heat relief: 1043 W/m

Total losses = 209W @ .12m

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