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A UNIFIED APPROACH TO DYNAMIC MODELING OF HIGH SWITCHING FREQUENCY PWM CONVERTERS

by

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ABSTRACT

This dissertation will present the development of a unified approach for dynamic modeling of the PWM and soft-switching power converters. Dynamic modeling of non-linear power converters is very important for the design and stability of their closed loop control. While the use of equivalent circuits is often preferred due to simulation efficiency issues, no unified and widely applicable method for the formulation of these equivalents exists.

A review of conventional modeling technique via the method of state-space averaging will be carried out. Complete development of the averaged, equivalent circuit models for the nonlinear power switch/diode combination in modern power converters via the Vorperian method will also be given. After highlighting the limitation's of the Vorperian approach, a more widely applicable approach will be developed. This approach will capitalize on the notion that the derivative of the average of a time varying parameter is equal to the average of the derivative of that parameter.

First, the development will show the formulation of the dc modeling equations, then show how these modeling equations are implemented using PSPICE's Analog Behavioral Modeling capability. Next, the validation of the models produced will be presented via comparison to actual circuit simulation and experimental results.

The unified approach presented has several advantages over conventional techniques. The unified approach is applicable to virtually any type of converter and is not restricted by topological issues. It is easily derived by a methodical approach, it simulates accurately and quickly, and it produces models that can work equally well in CCM and DCM. Model results agree well with other averaged models and the actual circuit.

In addition, the approach will be expanded to include non-ideal effects such as conduction loss for both CCM and DCM operational modes. It will also be applied to the more complicated class of soft-switching topologies.

The purpose of the research is to develop a methodology that makes more effective use of computer simulation tools during power converter prototype development. Although, predictions about converter operation are often very good when using this unified method, it should not be considered a substitute for actual circuit simulation or bench top prototyping which often reveal subtle issues not evident from average modeling. The following work will show that the types of computer-based analysis used in the design approach are the necessary and prudent first steps in the design process.

ACKNOWLEDGMENTS

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As for my family and friends, I can only say I am so very fortunate to have such an understanding group behind me. I have been blessed with parents who have taught me the meaning of hard work and friends who care. To both, I have been more absent than not over the course of this work. With its completion, I look forward to spending more time with them.

Overall, I am glad to have had the experience and to conduct this research. Having said all that, I am also glad this effort has come to an end.

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CHAPTER 1: INTRODUCTION

Power converter design requires a method for modeling the inevitable disturbances that cause the circuit to deviate from its normal operation (source and load variation, switching time perturbation, component drift etc). Traditionally, this has presented a significant obstacle to design engineers. This difficulty centers on the fact that, in modern power converters, the transistor operates as a switch in either saturation or cut-off states. As a result, depending on the switch's state, the circuit can take on drastically different configurations. This makes conventional circuit analysis significantly more difficult. Until recently, the bulk of converter modeling was done by the tedious but effective method of state-space averaging, introduced by Dr. S. Cuk, of Cal. Tech. [1]. This method involves formulating a time averaged, state-space representation as a model. The model is then linearized and equations are solved for the linear, or so called small-signal transfer functions. While the method is effective, it is heavily dependent on matrix algebra and equation manipulation, and seems far removed from the primary objective- circuit modeling. While model complexities such as on-state resistance and storage time modulation can be addressed in this method, it is not done in a straightforward manner. Further, the method is not well suited to computer simulation.

More recently, equivalent circuit models have been developed [2]. These models are more closely related to the actual circuit and as a result, non-ideal effects are accounted for in a more straightforward way. These equivalent circuits accurately model the non-linear power converter in terms of dc characteristics, as well as large signal, or transient behavior and can be directly input into circuit simulators for simulation. Further, through the use of circuit simulators such as PSPICE, these averaged models, which are generally nonlinear, can be linearized to obtain the converter's small-signal characteristics without any special manipulation of the equivalent circuit model. The small-signal transfer function curves can be used to characterize the power converter's frequency response and serve as the basis for the controller design.

1.1 PWM Converter Overview

The largest and most common family of power electronic circuits is called switch-mode converters because they take on different circuit configurations cyclically during normal operation. This process is facilitated through the use of various nonlinear elements (such as transistors and diodes), which act as switches. As these switches change state, new circuit configurations or "modes" are developed. During operation, the main power switch is gated on for a period and then remains off until the next switching cycle begins. The combined on and off times of the main power switch is fixed and is referred to as the switching cycle, or period, T_s. While the switching period is, generally, a fixed quantity, the percentage of the period in which the switch is on, is varied, and is called the duty ratio,

D. While the switch is on, energy is drawn from the source and transferred into energy storage elements (inductors and capacitors). When the switch is turned off, this energy is transferred from the energy storage elements to the load of the power converter. By controlling the duty ratio, the energy transferred is also controlled. This process allows the output voltage of the converter to be regulated.

The number of modes of a power converter is dependent on the circuit configuration. By design, as the stored energy in the circuit is passed from one element to another, various nonlinear elements can change state creating additional circuit modes. This concept is more easily understood by example.

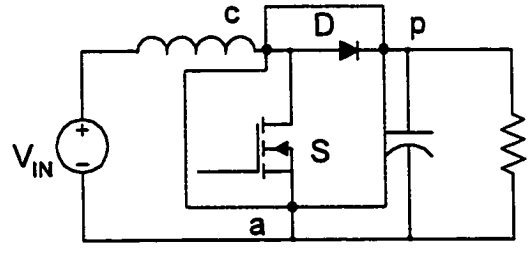


Figure 1.1: Boost converter

In Figure 1.1, one of the classic converter topologies known as boost is shown. On the diagram, the area in the box represents the nonlinear elements in the circuit. The terminal lettering scheme will be used to identify terminal characteristics when we begin to formulate the DC modeling equations.

In this circuit, Mode I begins when the switch is turned on as illustrated in Figure 1.2a. This reverse biases the diode forcing it off and separating the input portion of the circuit from the output portion. During this interval, energy is drawn from the source and stored in the inductor as a current. Controlling the time the circuit is in this mode, DTs, controls the amount of energy stored (where D is the duty ratio of the switch and takes values from 0 to 1). When the appropriate amount of energy is stored, Mode II begins and the switch is turned off as shown in Figure 1.2b. Energy stored in the inductor is transferred to the load as a current thus forcing the diode to conduct.

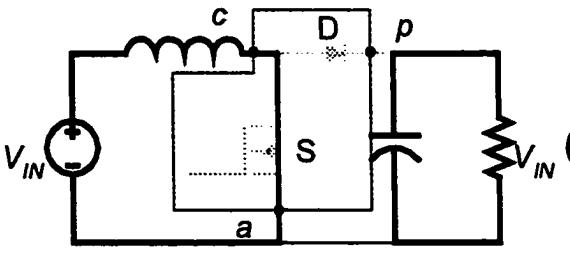


Figure (1.2a)

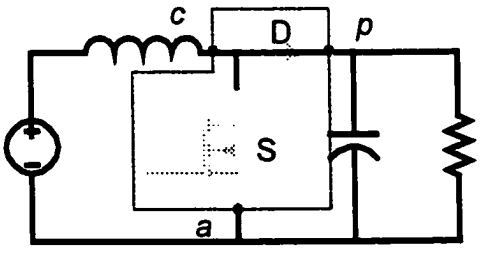


Figure (1.2b)

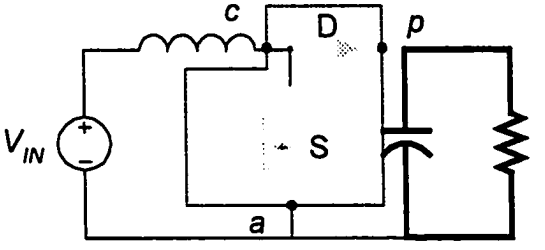


Figure (1.2c)

Figure 1.2: Equivalent circuit modes
(a.) Mode I-S on, D off (b.) Mode II-S off, D on(c.)Mode III-S off, D off

When all the stored energy is transferred to the load, the diode ceases to conduct and converter enters Mode III as shown in Figure 1.2c. The load's energy requirement is now supported by the output capacitor until the beginning of the next switching cycle. It should be noted that the discussion above assumes all the energy in the inductor is passed to the load. As a result, the inductor current goes to zero during this interval. For this reason, this type of operation is called Discontinuous Conduction Mode (DCM). Another possibility is to design the circuit so that only a portion of the energy stored in the inductor is transferred.

This type of operation is called Continuous Conduction Mode (CCM) as the inductor current is not allowed to discharge to zero. This dissertation will largely deal with the DCM mode of operation as it is more widely applicable to Power Factor Correction, hence the focus of our research at UCF. For a detailed treatment of the CCM operation see [2].

The discussion above highlights the nonlinear nature of all modern power converters. This nonlinear nature presents several design problems caused by the difficulty in effectively using circuit modeling and simulation technique. In the subsequent chapters, we will discuss these problems and then present methods for resolution.

Here we will move the discussion to an overview of modeling and simulation as it pertains to modern power converters. In particular, a key goal here is to establish the benefit of modeling the converter versus the use of the actual circuit for simulation and controller design. It will be shown that the use of equivalent circuit models will facilitate control loop design and aid in the simulation process.

As with other systems, modeling and simulation play key roles in the design and development of power converters. During the design phase, modeling and simulation help to set the optimal converter operating point, chose circuit parameters wisely, and helps to produce an effective controller to regulate the output. During the development phase, simulation allows us to evaluate converter performance prior to prototyping.

In modern power converters, classical control loop design techniques (Bode, Nyquist, Root Locus, etc) are not directly applicable, and are only valid for linear systems. From the

previous section its clear that the power converter is highly nonlinear. As a result, a linearized model of the power stage is necessary to facilitate the control loop design process. An objective here is to evaluate existing modeling techniques and develop our own method that will facilitate circuit modeling and computer simulation.

The following sections will provide the detail on both the several conventional modeling techniques. Thorough derivations will be presented so that a comparison can be made to the approach presented here.

1.2 The Method of State-Space Averaging

Until recently, most power stage modeling was done by a matrix manipulation method called state-space averaging [1]. The method involves the formulation of a state matrix representation for each mode of operation. For the boost example given earlier, this would mean three different sets of matrices corresponding to the three modes of circuit operation. These state representations are then time averaged to create a single matrix representation of the "averaged" circuit. This single set of state equations can then be linearized by conventional algebraic techniques (Taylor Series Expansion) [1]. The final result is a small-signal transfer function representing the frequency response characteristics of the power stage. Based on this information, the design of the controller can be tailored to these characteristics.

While this method is functional, it has several significant shortcomings. First, since the method is primarily mathematical in nature, it is far removed from the actual circuit of interest. Although the method provides a closed form representation of the power stage in the frequency domain, it does not readily produce an equivalent circuit in terms of a time domain representation. In order to do time-based simulation (transient), designers must either use the actual circuit for simulation or fabricate a circuit model from the state equations generated earlier in the state-space averaging method. Often, the process of developing this equivalent circuit model from the equations requires some level of creativity and experience as no standard methods had existed [2].

The method of state-space averaging allows us to represent the power stage as a linear model (transfer function) and thereby allows the use of classic control theory for design of the closed loop control. However, in terms of time domain simulation, as stated earlier, the state-space averaging method does not readily produce a time domain model suitable for circuit simulation (complex circuit manipulation is required). At this point the reader might note that having tackled the control design issue what further need for modeling is there, particularly when the actual circuit can be used in the simulator for time domain simulations.

While the actual circuit can be used in the circuit simulator, an equivalent circuit model is often preferred. The abrupt discontinuities that occur in the actual circuit as the switch transitions state forces the calculated time step in PSPICE simulation to extremely small

increments. These small increments mean an increased number of calculated points and result in more convergence problems and significantly longer simulation times [3].

As a result of these difficulties, the design process has traditionally followed in two different and separate areas. The first involved using state-space averaging to develop a frequency domain model of the power stage for control loop design. The second involved time domain simulation using cleverly formulated equivalent circuit models or the brute force approach, direct simulation of the actual circuit [2].

The discussion will now provide the detailed approach and illustrate the procedure. The topology to be modeled was chosen because it is not easily handled by conventional, averaged equivalent circuit techniques. These difficulties will be discussed in greater detail in subsequent sections. However, these issues do not effect the application of the state-space averaging method, which is generally, more widely applicable.

The methodology is shown in Figure 1.3 as a step by step process which culminates in small-signal transfer functions representing the power stage.

Examining the methodology confirms the notion that state-space averaging is, generally, straightforward. However, under the DCM condition, several assertions made by Cuk are not so obvious. Further, some of these assertions have been scrutinized in open literature [2].

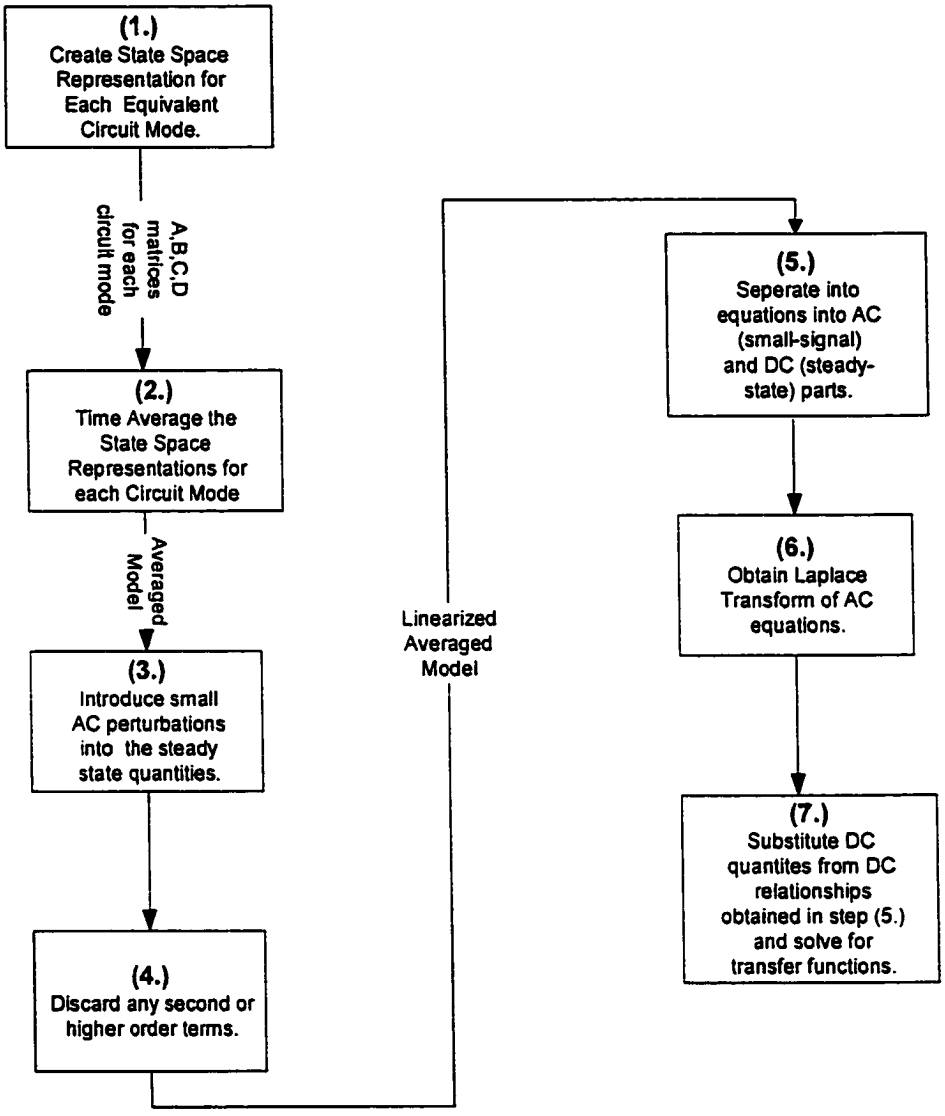


Figure 1.3: State-space averaging step by step process

The DCM assumptions differ from the CCM development in the state-space averaging method. The most significant assertion is that Cuk states in [1] that, "the inductor current,

i_L, ceases to be a true state variable since it has lost its dynamic properties"...(since it does not have free boundary conditions) and he goes further to say that as a result, Equation (1.1) is valid.

$$\frac{d}{dt} i_L = 0 \tag{1.1}$$

Thus, the system of the state model is reduced by an order for each inductor in DCM.

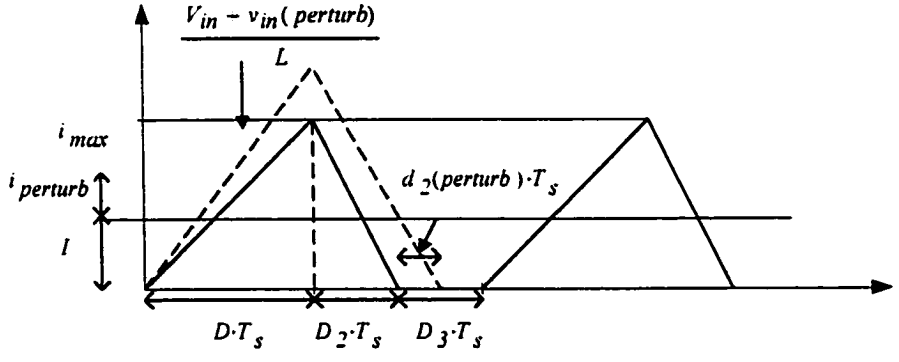


Figure 1.4: Inductor current in DCM

Figure 1.4 illustrates the dynamic properties of inductor current in DCM. Line voltage perturbation does introduce perturbations in the output voltage. Further, from the figure, it is clear that this also causes perturbations in the average inductor current, where the average takes on a unique definition and is defined over the interval, $(D+D_2)T_s$.

Cuk also states that the DCM case is in sharp contrast to the CCM case where the average inductor current does not change under small-signal perturbation but rather the initial and final conditions at 0 and T_s change to accommodate, maintaining the average value. Based on this, the Cuk's argument is finalized by stating that the average inductor current, as defined above, is the quantity that reflects the effect of the introduced perturbation.

To summaries the above discussion, the following assertions by Cuk in the method of state-space averaging set DCM apart from CCM.

1. Each discontinuous inductor current derivative is set to zero in the state-space representation.
2. An additional equation is added which represents the Cuk defined average inductor current to replace the "lost" state variable.

In particular, Cuk's assertion that system order reduction accompanies DCM operation is actively refuted in [2] stating that this is neither theoretically nor experimentally justifiable. Details about this argument will be explored in subsequent sections.

Having presented a flowchart of the methodology of state-space averaging, we now apply the approach to the single stage, single switch, separated PWM Switch converter of Figure 1.5 with its modes operation Figure 1.6. A description of the operation of this circuit is presented in [4] and will not be discussed here. However, it is important to note that the inductors in the circuit operated in DCM and as such, the assertions made previously apply.

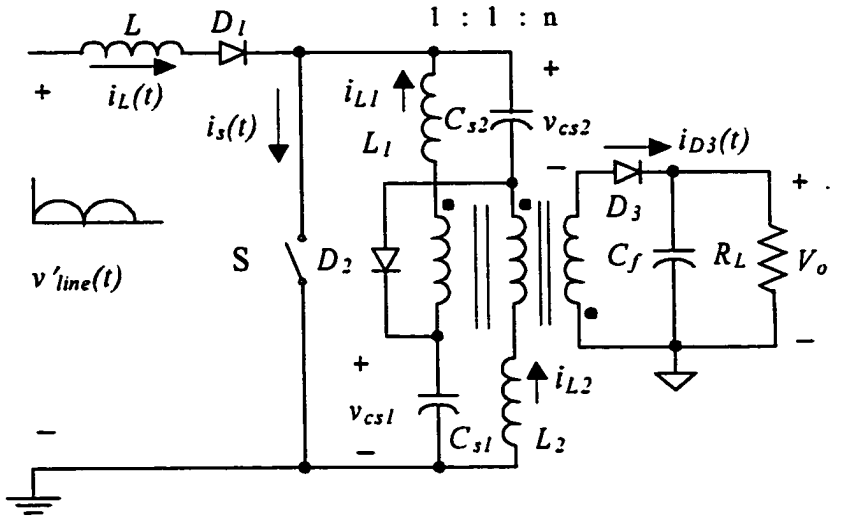


Figure 1.5: Single-stage single switch converter

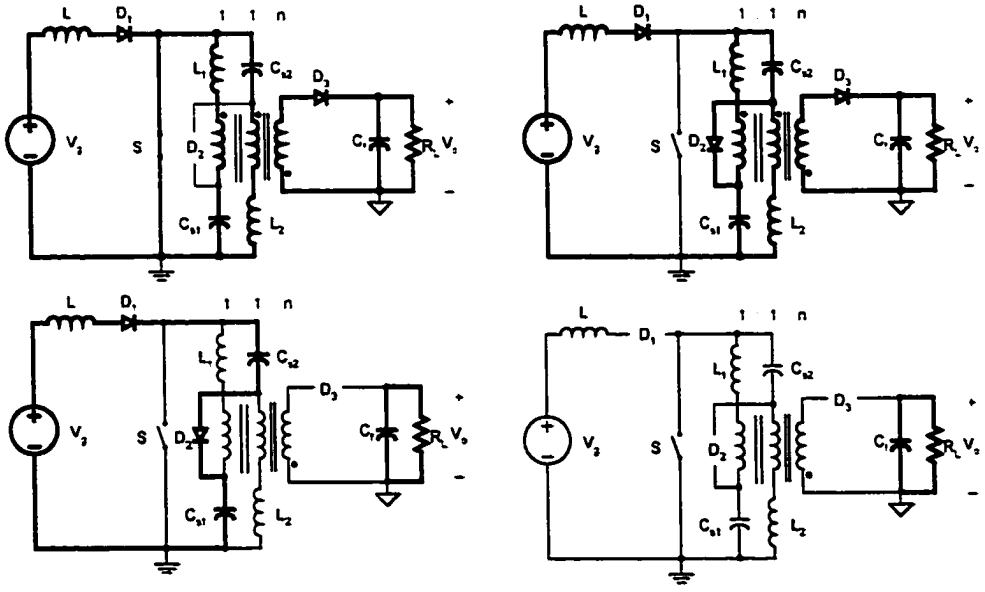


Figure 1.6: Modes of operation of single-stage single switch converter

From the flowchart of Figure 1.3, the first step is to create a state-space representation for each circuit mode of Figure 1.6. It should be noted that since $L_p=L_1=L_2$ and $C_s=C_{s1}=C_{s2}$ appear in identically functioning branches, inclusion of both branches in the state vector would lead to a non-minimal realization. Therefore, the state vector is fourth order and is given as: $[\, v_{cs}\ v_{Co}\ i_L\ i_{Lp}\,]$.

The A matrix development is step one in the methodology and is shown as Equations (1.2)-(1.4)

$$A_1 \equiv \begin{pmatrix} 0 & 0 & 0 & -\frac{1}{C_s} \\ 0 & -\frac{1}{R\cdot C_o} & 0 & \frac{2}{n\cdot C_0} \\ 0 & 0 & 0 & 0 \\ \frac{1}{L_p} & -\frac{1}{n\cdot L_p} & 0 & 0 \end{pmatrix} \quad A_2 \equiv \begin{pmatrix} 0 & 0 & \frac{1}{C_s} & \frac{1}{C_s} \\ 0 & -\frac{1}{R\cdot C_o} & 0 & \frac{2}{n\cdot C_o} \\ -\frac{2}{L} & 0 & 0 & 0 \\ -\frac{1}{L_p} & -\frac{1}{n\cdot L_p} & 0 & 0 \end{pmatrix}$$

$$A_3 \equiv \begin{pmatrix} 0 & 0 & \frac{1}{C_s} & 0 \\ 0 & -\frac{1}{R\cdot C_o} & 0 & 0 \\ -\frac{2}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \quad A_4 \equiv \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R\cdot C_o} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \tag{1.2}$$

$$A_1\cdot d + A_2\cdot d_1 + A_3\cdot d_2 + A_4\cdot\left[1 - (d + d_1 + d_2)\right] \equiv A \tag{1.3}$$

$$A = \begin{bmatrix} 0 & 0 & \frac{(d_1 + d_2)}{C_s} & \frac{(-d + d_1)}{C_s} \\ 0 & \frac{-1}{(R \cdot C_o)} & 0 & 2 \cdot \frac{(d + d_1)}{(n \cdot C_o)} \\ -2 \cdot \frac{(d_1 + d_2)}{L} & 0 & 0 & 0 \\ \frac{-(-d + d_1)}{L_p} & \frac{-(d + d_1)}{(n \cdot L_p)} & 0 & 0 \end{bmatrix} \quad (1.4)$$

The next step is to average the state-space representations developed in step one above. This is done by Equation (1.3) and yields a final result shown as Equation (1.4).

The B and C matrices are formulated in a similar fashion and are shown as Equations (1.5) and (1.6).

$$B = \begin{bmatrix} 0 \\ 0 \\ \frac{(d + d_1 + d_2)}{L} \\ 0 \end{bmatrix} \quad (1.5)$$

$$C = (0 \ 1 \ 0 \ 0) \quad (1.6)$$

Based on the Cuk DCM assumptions presented earlier, additional equations are obtained by writing the expressions for the Cuk defined average inductor currents. These equations are readily obtained by inspection of the instantaneous waveforms of the converter shown in Figure 1.7.

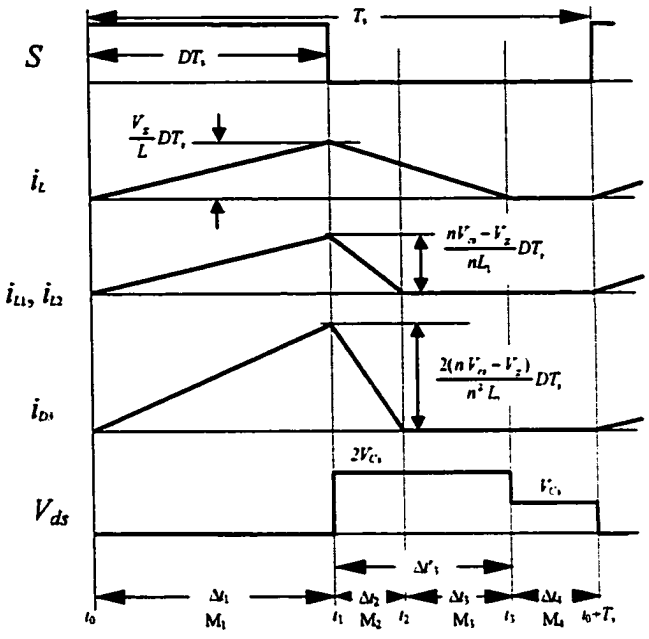


Figure 1.7: Instantaneous waveforms of single-stage single switch converter

Although the DC and AC relationships are usually derived simultaneously by separation, the development here will derive the DC relationships first for the sake of clarity. The DC relationships can be found by setting derivative vector in the state-space representation to zero and substituting DC variable names throughout. In the DC state vector, I_L and I_{Lp}= I_{L1}= I_{L2} are directly substituted

$$\dot{x} = A \cdot x + B \cdot u \tag{1.7}$$

$$y = C \cdot x$$

$$A \cdot X + B \cdot U = 0 \tag{1.8}$$

$$Y = C \cdot X$$

$$\begin{bmatrix} 0 & 0 & \frac{(D_1 + D_2)}{C_s} & \frac{(-D + D_1)}{C_s} \\ 0 & \frac{-1}{(R \cdot C_0)} & 0 & 2 \cdot \frac{(D + D_1)}{(n \cdot C_0)} \\ -2 \cdot \frac{(D_1 + D_2)}{L} & 0 & 0 & 0 \\ \frac{-(-D + D_1)}{L_p} & \frac{-(D + D_1)}{(n \cdot L_p)} & 0 & 0 \end{bmatrix} \cdot \begin{pmatrix} V_{cs} \\ V_o \\ \frac{1}{2} \cdot \frac{V_g}{L} \cdot D \cdot T_s \\ \frac{1}{2} \cdot \frac{n \cdot V_{cs} - V_o}{n \cdot L_p} \cdot D \cdot T_s \end{pmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{(D + D_1 + D_2)}{L} \\ 0 \end{bmatrix} \cdot V_g = 0 \tag{1.9}$$

Separating the matrix representation of Equation (1.9) and normalizing by Equation set (1.10), the DC relationships are presented in Equation set (1.11).

$$M = \frac{V_o}{V_g} \qquad m = \frac{V_{cs}}{V_o} \qquad \tau_n = \frac{\frac{L}{R}}{T_s} \qquad k = \frac{L_p}{L} \tag{1.10}$$

$$\left[m \cdot n \cdot (D - D_1) + D_1 - D\right] \cdot M + (-D_1 - D_2) \cdot n \cdot k = 0$$

$$(m \cdot n - 1) \cdot D^2 + (m \cdot n \cdot D_1 - D_1) \cdot D - n^2 \cdot k \cdot \tau_n = 0$$

$$2 \cdot m \cdot M \cdot (D_1 + D_2) - D - D_1 - D_2 = 0$$

$$m \cdot n \cdot (D - D_1) - D - D_1 = 0 \tag{1.11}$$

Using MathCAD's symbolic solver, Equation set (1.11) can be solved for any variable in terms of constant circuit parameters. The solution of these equations provides the DC

operating point data used for substitution into the AC equations in step 7 of Figure 1.3. Next, the AC relationships will be presented as Equation set (1.12).

$$C_s \cdot \frac{d}{dt} v_{cs} = (d_1 + d_2) \cdot i_L + (d_1 - d) \cdot i_{Lp}$$

$$C_o \cdot \frac{d}{dt} v_o = \frac{-v_o}{R} + \frac{2 \cdot (d + d_1)}{n} \cdot i_{Lp}$$

$$L \cdot \frac{d}{dt} i_L = -2 \cdot (d_1 + d_2) \cdot v_{cs} + (d + d_1 + d_2) \cdot v_g$$

$$L_p \cdot \frac{d}{dt} i_{Lp} = (d - d_1) \cdot v_{cs} - \frac{(d_1 + d)}{n} \cdot v_o$$

$$i_L = \frac{1}{2} \cdot \frac{v_g}{L} \cdot d \cdot T_s$$

$$i_{Lp} = \frac{1}{2} \cdot \frac{\left(v_{cs} - \frac{v_o}{n} \right)}{L_p} \cdot d \cdot T_s \qquad (1.12)$$

Next, small perturbations are introduced into the steady state quantities by substituting Equation set (1.13) into Equation set (1.12), and then by setting discontinuous inductor currents to zero in accordance with the Cuk method to yield Equation set (1.14).

$$v_g \equiv V_g + v_{gac} \qquad i_{Lp} \equiv I_{Lp} + i_{Lpac}$$

$$v_{cs} \equiv V_{cs} + v_{csac} \qquad d \equiv D + d_{ac}$$

$$v_o \equiv V_o + v_{oac} \qquad d_1 \equiv D_1 + d_{1ac}$$

$$i_L \equiv I_L + i_{Lac} \qquad d_2 \equiv D_2 + d_{2ac} \tag{1.13}$$

$$C_s \frac{d}{dt} v_{csac} \equiv (D_1 + D_2)\cdot i_{Lac} + (d_{1ac} + d_{2ac})\cdot I_L + (D_1 - D)\cdot i_{Lpac} + (d_{1ac} - d_{ac})\cdot I_{Lp}$$

$$C_o \frac{d}{dt} v_{oac} \equiv \frac{-v_{oac}}{R} + \frac{2}{n}\cdot\left[(D + D_1)\cdot i_{Lpac} + (d_{ac} + d_{1ac})\cdot I_{Lp}\right]$$

$$0 \equiv -2\cdot(D_1 + D_2)\cdot v_{csac} - 2\cdot(d_{1ac} + d_{2ac})\cdot V_{cs} + (D + D_1 + D_2)\cdot v_{gac} + (d_{ac} + d_{1ac} + d_{2ac})\cdot V_g$$

$$0 \equiv (D - D_1)\cdot v_{csac} + (d_{ac} - d_{1ac})\cdot V_{cs} - \frac{1}{n}\cdot(D_1 + D)\cdot v_{oac} - \frac{1}{n}\cdot(d_{1ac} + d_{ac})\cdot V_o$$

$$i_{Lac} \equiv \frac{I_L}{D}\cdot d_{ac} + \frac{I_L}{V_g}\cdot v_{gac}$$

$$i_{Lpac} \equiv \frac{\left(v_{csac} - \frac{v_{oac}}{n}\right)}{\left(V_{cs} - \frac{V_o}{n}\right)}\cdot I_{Lp} + \frac{I_{Lp}}{D}\cdot d_{ac} \tag{1.14}$$

Taking the Laplace transform of the AC equations and making variable assignments to simplify we arrive at Equation sets (1.15) through (1.54) with the transfer function shown as Equation (1.55).

$$0 = A \cdot v_g(s) + B \cdot d_1(s) + C \cdot d_2(s) + E \cdot v_o(s) + F \cdot d(s) \tag{1.15}$$

$$G \cdot s \cdot v_o(s) = H \cdot d_1(s) + I \cdot v_o(s) + J \cdot d(s) \tag{1.16}$$

$$\left(K \cdot d_1(s) - L \cdot v_o(s) - M \cdot d(s)\right) \cdot s = N \cdot d_2(s) + O \cdot v_g(s) + P \cdot d_1(s) + Q \cdot v_o(s) + R \cdot d(s) \tag{1.17}$$

$$A = \left(D + D_1 + D_2\right) \tag{1.18}$$

$$B = \frac{\left(2 \cdot D_1 \cdot V_o + 2 \cdot n \cdot V_{cs} \cdot D - V_g \cdot n \cdot D + 2 \cdot D_2 \cdot V_{cs} \cdot n + 2 \cdot D_2 \cdot V_o + V_g \cdot n \cdot D_1\right)}{\left[n \cdot \left(D_1 - D\right)\right]} \tag{1.19}$$

$$C = \left(-2 \cdot V_{cs} + V_g\right) \tag{1.20}$$

$$E = 2 \cdot \frac{\left(D_1^{\,2} + D_1 \cdot D + D_2 \cdot D_1 + D_2 \cdot D\right)}{\left[n \cdot \left(D_1 - D\right)\right]} \tag{1.21}$$

$$F = \frac{\left(-2 \cdot D_1 \cdot V_{cs} \cdot n + 2 \cdot D_2 \cdot V_o - V_g \cdot n \cdot D - 2 \cdot D_2 \cdot V_{cs} \cdot n + V_g \cdot n \cdot D_1 + 2 \cdot D_1 \cdot V_o\right)}{\left[n \cdot \left(D_1 - D\right)\right]} \tag{1.22}$$

$$G = C_o \tag{1.23}$$

$$H = 4 \cdot I_{Lp} \cdot \frac{\left(D_1 \cdot V_o + D \cdot V_{cs} \cdot n\right)}{\left[\left(-n \cdot V_{cs} + V_o\right) \cdot \left[n \cdot \left(D_1 - D\right)\right]\right]} \tag{1.24}$$

$$I = \frac{-\left(n \cdot V_o \cdot D_1 - 4 \cdot I_{Lp} \cdot R \cdot D_1^{\,2} - n^2 \cdot V_{cs} \cdot D_1 - 4 \cdot I_{Lp} \cdot R \cdot D \cdot D_1 - D \cdot n \cdot V_o + D \cdot n^2 \cdot V_{cs}\right)}{\left[\left(-n \cdot V_{cs} + V_o\right) \cdot \left[n \cdot \left[\left(D_1 - D\right) \cdot R\right]\right]\right]} \tag{1.25}$$

$$J = 2 \cdot \left(D_1^{\,2} + 2 \cdot D \cdot D_1 - D^2\right) \cdot \frac{I_{Lp}}{\left[n \cdot \left[\left(D_1 - D\right) \cdot D\right]\right]} \tag{1.26}$$

$$K \equiv -C_s \cdot \frac{(n \cdot V_{cs} + V_o)}{[n \cdot (D_1 - D)]} \tag{1.27}$$

$$L \equiv C_s \cdot \frac{(D + D_1)}{[n \cdot (D_1 - D)]} \tag{1.28}$$

$$M \equiv C_s \cdot \frac{(-n \cdot V_{cs} + V_o)}{[n \cdot (D_1 - D)]} \tag{1.29}$$

$$N \equiv I_L \tag{1.30}$$

$$O \equiv (D_1 + D_2) \cdot \frac{I_L}{V_g} \tag{1.31}$$

$$P \equiv \frac{(2 \cdot I_{Lp} \cdot V_o + I_L \cdot V_o - I_L \cdot n \cdot V_{cs})}{(-n \cdot V_{cs} + V_o)} \tag{1.32}$$

$$Q \equiv 2 \cdot I_{Lp} \cdot \frac{D_1}{(-n \cdot V_{cs} + V_o)} \qquad R \equiv \left[\frac{(D_1 + D_2)}{D} \cdot I_L + \frac{(D_1 - D)}{D} \cdot I_{Lp} \right] \tag{1.33}$$

These equations can be solved to plot the small-signal characteristics for a given DC operating point. For the given DC operating point, the steady state parameters are solved from Equations (1.34) through (1.54), where voltage is in the unit volts, resistance is in ohms.

$$V_o := 50 \tag{1.34}$$

$$V_g := 120 \tag{1.35}$$

$$M := \frac{V_o}{V_g} \tag{1.36}$$

$$T_s := \frac{1}{50000} \tag{1.37}$$

$$n := .27 \tag{1.38}$$

$$R := 50 \tag{1.39}$$

$$C_o := 900 \cdot 10^{-6} \tag{1.40}$$

$$L := 482.3 \cdot 10^{-6} \tag{1.41}$$

$$L_p := 80.9 \cdot 10^{-6} \tag{1.42}$$

$$k := \frac{L_p}{L} \tag{1.43}$$

$$k_{Lp} := \frac{2 \cdot L_p}{R \cdot T_s} \tag{1.44}$$

$$k_L := \frac{2 \cdot L}{R \cdot T_s} \tag{1.45}$$

$$\tau_n := \frac{\frac{L}{R}}{T_s} \tag{1.46}$$

$$C_s := 820 \cdot 10^{-6} \tag{1.47}$$

$$m := \frac{1}{\left\lceil 8\cdot\left(M^2\cdot n\right)\right\rceil}\cdot\left(n^2\cdot k + 2\cdot M\cdot n + 4\cdot M^2 + \sqrt{n^4\cdot k^2 + 4\cdot n^3\cdot k\cdot M + 24\cdot n^2\cdot k\cdot M^2 + 4\cdot M^2\cdot n^2 - 16\cdot M^3\cdot n + 16\cdot M^4}\right) \tag{1.48}$$

$$V_{cs} := m\cdot V_o \tag{1.49}$$

$$I_{Lp} := \frac{(m\cdot n - 1)\cdot D\cdot V_o}{n\cdot k_{Lp}\cdot R} \tag{1.50}$$

$$D_2 := \frac{D}{2\cdot m\cdot M - 1} - D_1 \tag{1.51}$$

$$I_L := \frac{V_o\cdot D}{M\cdot k_L\cdot R} \tag{1.52}$$

$$D_1 := D\cdot\frac{(m\cdot n - 1)}{m\cdot n + 1} \tag{1.53}$$

$$D := \frac{1}{\left[2\cdot\left[\sqrt{m}\cdot(m\cdot n - 1)\right]\right]}\cdot\sqrt{2}\cdot\sqrt{k}\cdot\sqrt{\tau_n}\cdot\sqrt{n}\cdot\sqrt{m^2\cdot n^2 - 1} \tag{1.54}$$

Equation (1.55) shows the control to output transfer function with variable assignments. Equation (1.55) is solved for the control to output transfer function at the given operation point and shown in Equation (1.56).

$$\frac{v_o(s)}{d(s)} = -1\cdot\frac{\left(C\cdot s\cdot M_{new}\cdot H + C\cdot s\cdot K\cdot J - C\cdot P\cdot J + C\cdot R\cdot H + B\cdot N\cdot J - F\cdot N\cdot H\right)}{\left(C\cdot s\cdot K\cdot I + B\cdot N\cdot I + C\cdot Q\cdot H + C\cdot P\cdot G\cdot s - C\cdot P\cdot I + C\cdot s\cdot L\cdot H - C\cdot K\cdot G\cdot s^2 - E\cdot N\cdot H - B\cdot N\cdot G\cdot s\right)} \tag{1.55}$$

Substituting the previous equations into Equation (1.55), we arrive at the numerical control to output transfer function in Equation (1.56).

$$H_d(s) := \frac{653.1(s + 17.78)}{s^2 + 497.7s + 947.3} \tag{1.56}$$

A plot of magnitude and phase of Equation (1.56) is shown in Figure 1.8 and Figure 1.9.

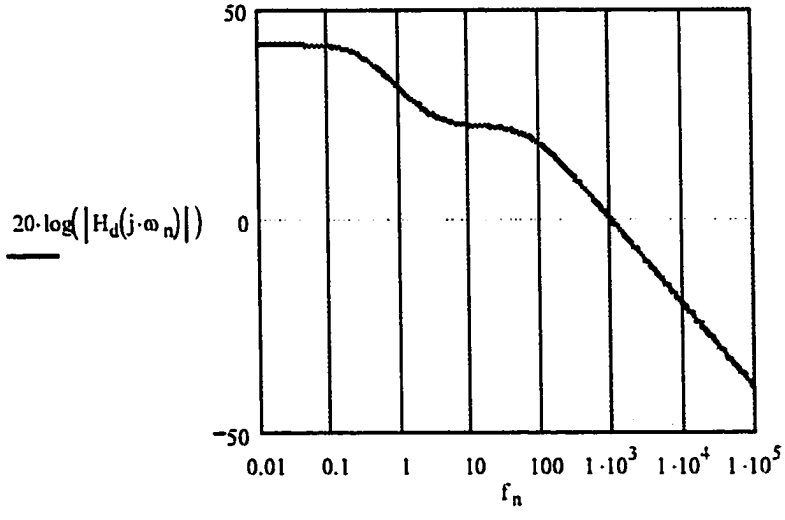


Figure 1.8: Magnitude for single stage PFC converter (control-output)

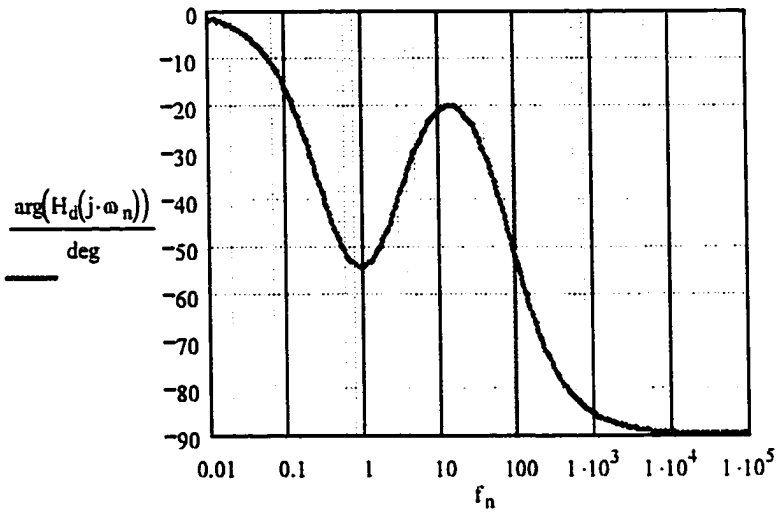


Figure 1.9: Phase for single stage PFC converter (control-output)

While tedious and strongly mathematical in nature, the method of state-space averaging introduced the notion of time-based averaging of circuit modes and the concept of system linearization to facilitate the use of classic design techniques. Its impact on the devlopment of power converter analsys and design are significant.

More recently, equivalent circuit models have been used in place of state-space averaging. One of the earliest and most prominent is the PWM Switch model [2]. The following section will provide an overview of this method.

1.3 Vorperian's Method of PWM Switch Modeling

By the early 1990s, members of the technical community recognized the need for a more unified approach for modeling PWM converters. One of the most notable methods, called PWM Switch modeling by Vorperian, makes an analogy to BJT amplifier analysis and suggests that equivalent circuits be developed for the nonlinear elements in the circuit [2]. In this method, the nonlinear elements in the circuit are replaced by controlled sources representing the time averaged electrical quantities.

In many ways the method of PWM Switch modeling is similar to state-space averaging. Both methods use time averaging to develop a unified converter representation from its distinct and separate modes. However, unlike state-space averaging, a representation that is purely mathematical in nature (a set of state equations), PWM switch modeling produces an equivalent, averaged circuit model by a very methodical and standardized approach. This model is suitable for direct time domain simulation. Further, since this equivalent circuit is generated by time averaging the modes of the discontinuous, actual circuit, the abrupt jumps seen in the actual circuit are not present in the averaged model resulting in less convergence problems and faster simulation [2].

While PWM Switch modeling easily formulates the time domain circuit model, the linear or small-signal representation of the power stage is not. In general, the averaged equivalent circuit models are also nonlinear and must be linearized to do control loop design. Linearizing the converter's averaged equivalent circuit involves significant mathematical

manipulation and might be more easily accomplished using state-space averaging. Fortunately, the advances in simulator software make this unnecessary. The averaged equivalent circuit model can be linearized directly in circuit simulators such as PSPICE. The linearization process traditionally carried by hand via equation manipulation is directly performed on circuit models in PSPICE via the AC Sweep analysis [3].

The preceding development gave a general overview of the modeling issue and described the method of PWM Switch Modeling. This modeling approach will be discussed in more detail and a DCM model for the circuit in Figure. 1.1 will be derived. It should be noted that although the boost converter will be used for the derivation, the model developed will be applicable to any converter in which the PWM Switch (3 terminal structure boxed in Figure 1.2 can be identified.

The first step is to draw the instantaneous waveforms of the actual circuit crossing the dashed boundary in Figure 1.1 for all modes of converter operation.

By inspection of Figures 1.2a-1.2c, we arrive at the instantaneous currents at nodes "a" and "p" as shown in Figure 1.10. We note the abrupt discontinuities as the circuit moves from one mode to another. The next step is to formulate modeling equations representing the average values of these current waveforms over the switching period, T_s.

Directly from the instantaneous terminal current waveforms of Figure 1.10, we can write the expressions for the average quantities as Equation (1.57)-(1.60).

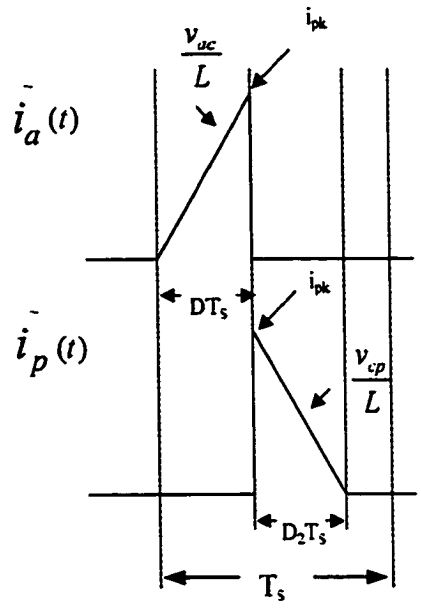


Figure 1.10: Instantaneous waveforms for boost (DCM)

$$v_{cp} = L \cdot \frac{i_{pk}}{d_2 \cdot T_s} \tag{1.57}$$

$$v_{ac} = L \cdot \frac{i_{pk}}{d \cdot T_s} \tag{1.58}$$

$$i_p = \frac{i_{pk}}{2} \cdot d_2 \tag{1.59}$$

$$i_a = \frac{i_{pk}}{2} \cdot d \tag{1.60}$$

Where $\tilde{i}_a$ and $\tilde{i}_p$ are instantaneous values and i_a and i_p are the average values.

Rearranging the expressions, we relate these averaged quantities to one another to arrive at Equation (1.61)-(1.63).

$$v_{ac} = \frac{d_2}{d} \cdot v_{cp} \tag{1.61}$$

$$i_a = \frac{d}{d_2} \cdot i_p \tag{1.62}$$

$$d_2 = \frac{2 \cdot L \cdot F_s}{d} \cdot \frac{i_p}{v_{ac}} \tag{1.63}$$

The averaged model follows directly as Equation (1.64)-(1.66).

$$i_a = \mu \cdot i_p \tag{1.64}$$

$$v_{cp} = \mu \cdot v_a \tag{1.65}$$

$$\mu = \frac{d^2}{2 \cdot L \cdot F_s} \frac{v_{ac}}{i_p} \tag{1.66}$$

From the development above, we see that simple relationships exist between the input and output port of the PWM Switch. All that remains is to represent the modeling equations, Equation (1.64)-(1.66), in circuit form as shown in Figure 1.11. Figure 1.11 represents an averaged, equivalent circuit model for the dashed box in Figure 1.1.

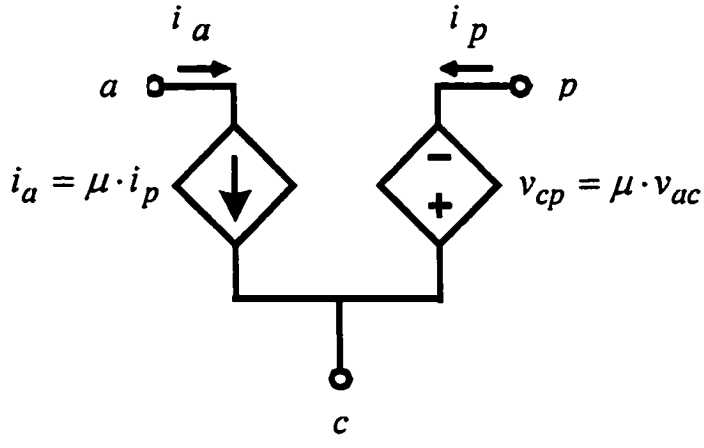


Figure 1.11: PWM Switch Model (DCM)

By replacing the transistor and diode with this model we eliminate the abrupt discontinuities in the terminal characteristics and represent the instantaneous waveforms by their averaged values. In so doing, we will see that the time domain simulation run will be much faster at the expense of resolution.

Having addressed the time domain aspects of the model, we now ready move to the small-signal or frequency domain characteristics. A close examination of the modeling equations reveals a nonlinear dependence on time varying circuit parameters, e.g. duty ratio. As a result of this nonlinearity, the averaged model must be linearized to produce the frequency response of the power stage. As pointed out in the previous section, armed with this information we will be able to design an effective controller tailored for this specific power stage. The linearization process is performed through the use of PSPICE's AC Sweep

Analysis [3] to produce Bode plots of the converter's control to output transfer function ($v_o(s)/d(s)$). By classic control design theory, these plots provide all the information necessary to design an effective controller for a given power stage via classic techniques. For the sake of brevity the design process is not shown here.

As mentioned above, the modeling technique presented by Vorperian [2] has several outstanding features including its simplicity and its direct application to the classic topologies. Unfortunately, his PWM Switch model is limited to applications involving converters that exhibit the PWM Switch cell. The reason for this can be understood by a more detailed evaluation of Vorperian's approach.

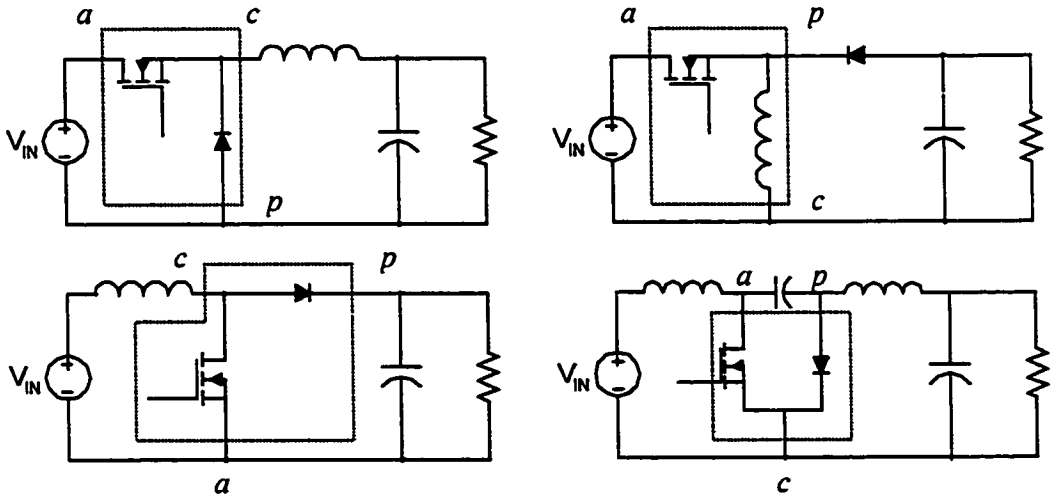


Figure 1.12: PWM Switching Cell in classic topologies

In the classic converter topologies (buck, boost, buck-boost, and Cuk) the PWM Switch Cell, as identified by Vorperian, consists of an active and passive switching device, which share a common node. Figure 1.12 boxes the PWM Switch Cell in each of the classic topologies.

Examining these diagrams reveals that the focus is on the portion of the circuit containing the switching elements while excluding the energy storage elements. By isolating this cell, it is possible to consider the entire nonlinear and discontinuous nature of the converter. After applying the averaging process to the current flowing into and out of the cell, Vorperian's model is able to replace the discontinuous switching elements with devices that represent the average electrical quantities at the ports of the cell. In so doing, the abrupt discontinuities of the actual circuit are substituted by smooth functions in the averaged equivalent model.

A second key issue is that the entire derivation of the Vorperian's model is based on the waveforms of the instantaneous currents through branches "a" and "p" as well as their dependence on cell port voltages v_{ap} and v_{ac}. Examining Figure 1.10, we see that the waveforms used in the derivation of Vorperian's model are not specific to any one of the classic converter topologies, but are in fact generic. Vorperian terms this "invariant" in that the terminal voltage and current characteristics of the PWM switch cell are the same regardless of the particular converter topology it is identified in. A comparison of Figures 1.10 and 1.12 reveals that Figure 1.10 could be the waveforms of any of the presented classic topologies when the generic labels i_a, i_p, i_c, v_{ac}, v_{cp} etc. are replaced by the topology

specific quantities seen in the actual circuit. For example, in the boost converter, the parameters v_{ap}, i_c, and i_p are v_o, i_L, and i_{out}, respectively It is for this reason that the Vorperian model can be directly applied to any of the classic topologies.

Clearly, Vorperian's choice of the PWM Switch Cell is deliberate. Choosing this cell establishes a common construct in the classic topologies that embodies the entire discontinuous nature of the circuit and presents a standard set of waveforms with regard to terminal currents and voltages in the derived model. However, when the switching elements cannot be localized to a particular region of the circuit, the waveforms at the nonlinear elements are not bound to behave as they do in Figure 1.10. The resulting conclusion is that Vorperian's model cannot be applied in converter topologies where the PWM Switch cell configuration and its associated terminal waveforms are not present.

Unfortunately, in many converter topologies, the inherent nonlinear and discontinuous nature is not localized to a particular area of the circuit as the switch-diode position in the conventional converters. In fact, many popular converters have switching elements spread throughout the topology with waveforms at these points not exactly matching those required by Vorperian's model. As a specific example, at UCF's Florida Power Electronics Research Center (FloridaPEC), work is being performed on a family of converter topologies that cannot be directly modeled by Vorperian's approach as they do not exhibit the PWM Switch Cell required. For topologies of this type, where switching elements are not localized to a particular region of the circuit, a new modeling approach is required.

Having reviewed the small-signal averaging and PWM switch modeling techniques, in the next section we will present a more unified modeling technique that uses concepts in the above methods.

1.4 Theory of Unified Approach

The method of PWM Switch modeling mentioned above provides a simple method for the formulation of averaged, equivalent circuit models. Clearly, the averaging of the instantaneous current waveforms and subsequent manipulations are the basis of this approach. Unfortunately, current waveform averaging is limited in its applications, particularly when energy storage elements are a part of the averaging cell. In that instance, inductor current is represented by a controlled current source whose magnitude is calculated by algebraic expression. By using an expression in place of the inductor, the natural time delays that would be created by the inductor are neglected in favor of a dependent current source which is effectively instantaneous. The net effect is a system order reduction which can lead to model inaccuracies at high frequency as shown later.

A more prudent approach is to maintain the integrity of the energy storage elements within the system by not averaging them out. This is a difficult task when a cellular modeling approach is used since the cell must necessarily contain all the nonlinear switching elements but should not contain energy storage components that effect the system's dynamic response.

Many converter topologies exhibit a structure that cannot be adapted to this requirement easily. This results in a need for a more widely applicable methodology. The approach presented here discards the notion of inductor current waveform averaging exploiting the property that the average of a variable's derivative is equal to the derivative of the variable's average when the averaging process is defined as a time varying average over a sliding window. By using this property the method presented will ensure average differential voltage appears across each inductor and average current flows through each system capacitor making sure to keep all the energy storage elements which contribute to dynamic response.

As will be shown in subsequent chapters, this approach leads to a simple methodology which can be applied to virtually any converter topology. Application of the approach will be performed on several examples including: the conventional boost, a new PFC single-switch converter, and a representative soft-switching. The models derived will then be compared with simulations of the actual circuit as well as other models.

1.5 Dissertation Outline

This dissertation began in Chapter 1 with a review the method of state-space averaging, then discussed the creation of the averaged, equivalent circuit models for the nonlinear power switch/diode combination in modern power converters via the Vorperian method and via a more unified modeling approach. Detailed examples of these conventional

modeling techniques are presented and limitations to these approaches are discussed. An introduction to the unified theory of average modeling is also given in Chapter 1.

In Chapter 2, we will apply this unified approach to several examples and validate these models by simulation comparisons with the actual circuit and other models. Also we will show how the implementation of these modeling equations in PSPICE can be streamlined using its Analog Behavioral Modeling capability. The validation of the models produced will be presented in this chapter by making a comparison between simulation results obtained from the actual, switched circuit and those obtained from the averaged equivalent circuit models. Models will be further validated by comparison to experimental data.

Chapter 3 will investigate current techniques and concepts involved with loss modeling in modern power converters. It will then explore the validity of these concepts by performing a series of simulations to determine validity. Once the most appropriate modeling theory is determined, the work will strive to apply these theoretical concepts to the unified modeling approach presented in this dissertation. The intent is to produce loss models for conduction losses that can be easily implemented during the model design phase, account for both CCM and DCM operation, be as simple as possible, and yield relatively good predictions of component conduction loss.

In Chapters 4 and 5, the unified technique will be applied to a soft-switching topology. This will present new challenges as the instantaneous waveforms vary widely over the operating range. In addition, Chapter 5 will address a different type of control scheme, thus

establishing that the unified approach here is applicable to non-duty ratio controlled converters.

The conclusion and future work will be presented in Chapter 6.

CHAPTER 2: THEORY AND METHODOLOGY OF UNIFIED APPROACH

This chapter introduces the objectives of the unified modeling approach, investigates other techniques for average modeling, and presents the fundamental theory of the approach presented here. The basis for this approach is the mathematical property that the average of a variable's derivative is equal to the derivative of the variable's average when the averaging process is defined as a time varying average over a sliding window. Utilizing this equality, another approach at circuit averaging can be implemented which is more easily applied and more widely applicable.

2.1 Introduction and Objectives

Having established the need for a different modeling approach, it is appropriate to consider the desirable characteristics of the newly generated models. One may summarize the objective of the dissertation:

To produce a unified, methodical approach to modeling virtually any type of power converter circuits while achieving the following goals:

1. A high level of accuracy over a wide frequency range

2. Fast simulation time

3. Simple modeling methodology

4. Account for both CCM and DCM operation in a single model

5. Remain as close to the actual circuit as possible and total visibility of all circuit parameters (D_1, D_2, I_L, etc.)

6. Allow for easy implementation in PSPICE

7. Serve as the precursor to conventional design techniques such as actual circuit simulation and experimental prototyping.

Certainly, objectives (1) and (2) are self-evident and require no further explanation. However, the remaining items will be discussed briefly.

Regarding item (3), there is a wide variety of modeling approaches published in the technical journals, [1], [2], [6], [7], [8]. Most of these modeling approaches trade the simplicity of Vorperian's approach for added functionality. In particular, the requirement of a more widely applicable modeling approach often results in significantly more complex modeling schemes. Further, the added complexity of these schemes often results in models that are more like mathematical abstractions than the circuit being modeled (item (5)). The modeling approach presented here will, whenever possible, avoid strict mathematical representations and attempt to capture the essence of the circuit's natural operation.

On item (4), the derivation of Vorperian's model is predicated on a particular set of waveforms. The waveforms shown in Figure 1.10 are drawn for the DCM case and result

in a model that is valid only for converter's operating in this mode. The result is that for any given Vorperian model, simulations are constrained to either DCM or CCM operation. This presents a problem during converter time domain startup modeling or transient modeling when the converter's operating point would transition from CCM to DCM operation or vice versa. When using a model that is CCM or DCM specific, the transition to the other operating mode cannot be simulated seamlessly. The designer is left with the task of piecing together results from two different simulation runs, one using the CCM model and the other using the DCM version. Certainly if the model can make this transition seamlessly while producing accurate results it would provide a significant functional improvement. Several of the recent modeling schemes in the published technical literature account for this need and present single models that accurately represent both CCM and DCM operation. The modeling approach presented here will also include this functionality.

Regarding item (6), another consideration is the method by which the derived models are input into the software packages for simulation. Since it is a common trait of these models to involve lengthy algebraic expressions, it is often easier for developers to "code" their models using the script format supported by their simulator packages. In the case of PSPICE, the graphical interface does not come with device blocks that will support the necessary controlled sources. However, the scripting language used by PSPICE does support the required functionality. As a part of the unified approach generated here,

custom devices will be created within the PSPICE package to facilitate direct input of model in schematic form rather than in script code.

On objective (5), when models are implemented using the scripting mechanism, the code or sub-circuit definition representing the model is usually represented as a rectangular block in the simulator schematic package. Various quantities, which are contained within the model's script, are inaccessible when running simulations. Clearly, there is often some interest in the activity or movement of these quantities as the simulation progresses, particularly during model debug. By employing, the graphical approach mentioned in the previous section, all the quantities of interest are visible to the modeler during simulation. As an example, during model debug, if the model has a problem the user might wish to ensure all the circuit parameters are converging to the proper values. In most cases the design engineer will have solved for the nominal operating point of the converter and need only place trace markers at the nodes of interest. The modeler can then compare the parameter's activity with its expected value. This is a significant improvement as the complex nature of the algebraic expressions employed often breeds model bugs. To correct these issues, good visibility into the activity of all model parameters is a must. If the user were working with the scripted form of the model, debug would be, at the very least, tedious if not impossible.

And finally, objective (7) establishes the notion of design order. While classic design techniques such as actual circuit simulation and experimental prototyping are effective and necessary, they are often not the logical first step in the design process. Initial efforts in

most designs include macroscopic evaluations of converter performance, component and operating point selection, and control loop design. Complications involving the simulation and construction of the actual topology often make this high-level evaluation difficult. The beauty of the unified model presented is that it allows the designer to gain significant insight into the design process providing an overview of every aspect of performance. Once these top-level issues are tackled, the detailed design process becomes fine tuning an already functional design.

2.2 Variant Technique Evaluation

Having covered the objectives of the new modeling approach, we are now prepared to discuss potential techniques. As the first candidate, the possibility of modifying Vorperian's approach will be discussed. The idea would be to expand Vorperian's approach to cases not exhibiting the PWM Switch cell and to incorporate the added functionality listed in the above objectives. Several papers were reviewed that make variations on Vorperian's approach and attempt to apply their new modeling schemes to converters where the PWM Switch cell is not present.

Certainly, this is an attractive methodology owing to the powerful and simplistic nature of the Vorperian scheme. Further, intuitively, we might expect that this approach could be extend to the more general circuit topologies with little effort while maintaining an accurate equivalent circuit model. In fact, a large portion of the research done for this dissertation

was dedicated to doing just that. Unfortunately, as will be seen in the next section, the extension of Vorperian's approach is not so easily done. The intuitive way to apply Vorperian's modeling theory to the more general class of converters often yields inaccurate results. It was shown that at the core of Vorperian's methodology is the requirement that all the switching elements are contained within the block to be modeled and that this block does not contain any of the energy storage elements within the system.

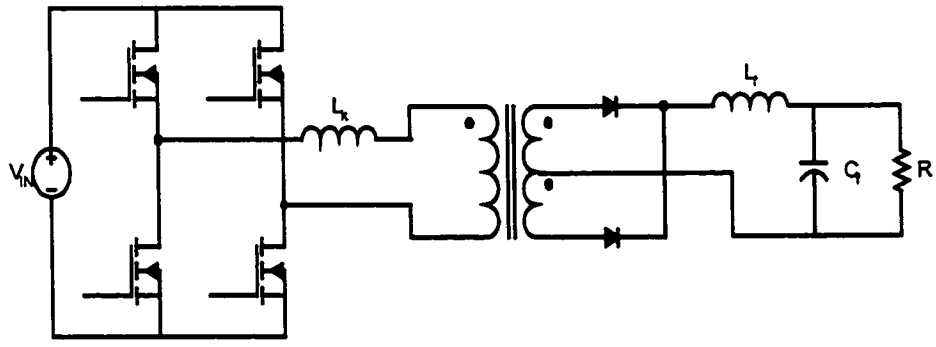


Figure 2.1: Separated PWM switch topology in [6]

Consider the circuit topology modeled in [6] and shown in Figure 2.1. It should be noted that the Vorperian PWM Switch cell configuration is not present in this circuit as the active and passive elements are not localized to a particular region. However, using the same notation developed in Vorperian's work (node labeling a, p, and c), the author attempts to follow Vorperian's methodology to produce an averaged model. As in the Vorperian

approach, the cell to be modeled is chosen to include all the switching elements in the topology. In the development of [6], the author averages the instantaneous waveforms at the ports of the cell just as Vorperian did in his work. Manipulating the averaged expressions and comparing the expressions from the CCM and DCM cases, it is possible to identify the CCM equations as a special case of DCM equations. Using this fact in conjunction with the scripting code available within the simulator package employed, the model is able to account for seamless transitions between CCM and DCM during time domain simulations of his model.

Evaluation of the small-signal curves presented in the paper represent a system order reduction by the derived model. While in this case this reduction results in no loss of accuracy, it represents an inaccurate approximation in the more general case. To investigate the cause of the apparent system order reduction, it is appropriate to consider a simpler circuit while applying the same methodology.

Consider the classic buck-boost topology with its instantaneous current waveforms shown in Figure 2.2.

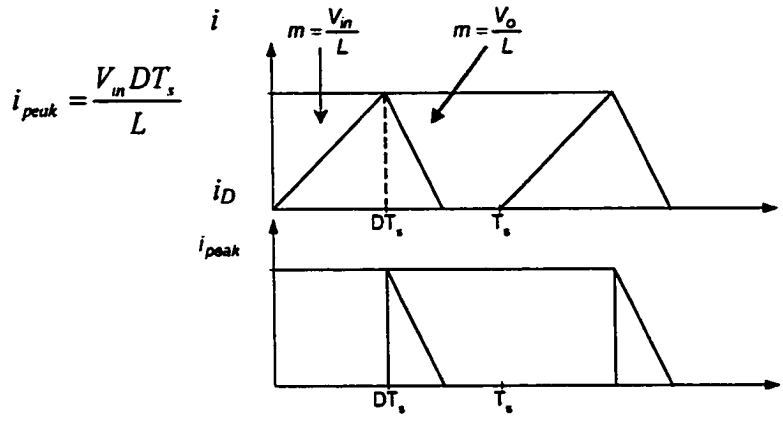


Figure 2.2: Buck-boost waveforms in DCM

In Vorperian's approach, the PWM Switch cell is blocked off and the instantaneous waveforms at the cell ports are averaged. However, applying the Vorperian modeling approach on Figure 2.1, the PWM Switch cell is not present as the passive switches are separated from the active switches by other elements, specifically a transformer and an inductor. In order to average all the switching elements within the topology, the author is forced to block a large area of the schematic as shown in [6]. This area, while it does include all switching elements, also includes the leakage inductance and the ideal transformer. The effect of averaging a cell block that includes an inductor can be investigated by applying such a block to the classic buck-boost topology shown in Figure 2.3.

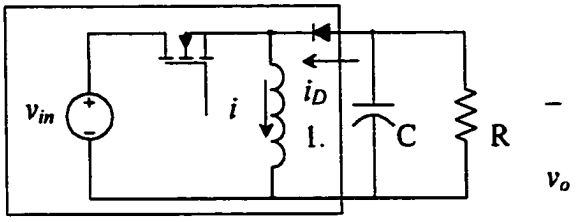


Figure 2.3: Modeling cell in Buck-Boost

In Figure 2.3, rather using the PWM Switch cell defined by Vorperian, consider the use of a block which contains the entire input portion of the circuit including the inductor as shown below.

This cell is analogous to the one used in [6] in that it includes the inductor within the cell to be averaged. In keeping with the methodology, the next step is to average the instantaneous waveforms at the cell boundaries. Referring to Figure 2.14 we can write the expression for the average diode current as shown in Equation (2.1).

$$i_{D_{AVG}} = \frac{V_{in}^2 \cdot T_s \cdot D^2}{2 \cdot L \cdot V_o} \tag{2.1}$$

The resulting averaged circuit can be drawn by substituting the blocked portion of the circuit with its averaged equivalent, Equation (2.1). That circuit is shown as Figure 2.4.

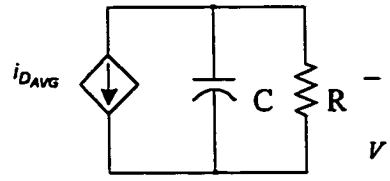


Figure 2.4: Averaged equivalent circuit

In the equivalent circuit of Figure 2.4, the controlled current source represents the average value of the diode current, which is the output current. The expression for i_{DAVG} is a function of multiple time varying quantities, such as V_o and D, and is therefore a nonlinear expression. In order to plot the small-signal characteristics of the circuit of Figure 2.4, the nonlinear elements must be linearized. As presented in the introductory material, we linearize using a first order Taylor series expansion up to and including the first order terms. This process results in the linearization of the nonlinear controlled current source shown in Equation (2.2).

$$\tilde{i}_d \approx \frac{\partial f}{\partial \bar{v}_o}\cdot\tilde{v}_o + \frac{\partial f}{\partial \bar{d}}\cdot\tilde{d} = \frac{V_{in}^2\cdot T}{L}\cdot\left(\frac{D^2}{2\cdot V_o^{\,2}}\cdot\tilde{v}_o - \frac{\tilde{d}\cdot D}{V_o}\right) \tag{2.2}$$

where

$$f = \bar{i}_D(t) = \frac{V_{in}^2\cdot T\cdot D^2}{2\cdot L\cdot \bar{v}_o(t)} \tag{2.3}$$

From the DC solutions, we can obtain the the operating point of the linearization as Equation (2.4).

$$V_o = -R \cdot I_{D_{ave}} = R \cdot \frac{V_{in}^2 \cdot T \cdot D^2}{2 \cdot L \cdot V_o} \tag{2.4}$$

Solving for V_o we obtain Equation (2.5).

$$V_o = -V_{in} \cdot D \cdot \sqrt{\frac{R \cdot T}{2 \cdot L}} \tag{2.5}$$

Substituting the operating point into the small-signal or linearized equation for i we obtain Equation (2.6).

$$\tilde{i}_d = \frac{1}{R} \cdot \tilde{v}_o + V_{in} \cdot D \cdot \sqrt{\frac{2 \cdot T}{R \cdot L}} \cdot \tilde{d} \tag{2.6}$$

From Equation (2.6), we can, by inspection, write the small-signal equivalent model as shown below in Figure 2.5.

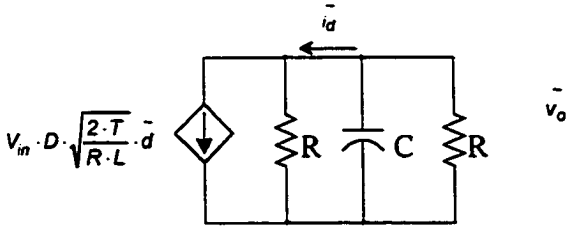


Figure 2.5: Linearized, averaged Circuit

Examining the small-signal equivalent circuit of Figure 2.5, it is apparent that the system will produce a first order response for the control-to-output transfer function. However, in the Vorperian paper [2], Vorperian makes a clear assertion that this response should be second order, owing to the presence of an inductor and a capacitor in the buck-boost topology. While this determination could have been made by a simple inspection of the circuit, the preceding linearization was done to emphasize that including the inductor in the cell block effectively "averages out" one element of the state vector. This element corresponds to the time derivative contributed by the inductor within the block. This development tends to refute the notion that it is acceptable to choose a cell block which includes components that would otherwise contribute an element to the state vector.

2.3 Fundamental Theory of Unified Modeling Approach

So, the development above shows that the intuitive way to extend Vorperian's approach can lead to inaccurate results. With this in mind, a different modeling approach must be considered as topologies often include instances were switching elements are separated by energy storage elements. To develop this concept, it is instructive to examine, once again, Vorperian's methodology at a fundamental level.

Recall, as a part of his averaging process, Vorperian presents the instantaneous current waveforms at nodes "a" and "p". After taking the average of these instantaneous current waveforms, Vorperian manipulates the expressions for these averaged currents and relates

them to one another in much the same way one would relate the terminal characteristics of any two-port model. Since the expressions for the terminal currents at nodes "a" and "p" are a function of the cell port voltages v and v , the expressions for the averaged currents at "a" and "p" are as well. As a result, the same averaged current equations can be manipulated in a different fashion to relate the average values of v and v , the port voltages of the PWM Switch cell. At this point, the port characteristics, both voltage and current, of the averaged PWM Switch model are well defined and take the form of algebraic expressions. As was seen previously, an equivalent circuit readily represents these expressions.

Clearly, the averaging of the instantaneous current waveforms and subsequent manipulations are at the very core of this approach. Unfortunately, based on the above development, one can infer that current waveform averaging is limited in its applications, particularly when energy storage elements are a part of the averaging cell.

A key point here is that although Vorperian does not include inductors in his averaging cell, the current waveforms crossing the PWM Switch cell boundaries exhibit waveshapes that are a direct consequence of the inductor(s) external to the cell. Considering Figure 1.10 it is evident that although these currents represent the instantaneous cell currents, their shape is a direct result of the i-v relationship of the inductor(s) in the circuit as shown Equation (2.7) below.

$$\frac{d}{dt} i_L = \frac{v_L}{L} \tag{2.7}$$

Further, by averaging these waveforms, Vorperian is, in some sense, averaging i since in each case the waveforms are actually inductor current as it is carried by either the active or the passive switch.

From [5], a mathematical property of key importance is that the average of a variable's derivative is equal to the derivative of the variable's average when the averaging process is defined as a time varying average over a sliding window as shown in Equation (2.8).

$$x_{avg}(t) = \frac{1}{T_s} \cdot \int_{t-T}^{t} x(\zeta)\, d\zeta \tag{2.8}$$

Therefore, if Vorperian's approach is to, in some sense, average i, an equally valid approach would be to work on the other side of Equation (2.7) and somehow take the average of the derivative. This mathematical equality will be exploited to produce a different modeling approach. Several models in the open literature [8] exploit a similar concept but the wider application of this property as a unified approach to averaged circuit modeling has, to the author's knowledge, not been explored.

To clarify how this task might be accomplished let us consider, again, that the instantaneous current waveforms of Figure 1.10 are being averaged in Vorperian's method. If one likens this to taking the derivative of the average of i, an equally valid approach would be to average the derivative of i. Since the right hand side of Equation (2.7) is v divided by a constant, L, averaging the differential voltage v is effectively averaging the derivative. In terms of the circuit, rather than average the instantaneous current waveforms

generated by the derivative function, another option should be to the average the instantaneous voltage waveforms at the nodes in the circuit on either side of the inductor. In this way, the differential voltage across the inductor becomes an average. Current through the inductor is then generated by allowing the inductor's derivative function, Equation (2.7), to operate on averaged values of differential inductor voltage.

It should be emphasized that using this approach keeps the resulting model close to the actual circuit's operation. In the actual circuit, during a transient, if the line or load characteristics change, the instantaneous differential voltage applied to the inductor is also affected. Given enough time, this change in differential voltage will effect inductor current, and thereby change the energy transfer characteristics of the converter. In the new averaged model, the integrity of this operation is left intact with the only difference being that the differential voltage across the inductor is no longer the discontinuous, instantaneous function of the actual circuit but rather a smooth, continuous averaged value.

A key point in the previous discussion is that in the actual circuit, the differential voltage applied across the inductor is the independent or controlled variable. The inductor current is then generated by natural circuit operation and is a consequence of the applied differential voltage, making the inductor current a dependent quantity. In the averaged circuit, this cause-effect relationship is maintained.

This is in sharp contrast to other modeling schemes where inductor current is created in an artificial manner [7]. In these schemes, a current is forced by a controlled current source

whose magnitude is calculated by algebraic expression. This approach moves away from the cause-effect relationship discussed above. Further, in the actual circuit, it should be noted that the converter's response to transient effects is somewhat delayed due to the presence of the inductor (inductor current cannot change instantaneously). By using an algebraic expression in its place, the architects of these other schemes seem to neglect these natural time delays substituting an algebraically controlled current source that is effectively instantaneous.

In Reference [7], Ben-Yaakov's modeling approach to the DCM operating mode includes a controlled source to force a calculated value of inductor current through the circuit. From the previous development, it was shown that replacing the inductor with an algebraic expression removes some measure of the dynamic nature of the converter. Specifically, it is this author's opinion that the use of a controlled source in place of the inductor reduces system order and introduces some inaccuracies in the model's dynamic characteristics when compared with the actual circuit.

In the defense of Ben-Yaakov's approach, it should be considered that the classic converter's operating in DCM exhibit a first order-like response at lower frequencies. However, as pointed out by Vorperian [2], the system is still second order due to the presence of a pole outside the frequencies of interest (greater than F_s/π). Therefore, the substitution of a controlled source for an inductor in DCM by can produce a model with reasonable accuracy at low frequencies. However, it should be emphasized that this is a

simplifying assumption that may not be valid for a wide range of frequencies. Further, the use of this controlled source moves away from the natural operation of the actual circuit adding unnecessary complexity and reducing model accuracy.

2.4 Application of Modeling Theory to Boost Converter

Having evaluated the shortcomings of other schemes, it is appropriate to continue on with the development of the approach to be used here. As mentioned previously, this approach will capitalize on the notion that averaging the differential inductor voltage is equivalent to averaging the inductor current. Further, it has been proven, exhaustively, that the inductor's presence often serves a necessary function to the dynamic operation of the converter and should often be retained. And finally, the functional capability of seamless transition from CCM to DCM converter operation will be incorporated by some method similar to that used in [6] assuming that the expressions for CCM can be manipulated into a special case of the DCM equations.

With these basic concepts in mind, we are prepared to apply this modeling approach to the classic boost topology as a test case. The operation of the boost topology in DCM operation was reviewed earlier and will not be repeated here. Consider the converter of Figure 2.6.

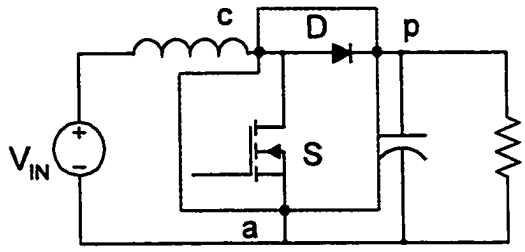


Figure 2.6: Boost converter.

From the modes of operation, Figure 1.2, we can draw the instantaneous voltage and current waveforms needed to produce the model. Plotting the instantaneous waveforms, we arrive at Figure 2.7.

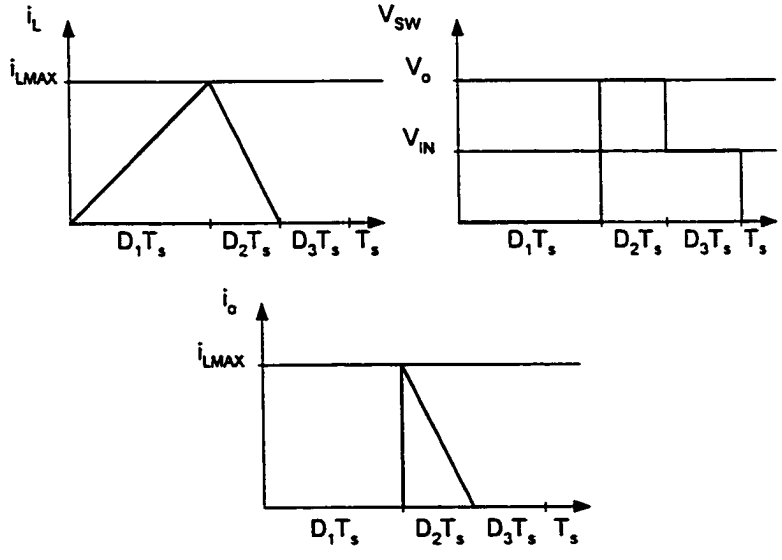


Figure 2.7: Instantaneous waveforms of boost (DCM)

Specifically, since the core of the approach is to apply the correct average, differential inductor voltage, we might plot the instantaneous value of v. However, since we anticipate connecting a source at one of the inductor's terminals, it is more convenient to average the voltage at the immediate right hand side node. This corresponds to v_w in this topology.

From Figure 2.7, the instantaneous waveforms can be averaged to produce the Equations (2.9) through (2.11):

$$I_{oavg} = I_{Lavg} \cdot \frac{D_2}{D_1 + D_2} \tag{2.9}$$

$$I_{Lavg} = \frac{1}{2} \cdot \frac{V_{in}}{L} \cdot D_1 \cdot T_s \cdot (D_1 + D_2) \tag{2.10}$$

$$V_{swavg} = V_o \cdot D_2 + V_{in} \cdot D_3 \tag{2.11}$$

These equations will form the basis of the new averaged model. Beginning with the inductor, the proposed approach would impress the correct averaged differential voltage. Having derived average voltage at the immediate right hand node of the indictor, a possible equivalent circuit is shown in Figure 2.8.

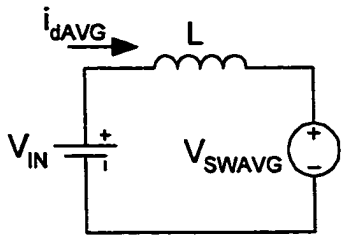


Figure 2.8: Partial averaged equivalent for inductor

The symbolism used for V_{in} represents an externally provided value. The symbol choice for V_{SWAVG} represents a controlled voltage source. With the average differential voltage across the choke inductor, the steady state value for this source will be equal to V_{IN} just as volt-second balance must be maintained in the actual circuit during steady state. Transient conditions in the line or load will impress a non-zero voltage across the inductor initiating a dynamic response of the converter. Further, since the average output current, i_o, is dependent on the inductor current, a controlled source relating these two currents is appropriate. This does not result in a loss of accuracy as the dynamic nature of the inductor current is already captured in the model. Including the controlled current source for the output stage we have the circuit shown in Figure 2.9.

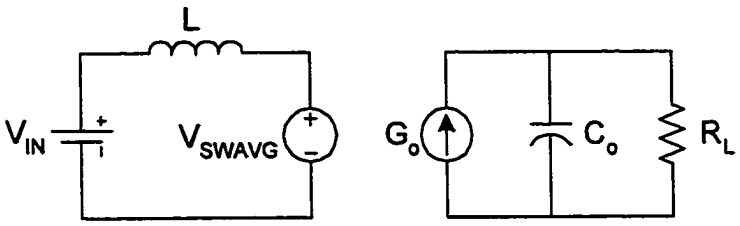


Figure 2.9: Partial averaged equivalent

Where, the expression controlling V_{SW} is given in Equation (2.11) and the expression controlling G_o is given in Equation (2.9). With the core of the model intact, it is appropriate to consider its implementation in the circuit simulator. Examining the equations for V_{SW} and G_o, we can see that the parameters L and T will have to be supplied to the model up front, as will the parameters not distinctly appearing in the equations, C_o and R. The parameters V_{IN}, V_o, and I_{vg} can be directly obtained from the model, real-time, during the simulation. In particular, when V_{IN} or V_o appears in the modeling equations, we simply input the node voltage corresponding to that value. This allows for the dynamic operation of the model. If the nominal values were used, say V_o equals 50V, transient changes at the output would not be represented accurately. Therefore, the conclusion is that it is crucial to represent these quantities as variables in the model, which are totally dependent on the instantaneous and time varying electrical quantities in the circuit.

Addressing the I_{vg} term, the entire basis for the approach presented here is to maintain the accurate generation of the inductor current by using the correct differential inductor voltage and allowing natural circuit operation to produce the inductor current. It was established that rather than averaging the inductor current waveforms, an equally valid approach is to average the differential inductor voltage. Since we have replaced the instantaneous differential inductor voltage with its average, it is reasonable that the current produced in the averaged equivalent model represents the average of the instantaneous current. With this in mind, when the I_{vg} term appears in the expression for G_o, we input a reference to the real time current flowing through the inductor. This approach captures the output current's dynamic dependence on the inductor current.

A final sweep of the model parameters reveals that all the parameters have been considered except the duty ratios D , D_2, and D_3., the switch duty ratio, D , is supplied as a defined parameter if the circuit is simulated in open loop or as a product of the control schematic if simulated in closed loop. However, from basic converter analysis, it is clear that D_2 and D_3 are dependent on converters operating conditions. Examining Equation (2.10), we can see that all the parameters are accounted for with the exception of D_2. As a result, this equation can be used to generate D_2. It should be emphasized here that Equation (2.10), the average inductor current, is not used to create or force an artificially generated inductor current. However, since the value of the time varying inductor current is an accessible parameter in the model, it can be used in conjunction with Equation (2.10) dynamically generate D_2.

Finally, D_3 is solved by noting that it is equal to one minus the summation of the other duty ratios.

Based on the above discussion, the completed model is present in Figure 2.10.

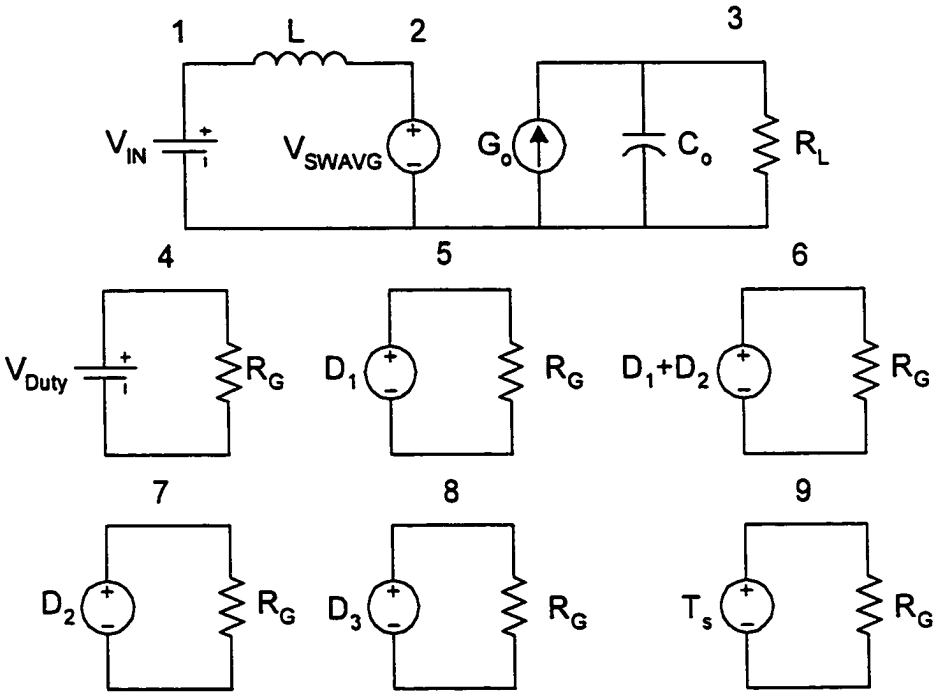


Figure 2.10: Complete averaged equivalent model

The additional loops formed at nodes 4 through 9 are used for duty ratio generation. The resistance R is used as a high resistance to the controlled source in the loop. As before, the

symbolism for $V_{\ y}$ and V_{IN} is used to represent externally supplied parameters, while the other source symbols represent controlled sources.

The controlled voltage source D will have a value equal to the node 4 voltage but will be limited to values between 0 and 1. If the node voltage at 4 is with in this range, the voltages at nodes 4 and 5 will be equal.

The controlled voltage source $D + D_2$ will be controlled by Equation (2.12) which is rearranged and shown below.

$$D_1 + D_2 = \frac{I_{Lavg}}{\left(\frac{1}{2}\cdot\frac{V_{in}}{L}\cdot D_1\cdot T_s\right)} \tag{2.12}$$

It is important to note that when $D + D_2$ equals one, the converter makes the transition from DCM to CCM operation. In fact, an examination of all the boost converter's equations reveals a similar relationship. Therefore, as in [6], the CCM equations are a special case of the DCM equations. Capitalizing on this fact, we limit the range of $D + D_2$ to 0 to 1 also. This is the key factor in allowing the model to transition from DCM to CCM seamlessly.

The controlled voltage source D_2 will be controlled by an equation that simply subtracts the node 5 voltage from the node 6 voltage. Although not strictly required, a 0 to 1 limit will also be employed here. The reason is that when the circuit simulator solves the model for its operating point, the limiters will force it to choose a valid solution to the system of

nonlinear equations. If a possible solution to the system involved a solution for D_2 that was outside the allowable range, we would expect the simulator to discard this solution. This will be investigated in more detail in the next section.

The controlled voltage source D_3 will be controlled by an equation that simply subtracts the sum of the voltages at nodes 5 and 7 from 1. This value is also limited to the range 0 to 1 for the same reasons mentioned above.

Before moving the model to the simulator, it is helpful to verify the model's equations and investigate all the possible solution sets to these equations for a given set of parameters. Using MathCAD's nonlinear equation solver, the model's equations can be directly input and solved for all possible solutions. Choosing a set of parameters, the information is input into MathCAD producing the results shown in Equation set (2.13).

$L := 1 \cdot 10^{-6}$ $R := 11$ $F_s := 100 \cdot 10^{3}$

$V_{in} := 20$ $D_1 := .261$ $T_s := \frac{1}{F_s}$

Given

$$V_{in} - (V_o \cdot D_2 + V_{in} \cdot D_3) \equiv 0$$

$$D_1 + D_2 \equiv \frac{2 \cdot I_{Lavg}}{V_{in} \cdot D_1 \cdot T_s \cdot \frac{1}{L}}$$

$$\frac{V_o}{R} \equiv I_{Lavg} \cdot \frac{D_2}{D_1 + D_2}$$

$$D_3 \equiv 1 - D_1 - D_2$$

$$\text{Find}(V_o, D_2, D_3, I_{Lavg}) \text{ float}, 3 \rightarrow \begin{pmatrix} -30.0 & 50.0 \\ -.104 & .174 \\ .843 & .565 \\ 4.09 & 11.4 \end{pmatrix} \tag{2.13}$$

While MathCAD returns two mathematically valid solutions, only solution vector 2 [V_o=50V, D_2=.174, D_3=.565, I_{Lavg}=11.36A] is physically realizable and should be taken as the solution.

Examining the possible steady state solutions to the given system from MathCAD, it should be noted that the simulator should arrive at the same possibilities. At the time of the transient simulation, the user has the opportunity to force the simulator to a particular solution by providing initial conditions. In the case of PSPICE, initial conditions can be given to the energy storage elements to control the "initial bias point solution" chosen by

PSPICE. However, it is conceivable that the model's user would not know appropriate initial conditions to provide. In this case, the user might submit an initial condition for one or more elements that solves to an inappropriate operating point.

Inspection of the two solution vectors reveals that only the second solution vector is physically realizable since D_2 in solution vector 1 is negative, and therefore, not possible. However, if an initial condition is presented that is closer to the erroneous solution, the simulation will produce inaccurate results. The limiter on the D_2 controlled source prevents this from occurring. With the final value for D_2 is limited to the range from 0 to 1, the model simulation will fail to converge before it will produce erroneous results. Therefore, the more powerful application of the model is, whenever possible, to not provide initial conditions. In the above method, when PSPICE calculates its initial bias point solution, it will arrive at the only physically valid solution.

The use of MathCAD in the above analysis is invaluable. The MathCAD solver allows the model designer the opportunity to verify his or her model's DC solution before going to the simulator, where debug will be more difficult. Further, the use of MathCAD allows the modeler some level of insight into possible erroneous solutions to the given set of nonlinear equations. Armed with this information, the modeler can place more appropriate limits on the controlled sources of the model.

2.5 Implementation of Averaged Models in PSPICE

Having verified solution vector 2 as the valid DC solution to the system, it is appropriate to move the model to the simulator package. For this development, Orcad PSPICE Version 9 will be used because of its widespread availability and functionality. A review of the technical literature concerning average model implementation in PSPICE suggests that most models are implemented via the PSPICE scripting method commonly referred to as "subcircuit definition".

In earlier versions of PSPICE, modeling equations could be implemented but the new equations would actually modify the program's source code. MicroSim admittedly called this "difficult to use and more prone to error" [3]. More recent versions of PSPICE have a new functionality termed Analog Behavioral Modeling (ABM). In a nutshell, this new functionality allows modeling equations to be implemented in closed form using existing PSPICE primitives (controlled sources) [3]. The development of the averaged model in PSPICE will rely on this new functionality to produce the circuit model.

PSPICE Professional includes a standard library with the all of the Vorperian PWM Switch models. These models are to serve as examples of how to implement averaged equivalent circuit models with in PSPICE. The library, called "swit_rav.lib", consists of all the models Vorperian derived in his various papers including CCM and DCM versions for both large signal and small-signal simulation with an additional designator for voltage mode or current mode control. The model type information is coded into the model name as

follows: the first two characters, VM or CM, represent control type, the second two characters, LS or SS, represent large or small-signal, and the final three characters are DCM or CCM denoting converter operational mode.

As an example consider the subcircuit definition for the voltage mode, large signal, DCM Vorperian model (VMLSDCM). This model is the PSPICE representation of the Vorperian DCM model derived earlier in this thesis. The PSPICE subcircuit definition is shown in Figure 2.11.

Step by step implementation of the modeling equations is relatively straightforward. Rather than go through the details of the development here, we will highlight some of the more notable characteristics of the PSPICE model. The modeling equations were derived earlier but are repeated here for convenience.

$$v_{cp} = \mu \cdot v_a \tag{2.14}$$

$$i_a = \mu \cdot i_p \tag{2.15}$$

$$\mu = \frac{d^2}{2 \cdot L \cdot F_s} \frac{v_{ac}}{i_p} \tag{2.16}$$

```
*$
**** VMLSDCM ****
.subckt VMLSDCM A P C Vc
Params: RMPHITE=2 VALLEYV=1 LFIL=500u FS=50k
 vconv conv 0 1
 emod d   0 table {v(conv)*(v(vc)-VALLEYV)/RMPHITE} = (.01,.01) (.99,.99)
 etbl anum 0 table {2*lfil*fs*i(vmp)} (1e-8,1e-8) (400,400)
 emew mew 0 value={v(conv)*v(d)*v(d)*v(a,c)/v(anum) }
 gac a   c value={v(conv)*v(mew)*i(vmp) }
 ecp c   x value={v(conv)*v(mew)*v(a,c)}
 vmp p   x 0
 rconv d   0 1g
 rc  conv 0 1g
 ranum anum 0 1g
 r5  mew 0 1g
.ends
```

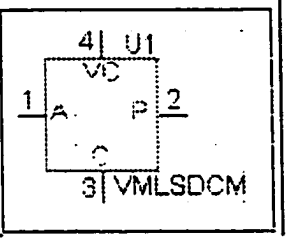


Figure 2.11: PSPICE Subcircuit and model symbol for Vorperian DCM

Figure 2.11 shows how the modeling equations are implemented in PSPICE using the ABM keywords. It should be noted this is a direct representation of the model equations developed earlier with additions to aid in numerical convergence. For example, from Figure 1.11, the controlled current source in the model is labeled *gac* in the sub-circuit listing and is equal to v(conv)*v(mew)*i(vmp), v(mew) is v(conv)*v(d)*v(d)*v(a,c)/v(anum), and i(vmp) is i . where v(anum) is the denominator of the μ expression, v(d) is the duty ratio, and v(conv) is to aid in convergence. A notable characteristic of the subcircuit listing is the table construct. PSPICE's ABM allows equation results to be constrained to a particular range [3]. As an example, examine the expression for *etbl* in the subcircuit list. It is easily verified that this expression represents

the denominator of equation for μ. In the expression, if *i* (or *i(vmp)* as its identified in the model) is initially zero, the simulation will fail instantly with a divide by zero overflow. To address this situation, the table construct limits the value of the expression to a near zero number on the low end. On the high end, the table construct limits the value to an arbitrarily high value. The purpose is to constrain μ to a reasonable value during startup. As the converter starts, *i(vmp)* rises quickly bringing μ to within the constrained range.

The above discussion highlights how the hand derived modeling equations are implemented in PSPICE. The advanced features of ABM allow the designer to directly implement the modeling equations and account for potential convergence pitfalls along the way.

However, although this PSPICE scripting method offers all the required functionality, it is a very tedious form of model input and development. Referring back to Figure 2.11, the subcircuit definition shown is stored in a *.lib library file. This is a text file that is used by the schematic package to netlist the model portion of the circuit. After the netlist is created, the information is passed to the PSPICE A\D Simulator engine for actual simulation. The subcircuit definition is necessary because the schematic package must be told how the model functions and how it is interconnected in the circuit. Common elements such as sources, resistors, capacitors etc. do not require a subcircuit definition, as they have symbols and definitions already.

The subcircuit definition or script file is represented graphically in schematics as the block in the lower right portion of Figure 2.11. This is the only graphical representation of the model. For subcircuit definitions, schematic diagrams found in the technical literature are generally representative in nature and do not come from the simulator package. Generally, these diagrams are generated externally via some drawing tool.

Having described how averaged models are commonly implemented in PSPICE, we've established the basis for a discussion of the limitations to this approach. First, since model parameters are completely internal to the rectangular block they are inaccessible from the schematics package. As mentioned previously, this makes it difficult to track the values of those parameters. Second, updates to the model require the modeler to modify it via a text editor rather than graphically as would be done with any other schematic. And finally, simulations involving the model require the specialized libraries for simulation. So a simple schematic diagram is not all that's required to make the simulation run.

Considering these limitations, it is clear that some graphical approach to model implementation would be preferred. Further, for the graphical method to be useful, it must incorporate the same ABM functions used in the text-based approach, TABLE and VALUE. An examination of the PSPICE ABM library reveals there are sources available with the necessary ABM functions. Consider the PSPICE source symbols shown in Figure 2.12 below.

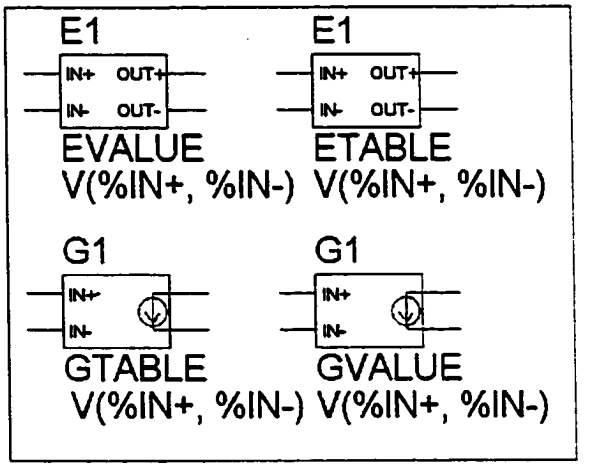


Figure 2.12: PSPICE ABM Symbols

These symbols are used in PSPICE to represent controlled sources implementing the ABM functions of interest. Note that each device has an input port and an output port. However, models created using the method here will often result in lengthy algebraic equations that are a function of multiple time varying parameters. The limitation comes in that these devices require a single input.

With that problem in mind, a custom solution is required. A review of the PSPICE User's Guide shows that custom devices can be created within PSPICE Schematics. These custom devices can then be "coded" with the appropriate ABM function.

Creation of the device is done partially with the PSPICE Schematics package and partially with a text editor. In the Schematics editor, a new file is generated with the *.slb file extension representing the symbol library. This is a binary file representing the graphic to

be used for the device, as well as the information the schematics package will use to successfully net list it. From a text editor, the *.lib file must be generated housing the subcircuit definition for the new source. The ABM keywords TABLE and VALUE are used here.

For the Schematics editor part, the first step is to draw the symbol for the device. The symbol can be drawn by the drawing tools in Schematics or copied from another part. The sources created here have symbols which are modified versions of those already existing in the symbol library. To begin, from the File menu, chose Edit Library. This takes you to the Symbol Editor. To use a symbol from an existing graphic, from the Parts menu, chose Get Symbol Graphics. From here, after choosing the correct library choose the part symbol you wish to copy. It will appear in the graphics editor allowing you to modify its appearance.

The next step is to set the appropriate symbol parameters. These parameters tell PSPICE how to net list the pins of the new source, where to look for the subcircuit definition, and the parameters to display when the source is double-clicked in Schematics. All of these parameters are configured from the Part menu.

From the Part menu, under the Attribute heading, the symbol's parameters are configured, a screen shot of this window is shown in Figure 2.13. The necessary parameters are not all present when the symbol is first generated and must be created. These include REFDES, PART, TEMPLATE, EXPR, MODEL, and DESCRIPTION. For this work, the discussion

will be limited to those attributes that must be created from scratch for successful operation.

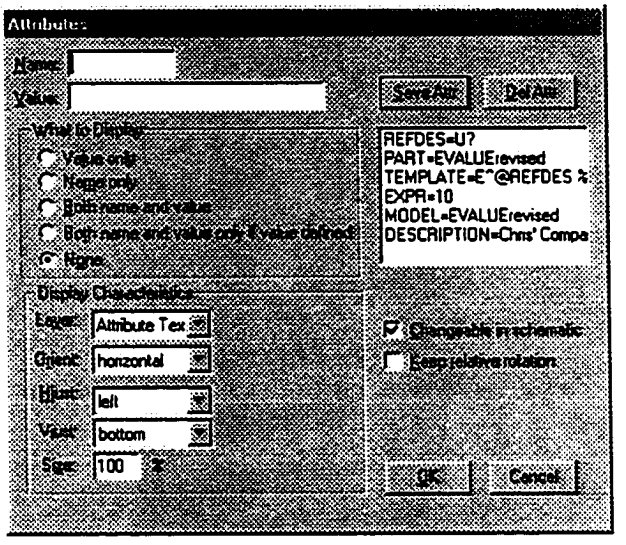


Figure 2.13: PSPICE Attributes dialog box

The PART attribute is displayed when the source is double clicked in Schematics. The MODEL attribute must be defined and tells Schematics which subcircuit definition to look for within the *.lib file (the *.lib file must have the same name as the *.slb file the device symbol resides in eg. test.slb and the corresponding test.lib). The EXPR attribute will be user configurable by double clicking on the source in schematics. It is simply a string variable which will be the receptacle used to pass the algebraic expression from the schematics dialog box to the netlist. The TEMPLATE attribute is used by Schematics to

map the pin numbers used by the source to the net list. It also handles the passing of any ABM keywords data to the netlist. For example, the expression entered for the EXPR attribute in the Schematics dialog box is passed to the netlist using the format called out in the TEMPLATE statement. The various wildcard characters can be found in the PSPICE A\D User's Guide and will not be discussed here.

The Pin List and Definition items on the Part menu must also be addressed. These windows are self-explanatory. The Pin List menu allows the user to define pin names. These names must be consistent with those used in the *.lib file as well as those used in the TEMPLATE statement. The Definition menu is used to assign part description and type and should be consistent with those used earlier in the model's development. The screen shots of the Pin List and Definition dialogs, the TEMPLATE statement, as well as the model's associated *.lib file are included here for reference as Figure 2.14 through 2.16 below.

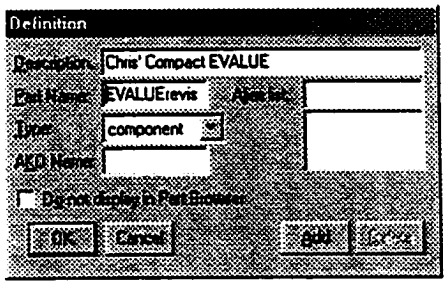


Figure 2.14: PSPICE Definition dialog box

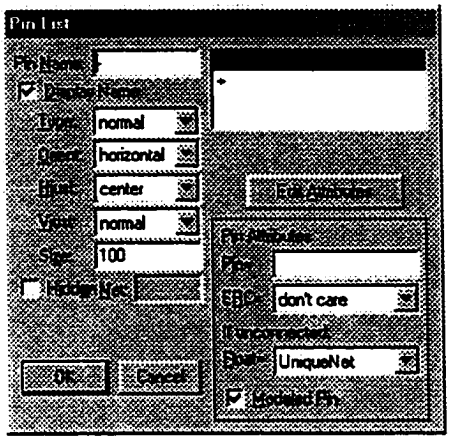


Figure 2.15: PSPICE Pin dialog box

```
E^@REFDES %+ %- VALUE { @EXPR }
```

Figure 2.16: PSPICE Template statement

```
.SUBCKT EVALUErevised + - PARAMS: EXPR={EXPR}
  EVALUE + - VALUE = {EXPR}
.ENDS EVALUErevised

.SUBCKT GVALUErevised + - PARAMS: EXPR={EXPR}
  GVALUE - + VALUE = {EXPR}
.ENDS GVALUErevised

.SUBCKT ETABLErevised + - PARAMS: EXPR={EXPR}
TABLE={TABLE}
  ETABLE + - TABLE {EXPR} = {TABLE}
.ENDS ETABLErevised
```

Figure 2.17: PSPICE Custom Library

The previous screen shots are for the custom EVALUErevised source. The other two can be generated following a similar procedure using the appropriate syntax for the ABM keyword.

The final product is a custom source that has no input pins and follows the graphics symbolism used in the development of the modeling approach. Information about the sources controlling expression is input within the Schematics editor by double clicking on the source. An example of the ETABLErevised source and its associated dialog box is shown as Figure 2.18 for reference.

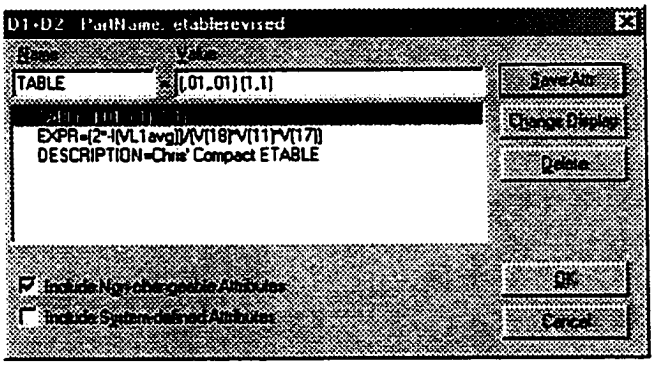


Figure 2.18: PSPICE custom source dialog box

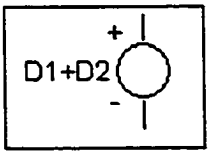


Figure 2.19: PSPICE custom source symbol

2.6 Boost Model Validation

Having established the proper tools to implement the averaged equivalent models in PSPICE, we are prepared to investigate the boost converter model as a test case. Figure 2.20 shows the boost converter as it appears in the Schematics package.

Looking at the schematic we see that it is the PSPICE representation of the boost model derived in the previous section, Figure 2.20. A noticeable difference is that the sources for D_3 and T are not present. Since these values are either supplied by the modeler or easily calculated there is no need to show their values explicitly. The numbering scheme used in the development of the boost model varies from the one used in PSPICE.

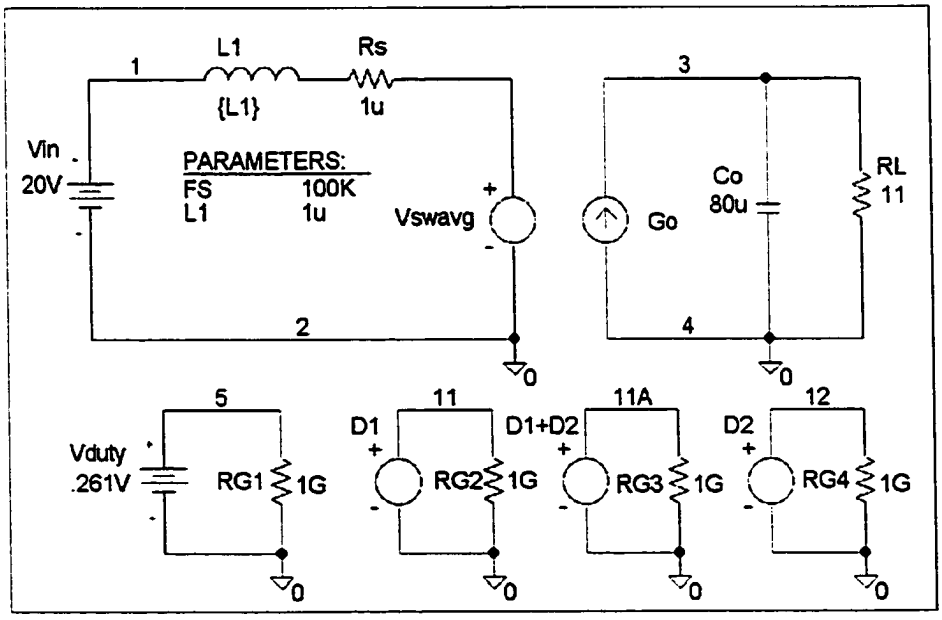


Figure 2.20: PSPICE schematic model of boost

The reader should refer to the PSPICE node numbers when validating equations. The controlled source equations and table parameters are directly from the earlier development and are shown below for reference in Table 2.1.

Table 2.1: Boost modeling equations

	Controlling Expression	Table Limit
Vswavg	V(1,2)*(1-V(11)-V(12))+V(3,4)*V(12)	N\A
Go	I(Vswavg)*V(12))/(V(11)+V(12))	N\A
D1	V(5)	(.001,.001) (1,1)
D1+D2	(2*I(Vswavg)*FS*L1)/(V(1,2)*V(11))	(.001,.001) (1,1)
D2	V(11A)-V(11)	(.001,.001) (1,1)

As a first test, a Bias Point Detail simulation will be run to compare PSPICE's solution with the one produced by MathCAD. The results of this simulation will validate the DC solution of the model assuming the initial bias point solution chosen by PSPICE is the valid choice.

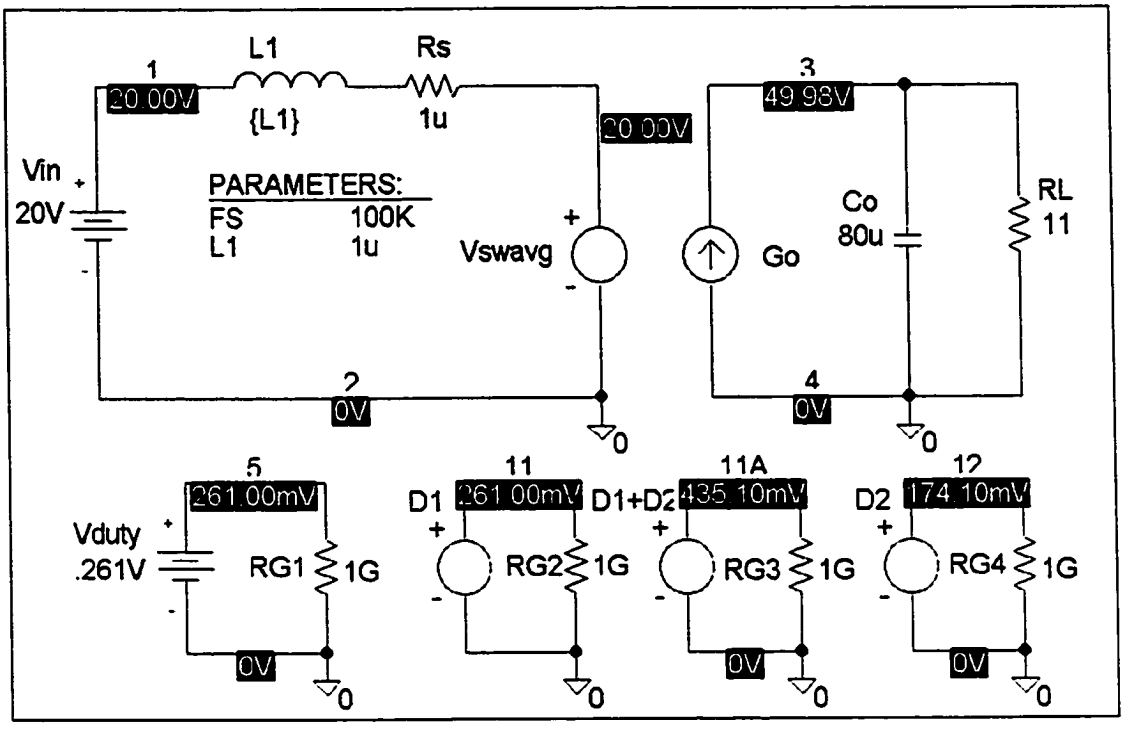


Figure 2.21: Bias point solution of boost model

Several characteristics should be noted from these results. First, the results show that the solution by PSPICE is exactly equal the MathCAD solution of Equation (2.13) down to the thousandth. Second, note that in the steady state solution, the voltage across the inductor is zero as is expected since the circuit is based on average values. And finally, this initial bias point solution done by PSPICE, is the correct operating point, so for any length simulation, the values would not change, they were solved for correctly at the initial "guess".

Comparison Study:

To continue model testing it is appropriate to introduce two benchmark circuits for comparison. The first will be the actual switched circuit and the second, one using the Vorperian model. It should be noted that for the given operating point the converter is in DCM ($D + D_2$ is less than 1 in Figure 2.21) so the Vorperian DCM model will be used.

Testing will continue by evaluating the model's small-signal characteristic control to output transfer function as compared to those of the actual circuit and the Vorperian model. The small-signal characteristics will be generated by using PSPICE's AC Sweep analysis for the averaged models. The actual circuit cannot be used in conjunction with PSPICE to develop these curves due to the presence of the switching elements so the transfer functions developed earlier by State-Space Averaging will be referenced.

The circuits used in the PSPICE analysis are shown in Figures 2.22 and 2.23 below. In both cases, the DC source V_{dy} is replaced with a composite source V_{dyc} which has two components, a DC value to set the operating point and a 1V AC value that will be swept by the simulator during the analysis. Markers for magnitude and phase of the control to output transfer function are placed at the output voltage.

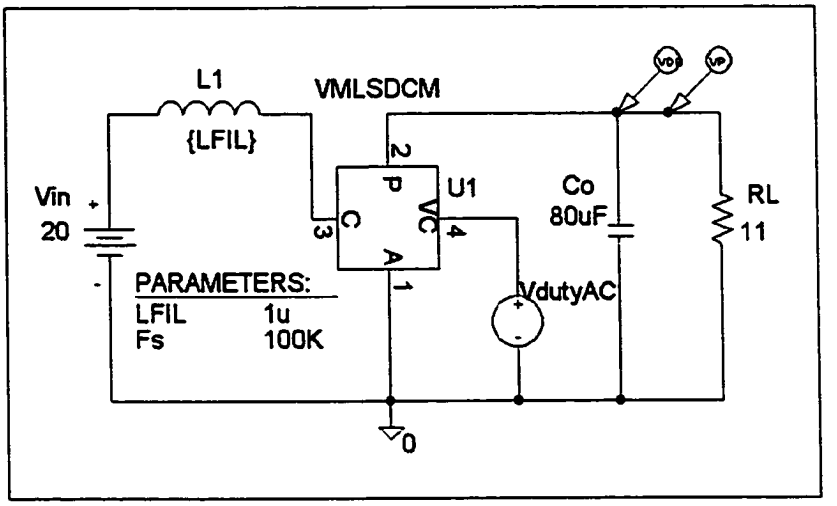


Figure 2.22: AC Sweep Schematic: Vorperian

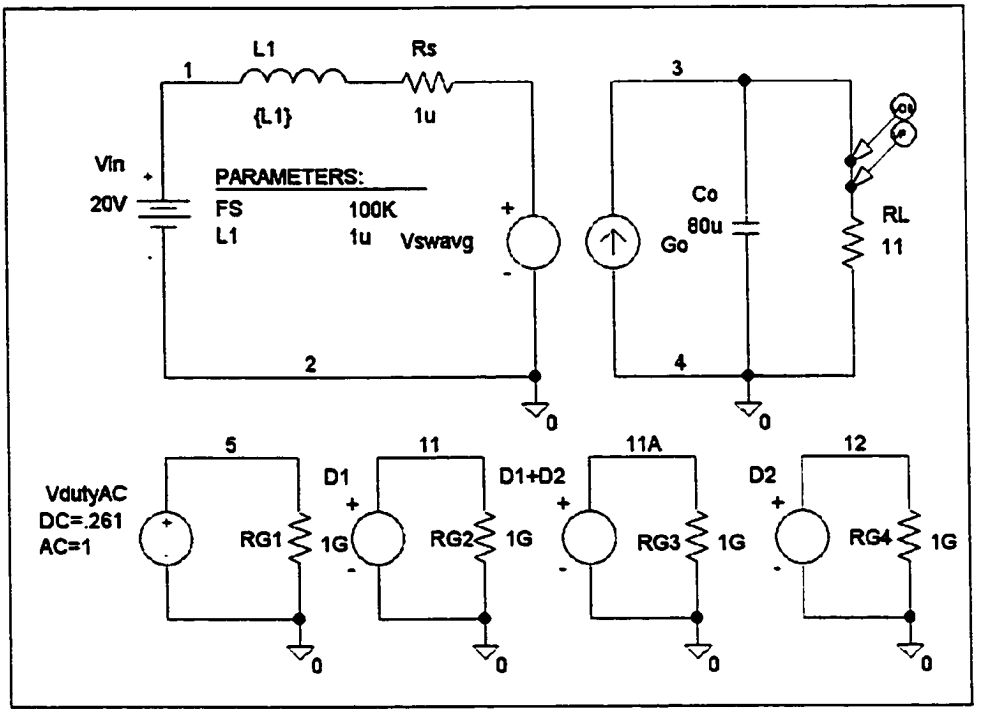


Figure 2.23: AC Sweep Schematic: New model

Frequency Response:

The control-to-output transfer functions for Figures 2.22 and 2.23 are superimposed in Figure 2.24. In addition, the results from the State-Space Averaging method are also shown. The curves for node R7:1 represents the results from State-Space Averaging while the curves for node RL:1 represent the results of the averaged models. Note that both the averaged models show near perfect agreement with the results obtained from State-Space Averaging at low frequencies. However, as discussed in the section on Vorperian's models, both average models deviate from the State-Space Averaging results as the frequency approaches the switching frequency. This is a direct result of the order reduction endorsed by Cuk in his development of State-Space Averaging. Agreement between the averaged models is also good with a slight deviation as the frequency is increased.

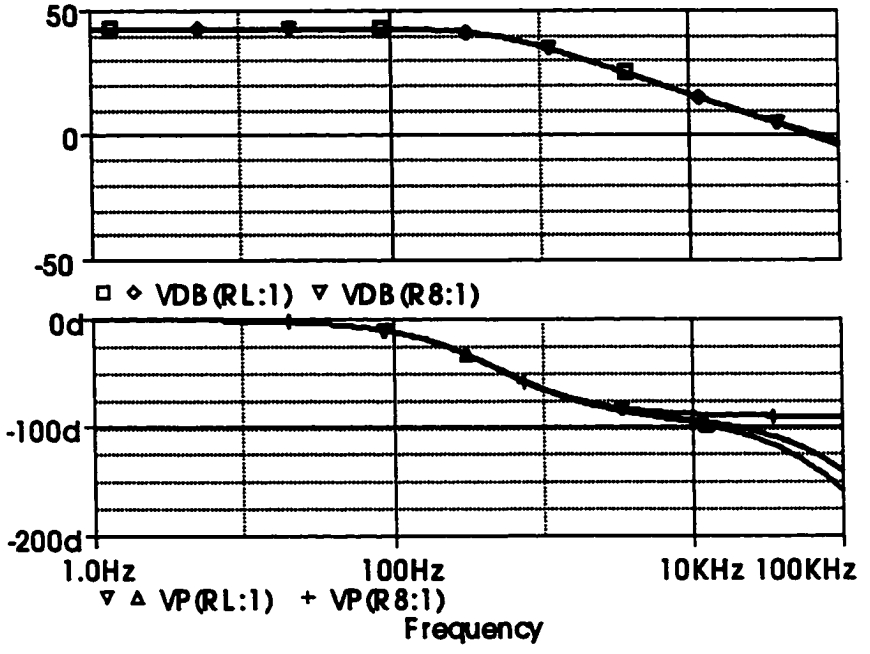


Figure 2.24: Small-signal curves superimposed

Transient Response:

The next model test will take the form of a time domain transient simulation. The purpose is to evaluate the model's dynamic response characteristics. Once again, a comparison will be made between the results of the actual circuit, the Vorperian model, and the new model. All circuits will employ the same controller so that the model can be directly compared. The circuits used for the simulation are shown in Figures 2.25 through 2.27 below.

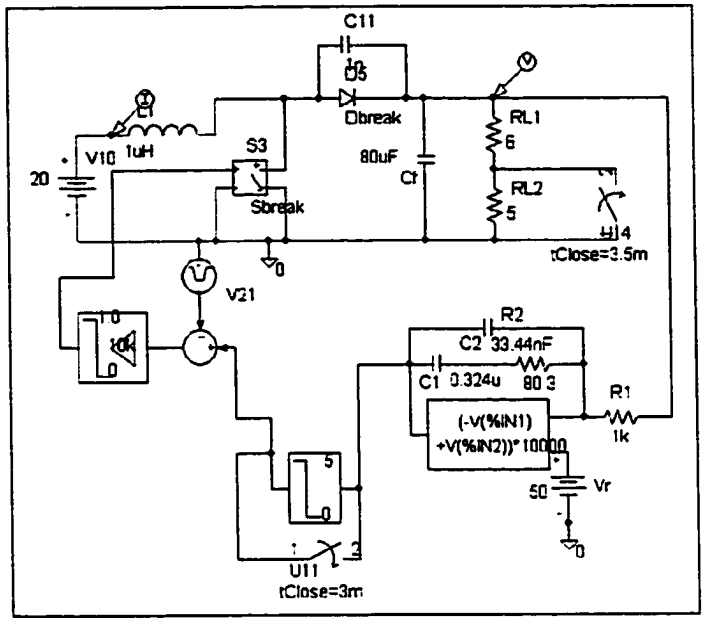


Figure 2.25: Boost schematic: Actual Circuit

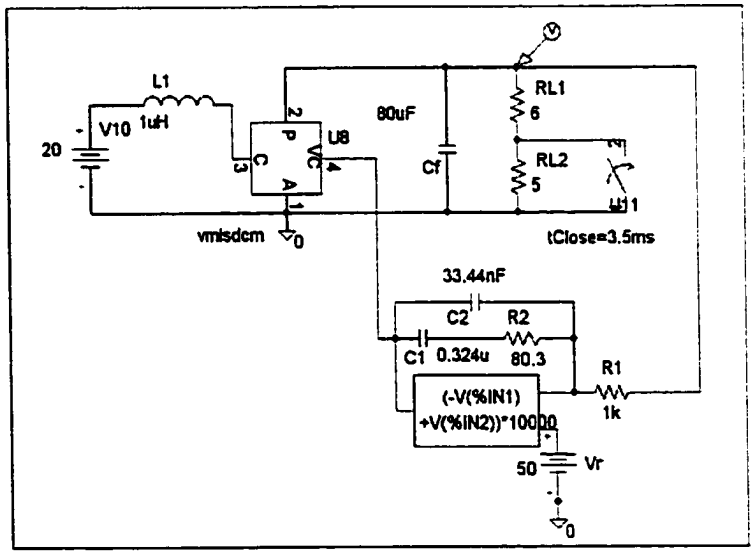


Figure 2.26: Boost schematic: Vorperian

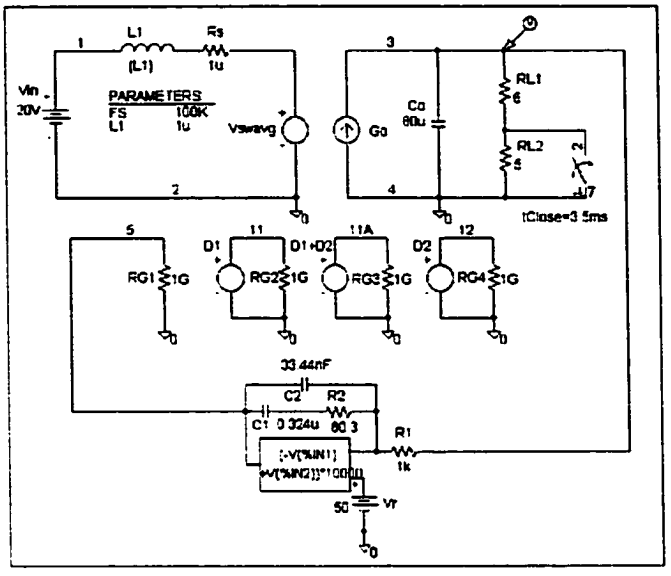


Figure 2.27: Boost schematic: New Model

First, a comparison of the two averaged models is made by superimposing the output of the two models during the transient. Figure 2.28 shows that the two averaged models respond virtually identically during the transient and are in complete agreement.

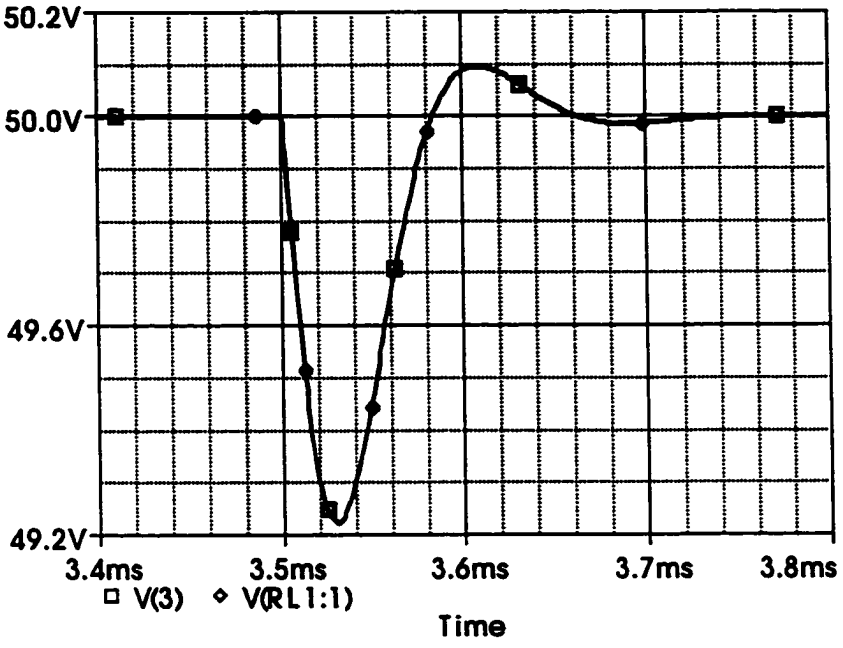


Figure 2.28: Average model transient comparison

Finally, Figure 2.29 compares the outputs of the averaged models to that of the actual circuit where all are superimposed. The top plot is the output voltage and the bottom is the choke inductor current.

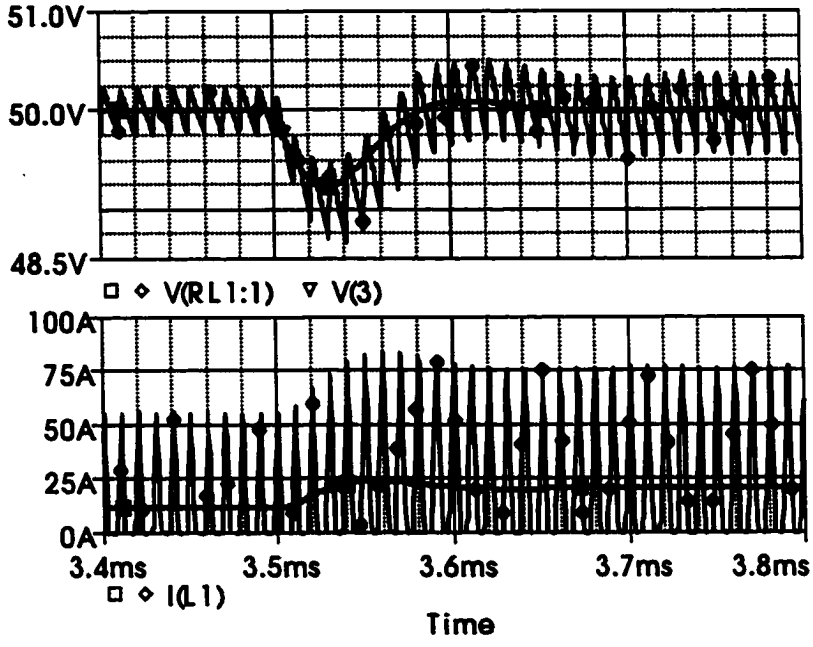


Figure 2.29: Simulation output comparison

With the inclusion of the actual circuit, the most notable difference when compared to the averaged model's results is the presence of output voltage ripple. In the actual circuit, the high frequency oscillations are present because the low pass effect exhibited by the output capacitor is not enough to completely smooth the abrupt discontinuities in the switching function. Although the same output capacitance is used in all simulations, the ripple is not present averaged circuit. This can be explained by considering the averaged model approach.

It is apparent that the averaged models produce results that closely follow the transient in the actual circuit. In fact, if we were to average the results of the actual circuit over one

ripple cycle and adjust the step ceiling used in the averaged circuit simulation, we would arrive at the same results as that of the averaged models.

In the design of the power stages simulated here, a small output capacitor was used to exacerbate the differences between the actual and averaged circuits due to voltage ripple. In practical power converter designs, the output capacitor is much larger and hence the ripple is significantly reduced. In this situation, the averaged models will exhibit nearly identical output voltage characteristics as the actual circuit during the transient.

From the previous discussion, the conclusion might be that the averaged circuit model is very accurate, producing the identical results when the proper capacitance is used. However, an examination of the inductor current reveals this approach is not without shortcomings. The bottom plot in Figure 2.29 shows the inductor current waveform from the two simulations superimposed on one another. Here we see a more significant difference. Since the inductor current only flows during Modes I and II, the average value is significantly lower than the its peak value. The choice of larger inductors would reduce this ripple. However, the condition of DCM operation would prevent this design change from significantly improving the differences between the actual and averaged circuits. Based on this deviation, the user should assume that the averaged models produce accurate results only when the instantaneous values of interest closely approximate their averages.

CCM Case:

Having thoroughly tested the boost model in DCM operation, the only remaining task is to demonstrate the model's ability to produce an accurate solution under CCM conditions. Recall, that the voltage conversion ratio, M, undergoes a change when the converter operating mode changes. The expressions for each mode are shown below as Equations (2.17) and (2.18).

For CCM,

$$M = \frac{1}{1 - D_1} \tag{2.17}$$

For DCM,

$$M = \frac{D_2 + D_1}{D_2} \tag{2.18}$$

From the MathCAD solution in Equation Set (2.19), the voltage conversion ratio is calculated is as shown in the following:

$$V_{in} := 20 \qquad D_1 := .261 \;\Big|\; D_2 := .17409707942168902635$$
$$M := \frac{D_2 + D_1}{D_2} \qquad V_o := V_{in} \cdot M \qquad V_o = 49.983 \tag{2.19}$$

Based on the above, since the converter's nominal output voltage satisfies Equation (2.18), it is clear the converter is in DCM mode.

In order to test the model's solution under the CCM case it is necessary to move the converter to CCM mode and ensure that the proper relationship, Equation (2.17), is satisfied. To ensure the converter is in CCM, the output load resistance will be reduced to an extremely small value, .1 Ω. With the new load, the converter should produce the new conversion ratio, Equation (2.17). To test the model, a transient simulation will be performed with the small R_L. Data from the simulation will be plugged into Equation (2.17) to verify CCM operation.

The boost model schematic for the CCM\DCM test is shown in Figure 2.30.

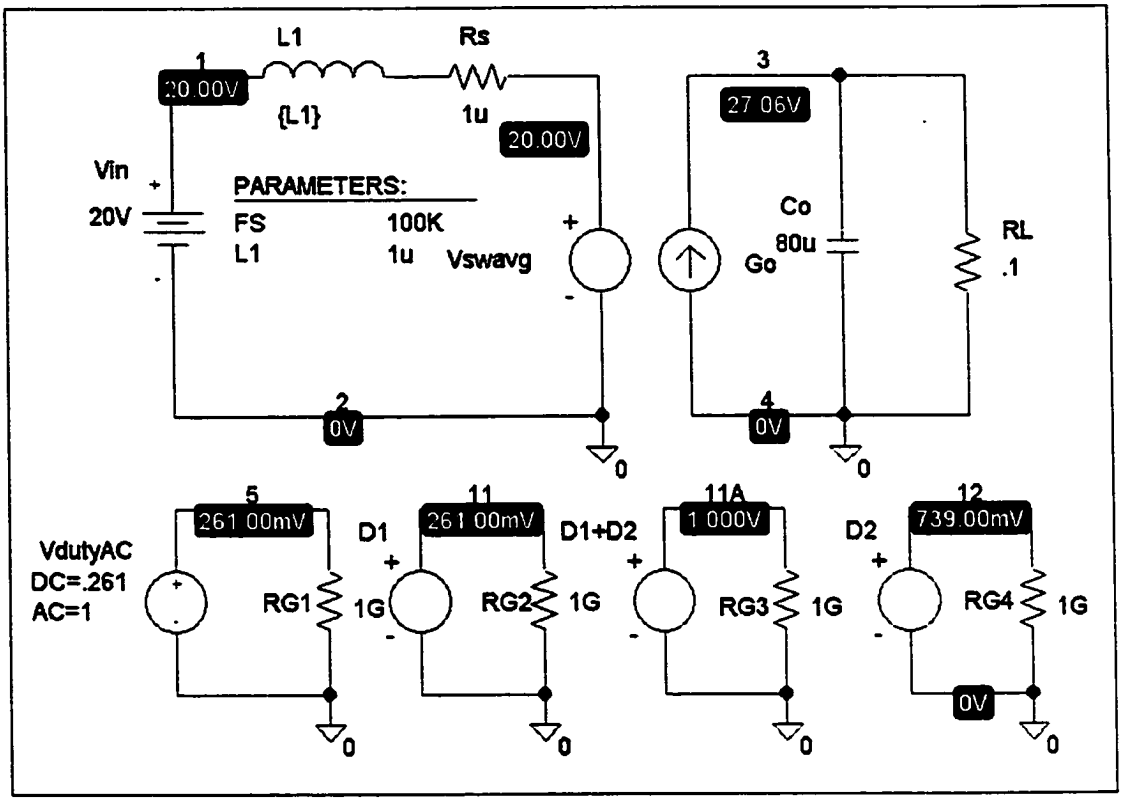


Figure 2.30: Boost CCM/DCM Schematic

Note that, with the exception of the load resistance change, all other parameters remain the same. The bias point solution shown on the schematic is representative of the final transient solution. Note that the controlled source, $D + D_2$ is at its limit value of 1. With $D + D_2$ equal to one, the converter is in CCM operation. To further validate this claim, the CCM voltage conversion ratio, Equation (2.17), will be used as a check.

$$M := \frac{1}{1 - D_1} \qquad M = 1.353 \qquad V_o := M \cdot V_{in} \qquad V_o = 27.064 \tag{2.20}$$

With the CCM voltage conversion ratio valid, the boost model can successfully represent both CCM and DCM operation where as, in the large signal model for Vorperian, the circuit model must be modified.

2.7 Application of Unified Approach to Separated PWM Switch Converter

Following the methodology laid out for the boost test case, this section will present a model for the single stage, single switch , separated PWM Switch converter of Figure 1.5 (Repeated here for convenience).

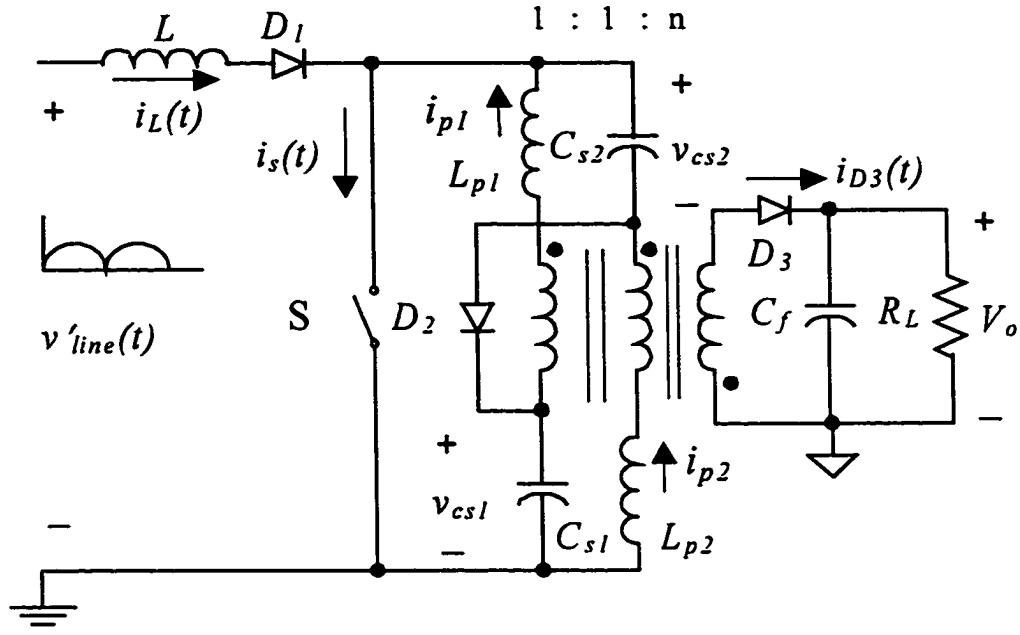


Figure 2.31: Single-stage single switch converter

Examining the circuit reveals that the localized PWM Switch Cell is not present. As a result, the application of Vorperian models requires significant model manipulation [9]. A main focus of this dissertation is to present a more methodical and manageable way to deal with modeling converters of this type.

As in the test case, the modes of operation, and their associated waveforms present a starting point for the approach. A detailed description of converter operation and its steady state analysis is presented in [4] and will not be repeated here. In the boost case, a detailed presentation was made justifying the need to maintain the functionality of the

energy storage elements within the converter. For that case, the choke inductor was the only element considered as part of the model. However, for the circuit of Figure 1.5, the two capacitors, C, are also present and do contribute to the dynamic nature of the converter. Based on the previous discussion for the inductor, a similar approach can be applied by taking the average of the capacitor current. Further, since the two capacitors appear in identically functioning branches, only one need be considered to produce a minimal representation.

Average Equation Derivation:

The instantaneous waveforms needed are shown in Figure 2.32. Averages for the instantaneous functions form the expressions that will make up the model. The equations for the average values are shown as Equations (2.21) through (2.25) below.

$$V_{swavg} = 2 \cdot V_{cs} \cdot (D_2 + D_3) + V_{in} \cdot D_4 \tag{2.21}$$

$$I_{cavg} = \frac{T_s}{2} \cdot \left[\frac{V_{cs} - \frac{V_o}{n}}{L_1} \cdot D_1 \cdot (D_2 - D_1) + \frac{V_{in} - 2 \cdot V_{cs}}{L} \cdot D_2 \cdot (D_2 + D_3) + \frac{V_{in}}{L} \cdot D_1 \cdot (2 \cdot D_2 + D_3) \right] \tag{2.22}$$

$$I_{Lavg} = \frac{1}{2} \cdot \frac{V_{in}}{L} \cdot D_1 \cdot T_s \cdot (D_1 + D_2 + D_3) \tag{2.23}$$

$$I_{L1avg} = \frac{1}{2} \cdot \frac{V_{cs} - \frac{V_o}{n}}{L_1} \cdot D_1 \cdot T_s \cdot (D_1 + D_2) \tag{2.24}$$

$$V_{L1avg} = V_{cs}\cdot(D_1 - D_2) - \frac{V_o}{n}\cdot(D_1 + D_2) \tag{2.25}$$

$$I_o = \frac{2}{n}\cdot I_{L1avg} \tag{2.26}$$

As in the boost example, these equations represent the core of the model. The equations for average voltage across the inductor and average current through the capacitor are used in conjunction with controlled sources to form the model. As expected, in the steady state operation, these equations will equal zero. Nonzero values will only result during transients.

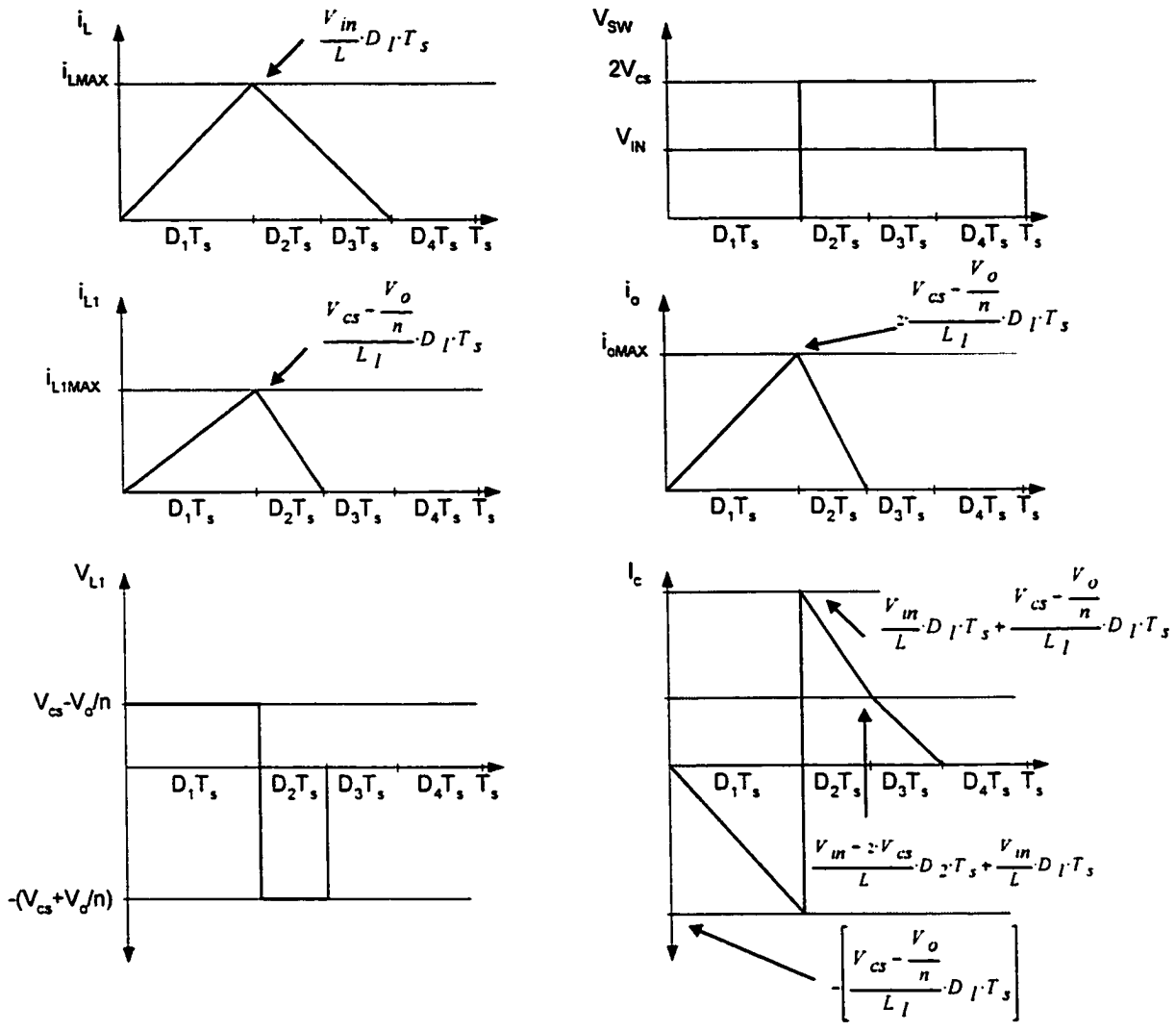


Figure 2.32: Instantaneous waveforms of single-stage single switch converter

The equation for $V_{w\ vg}$ is actually the voltage to the immediate right hand side of the inductor and not the switch voltage, due to the presence of diode, D. As in the boost case, the voltage at the inductor right hand side node is averaged rather than the differential voltage in anticipation of the externally applied V_{IN}.

The duty ratios are formed from the expressions for average inductor currents. Rearranging Equations (2.23) and (2.24), we arrive at the expressions for the two duty ratio sums as shown below in Equations (2.27) and (2.28).

$$D_1 + D_2 = \frac{2 \cdot I_{L1avg}}{\frac{V_{cs} - \frac{V_o}{n}}{L_1} \cdot D_1 \cdot T_s} \tag{2.27}$$

$$D_1 + D_2 + D_3 = \frac{2 \cdot I_{Lavg}}{\frac{V_{in}}{L} \cdot D_1 \cdot T_s} \tag{2.28}$$

Since D is provided as input, Equation (2.27) can be used to solve for D_2. With D_2 known, Equation (2.28) can be used to obtain D_3 and D_4 ($D_4 = 1 - D - D_2 - D_3$). As before, references to inductor current in the duty ratio expressions are the real time values in the averaged circuit to maintain the dynamic nature of the actual circuit in the model.

Average Circuit Derivation:

The completed model schematic is shown in Figure 2.33.

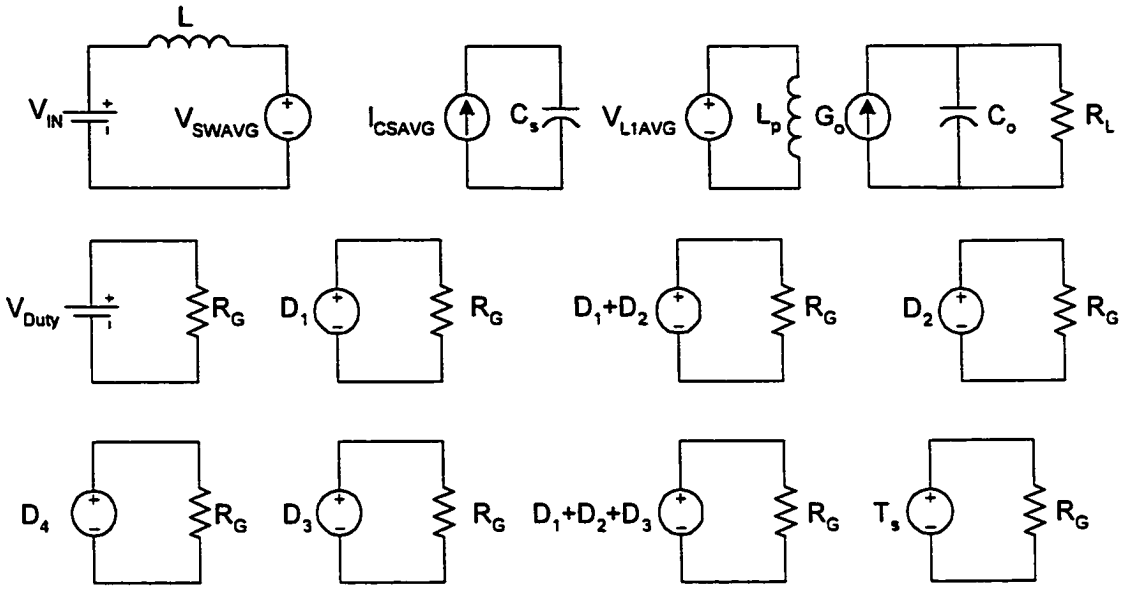


Figure 2.33: Completed model for circuit of Figure 1.5

The same fundamental arguments used in the boost discussion apply here. In particular, limiters will be used to allow CCM to DCM transition for either of the two inductors. The duty ratio sum sources, in combination with the D input, are the mechanism used to create all the individual duty ratios.

Before moving the model to the simulator, it is now appropriate to apply MathCAD's nonlinear solver to the model equations. Equation set (2.29) below shows the valid solution set for the given model.

$$L := 482.3\cdot10^{-6} \qquad R := 50 \qquad n := .27 \qquad F_s := 50\cdot10^{3}$$

$$V_{in} := 120 \qquad L_1 := 80.9\cdot10^{-6} \qquad D_1 := .3406 \qquad T_s := \frac{1}{F_s}$$

Given

$$V_{in} - \left[\left[2\cdot V_{cs}\cdot(D_3 + D_2)\right] + V_{in}\cdot D_4\right] = 0$$

$$\frac{V_o}{R} = \frac{1}{2}\cdot(D_1 + D_2)\cdot\frac{(n\cdot V_{cs} - V_o)}{n^2\cdot\frac{L_1}{2}}\cdot D_1\cdot T_s$$

$$D_1 + D_2 + D_3 = \frac{I_{Lavg}2}{\frac{V_{in}}{L}\cdot D_1\cdot T_s}$$

$$0 = \frac{T_s}{2}\cdot\left[\frac{\left(V_{cs} - \frac{V_o}{n}\right)}{L_1}\cdot D_1\cdot(D_2 - D_1) + \frac{V_{in} - 2\cdot V_{cs}}{L}\cdot D_2\cdot(D_2 + D_3) + \frac{V_{in}}{L}\cdot D_1\cdot(2\cdot D_2 + D_3)\right]$$

$$D_4 = 1 - (D_1 + D_2 + D_3)$$

$$0 = V_{cs}\cdot(D_1 - D_2) - \frac{V_o}{n}\cdot(D_1 + D_2)$$

$$\text{Find}(V_o, V_{cs}, D_2, D_3, D_4, I_{Lavg})\ \text{float},3 \rightarrow \begin{pmatrix} 0 & 2.58 & -672. & -34.6 & 50.0 \\ 0 & -.231 & 60.2 & -135. & 195. \\ -1.19\cdot10^{19} & -.358 & -.358 & 8.25\cdot10^{-3} & 8.25\cdot10^{-3} \\ 1.19\cdot10^{19} & 1.82\cdot10^{-2} & 88.7 & -.113 & .144 \\ 1. & .999 & -87.7 & .764 & .508 \\ 0 & 1.11\cdot10^{-3} & 75.2 & .200 & .417 \end{pmatrix} \qquad (2.29)$$

MathCAD puts forward five potential solutions. It should be note that the fifth solution is the only physically possible choice. Therefore, the fifth solution should be considered

the nominal operating point. This solution corresponds to the one arrived at by conventional analysis techniques and therefore the model has been verified.

In the next section, the model will be tested in the simulator package. As in the boost case, the model will be compared with the actual circuit for time domain transients and its small-signal response will be compared with the results from state-space averaging. Since the Vorperian model is not directly applicable to this circuit, no comparison will be made.

Simulation Study:

The model, as it appears in PSPICE Schematics, is shown in Figure 2.34. The form of the model varies from the development in the previous section but the core expressions are the same.

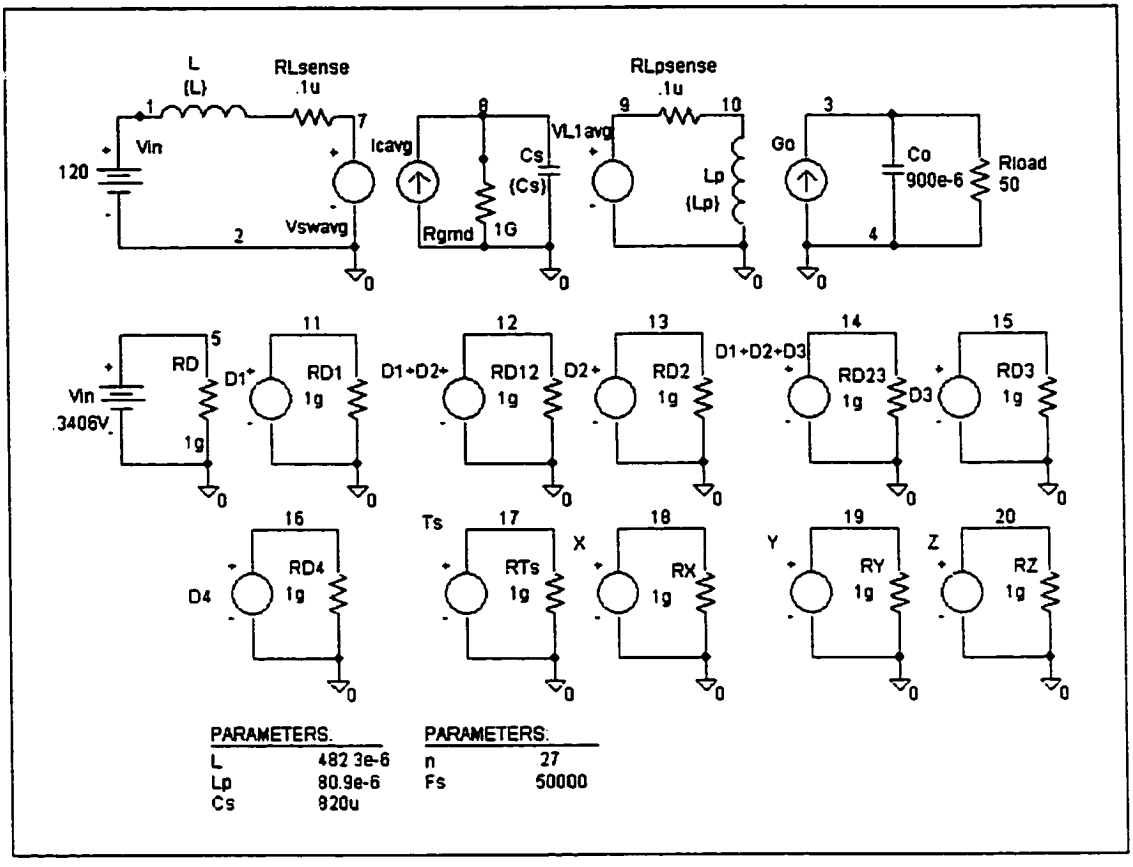


Figure 2.34: PSPICE Schematic for model of Figure 2.33

Sources X, Y, and Z are used to simplify references and represent common factors in the averaged expressions. In Figure 2.34, the modeling equations are broken down into its simplest terms. However, the source equations can be combined reducing the number of components. For the development here, the choice of the most readable form is made.

The modeling equations are shown in Table 2.2 below. Note that the sources X, Y, and Z are representations of the inductor current slope and, as such occur, with some frequency in the model. The definition of common terms simplifies model input but makes numerical convergence more difficult. As a part of a future work, a comparison will be made between the simple form of Figure 2.24 and a more compact approach. Comments on potential shortcomings of the simple form will be made in a subsequent section.

Table 2.2: Modeling equations for Figure 2.34

	Controlling Expression	Table Limit
Vswavg	2*V(8)*(V(14)-V(11))+V(1,2)*(1-V(14))	(.01,.01) (400,400)
Icavg	/(17)/2)*(V(18)*V(11)*(V(13)-V(11))+V(19)*V(13)*(V(13)+V(15))+V(20)*V(11)*(2*V(13)+V(15	N/A
VLlavg	V(8)*(V(11)-V(13))-(V(3,4)/n)*(V(11)+V(13))	(-200,-200) (200,200)
Go	(2/n)*-I(VLlavg)	N/A
D1+D2	(2*-I(VLlavg))/(V(18)*V(11)*V(17))	(.01,.01) (1,1)
D1+D2+D3	(2*I(Vswavg))/(V(20)*V(11)*V(17))	(.01,.01) (1,1)
D1	V(5)	(.01,.01) (1,1)
D2	V(12)-V(11)	(.001,.001) (1,1)
D3	V(14)-V(12)	(.01,.01) (1,1)
D4	1-V(14)	(.01,.01) (1,1)
Ts	1/(Fs)	N/A
X	(V(8)-(V(3,4)/n))/Lp	(1,1) (1e6,1e6)
Y	(V(1,2)-2*V(8))/L	N/A
Z	V(1,2)/L	N/A

The bias point solution is shown in Figure 2.35 below. Note that this corresponds to the appropriate MathCAD solution. It should be noted that, as opposed to the boost test case, this model requires initial conditions to converge to the appropriate solution.

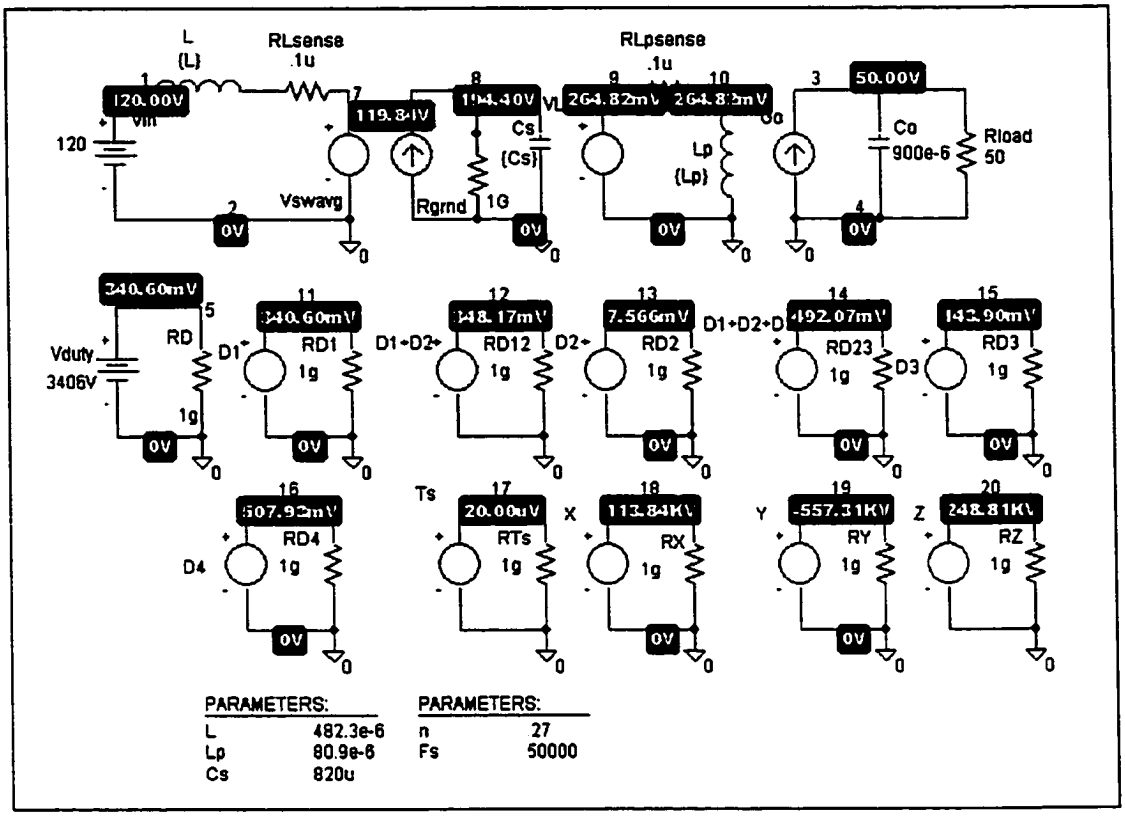


Figure 2.35: Bias point solution for Figure 2.34

Following the development from the boost case, a comparison will be made between the simulation results of the model and those of the actual circuit. The simulation testing will again consist of a small-signal and a time domain transient comparison.

Comparison of Results:

Beginning with the small-signal comparison, the control to output transfer function for this circuit was produced by the method of State-Space Averaging and is presented as

Equation (1.56) in a previous section. This transfer function is compared with the one generated by the model in the schematic below, Figure 2.36.

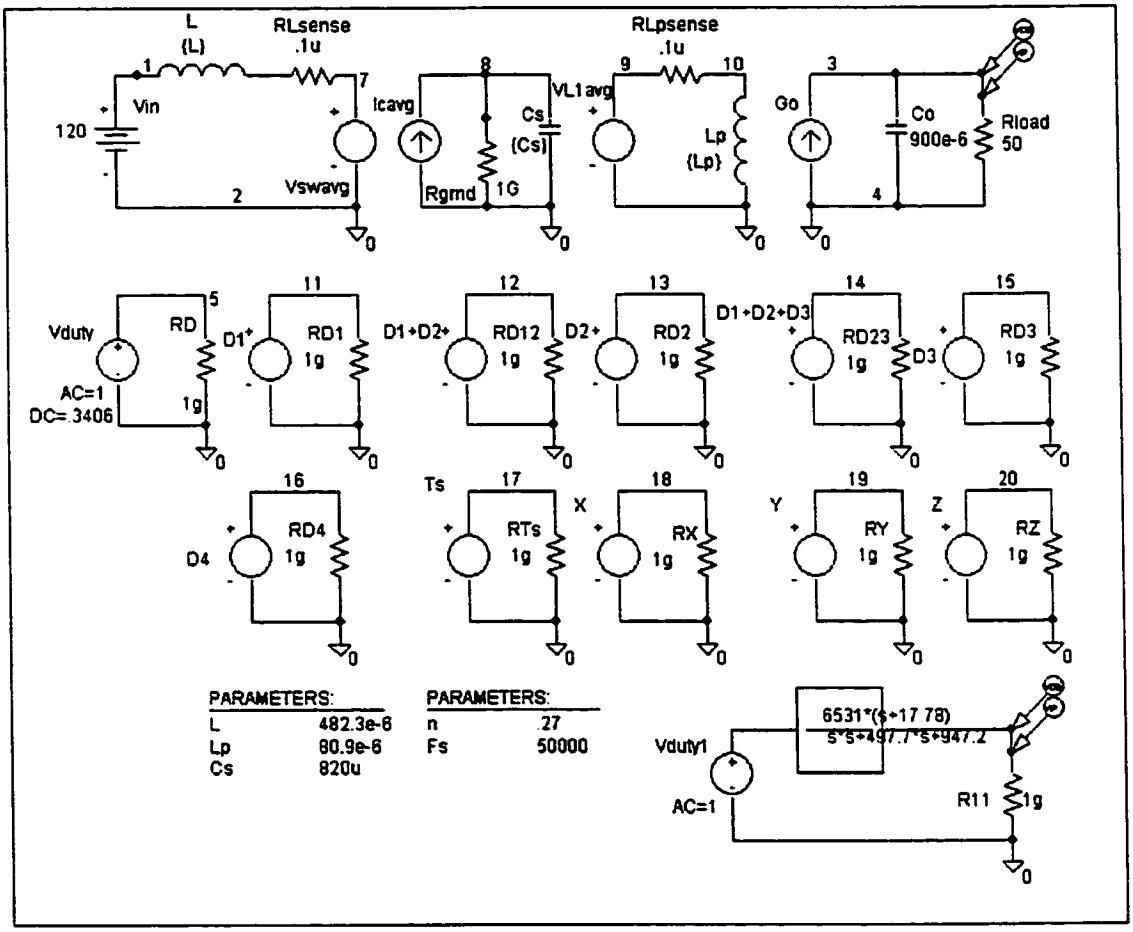


Figure 2.36: AC Sweep Schematic for Figure 2.34

The simulation results show excellent agreement at frequencies below the switching frequency, the results are shown as Figure 2.37. As in the previous case, this deviation is expected owing to inherent differences in the derivation of the curves.

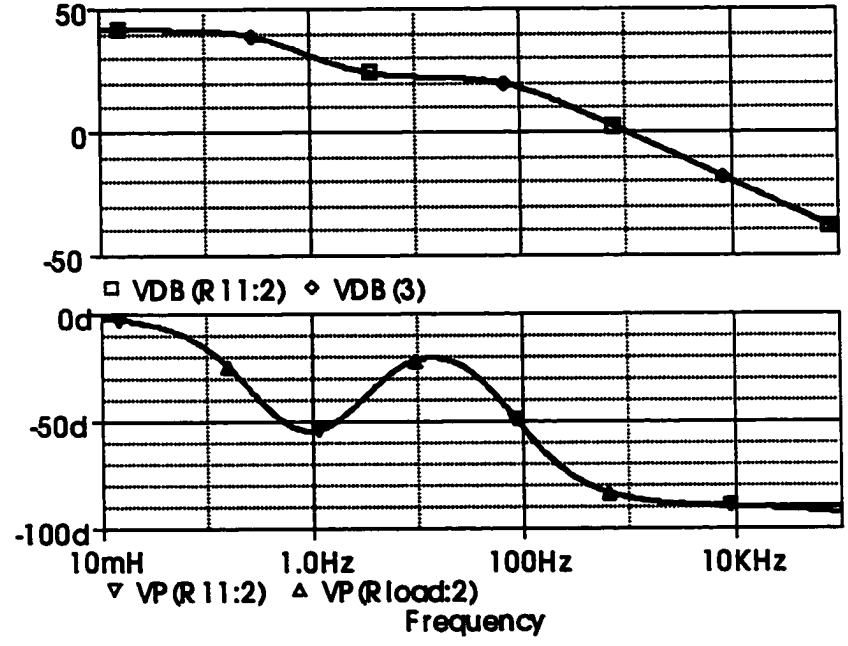


Figure 2.37: Small-signal comparison: Model to SSA

In order to more fully validate the small-signal model, a comparison is made to experimental results. A prototype was built using the same parameters and controller as those used in the simulation models. Since the prototype's output capacitor has an esr,

the model is modified to include a .05 ohm esr. Figure 2.38 shows the results of the small-signal simulation with this esr included.

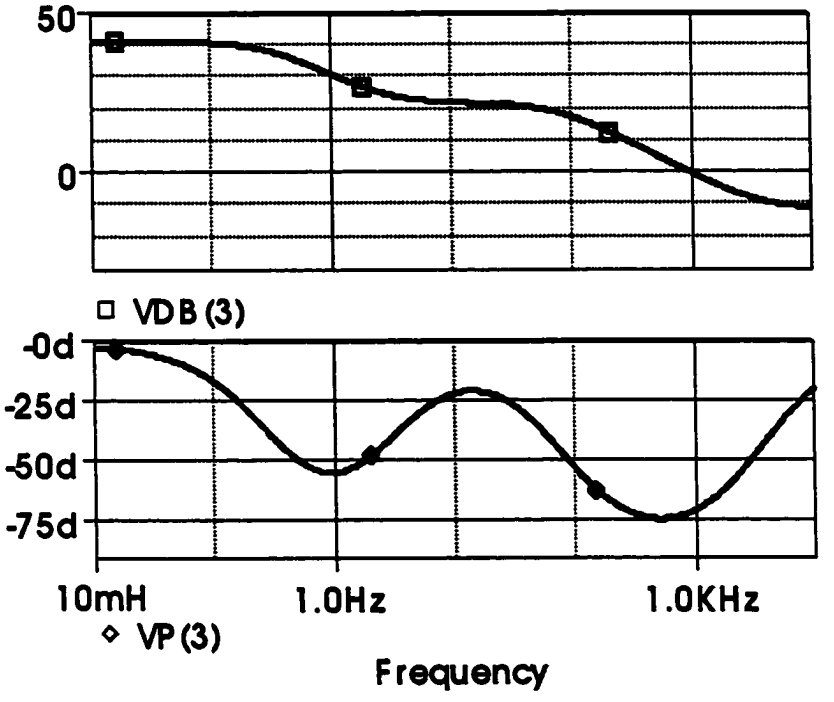


Figure 2.38: Simulated control-to-output response

These simulation results are then compared to those obtained from the prototype as shown in Figure 2.39. Excellent agreement exists with less than 5 dB of difference in the magnitude plots and 6 degrees on the phase plots.

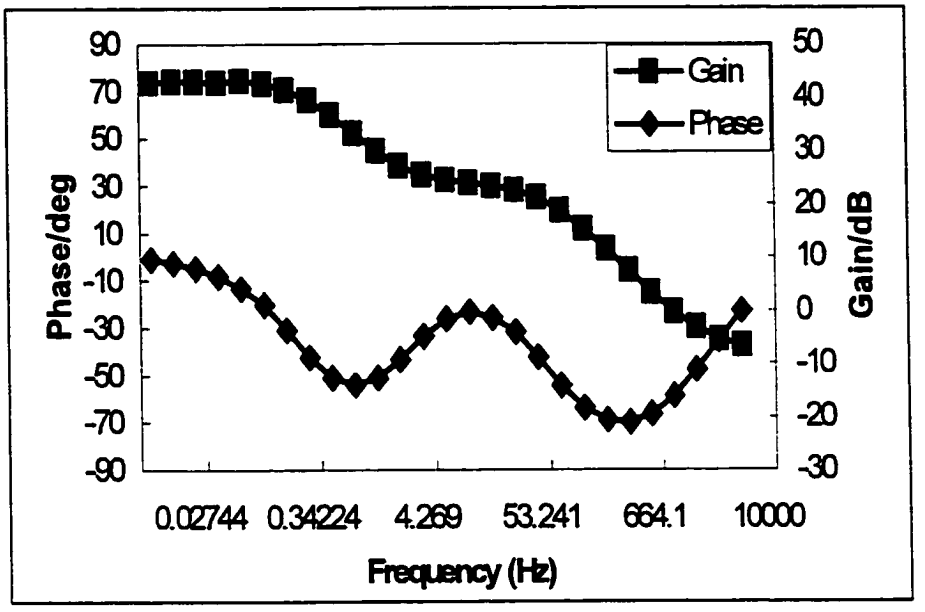


Figure 2.39: Experimental control-to-output response

Next, the dynamic response will be investigated. A comparison will be made between the actual circuit, the model derived above and another averaged model developed by FloridaPEC during a time domain transient. The circuits to be tested are shown as Figures 2.40, 2.41, and 2.42.

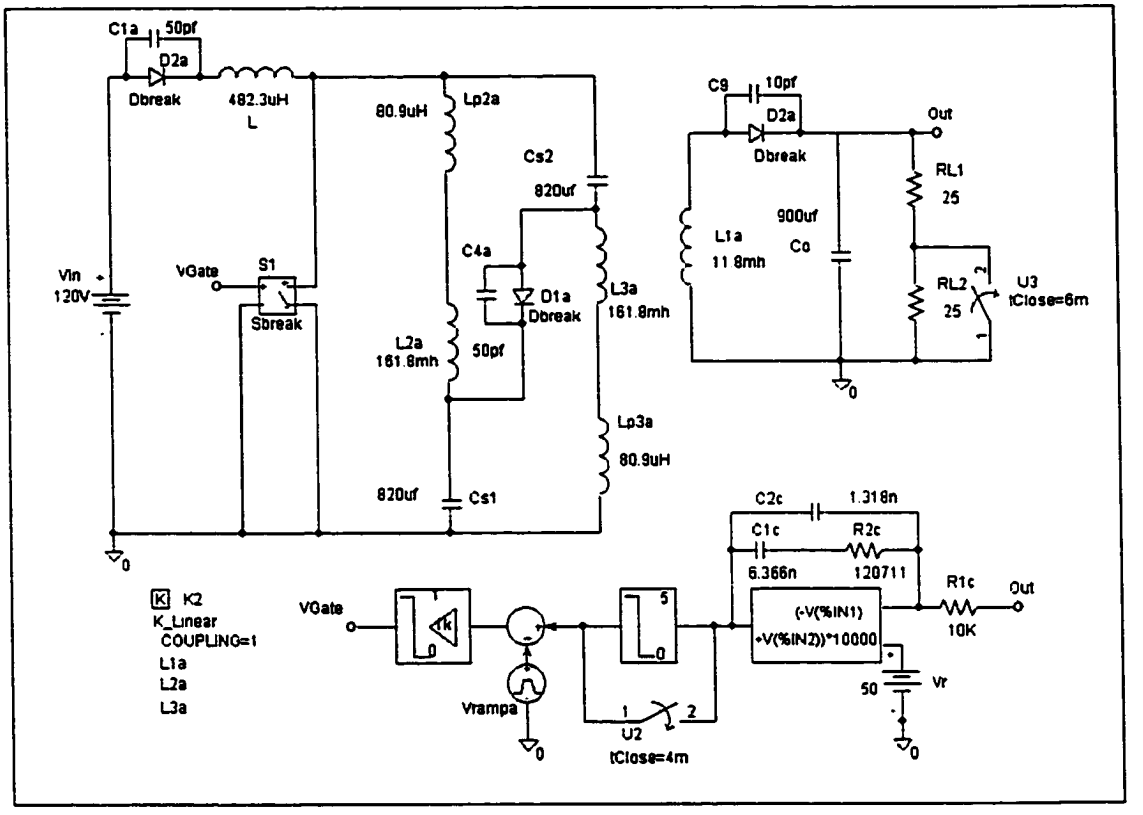


Figure 2.40: Actual circuit schematic-closed loop

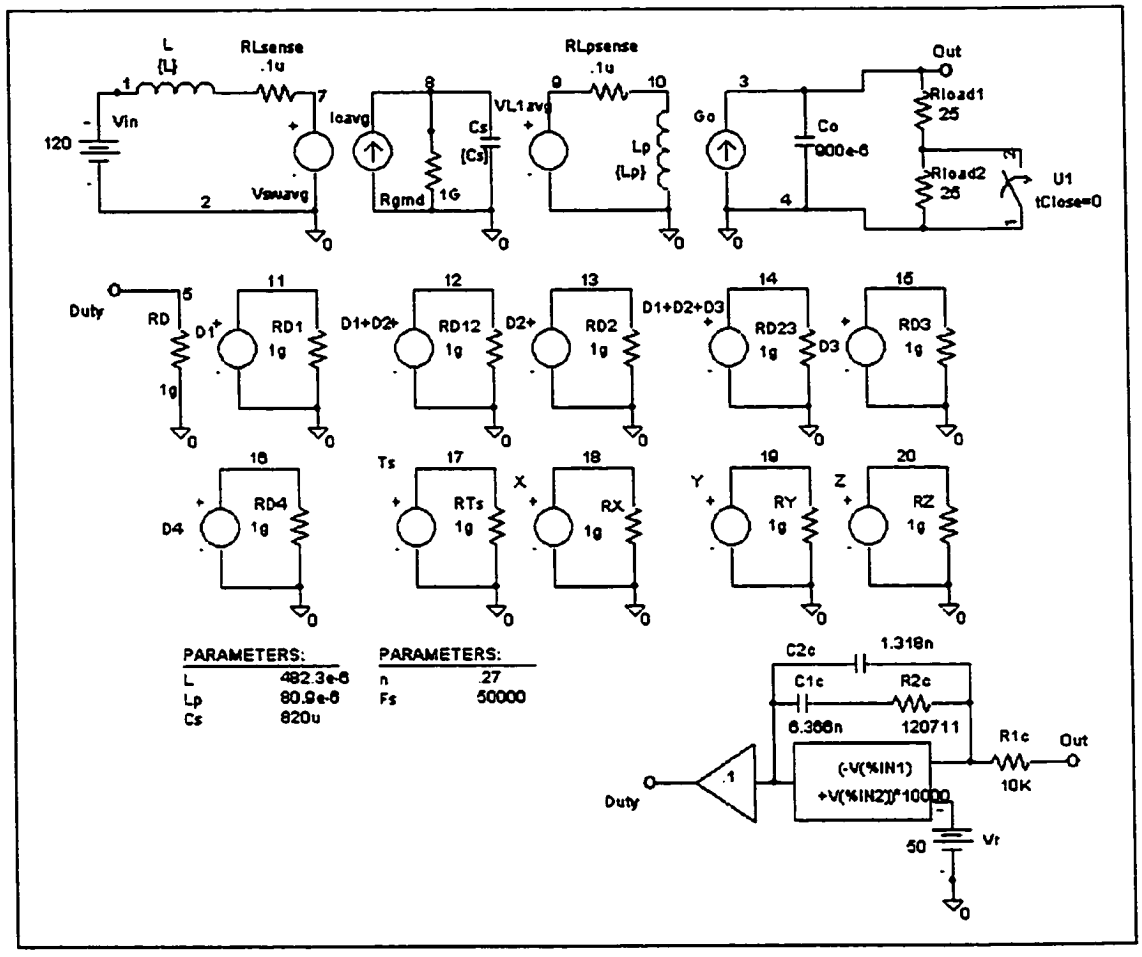


Figure 2.41: New model schematic-closed loop

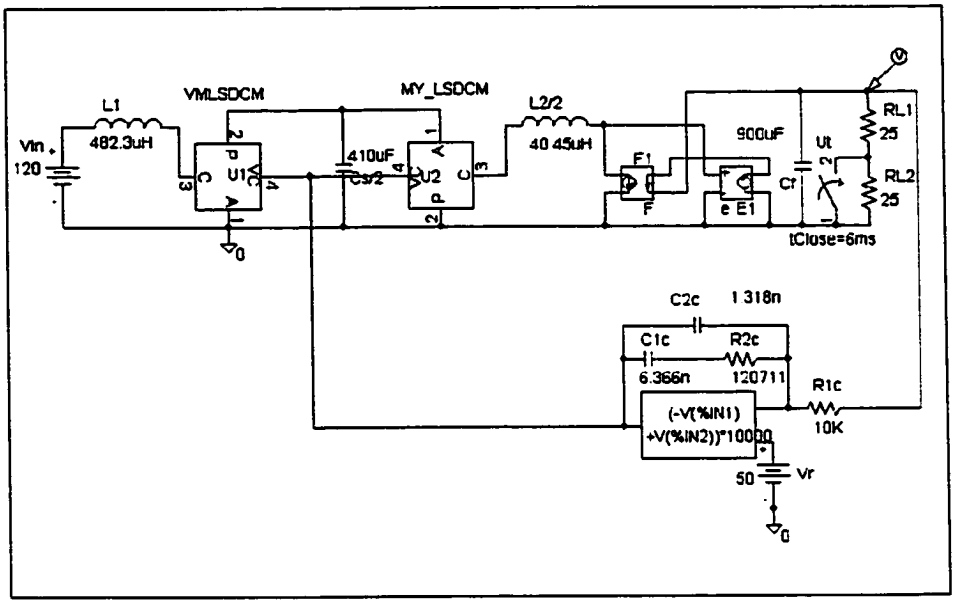


Figure 2.42: Comparative model schematic-closed loop

The circuit of Figure 2.40 represents the benchmark, actual circuit to be modeled. As mentioned previously, the simulation of this circuit is difficult due to significant numerical convergence problems. To aid in these problems, small resistances are included in series with the transformer inductances. These slow system response and improve the chance for convergence. However, although these are necessary for the actual circuit to converge during simulation, their presence in conjunction with that of the non-ideal transformer effect the converter's transient response. In the development of the averaged models, the transformer and resistances are not included and therefore transient response characteristic will differ.

In Figure 2.40, the 0 to 5 limiter is used to allow the actual circuit to start operation. At 4 ms, this limiter is removed to allow the full dynamic range of the control loop. At the output of the limiter, there is a standard ramp and comparator function. This introduces a constant multiplier in the loop gain equal to in inverse of the ramp height. For this case, the ramp height is 10V so the averaged models must account for this constant .1 in their respective loop gains.

In Figure 2.41, the new model developed here is presented in closed loop form. Note as before the same compensator is used. The gain factor of .1, which follows the compensator, is used to account for the comparator's gain term in the actual circuit's loop gain.

In Figure 2.42, another averaged model for the circuit of Figure 2.40 is presented. This model, also developed by FloridaPEC, used a variation of Vorperian's method to develop the model. The ramp height gain is included within the model block and does not need to be distinctly included. The purpose of including this circuit in the comparison is to show good agreement between the averaged models. The development of this model is not shown here but can be obtain from the FloridaPEC website. As in the model developed here, parasitic elements are not included in the model development. The results will show that the averaged models agree well with one another but differ slightly from the actual circuit. This is due to the nonideal aspects included in the actual circuit but neglected in the averaged model development.

The intent here is to show that the averaged models are in good agreement and that they approximate the response of the circuit of Figure 2.40 with the deviation explained above.

In Figure 2.43, the results from each of the averaged model's transient simulations are superimposed.

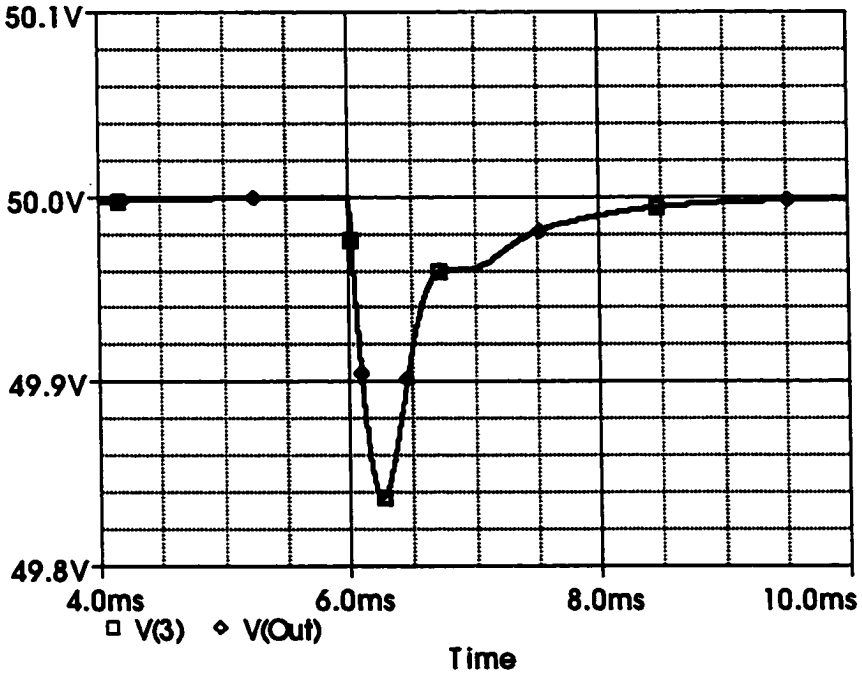


Figure 2.43: Averaged models' output voltage superimposed

Note that the response of the two averaged models is virtually identical as expected.

As presented below, the results of Figure 2.40 are not so close a match. Figure 2.44 shows the results of the actual circuit simulation superimposed on Figure 2.43.

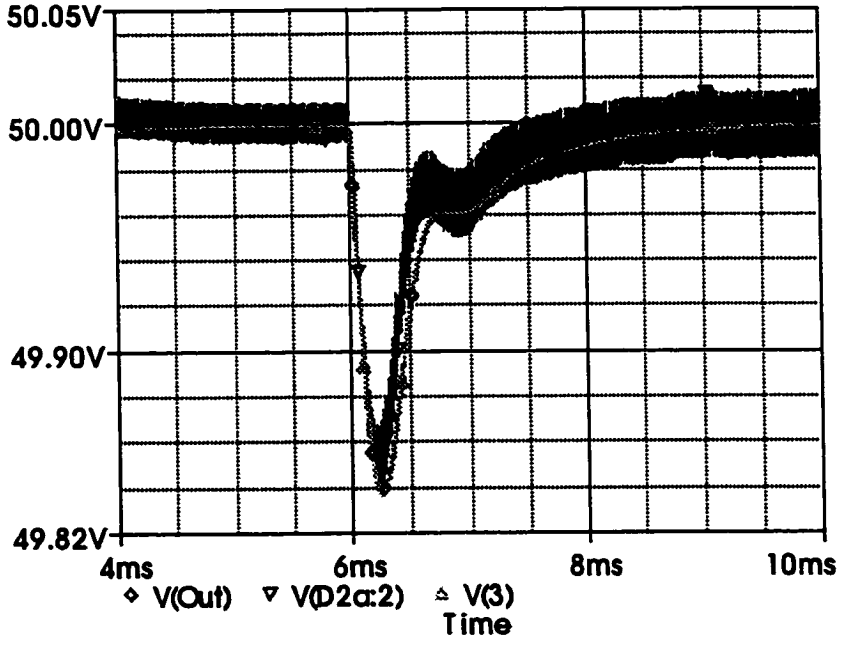


Figure 2.44: The output voltage of the models superimposed with that of the actual circuit

From Figure 2.44, as expected, the results of the averaged models deviate from the results of Figure 2.43.

CHAPTER 3: INCORPORATION OF LOSS MODELING

3.1 Introduction

For power converters, the most significant nonideal effects come from component conduction and switching losses. These loss mechanisms have a significant and measurable impact on the energy input/output transfer and the converter's transient response.

In Chapter 2, it is shown that including nonidealites in the actual circuit simulation led to significant changes in the transient response characteristics of the power stage. As a result, the new, average model developed does not yield results consistent with those obtained by the actual circuit simulation during transient conditions. Moreover, in some instances, particularly resonant periods in soft-switching converters and device switching loss in all cases, the use of nonlinear waveforms in model development is unavoidable, and modelers must deal with more complex functions.

Since these nonidealities are not considered during the model's development, the inaccuracy of the model comes as no surprise. A simple way to correct the model is to include the nonideal effects during the model construction phase. However, this approach leads to a significant increase in model complexity.

The model's derivation is based on averaging the converter's instantaneous waveforms. For the ideal converter, these waveforms are piecewise linear functions, and hence, are easy to work with, yielding average expressions that are simple in nature. By including the nonideal effects, these waveforms will take on nonlinear characteristics. These nonlinear characteristics arise due to various nonideal effects. As an example, when considering switch conduction resistance, the introduction of charging/discharging time constants must be considered. The impact of these time constants is that the converter's waveforms will be exponential functions and inductor current will be, as in the actual converter, exponential in nature. This results in complex average expressions. Fortunately, it will be shown that for most cases, the exponential nature introduced by the nonidealalities does not have a significant effect on the converter waveforms. However, losses incurred by these nonideal components do have a measurable effect and alter the converter's transient response.

Recent work in open literature avoids these unwieldy issues by a several methods. These methods make simplifying assumptions. For example, these assumptions include small current ripple for CCM operation and linear charge/discharge waveforms. The validity of these assumptions will be explored in the following chapter.

3.2 Conduction Loss Modeling in CCM

Conduction loss modeling should be addressed paying close attention to the converter's operating mode, CCM or DCM. Several models exist that model conduction losses as a

simple series resistance. Generally, this series resistance will alter the converter's instantaneous waveforms by the creation of voltage drops. In most cases, these models neglect charging/discharging time constants and assume a straight line approximation to actual exponential curve. Further, it is assumed that inductor current is ripple free so that it can assumed constant. These assumptions make CCM conduction loss modeling fairly straightforward and still yield adequate results.

For DCM however, the assumption of ripple free inductor current cannot be made so a new approach must be presented. Recently, a colleague here at UCF has presented a concept that works with the energy conservation principle [30]. The adequacy of this concept will be explored, and if satisfactory, it will be applied to the unified modeling approach presented in this dissertation.

Several CCM conduction loss models are available in open literature. One example is presented by Erikson and company from the University of Colorado [44]. The approach, like most CCM loss modeling schemes, assumes a constant (ripple-free) inductor current. To investigate the validity of this approach, we will develop a loss-based model by the Erikson approach and perform several simulations to evaluate its validity.

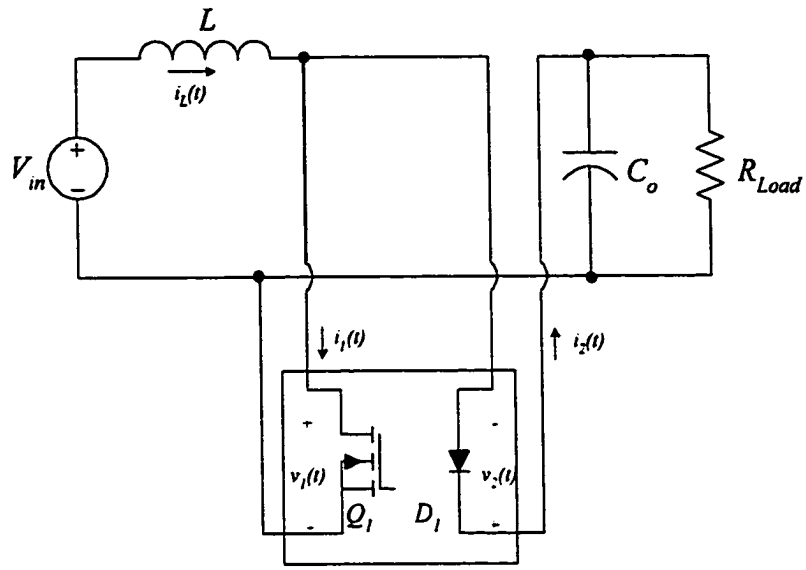


Figure 3.1: Erikson two-port network

The Erikson average modeling concept involves removing all the switching elements in a circuit by averaging their terminal voltage and current characteristics. For the classic topologies, where a single diode and switch combination exists, this amounts to averaging the voltage and current of a two port network. The Figure 3.1 illustrates the formation of the two port network for the boost converter.

The Erikson approach assumes a constant on state resistance for both the switch, R_{on} and diode, R . It also incorporates the diode voltage drop as a constant DC source. Further, this technique makes the simplifying assumption that, for CCM, inductor current is ripple-free i.e. constant. By including these factors, the instantaneous waveforms are altered as shown.

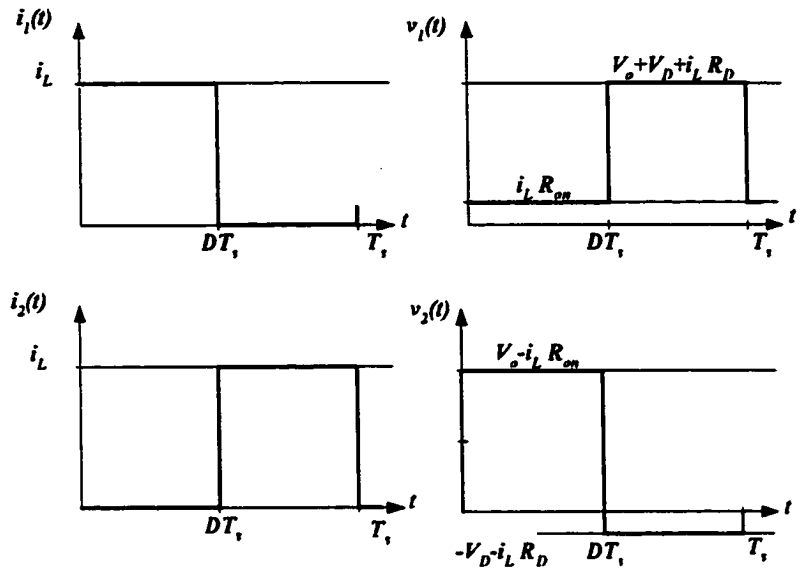


Figure 3.2: Waveforms for Erikson two-port network

From the above waveforms, each terminal quantity can be averaged. These average expressions can then be rearranged and related to one another forming an average model as shown below.

$$i_1(t)_{Average} = D \cdot i_L \tag{3.1}$$

$$i_2(t)_{Average} = (1-D) \cdot i_L \tag{3.2}$$

$$v_1(t)_{Average} = D \cdot R_{on} \cdot i_L + (1-D) \cdot (V_o + i_L \cdot R_D + V_D) \tag{3.3}$$

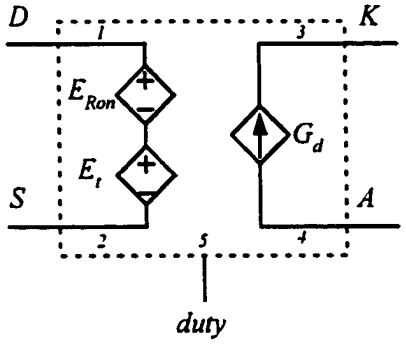
$$v_1(t)_{Average} + v_2(t)_{Average} = V_o \tag{3.4}$$

Relating one average terminal parameter to another while removing references external to the cell we have.

$$i_2(t)_{Average} = \frac{(1-D)}{D} \cdot i_1(t)_{Average} \tag{3.5}$$

$$v_1(t)_{Average} = \frac{i_1(t)_{Average} \cdot R_{on}}{D} + \frac{(1-D) \cdot R_D \cdot i_1(t)_{Average}}{D^2} + \frac{(1-D)}{D} \cdot (v_2(t)_{Average} + V_D) \tag{3.6}$$

We now have the equations necessary to produce the average model in PSPICE as shown in Figure 3.3.




```
**************************************************
******
* MODEL: ccm2
* Application: two-switch PWM converters, includes
*conduction losses due to Ron, VD, Rd
* Limitations: CCM only, no transformer
**************************************************
******
* Parameters:
*     Ron=transistor on resistance
*     VD=diode forward voltage drop (constant)
*     RD=diode on resistance
**************************************************
******
* Nodes:
* 1: transistor+ (D)
* 2: transistor- (S)
* 3: diode cathode (K)
* 4: diode anode (A)
* 5: duty ratio (duty)
**************************************************
******
.subckt ccm2 1 2 3 4 5
+params: Ron=0 VD=0 Rd=0
```

Figure 3.3: Erikson PSPICE Model-CCM with losses

To investigate the model's accuracy, simulations will be performed to compare losses predicted by the model to the losses generated by the actual circuit. To further understanding, the lossless boost model developed in Chapter 2 will also be used as a point of reference. Since the assumption of ripple-free inductor current is used in the development of the conduction loss model for CCM, the test circuit will be intentionally designed to have an insignificant current ripple. The modeled circuit is shown in Figure 3.4. The plot of actual inductor current and capacitor voltage is shown in Figure 3.5. The plot of inductor current shows that the test circuit has a relatively small current ripple. Further, the converter's load is intentionally made very large to exaggerate losses. After all the simulation plots are presented, a table allowing a case by case comparison will be shown.

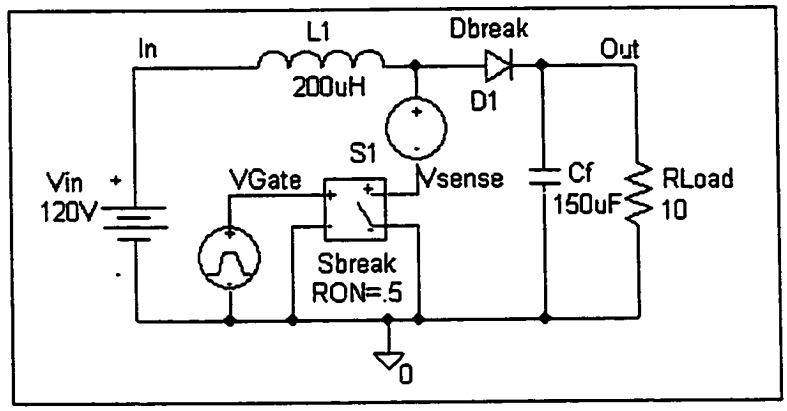


Figure 3.4: Actual Boost with non-ideal components

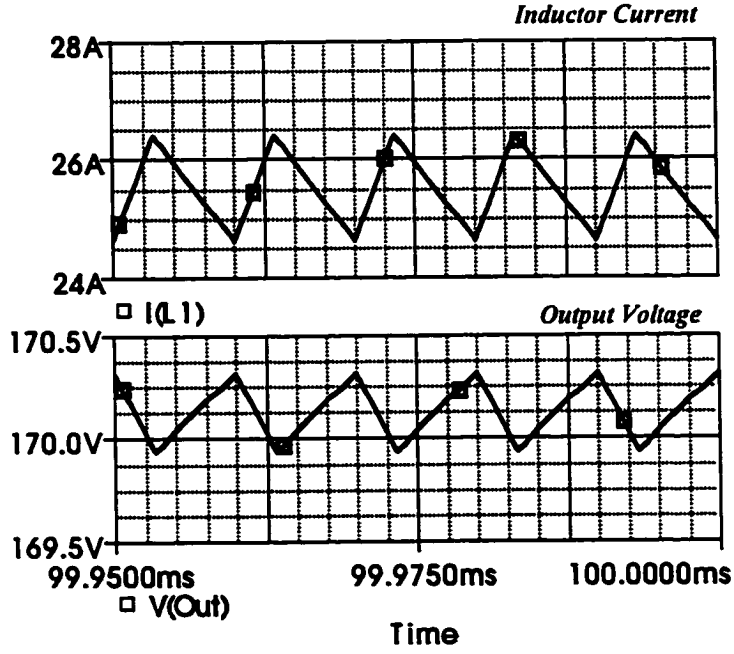


Figure 3.5: Actual Boost waveforms-i (t) top and $v_o(t)$ bottom

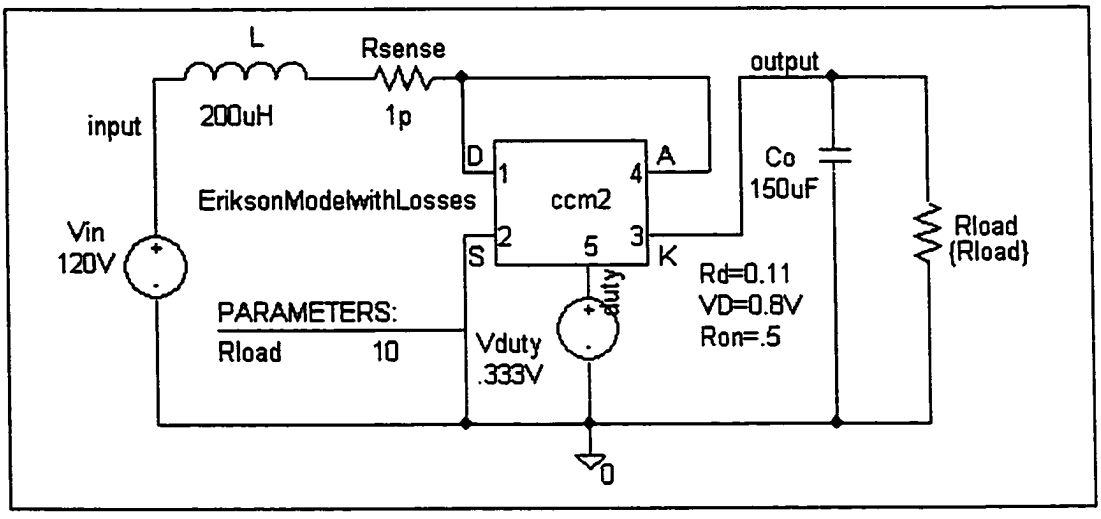
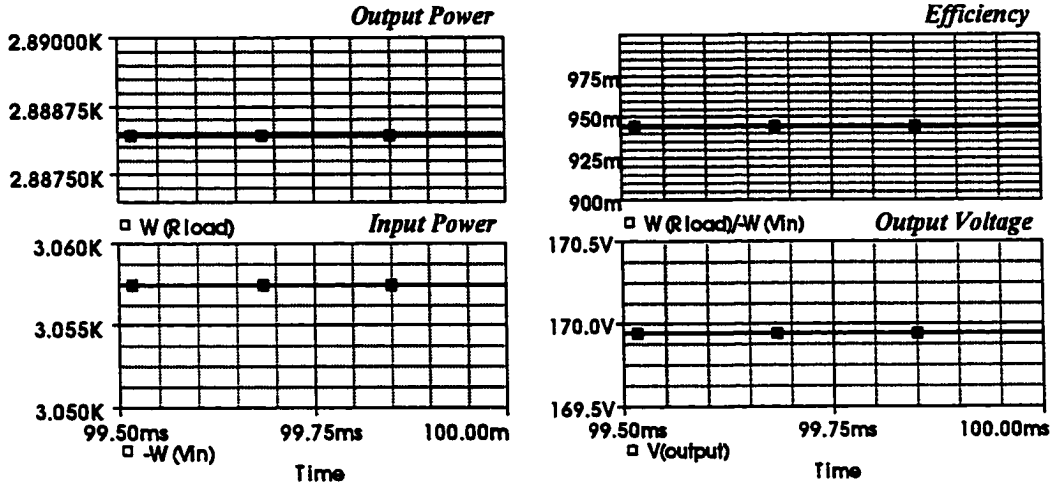


Figure 3.6: Erikson loss-based, CCM model

The parameters for R and V are set so as to match the default diode model in PSPICE, DBreak. Simulation results are presented in the plot below showing average input power, output power, efficiency, and output voltage respectively.



(a) (b)

Figure 3.7: Power balance and output for Erikson model (a) P_{in} (top) P_{out} (bottom) (b) efficiency (top) V_o (bottom)

The same boost converter is produced using the lossless model developed in Chapter 2. The simulated circuit is shown as Figure 3.8. Note that switch and diode conduction losses are not considered in this model and, with the exception of the sense resistance, is totally ideal. It is totally ideal because each of the components are lossless and the averaging waveforms used to develop the model of Figure 3.8 did not account for any nonidealities. The use of this model is the comparison is to evaluate the magnitude of error involved with the ideal model when losses are considered.

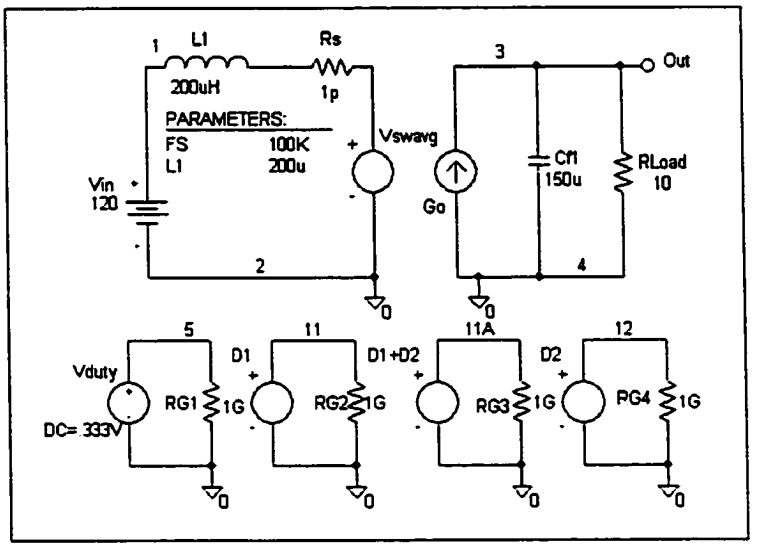


Figure 3.8: Lossless boost model

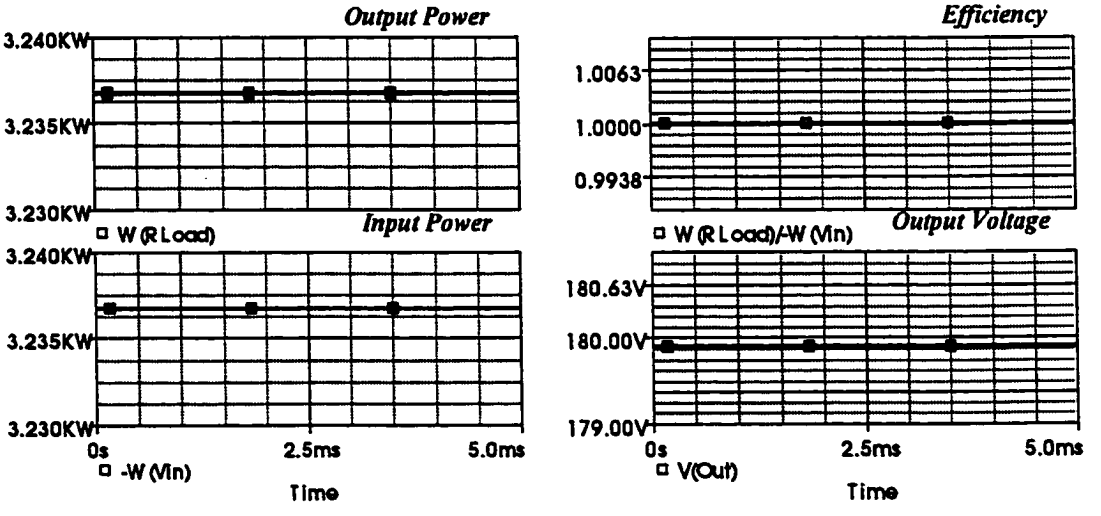


Figure 3.9: Power balance and output for lossless boost model (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

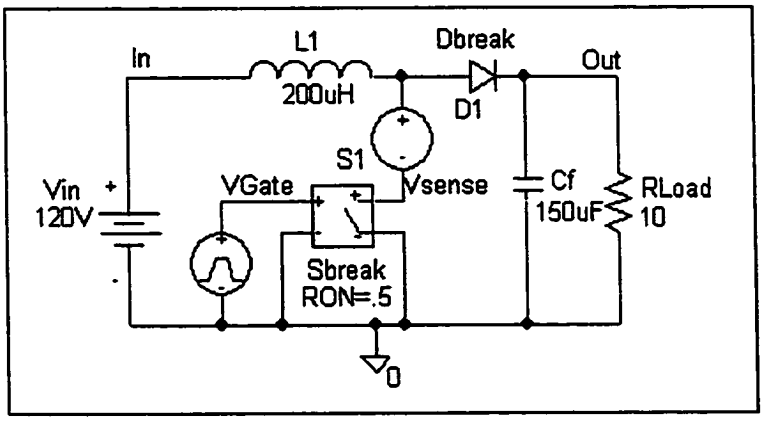
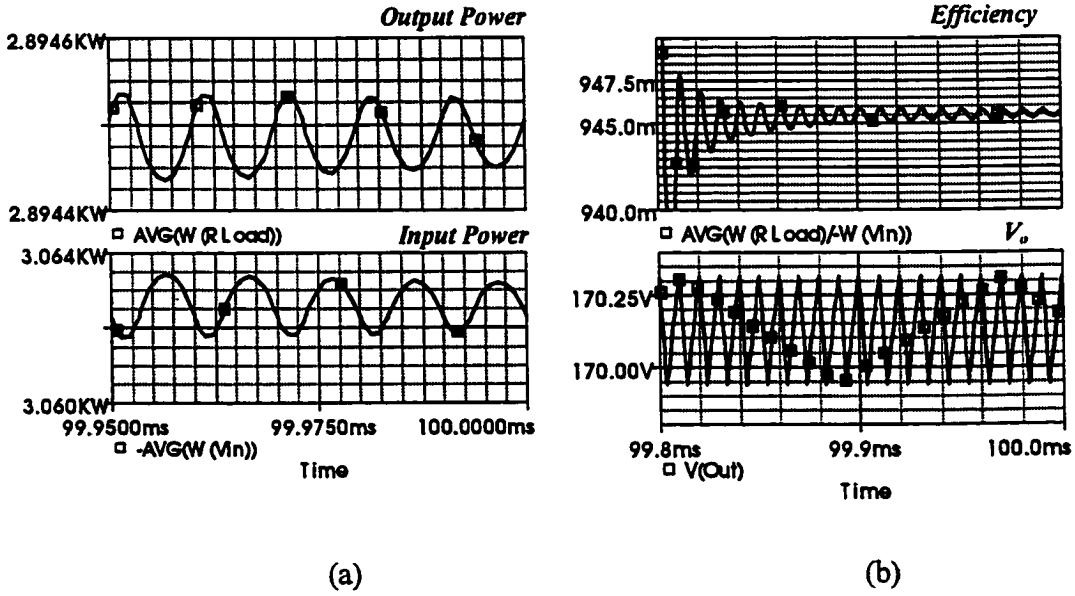


Figure 3.10: Actual circuit used for comparison simulation



(a) (b)

Figure 3.11: Power balance and output for actual circuit (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

A results comparison is shown in Table 3.1.

Table 3.1: Loss comparison

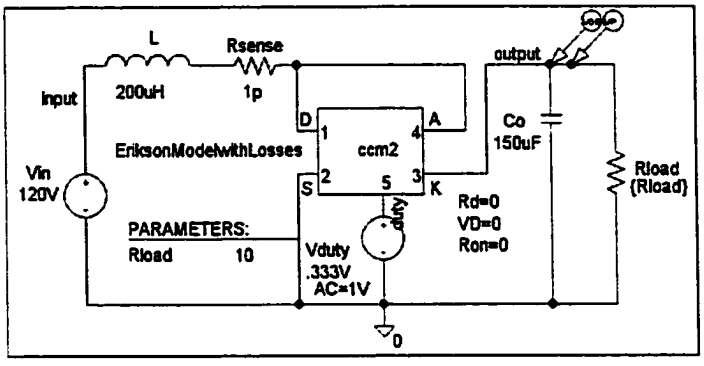
Model	P_{input}	P_{output}	η	V_o
Erikson Loss Model (CCM2)	3058W	2889W	94.5%	169.9V
Proposed Lossless Model*	3237W	3237W	100%	179.9V
Actual Circuit	3063W	2895W	94.6%	170.1V

* In Section 3.3 losses will be included

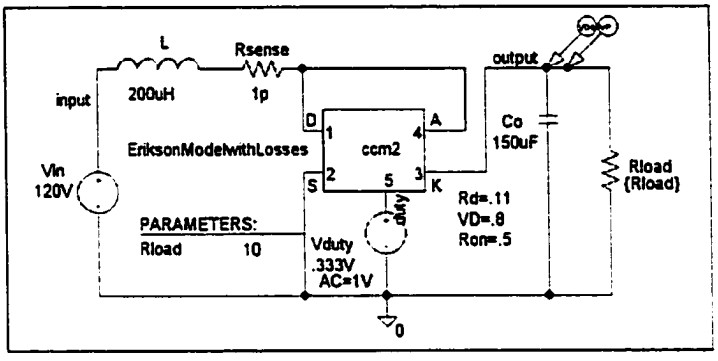
Comparing the energy transfer characteristics, it can be seen that for negligible inductor current ripple, the conduction loss model is very good showing only a -0.1% variance from the actual circuit. However, the lossless model shows significant error, for P_{in} , a +5.7% variance, for P_o , a 11.8% variance, an increase of 5.4 percentage points in efficiency, and an increase in output voltage of 5.8%. Clearly, the lossless model has significant accuracy problems when actual circuit losses are considered. However, for small inductor current ripple, the CCM conduction loss model quite accurate.

So the previous development outlines the energy transfer characteristics of loss-based and lossless models versus the actual circuit. Transient response characteristics are also a subject of this work and will now be investigated. The small-signal characteristic curve control-to-output for the loss-based model, the loss-based model with losses set to zero, and the lossless model produced in Chapter 2 are produced from the schematics shown as Figure 3.12 where the schematics are (a) Erikson loss-based model with losses set to zero

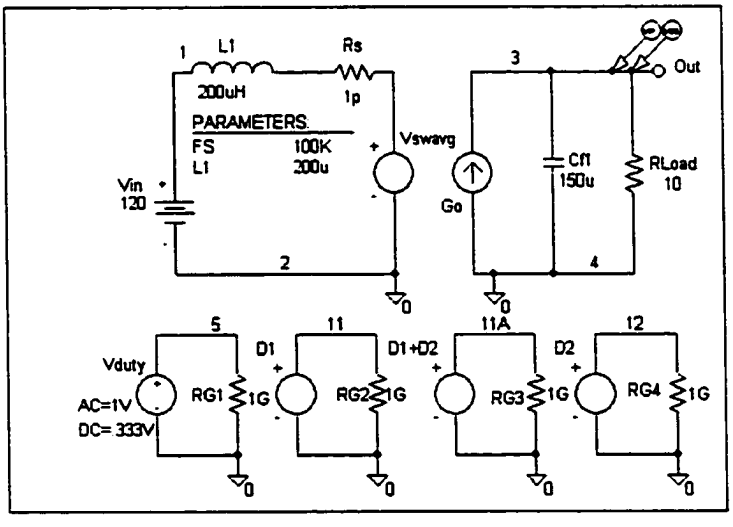
(b) Erikson loss-based model with switch and diode losses included and (c) ideal model developed in Chapter 2. The results are superimposed on one another and are shown in Figure 3.13. Note that the inclusion of losses does have an effect of the small-signal results of the converter. This effect is most noticeable on the magnitude plot yet some deformation of the phase response is also present. Figure 3.13 shows that the results of Figure 3.12 (a) and (c) show identical results as expected. However, the loss-based model of Figure 3.12 (b) shows the effect of the nonidealites included.



(a)



(b)



(c)

Figure 3.12: Schematics for small-signal curves (a) Erikson lossless (b) Erikson with diode and switch loss (c) Proposed model lossless

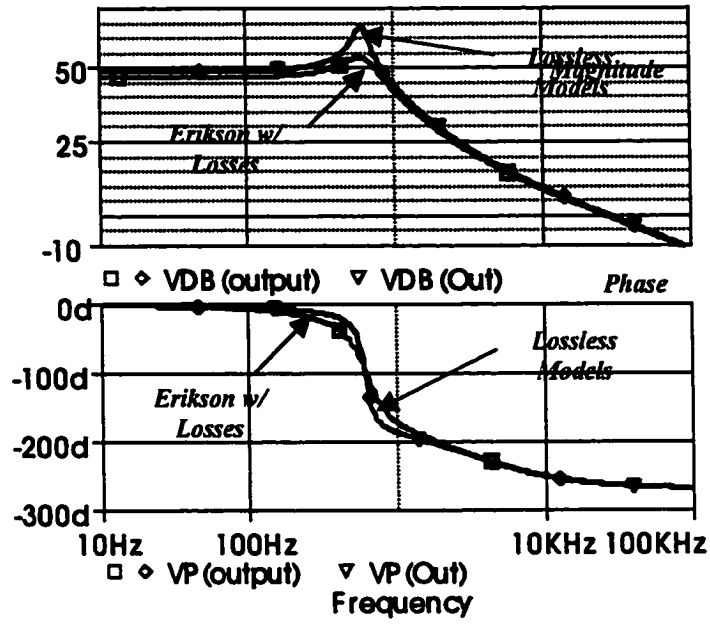


Figure 3.13: Small-signal curves superimposed

From the results of Figure 3.13, we would then expect a different transient response under closed loop simulation when losses are included.

Now it would be of interest to run this same test again choosing a circuit design that exhibits extreme inductor current ripple but stays in CCM operation. We would expect that the accuracy of the loss model will sharply decline with increasing current ripple.

For this new test the same converter will be used but the load and inductance will be decreased to worsen the ripple. Figure 3.14 shows the new design with the inductor value

reduced to 50 μH and the load resistance increased to 50 Ω. This design presents a high inductor current ripple yet remains in CCM operation as demonstrated in Figure 3.15.

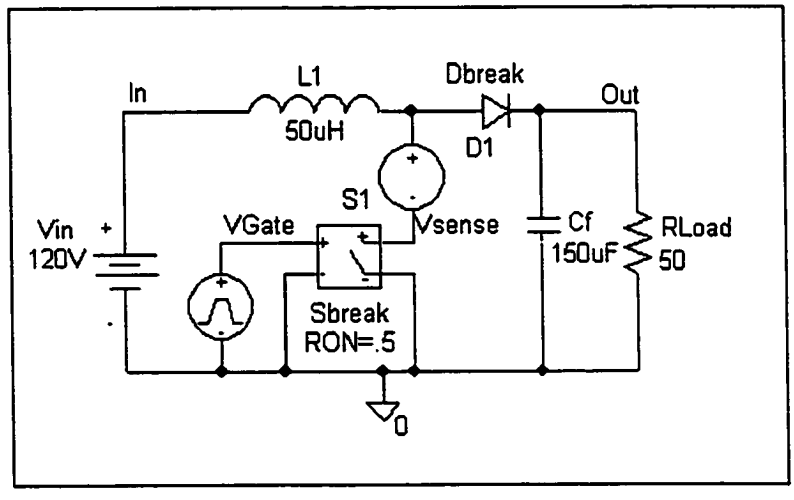


Figure 3.14: Actual circuit with high ripple

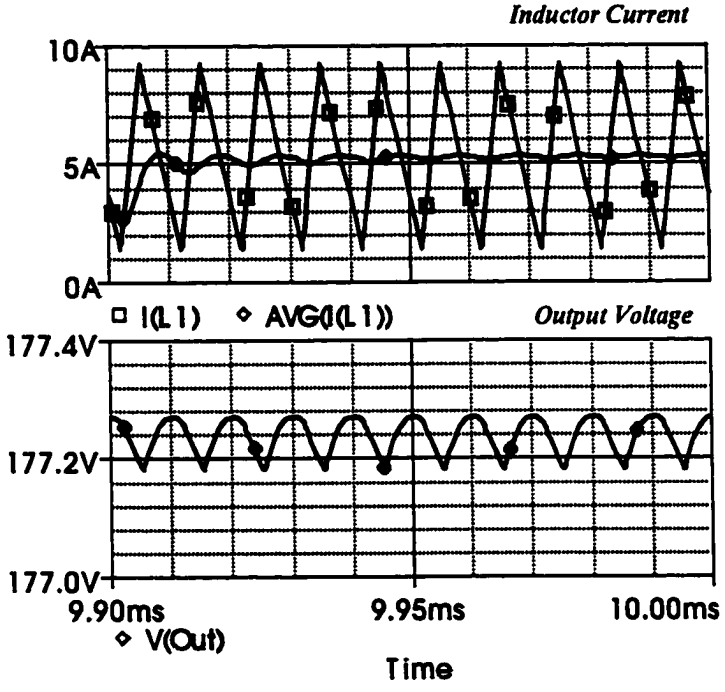
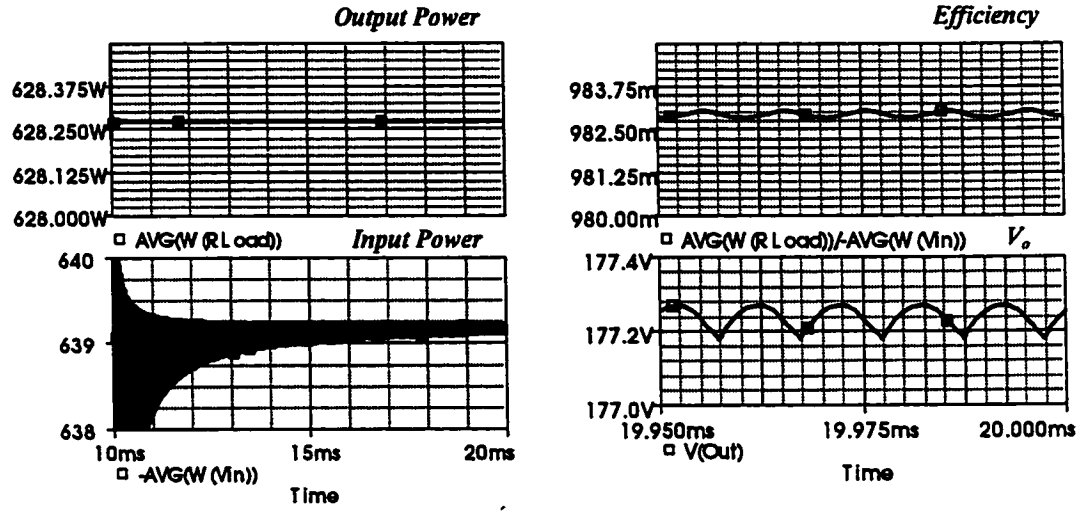


Figure 3.15: Actual circuit waveforms for high ripple case- i *(t)* top and $v_o(t)$ bottom

Because of the lighter load, conduction losses are significantly less as expected and efficiency has gone up as shown in Figure 3.16 with efficiency at 98.3%.



(a) (b)

Figure 3.16: Power balance and output voltage for high ripple case (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

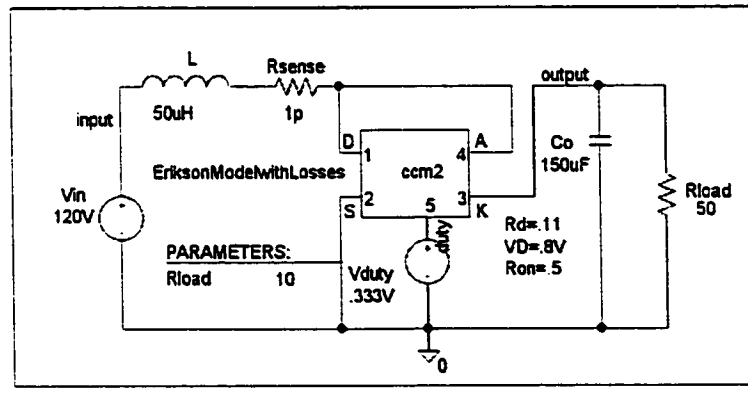


Figure 3.17: Erikson model for high ripple case

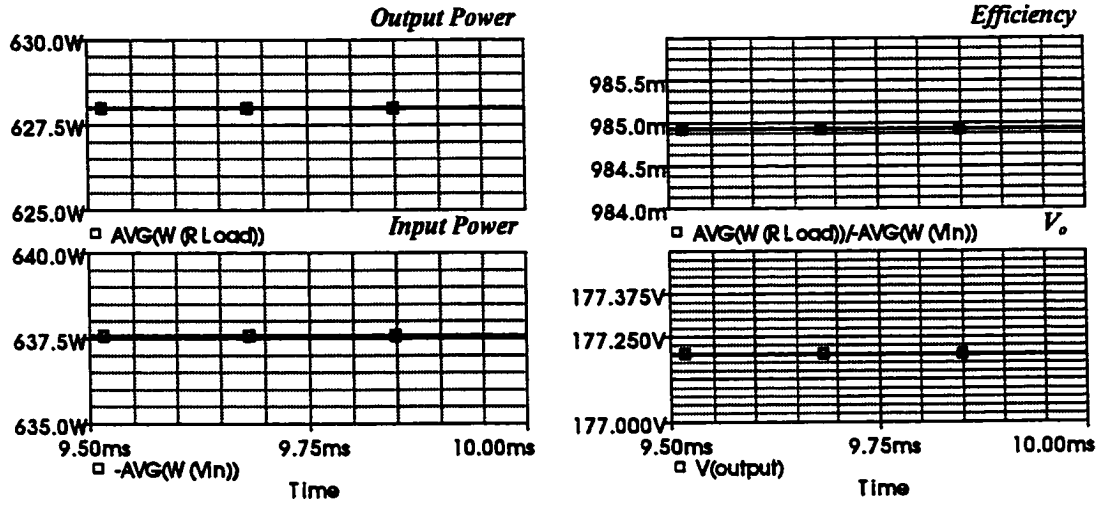


Figure 3.18: Power balance and output voltage for high ripple using Erikson model (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

From Figure 3.18 can see that the accuracy of the model is still quite good with a .1% variance in efficiency as compared to the actual circuit simulation. Figure 3.19 is the lossless model of Chapter 2 at the new design operating point. It is once again included to serve as a reference when evaluating the effect of nonidealities on model accuracy. As expected the results in Figure 3.20 show 100% efficiency and it is interesting to note the shift in input/output power.

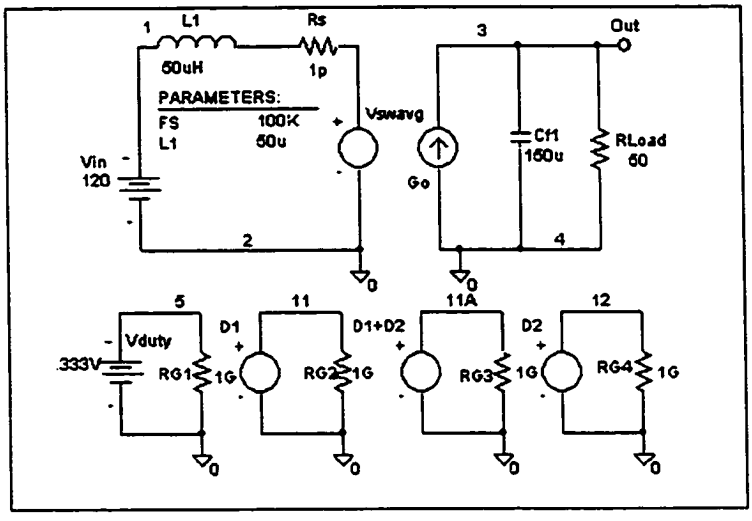


Figure 3.19: Lossless boost model for high ripple CCM case

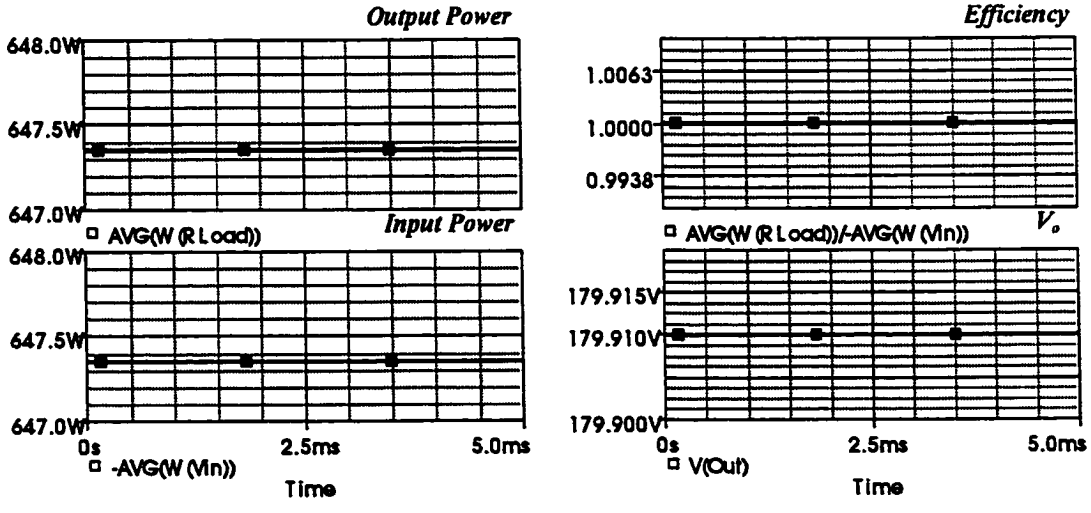


Figure 3.20: Power balance and output voltage for high ripple using lossless model (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

Table 3.2 the simulation results for moderate inductor current ripple summarized. Overall, we see a slight decease in the Erikson model's accuracy. This is expected to decrease further as inductor current ripple increases.

Table 3.2: Comparison of high ripple case

Model	P_{input}	P_{output}	η	V_o
Erikson Loss Model (CCM2-High Ripple)	638W	628W	98.5%	177.2V
Actual Circuit (High Ripple)	639W	628W	98.3%	177.2V
Proposed Lossless Model	647W	647W	100%	179.9V

From the data, surprisingly, the model does yield good results for a wide range of CCM operation, even when inductor current ripple is relatively large. However, the model's derivation assumes CCM operation and cannot be applied to DCM operation. Further, even if the model did account for DCM operation, then it should be expected that small inductor current ripple assumption would be invalid since, in DCM, ripple is large. The conclusion being that while this approach is suitable for CCM operation, it is clearly not applicable to DCM. Therefore, a new method of addressing conduction losses for DCM must be developed. Inductor current ripple in the extreme case, DCM, very significant. The next simulation will evaluate the accuracy of the model when used in a DCM application.

3.3 Conduction Losses in DCM-Energy Equivalence

Recently, a colleague here at UCF has developed a concept for treatment of conduction losses in DCM based on energy equivalence [30]. In [30], preliminary discussion and simulation show promising results. In this section, this DCM loss concept will be more thoroughly examined and be applied to the unified modeling approach presented in this dissertation.

This issue was considered in the past only with the assumption that the inductor current ripple is negligible. Conduction losses have been addressed when the converter operated in continuous conduction mode (CCM) and under a small ripple assumption. However, accuracy of the model decreases with the increasing of inductor current ripple with respect to its average value as seen in the previous simulation.

A PWM switch model is developed here that uses equivalent resistors to maintain the same losses when compared to the actual circuit. Derivation of the model is based on the energy conservation principle. The resulting model will address large inductor current ripple.

In the following discussion, the diode is considered a constant voltage V_d in series with a linear on-resistor, r_d, when conducting, inductor has an equivalent series resistor, r, and the active switch has an on-resistance of r_d.

A basic problem in analyzing dc-dc converters with non-ideal components is that the inductor current will not be a triangular waveform as was considered in lossless converters. For converters operating in DCM, current rises and falls exponentially with an average

value of I' instead of I when ideal components are assumed, as shown in Figure 3.21. This difference in average values is determined by the time constants in charging and discharging of the inductor. As a first step, we assume that these time constants are much greater than the charging, dT, and discharging time $(1-d)T$ of the inductor, i.e.:

$$\frac{L}{r_{on}+r_L} >> dT_s, \quad \frac{L}{r_d+r_L} >> (1-d)T_s \tag{3.7}$$

$$\frac{v_{dis}}{r_d+r_L} >> I'_{max} \tag{3.8}$$

where v_{di} denotes the voltage applied to the first order L-R circuit to discharge the inductor.

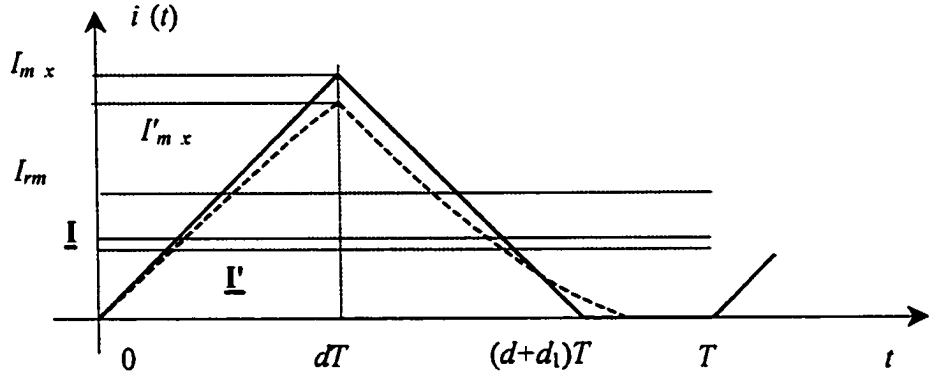


Figure 3.21: Inductor current with ideal (solid line) and non-ideal (dashed line) components

Under these conditions, although the difference between actual and ideal inductor current waveforms is small energy lost on these nonideal components does have a measurable affect on converter performance.

In an average model, inductor current is the average value over each switching cycle in the actual circuit. This current generates energy losses on the parasitic resistors, which should be calculated by the RMS value of the current in the actual circuit. However, the actual current, and hence its RMS value, is unavailable in the average model. As qualitatively shown in Figure 3.21, the RMS value is clearly larger than the average value. To correctly model energy losses on the parasitic resistors in PWM converters, the energy loss in the average model must be the same as in the actual switching converter. As a result, the RMS and average values of the inductor current as shown in Figure 3.21 are first determined and they are given below:

$$I_{rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_L^2(t)dt} = \sqrt{\frac{d+d_1}{3}} I_{max} \tag{3.9}$$

$$I = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt = \frac{1}{2}(d+d_1)I_{max} \tag{3.10}$$

The energy dissipated on the ESR of the inductor over one switching period is given by Equation (3.11):

$$W_{rL} = I_{rms}^2 r_L T_s = \frac{1}{3}(d + d_1) I_{max}^2 r_L T_s \tag{3.11}$$

where $I_{m\ x}$ is shown in Figure 3.21

Assuming equal energy loss, the same amount of energy should also be dissipated in the averaged model based on the average current. This implies that the ESR of the inductor should be replaced by an equivalent resistor to accommodate the difference between the *rms* and *average* values of the inductor current, i.e.,

$$W_{rL} = I^2 r_L' T_s = \frac{1}{4}(d + d_1)^2 I_{max}^2 r_L' T_s \tag{3.12}$$

where r_L' is equivalent ESR of the inductor in the averaged model.

From Equations. (3.11) and (3.12) it is easy to obtain the following equivalent.

$$r_L' = \frac{4}{3}\frac{r_L}{d + d_1} \tag{3.13}$$

Equation (3.13) suggests that the ESR of the inductor be replaced by a larger resistor in the averaged model. It is also noted that in the denominator, $(d+d_1)$ is the relative duration of the inductor current in each switch cycle within which this current is greater than zero. This equivalent resistance depends on control duty cycle and circuit parameters.

To calculate the equivalent on-resistance for the active switch and the passive switch, same procedure described from Equation (3.9) to Equation (3.13) can be followed. However, the result can also be obtained simply by observing that the relative duration of the current

flowing through the active switch is d and that flowing through the passive switch is d_1. Therefore,

$$r_{on}^{'} = \frac{4}{3}\frac{r_{on}}{d}, \quad r_d^{'} = \frac{4}{3}\frac{r_d}{d_1} \tag{3.14}$$

where $r_{on}^{'}, r_d^{'}$ is equivalent on-resistances of the active switch and the diode in the averaged model, respectively.

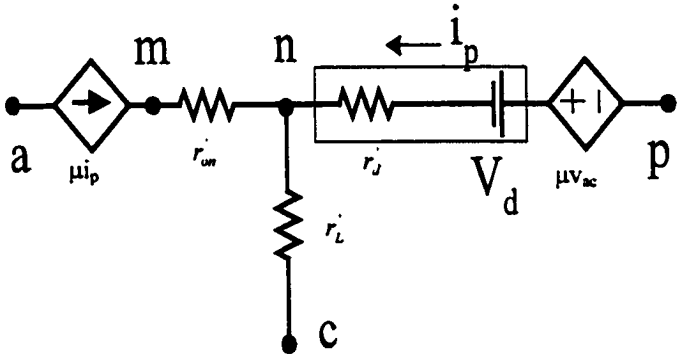


Figure 3.22: DCM PWM switch circuit model with conduction losses

$$\mu = \frac{d^2 T_s}{2L}\frac{v_{ac}}{i_p}, \quad d_1 = \frac{d}{\mu} \tag{3.15}$$

The non-ideal PWM switch model shown in Figure 3.22 can be readily implemented in PSPICE. Its PSPICE netlist is given in Figure 3.23. Note that in the netlist, the controlled voltage source *evdrd* denotes the voltage across the conducting diode. The direction of the

diode forward voltage drop V_d depends on the direction of current *i*(*vxy*) (*i* in Figure 3.22). For the boost converter, this current is negative and therefore the controlled voltage source *evdrd* should take this into account.

Another phenomenon about the equivalent resistors, Equation (3.14), is that although their dependency on control duty ratio is somewhat different, the voltages across them turn out to have the same expressions as given below:

$$v_r = \frac{4}{3}\frac{\mu i_p}{d} r \tag{3.16}$$

where *r* denotes the ESR of the inductor or on-resistances of the switches. This relation has been used in the netlist to describe the controlled voltage sources *evdrd*, *ers* and *erl*.

```
*Large signal discontinuous conduction voltage mode *model (including ESR of the inductor, on-
resistance of *switches and diode voltage drop)
* Params: Rmphite→External ramp height, Valleyv→ *Valley voltage of external ramp
*LFIL→Filter inductance, FS→Operating frequency
*rs→on-resistance of the active switch, rd→on-resistance *of the diode, rL→ESR of the inductor
*Vd→diode forward voltage drop
*Pins: active (A), passive (P), common (C), control voltage (Vc)
.subckt LOSSY_LSDCM A P C Vc  Params: +RMPHITE=2 VALLEYV=1 FS=50k LFIL=500u
RL=0 +RS=0 RD=0 VD=0
emod    d       0   table {(v(vc)-VALLEYV)/RMPHITE} +
remod   d       0   1g
etbl    anum    0   value={2*LFIL*FS*i(vxy)}
ranum   anum    0   1g
emew    mew     0   value={v(d)*v(d)*v(a,n)/v(anum)}
gac     a       m   value={v(mew)*i(vxy)}
ecp     x       p   value={v(mew)* (v(a,m)+v(n,c))}
rmew    mew     0   1g
vxy     x       y   0
ers     m       n   value={v(mew)*i(vxy)*4*rs/3/v(d)}
evdrd   y       n   value={i(vxy)*4*rd*v(mew)/3/v(d)+
+                       Vd*SGN(i(vxy))}
erl     n       c   value={v(mew)*i(vxy)*4*rL/3/v(d)}
.ends
```

Figure 3.23: PSPICE DCM conduction loss model

Having presented the loss modeling concept, simulations will be performed to validate the theory. A boost converter operating well into DCM will be used to test model validity and is shown as Figure 3.24 which includes the diode, switch, and inductor conduction loss models. From Figure 3.25, it is clear the converter is operating well into DCM with high inductor current ripple.

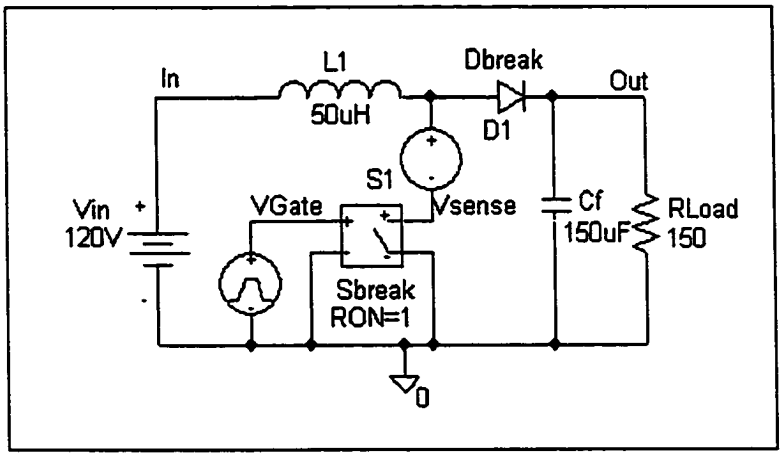


Figure 3.24: Actual boost circuit with losses operating in DCM

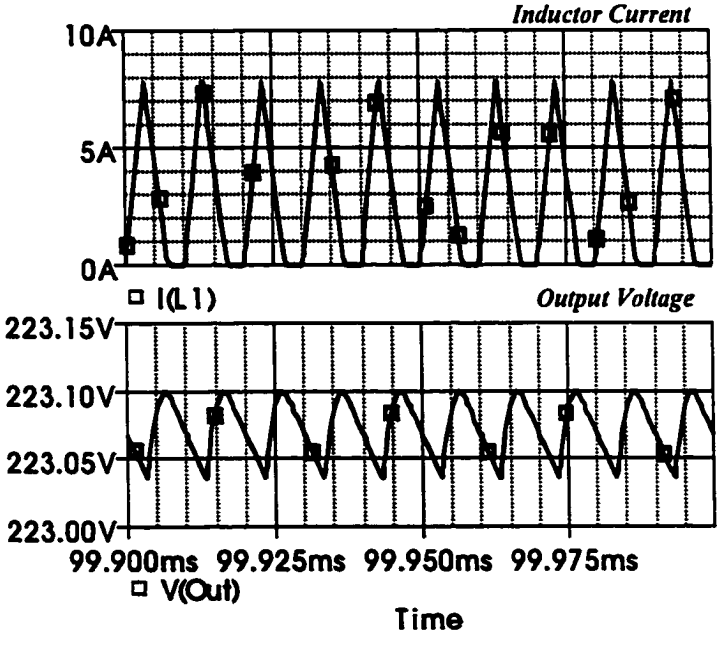
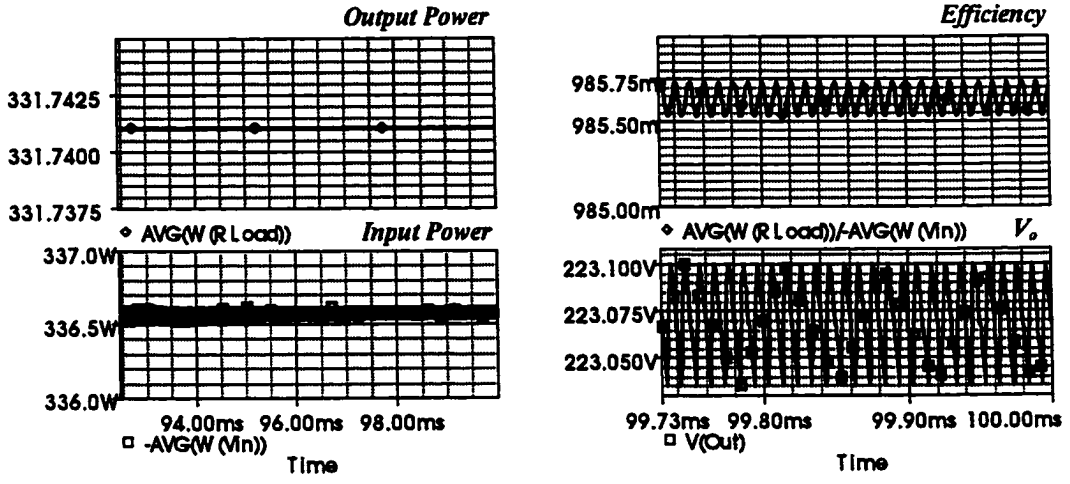


Figure 3.25: Actual circuit waveforms for DCM- $i\ (t)$ top and $v_o(t)$ bottom



(a) (b)

Figure 3.26: Power balance and output voltage for the actual circuit (DCM) (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

To drive the design of Figure 3.24 into DCM, the load is decreased significantly. This decrease results in a higher efficiency as shown in Figure 3.26 (b).

Now for the same operating conditions, we test the DCM loss model presented in [30] by comparison to actual circuit losses. The derived model uses the energy equivalence principle described above with its netlist model given in Figure 3.23. The equivalent DCM circuit model is shown in Figure 3.27. Figure 3.28 shows the simulation results of the model of Figure 3.27.

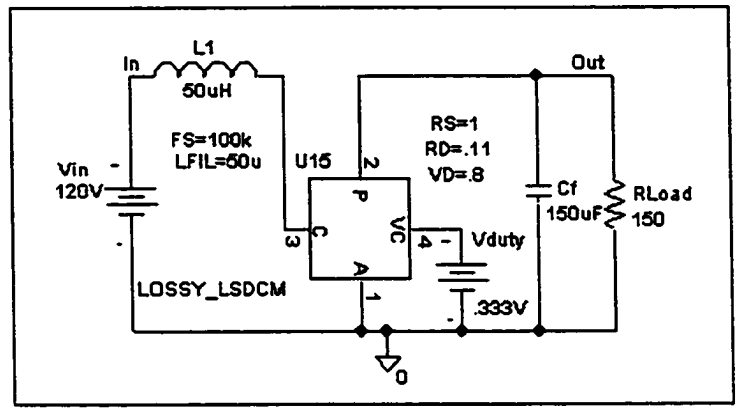
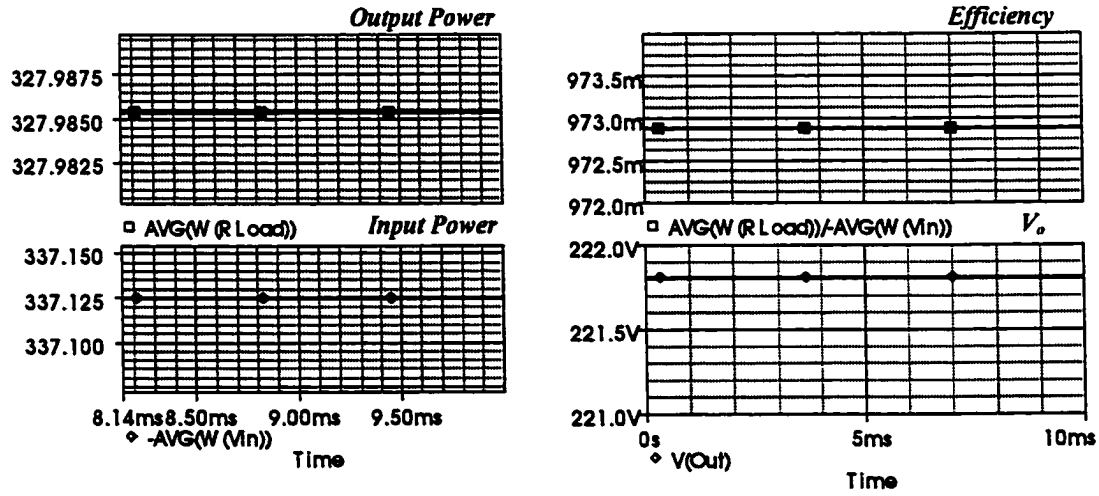


Figure 3.27: DCM conduction loss model



(a) (b)

Figure 3.28: Power balance and output voltage for DCM conduction loss model (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

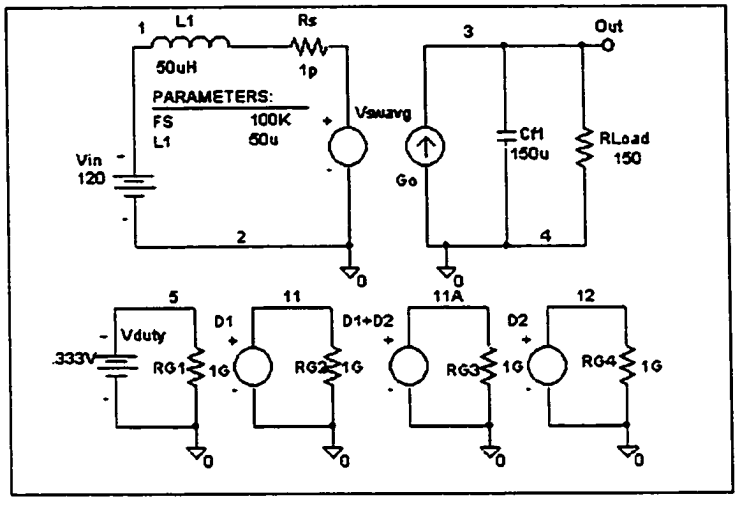
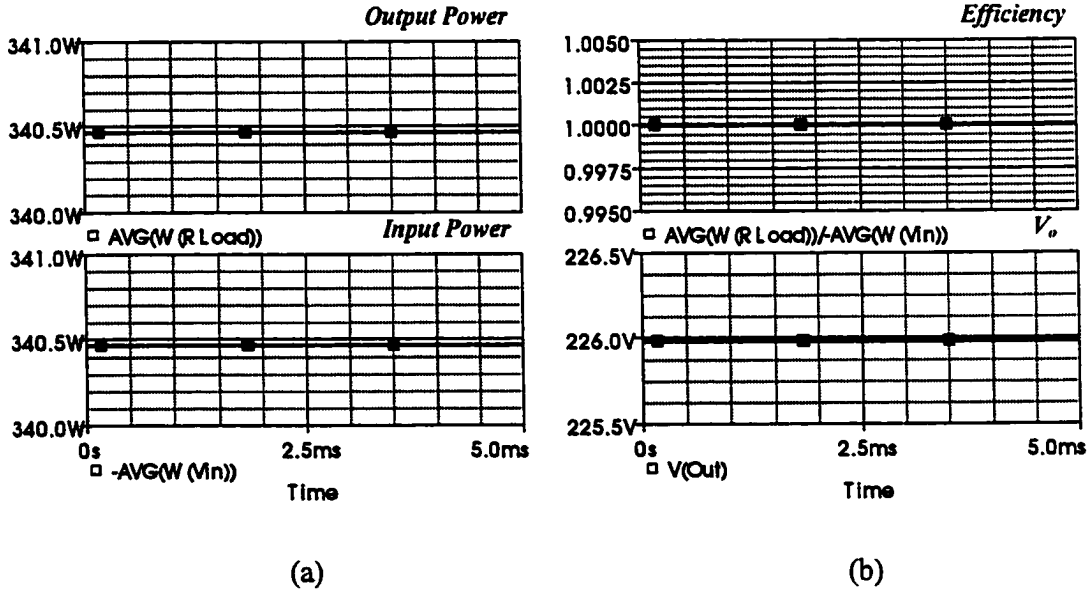


Figure 3.29: Lossless boost model in DCM



(a) (b)

Figure 3.30: Power balance and output voltage for DCM lossless model (a) P_{in} (top) P_o (bottom) (b) efficiency (top) V_o (bottom)

Figure 3.29 represents the lossless model of Chapter 2 operated at the DCM operating point of Figure 3.24. This circuit is, once again, used as a reference comparison to the nonideal simulation.

The results are compared in Table 3.3 where we see the DCM conduction loss model tracks the actual circuit losses but with less accuracy than the CCM model. Several factors are contributing to the reduced accuracy including the effect of the on resistance of the output diode which is estimated here and used for all operating points. Table 3.3 shows near perfect agreement on the input side between the actual circuit simulation and the loss-based, DCM model but the output voltage drop creates a difference in the output powers. Overall efficiency varies by 1.3%, with the DCM loss model over estimating conduction losses.

Table 3.3: DCM conduction loss comparison

Model	P_{input}	P_{output}	η	V_o
DCM Conduction Loss Model (Fig.3.29)	337W	328W	97.3%	221.8V
Actual Circuit (Fig. 3.26)	337W	332W	98.6%	223.1V
Lossless model in DCM (Fig. 3.31)	340.5W	340.5W	100%	226V

In the next section, loss modeling is applied the unified approach. The emphasis being to incorporate and refine the DCM model to improve accuracy. The CCM model presented

does remarkably well in circuits with both low and moderate ripple and as such will not be further refined.

3.4 Conduction Loss Modeling Implemented in the Unified Modeling Approach

The DCM conduction loss model presented in [30] and evaluated in the previous section presents an innovative way to incorporate conduction loss modeling in the unified approach. Preliminary simulation results show a significant improvement in accuracy when nonideal components are considered. In this section, this model refinement will be incorporated into the unified approach and the analysis will be moved from the top-level input/output relationships to component level loss evaluation.

In the PWM switch model presented in Figure 3.22, equivalent, variable resistances are placed in the branches of the circuit where conduction losses are present. For example, the passive diode branch contains its model, the active switch branch contains the variable on-state switch resistance, etc. In the unified approach, the derived model may or may not contain circuit branches with one-to-one correspondence to the branches of the actual circuit. For example, in the boost model of Figure 3.29, the branch containing the active switch is not present and the average switch current is not directly available in the model. This presents an obstacle, as the equivalent resistance of the switch needs to be placed in the branch that represents average switch current. This presents no problem for the diode model or the equivalent series resistance of the inductor as those branches do appear in the

same place in the model of Figure 3.29. Therefore, special consideration must be given to the inclusion of the switch conduction loss model into the average model of Figure 3.29.

To overcome this obstacle we revisit the derivation of the model and note the effects of the nonidealalities on the instantaneous waveforms. Figure 3.31 shows the boost DCM waveforms when r_{ds} and diode nonidealalities are considered and approximated as straightlines. A comparison to the ideal model development, Figure 2.7, reveals several key differences. These differences include:

1. A shift in steady state operating point as denoted by the primes on each duty ratio, peak current, etc.
2. A non-zero value for v_{sw} during Mode I due to r_{ds}.
3. The diodes effect on v_{sw} during Mode II.

It is important to point out that although these resistances cause exponential charging and discharging of the reactive components, the straight-line approximation is used based on the rationale of section 3.3 and Equations (3.7) and (3.8).

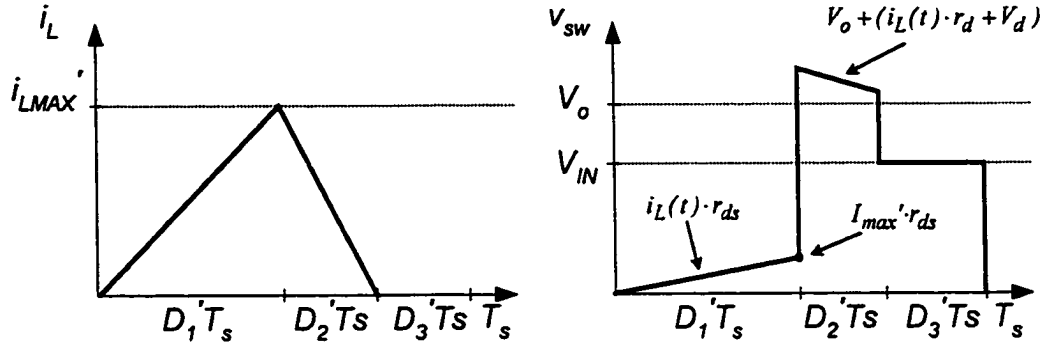


Figure 3.31: Approximated nonideal boost DCM waveforms

The most direct treatment of the conduction losses in the unified approach is include the variable, equivalent resistances from Section 3.3 into the model where the appropriate branch has a one-to-one correspondence with the actual circuit. For the switch conduction loss, because this current is unavailable in the model, it is more appropriate to make some approximation of the actual instantaneous waveforms and rederive the model.

It is important to note that the total effect of the switch resistance is seen during Mode I when v_{sw} is non-zero and is the product of $i_L(t)$ and r_{ds}. Similarly, the total effect of the diode nonidealalities is seen during Mode II where v_{sw} is not strictly V_o as in the ideal circuit but has the addition of the diode forward voltage drop.

To begin, the development will incorporate one nonidealality at a time beginning with the diode losses and then moving onto include the main switch losses in a simple boost

converter. After each loss mechanism is derived and incorporated, simulation tests are performed to evaluate the validity of the model.

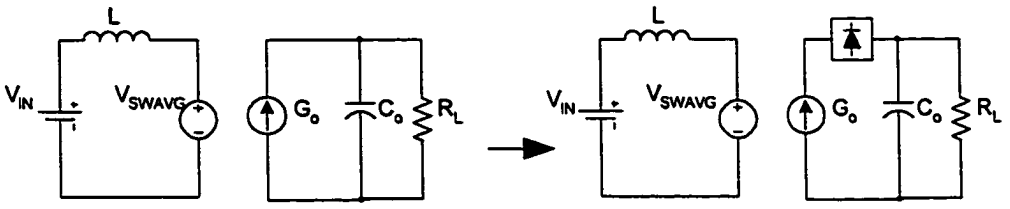


Figure 3.32: Diode loss element location in the boost model

For the diode loss, the approach developed in Section 3.3 will be used as the boost converter's output branch is intact in the average model as shown in Figure 3.32.

In Figure 3.32, the ideal model shown on the left has the average output current available, shown as current source G_o. In the classic boost, the output diode sees the output current such that $I_{oavg}=I_{diodeavg}$. Therefore, this branch in the model carries the same average diode current. Recalling that the equivalent resistance developed in Section 3.3 were designed to predict the correct actual circuit losses when subjected to the smooth, average current value which is less than its RMS value. As such, this equivalent resistance will produce a correct prediction of actual circuit losses when placed in this branch as it is subjected to the average output current.

In addition, the differential voltage impressed across the inductor during Mode II is the difference between the input and output voltage in the ideal, actual circuit during Mode II. The ideal model accounts for this in the expression for V_{swavg} repeated here as Equation (3.17) for convenience.

$$V_{swavg} = V_o \cdot D_2 + V_{in} \cdot D_3 \tag{3.17}$$

In the actual circuit, the presence of the diode modifies and increases the voltage on the right-hand node of the inductor thus decreasing the differential voltage across it. In the model, Equation (3.17) is a function of V_o times the Mode II weighting factor, the duty ratio, D_2. This dependence on the output voltage must be modified to account for the forward voltage drop of the diode. By including the diode loss model in the average model in the location shown in Figure 3.32, the voltage across the current source G_o is increased by the diode model's voltage drop. As such, the voltage across G_o is the appropriate voltage to use in place of V_o in Equation (3.17) when the diode's nonideal effects are considered. While these voltages are the same in the ideal model, it is important to take the voltage across G_o rather than the output voltage in the V_{swavg} expression.

The diode model's effect on Equation (3.17) is then to increase the V_o contribution to the V_{swavg} expression. Since average inductor voltage is zero in steady-state, the value of the V_{swavg} expression is constrained to the input voltage value. This constraint in conjunction with the shift in the value of V_o means the values of the duty ratios in Equation (3.17)

change. This change in operating point is a representation of the effect of losses in the actual circuit.

In order to validate the assertions above, an actual circuit simulation is performed with the nonideal Dbreak model used for the output diode. The actual circuit schematic is shown as Figure 3.33, where the main switch is represented as an instantaneous, voltage controlled switch with on-state resistance removed, thus totally ideal. Further, this series of simulations will be run closed loop to hold output voltage, and hence output power constant.

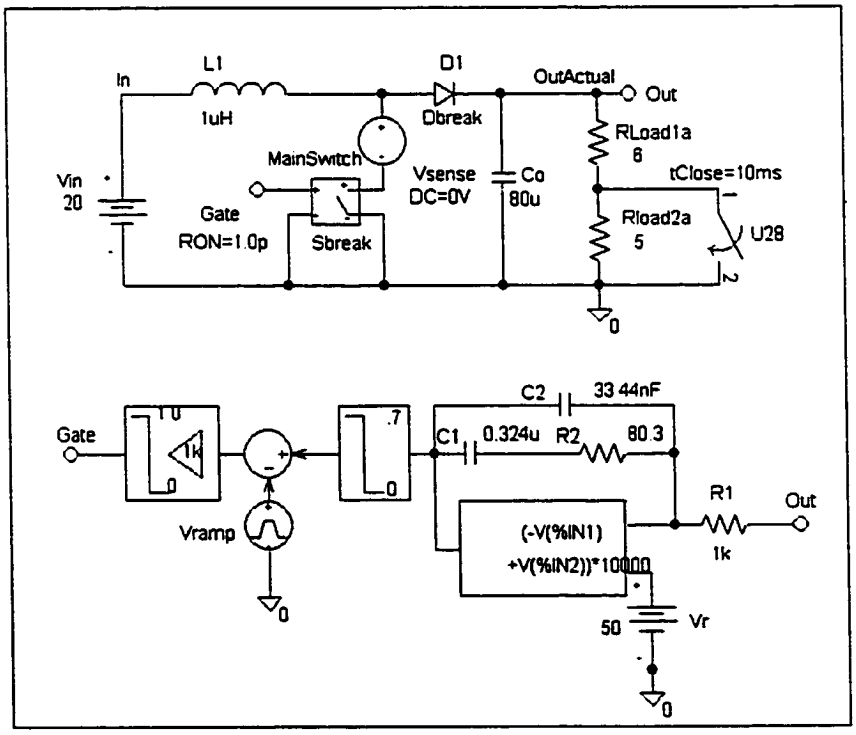


Figure 3.33: Actual boost with Dbreak and ideal switch

Simulation results for the instantaneous waveforms are shown in Figure 3.34 where nonideal effects of the diode can be seen in the switch voltage where the Mode II voltage is the sum of the diode forward voltage drop and the output voltage.

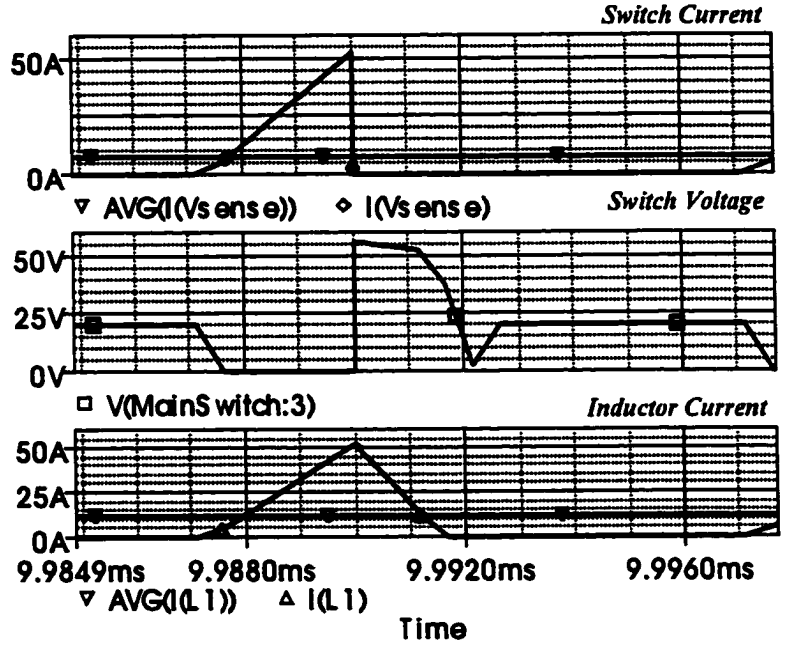


Figure 3.34: Actual boost simulation results: switch current (top), switch voltage (middle), inductor current (bottom)

Power losses are investigated in Figure 3.35 where the diode loss is ≈21.4W and ideal switch losses are effectively zero as expected.

From the simulation results, the assumptions made during the diode loss model development above are valid. To evaluate the modeling approach, the ideal boost average

model is then modified to incorporate the diode loss model as shown in Figure 3.32 and input into a PSPICE schematic as Figure 3.36.

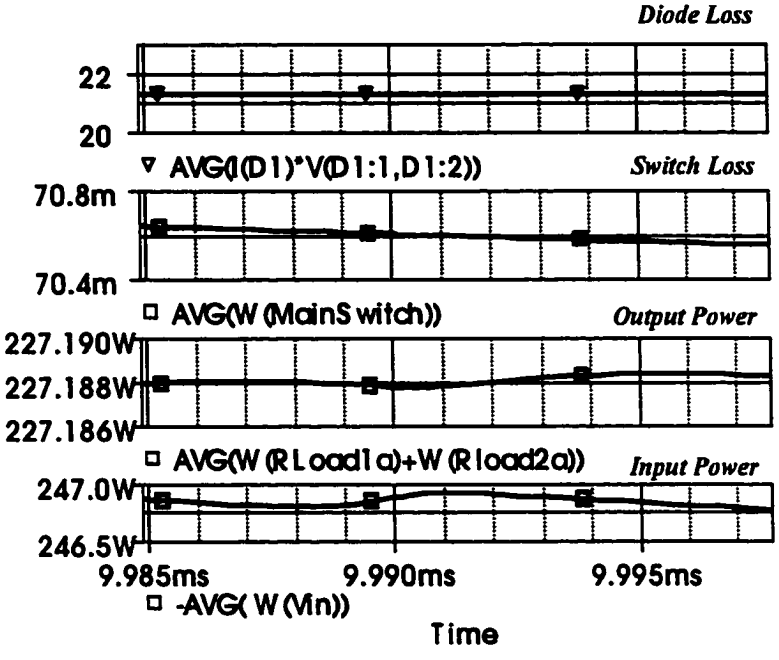


Figure 3.35: Actual boost simulation results: diode loss (top), switch loss ,output power, input power (bottom)

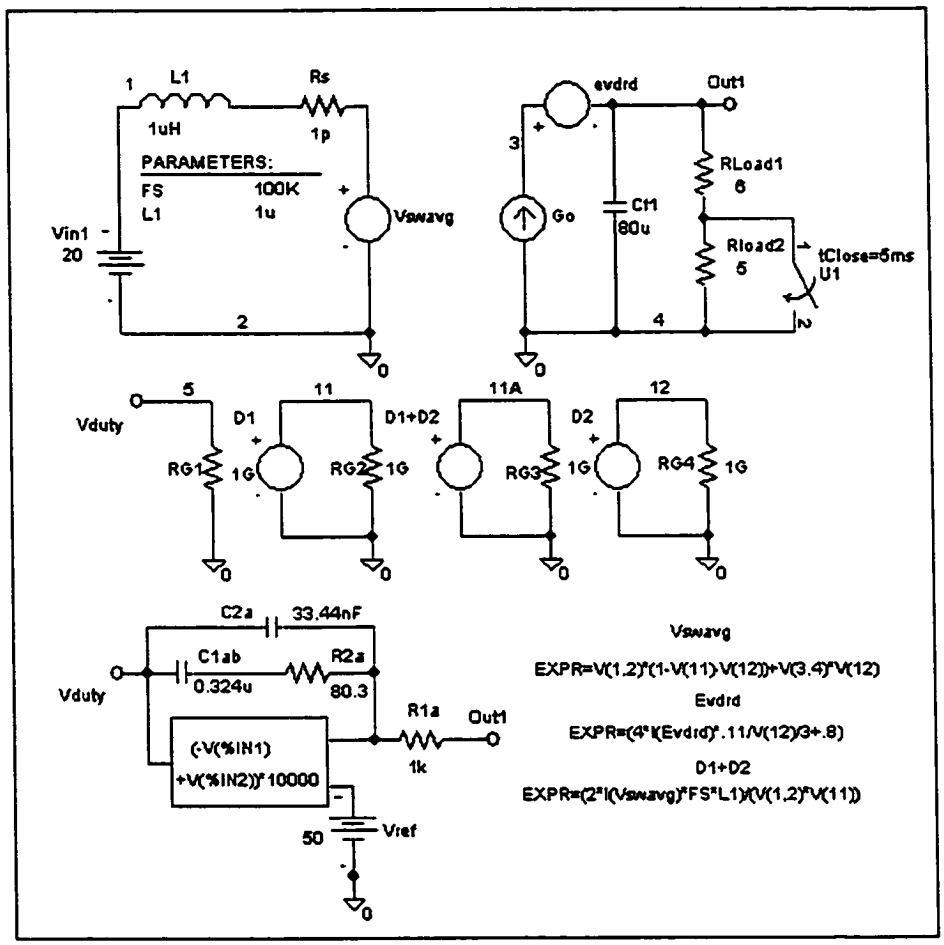


Figure 3.36: Average boost model with diode loss model

Figure 3.36 is a modified version of the ideal boost model derived in Chapter 2 with the exception of the inclusion of the diode loss model. This diode loss model, shown as the *evdrd* source in Figure 3.36, is based on the development of Section 3.3 as displayed in the box in Figure 3.22. In Figure 3.36, the controlling expression for the *evdrd* source uses

model parameters to match the Dbreak model with r_d=.11Ω and V_d=.8V. The expression for the variable resistance is based entirely on the energy equivalence approach developed in Section 3.3.

The equations forming this model are input into MathCAD for solution in Figure 3.37. The expression for V_{od} represents the modified output voltage in the V_{swavg} expression of the model and includes the sum of the diode voltage drop and the output voltage.

$$L := 1\cdot 10^{-6} \qquad R := 11 \qquad F_s := 100\cdot 10^{3}$$

$$V_{in} := 20 \qquad T_s := \frac{1}{F_s} \qquad V_o := 50$$

Given

$$V_{in} - \left(V_{od}\cdot D_2 + V_{in}\cdot D_3\right) \equiv 0$$

$$D_1 + D_2 \equiv \frac{2\cdot I_{Lavg}}{V_{in}\cdot D_1\cdot T_s\cdot\frac{1}{L}} \qquad V_{od} \equiv \left(\frac{4}{3}\cdot\frac{.11}{D_2}\cdot\frac{V_o}{R}\right) + .8 + V_o$$

$$\frac{V_o}{R} \equiv I_{Lavg}\frac{D_2}{D_1 + D_2}$$

$$D_3 \equiv 1 - D_1 - D_2$$

$$\text{Find}\left(D_1, D_2, D_3, I_{Lavg}, V_{od}\right) \text{ float},3 \rightarrow \begin{pmatrix} -.248 & .282 \\ -.183 & .161 \\ 1.43 & .557 \\ 10.7 & 12.5 \\ 47.2 & 54.9 \end{pmatrix}$$

Figure 3.37: Solution of average model with diode loss

It is instructive to solve these same equations with diode nonidealalities not considered. Figure 3.38 shows the MathCAD solution of the ideal modeling equations for this operating point.

$$L := 1 \cdot 10^{-6} \qquad R := 11 \qquad F_s := 100 \cdot 10^3$$

$$V_{in} := 20 \qquad T_s := \frac{1}{F_s} \qquad V_o := 50$$

Given

$$V_{in} - \left(V_o \cdot D_2 + V_{in} \cdot D_3\right) \equiv 0 \qquad \frac{V_o}{R} \equiv I_{Lavg} \frac{D_2}{D_1 + D_2}$$

$$D_1 + D_2 \equiv \frac{2 \cdot I_{Lavg}}{V_{in} \cdot D_1 \cdot T_s \cdot \frac{1}{L}} \qquad D_3 \equiv 1 - D_1 - D_2$$

$$\text{Find}\left(D_1, D_2, D_3, I_{Lavg}\right) \text{ float}, 3 \rightarrow \begin{pmatrix} .261 & -.261 \\ .174 & -.174 \\ .565 & 1.44 \\ 11.4 & 11.4 \end{pmatrix}$$

Figure 3.38: Solution of the ideal average model without diode loss

A comparison of Figures 3.37 and 3.38 shows a significant shift in operating point. To evaluate the model's accuracy, the simulation results of the average model with diode loss, Figure 3.36, is presented for comparison as Table 3.4. In addition, the actual circuit's results are included in the comparison. From Table 3.4, an evaluation of the diode loss model shows a close prediction of the diode loss with less than 5% of error. Further, the addition of the diode loss model has moved the model's operating point from its ideal to

one that accurately reflects the operating point of the actual circuit. This is in contrast to the ideal model yields inaccurate results.

Table 3.4: Results comparison for diode loss evaluation

BOOST CONDUCTION LOSS ANALYSIS	ACTUAL CIRCUIT SIMULATION RdsON= 1 picoOhm	AVERAGE MODEL SIMULATION IDEAL	AVERAGE MODEL SIMULATION DIODE LOSS INCLUDED
Output Power (W)	227.19	227.25	227.27
Input Power (W)	246.8	227.27	249.7
Total Loss (W)	19.61	0.02	22.43
Efficiency (%)	92.1%	100.0%	91.0%
Conduction Loss (W) Main Switch Actual Circuit	0.07	N/A	N/A
Conduction Loss (W) Output Diode Actual Circuit	21.40	N/A	N/A
Conduction Loss (W) Output Diode (Evrd)	N/A	N/A	22.42
Voltage Drop (V) Diode Model (Evdrd)	N/A	N/A	4.93
Current (A) Diode Model (Evdrd)	N/A	N/A	4.54
Duty Ratio D1	0.279	0.261	0.282
Duty Ratio D2	0.162	0.174	0.162
Inductor Current (A) Average Value	12.4	11.36	12.48
Switch Current (A) Average Value	7.83	6.82	7.93

Table 3.4 demonstrates the accuracy of the diode loss model in the unified approach. The next step is to incorporate the conduction losses of the main switch. As discussed previously, special consideration must be given to the inclusion of the switch conduction loss model into the average model. Treatment of these losses cannot be accomplished as done with the diode loss model as the average switch current is not present in the model. For the switch conduction loss, because this current is unavailable in the model, it is more appropriate to make some approximation of the actual instantaneous waveforms and rederive the model.

In Figure 3.31, it is important to note that the total effect of the switch resistance is seen during Mode I when V_{sw} is non-zero. Following the methodology of Chapter 2, the instantaneous waveform of V_{swavg} in Figure 3.31 must be reaveraged accounting for this non-zero voltage during Mode I. By rederiving the expression for this voltage, the true average inductor current is produced, thus reflecting the shift I operating point expected with additional conduction loss.

The question then becomes how should this non-zero voltage during Mode I be accounted for. A trade between accuracy and simplicity is presented here. As mentioned earlier, this is actually an exponential charging of the input inductor. To accurately account for its average value, a nonlinear exponential function should be used here. However, it will be shown that the straight-line approximation can be made without a significant loss in accuracy. Next, assuming this charging is a straight-line, the slope of this line is needed to calculate its average value. As an assumption, the model derived here will assume that the

slope of the line is unaffected by the presence of switch on-state resistance. Equation (3.18) is the average value of this non-zero voltage in Figure 3.31 Mode I,

$$V_{rdsAVG} = \frac{1}{2} \cdot D_1' \cdot I_{max}' \cdot r_{ds} \tag{3.18}$$

where,

$$I_{max}' = \frac{V_{in}}{L} \cdot D_1' \cdot T_s \tag{3.19}$$

Having derived an expression for this voltage, the V_{swavg} expression can be refined to include this approximation. It is an approximation because, in Figure 3.31, the presence of r_{ds} does effect the slope of the Mode I V_{swavg} voltage and the peak inductor current reached during Mode I. The development here makes these simplifying assumptions with the understanding that if the results do not show enough accuracy, further refinement of the model expression is required. The rederived expression for V_{swavg} is marked with a prime and shown as Equation (3.20).

$$V_{swavg}' = V_{rdsAVG} + D_2 \cdot V_o + D_3 \cdot V_{in} = \frac{1}{2} \cdot D_1' \cdot \frac{V_{in}}{L} \cdot D_1' \cdot T_s \cdot r_{ds} + D_2 \cdot V_o + D_3 \cdot V_{in} \tag{3.20}$$

In order, to address both switch and diode conduction loss, Equation (3.18) would have to be updated to include the modified output voltage derived above as the sum of the diode voltage drop and the output voltage. The updated equation is shown as Equation (3.21) and (3.22) addresses both switch and diode conduction loss.

$$V_{swavg}' = \frac{1}{2} \cdot D_1' \cdot \frac{V_{in}}{L} \cdot D_1' \cdot T_s \cdot r_{ds} + D_2 \cdot V_{od} + D_3 \cdot V_{in} \tag{3.21}$$

where,

$$V_{od} = \frac{4}{3} \cdot \frac{r_{ds}}{D_2} \cdot I_{oavg} + V_d + V_o \tag{3.22}$$

These model modifications are incorporated in the average boost model of Figure 3.39.

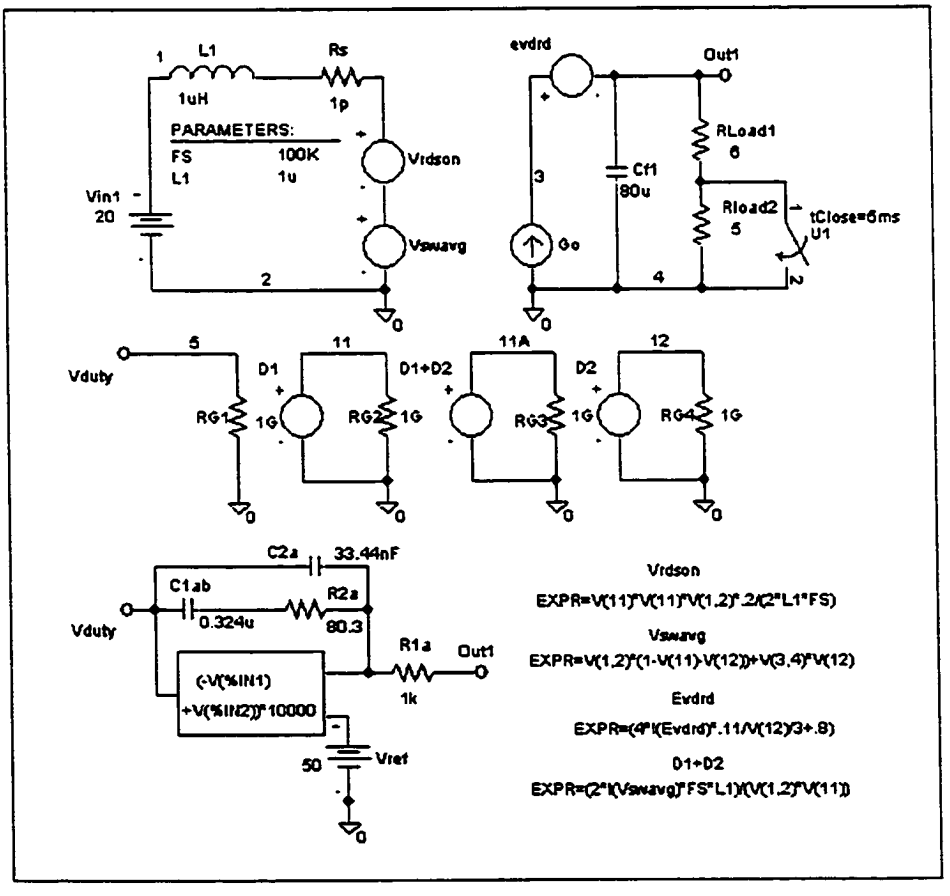


Figure 3.39: Boost model with diode and switch losses

Figure 3.39 incorporates the *Vrdon* source to correct the *Vsw* waveform's average expression. It also uses the diode loss model, *evdrd*, developed in the previous simulation set. In Figure 3.39, the on-state resistance of the switch is set to r_{ds}=.2Ω and diode model parameters are again set to V_d=.8V with r_d=.11Ω.

To evaluate the model, another actual circuit simulation run is made with the main switch on-state resistance set to r_{ds}=.2Ω. The simulation schematic for the this case is given as Figure 3.40.

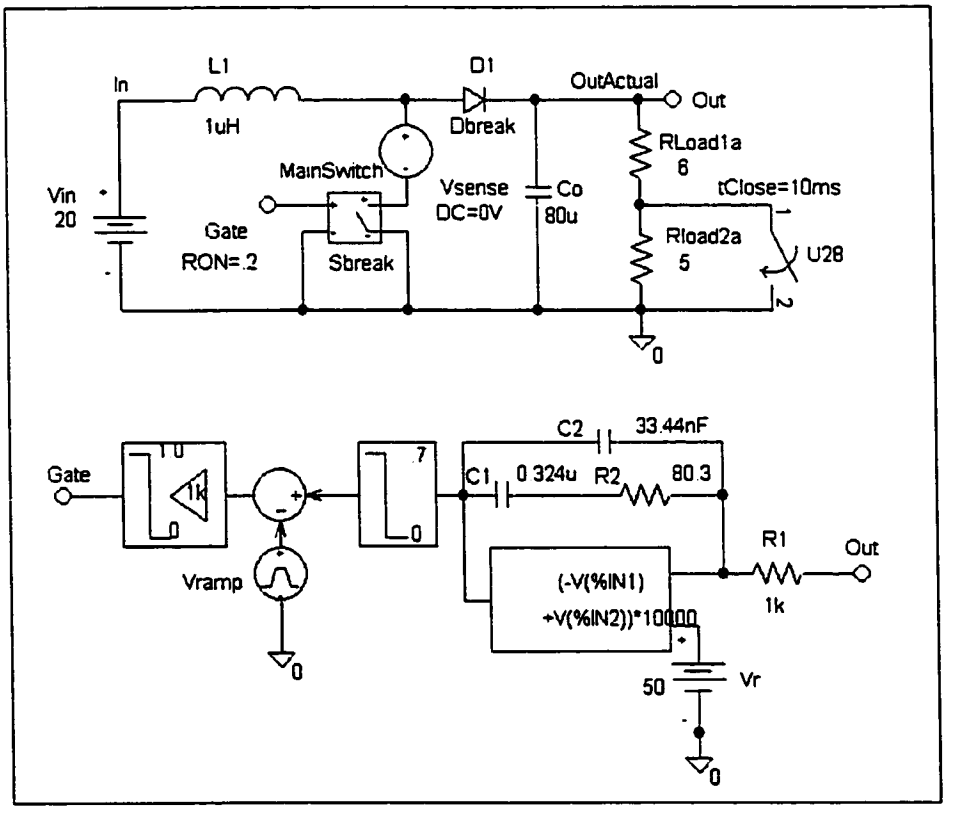


Figure 3.40: Actual boost circuit with switch and diode losses

The key waveforms of the simulation of Figure 3.40 are given as Figure 3.41. As covered previously, the nonidealalities introduced by the diode and switch have a significant effect on the key waveforms. Clearly, the inclusion of the switch on-state resistance effects the Mode I switch voltage and some exponential charging of the input inductor is noticeable.

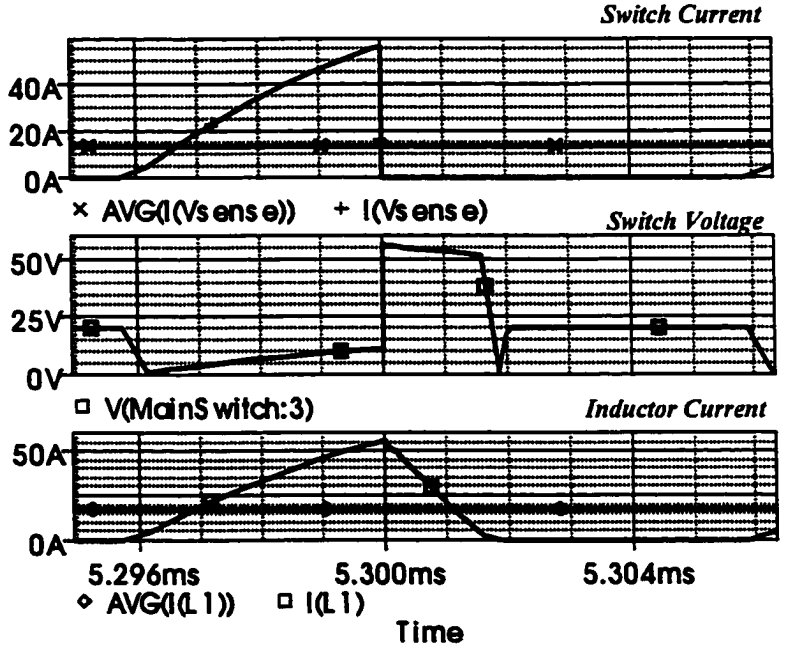


Figure 3.41: Key waveforms of actual boost circuit with switch and diode losses

A comparative study of the actual circuit simulation and the average model with losses is performed and presented in Table 3.5. Overall, the model represents a significant improvement over the lossless model when predicting actual circuit conduction losses. It is interesting to note that total loss prediction and main switch loss prediction is quite good with less than 4% error. However, the diode loss model's accuracy has decreased in this

simulation when switch losses are considered. This can be understood by considering the effect of several approximations on one another and their cumulative error. In the model, the duty ratios calculated are lower than their actual values. This is a direct result of the error factor involved with V_{rds} approximations mentioned above. Since the diode on resistance is inversely proportional to duty ratio D_2, diode losses are overstated in the model and total loss distribution is slightly skewed.

Table 3.5: Results comparison for switch and diode loss evaluation

BOOST CONDUCTION LOSS ANALYSIS	ACTUAL CIRCUIT SIMULATION Rds=.2 Ohms	AVERAGE MODEL SIMULATION IDEAL	AVERAGE MODEL SIMULATION SWITCH/DIODE LOSS INCLUDED (WAVEFORM CORRECTION)
Output Power (W)	227.15	227.25	227.27
Input Power (W)	351.15	227.27	346.27
Total Loss (W)	124	0.02	119
Efficiency (%)	64.7%	100.0%	65.6%
Conduction Loss (W) Main Switch Actual Circuit	101.35	N/A	N/A
Conduction Loss (W) Output Diode Actual Circuit	21.40	N/A	N/A
Conduction Loss (W) Output Diode Simulation (Evdrd)	N/A	N/A	25.27
Conduction Loss (W) Main Switch Simulation	N/A	N/A	93.73
Duty Ratio D1	0.382	0.261	0.357
Duty Ratio D2	0.166	0.174	0.127
Inductor Current (A) Average Value	17.56	11.36	17.26
Switch Current (A) Average Value	13.1	6.82	12.73

Overall the development of these loss-based models shows excellent simulation results. The next step is to test these loss-based models against experiment data to investigate their accuracy. In the next section, loss model prediction will be tested against an experimental prototype.

3.5 Experimental Validation of Newly Formed Loss Models

To further investigate the loss models developed in the previous section, an experimental prototype was used to tabulate total losses and specifically losses of the main switch. The schematic diagram, Figure 3.42, shows the actual circuit configuration of the prototype.

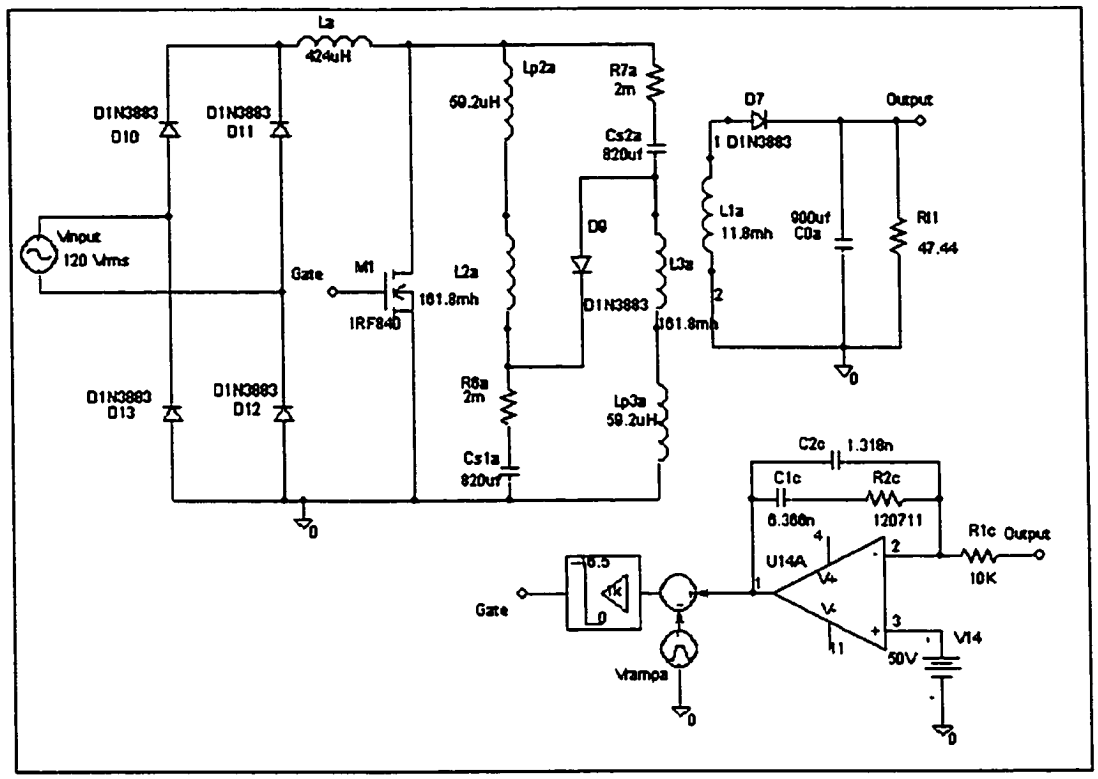


Figure 3.42: Prototype schematic diagram

Figure 3.42 shows the prototype design schematically. It represents the experimental design for the power factor corrector of used through this work. The presence of the closed loop controller allows for a regulated DC output under universal AC input. Experimental data will be collected at different input voltages so that model accuracy over a wide range of operating points can be tested. The IRF840 MOSFET was chosen because of its poor on-state resistance ($r_{ds} \approx .8\Omega$). This large on-state resistance will exacerbate switch conduction loss and facilitate the investigation of model accuracy. Auxiliary power for the

control loop was derived from a benchtop power supply and as such does not contribute to circuit losses.

Loss measurements of the prototype of Figure 3.42 were conducted. Total losses were measured electrically as the difference between input and output power. Conduction losses in the IRF840 were measured by the combination of done by two separate procedures. The first procedure used the oscilloscope to calculate the IRF840's conduction loss from traces of switch voltage and current. The second procedure made thermal comparisons to known electrical inputs to derive the total switch loss (conduction plus switching losses).

Experimental data was gathered at five input voltages which ranged from 100VAC-140VAC in increments of 10VAC. At each different input, the circuit is allowed several minutes to reach thermal equilibrium. The next step involved a measurement of the IRF840 r_{ds}. To make this measurement, the oscilloscope was used to display the conduction region of the IRF840 at various points along the 60Hz input waveform. At each of these points, the scope calculates the trace for the division of the switch drain to source voltage by its drain current during the Mode I switch on interval, V_{ds}/I_{ds}. Figure 3.43 shows the oscilloscope trace used to determine r_{ds}.

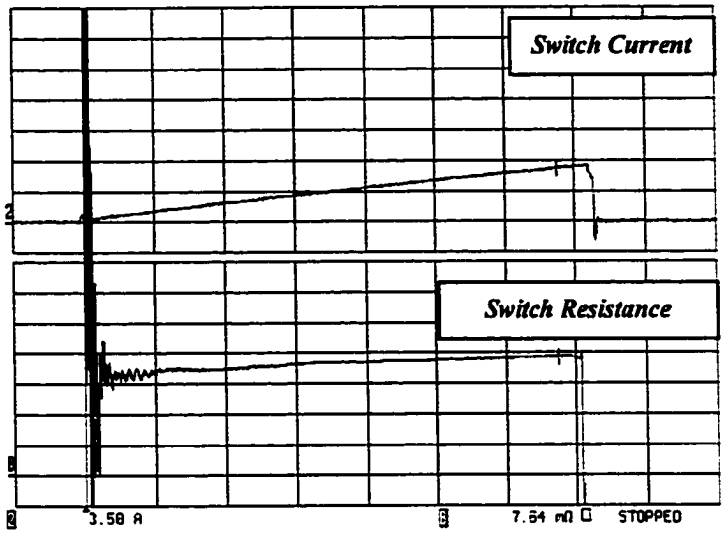


Figure 3.43: Drain current and calculated on-resistance of main switch
Vline=110VAC, measured at phase=90 Deg (line voltage), Temp=68DegC
Top: Idrain (2A/Div); Bottom: Rdson (200mOhm/Div); Time: 1us/Div

From Figure 3.43, the bottom plot shows the calculated r_{dson} value, which is largely constant over the switch on time with an average value of .764Ω. It is interesting to note that this value is nearly constant and that the same value is measured when the prototype is operated at the five different input voltages.

Loss data is gathered first from electrical measurement of the input and output powers. From this information total prototype losses are established.

Next, the data collection focuses on main switch losses. Total loss of the main switch is derived by temperature measurement. In order to obtain reasonable accuracy, the switch must be unaffected by the other heat sources within the circuit. To move toward this goal,

the main switch and its attached heatsink, which form a thermal system, are isolated physically from the other heat producing elements within the prototype by placing a slight bend on the leads of the assembly and isolating it further through the use of a cardboard shield. From here an infrared thermal probe is used to measure the temperature of the assembly at each of the five input voltages. Special care is taken to allow the circuit to reach thermal equilibrium prior to the measurement. This part of the experiment results in a known temperature of the heatsink/transistor assembly for a given input voltage.

Once this series of measurements is complete, the main switch and its heatsink are removed as a complete assembly from the circuit. Then, using the benchtop power supply, the main switch is gated on, and a known drain current is developed. This new system is allowed to reach thermal equilibrium and the electrical power dissipated is measured. A thermal measurement via the infrared probe is paired with the value of the electrical power dissipated in the transistor assembly. Several datapoints are collected forming a relationship between electrical power sunk into the transistor assembly and the temperature of the assembly. These datapoints represent the total electrical losses dissipated over the thermal system based on a temperature of that system. Since the transistor and its heatsink are designed to evenly distribute heat, temperature across the external surfaces of both the heatsink and transistor is very uniform. Thus, for a given temperature, this relationship yields the total electrical loss in watts dissipated by the switch. It is important to note this number represents total loss generation of the switch (both conduction and switching).

With the curve derived above, the main switch temperature measurements made at each of the five prototype input voltages are converted to a total loss value.

A curve generated by this series of known loss versus temperature pairs is generated to allow a mapping between the temperature of the transistor assembly when measured during normal circuit operation and the total loss generated in the main switch at that operating voltage.

With total loss of the main switch known for each input voltage, the next task is to separate this total loss figure into two parts: conduction loss and switching loss. The oscilloscope's mathematical functions are used to calculate switch conduction loss. This is done by positioning the scope cursors at the end points of the switch conduction interval on a trace of the product of switch voltage and current. The scope then provides a measure of the area under the curve, which is then translated into watts lost.

As similar procedure was attempted to identify switching loss. To accomplish this goal, the scope cursors are moved to the transition area of the switch. Unlike the product curve in the conduction region, the transition region demonstrates extremely high dv/dt. These high transient values made an accurate measurement of switching losses via this method impossible.

With total loss and conduction loss values for each of the five operating points known, the next step is to develop a loss-based model for the circuit of Figure 3.42. Since the topology in Figure 3.42 is boost like at the input and output sections, the derived diode and switch

loss models will be applied to the main switch and the output diode. Diodes in the rectifier bridge and in the capacitor charging path will not be considered as there total loss in neglibile.

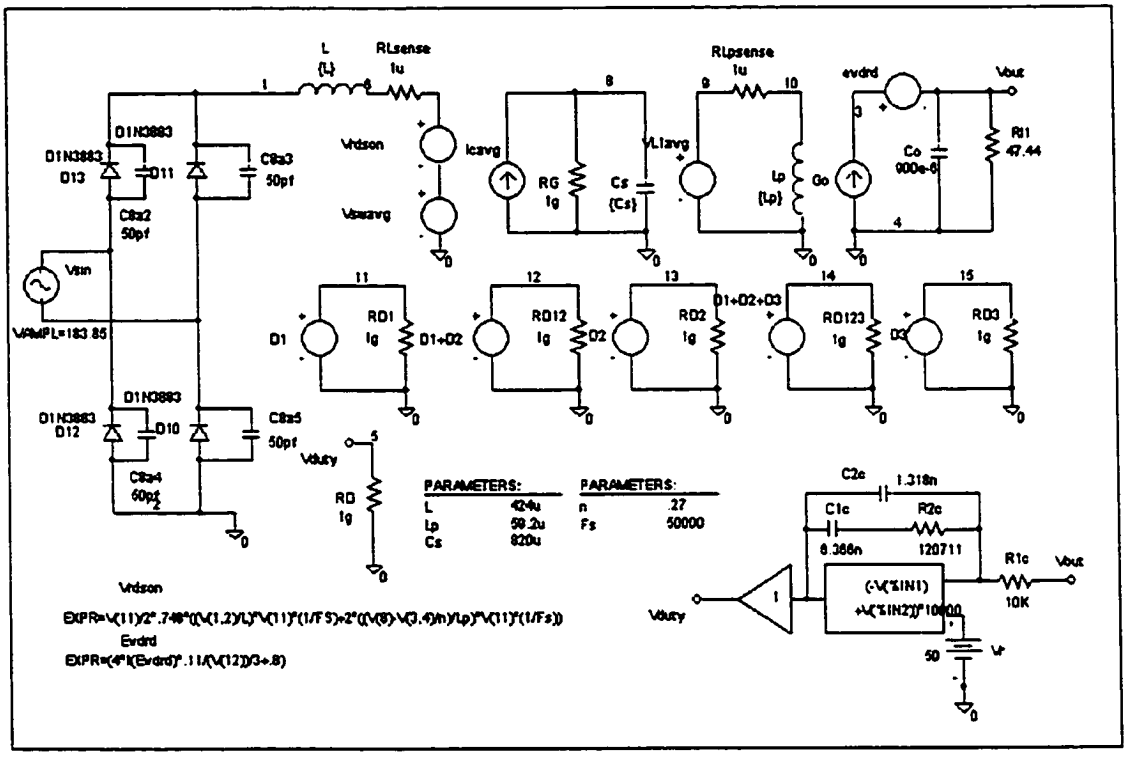


Figure 3.44: Loss-based model derived for circuit of Figure 3.42

In Figure 3.44, the controlling expression for the *Vrdson* and *evdrd* sources are derived in the same manner as presented for the boost in Section 3.3. The expression for *evdrd* and *Vrdson* are presented as Equations (3.23) and (3.24), respectively.

$$E_{vdrd} = \frac{4}{3} \cdot \frac{r_d}{D_1 + D_2} \cdot i_d + V_d \tag{3.23}$$

$$V_{rdson} = \frac{1}{2} \cdot D_1 \cdot r_{dson} \cdot \frac{V_{in}}{L} \cdot D_1 \cdot T_s + 2 \cdot \frac{(V_{cs} - \frac{Vo}{n})}{L_p} \cdot D_1 \cdot T \tag{3.24}$$

A comparative study is now performed to evaluate the results of the average model as compared with the experimental data and as compared to an actual circuit simulation. The purpose of using an actual circuit simulation here is to perform a sanity check on the experimental data and to develop a comfort level regarding the accuracy of the model prediction.

Figure 3.45 shows the simulation schematic of the experimental prototype. Although, it is merely a simulation of the actual circuit prototype, it is expected to produce relatively accurate loss predictions as each component in the simulation is taken from the professional PSPICE part libraries where each part's characteristics are modeled at a high level.

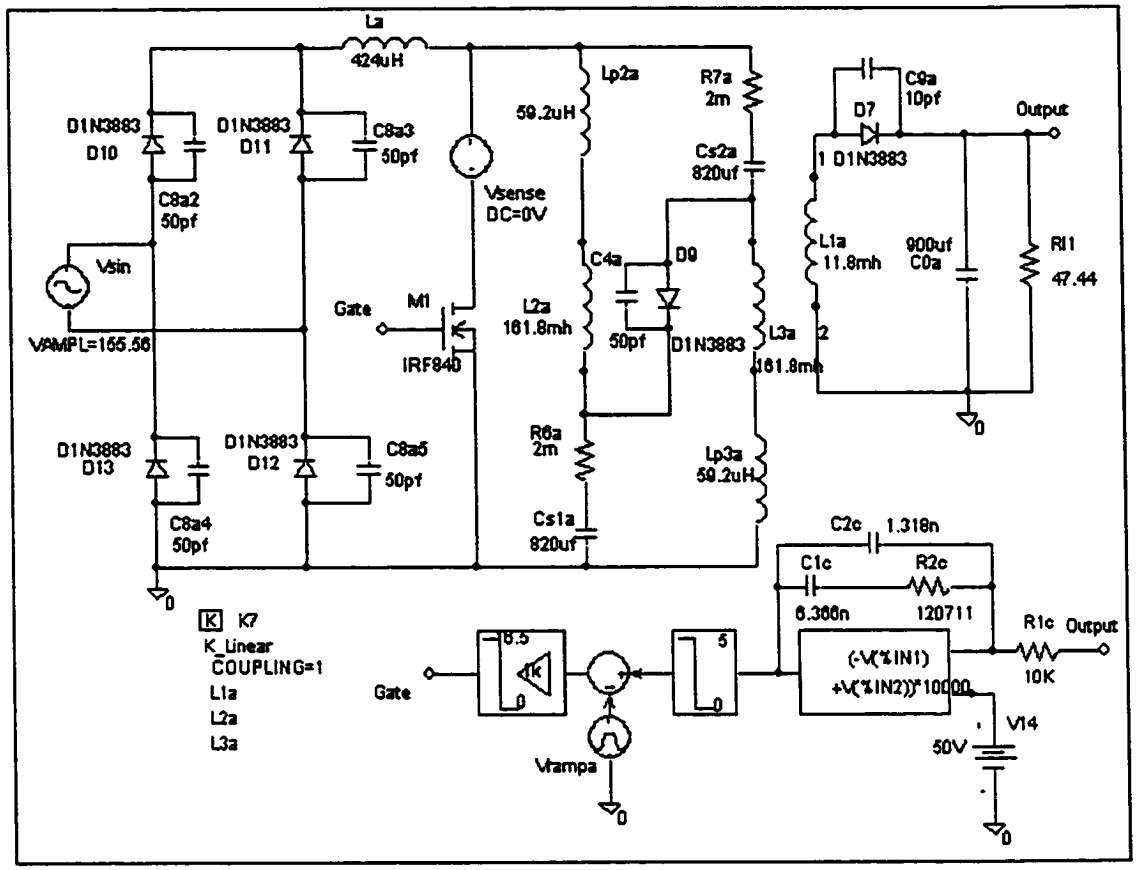


Figure 3.45: Actual circuit simulation of prototype

Table 3.6 shows the final comparison of the results of the experimental work, the results of the actual circuit simulation, and the results of the newly derived loss based model.

Table 3.6: Comparison of loss predictions to experimental data

POWER FACTOR CORRECTOR LOSS ANALYSIS					
Input Voltage (VRMS)	**100**	**110**	**120**	**130**	**140**
Output Power (W) Experimental	52.7	52.7	52.8	52.8	52.7
Input Power (W) Experimental	61.3	61.1	61.1	61.1	61.1
Total Loss (W) Experimental	8.6	8.4	8.3	8.3	8.4
Efficiency (%) Experimental	86.0%	86.3%	86.4%	86.4%	86.3%
Conduction Loss (W) Main Switch Experimental	0.94	0.88	0.75	0.71	0.66
Conduction Loss (W) Main Switch NEW MODEL Simulation	**0.95**	**0.91**	**0.79**	**0.75**	**0.7**
Total Loss (W) Main Switch Experimental	1.51	1.31	1.24	1.14	1.13
Total Loss (W) Main Switch Actual Circuit Simulation	1.43	1.3	1.22	1.19	1.08
RDSon (MilliOhms) Experimental	0.748	0.748	0.748	0.748	0.748
Prediction Error- Actual Circuit Simulation of Total Switch Loss to Experimental	**-5.2%**	**-0.8%**	**-1.9%**	**4.0%**	**-4.4%**
Prediction Error- New Model Conduction Loss Error to Experimental	**1.1%**	**3.4%**	**5.3%**	**5.6%**	**6.1%**

In Table 3.6, all the data experimentally gathered is in rows denotes "Experimental", the data from the simulation of Figure 3.45 is denoted "Actual Circuit Simulation", and the

data predicted by the model derived here is denoted "NEW MODEL" and is shown in large font and bold. The final two rows show the error in the predicted value as compared with the experimental data.

From Table 3.6, an examination of the Prediction Error rows reveals relatively good loss predictions for 100-140VAC case. Overall, model prediction is quite good with the average prediction error of the actual circuit simulation over all five inputs at 3.3% versus the average new model prediction error of 4.3%.

It is interesting to note that for these operating points, total switch loss does not account for the majority of the losses in the circuit with switch loss approximately 20% or less of the total. The remaining losses, most of which are with the output diode, make-up a significantly larger portion.

3.6 Evaluation of Conduction Loss Models

In the preceding chapter, conduction loss models where validated for both CCM and DCM operating modes. Results showed that excellent accuracy can be obtained from conventional CCM models [44]. For the DCM model, accuracy of the approach in [30] was also relatively good but additional refinement was done to improve accuracy and to adapt the concept to the unified modeling approach.

Simulation and experimental comparisons show the average model with the derived loss mechanisms predict conduction losses within 10% of error overall. If additional accuracy

is required, the simplifications made during loss model development be replaced by more detailed models.

As an example, the *Vrdson* expressions derived, which use the straightline approximation, can be rewritten as exponential functions and the effect of dynamic on-state resistance of the switch on $I_{Switchmax}$ can be considered.

It should be noted that this represents a fundamental trade-off between computational ease and accuracy. With the model simplifying assumptions, average model simulations were instantaneous while actual circuit runs varied from 15-30 minutes. PSPICE data files produced during these simulations ran 100-250 MB for the actual circuit simulations versus 1-5MB for the simulations of the model. These statistics serve to underscore that average models yield excellent accuracy with significantly reduced computational difficulty even when nonidealalities are considered.

CHAPTER 4: APPLICATION TO SOFT-SWITCHING TOPOLOGIES-STEADY STATE

4.1 Introduction

The previous work on modeling focused on hard-switching converter topologies exhibiting either the separated or conventional PWM switch. The successful application of the presented modeling approach proves the methodology is suitable for a very wide cross section of power electronics. While this subset represents the majority of current power electronic converters, new converter topologies incorporating the soft-switching concept are becoming more common due to the promise of smaller switching loss, higher energy density, and efficiency. As a result of these new features, soft-switching topologies are becoming more attractive. However, in the past, difficulties with their control and the complexity of their designs precluded them from large-scale acceptance in the commercial market. More recently, innovative techniques have been developed to mitigate the shortcomings of the soft-switching families. These new advances in control and switching technology have facilitated the production of commercially available soft-switching converters. These newer design concepts might represent the future of power electronics.

With this in mind, it is appropriate to investigate the application of the modeling approach presented here to soft-switching topologies. To that end, this chapter will discuss the modeling work on soft-switching converters. It will provide a brief description of the soft-

switching concept, present the target topology qualitatively, discuss the topology's operation and provide the mathematical analysis of the target converter's operation. The subsequent chapter will build on this analysis producing an average model and use it to produce the small-signal results.

4.2 The Concept of Soft-switching

The term soft-switching generally refers to the use of resonant modes to bring voltage and/or current stress at the switch to zero prior to state transition. Fundamentally, soft-switching occurs in two forms zero voltage switching (ZVS) and zero current switching (ZCS). For ZVS, switch voltage is resonates to zero, in the previous mode, before switch turn-on. For ZCS, switch current resonates to zero before switch turn-off. The target topology employs ZCS but the concepts presented apply equally well to both.

4.3 Overview of High Voltage, High Power Converters

High-voltage DC-DC converters are widely used in different types of electronic equipment such as industrial and medical X-ray imaging, traveling wave tube, R.F. generation etc. However, the design of high-voltage DC-DC converters is problematic because the large turns ratio of the transformer exacerbates the transformer non-idealities. In particular the leakage inductance and the winding capacitance can significantly change converter behavior. In switched-mode converters, the output transformer leakage inductance causes

undesirable voltage spikes that may damage circuit components and the winding capacitance may result in current spikes and slow rise times. These non-idealities can lead to greatly increased switching and snubber losses and reduced converter efficiency and reliability [34,39,42].

The choice of a converter topology for high-frequency, high-voltage applications is severely limited. The high voltage transformer, the central component in any high voltage application, limits topology choice. Further, output filter inductors at high voltage side often can not be used due to the high voltage drop on the inductors and reverse over-voltage across diodes caused by ringing of parasitic parameters. Based on the above considerations, many power converters have been proposed in the past as a means of supplying high output voltages. Of these converters, the most commonly used have been the conventional series and parallel resonant converters [35-41].

Regarding the SRC and PRC converters, while operating at light load, the series resonant converter (SRC) becomes virtually uncontrollable. Moreover, parasitic capacitance is not integrated into the resonant tank in the SRC [35,37,41]. The parallel resonant converter (PRC) with capacitive output filter proposed in [36] and [39-41] are relatively simple, but are difficult to control over a wide voltage conversion ratio and load ranges. In addition, saturation problems in the high-voltage transformer can occur in the full bridge implementation of the PRC. To remove the above limitations, the resonant converter with three or more resonant elements is proposed in [38]. In this converter, control and soft switching are maintained over wide load and voltage conversion ratio ranges by circulating

an additional amount of reactive energy through the resonant components. Due to the increased complexity of the resonant circuits, multi-element resonant converters exhibit complex dynamic behavior. This characteristic often precludes fast and robust transient response. To realize constant frequency and ZVS operation, the improved version series resonant converters are proposed in [33] and [37]. However, in case of the high power/power factor application, the three-phase power factor correction converter will generally be employed as a front-end regulator, and the intermediate DC bus voltage is often over 600V. The minority–carrier devices such as BJTs, IGBTs and GTOs are predominantly used in this type of application. For these applications, converters with ZCS operation will be more attractive than those with ZVS. In addition, the rectifier diodes usually suffer from severe reverse recovery problems under high DC output voltage situation. Therefore, the operation of the rectifier diodes with ZVS is desired.

The FB-ZCS topology studied in this chapter avoids many of the potential pitfalls mentioned and exhibits several outstanding features. The next section will present a variation the FB-ZCS suited for high voltage applications.

4.4 Topology Overview

Although relatively few soft-switching topologies have made it to the market, the Full-Bridge Zero-Voltage-Switched (FB-ZVS) topology has achieved commercial success. The topology, Figure 4.1, has attracted much attention in high power applications due to its

distinctive features such as ZVS, low current stress, use of parasitic components, and simple structure.

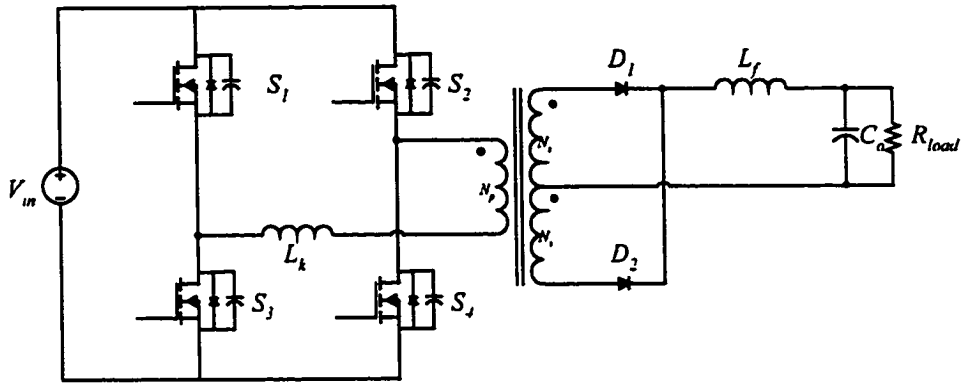


Figure 4.1: FB-ZVS topology

Because of the converter's widespread use, this topology has been thoroughly studied in open literature where one can find the steady-state analysis, small-signal analysis, and dynamic models for simulation.

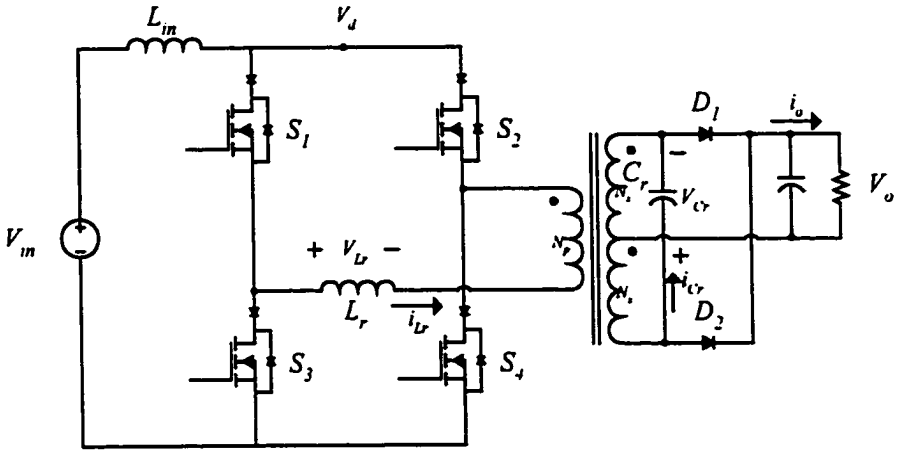


Figure 4.2: FB-ZCS topology

The FB-ZVS topology is a buck-like converter which makes use of transformer and switch parasitic elements to achieve ZVS. The FB-ZVS converter's dual, the FB-ZCS, Figure 4.2, is boost like and exhibits many of the desirable features of its ZVS counterpart. Further, unlike the FB-ZVS converter, the FB-ZCS topology has only been briefly covered in open literature. A qualitative description can be found in [32], which describes operational modes, but no detailed analytical analysis is provided. To the best of the author's knowledge, a detailed analysis of the FB-ZCS topology has not been done previously.

The FB-ZCS converter is deemed desirable for high power applications since it combines the advantages of conventional PWM and ZCS-QRC techniques, while overcoming their control limitations. The FB-ZCS converter utilizes phase-shift control and thus achieves constant frequency operation. All the primary switches operated with ZCS while the

rectifier diodes operate with ZVS without an auxiliary switch. Since the rectifier diodes operate on the high voltage side of the converter, the ZVS operation is particularly useful. Both the primary switches and rectifier diodes operate with low current/voltage stress. Therefore, switching losses are greatly reduced without the increase in switch stress normally associated with converters of this type.

When compared to the PWM converter, switching losses are greatly reduced at the expense of a modest increase in conduction losses. Since the parasitic capacitance of the switches are not used (standard for ZCS operation), capacitive turn-on loss and parasitic ringing are present in this circuit. For high power applications, devices such as IGBT's are commonly used. These are minority carrier devices and thus have smaller output capacitance. Problems with capacitive turn-on loss and parasitic ringing are less pronounced when these devices are employed.

As mentioned earlier, the rectifier diodes are operated with ZVS. This feature is particularly attractive for high output voltage applications where the diodes suffer from severe reverse recovery problems when conventional PWM or ZVS-QRC techniques are used.

4.5 Presentation of Target Topology

A traditional FB-ZCS topology was shown in Figure 4.2, which is a dual topology of the well-known FB-ZVS-PWM converter. For high voltage applications, Figure 4.3 represents

a more practical form of Figure 4.2. In Figure 4.3, L_r is the resonant inductance which incorporates the leakage inductance of the transformer, and C_r is the resonant capacitor which incorporates the junction capacitance of the rectifier diodes and the reflected winding capacitance from secondary side of the power transformer. The insertion L_{in} between input and inverter is to achieve a current-fed source.

In this chapter, the target application is the high voltage, high power load. A practical power supply system for this application usually requires a power converter with multiple high voltage DC outputs, typically 15kV, 10 kV and 5kV etc. For the sake of simplicity, the multi-output load is reduced into a single output load R (15kV, 5kW rating) in this analysis.

Generally, in a high voltage, DC/DC converter, output-filtering inductors can't be used on the high voltage side due to high voltage drop. Therefore, only output capacitors can be used at the secondary side and the primary side of the transformer should be a current-fed source. The traditional FB-ZCS topology fits this structure well. However, to obtain safe operation of transformer and high output voltage, multiple secondary rectifier circuits are needed in series to feed the high voltage load. Further, each single rectifier circuit is a full bridge configuration in order to maximize the rectifier's reverse blocking capability. A practical schematic diagram of the high voltage FB-ZCS converter would feature a high voltage transformer with 6 same section secondary windings, series connected diodes, and a resonant tank at low voltage side.

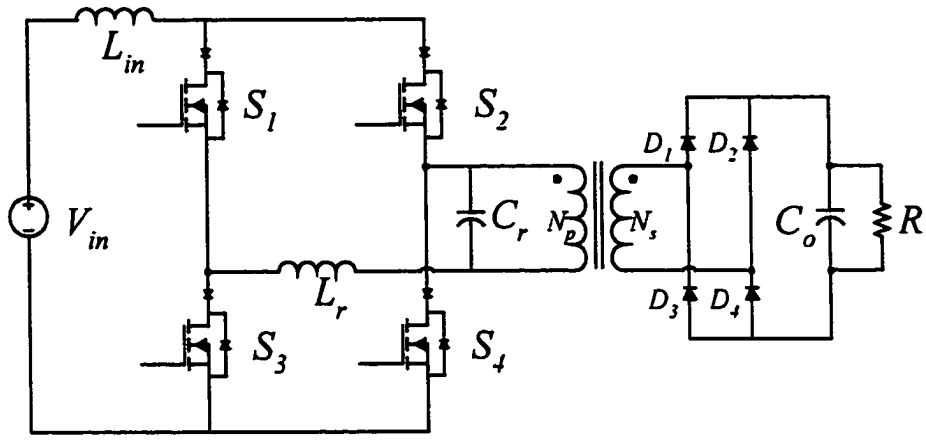


Figure 4.3: Simplified high-voltage FB-ZCS converter

Figure 4.3 is a simplified equivalent circuit based on the lumped parameter model of the high voltage transformer [40]. In the equivalent circuit, all leakage inductors are reflected and integrated into resonant inductor, L_r, on the primary side, and capacitors are reflected and incorporated into resonant capacitor, C_r. Similar to the FB-ZVS-PWM converter, the modified FB-ZCS-PWM converter also uses phase-shift control to obtain fixed frequency operation.

4.6 Operational Modes

It can be shown that the proposed converter has ten operation intervals during a single switching cycle. The equivalent circuit for each interval during the half-cycle is shown in Figure 4.4-4.8, and key waveforms are shown in Figure 4.11-4.13. Symmetry exists

between the first and second five modes. The derived equations, characterizing the converter's behavior during each mode, are based on the following assumptions:

(1) L_{in} current is ripple free and can be considered a constant current source, I_{in}

(2) output voltage is a constant, V_o

(3) all components are considered ideal

(4) from the high voltage transformer, the leakage inductance is used as resonant inductor, L_r and its capacitance is integrated into the resonant capacitor, C_r.

Mode I: $[t_o \le t \le t_1]$ ***-S_3/S_4 Overlap (linear transfer)***

Operation begins with S_1, S_3, S_4, and D_2/ D_3 on. During this mode, S_4 current is transferred to S_3 in a non-resonant, linear fashion so that S_4 can turn off with ZCS. During this mode, energy is transfer to the output. Mode I ends when the current in S_4 reaches zero and S_4 is turned off.

Equivalent Circuit (Model):

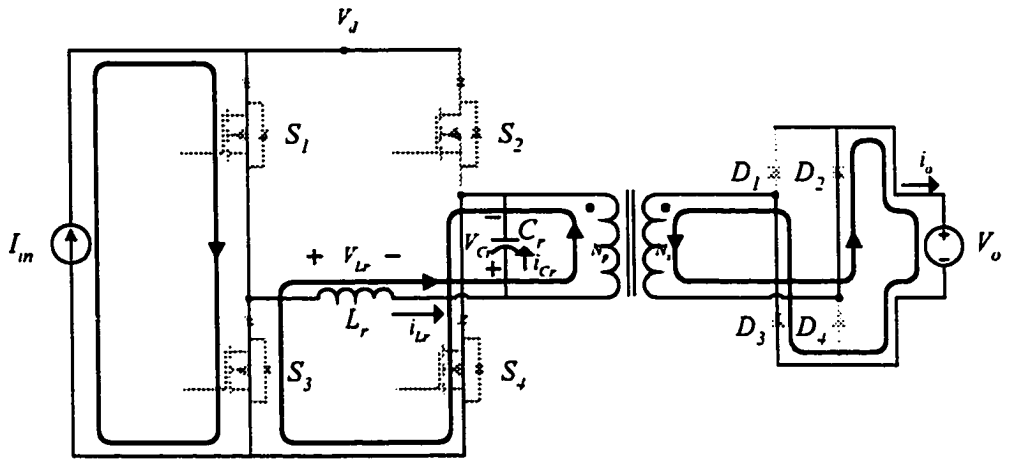


Figure 4.4: FB-ZCS Mode I

Key Equations:

$$i_{Lr}(t_o) = I_{in}\ n = \frac{N_p}{N_s} \tag{4.1}$$

$$i_{Lr}(t) = i_{sw4}(t) = -\frac{n \cdot V_o}{L_r} \cdot (t - t_o) + i_{Lr}(t_o) \tag{4.2}$$

$$i_{Cr}(t) = 0 \tag{4.3}$$

$$v_{Cr}(t) = n \cdot V_o \tag{4.4}$$

$$v_{Lr}(t) = -n \cdot V \tag{4.5}$$

$$i_{sw1}(t) = I_{in} \tag{4.6}$$

$$i_{sw2}(t) = 0 \tag{4.7}$$

$$i_{sw3}(t) = I_{in} - i_{Lr}(t) \tag{4.8}$$

$$i_{sw4}(t) = i_{Lr}(t) \tag{4.9}$$

$$i_o(t) = -\frac{n^2 \cdot V_o}{L_r} \cdot (t - t_o) + n \cdot I_{in} \tag{4.10}$$

Constraint:

Overlap of S_3/S_4 must be long enough to allow S_4 current to reach zero. At $t=t_1$, i_{Lr} becomes zero and Equation (4.13.) leads to the following interval,

$$i_{Lr}(t) = i_{sw4}(t) = -\frac{n \cdot V_o}{L_r} \cdot (t - t_o) + i_{Lr}(t_o) \tag{4.11}$$

$$i_r\ (t_o) = I_{in} \qquad\qquad n = \frac{N}{N} \tag{4.12}$$

$$i_{sw4}(t_1) = 0 = -\frac{n \cdot V_o}{L_r} \cdot (t_1 - t_o) + I_{in} \tag{4.13}$$

Solving (4.13) we obtain (4.14).

$$(t_1 - t_o) = \frac{I_{in}}{\frac{n \cdot V_o}{L_r}} \tag{4.14}$$

Mode II:: $[\ t_1 \le t \le t_2\ ]$ ***-Input Inductor Charging Interval***

With S_1 and S_3 both on, the input inductor stores energy. No energy is transferred from the input to the load, which is supported by C_o. This interval duration is assigned/controlled

for nominal operation and ends when S_2 is turned on. No constraint on interval duration exists accept that an increase in this interval duration will be accompanied by a corresponding decrease in the Mode IV interval duration since the other modes have minimum durations to achieve ZCS and the total switching period is fixed.

Equivalent Circuit (Mode II):

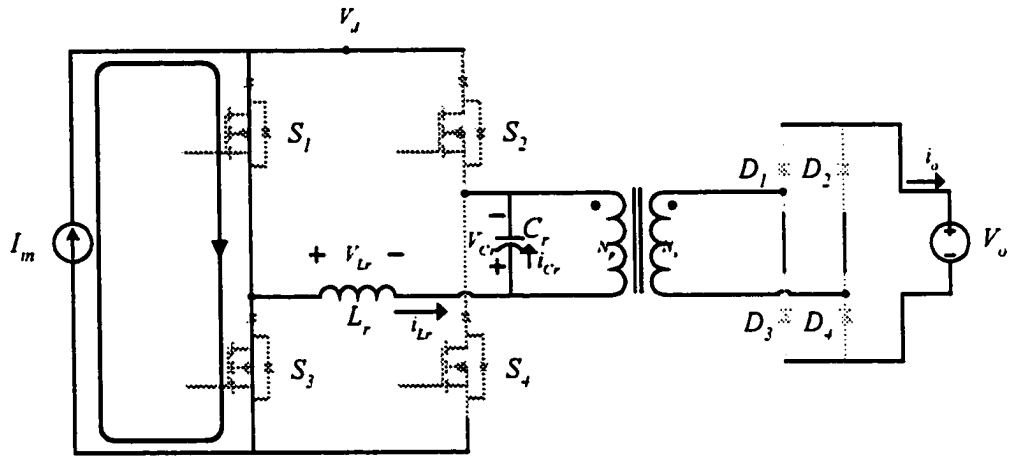


Figure 4.5: FB-ZCS Mode II

Key Equations:

$$i_{Lr}(t) = 0 \tag{4.15}$$

$$i_{Cr}(t) = 0 \tag{4.16}$$

$$v_{Cr}(t) = n \cdot V_o \tag{4.17}$$

$$v_{Lr}(t) = 0 \tag{4.18}$$

$$i_{sw1}(t) = I_{in} \tag{4.19}$$

$$i_{sw2}(t) = 0 \tag{4.20}$$

$$i_{sw3}(t) = I \tag{4.21}$$

$$i_{sw4}(t) = 0 \tag{4.22}$$

$$i_o(t) = 0 \tag{4.23}$$

Mode III: $[\, t_2 \le t \le t_3 \,]$ ***- S_1 to S_2 Overlap (resonant transfer)***

At $t=t_2$, when S_2 is turned on, S_1 current is transferred to S_2 in a resonant fashion. S_1 and S_2 overlap during this mode for the transfer. Specifically, by allowing inductor current to resonant to $-I_{in}$, S_1 current goes to zero allowing ZCS. Mode III ends when S_1 is turned off at $t=t_3$.

Equivalent Circuit (ModeIII):

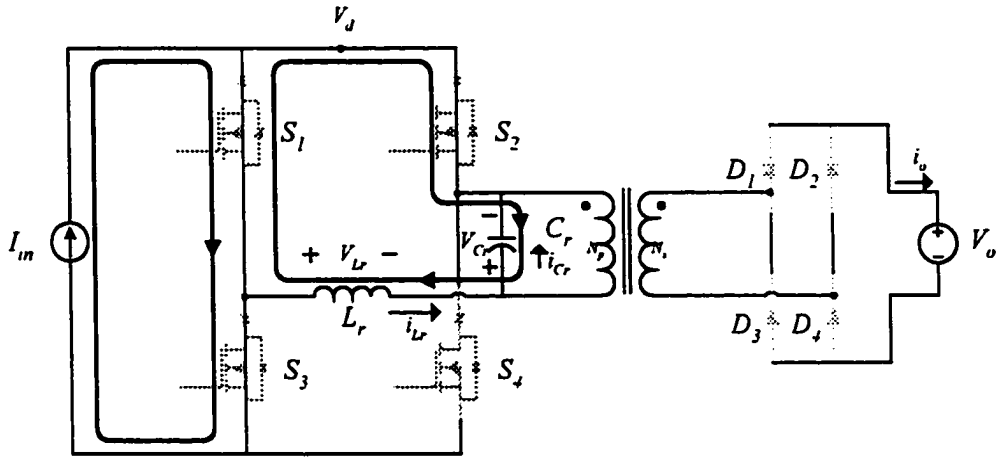


Figure 4.6: FB-ZCS Mode III

Key Equations:

$$i_{Lr}(t) = -\frac{n \cdot V_o}{Z_o}\sin(\omega_o(t - t_2)) \tag{4.24}$$

$$v_{Cr}(t) = n \cdot V_o \cos(\omega_o(t - t_2)) \tag{4.25}$$

$$i_{sw1}(t) = I_{in} + i_{Lr}(t) \tag{4.26}$$

$$i_{sw2}(t) = -i_{Lr}(t) \tag{4.27}$$

$$i_{sw}(t) = I_{in} \tag{4.28}$$

$$i_{sw}(t) = 0 \tag{4.29}$$

$$i(t) = 0 \tag{4.30}$$

Constraint:

Overlap of S_1/S_2 must be long enough to allow S_1 current to reach zero. Evaluating Equation (4.24) at $t=t_3$, with $i_{Lr}(t_3)= -I_{in}$, we obtain the following relation,

$$i_{Lr}(t) = i_{sw1}(t) - I_{in} = -I_{in} = i_{Lr}(t) = -\frac{n \cdot V}{\sqrt{L_r/C_r}} \cdot \sin\left(\frac{1}{\sqrt{L_r \cdot C_r}} \cdot (t - t_2)\right) \tag{4.31}$$

where the resonant frequency, ω_o, and the characteristic impedance, Z_o, are defined by,

$$\omega_o = \frac{1}{\sqrt{L_r \cdot C_r}} \tag{4.32}$$

$$Z_o = \sqrt{L_r/C_r} \tag{4.33}$$

Solving (4.31) we obtain (4.34).

$$\gamma = \omega_o(t_3 - t_2) = \sin^{-1}\left(\frac{I_{in}Z_o}{nV_o}\right) \tag{4.34}$$

Fundamentally this means the energy stored in the capacitor must be able to overcome that stored in the inductor.

$$\frac{1}{2}L_r(-I_{in\max})^2 \le \frac{1}{2}C_r((nV_0)^2 - (nV_0 \cdot \cos\gamma)^2) \tag{4.35}$$

In the limiting case, $\gamma=90°$, energy transfer from resonant capacitor is maximum. This maximum must be enough to drive resonant inductor current to $-I_{in}$.

Therefore, for ZCS under all line and load,

$$\frac{1}{2}\cdot C_r\cdot(n\cdot V_0)^2 \geq \frac{1}{2}\cdot L_r\cdot(-I_{inMAX})^2 \tag{4.36}$$

Values at t_3:

$$v_{Cr}(t_3) = n\cdot V_o\cdot\cos\gamma \tag{4.37}$$

$$i_{Cr}(t_3) = -I_{in} \tag{4.38}$$

Others by inspection.

Mode IV: $[\ t_3 \leq t \leq t_4\ ]$ ***-Resonant Capacitor Discharging Interval***

During this mode, the resonant capacitor discharges linearly to $-nV_o$. Mode IV ends at $t=$ t_4 when capacitor is discharged allowing D_1/D_4 to conduct. When D_1/D_4 conducts energy will be transferred from input inductor to output in a boost like fashion. Mode IV ends when capacitor is discharged allowing D_1/D_4 to conduct at t_4 mode end.

Equivalent Circuit (ModeIV):

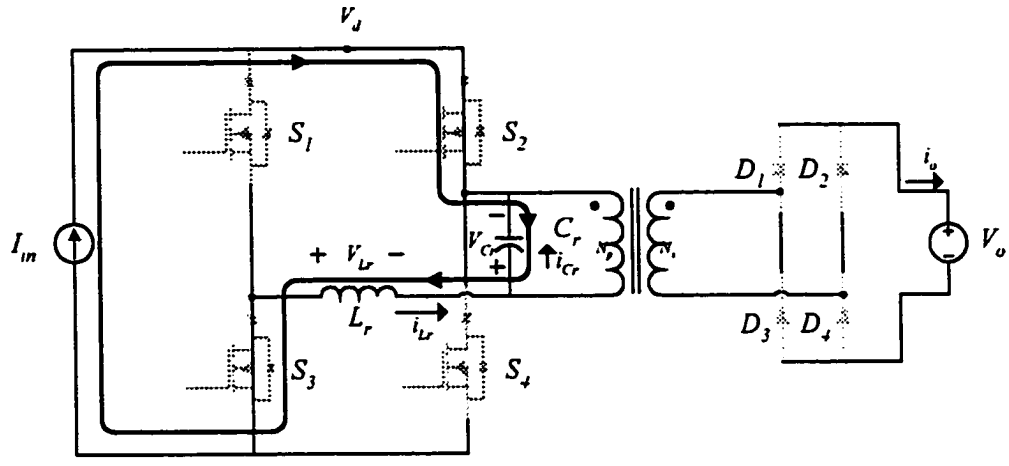


Figure 4.7: FB-ZCS Mode IV

Key Equations:

$$i_{Lr}(t) = -I_{in} \tag{4.39}$$

$$i_{Cr}(t) = -I_{in} \tag{4.40}$$

$$v_{Cr}(t) = -\frac{I_{in}}{C_r}\cdot(t-t_3) + n\cdot V_o\cdot\cos\gamma \tag{4.41}$$

$$v_{Lr}(t) = 0 \tag{4.42}$$

$$i_{sw1}(t) = 0 \tag{4.43}$$

$$i_{sw2}(t) = I_{in} \tag{4.44}$$

$$i_{sw3}(t) = I_{in} \tag{4.45}$$

$$i_{sw4}(t) = 0 \tag{4.46}$$

$$i_o(t) = 0 \tag{4.47}$$

Constraint:

Interval duration is naturally controlled. Mode ends when D_1 conducts.

$$v_{Cr}(t_4) = -n \cdot V_o = -\frac{I_{in}}{C_r} \cdot (t_4 - t_3) + n \cdot V_o \cdot \cos\gamma \tag{4.48}$$

Solving for the time interval (t_4-t_3) we obtain,

$$(t_4 - t_3) = \frac{n \cdot V_o \cdot C_r \cdot (1 + \cos\gamma)}{I_{in}} \tag{4.49}$$

Mode V: $[\, t_4 \le t \le t_5 \,]$ ***-Input Inductor Energy Transferred to Output***

During this mode, D_1 are on and energy will be transferred from input inductor to output in a boost-like fashion. This interval duration is controlled.

Equivalent Circuit (ModeV):

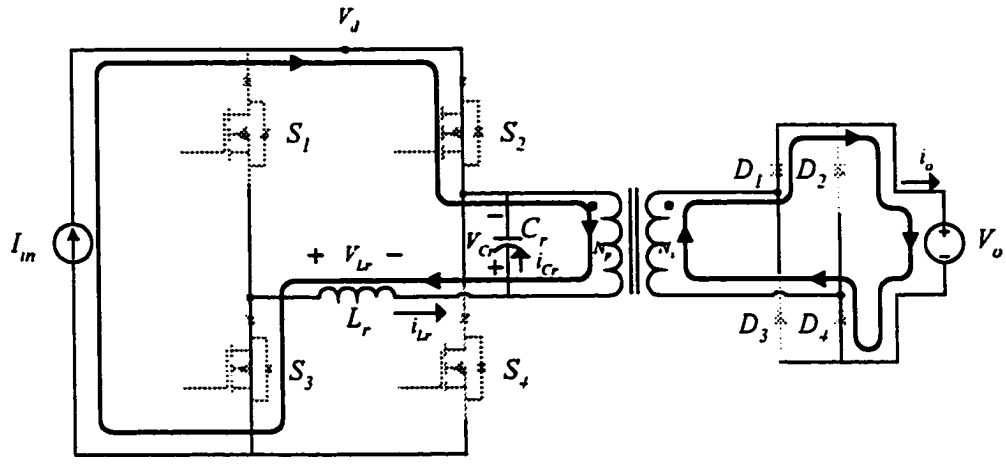


Figure 4.8: FB-ZCS Mode V

Key Equations:

$$i\ (t) = -I \tag{4.50}$$

$$i_{Cr}(t) = 0 \tag{4.51}$$

$$v_{Cr}(t) = -n \cdot V \tag{4.52}$$

$$v_{Lr}(t) = 0 \tag{4.53}$$

$$i_{sw}\ (t) = 0 \tag{4.54}$$

$$i_{sw2}(t) = I_{in} \tag{4.55}$$

$$i_{sw3}(t) = I_{in} \tag{4.56}$$

$$i_{sw4}(t) = 0 \tag{4.57}$$

$$i_o(t) = n \cdot I_{in} \tag{4.58}$$

Constraint:

None accept those mentioned in Mode I

Summary Issues/Concerns:

1. Current in S_4 might reach zero before or after S_4 turns off due to changes in line and load. During closed loop transients, periods of non-ZCS operation may occur.
2. When producing instantaneous waveforms, assume that γ is 1st quadrant angle and therefore that sine and cosine have values from 0 to 1.
3. For Mode III, the end value of inductor current and therefore switch current depends on line and load and therefore will change in transient situations, during transient resonant inductor current might reach zero before or after t_3. Average model must somehow predict this large signal behavior.

Modes VI through X are symmetric with respect to the first five modes. Table 4.1 shows device conduction states for all ten modes.

Table 4.1: FB-ZCS Mode Summary Table

Mode	S_1	S_2	S_3	S_4	D_1/D_4	D_2/D_3	*Mode Description*
Mode I	X		X	X		X	S_4 *to* S_3 *Overlap*
Mode II	X		X				L_{in} *Charge*
Mode III	X	X	X				*Resonant Transfer S1 to S2*
Mode IV		X	X				C_r *Discharge*
Mode V		X	X		X		L_{in} *Energy to Output*
Mode V		X	X	X	X		S_3 *to* S_4 *Overlap*
Mode VII		X		X			L_{in} *Charge*
Mode VIII	X	X		X			*Resonant Transfer S2 to S1*
Mode IX	X			X			C_r *Charge*
Mode X	X			X		X	L_{in} *Energy to Output*

Waveforms for several key parameters are plotted in Figures 4.9-4.11. The choice for parameters to plot was made based on three issues. First, all parameters needed to review mode interval length are plotted. Second, ZCS and ZVS is shown for the primary switches and rectifier diodes respectively. Finally, inductor voltage, Node V_d, capacitor current and output current are plotted in anticipation of further modeling efforts.

Maximum switch and diode stress occurs at different instants depending on the particular element and mode of operation as shown in Table 4.2.

Table 4.2: Maximum stress table

Parameter	v_{sw1-4}	i_{sw1-4}	v_{D1-4}	i_{D1-4}	v_{Cr}	i_{Lr}
Max Stress Value	$n \cdot V_o$	I_{IN}	V_O	$n \cdot I_{in}$	$n \cdot V_o$	I_{IN}

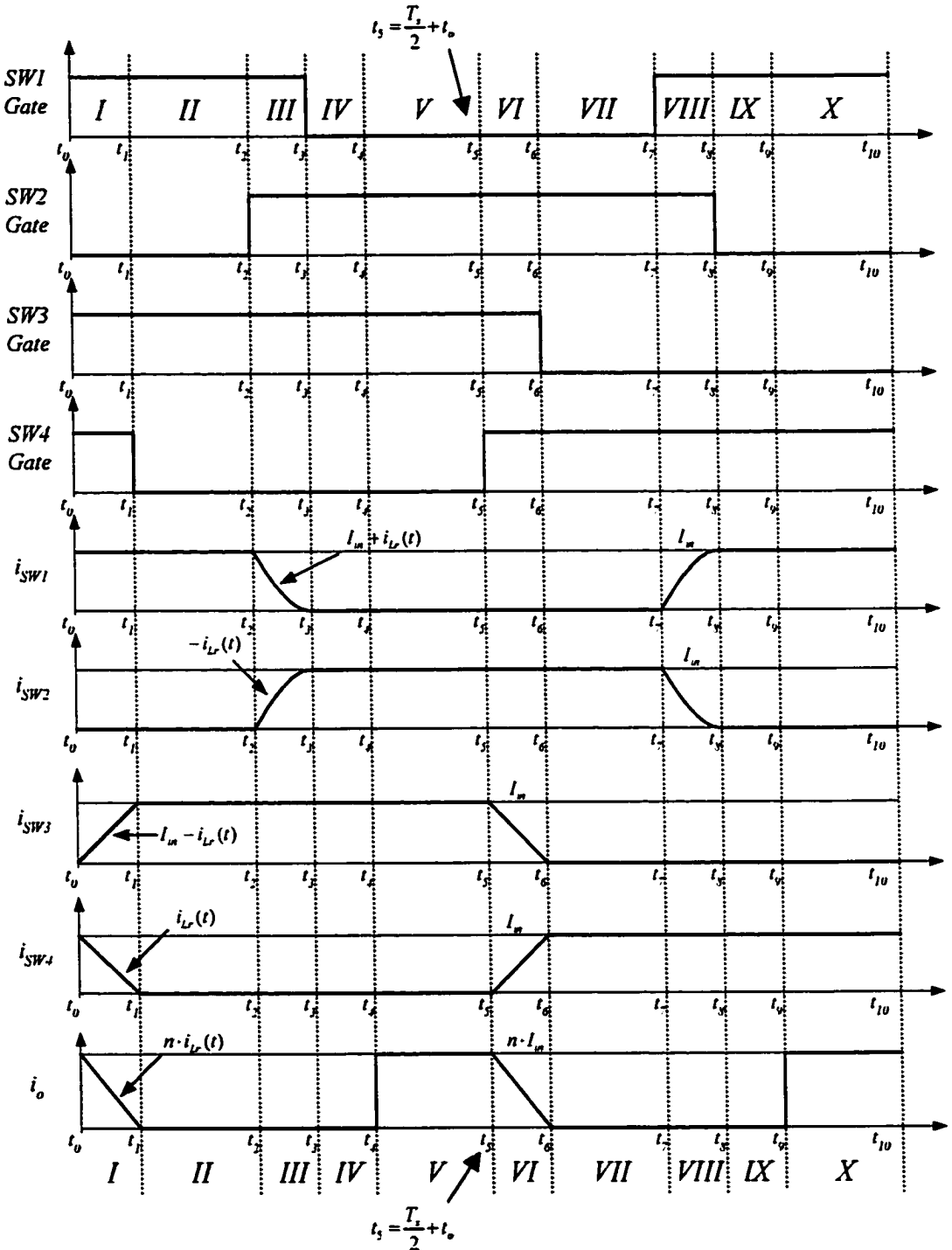


Figure 4.9: FB-ZCS Instantaneous waveforms

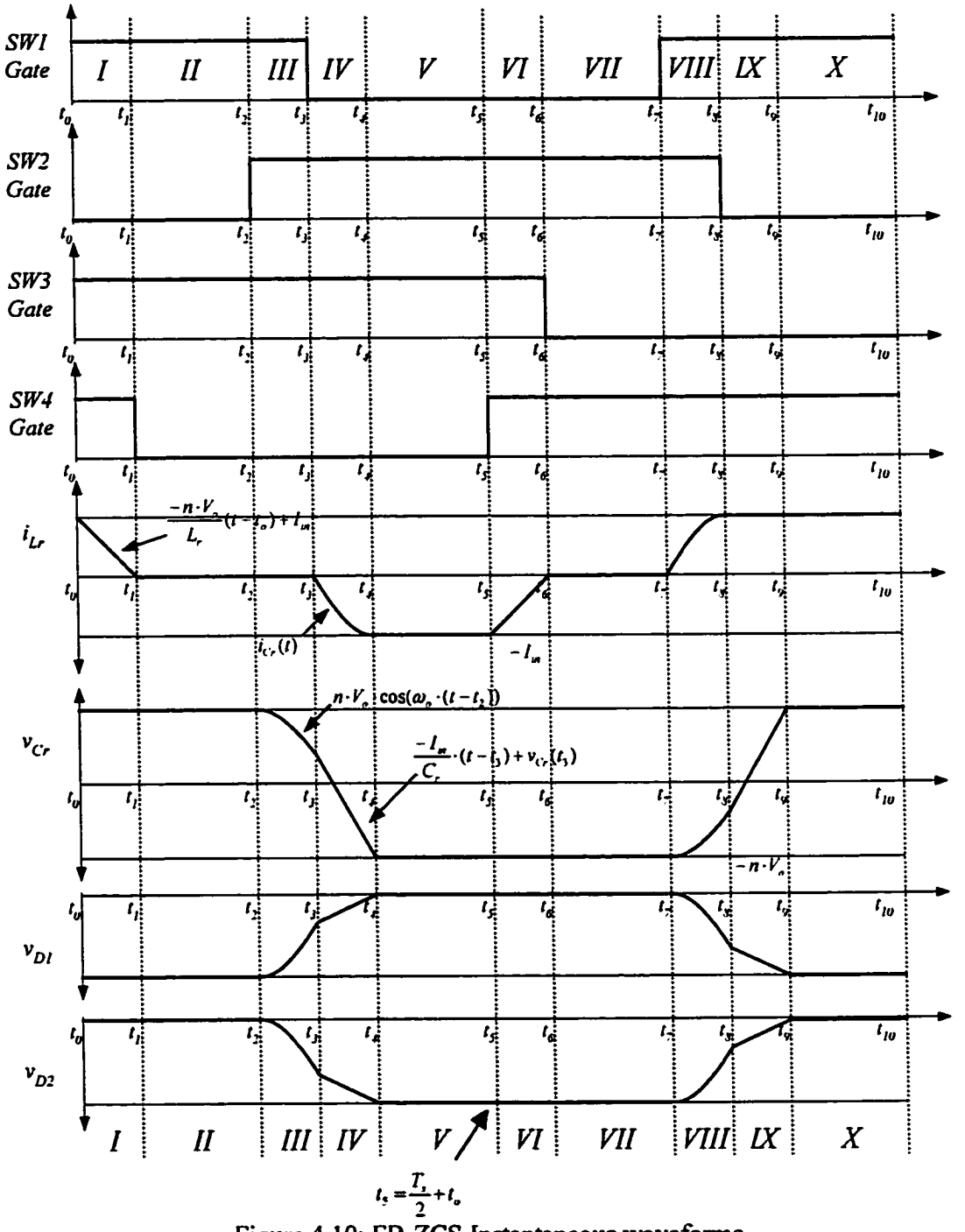


Figure 4.10: FB-ZCS Instantaneous waveforms

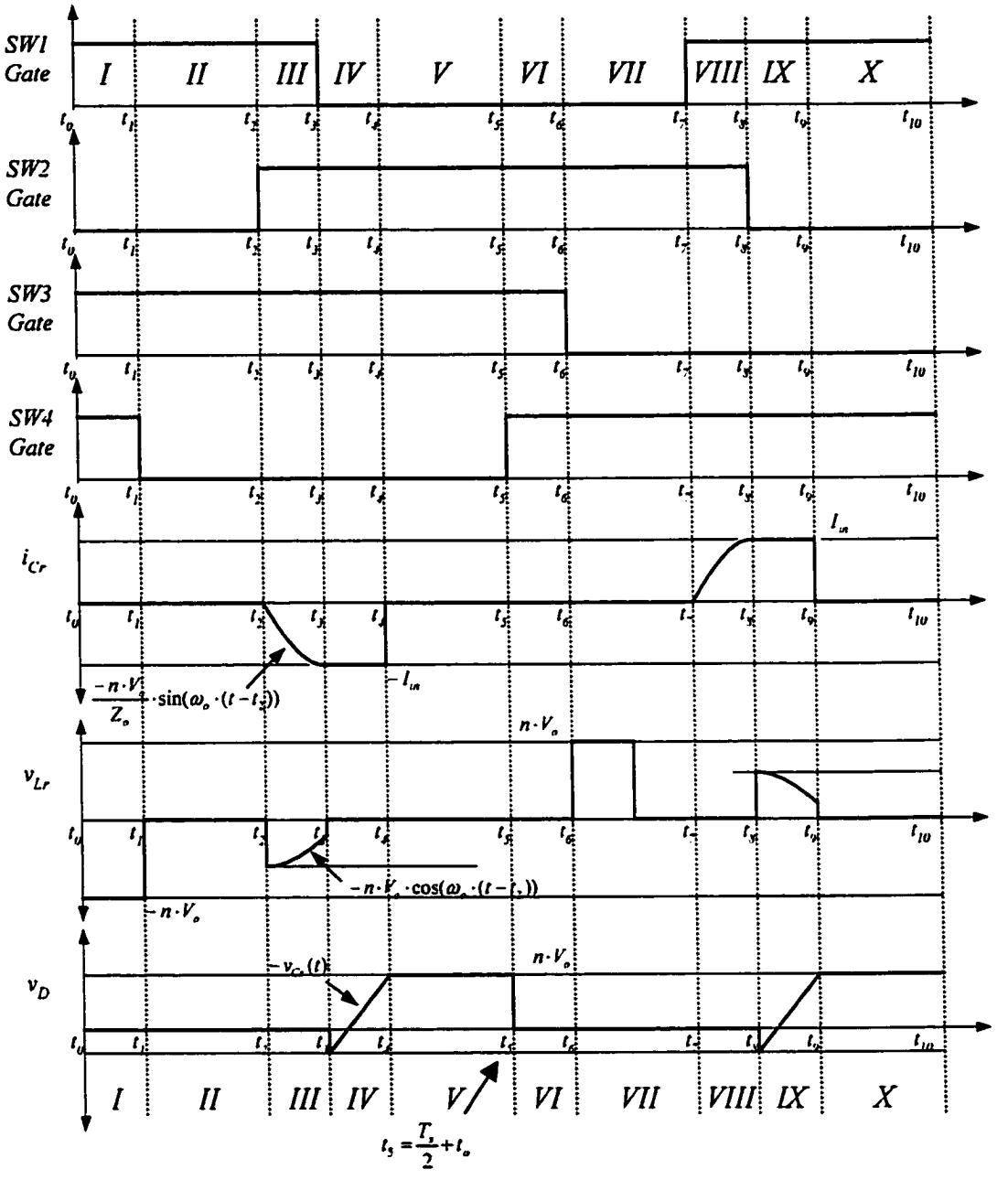


Figure 4.11: FB-ZCS Instantaneous waveforms

4.7 Steady-State Analysis of FB-ZCS with Design Example

In Section 4.6, the equations describing the modes of operation were produced. From these equations, waveforms for each of the key electrical parameters are plotted in detail. This data constitutes all the necessary information to perform the steady state analysis of the FB-ZCS converter.

Modes Summary Equations:

From Mode I

$$(t_1 - t_o) = \frac{I_{in}}{\frac{n \cdot V_o}{L_r}} \tag{4.59}$$

From Mode III

$$\gamma = \frac{1}{\sqrt{L_r \cdot C_r}} \cdot (t_3 - t_2) = \sin^{-1}\left(\frac{I_{in} \cdot \sqrt{L_r / C_r}}{n \cdot V_o}\right) \tag{4.60}$$

From Mode IV

$$(t_4 - t_3) = \frac{n \cdot V_o \cdot (1 + \cos\gamma)}{\frac{I_{in}}{C_r}} \tag{4.61}$$

And the final equation comes from averaging the output current waveform during the half period $T_s/2$

$$I_0 = \frac{\frac{1}{2}\cdot(t_1 - t_0)\cdot n\cdot I_{in} + n\cdot I_{in}\cdot(t_5 - t_4)}{\frac{T_s}{2}} \tag{4.62}$$

$$\frac{T_s}{2} = (t_1 - t_0) + (t_2 - t_1) + (t_3 - t_2) + (t_4 - t_3) + (t_5 - t_4) \tag{4.63}$$

Assigning angles to intervals and normalizing all equations we have,

$$\alpha = \omega_o \cdot (t_1 - t_0) = \frac{M}{n\cdot Q} \tag{4.64}$$

$$\beta = \omega_o \cdot (t_2 - t_1) \tag{4.65}$$

$$\gamma = \omega_o \cdot (t_3 - t_2) = \sin^{-1}(\frac{M}{n\cdot Q}) \tag{4.66}$$

$$\delta = \omega_o \cdot (t_4 - t_3) = \frac{n\cdot Q}{M}\cdot(1 + \cos(\gamma)) \tag{4.67}$$

$$\varepsilon = \omega_o \cdot (t_5 - t_4) \tag{4.68}$$

$$\frac{\omega_o \cdot T_s}{2} = \frac{\pi}{f_{ns}} = n\cdot M\cdot(\frac{1}{2}\cdot\alpha + \varepsilon) \tag{4.69}$$

$$\frac{\omega_o \cdot T_s}{2} = \frac{\pi}{f_{ns}} = \alpha + \beta + \gamma + \delta + \varepsilon \tag{4.70}$$

where normalized parameters are defined as,

L_r, resonant inductor (4.71)

C_r, resonant capacitor (4.72)

$n = \frac{N_p}{N_s}$, transformer turns ratio (4.73)

$M = \frac{V_0}{V_{in}} = \frac{I_{in}}{I_o}$, gain (4.74)

$Z_o = \sqrt{\frac{L_r}{C_r}}$, normalized resonant impedance (4.75)

$Q = \frac{R_{Load}}{Z_o}$, normalized load (4.76)

$\omega_o = \sqrt{\frac{1}{L_r \cdot C_r}}$, resonant frequency (defined not considering transformer) (4.77)

$f_{ns} = \frac{f_s}{f_o}$, normalized switching frequency (4.78)

This set of nonlinear equations form the operating point of the converter. Although they are complicated, nonlinear equations, numerical software packages provide the tools to quickly produce operating curves for converter design.

To accomplish this task, the equations are input into the MathCAD package and are solved using the Solve Block construct. The constraint equations are listed inside the Given and Find keywords. Initial guesses are provided before the Given keyword. The arguments of the Find function are then solved. Any definitions previous to the Given keyword that are

not called for in the Find function argument are considered "knowns" and are fixed to the given value. For a total 9 unknown variables in the equations, 9 equations are required for a single valid solution. We will define 2 (f_{ns} and n), pass 2 via the defined function SolveBlock(M,Q), and solve for the remaining 5 unknowns (α, β, γ, δ, ε) with the five equations provided. The MathCAD worksheet employed is shown below as Equation set (4.79).

Equations for Solve Block:

Given

$$\alpha = \frac{M}{n \cdot Q} \qquad \delta = \frac{n \cdot Q}{M} \cdot (1 + \cos(\gamma))$$

$$\gamma = \operatorname{asin}\left(\frac{M}{n \cdot Q}\right) \qquad \frac{\pi}{f_{ns}} = n \cdot M \cdot \left(\frac{1}{2} \cdot \alpha + \varepsilon\right)$$

$$\frac{\pi}{f_{ns}} = \alpha + \beta + \gamma + \delta + \varepsilon \qquad \beta \geq 0$$

$$\varepsilon \geq 0$$

$$\text{SolveBlock}(M, Q) := \text{Find}(\alpha, \beta, \gamma, \delta, \varepsilon)$$

$$Q_{base} := 636.396 \qquad M_{design} := 18.75$$

$$\begin{pmatrix} \alpha \\ \beta \\ \gamma \\ \delta \\ \varepsilon \end{pmatrix} := \text{SolveBlock}(M_{design}, Q_{base})$$

MathCAD Solution:

$$\begin{pmatrix} \alpha \\ \beta \\ \gamma \\ \delta \\ \varepsilon \end{pmatrix} = \begin{pmatrix} 0.324 \\ 8.117 \\ 0.33 \\ 6.005 \\ 20.58 \end{pmatrix} \qquad (4.79)$$

If the solve block is successful, the function SolveBlock(M,Q) returns a solution vector containing 5 elements (index 0 to 4) corresponding to each of the five elements of the Find function argument. The function SolveBlock(M,Q) can be called successively to generate operating point plots for design by setting a value of load (Q) and specifying a range of M. By including the constraint $\varepsilon \geq 0$, we ensure MathCAD doesn't accept mathematically correct solutions that are physically unrealizable.

Now that the appropriate framework is constructed, functions can be written to plot any of the desired parameters. So for this particular run, $f_{ns} = f_{nsBASE} = .089$, $n = 1/11$, we chose to solve for the mode intervals for the design M and Q (18.75 and 636.4, respectively). Since the normalized half period length is $\frac{\pi}{f_{ns}}$, no valid solution for β greater than this value will exist. In fact, since the remaining four intervals must take some portion of the half period, β will only have valid values slightly less. In fact, we could specify the range of β to be too large without concern since the solve block is constrained to physical solutions. However, we will choose β wisely to avoid undue workload on simulator and thus reduce plot time.

Other curves can be produced for different values of f_{ns}, and n to facilitate the design process. Several curves for this topology were generated in the search for a potential operating point.

Each of these curves allows the designer quick access to the data necessary for converter design. While other curves are also needed to optimize the design process, the M vs. β curve serves as the starting point.

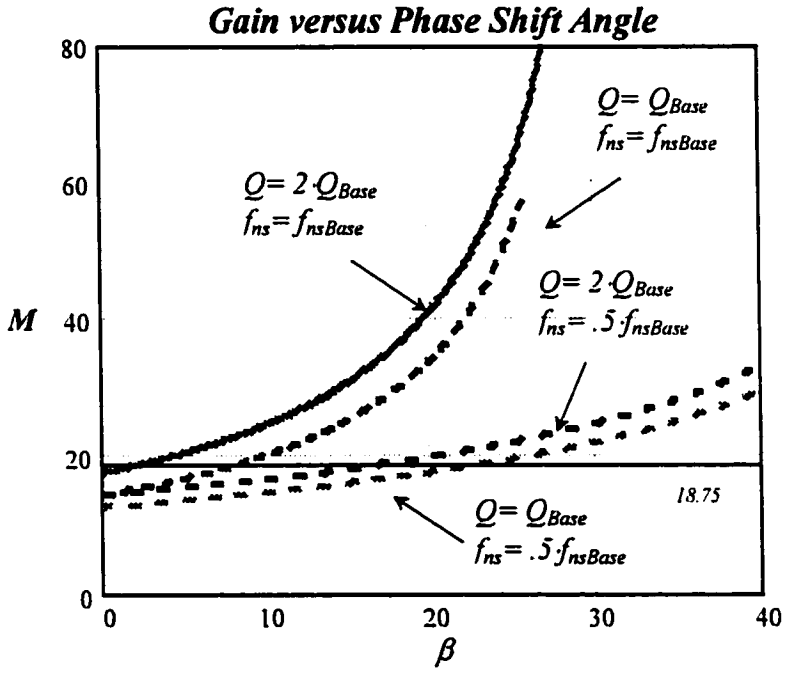


Figure 4.12: Gain, M, vs. Phase shift angle, β for various loads

The MathCAD Solve Block is used to solve for various steady state control characteristic curves. Figure 4.12 shows the curve for M vs. β under various normalized load and switching conditions. The curves are drawn for base values of Q_{Base}=636.4 and f_{nsBase}=.089

with n=1/11. The curves are presented to show the qualitative relationships between load, voltage gain, switching and resonant frequencies.

The parameter β represents the fundamental control parameter. Increasing β corresponds to a gain increase and is analogous to increasing D in the boost converter. From the curves, it is clear that an increase in load results in a decrease load regulation range for constant f_{ns} and Z_o, yet this decrease is not linear. It is shown that a 50% load variation results in a change in β of 26%. A more significant decrease in regulation range comes from reducing f_{ns}. At first glance this could seem incorrect, as it might appear that a smaller f_{ns} means less of the half period is taken by the resonant mode. While this is true, a smaller f_{ns} also means an increase Mode IV duration, resulting in less power transfer. As a final note on Figure 4.12, we observe that the curves are plotted over differing ranges of M and β. These limited ranges represent the total set of valid operating points for the given Q and f_{ns}. It is not possible to choose operating points off the plotted curve set. This is a result of several factors. First, the arcsine argument of Equation (4.66) is a representation of the ZCS condition, Equation (4.36), and establishes an upper limit on M for a given Q. Second, since the total of the five intervals equals the half period length, an increase in β means less of the half period is available for the other modes. In the limiting case, since several modes have duration fixed by operating state, β will have a fixed upper limit that is less than the half period length and is a function of load and f_{ns}. These mechanisms effectively reduce

the valid operating range of the converter. Since MathCAD only plots valid system solutions, these curves end abruptly at the maximum gain, M_{max}, for a given Q and f_{ns}.

Design Example:

With these curves created, a design example can now be performed. Since the converter is well-suited to high-power, high-voltage applications, the following design parameters will be used: $P_{OUTPUT}=5kW$, $V_{IN}=800V$, $V_{OUT}=15kV$, $f_s=20kHz$. The choice of this operating point calls for gain of 18.75. This value is marked on the design curves as a dashed horizontal line. From the $f_{ns}=f_{nsBASE}$, $Q=Q_{BASE}$ curve, we choose the nominal operating point as its intersection with M=18.75. Noting that curve for $Q=2Q_{BASE}$ also has a valid intersection with the gain line M=18.75. Anticipating future dynamic response investigation, the choice of this operating point will allow us to perform step load changes during the closed loop transient simulations. The curves indicate that a full, 100% load increase can occur ($Q=2Q_{BASE}$ to $Q=Q_{BASE}$) and still maintain a valid, ZCS operating point.

By choosing, f_{ns} and Q, the values for L_r and C_r can be selected. The numerical solver is again employed to solve for these values. With the values for L_r and C_r selected, the next step is to do a more detailed analysis of the chosen operating point to determine how suitable it is for the desired application. First, for the specific values of L_r and C_r chosen, curves will be plotted to examine the various interval lengths as a function of load. The purpose here is to rule out mathematically correct solutions that may be difficult to

implement in practice. For example, when doing the initial simulations for this converter, a valid operating point was chosen that resided on the far-right side of the M vs. β curve. This point represented a large value of β and corresponded to a proportionally small value of ε. The interval ε represents the time when the either of the output diode pairs conduct passing energy to the load. During the preliminary simulations, it was found that the small length of ε did not allow for the switching time of the PSPICE diode model. Therefore, full conduction was not achieved before mode end and the design output voltage was not realized. In summary, it is important to utilize the design tools effectively to fully evaluate the chosen operating point.

After evaluating the interval lengths for varying load, it is established that adequate load regulation is possible with the chosen operating. The next step is to calculate the steady state gating sequence of the bridge switches. For this step, the normalized interval lengths are converted back to time values. The angular intervals, calculated at full load in Equation (4.79), are converted to time in Table 4.3.

Table 4.3: Timing for design example, $Q=Q_{BASE}$

Mode I (t_1-t_0)	*Mode II* (t_2-t_1)	*Mode III* (t_3-t_2)	*Mode IV* (t_4-t_3)	*Mode V* (t_5-t_4)
.22917μs	*5.7395μs*	*.23338μs*	*4.2459μs*	*14.552μs*

We see that the some of these intervals equals the half period length as expected. Overlap periods are design for Modes I and III by looking to the largest required minimum value that will allow ZCS operation. For this case, Mode III requires approximately .25μs. This is the larger of the two intervals and it can be concluded that the resonant Mode III will always require more time than the Mode I. By choosing the overlap time of the switch gating to be at least .25μs, we guarantee than the converter will operate with ZCS for the given operating point. Generally speaking, since this time intervals for Mode I and III are functions of the load, it is wise to chose these values slightly greater than what is strictly required so than ZCS can be maintained for all nominal conditions A quick check in MathCAD shows the required overalp interval (Modes I and III) for $Q=2Q_{BASE}$ are less than those for $Q=Q_{BASE}$. It can be inferred that it is good design practice to design overlap intervals at full load to maintain ZCS over the full operating range.

The gating sequence is calculated as follows: First, the duty ratio of the main switches is calculated. For the FB-ZCS, the duty ration of the switches must be greater than 50% to allow for overlap.

In fact, duty ratio is directly related to overlap so from the overlap assignment one can calculate duty ratio and pulse width as in Equation (4.80-4.85).

$$Overlap = .25\mu s \tag{4.80}$$

$$\begin{aligned} &2 \cdot Overlap + (1 - D) \cdot T_s = D \cdot T_s \\ &\Rightarrow D = .505 \Rightarrow PW = 25.25\mu s \end{aligned} \tag{4.81}$$

$$TD1 = TD2 + PW - Overlap = 30.96865\mu s \tag{4.82}$$

$$TD2 = (t_1 - t_0) + (t_2 - t_1) = 5.96865\mu s \tag{4.83}$$

$$TD3 = 0\mu s \tag{4.84}$$

$$TD4 = PW - Overlap = 25\mu s \tag{4.85}$$

Having calculated duty ratio (pulsewidth) for the four switches, the sequence for S_1 with respect to S_2 and S_3 with respect to S_4 is fixed such that S_1 is synchronized to S_2 and S_3 is synchronized to S_4. This synchronization facilitates the switches to pass current back and forth allowing ZCS. Specifically, the overlap periods are designed to pass the current flowing in one switch to the lateral opposing switch, with the S_1/S_2 pair commutating resonantly and the S_3/S_4 pair in a linear fashion. The output voltage of the converter is regulated by adjusting the relative shift between the S_1/S_2 pair and the S_3/S_4 pair. This interval corresponds to β in the previous analysis and this will be the control parameter. For the steady state design β is achieved by delaying the turn on of holding S_3's turn on as the reference (S_3 ON begins Mode I). This means that since S_4 is synchronized to S_3 it will turn off one overlap length later. The next period is the control parameter. If the current in S_4 goes to zero at the instant S_4 is turned off, the delay between S_4 turn off and S_3 turn on is β. However, in the general case, the current in S_4 during Mode I goes to zero before S_4 is turned off. Therefore, the interval β would actually begin before S_4 turn off and not correspond to a switch state transition. This presents a unique control problem since switch

gating (the physically controllable parameter) and the interval β (the desired control parameter) are generally not coincident. The dynamic control of this converter will be addressed in more detail in the next chapter. For the steady state operation, we can see that in would be prudent to fix S_3 as the reference gating signal. This, in turn, sets the S_4 gating. Then the next interval, Mode II is the controlled interval and is ended when S_2 is turned on. The delay for S_2 to turn on is then $\alpha+\beta$. The gating sequence is calculated for the specific example (Q=25) below in Equation set (4.83).

Now all parameters are designed. To test the mathematics behind the design process, a simulation is run using the design parameters. The designed circuit, as it appears in PSPICE is shown below in Figure 4.13.

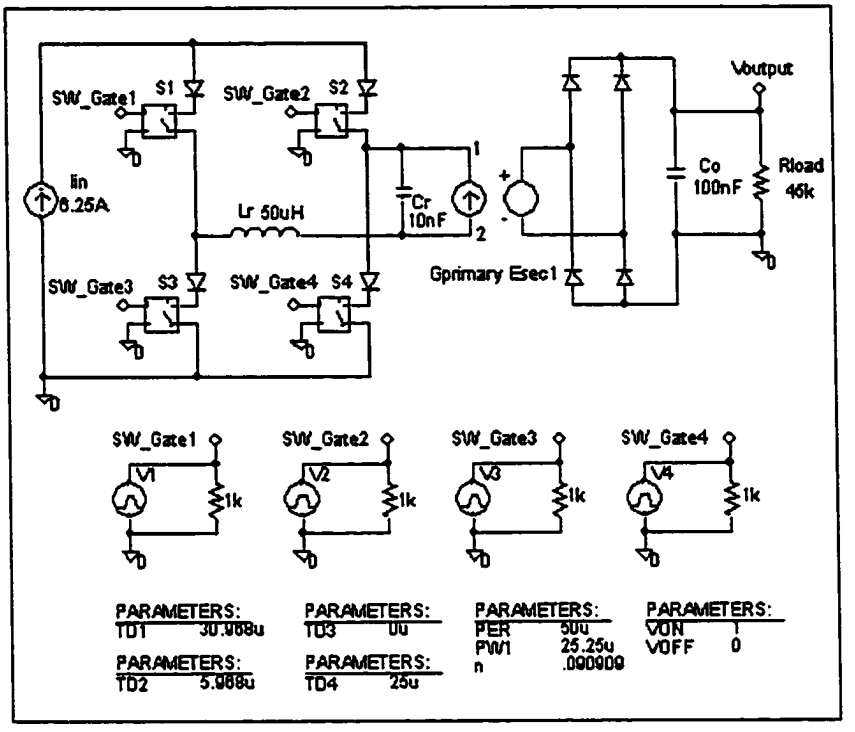


Figure 4.13: Simulation of design example

A transient simulation is run for the converter operating in open loop as shown in Figure 4.13. For the validation of the steady state analysis, the high voltage transformer is considered ideal with its leakage inductance and winding capacitance incorporated in the resonant components L_r and C_r. In Figure 4.13, switch gating signals are obtained from the pulse sources V1-V4. The sequencing and relative phase shift is shown under the Parameters part with time delays, TD1-4, a direct consequence of the calculations in Equations (4.80)-(4.85). The waveforms produced show good agreement with the

theoretical development. The ZCS condition is achieved for all the primary switches as shown in Figure 4.14.

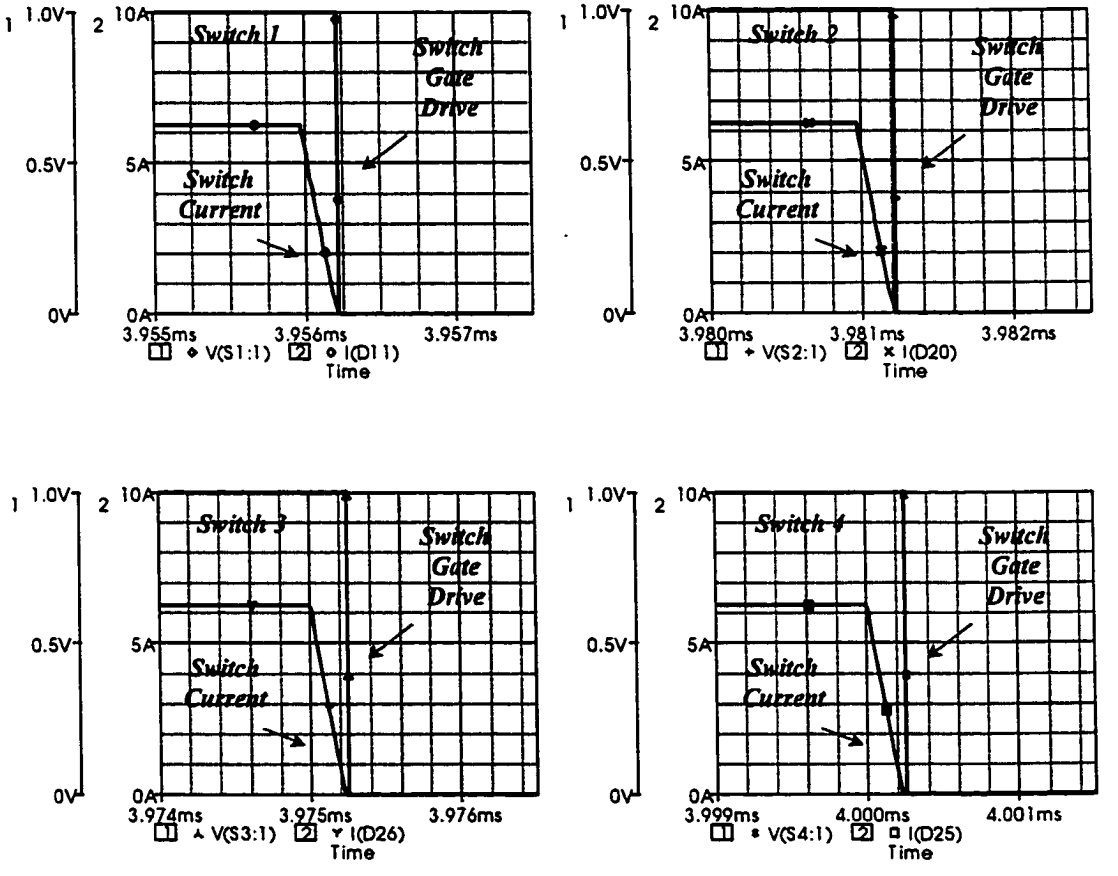


Figure 4.14: Simulation results of design example-ZCS condition

In Figure 4.15, inductor current and capacitor and voltage are shown with good agreement with theoretical derivation notwithstanding the switching transients that are expected but not considered in the theoretical analysis. Output voltage is developed at the nominal value as shown in Figure 4.16.

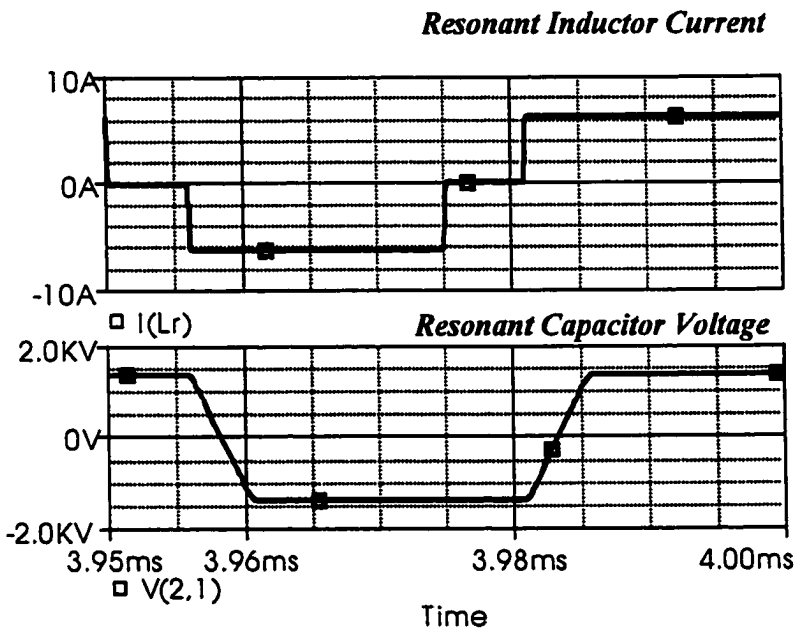


Figure 4.15: Simulation results of design example (inductor current and capacitor voltage)

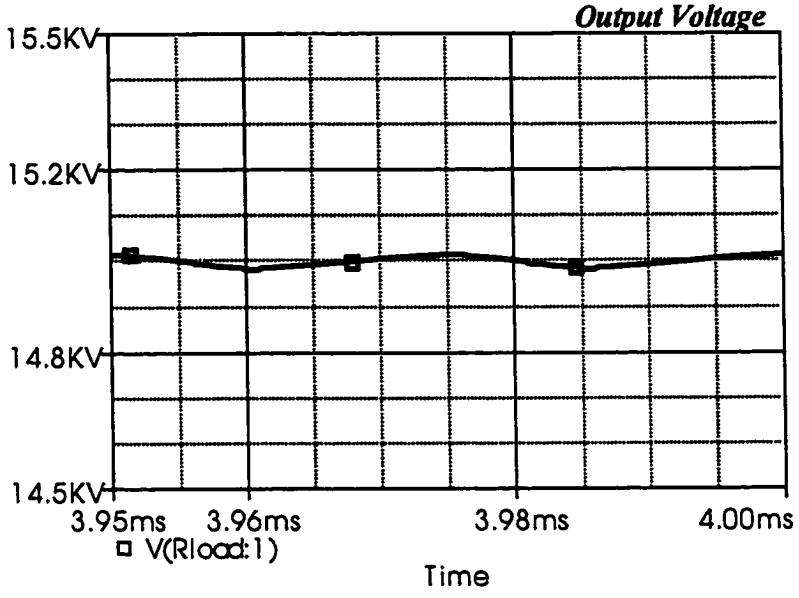


Figure 4.16: Simulation results for design example-output voltage

Additional equations are derived to predict RMS currents in the resonant inductor and main switches. Equation set (4.86) shows these equations as a part of the MathCAD solve block. Equations are shown with both currents normalized by the average output current, I_o. By observation of the converter steady state waveforms, it is clear that lateral switches will carry the same RMS current during steady state operation. As such, the mathematical development derives the equations for a representative high leg switch and a representative low leg switch. For the operating point chosen, all four switches carry approximately the same RMS current. In addition, it is interesting to note that the resonant inductor carries approximately 20% more RMS current than any of the primary switches.

It should be noted that the complexity and form of the nonlinear equation set formed by (4.86) requires the use of a different numerical algorithm to solve. MathCAD's default Conjugate-Gradient routine was unsuccessful in arriving at a solution. However, its Levenberg-Marquardt routine handles the system well.

Figures 4.17 and 4.18 show plots of normalized inductor and switch RMS current for different operating points based on the analysis above.

Equations for Solve Block

Given

$$\alpha = \frac{M}{n \cdot Q} \qquad \frac{\pi}{f_{ns}} = n \cdot M \cdot \left(\frac{1}{2} \cdot \alpha + \varepsilon\right) \qquad \beta \geq 0$$

$$\gamma = \operatorname{asin}\left(\frac{M}{n \cdot Q}\right) \qquad \frac{\pi}{f_{ns}} = \alpha + \beta + \gamma + \delta + \varepsilon \qquad \varepsilon \geq 0$$

$$\delta = \frac{n \cdot Q}{M} \cdot (1 + \cos(\gamma))$$

$$i_{nLrRMS} = \sqrt{\frac{f_{ns}}{\pi} \cdot \left[\frac{n^2 \cdot Q^2}{3} \cdot \alpha^3 - n \cdot M \cdot Q \cdot \alpha^2 + M^2 \cdot \alpha + \frac{n^2 Q^2}{2} \gamma - \frac{n^2 \cdot Q^2}{4} \cdot \sin(2 \cdot \gamma) + M^2 \cdot (\delta + \varepsilon)\right]}$$

$$i_{nSW2RMS} = \sqrt{\frac{f_{ns}}{2 \cdot \pi} \cdot \left[n^2 \cdot Q^2 \cdot \left(\gamma - \frac{\sin(2 \cdot \gamma)}{2}\right) + M^2 \cdot (\alpha + \beta + \gamma + \delta + \varepsilon) - 2 \cdot Q \cdot n \cdot M \cdot (1 - \cos(\gamma))\right.}$$

$$i_{nSW3RMS} = \sqrt{\frac{f_{ns}}{2\pi} \cdot \left[\frac{n^2 \cdot Q^2}{3} \cdot 2\alpha^3 + M^2 \cdot (\beta + \gamma + \delta + \varepsilon)\right]}$$

$$\text{SolveBlock}(\beta, Q, f_{ns}) := \text{Find}(\alpha, M, \gamma, \delta, \varepsilon, i_{nLrRMS}, i_{nSW2RMS}, i_{nSW3RMS})$$

MathCAD Solution:

$$\text{SolveBlock}(8.117, 636.3961, .089) = \begin{pmatrix} 0.32438 \\ 18.76661 \\ 0.33035 \\ 5.99896 \\ 20.52811 \\ 16.33589 \\ 13.24932 \\ 13.24966 \end{pmatrix} \qquad (4.86)$$

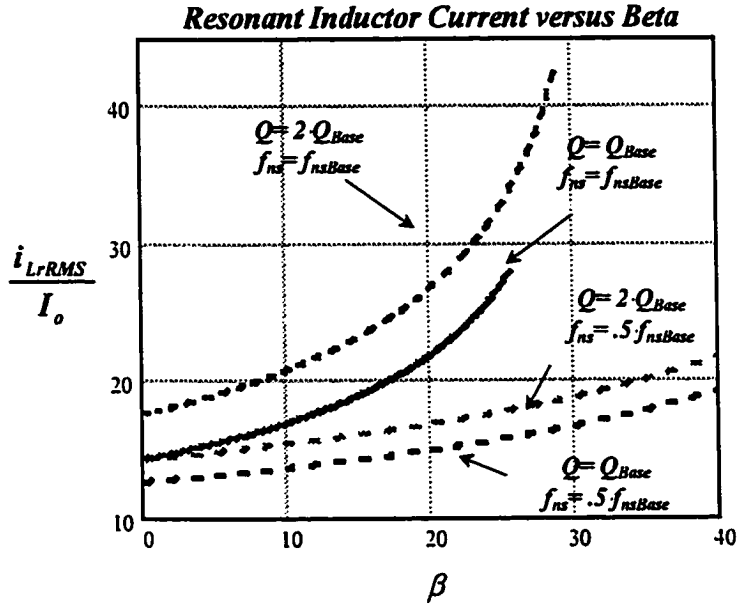


Figure 4.17: Normalized resonant inductor current

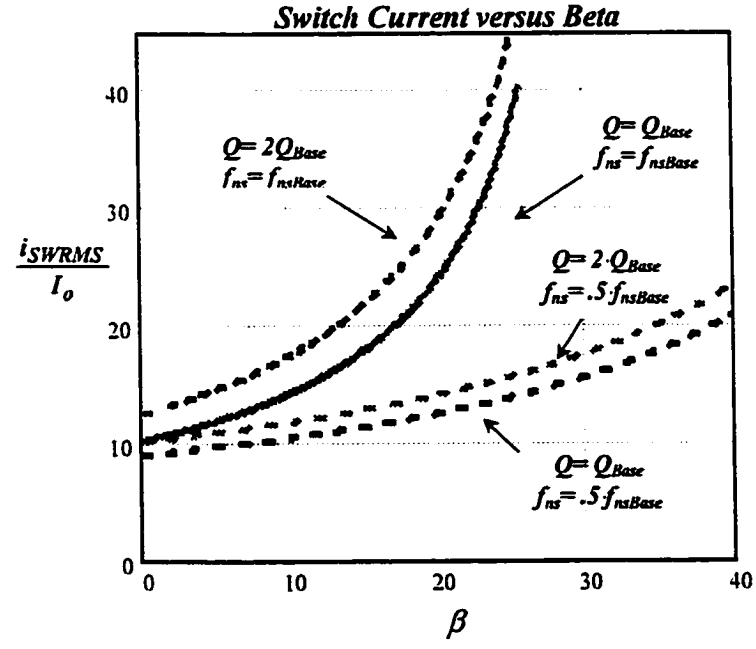


Figure 4.18: Normalized primary switch current

Table 4.4 makes a detailed comparison of the theoretical analysis and the simulation results for several key parameters. Excellent agreement is demonstrated.

Table 4.4: Theoretical result validation

Analysis Parameter	***Analysis Prediction***	***Simulation Result***
Mode I	.229μs	.22917μs
Mode II	5.74μs	5.7395μs
Mode III	.233μs	.23338μs
Mode IV	4.25μs	4.2459μs
Mode V	14.6μs	14.552μs
V_{CR} ***Clamp***	1364V	1364V
i_{Lr} ***Clamp***	6.25A	6.247A
i_{LrRMS}	5.44A	5.4401A
i_{SWRMS}	4.41A	4.4124
V_o	15kV	15kV +/- 16V

4.8 Evaluation of Steady State Analysis

The previous chapter explored the FB-ZCS converter's operation both qualitatively and mathematically. The nonlinear equation set developed during the converter analysis was solved using MathCAD and used to investigate converter operation and to choose a suitable operating point for the design example. The chosen operating point results in designed values for L_r, C_r, and switch timing. The steady state simulation performed based on the design agrees well with the calculated results and validates the design process used.

The following chapter will build on this analysis to construct and average model of the FB-ZCS converter. This new model will be used for the study of the converter's dynamic behavior under closed loop regulation.

CHAPTER 5: APPLICATION TO SOFT-SWITCHING TOPOLOGIES-SMALL-SIGNAL AND TRANSIENT

5.1 Introduction

Dynamic modeling begins with the development of an average model. The average model is once again used to produce small-signal characteristics of the FB-ZCS converter and to perform transient response simulations. The average model is derived by performing the averaging process on the converter's steady-state waveforms following the approach demonstrated in Chapter 2.

5.2 Average Model development of FB-ZCS

As in the previous sections, the approach presented here discards the cellular approach in favor of a more general method. The method here will ensure the correct average, differential voltage appears across each inductor and the correct average current flows through each system capacitor in the model, maintaining the significant dynamic mechanisms that exist in the actual circuit.

Average model development via this approach begins with inspection of the circuit schematic. Dynamic elements are identified and the steady-state waveforms are evaluated to give a qualitative idea of their effect. Certainly L_{in} and C_o have a significant effect on

dynamic response, and as such, these must appear in the model. Evaluating L_r and C_r in Figures 4.4-4.8, we examine the schematics for Modes I and III noting the resonant component will have an effect on the dynamic response of the converter. However, the relative size of resonant components is small when compared to L_{in} and C_o. Further, their contribution to the converter's dynamic response is predominately during the interval durations for Modes I and III (In this topology, Modes I and III are designed to be a small fraction of the total period, used only to achieve ZCS). Based on the above, the resonant components contribution to the overall dynamic response of the converter is extremely small and is, for the most part, limited to an effect on mode duration. As such, resonant components will appear in the controlling expressions but will not distinctly appear as components within the model.

With these assumptions in mind, the model development begins considering the model must impress the correct, average differential voltage across the input inductor and drive the correct, average current through the output capacitor. To accomplish this task, the instantaneous waveform for the voltage, v_d, voltage at the node to the immediate right of L_{in}, and the output current, i_o, are plotted in Figure 5.1 and averaging equations given in Equations (5.1)-(5.2), respectively.

$$v_{dAvg} = \frac{2}{T_s} \cdot \left(\frac{n \cdot V_o \cdot \varepsilon}{\omega_o} + \frac{(n \cdot V_o)^2}{2 \cdot i_{LinAVG}} \cdot C_r \cdot (1 - \cos(\gamma)^2) \right) \tag{5.1}$$

$$I_o = \frac{2}{T_s} \cdot n \cdot i_{LinAVG} \cdot \left(\frac{i_{LinAVG} \cdot L_r}{2 \cdot n \cdot V_o} + \frac{\varepsilon}{\omega_o} \right) \tag{5.2}$$

Inspection of these equations shows terms including both constants and time-dependent variables. Each term in these primary equations must be resolved to accommodate simulation. T_s, n, ω_o, L_r, and C_r are all constant and can be directly substituted. I_{Linavg} and V_o are circuit quantities that are iteratively calculated during numerical simulation. These values are represented by circuit schematic references in the simulator model. This leaves ε, γ, and *Duty*, which represent variable mode durations and must be solved to arrive at a solution to the system.

Additional controlling equations are added to solve for these durations by referring to the steady-state development which was discussed in detail in Chapter 4. Theses additional equations are given as,

$$\varepsilon = (1 - Duty) \cdot \frac{T_s}{2} \cdot \omega_n - \frac{n \cdot V_o}{i_{LinAVG}} \cdot C_r \cdot (1 + \cos(\gamma)) \cdot \omega_o \tag{5.3}$$

$$\gamma = a\sin\left(\frac{i_{LinAvg} \cdot Z_n}{n \cdot V_o}\right) \tag{5.4}$$

$$Duty = PWM + \frac{2 \cdot \gamma}{\omega_n \cdot T_s} \tag{5.5}$$

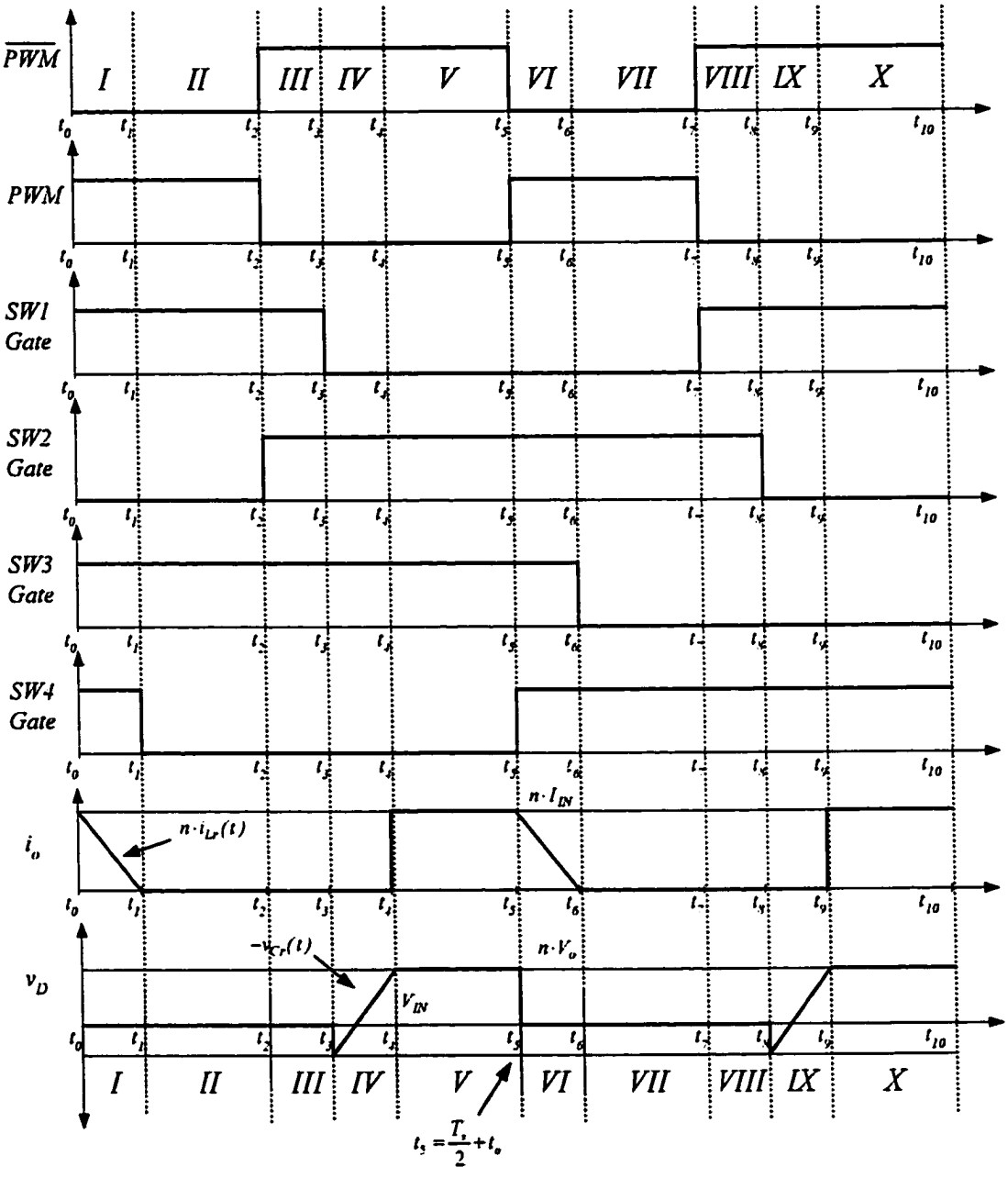


Figure 5.1: FB-ZCS Instantaneous Waveforms

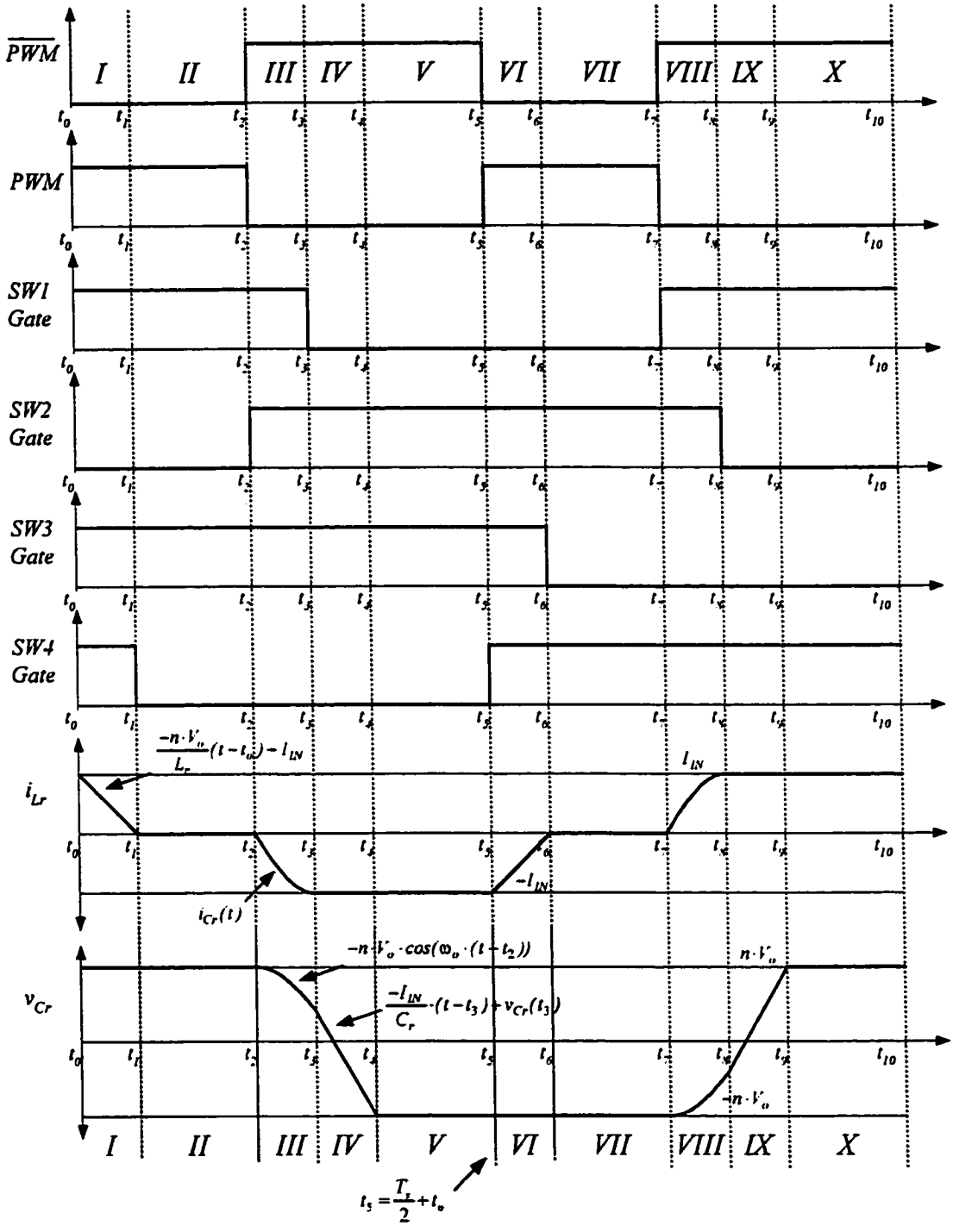


Figure 5.2: FB-ZCS Instantaneous Waveforms

An evaluation of the waveforms of Figure 5.1-5.2 shows that PWM does not directly correspond to *Duty* or (1-*Duty*), which are variable assignments that are made to correspond to boost-like intervals. The variable, *Duty*, represents primary switch on time and is shown in Equation (5.5). As such, the gain versus control will be represented as gain to PWM and is shown in Figure 5.5.

The derived equations can be directly implemented in a PSPICE subcircuit, shown in schematic form in Figure 5.4 with the circuit parameters for the design example included and with minor modifications to aid in numerical convergence. The equations, as they appear in the model within PSPICE, are shown in Table 5.1. TABLE limits in addition to LIMIT keywords are used through out to disallow divide by zero overflow.

Table 5.1: PSPICE Model Equations- FB-ZCS

	Controlling Expression	Table Limit
Vdavg	2/Ts*n*V(Output)*V(e)*sqrt(Lr*Cr)+.5*n*V(Output)*n*V(Output)/ LIMIT(I(Lin),.1,100)*Cr*(1- cos(V(gamma))*cos(V(gamma)))	(.01,.01)(2000,2000)
Go	2/Ts*n*I(Lin)*(.5*I(Lin)*Lr/(n*LIMIT(V(Output),.1,1e6))+V(e)*sqrt(Lr*Cr))	N/A
Vg_arg	I(Lin)*sqrt(Lr/Cr)/(n*LIMIT(V(Output),.1,1e6))	(-1,-1)(1,1)
VPWM	V(PWMraw)	(1m,1m)(1,1)
Vduty	V(PWM)+2*V(gamma)*sqrt(Lr*Cr)/Ts	(1m,1m)(1,1)
Ve	(1-V(Duty))*(Ts/2)*(1/sqrt(Lr*Cr))-n*V(Output)*(1/sqrt(Lr*Cr))/ (LIMIT(I(Lin),.1,100))*Cr*(1+cos(V(gamma)))	(1p,1p)(100,100)
Vgamma	asin(LIMIT(V(gamma_arg),0,.571))	(.01,.01)(1,1)

MathCAD verification of the modeling equations is shown as Figure 5.3. A comparison of the MathCAD results and the bias point overlay in Figure 5.4 shows complete agreement.

$n := \frac{1}{11}$ $V_{in} := 800$ $C_r := 10 \cdot 10^{-9}$ $L_r := 50 \cdot 10^{-6}$

$\omega_o := \frac{1}{\sqrt{L_r \cdot C_r}}$ $I_{in} := 6.25$ $PWM := .2$ $\varepsilon := .2$

$R_{Load} := 45000$ $\gamma := .2$ $Duty := 2$ $T_s := 50 \cdot 10^{-6}$

Average Model Equations

Given

$$V_{in} \equiv \frac{2}{T_s} \cdot \left[n \cdot V_o \cdot \frac{\varepsilon}{\omega_o} + \frac{1}{2} \cdot \frac{(n \cdot V_o)^2}{I_{in}} \cdot C_r \cdot \left(1 - \cos(\gamma)^2\right) \right]$$

$$\frac{V_o}{R_{Load}} \equiv \frac{2}{T_s} \cdot n \cdot I_{in} \cdot \left(\frac{1}{2} \cdot \frac{I_{in} \cdot L_r}{n \cdot V_o} + \frac{\varepsilon}{\omega_o} \right)$$

$$\varepsilon \equiv (1 - Duty) \cdot \frac{T_s}{2} \cdot \omega_o - \frac{n \cdot V_o}{I_{in}} \cdot C_r \cdot (1 + \cos(\gamma)) \cdot \omega_o$$

$$\gamma \equiv \operatorname{asin}\left(\frac{I_{in} \cdot \sqrt{\frac{L_r}{C_r}}}{n \cdot V_o} \right)$$

$$Duty \equiv (PWM) + 2 \cdot \frac{\gamma}{(\omega_o \cdot T_s)}$$

MathCAD Solution

$$\text{Find}(V_o, Duty, \varepsilon, \gamma, PWM) \text{ float}, 5 \rightarrow \begin{pmatrix} -15000. & 15000. \\ 1.7519 & .24808 \\ -20.580 & 20.580 \\ -.33005 & .33005 \\ 1.7613 & .23875 \end{pmatrix}$$

Figure 5.3: Results of steady state analysis using MathCAD

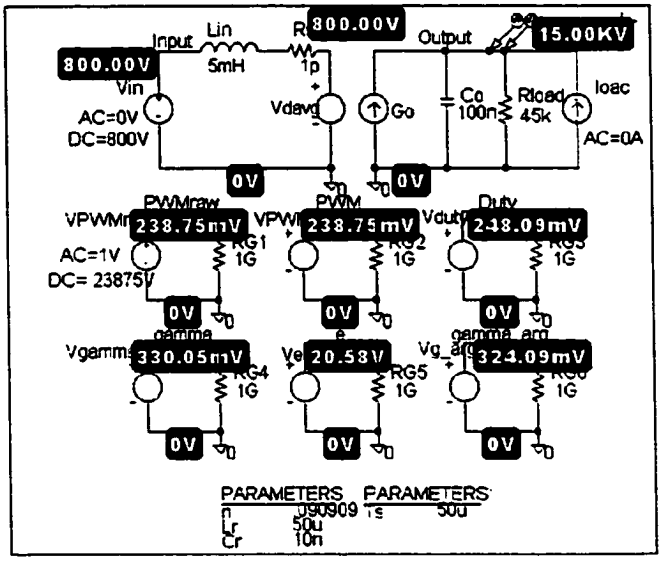


Figure 5.4: Average model for DC and AC Simulations, $Q=Q_{base}$

5.3 Small Signal Analysis and Closed Loop Design

Small-signal analysis forms the basis for effective control loop design. Before discussing the small-signal characteristics, it is necessary to go over the circuit that will deliver the control signal to the bridge. The development here uses a control method that delivers a single control signal to the bridge to allow for the necessary switch conduction overlap as well as adjust the phase shift to regulate the output. In this section, the development will discuss the circuit used to provide these functions. Next, the average model will be used to develop the small-signal characteristics of the converter. These small-signal characteristics are used to develop the closed loop design for the operating range chosen in Section 4.7. The derived model is then validated by simulating a step load transient with both the both the actual circuit and the derived model under the same closed loop control.

The PWM control input, shown in Figures 5.1-5.2, is used to establish switch timing and spans Modes I-II duration. Although, it is desirable to control β for regulation, it is more reasonable to control $\alpha+\beta$. This is because α has a variable duration that is a function of the load and can end before switch turn off. Therefore, β is not strictly a function of switch gating, while $\alpha+\beta$ is distinctly the time between S_3 and S_2 turn on times. Figure 5.6 (a) and (b) show the PSPICE power stage and feedback control circuits, respectively.

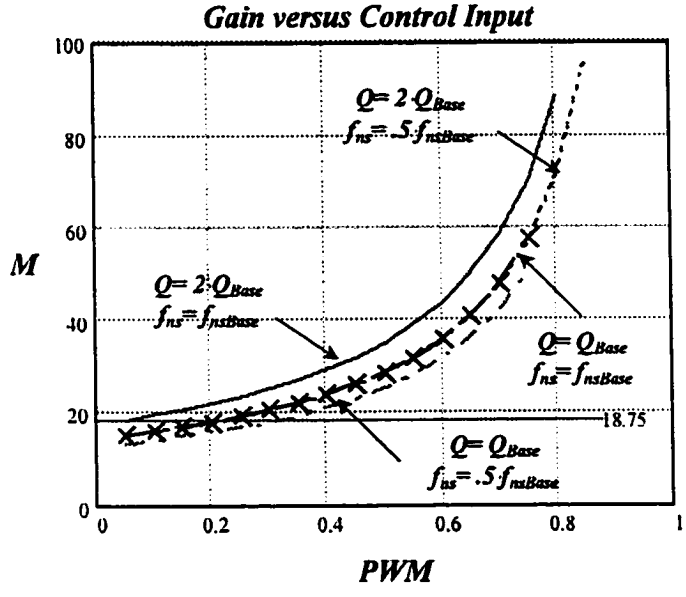
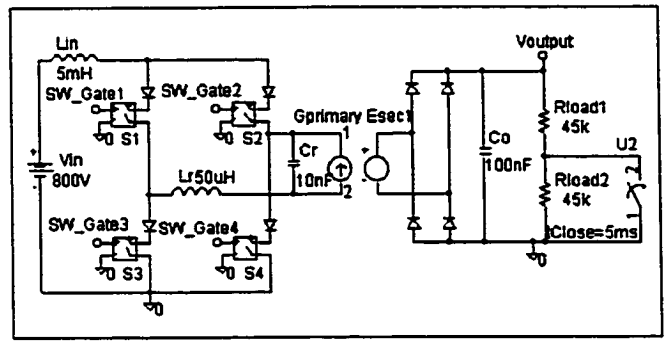


Figure 5.5: Gain, M, versus control input, PWM



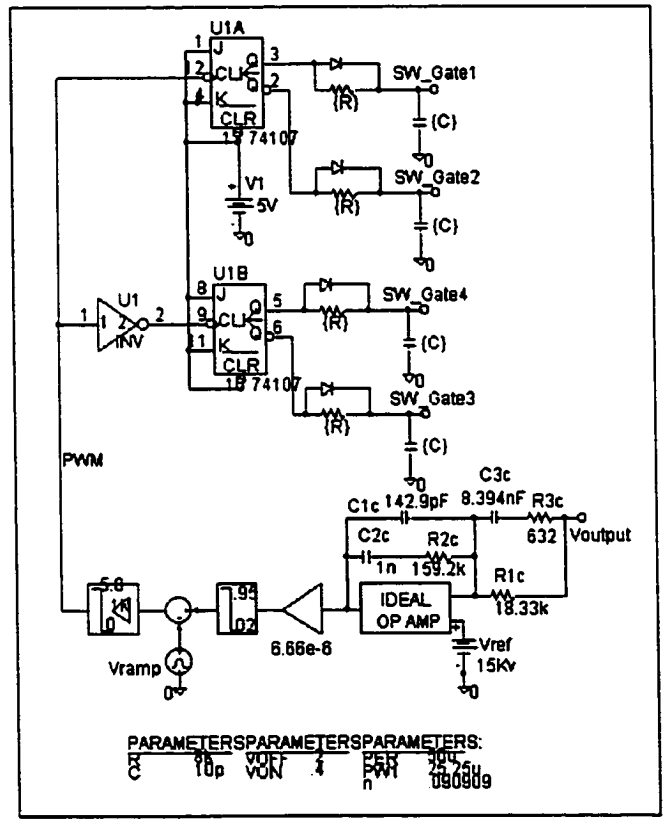


Figure 5.6: Actual circuit for transient simulations (a) the power stage (b) controller and gate drive

Figure 5.6 (b) shows a control scheme is implemented which allows a single control signal to generate gating signals for all four primary switches. PWM's period is half the switching period and its pulse width controls $\alpha+\beta$ duration.

This scheme makes use of negative-edge triggered, J-K Flip-Flops, U1A and U1B, to generate the complementary drive signals and the relative phase shift between upper and lower switches. The RC network on the flip-flop output is used to set a fixed overlap time for both the upper and lower switch sets.

To begin the discussion we assume the both flip-flops begin with the Q output high at t_0. Referring to the waveforms of Figures 5.1-5.2, when the PWM signal goes low at t_2, flip-flop U1A changes state, forward biasing the diode and sending the drive signal to S_2 without delay. At this same time, the Q output of U1A goes low, reverse biasing the upper diode. The time required for the SW_Gate1 node voltage to fall below the switch gate threshold can be controlled by appropriate selection of the RC time constant. By using this method, switch overlap time is held constant for the S_1/S_2 switch pair as either switch's turn off time follows the lateral switch's turn on time by a fixed interval. The same strategy is used for the lower switches S_3/S_4. The phase shift between the upper and lower switch pairs is achieved by sending an inverted version of PWM, PWMBAR, to flip-flop U1B.

In order to design an appropriate controller for the converter, expected operating conditions should be established and the controller design should account for these conditions. For the development here, transient simulations will be performed which take the converter from

half to full load. Referring to Figure 5.5, the curves for $Q=Q_{Base}$ and $Q=2Q_{Base}$ intersect the target gain line (M=18.75) at the two design operating points. The small-signal analysis will concentrate on the converter's dynamic response at these steady state operating points.

With this information, the average model of Figure 5.4 is first validated by a comparison to the steady-state solution from Figure 5.3. In Figure 5.4, the bias point solution, with $Q=Q_{Base}$, is shown superimposed on the schematic diagram. Note that the model yields perfect agreement with the steady-state analysis results, Figure 5.3.

Having validated the DC response of the model, it will be used to perform the small-signal analysis. This analysis is directly performed by PSPICE via AC Sweep. Small-signal characteristic curves for control-to-output, input-to-output, and output impedance are produced by the injection of an AC component into the ports of interest one at a time, as shown in Figure 5.7-5.9 for $Q=Q_{Base}$. Inspection of the characteristic control curves, Figures 5.7-5.9, shows the FB-ZCS converter is very boost-like, particularly when operated in CCM. The RHP zero is apparent here, causing 270° of phase lag and a relatively high filter pole frequency.

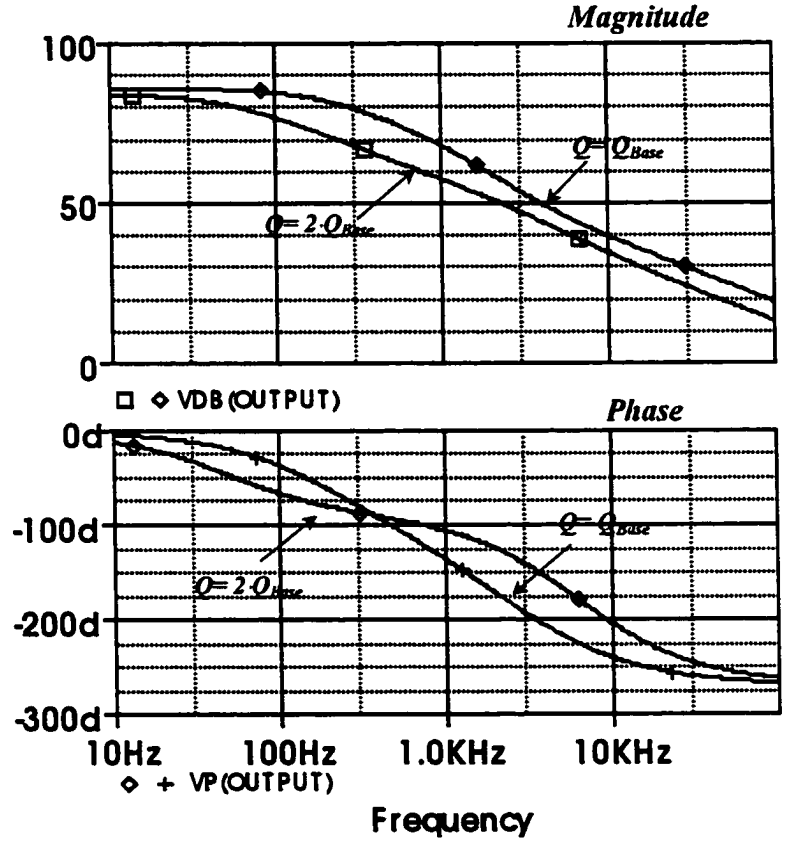


Figure 5.7: Small-signal characteristics (magnitude and phase), control-to-output

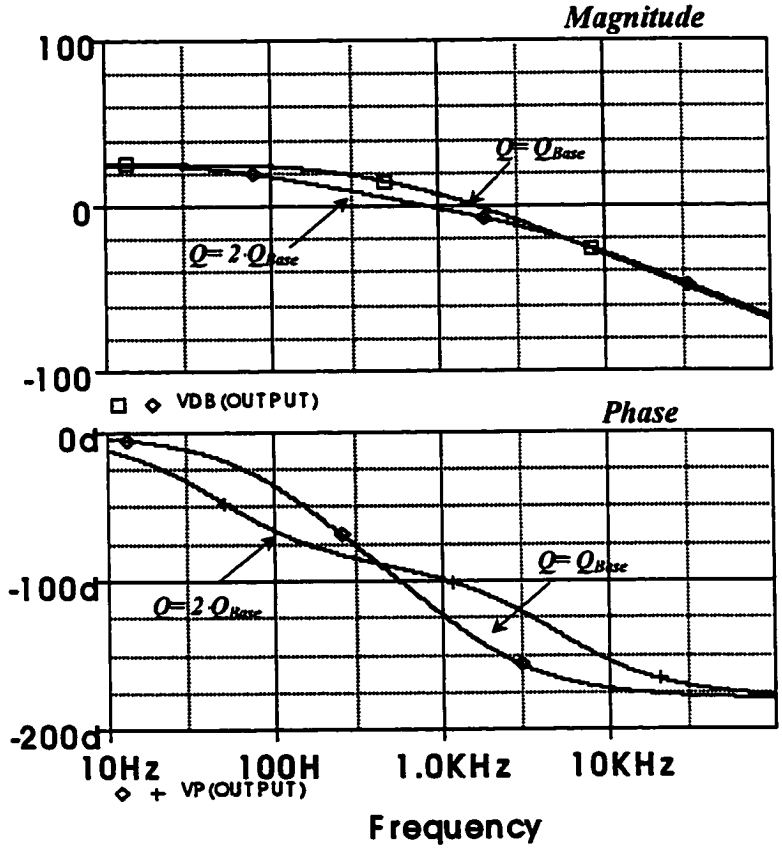


Figure 5.8: Small-signal characteristics (magnitude and phase), input-to-output

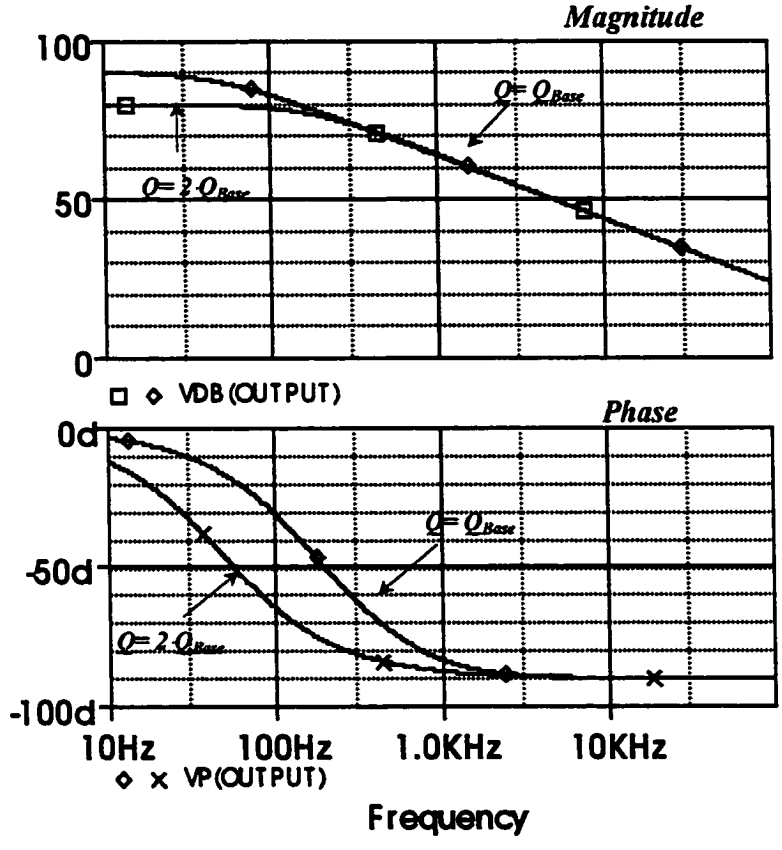
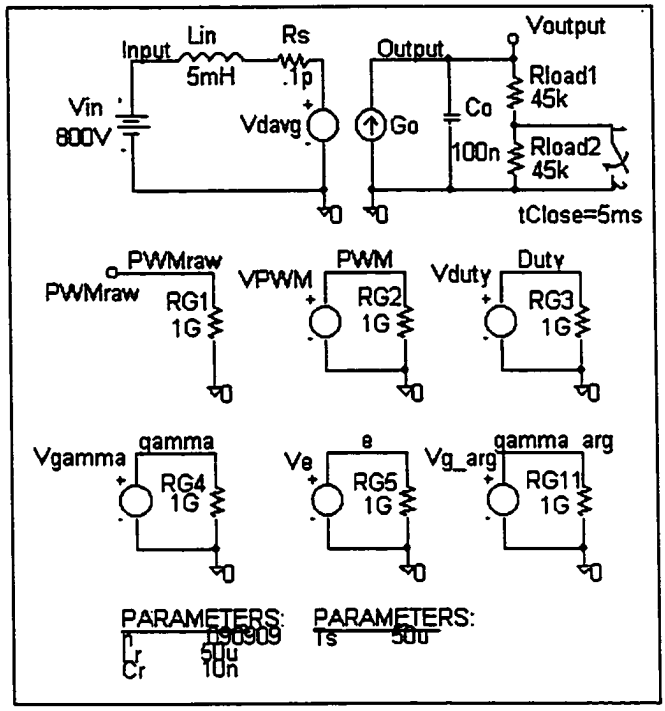


Figure 5.9: Small-signal characteristics (magnitude and phase), output impedance

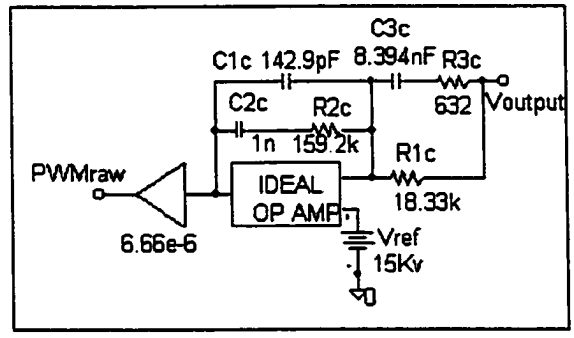
For small-signal characteristics of this sort, conventional compensation techniques would include current-mode control for fast response. For the development here, a single voltage-mode controller is used as the intent is not to design optimized control schemes but to validate the accuracy of the power stage model. As such, a slow-acting loop will be employed to exacerbate the transient response of the converter and thus aid in the comparative study. The design of the controller accounts for stability at both operating points in anticipation of the step load changes performed in the transient simulations.

5.4 Transient Analysis

Based on the derived small-signal characteristic curves, a controller shown in Figure 5.7 (b) is designed. This controller will be used for transient simulations with both the average model and the actual, switched circuit. The average circuit model for the actual circuit of Figure 5.6 is shown in Figure 5.10. A load transient from 50% to 100% full load is simulated at t=5ms by turning on the load switch. Results from the transient simulation from both the actual, switched circuit and the average model, under the same closed loop control, are shown superimposed in Figure 5.11. Results show total agreement, with the average model closely tracking those of the actual circuit.



(a)



(b)

Figure 5.10: Average model for transient simulations (a) average model of the power stage (b) controller

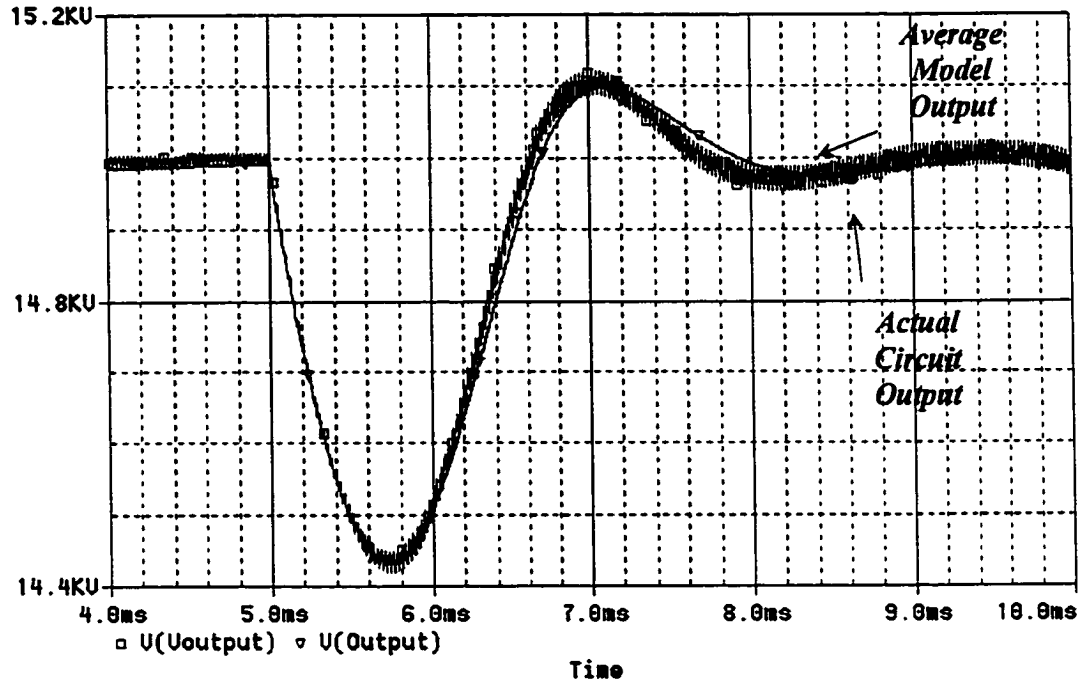


Figure 5.11: Transient simulation results, step load change from 50% to 100%

5.5 Evaluation of Dynamic Model of FB-ZCS

This previous development presents a small and large signal study of the given FB-ZCS PWM converter used in high-power, high-voltage DC applications. The presented development used to study the characteristics of the given FB-ZCS converter presents a simple and methodical approach to converter analysis via an average model. The approach is straightforward and applicable to virtually any topology. Simulation results for the FB-ZCS converter show the feasibility of the proposed topology in high-voltage, DC applications, validate the steady-state analysis, and verify the derived model. Validation of

the derived model is based on a comparison of DC, small-signal, and large-signal simulation results to those obtained from the simulation of the actual circuit.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions and Summary

A unified approach to high frequency PWM converter average modeling has been developed. The approach exploits the mathematical property that the derivative of the average of a time varying quantity is equal to the average of the derivative of that quantity. Using this property allows for a more uniform methodology than conventional methods.

In Chapter 1, conventional modeling and analysis techniques are reviewed. Application of these conventional techniques are demonstrated in order to highlight the limitations and inefficiencies involved with their methodology. These shortcomings become the focus of the development of the unified approach developed in Chapter 2.

In Chapter 2, the unified approach is developed, applied, and the derived models are tested by simulation and lab experiments using the actual, switched circuit. The chapter begins with a presentation of the underlying mathematical principles involved in the unified approach. It continues by applying this approach to the classic boost and a single stage, single switch PWM converter to develop average models. The derived models results match those obtained by actual circuit simulation and lab experiment.

The unified approach presented incorporates additional functionality and accuracy over many of the techniques published in open literature [2,6,7]. The models derived here make

the transition from Continuous Conduction Mode to Discontinuous Conduction Mode seamlessly, reflect no order reduction, and remain as close to natural circuit operation as possible.

The dissertation discussed the implementation of the models in PSPICE and gives details on how custom devices can be created to streamline the modeling process. The development also utilizes MathCAD to validate modeling equations and determine the converter's nominal operating point.

The dissertation continues with simulation results that validate the proposed modeling approach. The models derived are compared to the actual circuit as well as other averaged models to baseline performance. Further, simulations results from both the actual and average model circuits agree will with experimental data. Overall agreement is very good and simulation times are drastically reduced as compared to simulations of the actual circuit.

In particular, Figure 2.25 shows a comparison of the boost converter's small-signal characteristics as obtained from state-space averaging, the Vorperian average model, and the model derived be the unified approach. This comparison shows excellent agreement at low frequencies and an improvement in accuracy over the results from state-space averaging at high frequencies. Further studies with the separated switch topology of Figure 2.32 also show excellent agreement as indicated in Figures 2.39-2.41 and 2.45-2.47 where

simulated results with the new average model closely match those from actual circuit simulation and experimental results.

Chapter 3 investigates the incorporation of conduction loss modeling in model development. Several existing loss modeling techniques are reviewed and evaluated. After evaluating existing strategies, Chapter 3 presents additional concepts: Energy Equivalence and Waveform Correction. These concepts are then applied to the average model to incorporate conduction loss. Detailed evaluations of the strategies are performed including transient simulation and tabular loss comparison. After settling on the Waveform Correction approach, the conduction loss prediction is incorporated in the separated switch topology model of Figure 2.34 as Figure 3.49. Comparisons to actual circuit simulations and loss data obtained from an experimental prototype show that the average model with the loss modeling can predict conduction losses with +/-10% accuracy.

While Chapters 2 and 3 focus on hard-switching, PWM converters, Chapters 4 and 5 apply the presented methodology to a soft-switching topology known as the Full Bridge ZCS converter. Since waveform averaging is the core of the new methodology, it is necessary to show the approach is equally valid with highly nonlinear waveshapes. Simulation results shown in Chapters 4 and 5 that the new approach can accurately model soft-switching converters. Further, the chose of target topology employing phase-shift control presents no difficulty to the unified approach.

Results show the unified modeling approach has accomplished the its objectives. It is easily derived by a methodical approach, it simulates accurately and quickly, and it produces models that can work equally well in CCM and DCM. It can incorporate nonidealites with reasonable accuracy, can be applied to soft-switching topologies, and can work with control schemes outside the standard voltage-mode, duty ratio control.

Overall the dissertation presents a modeling approach that is a logical first step in the design process. While not a substitute for actual circuit simulation or experimental prototyping, it is a accurate and efficient method for topology evaluation and preliminary converter design. As it is more widely applicable, the unified approach presented is more suited to the research and development environment than approaches based on cellular equivalents.

6.2 Future Work

Future work will focus on control loop design and the expansion and refinement of loss modeling. Specifically, future work would include an expansion of the unified approach to include automatic and optimal controller design, would incorporate switching loss models and would refine the conduction loss models presented in Chapter 3. While the unified approach, in its present state, shows experimentally and theoretically justifiable results, it does not produce a present any new means of controller derivation nor does its predict

switching losses. Further, while its prediction of conduction losses is close, additional refinements in the model can result in greater accuracy.

Regarding controller design, the unified approach provides an efficient method of producing a converters small-signal characteristics, the basis of controller design. This represents a significant contribution when one considers the traditional approaches. However, once these characteristics are derived, the designer is still left with the task of designing a tailored controller. This portion of the design process, at present, remains manual. Although computers aid in the development of the controller, the task is often trial and error and relies on the designers skill in loop compensation. Further, results from these efforts often result in acceptable but non-optimal controllers. As a part of future work, the unified approach will be augmented to produce an optimal controller as a part of the modeling process and possible fully automate that process.

The unified approach can be expanded to include switching losses. Preliminary results on switching loss modeling by Erikson [44] show promising results. While not incorporated in the unified approach, the extension to include these loss mechanisms should be possible.

And finally, the conduction loss model developed as a part of the unified approach makes several simplifying assumptions about waveshape deformation due to on state resistance. These assumptions reduced the difficulty of model derivation at the expense of accuracy. If the particular application requires addition accuracy, a more detailed treatment of the waveshape deformation may be required.

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