CONTROL AND TOPOLOGY IMPROVEMENTS IN HALF-BRIDGE DC-DC CONVERTERS

By

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ABSTRACT

Efficiency and transient response are two key requirements for DC-DC converters. Topology and control are two key topics in this dissertation. A variety of techniques for DC-DC converter performance improvement are presented in this work.

Focusing on the efficiency issue, a variety of clamping techniques including both active and passive methods are presented after the ringing issues in DC-DC converters are investigated. By presenting the clamping techniques, a big variety of energy management concepts are introduced. The active bridge-capacitor tank clamping and FET-diode-capacitor tank clamping are close ideas, which transfer the leakage inductor energy to clamping capacitor to prevent oscillation between leakage inductor and junction capacitor of MOSFETs. The two-FET-clamping tank employs two MOSFETs to freewheeling the leakage current when the main MOSFETs of the half-bridge are both off. Driving voltage variation on the secondary side Synchronous Rectifier (SR) MOSFETs in self-driven circuit due to input voltage variation in bus converter applications is also investigated. One solution with a variety of derivations is proposed using zerner-capacitor combination to clamping the voltage while maintaining reasonable power losses.

Another efficiency improvement idea comes from phase-shift concept in DC-DC converters. By employing phase-shift scheme, the primary side and the secondary side two MOSFETs have complementary driving signals respectively, which allow the MOSFET to be turned on with Zero Voltage Switching (ZVS). Simulation verified the feasibility of the proposed phase-shifted DC-DC converter.

From the control scheme point of view, a novel peak current mode control concept for half-bridge topologies is presented. Aiming at compensating the imbalanced voltage due to peak current mode control in symmetric half-bridge topologies, an additional voltage compensation loop is used to bring the half-bridge capacitor voltage back to balance. In the proposed solutions, one scheme is applied on symmetric half-bridge topology and the other one is applied on Duty-cycle-shifted (DCS) half-bridge topology. Both schemes employ simple circuitry and are suitable for integration. Loop stability issues are also investigated in this work. Modeling work shows the uncompensated half-bridge topology cannot be stabilized under all conditions and the additional compensation loop helps to prevent the voltage imbalance effectively.

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Songquan Deng

October 2005

To my wife - YujingYang

To my parents – Qijing Deng

Zhenrong Lee

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1. INTRODUCTION

1.1 Research background and motivation

One of today's power supply design challenges is creating multiple-output Direct Current to Direct Current (DC-DC) converters with tight regulation on multiple low-voltage outputs connected to high slew rate dynamic loads. New generations of power supply architectures and specialized Pulse-Width-Modulation (PWM) controllers are emerging to meet these demands [A1]. Two application areas having very separate challenges in the past are beginning to converge: the 12V desktop power supply and the 48V telecom power supply. Both of these applications present unique challenges that are shaping the future of the power topologies and the power control technology used in modern DC-DC converters.

At the heart of communication systems and Desktop PCs are advanced microprocessors and a high-speed communication Application-Specific Integrated Circuit (ASIC) designed in deep sub-micron, low-voltage Metal Oxide Semiconductor (CMOS) logic technologies. Operating at GHz clock frequencies and supplying large currents (over 60A) on multiple tightly regulated, low-voltage supply rails (sub-2Vdc), presents major challenges to the DC-DC power conversion system [A2][A3]. In order to protect the expensive system chips from potentially destructive power conditions, multiple supply rails must be sequenced on-and-off in a prescribed order and ramped up and down within a finite amount of time and minimal overshoot beyond the desired output level.

New power supply topologies are emerging to meet the power conversion challenges of modern computing and communication systems. In communication systems, traditional 48V isolated power supply topologies (single-ended forward and flyback regulators) are yielding the way to higher power topologies (push-pull, half-bridge and full-bridge) [A4]. Also, new hybrid topologies, such as cascaded regulators, are emerging [A5][A6]. In computer systems, traditional non-isolated PC power supply topologies (multiphase buck regulators) are yielding the way to isolated power conversion topologies that take advantage of the transformer turns-ratio to create multiple low-voltage outputs in one conversion step to provide the many low-voltage rails required by advanced microprocessors [A7]. These ever changing power supply considerations create fresh opportunities for PWM control Integrated Circuit (IC) designers to match new process technologies with unique power integrated circuit design techniques to develop the next generation power system requirements.

A reversal in the roles of the traditional distributed power conversion architectures is emerging between computer and communication systems. Desktop PC power architectures are being proposed with developing multiple low-voltage supply rails from a 48V bus rather than a 12V distributed bus [A8]. This allows reducing the distribution losses expected with the ever-increasing power appetite of next generation processors. Conversely, telecom power architects are just now launching a new DC-DC modules to convert the 48V bus to a 12V distributed bus [A9] so they can take advantage of the vast array of point-of-load power controllers available on the market today. Some high-end workstation and server systems already use a 48V distributed power conversion system that maintains proper regulation while supplying very high load currents. Due to

the difficulty in achieving tight regulation on supplies with ever decreasing load voltages and geometrically increasing load currents, a 48V distributed power system is now being considered to replace the traditional 12V bus in desktop PC power supplies.

1.1.1 Centralized Power System (CPS)

The term “centralized power” originated in early 1980’s when a typical Alternating Current to Direct Current (AC-DC) power supply came packed in a silver-box chassis with an AC line cord on one side and a DC cable harness extending out the other side of the chassis for mating with a system power connector [A10]. Multiple DC voltages (typically +12V, +/-5V, +3.3V) were provided through the connector to the Printed Circuit Board (PCB) power planes [A11]. Advanced sub-micron CMOS technology emerged in the early 1990’s changing the power supply requirements from traditional +5Vdc and +3.3V supplies to multiple non-standard low-voltage supplies (2.5V, 1.8V, 1.2V, etc.) with high load currents being demanded by advanced microprocessors and ASICs.

1.1.2 Distributed Power System (DPS)

A combination of high slew-rate load currents and tight regulation specifications for very low-voltage outputs gave rise to usage of “distributed power” with point of load converters [A12-A16]. In a distributed power system, a single intermediate voltage (typically 12V or 48V) is generated by an offline AC-DC supply and converted to lower

voltages with a DC-DC regulator located on the motherboard closer to the point of the loading. The close proximity of the DC-DC regulator to the high slew-rate load reduces distribution impedances permitting more precise and easier to control regulation. Reduced parasitic elements in the control loop, lower voltage drop across the PCB power planes and a cost savings for distribution cables and connectors are obtained.

Several basic DPS structures can be identified according to the way the power processing functions are distributed among several different Power Processing Units (PPUs).

1. Paralleling structure:

Paralleling [A18-A19] has been widely used in many power supply systems and is often referred to as a modular power supply system. The characteristics of paralleling include:

Good thermal management: Since each module handles only one part of the total power, the more modules in paralleling, the less power dissipated in each module.

High reliability: Since the power processed by each module decreased, and even though the system has more components, the overall reliability is improved. The n+1 redundancy helps to build highly reliable DPS systems.

Modularity and maintainability: The paralleling structure simplifies the power system design. For higher power requirement, simply put more modules in parallel. The design for each module can be standardized. On-line replacement makes maintenances even easier.

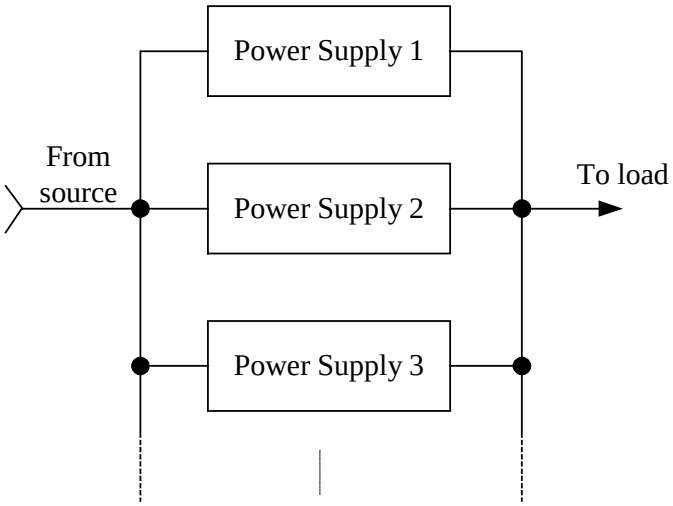


Fig. 1.1 Parallel modules

2. Cascading structure:

Cascading structure [A17] [A21] is generally applied in DPS. It has the following characteristics:

Point-Of-Load (POL) regulation: Since the power supply is placed as close as possible to the load, the parasitic is significantly reduced and fast transient response is obtained as a result.

High efficiency: Higher mid-bus voltage reduces the losses on the traces, which greatly improves the system efficiency.

Wide line variation: Cascading connection has good response to wide line variation due to the cascading structure.

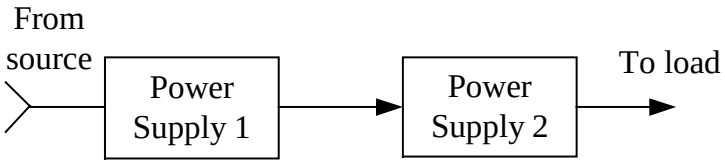


Fig. 1.2 Cascading structure

3. Source splitting structure:

Source splitting [A17] is used when different available sources such as battery backup, which is most commonly used to provide temporary power when primary power fails. It is also used to achieve redundancy for highly reliable power systems.

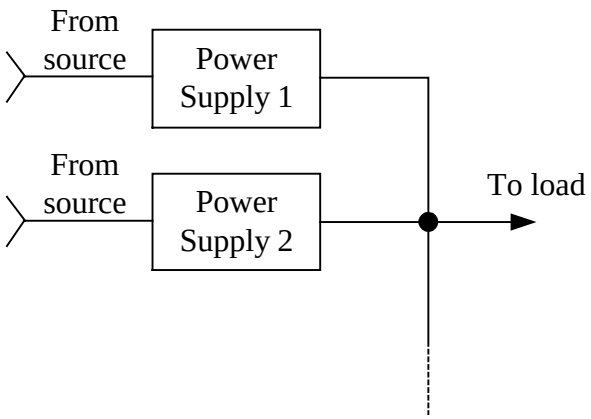


Fig. 1.3 Source splitting

4. Load splitting structure:

Load splitting [A17] is employed due to the following considerations:

Distributed load: For physical reasons, the loads are distributed in significant distance. A DPS with an intermediate bus is a natural solution. Each load has its own power supply module placed as close as possible to reduce the power loss on the traces. The regulation is solved as well since the converter is in close proximity to each load.

Noise considerations: For a DPS with common bus, the noise coupling occurs between loads. The load-splitting technique introduces two load converters between any two loads with their associate filter to attenuate the noise.

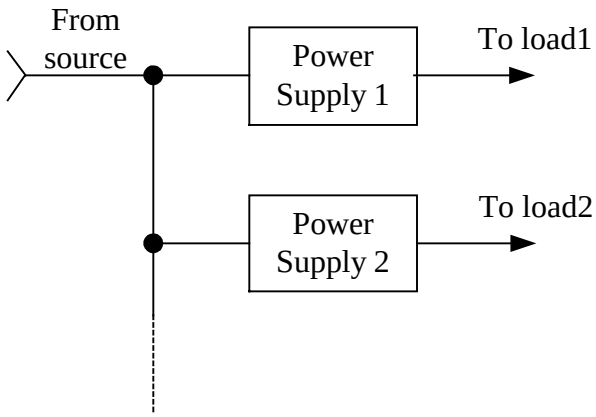


Fig. 1.4 Load splitting

1.1.3. DPS architectures

There exist two fundamental DPS architectures with the difference of the bus voltage, that is, the DC-bus and AC-bus. They consist of a variety of combinations of the four DPS structures.

DC-bus architecture vs. AC-bus architecture:

The DC-bus architecture [A21] block diagram is illustrated in Fig. 1.5.

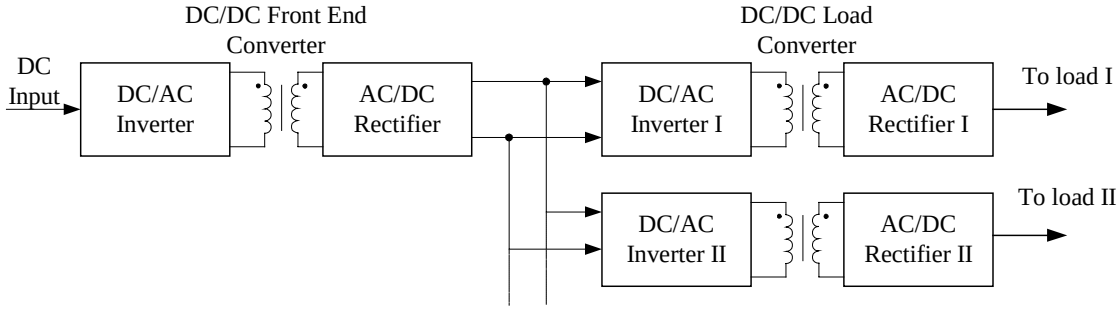


Fig. 1.5 DC architecture block diagram

In the DC-bus architecture, two DC-DC conversions are performed, that is, the front end DC-DC conversion and the load DC-DC conversion, which hurts system efficiency. The AC-architecture [A22], which is shown in Fig. 1.6, seems less complicated, since only one DC-DC conversion is performed and higher efficiency is expected. However, AC-bus structure has limited implementations. First, the AC bus brings Electromagnetic Interference (EMI) issues and special cables such as shielded or flat cables, and must be used to reduce the noise, which increases the cost. The skin effect from the AC bus increases the power losses especially at high switching frequency. For low frequency systems, bulky filter is required, which also increases the system cost. Furthermore, the AC voltage rectification injects current harmonics to the AC bus and hurts the power factor. As a result, DC-bus architecture has gained increased popularity and has become more and more mature due to the low noise and low power loss on the DC bus. The modularity of the DC-DC converter gains the DC-bus architecture wide acceptance and cost effective implementation in telecom and computing power supply systems.

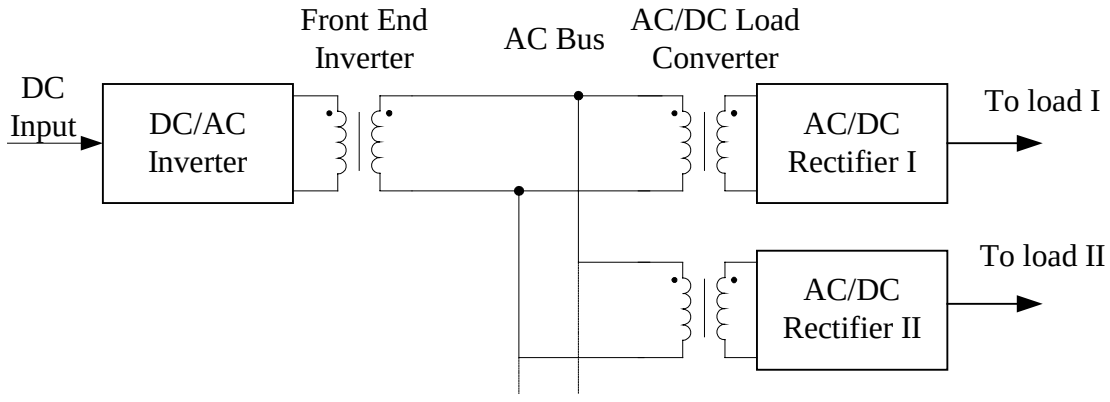


Fig. 1.6 AC bus architecture block diagram

The main work of this dissertation focuses on the on-board DC-DC converter power module in the DC-bus architecture of DPS.

Issues in power module:

A. Efficiency:

Efficiency is one of the key specifications for the overall performance of the converters. Excessive heating and heat transport, i.e., thermal management, is probably the most important parameter in the system design since it has a direct impact on the system reliability and available performance. The power module, as well as the power board, account for 10-20% of the heat. It is important to state that, the efficiency is high not only at max load, but also over the whole or at least main part of the load range. Another parameter that could be important is the idling power, i.e., input power at no load conditions, especially in telecom battery operated equipments where normally many functions are inactivated. Synchronous rectification should substantially increase the efficiency once suitable semiconductor devices and circuit techniques are developed. To achieve small size of point-of-load converters, high-frequency DC-DC converter designs must be employed. New converter technologies should be explored to combine low switching losses with low device voltage and current stresses. Semiconductor and magnetic devices should be improved to meet challenges of high-frequency, high-density on-board converters.

B. Power density and packaging:

One of the most advertised parameters today is the power density. Very high figures in excess of 50 W/in^3 have been announced for high power DC-DC power modules. However, the physical laws give a relationship between the temperature rise,

power dissipation and the thermal resistance, i.e. the thermal conductivity and the effective cooling surface area, which in practice means that additional heat sinks and forced cooling have to be used, or that the output power has to be derated substantially, at these power densities. New packaging techniques need to be developed to allow increase of the power density of on-board converters. High-voltage integrated circuit technology must be employed to improve electrical performance and power density. Hybrid thick-film technology or similar techniques will be necessary to achieve the required density and provides adequate thermal management.

C. Noise:

Placement of a high-frequency on-board converter in a close proximity to noise-sensitive electronic circuits may cause EMI problems. Extensive research is necessary in this area to provide better understanding of the problem and to develop appropriate design tools and techniques. New circuit techniques must be sought to minimize the EMI generated by the load converters. Innovative packaging and shielding techniques will be necessary to reduce the EMI problems.

D. Safety:

Safety requirements for Information Technology and telecom equipment, including equipment intended to be connected to telecom networks and telecommunication networks are specified in EN60950 as well as CSA-C22.2. In certain applications there are requirements of electrical separation between the input and output of DC-DC converters. As specified in EN60950, there is a requirement of 1500Vdc or 100Vac electrical separation between the telecommunication network and parts and circuitry that can be touched by the test finger. The 1500 Vdc is required because there is

a risk of high voltage transients due to lightning interference in the telecommunication network and in the bonding network in smaller remote access nodes. Also, other AC mains disturbances can cause high voltage transients in the bonding network.

E. Cost:

Manufacturing costs (measured in dollars per watt) for distributed-power modules are currently higher than those for centralized power supplies. This may cause an economical barrier in some applications where DPS architecture is desired, but economical considerations are an overriding factor. To make the DPS approach attractive for these applications, the manufacturing costs must be reduced. This can be achieved by extensive standardization of the DPS subsystems and full utilization of the surface-mount technology.

1.2 Dissertation outline

The dissertation consists of eight Chapters. In Chapter 1, the background introduction is carried out focusing on distributed power system. Important issues are discussed for on-board DC-DC converters. Efficiency is the first concern for a highly reliable distributed power system.

In Chapter 2, a review of existing converter topologies is carried out, which gives a general idea of the state-of-the-art work and techniques. Half-bridge is a promising topology for low-voltage high-current on-board DC-DC modules. Focusing on this topology, a variety of research work is done in the following Chapters, aimed at building the half-bridge topology based DC-DC converter with high efficiency and fast transient

response. To design a converter with fast transient response, high bandwidth is required. There generally exists several ways to obtain high bandwidth. The most straightforward solution is to go with high-frequency switching. The switching power supplies have limited bandwidth due to the limited switching frequency, which are limited by the switching losses. The switching losses are meaningful for frequencies higher than 500kHz. Also, high switching frequency and high-current increase the electromagnetic emissions, which creates interference in nearby electronic circuits. Employing control techniques can expand the bandwidth for a given switching frequency. Among the state-of-the-art control techniques, peak current mode control is widely employed which allow converter to have higher bandwidth for given switching frequency.

However, as introduced in Chapter 3, peak current mode control cannot be directly applied on half-bridge topology due to the voltage imbalance problem on the capacitors. A brand new capacitor voltage imbalance correction concept is proposed in Chapter 3, in which the voltage imbalance is detected and compensated. The error information is included in the driving signal, which corrects the voltage imbalance automatically. The novel compensation concept focuses on the control circuitry instead of modifications on power stage. As a result, the designer is free to design the power stage as it is and the converter electrical characteristics are not affected by the voltage imbalance correction. Based on the compensation concept, two control schemes are derived with one scheme for symmetric half-bridge topology and the other one scheme for Duty-Cycle-Shifted (DCS) half-bridge. Both proposed schemes focus on control to correct the capacitor voltage imbalance instead of modifying the power stage and are suitable for integration. For the first control scheme, the proposed compensation circuit

enable peak current mode control to be applied to conventional symmetrical half-bridge. For the second control scheme, the proposed circuit corrects the voltage imbalance and easily generates the DCS driving signal, which makes DCS topology simple for application in DC-DC on-board converters. With the proposed control scheme, DCS topology is now complete for implementation. Following this Chapter, detailed modeling work is demonstrated. The modeling methodology of the capacitor imbalance is different compared with the conventional modeling work since the control variable is the voltage imbalance of the half-bridge capacitors. The modeling results explained why peak current mode control cannot be directly applied on a symmetric half-bridge and the results are also applicable for Duty-Cycle-Shifted (DCS) half-bridge topology, which provides the theoretical understanding of the capacitor voltage imbalance in symmetrical half-bridge topology. The validity of the proposed control schemes is verified as well in the modeling point of view.

To reduce the power losses and improve the converter efficiency, a variety of clamping techniques are proposed in Chapter 4. For the primary side, the active-clamping-tank concept is proposed to manage the power stored in leakage inductor during the freewheeling interval. Three clamping tanks consisting of capacitor, diode and active switch are proposed along with stress analysis, schemes comparisons and practical design considerations. The proposed Two-FET-Clamping tank is suitable for larger duty cycle applications, in which freewheeling time is short. The oscillation caused by the leakage current and junction capacitance is eliminated and ZVS is obtained for both Metal-Oxide Semiconductor Field-effect Transistor (MOSFET)s. For small duty cycle applications, the proposed FET-Diode-Capacitor tank prevents current from freewheeling

through the switch during main MOSFET off-time. As a result, the conduction loss from current freewheeling is significantly reduced since leakage inductor current drops to zero in very short time and the diode blocked the oscillation between the clamp capacitor and the leakage inductance.

The power management concept in the clamping FET-Diode-Capacitor tank employs the clamping capacitor as energy storage so that the ringing in conventional half-bridge during main switch off-interval is not present due to the energy transferring from the leakage inductor to the clamping capacitor. The only disadvantage might be the non-ZVS turn-on of the main switch since the energy stored on the clamping capacitor is not effectively used to discharge the junction capacitor of the main MOSFETs prior to turning on them. In another proposed technique applied on active-clamp DC-DC converters, the energy stored in clamping capacitor is well used to realize the ZVS of the main switch and the freewheeling loss is reduced as well due to the fast charging to the clamping capacitor with the magnetizing energy. On the secondary side of the transformer, a lossless Zener-Capacitor clamping circuit is proposed to stabilize the driving voltage during line change. The proposed technique can be applied on all self-driven topologies with wide input line change, which may have wide applications on telecom power supply systems since the general input line range is from 35V to 75V. Issues in this circuit are also discussed and trade-offs between power loss and voltage stabilization shall be carefully made.

In Chapter 5, a novel phase-shift power delivery concept for the half-bridge topology is proposed. Since the MOSFETs are driven complimentarily for the primary side and secondary side MOSFET pair, the Zero Voltage Switching (ZVS) for the

MOSFET can be easily obtained. One important issue in the phase-shift half-bridge is the reactive power, which may affect efficiency significantly. Important conclusions are drawn from intensive analysis for the bi-directional phase-shift half-bridge DC-DC converter and design suggestions are given as well.

For the efficiency considerations, the power losses in converters are investigated using the proposed power losses estimation platform in Chapter 6. The proposed power losses estimation platform is based on simulation software such as Orcad suite, Maxwell and analysis software such as MathCAD and Microsoft Excel. With the proposed software platform, power losses estimation in any converters can be easily obtained, which gives a clear picture of the losses distribution and the percentage the losses on the key component amount to be. From one example given in Chapter 6 (a full-bridge DC-DC converter), it is illustrated the main losses come from the power MOSFET and the transformer in low-voltage high-current DC-DC converter. For low-voltage rated MOSFET, the driving loss has a relatively larger percentage compared to its high voltage rated counterpart. The efficiency curve comparison is also made for a specified converter between the software estimation and lab experimental results. The difference between them is less than 2 percent, which justifies the accuracy of the platform.

2. KEY APPROACHES TO BUILD ON-BOARD DC-DC CONVERTER WITH HIGH EFFICIENCY AND FAST TRANSIENT RESPONSE

2.1 Topology and control scheme overview

In recent years, there have been many significant technological changes in power supply design. There became possible with advances in power transistors, integrated circuits, capacitors and design techniques. This has resulted in lower cost per watt with improved performance. For the on-board DC-DC converter applications, there generally exist non-isolated and isolated DC-DC on-board converters. A typical non-isolated DC-DC on-board converter is Voltage Regulator Module (VRM) [B1-B7], which has dominant applications in server and workstation computing systems. VRM emerges from the so-called “Point-Of-Load” (POL) power delivery concept. In a computing system, the silver box works as the center unit for power delivery. Due to the parasitics between the silver box and the CPU, POL is proposed to deal with the extremely fast transient response requirement from the CPU. The converter delivers power to the CPU and is placed as close as possible so that the parasitics are not significant enough to degrade the power delivery quality. Buck topology is widely employed in VRM. Since the step down is quite limited due to the degraded performance for small duty cycle, 12V is generally employed as the standard input voltage. With the help of an isolation transformer, the designer has more flexibility to design the isolated on-board DC-DC converters. By

choosing transformer turns ratio, the duty cycle can be optimized to give the best performance of the on-board DC-DC converters. Buck derived topologies have the dominant applications in low-voltage DC-DC area due to their step down feature. The topology includes full-bridge, half-bridge, push-pull and forward.

2.1.1 Full-Bridge topology

The full-bridge topology [B8-B13] is shown in Fig. 2.1.

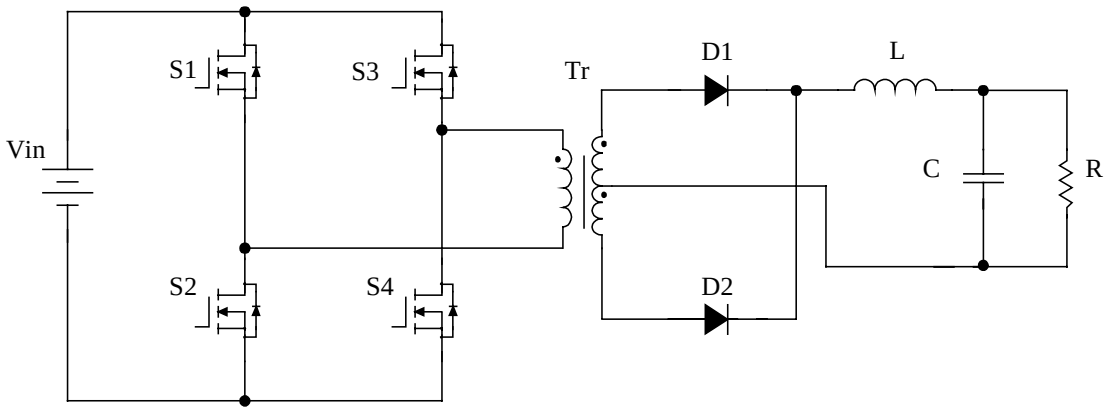


Fig. 2.1 Full-Bridge topology

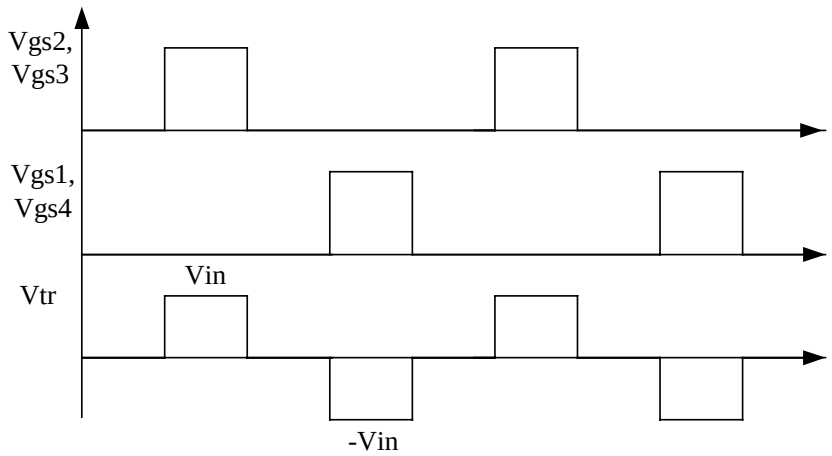


Fig. 2.2 Driving signal

Full-Bridge topology is derived from Buck topology and has popular applications on high power (>500W) converters. Four switches with two in each leg switches alternatively to deliver the power to the load. When S2 and S3 conduct at the same time, Vin is applied to transformer primary winding. The polarity of the voltage applied on primary side winding reverses when S1 and S4 conduct. As a result, transformer core is fully utilized and no core resetting circuit required. Smaller core can be employed for full-bridge topology for given power. To prevent DC bias in the transformer, a capacitor is usually added in series with the transformer winding.

Another topology called Phase-Shift-Controlled Full-Bridge [B12-B16] also has wide applications in high power converters. The only difference is the switching sequence of the four switches as shown in Fig. 2.3. For each leg, the high-side MOSFET and low-side MOSFET have complimentary driving signal with very short dead-time between them. The overlaps between S1, S3 and S2, S4 driving signals are modulated by PWM controller to regulate the converter output. The short dead-time allows MOSFET body diode conduct due to the discharging of the junction capacitance of the MOSFET by the leakage inductor energy to obtain ZVS condition. The switching losses are reduced significantly and ringing between transformer leakage inductance and MOSFET junction capacitance in conventional PWM full-bridge topology is eliminated, which gives good solution for EMI issue. Issues in the topology are found as: a) Freewheeling energy leads to power losses and hurts the efficiency especially at high line input with small duty ratio. b) The lagging leg may more easily lose ZVS due to insufficient energy stored in leakage inductance to discharge the MOSFET junction capacitance.

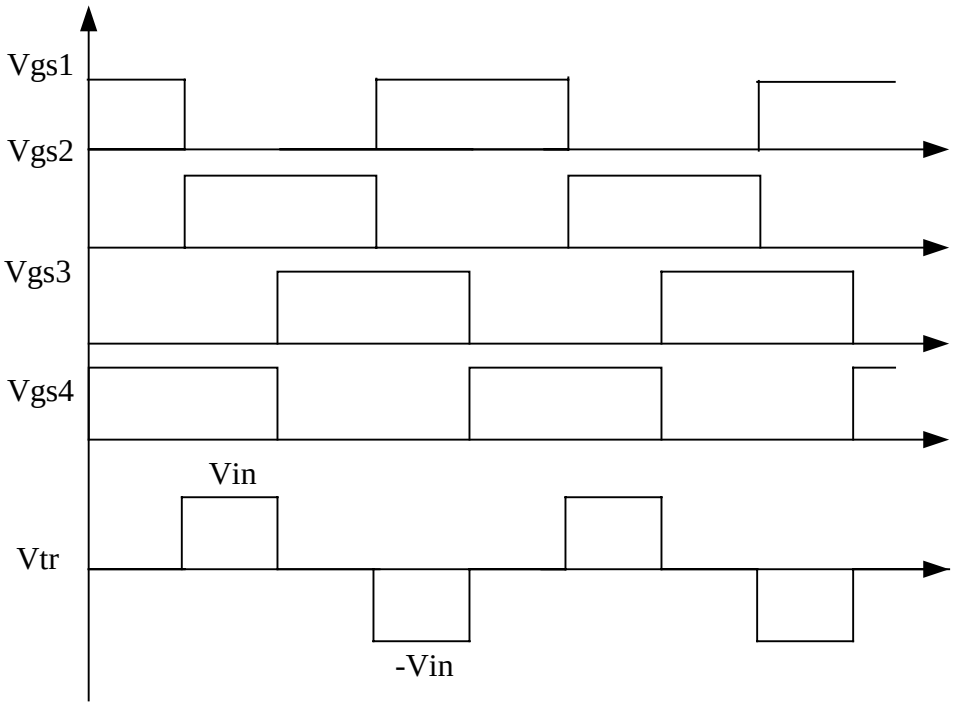


Fig. 2.3 Phase-shift full-bridge driving signal and transformer winding voltage

2.1.2 Half-Bridge topology

The half-bridge topology [B17-B25] is a promising topology for low and medium level power converters.

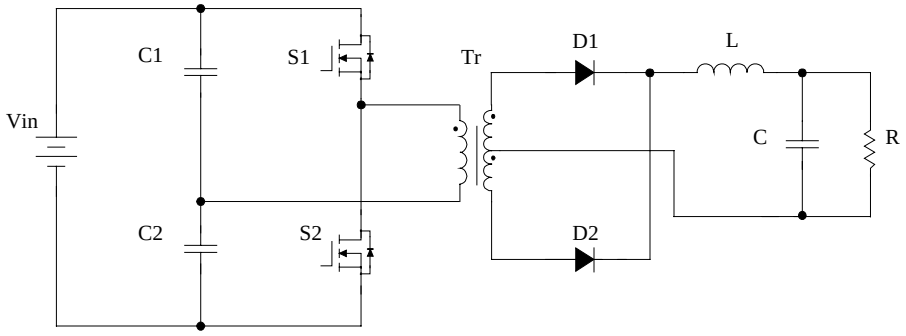


Fig. 2.4. Half-Bridge topology

The two switches connect the single transformer primary across the two capacitors alternately. The primary half-bridge voltages and currents are AC. DC current is not drawn from the center-tap of the input supply. Different with the full-bridge topology, no extra capacitor is needed to eliminate the DC bias in the transformer since the two capacitors automatically correct the mismatch of the switching by changing their voltage. Since two capacitors share the input voltage evenly, the voltage stress for the MOSFET is half of the input voltage compared with the case in full-bridge topology. As a result, lower voltage rated MOSFET is qualified for half-bridge topology application. Two half-bridge topologies are widely used in DC-DC converters, i.e., the symmetric half-bridge topology and the asymmetric half-bridge topology.

2.1.3 Symmetric Half-Bridge topology

The switch driving signals and transformer voltage waveform of the symmetric half-bridge topology [B17][B20][B25] are shown in Fig. 2.5.

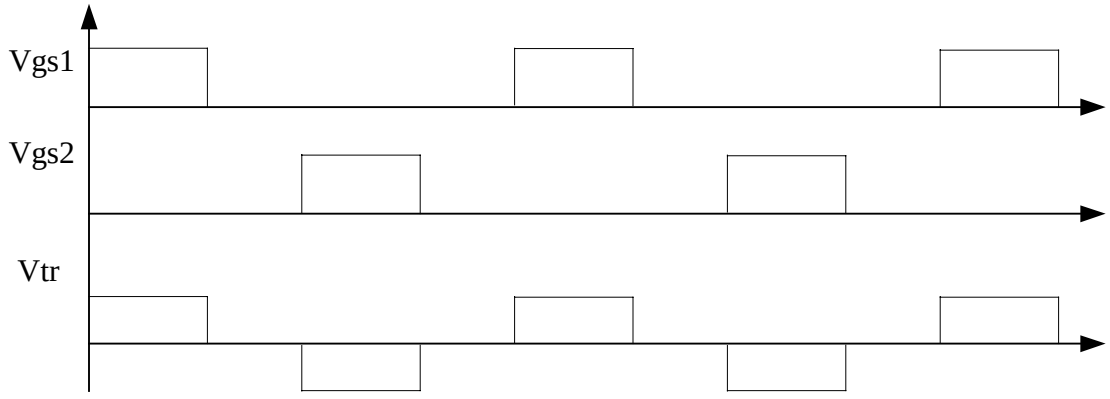


Fig. 2.5. Symmetric Half-Bridge driving waveform

Since the switches are driven symmetrically, all components including the secondary side synchronous rectifier MOSFETs have even stresses. The main drawback of the conventional symmetric half-bridge is that both primary switches in the converter operate with hard switching. Moreover, during the off-time interval of two switches, the oscillation between the transformer leakage inductance and junction capacitance of the switches results in energy dissipation and EMI emissions due to the reverse recovery of MOSFETs body diodes. To suppress the ringing, resistive snubbers are usually added. As a result, energy in the transformer leakage inductance is significantly dissipated in snubbers. Therefore, the symmetric half bridge is not a good candidate for high-switching frequency power conversion.

2.1.4 Asymmetric Half-Bridge topology

The asymmetric (complementary) control was proposed to achieve ZVS operation for half-bridge switches [B21-B24]. Two drive signals are complementarily generated and applied to high-side and low-side switches respectively. Therefore, the two HB switches may be turned on at ZVS conditions, attributing to the fact that the transformer primary current charges and discharges the junction capacitance.

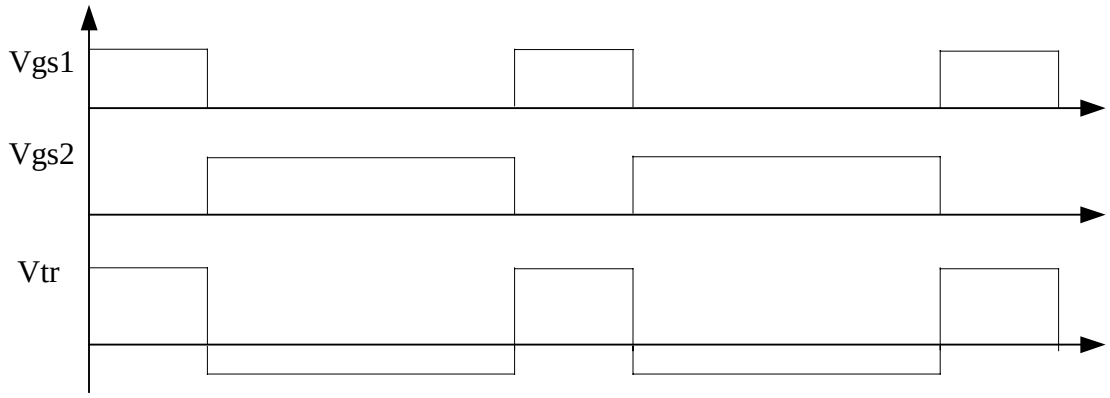


Fig. 2.6 Asymmetric Half-Bridge driving waveform

However, asymmetric stress distribution on the corresponding components may occur due to the asymmetric duty cycle distribution for the two primary switches. In other words, voltage and current stresses on the switches including both the primary side and secondary side MOSFETs are not identical. As a result, diodes or synchronous rectifiers with higher voltage rating are needed at the penalty of degrading the performance and efficiency of the rectifier stage. Furthermore, the DC gain of the converter is nonlinear, thus larger duty cycle variation is observed for the same input voltage variation in comparison with symmetric PWM control scheme. This makes the converter operate further beyond the optimum operating point at high input voltage. Therefore, the complementary (asymmetric) PWM control is more suitable for applications where the input voltage is fixed. As a solution to reduce the duty cycle variation for wide input voltage range, an asymmetric transformer turns ratio together with integrated-magnetic structure, was proposed in literature, such that rectifiers with lower withstanding voltage may be used to improve the performance. However, the power delivery of the transformer and current stresses in the switches and rectifiers are still uneven.

2.1.5 Push-Pull topology

Push-pull topology [B26-B29] is suitable for low input voltage, and it tends to exhibit low primary-side conduction losses, since at any given instant only one switch is connected in series with the DC source. As shown in Fig. 2.7, transistors S1 and S2 are alternately switched on for time period. This subjects the transformer core to an alternating voltage polarity to maximize its usefulness.

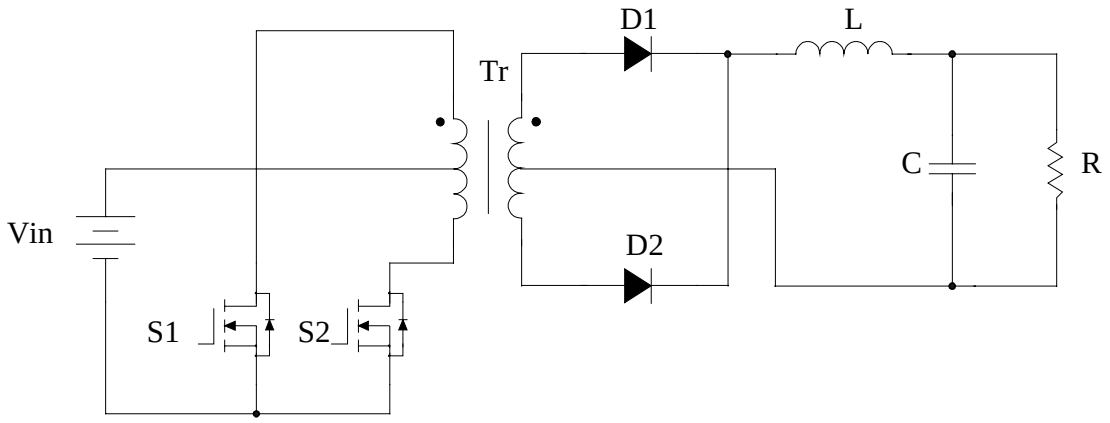


Fig. 2.7. Push-Pull topology

Compared with the other symmetrical converters such as full-bridge and half-bridge, this circuit has the advantage that the transistor switches share a common signal return line so that the driving is relatively easy. Its chief disadvantages are that the transformer center-tap connection complicates the transformer design and the primary windings must be tightly coupled in order to avoid voltage spikes when each transistor is turning off. The push-pull drive automatically provides core reset on alternate half cycles, but these alternate half cycles must be quite symmetrical or the volt-seconds will not cancel, which results in core saturation.

2.1.6 Forward topology

The forward topology [B30-B34] has several versions different in resetting the magnetizing energy.

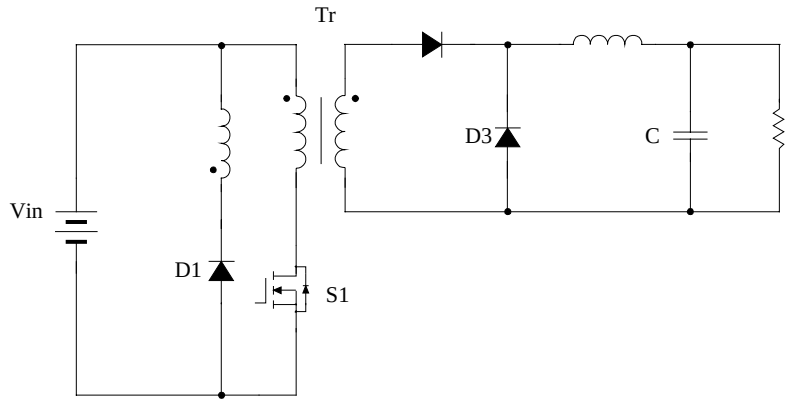


Fig. 2.8. The classical forward topology

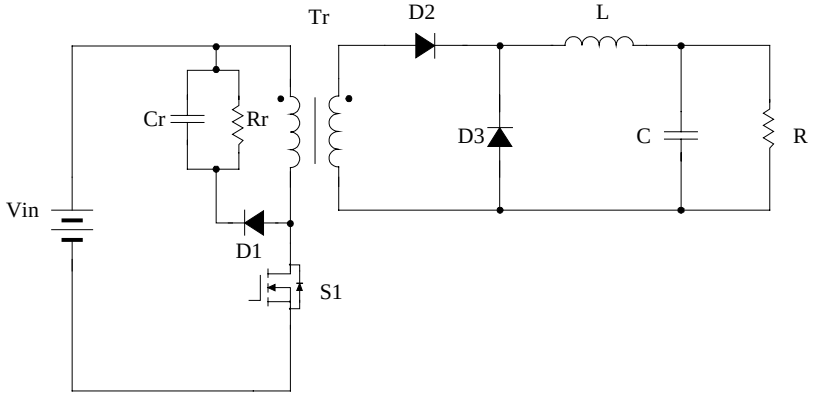


Fig. 2.9. The forward converter with RCD snubber

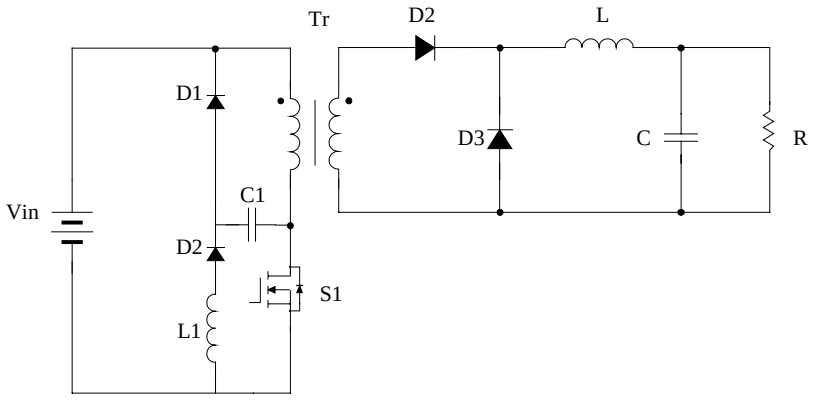


Fig. 2.10. The forward converter with a LCDD snubber

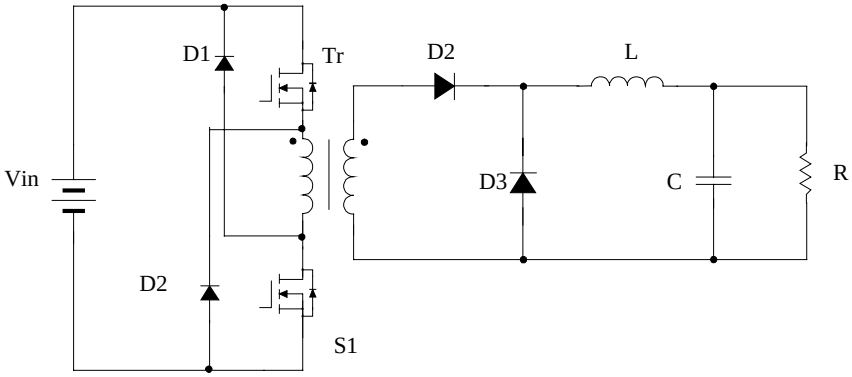
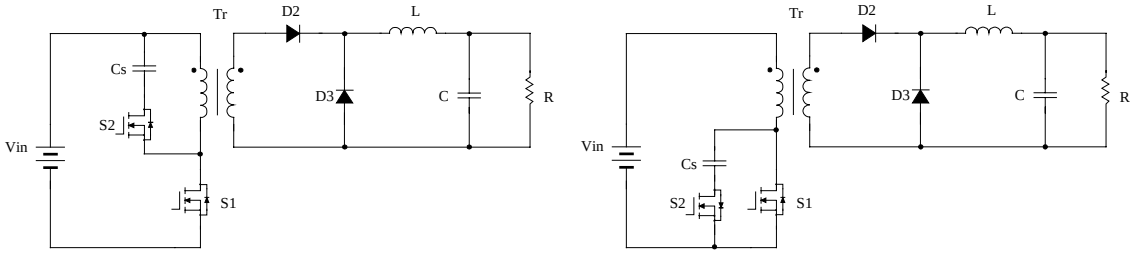


Fig. 2.11. The forward converter with two switches



(a) (b)

Fig. 2.9. Active-clamp Forward topology

A. The classical forward converter:

When switch is on, power is delivered to the load. When switch is off, an auxiliary winding resets the transformer through diode D1. For the same number of turns of the reset winding as the power transformer, which is a common choice, the duty ration is less than 50%. Voltage stress on the MOSFET is typically 2.6*Vinmax*, this is considered high and it limits the performance of the converter, especially when the input voltage is high. Another disadvantage is that the reset winding increases the complexity and hence the cost of the transformer.

B. The forward converter with RCD snubber:

When the switch is on, the main power forwarding is the same as in the classic forward converter. When switch is off, a diode D1 and a capacitor Cr clamp the voltage to a level determined by the input voltage and duty ratio. A resistor R resets the capacitor. The voltage stress on the MOSFET is typically 2*Vinmax.*

C. The forward converter with a LCDD snubber:

It recovers part of the energy dissipated in the previous scheme by the resistor. It uses an inductor, a capacitor and two diodes and is known as LCDD snubber. When the switch is on, the main power forwarding is as the previous forward converter, when the switch is off, a diode and a capacitor clamp the drain-source voltage in the same manner as in the case of a RCD snubber. Reset of the capacitors accomplished through a LC resonance formed by L1, C1 and D1, D2. The voltage stress on the MOSFET is typically 2*Vinmax*. This topology requires excessive design iterations to ensure proper operation over all load, line, and transient conditions due to the resonant features. The size of L1 can be large when the input voltage is high.

D. The forward with two switches:

At turn-off, two diodes connect the primary to the input, but in a reversed polarity resetting the transformer automatically. Because of the clamping, the voltage stress on the MOSFET is typically *Vinmax*. The disadvantage is it needs additional switch and one high side driver.

E. Active-clamp forward:

The operation during the turn-on interval of the main MOSFET is the same as the one before. When the main switch is off, an active device is used to reset the capacitor. The voltage stress on the MOSFET can be designed as low as 1.3*Vinmax*. A significant feature is that, it not only clamps the voltage across the main MOSFET during turn-off, but also provides improved switching condition at turn-on. The key to this soft switching scheme is that the drain-source current can be designed to start with a negative value. Since the current then has to flow in the body diode, the main MOSFET is switched on with virtually zero voltage. Furthermore, zero-voltage switching allows a lossless snubber to be used at turn-off. The auxiliary switch is also switched with zero voltage at turn-on and with a favorable condition at turn-off.

The disadvantage of this topology is that, an additional MOSFET and its associate driver are required. The conduction loss is increased by 30% to 50% due to small magnetizing inductance.

2.2 The relationship between efficiency and transient response

Efficiency and transient response are two critical specifications for on-board DC-DC converters. As mentioned before, high efficiency can reduce the power losses; better thermal management leads to high reliability. Fast transient response enable the converter react quickly to the line change and load change. As a result, the overshoot and under shoot is greatly reduced which reduces the fault risk of the on-board DC-DC converters.

2.2.1 Efficiency concern

Efficiency is defined as the ratio of the total output power to the input power. High efficiency means low power losses in the converter. Therefore, a clear understanding of the power losses in on-board DC-DC converters is very important. Fig. 2.10 shows the power losses distribution for one low-voltage high-current DC-DC converter with half-bridge& current doubler structure.

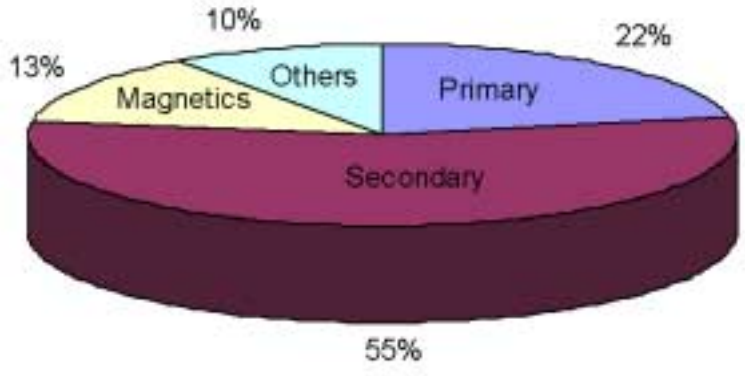


Fig. 2.10 The power losses distribution of one DC-DC converter in one typical low-voltage high-current application

Since secondary side of the transformer has high-current, the losses on the secondary side amount to be the main part. Generally, the power losses in DC-DC converters consist of the following part:

A. Losses in MOSFETs:

- Switching loss.
- Conduction loss (including body diode conduction).
- Driving loss.
- Body diode reverse recovery loss.

Switching loss and driving loss increase when switching frequency goes up. Soft switching techniques such as ZVS, Zero-Current-Switching (ZCS) can reduce the losses significantly. Conduction loss is decided by the current flows through it and the conduction resistance. Synchronous Rectification (SR) techniques replace the diode with MOSFET and is widely used in low-voltage high-current DC-DC converter applications where the body diode voltage drop is significant compared with the low converter output voltage. Connecting MOSFETs in parallel also reduce the conduction loss and is used quite popular in high-current applications.

B. Losses in magnetic components:

- Core loss.
- Copper loss.

Core loss is closely related to the material property and electrical performance of the circuit. Copper loss is related to current and winding trace physical properties, i.e., the trace resistance. When frequency goes up, core loss changes even the voltage-second keeps the same due to the magnetic material properties. The copper loss increases due to

the skin effect, which reduces the effective cross section area of the trace. For inductors, copper loss amounts to be the main part since DC current is relatively high compared with the AC ripple current while for transformers, core loss is larger due to the AC voltage applied on the windings.

2.2.2 Transient response concern.

In the impedance point of view, transient response is the response of the converter when external disturbance applied. Fig. 2.11 shows the DC-DC converter being disturbed by the load current change. The load current with different step rate contains harmonics at all frequency level with different amplitude as shown in Fig. 2.12.

Fig.2.11. DC-DC converter with load transient.

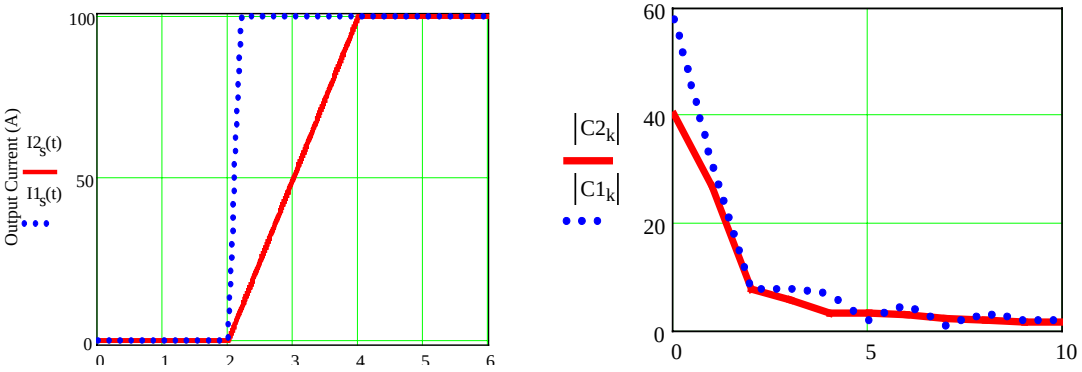
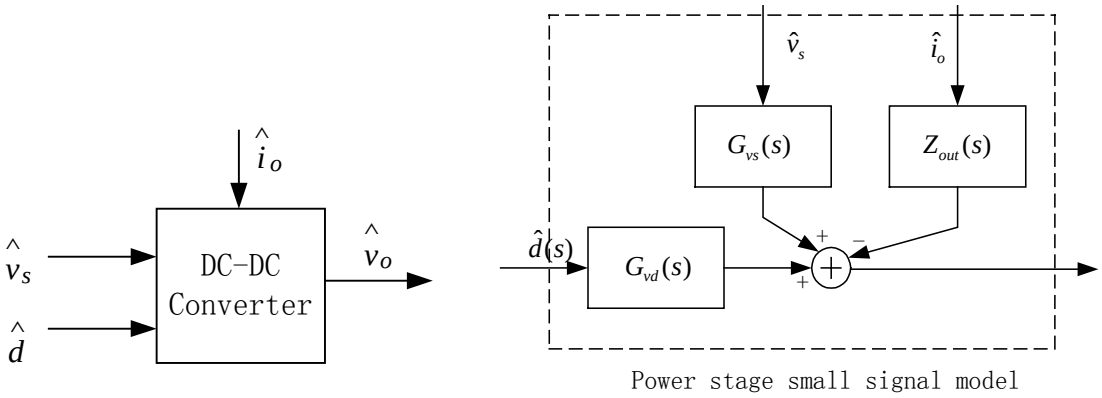


Fig. 2.12. The Fourier component of the transient step current.

The transient response of the converter, i.e., the so called ‘undershoot’ and ‘overshoot’, is the overall response of the converter to all the harmonics brought by the load step change. To analysis the transient property of the DC-DC converters, it is necessary to start with the converter modeling. The DC-DC converter can generally modeled as shown in Fig. 2.13. The open-loop output impedance is firmly related to the output filter. As a result, the filter components and their parasitics play important roles in the transient behavior of the converter. The output impedance of one DC-DC converter with different Equivalent Series Resistance (ESR) is illustrated in Fig. 2.14. Feeding back the output can reduce the closed-loop output impedance significantly within the bandwidth while beyond the bandwidth, the transient behavior of the converter is decided by the parasitics and nothing can be done for the converter with given filter parameters as shown in Fig. 2.15.



(a) (b)

Fig.2.13. Small-signal Model of the on-board DC-DC

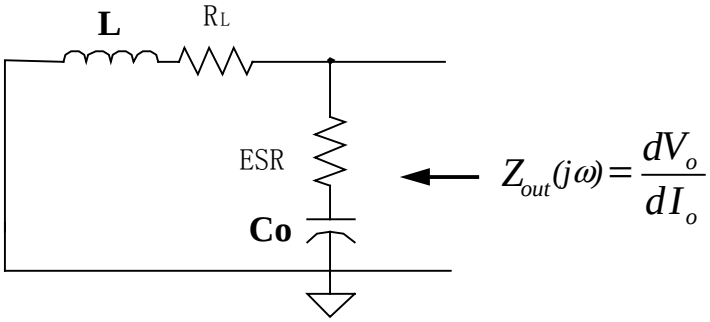


Fig. 2.14. The output impedance model

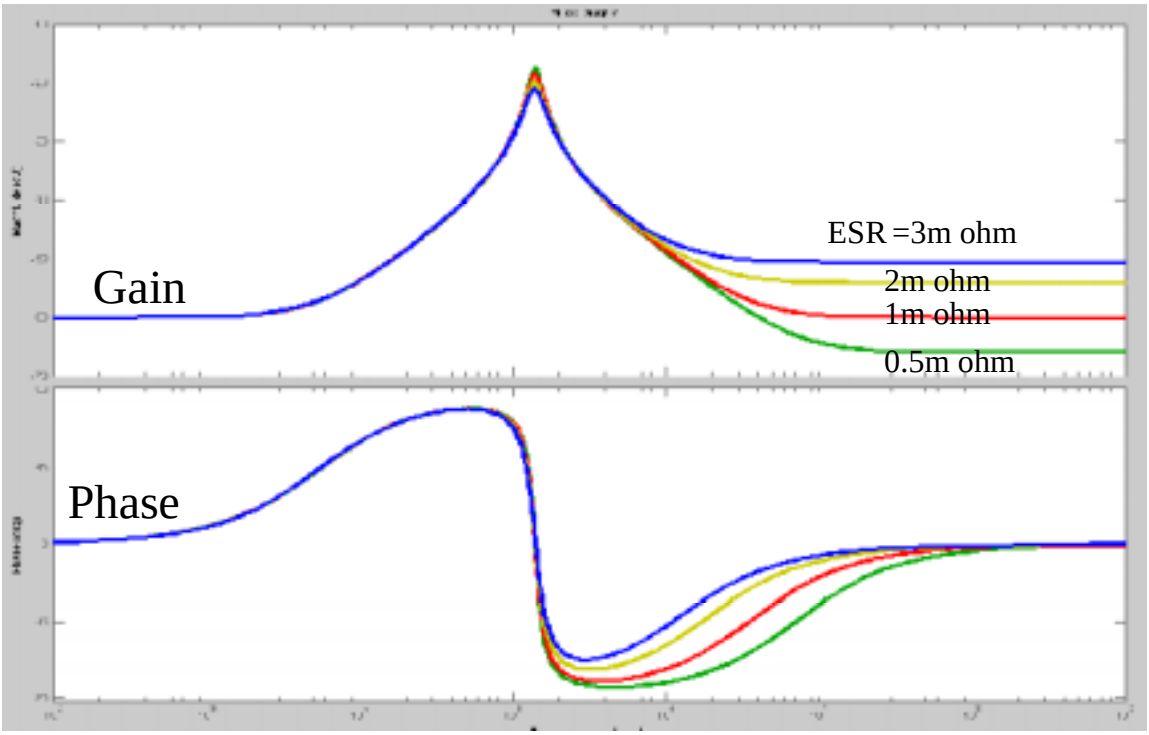


Fig. 2.15. The output impedance vs. different capacitor ESR

2.2.3 The relationship between transient response and efficiency

To obtain fast transient response, high bandwidth is required so that the closed-loop impedance can be controlled within the bandwidth in specific frequency range. There exists several ways to expand the bandwidth of DC-DC converters. The most straightforward one is choosing high switching frequency. With high-frequency switching, the filter may have smaller inductor, which reduces the output impedance of the converter. However, high switching frequency always means high losses and low efficiency. When switching frequency increases, the losses on the MOSFETs (switching loss, driving loss and body diode reverse recovery loss) go up, the losses on the magnetic component also increase due to the material property (core loss) and the skin effect of the windings (copper loss).

A large variety of solutions are proposed to expand the bandwidth in the literatures. From the topology point of view, soft switching techniques such as ZVS and ZCS are widely employed in high-frequency switching converters. From the control point of view, various control schemes are proposed to expand the bandwidth. Among which, the peak current mode control has long been introduced and applied in DC-DC converters.

3. NEW PEAK CURRENT MODE CONTROL CONCEPT AND DERIVED SCHEMES FOR HALF-BRIDGE TOPOLOGY

3.1 Introduction

In recent years, the peak current mode control has been widely investigated for DC-DC converter applications [C1-C5]. In [C2], the peak current mode control is applied to a push-pull DC-DC converter topology for space applications. Dynamic current sharing between paralleled converters can be achieved by using peak current mode control [C3]. In [C5], small-signal model of a phase-shift full-bridge is presented based on the peak current mode control. The advantages for peak current mode control can be summarized as follows:

a) One pole of the power stage is moved to higher frequency such that the voltage loop compensation becomes simpler and higher bandwidth and better transient response can be achieved.

b) Feed forward control to the input line disturbance, and good output regulation can be achieved.

c) Cycle-by-cycle current limit naturally provides over current protection.

d) Easy to achieve current sharing for paralleled converters

Half-bridge is a suitable topology for low-voltage high-current DC-DC converters due to its simplicity [C6-C8]. However, peak current mode control cannot be directly applied on symmetric half-bridge DC-DC converter topology due to the capacitor voltage imbalance problem.

In this Chapter, a new compensation concept is proposed to correct the capacitor voltage imbalance. A voltage compensation loop is added to the control circuit so that no modification and extra components are needed in the power stage. Two schemes are derived from the proposed compensation concept. Experimental results verified the feasibility of the proposed control schemes. In Section 3.2, the proposed compensation concept is introduced in detail. The first derived control scheme for symmetric half-bridge is proposed and analyzed in Section 3.3, implementation circuit is introduced as well. In Section 3.4, the second derived control scheme for DCS half-bridge topology is proposed with detail for implementation. Prototype is built and verified with experimental results shown in Section 3.5.

3.2 Proposed voltage imbalance compensation concept

3.2.1 The capacitor voltage imbalance problem in half-bridge topology

Fig. 3.1 shows the half-bridge topology. Capacitor C1 and C2 are necessary for circuit operation and the average voltages across them in one switching period are equal for ideal operation. However, the voltages across two capacitors C1 and C2 fall apart from equilibrium due to positive feedback induced from peak current mode control and finally one capacitor voltage (VC1 or VC2) drops to zero and the half-bridge topology stops working. For example, due to non-ideal component parameters when voltage across capacitor C2 is less than half of input bus voltage Vin and S2 is turned on, VAB=VAE<1/2Vin. It takes more time for iL to hit the current reference because of the

smaller di/dt induced by VAB. The capacitor C2 discharges more which leads to more voltage drop across C2. The positive feedback continues till VC2 drops to zero and half-bridge stops working. For VAE>1/2Vin case, the similar positive feedback exists and voltage across C1 is zero finally. Therefore, peak current mode control cannot be directly applied on half-bridge topology.

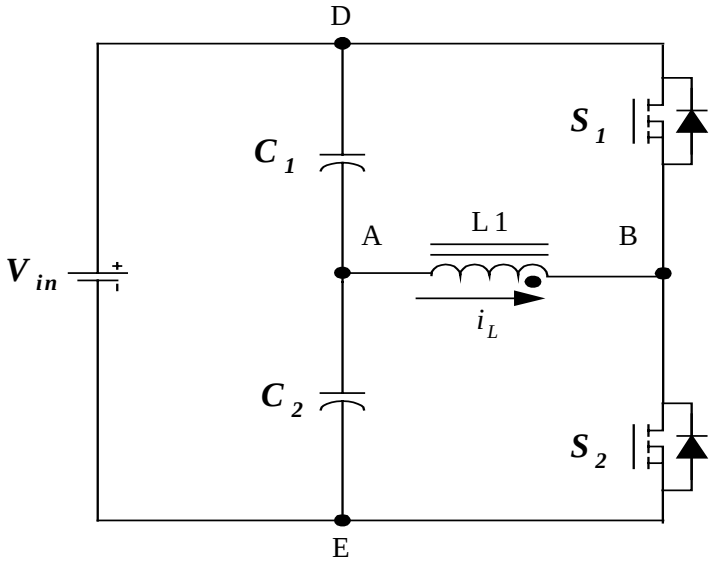


Fig. 3.1 Half-Bridge topology

One solution shown in Fig. 3.2 is presented by an unknown engineer attending Unitrode seminar [C9]. Three extra components are added to the power stage to balance the capacitor voltage. Winding L2 has the same number of turns as the transformer primary side winding and is coupled with transformer. Two fast recovery diodes D1 and D2 are connected which forms an additional branch to balance the capacitor voltage. When VAE>1/2Vin and S2 is on, VAB=VAE>1/2Vin. Since L2 and L1 have the same number of turns, VCA=VAB>1/2Vin, VCE=VCA+VAE>Vin, diode D1 conducts and VCE is clamped to Vin. For VAE<1/2Vin case, when S1 is on, VBC>Vin, the low side

diode D2 conducts and clamps VBC to Vin. The positive feedback is avoided finally and the voltage across the capacitor is brought back to normal.

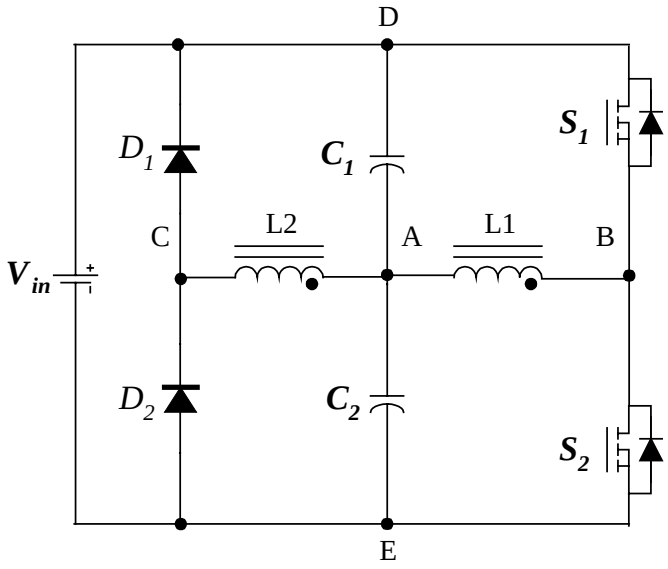


Fig. 3.2 One solution to balance capacitor voltages in half-bridge topology

The solution automatically corrects the voltage imbalance problem on the half-bridge capacitors and does not affect the efficiency much since power flow in the additional branch is not big. However, disadvantages are found as follows: a) Modifications on the power stage are required. b) An additional winding (even may be small but with the same number of turns as the transformer primary side winding) is needed which complicates the transformer structure and degrade the transformer performance.

3.2.2 The proposed capacitor voltage compensation concept

The idea to balance the capacitor voltage is to use an additional voltage compensation loop to correct the capacitor voltage imbalance. The the key waveforms for the proposed control scheme are shown in Fig. 3.4. Whenever voltage imbalance exists, the compensation loop corrects the capacitor voltage by changing duty ratio of one channel MOSFET driving signal to prevent positive feedback and bring the capacitor voltage back to balance. For example, if VAE is less than half of the input bus voltage Vin, the control loop decrease the duty ratio of S2 driving signal in spite of small current slop of iL. Less discharge of the capacitor prevents the positive feedback and brings back VC2 to normal. For the other case, the duty ratio is increased and the capacitor discharged more.

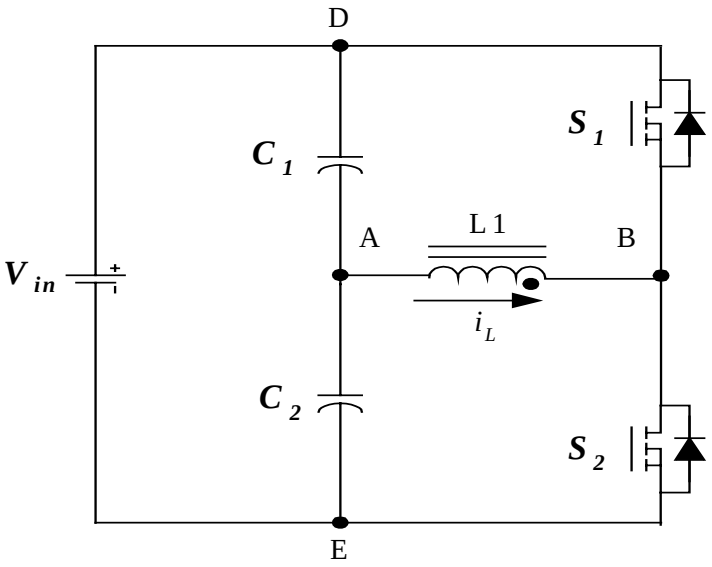


Fig. 3.3 Half-Bridge topology

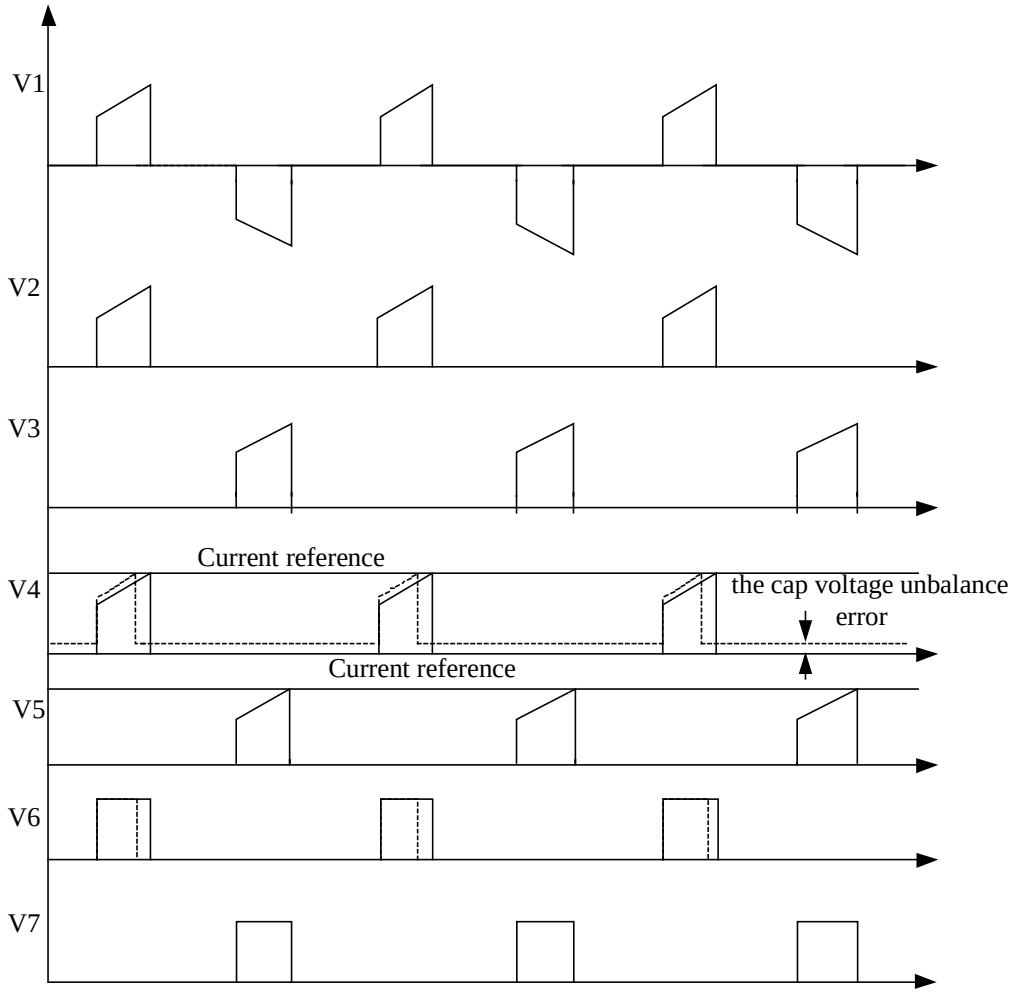


Fig. 3.4 Key waveforms for the proposed compensation concept on symmetric half-bridge topology

The proposed scheme has advantages as follows: 1) Positive feedback is prevented by proposed control scheme. Peak current mode control can be applied on half-bridge topology with the proposed control scheme. 2) No modification on the power stage, all compensations are done in control circuitry, no extra component needed for the power stage. 3) Simple control circuitry, suitable for integration.

3.3 Derived control scheme for symmetric half-bridge topology

The proposed control scheme is shown in Fig. 3.5. Key waveforms are shown in Fig. 3.4. Current flowing through transformer primary windings is detected by current transformer and is split into two channel signals by two diodes. The two current signals correspond with the on-off states of the two switches in half-bridge. The voltage imbalance error information is added to one channel current signal to compensate the duty ratio of the related MOSFET driving signal. The other channel MOSFET driving signal keeps unchanged without any compensation. The compensation is implemented by sensing the input bus voltage and the low side capacitor voltage of the primary side half-bridge. For a given stable input, if two capacitor parameters are equal, the low side capacitor voltage is half of the input bus voltage. As a result, half of the detected input line voltage value is compared with the capacitor voltage value. The difference contains the information of the capacitor voltage deviation. To generate the reset signal for peak current mode control so that to control the falling edge of the MOSFET driving signal, circuit in Fig. 3.5 is proposed in which, a comparator is used with the non-inverting pin connected to the current signal and the inverting pin connected to the current reference provided by the outer voltage loop. When the current signal hits the current reference, the comparator output is set to high, the RS flip-flop is reset and the control signal falling edge is generated.

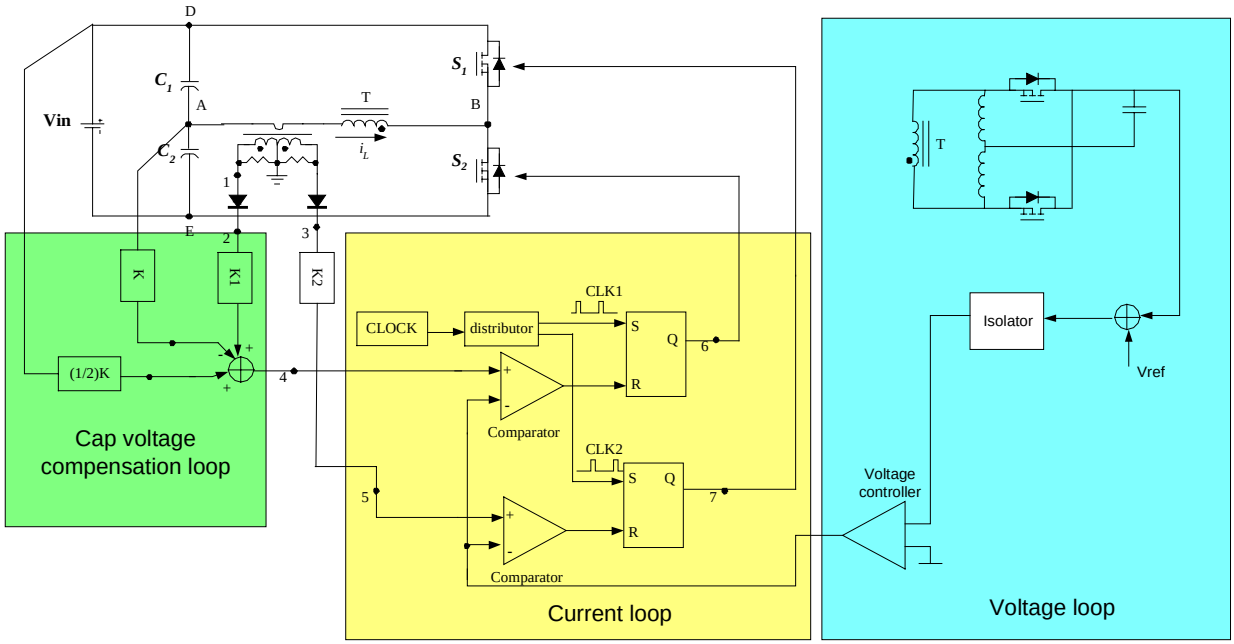


Fig. 3.5 The block diagram of the proposed control scheme for symmetric half-bridge topology

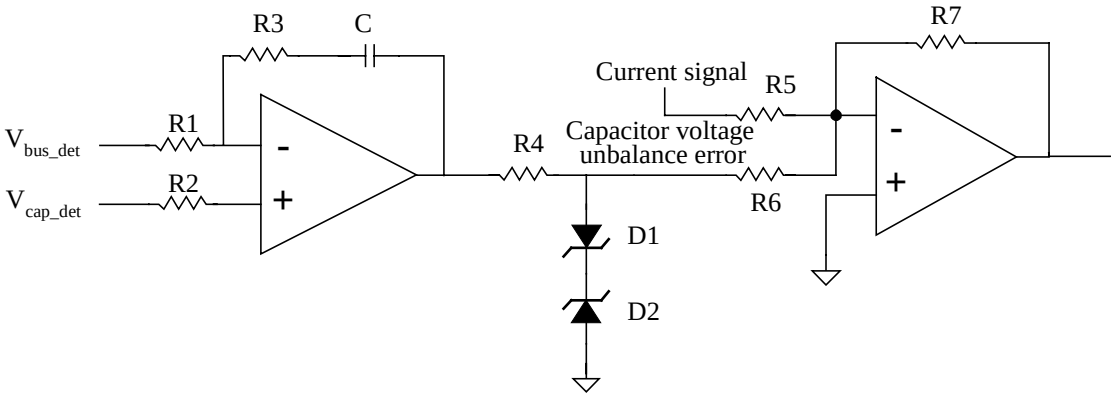


Fig. 3.6 Capacitor voltage compensation loop implementation

The detailed circuitry for compensation loop is shown in Fig. 3.6. Vbus_det is the input bus voltage detection and Vcap_det is the capacitor voltage detection. Both of them are from voltage divider and scaled to be equal if capacitor voltage is perfectly balanced. A PI controller is used to generate the error signal for the voltage imbalance correction.

Since voltage imbalance correction does not require very fast compensation, the compensation loop does not need wide bandwidth. Low speed operation amplifier is qualified for implementation. One channel current signal and capacitor voltage imbalance error are fed into adder (or other equivalent circuitry) causing current signal biased according to the voltage imbalance error. The new current signal contains both current information and voltage imbalance information, which can be used to compensate the capacitor voltage. If the voltage of the low side capacitor (Vc2) is less than half of the input bus voltage, the output of the PI controller is negative. Recalling the fact that the adder shown in Fig. 3.6 has negative gain, the current detection signal is lifted by the value of the error signal. To reverse the polarity, an additional opam with negative unit gain is used. For a given current reference, it takes less time for the current signal to hit the reference compared with its uncompensated counterpart. A less-pulse-width driving signal is induced and switch S2 has less on time. Therefore, capacitor C2 discharged less, which breaks the positive feedback and brings the voltage back to normal.

The diving signal is generated using logic block shown in Fig. 3.7. Two J-K flip-flops are used as R-S flip-flop in Fig. 3.5. Since J and K are tied high, the non-inverting output is set to high by the rising edge of the clock signal to initialize the driving signal. The falling edge of the driving signal is generated by comparator output. When current signal hits the current reference, the comparator output low-level voltage that clears the J-K flip-flop to generate the falling edge of the driving signal. The switching frequency is decided by clock signal. The clock signals for the two J-K flip-flops are complimentary and in good synchronization since they are from the same source. The driving signal are generated alternatively for symmetric half-bridge.

If current signal cannot hit the reference in half a switching period for some reason, J-K flip-flop cannot clear its output even after the second driving pulse is initialized and short circuit

occurs. Two AND gates S1 and S2 are used to interlock the driving signals as shown in Fig. 3.7. Driving signal is decided by both the J-K flip-flop output and the clock signal fed to the J-K flip-flop. It can be high only within half the switching period. Regardless of the flop-flop output, driving signal cannot be high since the clock signal in the other half of switching period is low. Since the two clock signals are complementary, simultaneous turn-on of S1 and S2 are effectively prevented.

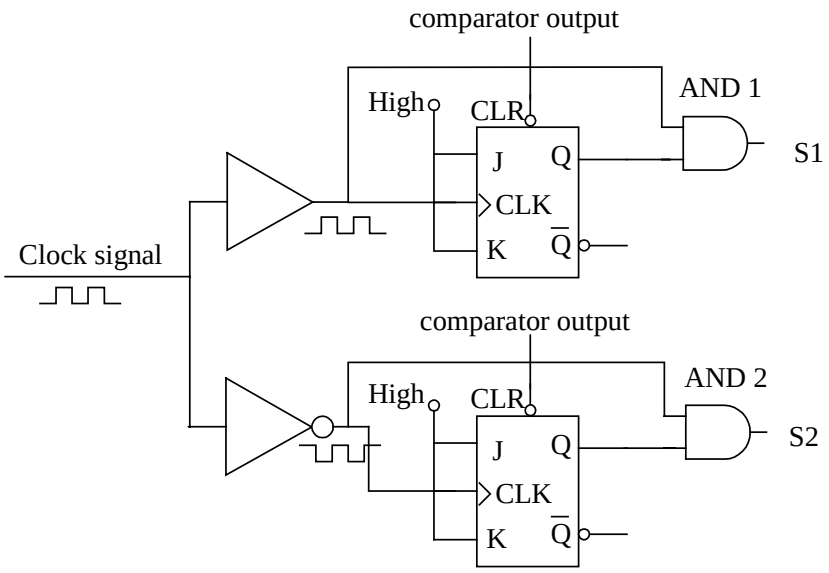


Fig. 3.7 Peak current mode control logic block

3.4 Derived control scheme for DCS half-bridge topology

3.4.1 Introduction to DCS half-bridge topology

The concept of the DCS PWM control is shifting one of the two-channel symmetric PWM driving signals close to the other, while keeping the pulse-width-modulation (PWM) control mode. As a result, ZVS may be achieved at one side because one switch

turns on just after the other switch is turned off. Moreover, because the width of the two switches duty cycles is kept equal, all corresponding components work at the conditions with even stresses as the case in the symmetric control scheme. For the similar reason described before, the peak current mode control cannot be directly applied on the DCS half-bridge topology.

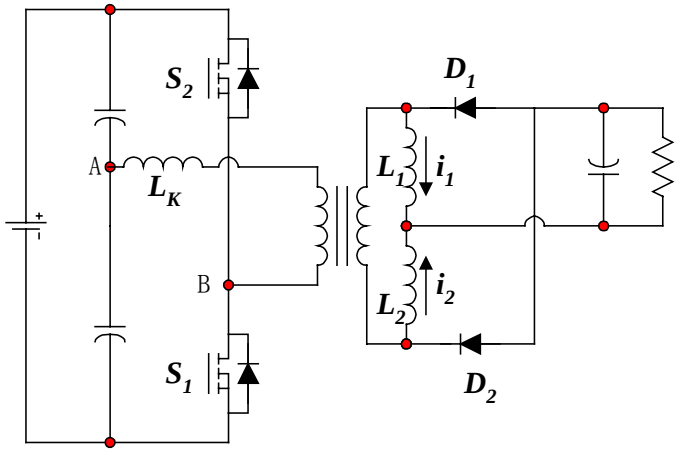


Fig. 3.8 Half-bridge topology

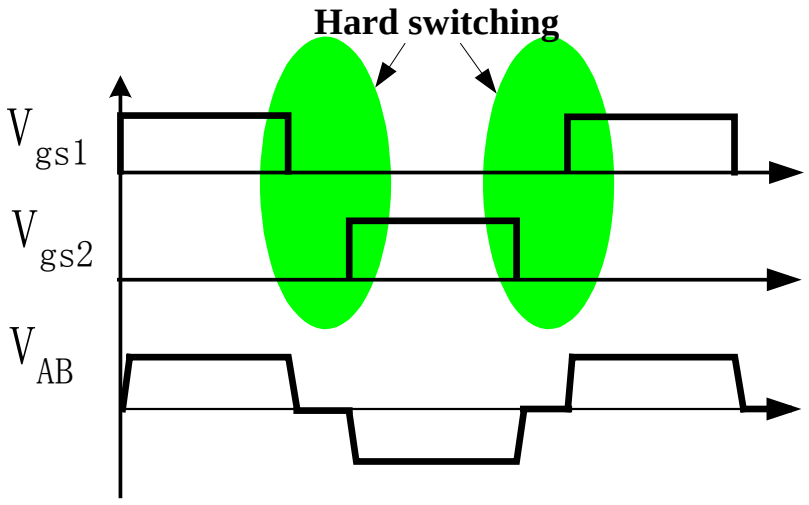


Fig. 3.9 Symmetric PWM control

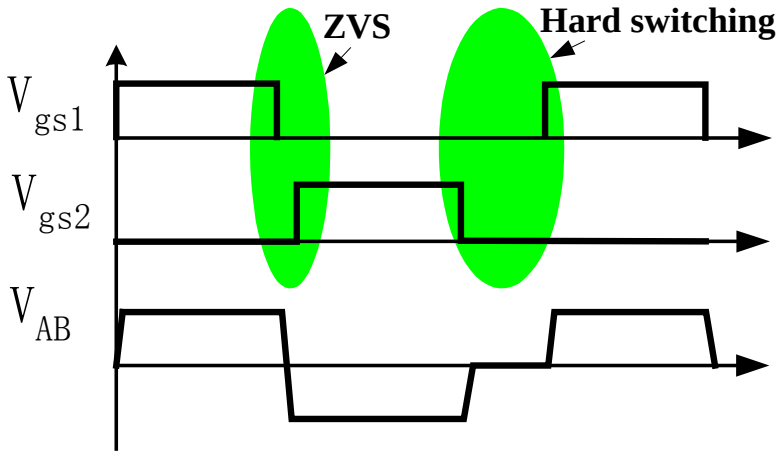


Fig. 3.10 DCS PWM control

3.4.2 Derived control scheme for DCS half-bridge topology

Fig. 3.11 shows a DCS half-bridge DC-DC converter with the proposed peak current mode control in which DCS half-bridge topology is used for the primary side and current doubler is used for the secondary side rectification. Three loops exist in the converter, the outer voltage loop, the inner current loop and the capacitor voltage compensation loop. Similarly, two voltage detections, the bus voltage (input voltage) detection and the low side capacitor voltage detection, are necessary for the provided control scheme. Key waveforms are shown in Fig. 3.12. The same as described in the scheme proposed for symmetric half-bridge topology, the voltage imbalance error signal is added to one channel current signal to compensate the duty ratio of the related MOSFET driving signal. The other channel MOSFET driving signal keeps unchanged without any compensation. The compensator circuit is the same with the one in the scheme for symmetric half-bridge as re-drawn in Fig. 3.13 and the description is omitted.

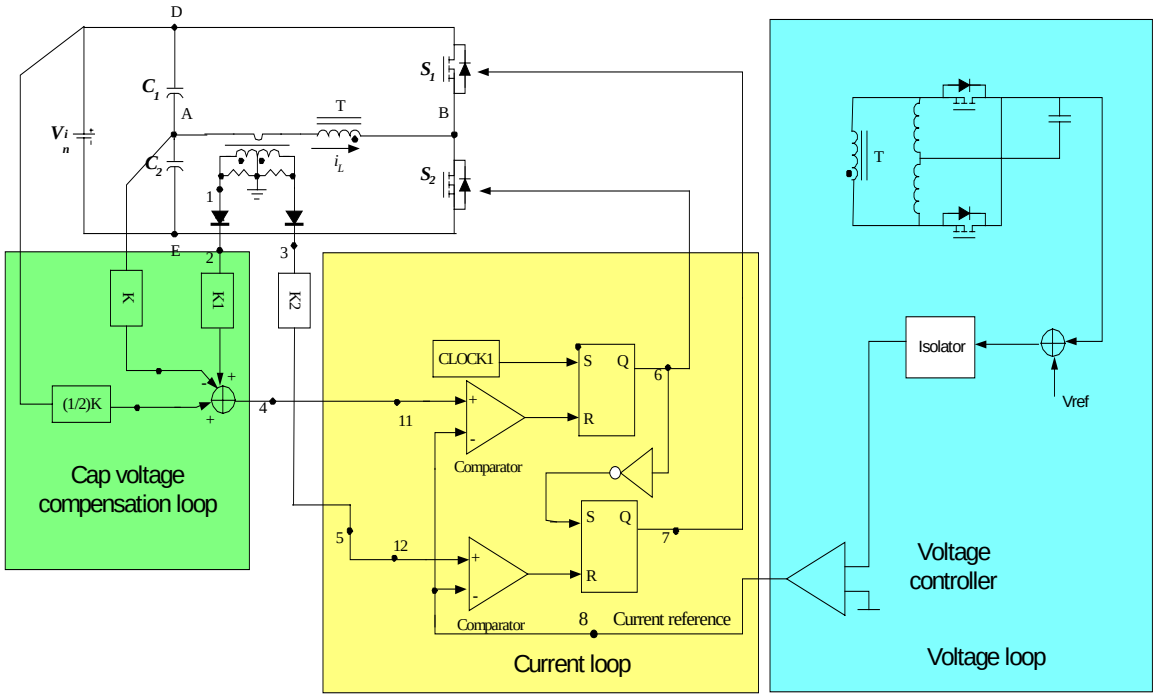


Fig. 3.11 The proposed control scheme block diagram

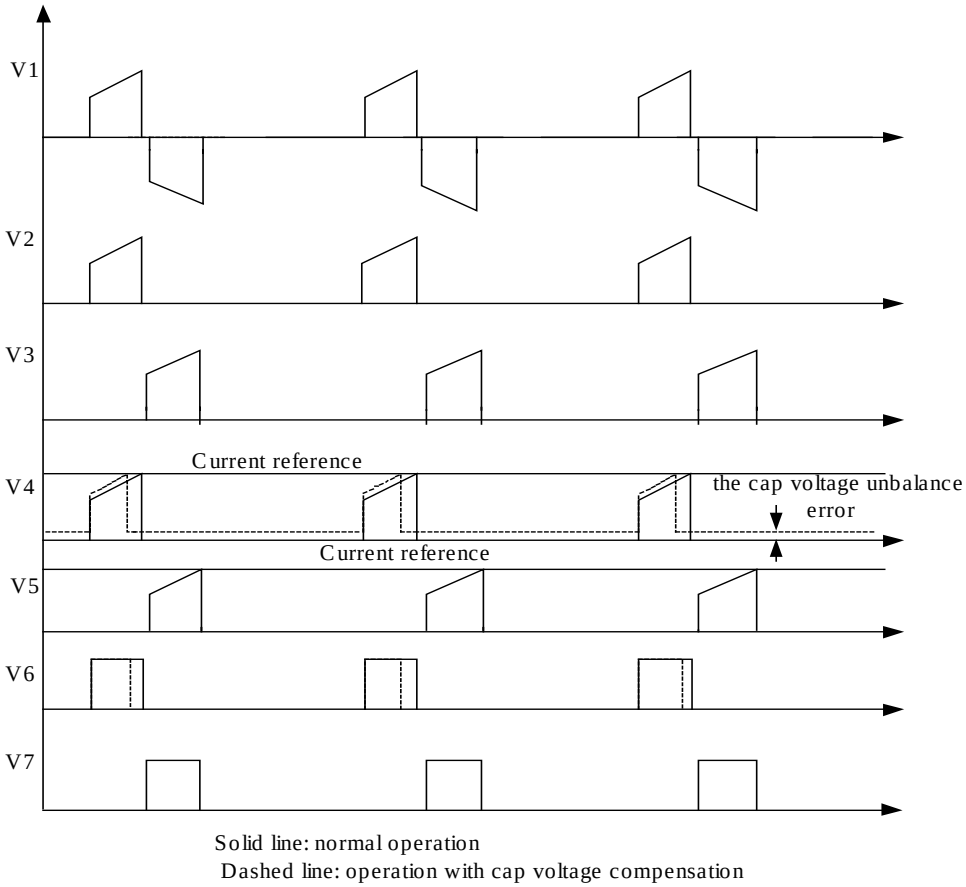


Fig. 3.12 Key waveforms for proposed compensation scheme

The logic components employed to do the job can be R-S flip-flop, J-K flip-flop or other qualified ones which can set and clear the output following the DCS peak current mode control logic. One implementation example for the above description is shown in Fig. 3.14.

External clock signal is used for J-K flip-flop U3 that sets the switching frequency. Two J-K flip-flops U3 and U4 tie both J and K high, the rising edge of the clock signal applied on clock pin sets the output high and initiates the rising edge of the driving signal. The comparator outputs 11 and 12 in Fig. 3.11 are tied to the CLR pin of the J-K flip-flop so as to clear the output when current signal hits the current reference, that is, turn off the MOSFET. If current signal cannot hit the reference in half a switching period for some reason, J-K flip-flop U3 cannot clear its output even after the second driving pulse is initialized by U4 and short circuit occurs. Two AND gates U5 and U6 are used to interlock the driving signals.

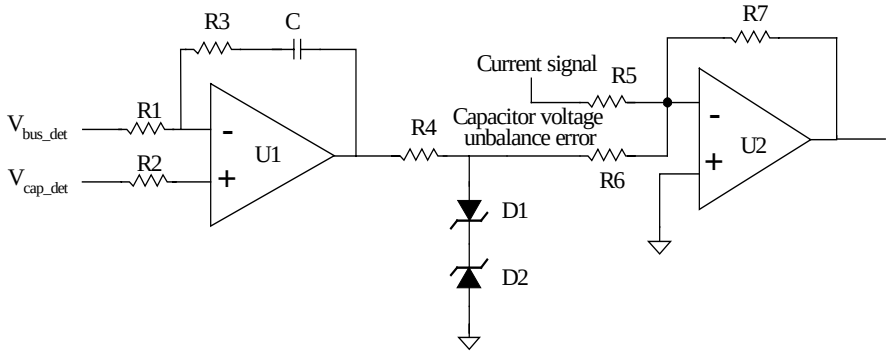


Fig. 3.13 Voltage imbalance detection and compensation circuit

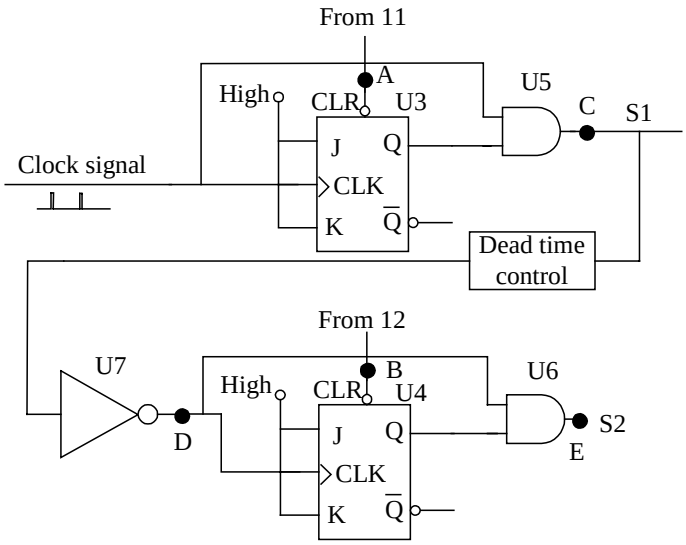


Fig. 3.14 DCS scheme implementation logic circuitry

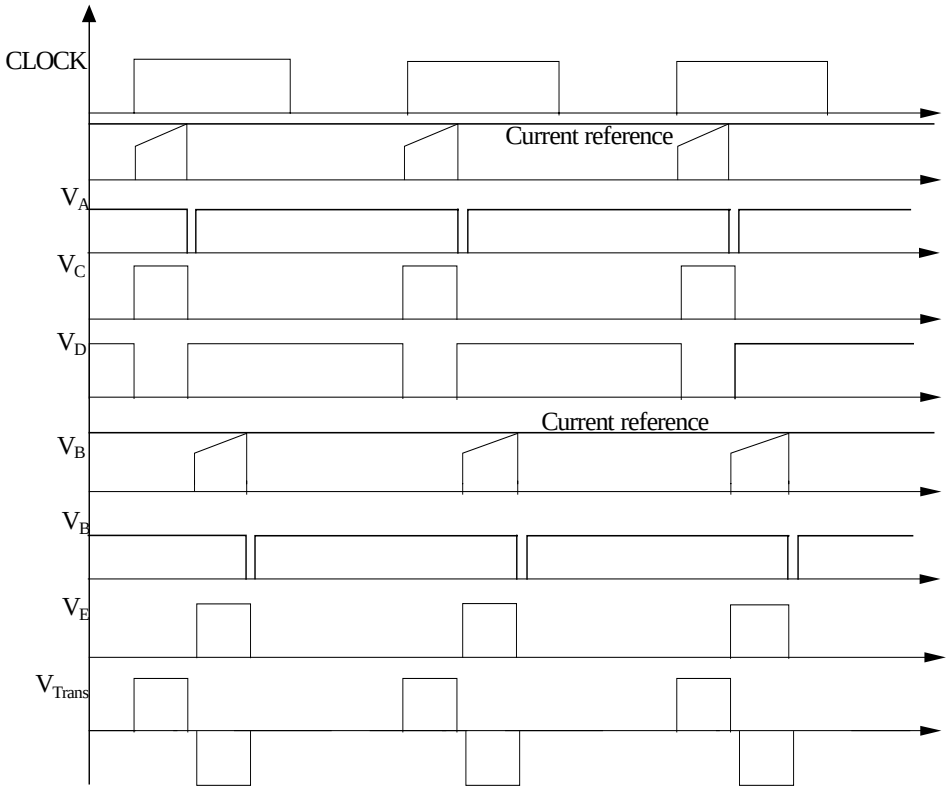


Fig. 3.15 Key waveforms for Fig. 3.14

Since the two driving signal pulses are shifting together in DCS control scheme, the control signal for the low side MOSFET is initiated right after the falling edge of the high side MOSFET driving signal. The output of U5, that is, the high side MOSFET driving signal S1, connect to inverter U7 after being delayed for several nanosecond dead time and is sent to CLK pin of J-K flip-flop U4. The falling edge of S1 triggers the J-K flip-flop U4 to initiate the low side MOSFET driving signal after dead time to prevent short circuit.

3.5 Experimental verification

To verify the feasibility of the proposed control scheme, a half-bridge DC-DC converter prototype with current doubler on the secondary side is built with the specification listed below:

Vin=36~60V variable, Vout=1.8V, Iout=40A, fs=200kHz.

For the primary side, two IRFB59N10D MOSFETs are used for S1 and S2, 6 IRFR3707Z MOSFETs (3 in parallel for each channel) are used for synchronous rectifier in the secondary side to reduce the losses. IR2110 is used to drive the primary two MOSFETs and two TC4422 are used for the secondary current doubler synchronous MOSFETs driving. PC44 is used as the transformer core material. For the control board, LT1016 is used as the comparator. LM324 is used as the opam for the compensation loop PI controller and the outer voltage loop compensator. JK flip-flop DM74109 is used for the peak current control. The prototype is shown in Fig. 3.16, Fig. 3.17 and Fig. 3.18.

Fig. 3.16 The power stage of the proposed peak current mode controlled DC-DC converter

Fig. 3.17 The control board employing proposed peak current mode control scheme for DCS half-bridge topology

Fig. 3.18 The control board employing proposed peak current mode control scheme for symmetric half-bridge

3.5.1 Experimental results for proposed peak current mode control scheme for symmetric half-bridge topology

The experimental results are shown in Fig. 3.19 and Fig. 3.20. Fig. 3.19 shows the key waveforms from the power stage. It is clear that the low side capacitor voltage (C3) is approximately half of the input bus voltage (C4), which indicates that the capacitor voltage is well balanced. The feasibility of the proposed control scheme is verified. Without the capacitor voltage compensation loop, one capacitor voltage is pulled down to zero and the converter stops working. Fig. 3.20 shows the key waveforms from the control board. When the half-bridge MOSFET is turned on, the current (C1) keeps increasing and hit the current reference. The low level output of the comparator resets the flip-flop and the falling edge of the driving signal is generated. Since there is big delay

from the flip-flop to the gate of the MOSFETs, the current signal keeps increasing for a while after it hits the current reference.

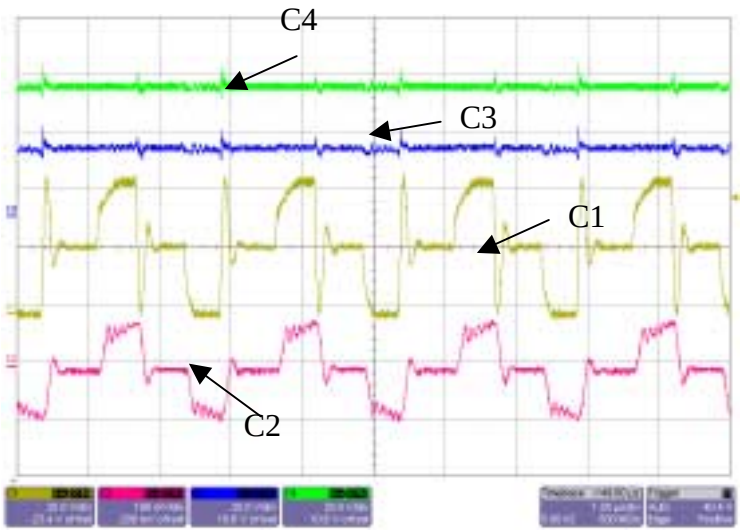


Fig. 3.19 The key waveform from the power stage

(time scale: 1us/div, C4: the input bus voltage, 20V/div; C3: the low side capacitor voltage, 20V/div; C1: Vds of the low side MOSFET, 20V/div; C2: the current flowing through the primary side winding, 5A/div)

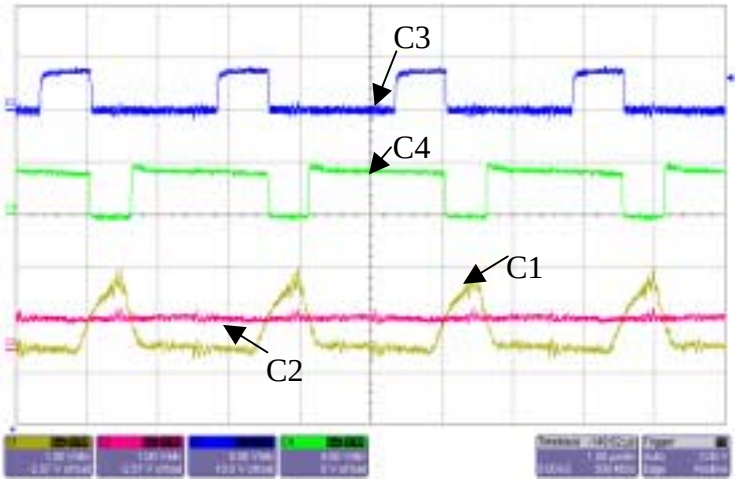


Fig. 3.20 The key waveform from the control board

(time scale: 1us/div; C3: the driving signal for one channel MOSFET, 5V/div; C4: the reset signal for the J-K flip-flop, 5V/div; C2: the current reference from the outer voltage loop, 1V/div; C1: the detected current signal, 1V/div)

3.5.2 Experimental results for proposed peak current mode control scheme for DCS half-bridge topology

The experimental results are shown in Fig. 3.21 and Fig. 3.22. Fig. 3.21 shows the key waveforms from the power stage. C4 is the low side MOSFET Vds voltage waveform. It has the same shape with transformer primary side windings voltage waveform.

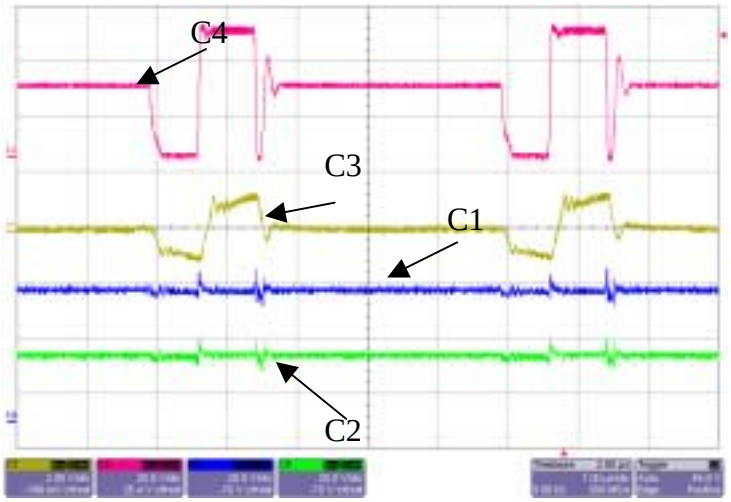


Fig. 3.21 Key waveform from the power stage

(time scale: 1us/div, C1: the input bus voltage, 20V/div; C2: the low side capacitor voltage, 20V/div; C4: Vds of the low side MOSFET, 20V/div; C2: the current flowing through the primary side windings, 5A/div)

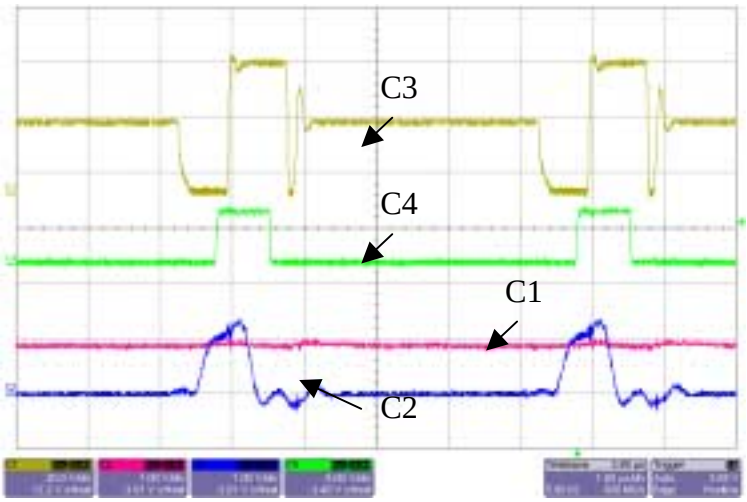


Fig. 3.22 Key waveform from the control board

(time scale: 1us/div; C4: the driving signal for one MOSFET, 5V/div; C3: Vds of the low side MOSFET, 10V/div; C1: the current reference from the outer voltage loop, 1V/div; C2: the detected current signal, 1V/div)

In DCS control, since two driving pulses are shifted together, the high side MOSFET is turned on right after low side MOSFET is turned off. As a result, the positive pulse and the negative pulse on transformer windings are together instead of distributed evenly in one switching period in conventional symmetric PWM control. From Fig. 3.21, it is clear that the low side capacitor voltage (C2) is approximately half of the input bus voltage (C1), which means the voltage on the two capacitors are well balanced and the feasibility of the proposed control scheme is verified. In the experiment, without the compensation of the capacitor voltage, one capacitor voltage drops to zero and the converter stops working. Fig. 3.22 shows the key waveforms from the control board. When the half-bridge MOSFET is turned on, the current through it (C2) keeps rising and then hit the current reference (C1). Then the low side MOSFET is turned off and the high

side one is turned on. Since there is big delay from the flip-flop to the gate of the MOSFETs, the current signal keeps rising for some time even after it hits the current reference.

4. MODELING THE PEAK CURRENT MODE CONTROLLED HALF-BRIDGE DC-DC CONVERTER

4.1 Motivation for the peak current mode controlled half-bridge modeling

In Chapter 3, a new peak current mode control scheme is proposed for the half-bridge topology. Based on the proposed voltage imbalance correction concept, two control schemes for implementation are proposed with one for symmetric half-bridge topology and the other one for the DCS topology. Detailed implementation effort is introduced and the experimental results provided by the lab prototype, which verified the feasibility of the proposed control scheme. Since all work in Chapter 3 focused on the implementation and experiment verification, it is necessary to carry out the analysis of the extra voltage imbalance correction loop on the overall behavior of the power converter. Below questions are to be answered by the modeling work to get a clear understanding of the theorem hiding behind the physical performance of the converter.

- Why does peak current mode control cause the capacitor voltage imbalance in half-bridge topology?
- Why can the extra voltage correction loop balance the capacitor voltage and stabilize the converter?

In this Chapter, the mechanism of the voltage imbalance is explained by the modeling and for the first time provides the mathematic understanding for the voltage imbalance. The effect from the extra compensation loop on the stability of the converter is extensively analyzed and is verified by the simulation results.

4.2 The small signal model for the peak current mode controlled half-bridge topology

The half-bridge DC-DC converter with center tap structure on the secondary side is shown in Fig. 4.1. To simplify the analysis, assumptions are made as follows:

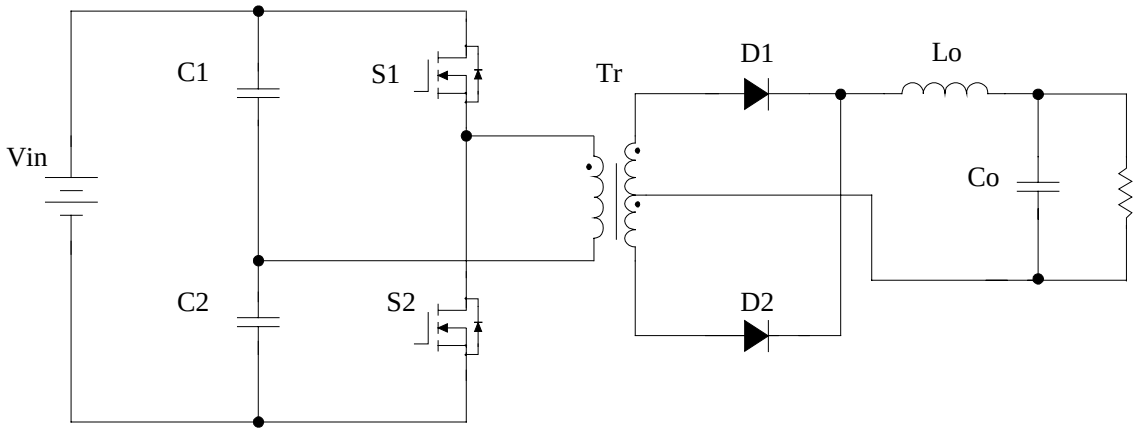


Fig. 4.1 Half-bridge topology

Assumption:

1. Switch S1 and S2 are ideal. Diode D1 and D2 are ideal and the forward voltage drop is ignored.
2. C1 and C2 have equal value so that when well balanced, VC1=VC2=1/2Vin.
3. Output capacitor is big enough so that output voltage is constant.
4. Transformer is ideal, the leakage inductance and magnetizing inductance are ignored.
5. The voltage feedback loop is slow so that the current command signal from the outer voltage loop in the peak current mode control scheme is taken as constant.

Define duty ratio of S1 and S2 as the conduction time of switch over one switching period as shown in Fig. 4.2:

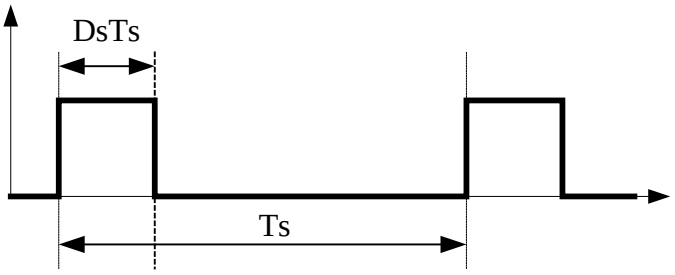


Fig. 4.2 Duty ratio definition

Be noticed that variable name in capital represents the steady-state value.

A. Modeling the transfer function from capacitor voltage to current slope rate:

When S1 is on, the current slope rate of output inductor is expressed as:

$$m1 = \frac{\frac{v_{C1}}{n} - Vo}{Lo} \tag{4.1}$$

where v_{C1} is the voltage across C1, n is the transformer turns ratio and defined as transformer primary side winding turns number over secondary side winding turns number. Vo is the output voltage, Lo is the filter inductance.

By assumption 3, the small signal transfer function from capacitor voltage to current slope rate on inductor is shown as:

$$G1vc\_m = \frac{d(m1)}{d(vc1)} = \frac{1}{n \cdot Lo} \tag{4.2}$$

Similarly, we have:

$$G2vc\_m = \frac{d(m2)}{d(vc2)} = \frac{1}{n \cdot Lo} \tag{4.3}$$

B. Modeling the transfer function from current slope rate of output inductor to duty ratio:

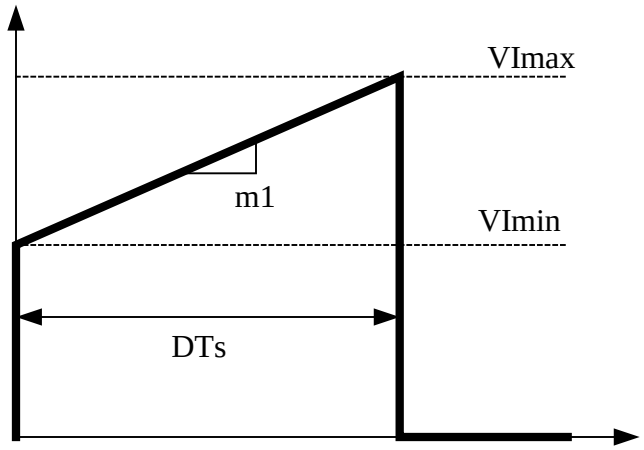


Fig. 4.3 Peak current mode modulator

Fig. 3 shows the peak current mode modulator, VImax is the control signal from the voltage loop, which also represents the detected maxim output inductor current. VImin is the detected minimum output inductor current.

$$V\,\mathrm{Im}\,ax = Ki\,\mathrm{det}\,Iind\,\max \tag{4.4}$$

$$V\,\mathrm{Im}\,in = Ki\,\mathrm{det}\,Iind\,\min \tag{4.5}$$

in which, Kidet is the current detection gain; Iindmax is the maxim output inductor current and Iindmin is the minimum output inductor current.

Suppose the voltage loop output is constant so that VInmax and VImin is constant. Duty ratio is calculated as:

$$d = \frac{(V\,\mathrm{Im}\,ax - V\,\mathrm{Im}\,in)\cdot Ki\,\mathrm{det}}{m\cdot Ki\,\mathrm{det}\cdot Ts} \tag{4.6}$$

in which m is the output inductor current slope rate and Ts is switching period, which is calculated as Ts=1/fs, fs is switching frequency.

The non-linear relationship between duty ratio D and current slope rate M is shown in Fig. 4.4.

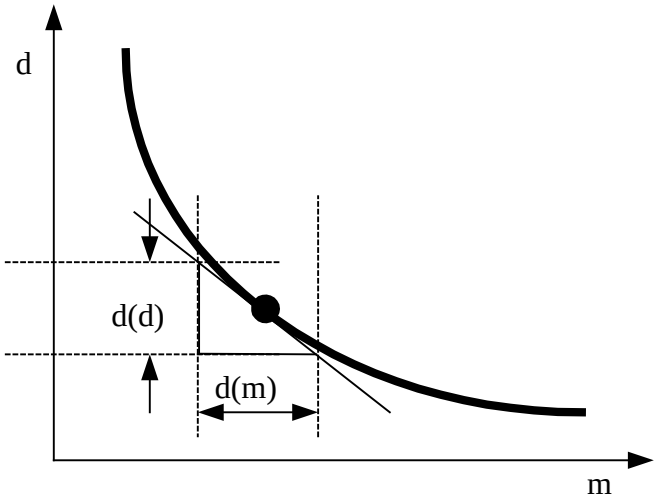


Fig. 4.4 Duty ratio vs. output inductor current slope rate

It can be linearized at steady state operation point as:

$$\frac{d(d)}{d(m)} = -\frac{(V\,\mathrm{Im}ax - V\,\mathrm{Im}in)\,fs}{m^2} \tag{4.7}$$

The transfer function can be obtained as:

$$G1m\_d = -\frac{(V\,\mathrm{Im}ax - V\,\mathrm{Im}in)\,fs}{m1^2} \tag{4.8}$$

$$G2m\_d = -\frac{(V\,\mathrm{Im}ax - V\,\mathrm{Im}in)\,fs}{m2^2} \tag{4.9}$$

C. Modeling the transfer function from duty ratio to capacitor voltage:

Applying voltage-second balance on output inductor, the relation ship between capacitor voltage and duty ratio is obtained.

$$\frac{vc}{n}\cdot d\cdot\frac{1}{fs} = Vo\cdot(\frac{1}{2}-d)\cdot\frac{1}{fs} \tag{4.10}$$

$$vc = \frac{Vo \cdot n \cdot (1-2d)}{2d} \tag{4.11}$$

$$vc1 = \frac{Vo \cdot n \cdot (1-2d1)}{2d1} \tag{4.12}$$

$$vc2 = \frac{Vo \cdot n \cdot (1-2d2)}{2d2} \tag{4.13}$$

The voltage imbalance can be calculated as:

$$vdiff\_out = vc1 - vc2 = \frac{vo \cdot n \cdot (d2-d1)}{2d1d2} \tag{4.14}$$

in which, voltage difference v_{diff}, duty ratio d1 and d2 are variables. Differentiate both side of the equation, the relationship between duty ratio and voltage difference is obtained.

$$\hat{vdiff}\_out = \frac{Vo \cdot n \cdot \hat{d}2}{2d2^2} - \frac{Vo \cdot n \cdot \hat{d}1}{2d1^2} \tag{4.15}$$

D. Calculate the voltage imbalance taking into consideration all the stages mentioned above.

Assume initially the converter is well balanced and the voltages across the two capacitors are equal:

$$V_{C1} = V_{C2} = \frac{1}{2}V_{in} \tag{4.16}$$

Apply a small perturbation on the capacitor voltage so that the capacitor voltage is:

$$vc1 = \frac{1}{2}Vin + \frac{1}{2}\hat{vdiff} \tag{4.17a}$$

$$\hat{vc1} = \frac{1}{2}\hat{vdiff} \tag{4.17b}$$

$$vc2 = \frac{1}{2}Vin - \frac{1}{2}\hat{vdiff} \tag{4.18a}$$

$$\hat{vc}2 = -\frac{1}{2}\hat{vdiff} \tag{4.18b}$$

$$vc1 - vc2 = \hat{vdiff} \tag{4.19}$$

Calculate the new voltage difference taking into consideration all stages above.

$$\hat{d}1 = \hat{vc}1 \cdot G1vc\_m \cdot G1m\_d = -\frac{\hat{vdiff}\,(Iind\,\max - Iind\,\min)\cdot fs}{2n \cdot Lo \cdot m1^2} \tag{4.20}$$

$$\hat{d}2 = \hat{vc}1 \cdot G1vc\_m \cdot G1m\_d = \frac{\hat{vdiff}\,(Iind\,\max - Iind\,\min)\cdot fs}{2n \cdot Lo \cdot m2^2} \tag{4.21}$$

Put 4.20 and 4.21 into 4.15, the new voltage imbalance is obtained:

$$\hat{vdiff}\_out = \frac{Vo(Io\,\max - Io\,\min)(d2^2 m2^2 + d1^2 m1^2)\,fs}{4Lo \cdot m1^2 \cdot m2^2 \cdot d1^2 \cdot d2^2} \cdot \hat{vdiff} \tag{4.22}$$

E. Calculate key steady-state values.

Assume converter capacitor voltage is well balanced, capacitor voltage is equal to 1/2Vin.

d1=d2=D.

Output voltage:

$$Vo = \frac{Vin}{2 \cdot n} D \tag{4.23}$$

Peak-peak output inductor current:

$$Iindpp = \frac{Vo}{Lo} \cdot (\frac{1}{2} - D) \cdot \frac{1}{fs} \tag{4.24}$$

Minimum output inductor current:

$$Iind\,\min = Io - \frac{1}{2} \cdot Iindpp \tag{4.25}$$

Maximum output inductor current:

$$Iind\max = Io + \frac{1}{2} \cdot Iindpp \tag{4.26}$$

Calculate the output inductor current slope rate of the operation point at which the relationship between duty ratio and current slope rate in peak current mode control modulator is linearized.

$$m1 = m2 = m = \frac{\frac{1}{2}Vin \cdot \frac{1}{n} - Vo}{Lo} \tag{4.27}$$

Using the results from 4.23-4.26 and simplifying 4.26, it can be rewritten as:

$$\hat{vdiff}\_out = \frac{1}{1-2D} \cdot \hat{vdiff} \tag{4.28}$$

Conclusions can be drawn from the above derivation:

- By the definition of duty ratio, 0<D<0.5, then $\hat{vdiff}\_out > \hat{vdiff}$. The small perturbation is amplified. This is the reason why peak current mode control cannot be directly applied on symmetric half-bridge topology.
- Equation 4.28 consists of only duty ratio D, which means the voltage imbalance is independent of the half-bridge capacitor value. Choosing large capacitor does not help to prevent the voltage imbalance in symmetric half-bridge topology with peak current mode control.
- The above analysis is applicable to Duty-Cycle-Shifted (DCS) half-bridge topology.

4.3 The small signal model for the voltage imbalance correction loop

As discussed before, the voltage difference is affected by both duty ratio of S1 and S2 driving signal. The peak current mode controlled half-bridge topology is not stable because of the duty ratio is affected by the initial capacitor voltage, the inductor current slope rate, which leads to different duty ratio of the driving signal. If by some means, the duty ratio of S1 (or S2) driving signal is changed according to the voltage imbalance as shown in Fig. 4.5, the unstable converter may be stabilized.

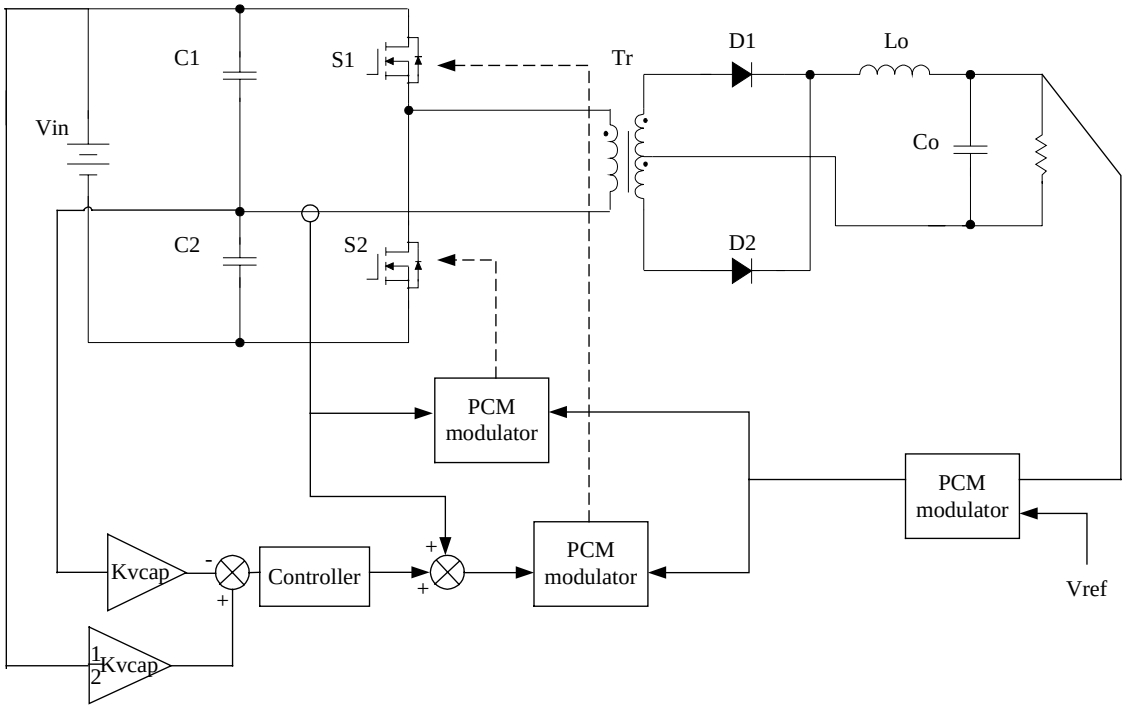


Fig. 4.5 The block diagram for the voltage imbalance correction loop

Assume similarly there is a small signal perturbation injected at the mid point of the half-bridge capacitors causing:

$$\hat{vc1} = \frac{1}{2}\hat{vdiff} \tag{4.29}$$

$$\hat{vc2} = -\frac{1}{2}\hat{vdiff} \tag{4.30}$$

The output of the controller is:

$$\hat{vcomp} = Gcon \cdot (\hat{vc1} - \hat{vc2}) \cdot Kvcap \tag{4.31}$$

An additional –1 gain is applied since the sum of the v_{comp} and the detected current signal is identical with the decrease of the control signal for the peak current mode modulator. Then, we have:

$$\hat{verror} = (-1)\hat{vcomp} \tag{4.32}$$

The error signal is summed with the detected current signal. As a result, the duty ratio of S1 driving signal consists of two parts, the one from the current detection under small signal perturbation and the one from the compensation loop, i.e., v_{error}.

The transfer function from v_{error} to duty ratio is:

$$Gerror\_d = \frac{1}{slope \cdot Ts} \tag{4.33}$$

The duty ratio small signal variation can be calculated as:

$$\hat{d1\_comp} = Gerror\_d \cdot \hat{verror} = \frac{\hat{verror}}{slope \cdot Ts} \tag{4.34}$$

The overall duty ratio can be expressed as the following taking into consideration the contribution from the voltage imbalance correction loop:

$$\hat{d1\_sum} = G1vc\_m \cdot G1m\_d \cdot \hat{vc1} + Gcon \cdot (\hat{vc1} + \hat{vc2}) \cdot Kvcap \cdot Gerror\_d \tag{4.35}$$

Put the above result into 4.15 and after simplification, the following result is obtained:

$$\hat{vdiff}\_out = \frac{2Ds \cdot Ts + Kvcap \cdot n \cdot Lo \cdot Gcon}{2(1-2Ds)Ds \cdot Ts} \cdot \hat{vdiff} \tag{4.36}$$

Compared with 4.28, we have freedom on G_{con} to change the loop gain. If an appropriate controller is selected, the peak current mode controlled converter may be stable for small signal perturbation. There are a big variety of controllers qualified for the application. Took the conventional PI controller as an example, which is shown in Fig. 4.6.

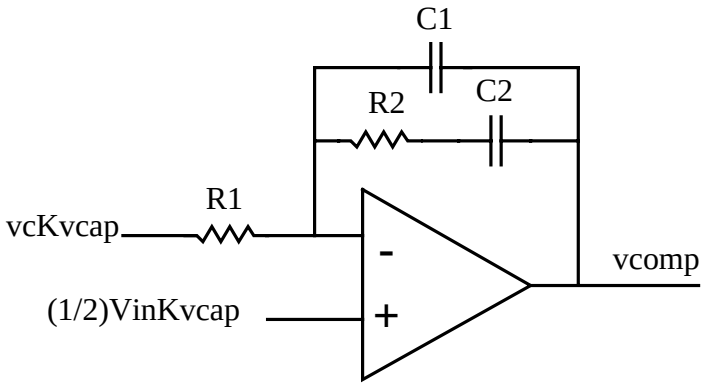


Fig. 4.6 The PI controller used for the voltage imbalance correction loop

The transfer function for the PI controller is shown as below:

$$Gcon = \frac{R1 \cdot C1 \cdot s + 1}{R2 \cdot s \cdot (\frac{R1 \cdot C1 \cdot C2}{C1 + C2} \cdot s + 1)} \tag{4.37}$$

For the application, the following set of component values are used:

R1=33.8kohm, R2=733ohm, C1=470nF, C2=2.9pF.

Using the steady state value calculated before, the bode plot below is obtained:

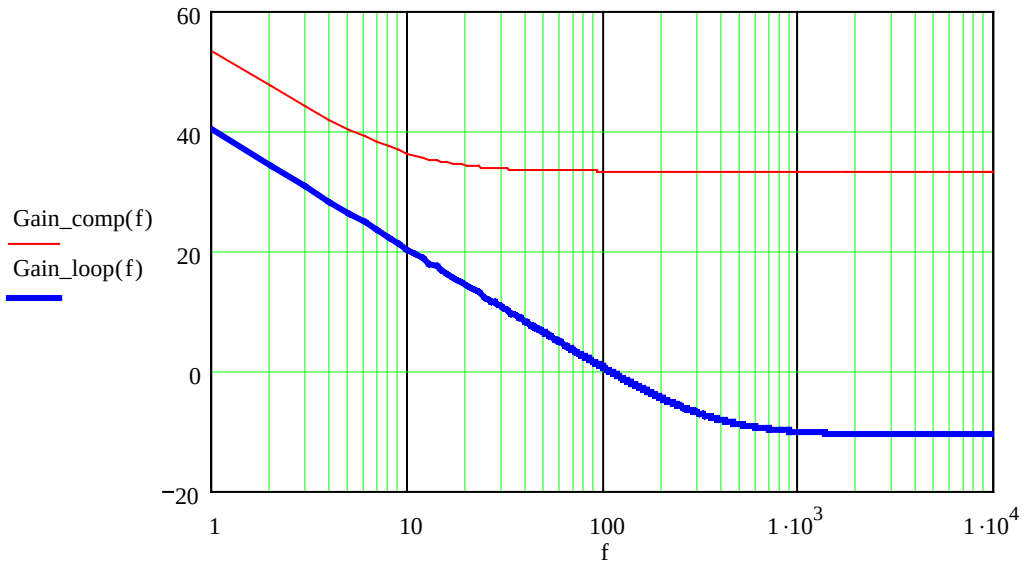


Fig. 4.7 (a) Gain

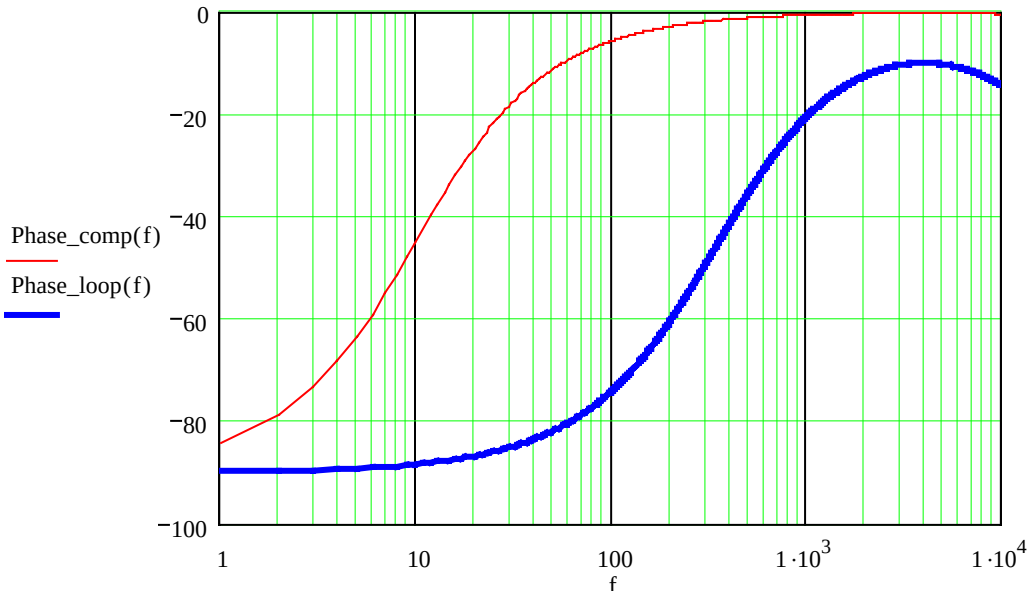


Fig. 4.7 (b) Phase

Fig. 4.7 The bode plot of the compensation loop

(red: the compensator; blue: the loop)

From the bode plot of the loop, the system is stable with the crossing over frequency of 100Hz and enough phase margin.

4.4 Simulation verifications

To verify the model of the peak current mode controlled half-bridge DC-DC converter, a simulation model is build with the following parameters.

Power stage parameters:

Vin=75V, Vout=1V, Iout=50A, fs=200kHz, primary half-bridge capacitor C1=C2=4uF, primary MOSFET: Si7456, secondary SR MOSFET: Si7868, np=6, ns=1. Current doubler structure is used with 2 inductors of 180nH each.

Control circuit parameters:

For the PI controller, R1=33.8kohm, R2=733ohm, C1=470nF, C2=2.9pF. The controller in the simulation model is shown in Fig. 4.8.

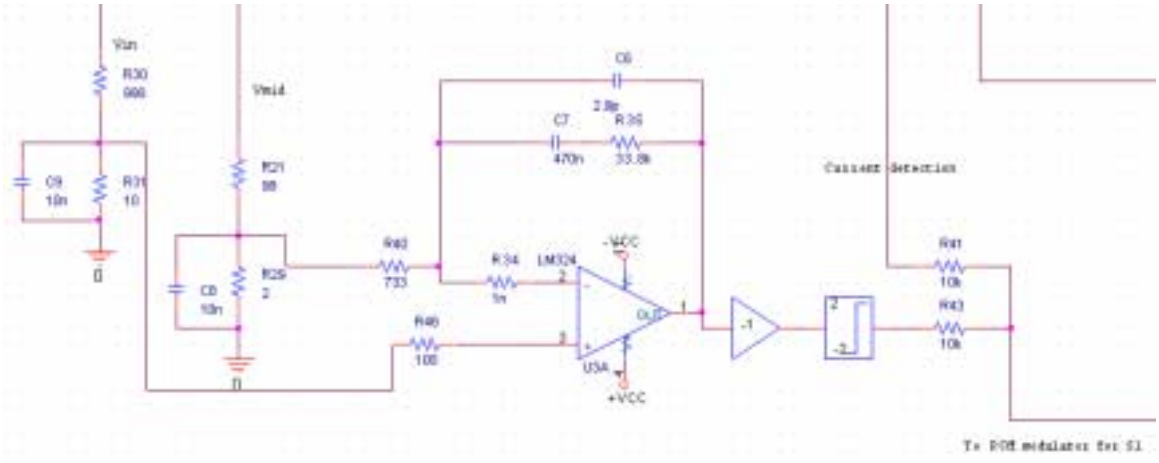


Fig. 4.8 The controller for the voltage imbalance correction loop in the simulation model

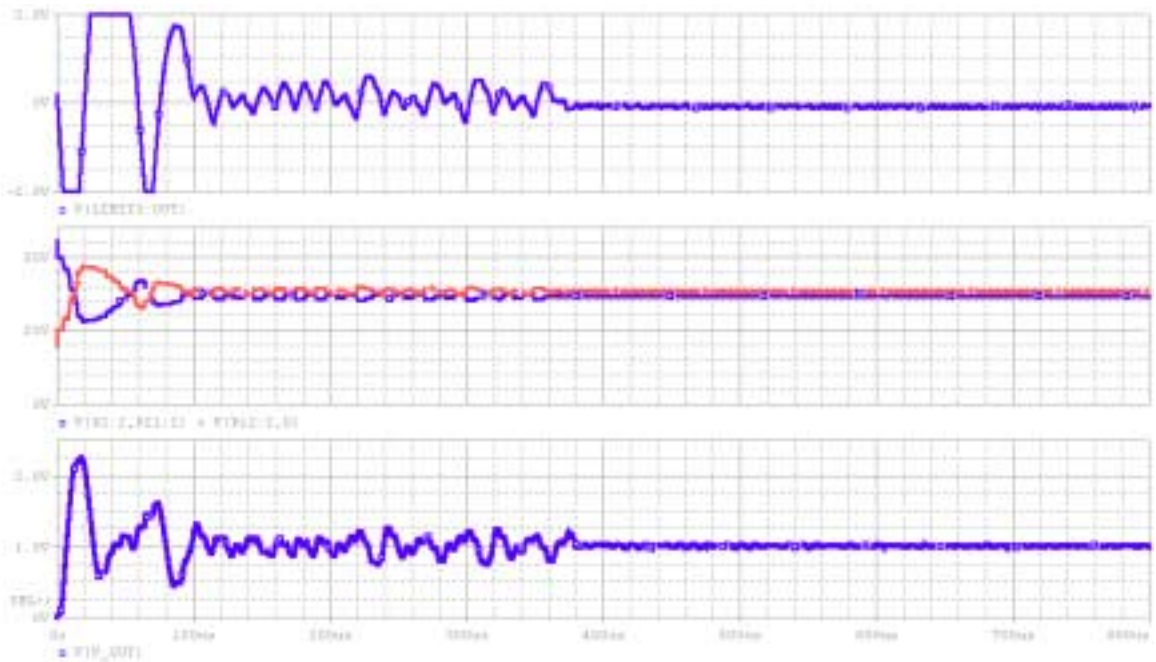


Fig. 4.9 Simulation results for the peak current mode controlled half-bridge DC-DC converter

The simulation result is shown in Fig. 4.9. The top trace is the voltage imbalance loop controller output. The two traces in the middle are the voltage across the two half-bridge capacitors C1 and C2. It is clear that the two voltage fight against each other initially and finally reach balance and share the same voltage. The bottom trace is the output voltage. In Fig. 4.10, the top trace shows the same controller output. The middle trace and the bottom trace show the driving signals for S1 and S2 respectively. When the controller output saturate high, the contribution of the voltage imbalance loop is maximum so that the duty ratio of S1 is zero to correct the significant voltage imbalance.
Fig. 4.11 shows the key waveforms for the peak current mode modulator. In the top picture, the red trace is the control signal from the voltage loop error amplifier, the blue one is the voltage imbalance correction controller output. The yellow one is the sum of the voltage imbalance correction controller output with one channel current detection. It is clear that the waveform is lifted above zero. The bottom picture is the driving signal sending to the gate of MOSFET S1.

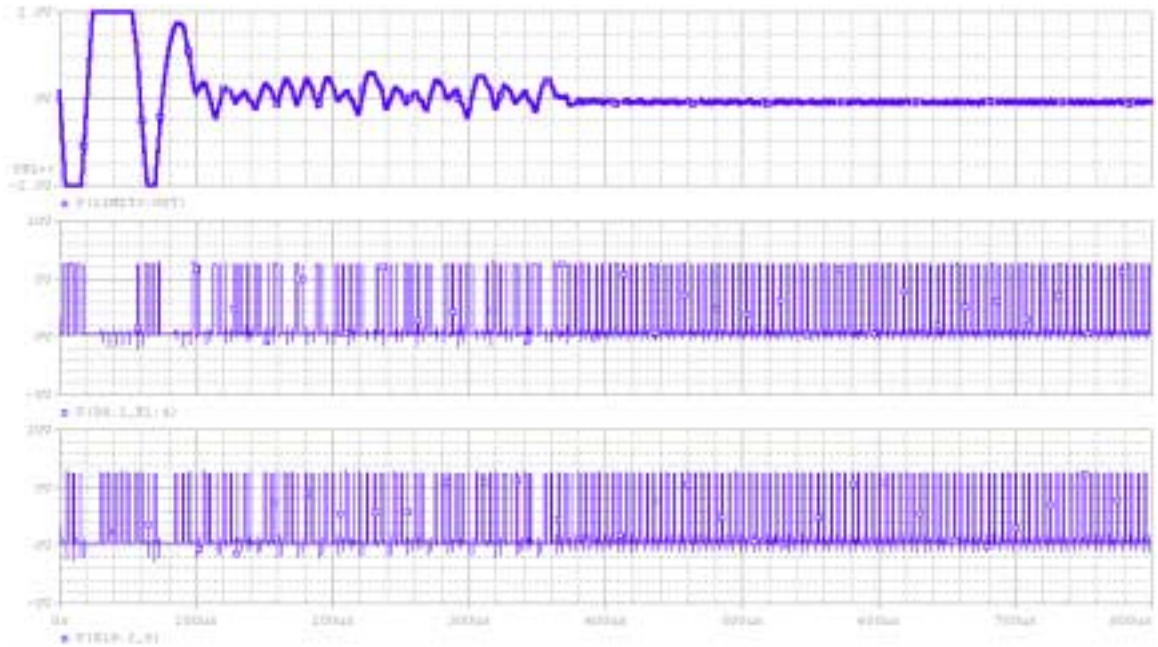


Fig. 4.10 Simulation results for the peak current mode controlled half-bridge DC-DC converter

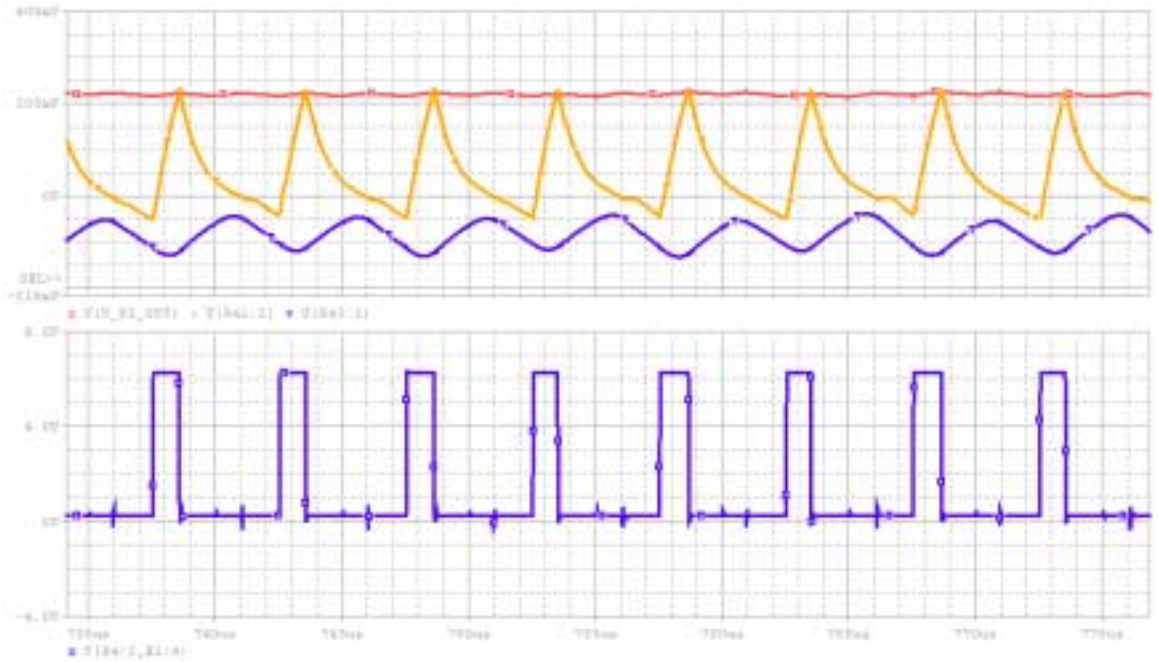


Fig. 4.11 The key waveforms for the peak current mode modulator

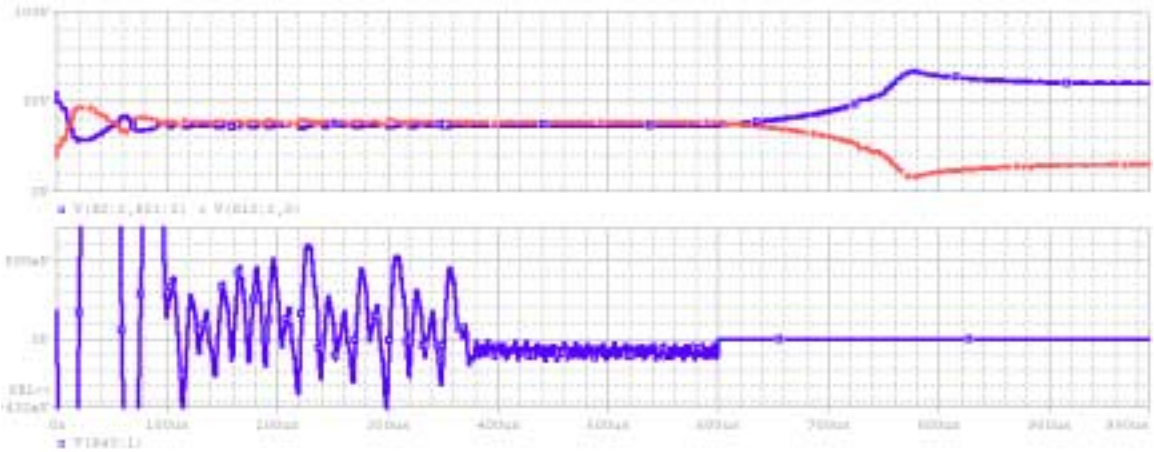


Fig. 4.12 The capacitor voltage runs into imbalance when correction loop is disabled

Fig. 4.12 shows interesting results in the simulation. The top two traces are the capacitor voltage waveforms. The bottom trace is the correction loop controller output voltage waveform. The converter stars at 0s and the capacitor voltages are balanced after a while (400us). At 600us, the controller is disabled by pulling the output down to zero. Without the correction loop, the two capacitor voltages run into imbalance shortly.

4.5 Summary

Following the experimental verification, the analysis work is done in this Chapter. The mechanism for the capacitor voltage imbalance is modeled and simulated. From the modeling, conclusion is drawn that without correction, the voltage imbalance is unavoidable under all conditions. Increasing the capacitor value cannot help to prevent the voltage imbalance. One widely used PI controller is employed for the voltage imbalance correction. The modeling results show the possibility for the capacitor voltage to be balanced, which is verified by the followed simulation results. The same circuit parameters are used in both modeling and simulation and the results agree with each other.

5. CLAMPING TECHNIQUES IN DC-DC CONVERTERS

5.1 Introduction

The advances in VLSI (very large scale integration) technologies impose a new challenge for delivering high-quality power to digital ICs. As more and more transistors are integrated into the integrated circuit chip, and with the transistors operating at higher switching frequencies, the power level to supply the chip is significantly increasing [E1-E3]. High reliability is always a critical requirement for on-board DC-DC converters to meet the power conversion challenges for the modern computing and communication systems. High efficiency, which related firmly to the reliability, is among the main concerns to evaluate the power supply systems. Less power dissipation leads to better thermal management and less component deratings, which increase the reliability for the on-board DC-DC converters. In the isolated on-board DC-DC converter, parasitics always have significant effect on the overall system efficiency. The parasitics existing in the converter are shown as below:

- Inductance. This includes the leakage inductance and magnetizing inductance for the isolation transformer, the trace inductance and the lead inductance for the power components. When switching frequency goes high, the effect of the inductance becomes more and more significant.
- Capacitance. Such as the output junction capacitance of the MOSFET, power diode and the winding capacitance coming from the planar transformer structure contribute to the parasitic capacitance in the converter.

- Resistance. All PCB traces, transformer and inductor windings, MOSFET at on-state and the ESR of the capacitors contribute to the parasitic resistance.

Due to the availability of the parasitics, the oscillation loops formed by reisitance, inductance and capacitance are presented in the converter. Ringings caused by oscillation are sometimes serious enough to cause both EMI issue and significant extra power losses. This part of energy stored in the inductance and capacitance, although appears small, may cause additional thermal issues like hot spot, over temperature break down for the components if it is not put in good management. In the following section of this Chapter, several energy management concepts are proposed aiming at reducing the losses on the parasitics in isolated on-board DC-DC converters. The first two concepts are proposed to reduce the ringings between the MOSFET junction capacitance and the leakage inductance in half-bridge topology. The third one helps to reduce the freewheeling loss on the magnetizing clamping MOSFET in active forward topology. The fourth one provides a good way to stabilize the driving voltage and can be applied on all self-driven circuit.

5.2 Proposed energy management concepts

Two issues are focused on in the proposed energy management concepts. One is the ringing issue causing by the parasitics such as the leakage inductance of the transformer and the junction capacitance of the MOSFETs, which always leads to serious EMI issue. The natural energy exchange between the parasitic inductance and capacitance is the key reason for the ringing. To remove the ringings, the energy needs to

be stored in an appropriate way instead of being dissipated. The other issue is the power dissipation, which has significant effect on the system efficiency and reliability. As a result, ZVS techniques are investigated, which reduce the switching loss for the MOSFET especially at high switching frequency.

5.2.1 Energy freewheeling concept

This concept is illustrated in Fig. 5.1 with one half-bridge example. When both power switches are off, clamp switch Sclamp conducts carrying the leakage current. The transformer leakage inductor is shorted and the current keeps freewheeling through clamp switch and transformer primary winding instead of flowing through switch S1 and S2 junction capacitor. The junction capacitance of the MOSFETs is not involved in energy commutation. As a result, the ringing is eliminated. The freewheeling energy can be used to obtain ZVS for both MOSFETs by releasing the current to discharge the junction capacitor before turns the power MOSFETs on. The disadvantage for this clamping concept is that, during freewheeling, the energy is dissipated partly on the clamping MOSFET and transformer winding due to the parasitic resistance. Therefore, this clamping circuit is not suitable for wide line change applications in which small duty ratio causes significant freewheeling loss.

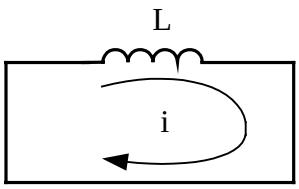


Fig. 5.1 (a) Energy freewheeling concept.

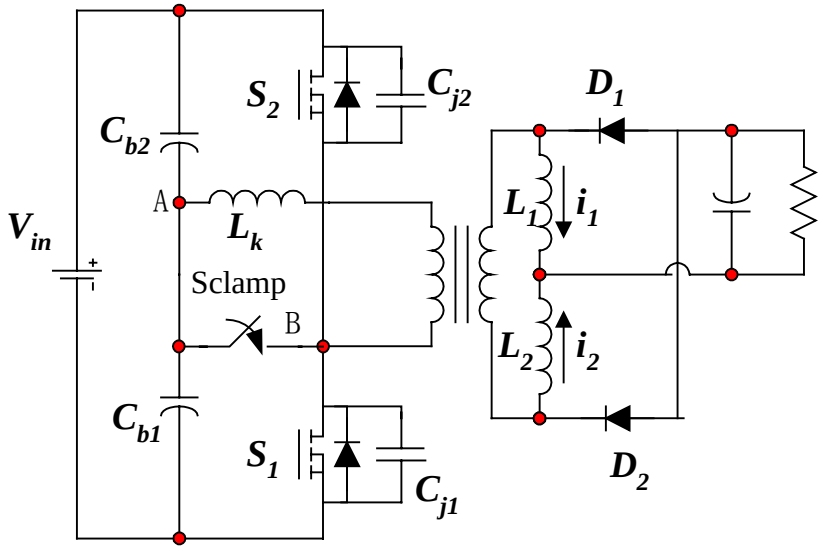


Fig. 5.1 (b) Application example on half-bridge topology

Fig. 5.1 Energy freewheeling concept illustration

5.2.2 Energy storage concept

When the two power MOSFETs are both off, the leakage inductor energy is transferred to a storage capacitor and there is no freewheeling current after the energy is moved from the leakage inductor to clamping capacitor. Fig. 5.2 with one half-bridge example shows the concept.

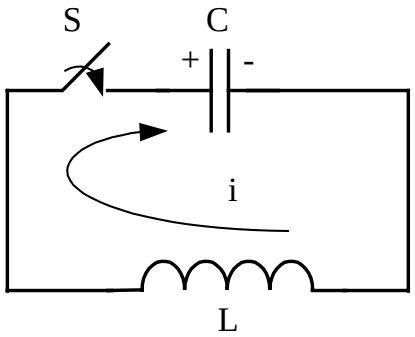


Fig. 5.2 (a)

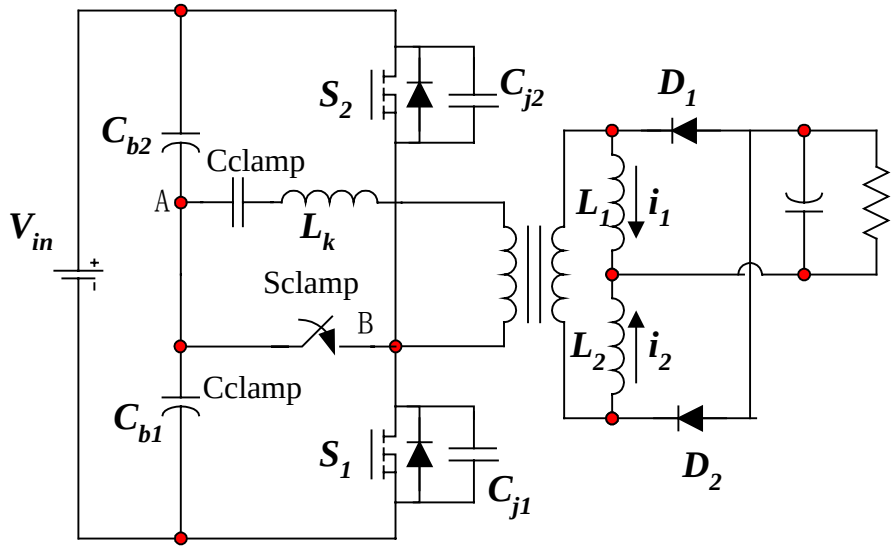


Fig. 5.2 (b)

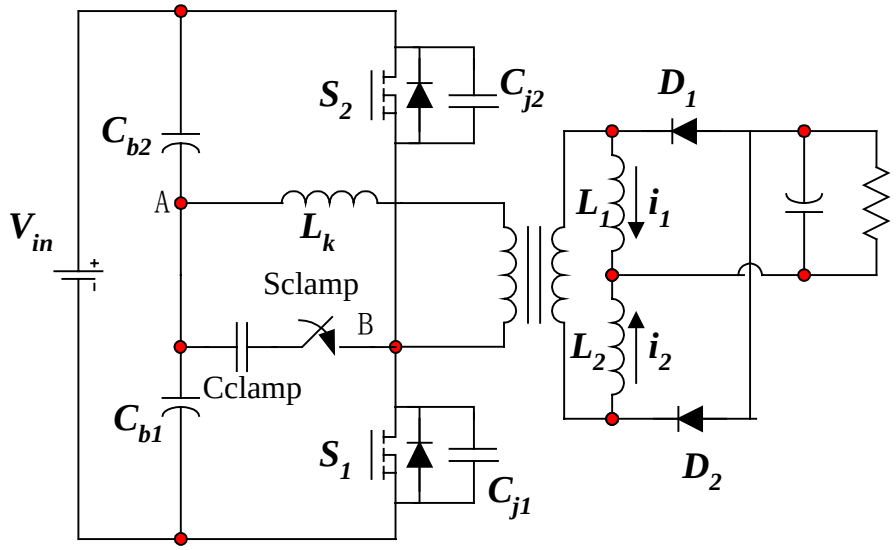


Fig. 5.2 (c)

Fig. 5.2 The illustration of energy storage concept with different clamping capacitor locations

When S1 and S2 are both off, Sclamp conducts so that the leakage current flowing through the clamping capacitor, which is large in value compared with the junction capacitance of the power MOSFETs. When the current drops to zero, which

indicates that all leakage inductor energy is moved to the clamping capacitor, the clamping switch is turned off so that the energy on clamping capacitor cannot move back to the leakage inductor. The whole energy transferring process is short compared with the off time of the power MOSFETs. As a result, no significant freewheeling loss incurred compared with the energy freewheeling concept. This concept is suitable for small duty ratio applications in which freewheeling loss is saved during the long interval when both power switches are off. The disadvantage for this concept is that, it does not make use of the stored energy.

5.2.3 Energy storage and release concept

This concept is well illustrated in active-clamp forward topology as shown in Fig. 5.3.

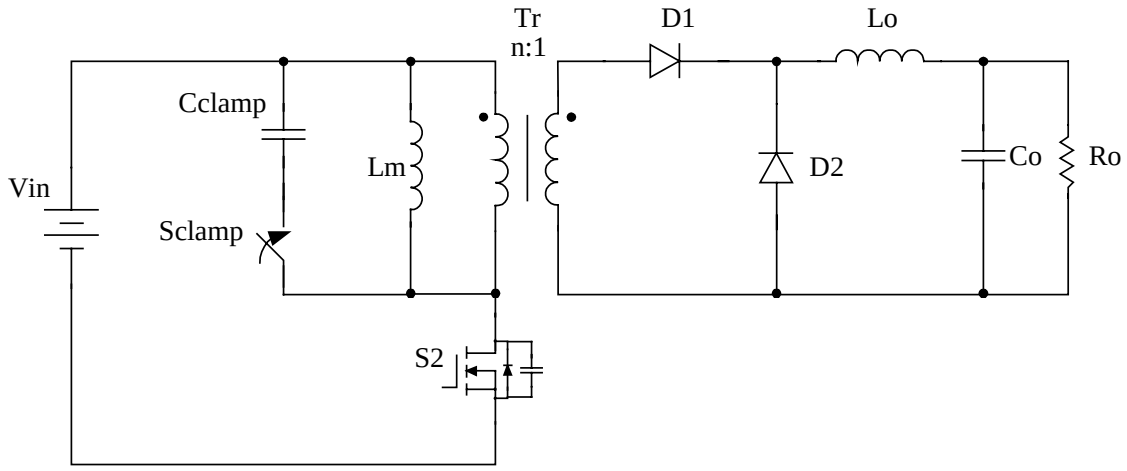


Fig. 5.3 The energy storage and release concept illustration

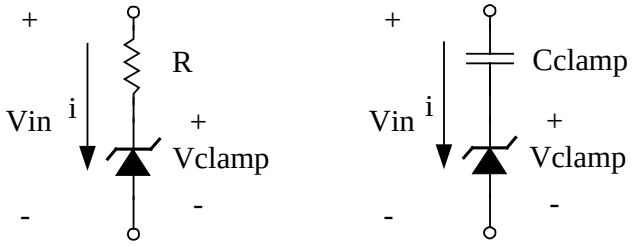
When power switch S1 turns off, Slcmap is turned on so that the magnetizing current flows through the clamping capacitor causing its voltage increase. When the current

drops to zero, the magnetizing energy is moved totally from the magnetizing inductor to the clamping capacitor. Sclamp is turned off and the energy is kept in the clamping capacitor for the main part of the interval when the power MOSFET is off. Before the power MOSFET is turned on, Sclamp is turned on so that the energy stored in the clamp capacitor is released to charge the magnetizing inductor and right before power MOSFET is turned on (certain deadtime between them is to be designed), Sclamp is turned off, which allow the magnetizing inductor current discharging the junction capacitor of the power MOSFET to create the ZVS condition for the power MOSFET to be turned on.

5.2.4 Lossless zener diode clamping concept

The zener diode is widely used when stable voltage is required such as bias circuit for ICs, clamping circuit preventing the voltage spikes from destroying the components. Fig. 5.4 (a) shows the typical applications of zener diode in the clamping circuit, in which one resistor R withstands the voltage difference between Vin and the voltage on zener diode Vclamp. The power consumed by the resistor is calculated by:

$$P_{diss} = \frac{(V_{in} - V_{clamp})^2}{R} \tag{5.1}$$



(a) (b)

Fig. 5.4 The lossless zener diode concept illustration

In order to keep the power dissipation low, large resistor value is normally selected for applications like bias supply circuit for the Opams and the voltage reference circuit, in which the load does not need much current (several mA). When load requires more current (such like the peak driving current of MOSFET gate), the circuit shown in Fig. 5.4 (a) is not suitable for applications due to the significant loss on the resistor. The lossless concept is introduced in Fig. 5.4 (b), in which the lossy resistor is replaced by a capacitor. Fig. 5.5 shows one application example of the lossless zener in self-driven circuit. The clamping capacitor C1 and C2 provide the voltage drop so that MOSFET SR1 and SR2 gate voltage is maintained stable when transformer voltage changes. Since capacitor does not consume power, the power loss is greatly reduced compared with its resistor-zener counterpart. The capacitor is placed in series with the MOSFET gate serving as a differentiator. As a result, the low impendence allows high instant driving current flowing through it so that the proposed circuit has excellent driving capability.

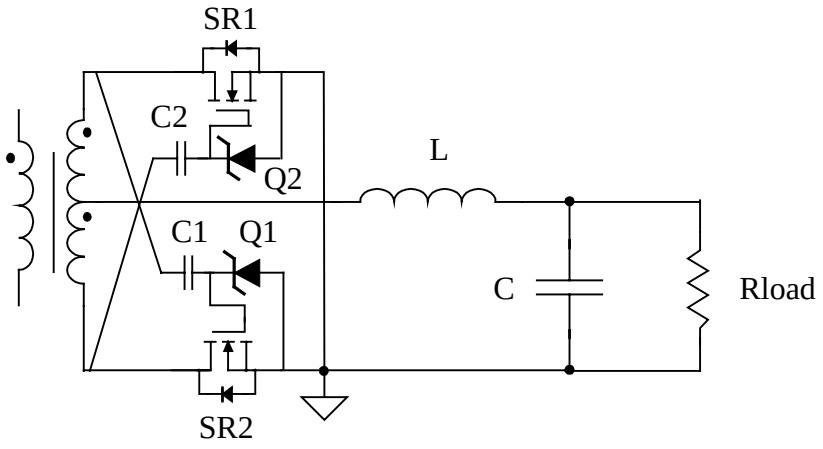


Fig. 5.5 The lossless zener diode concept applied on self-driven circuit

5.3 The energy freewheeling concept applied on half-bridge topology

5.3.1 Introduction

In isolated DC-DC converters, the isolation transformer leakage inductance is an important factor that affects the performance of converters. A variety of topologies and control methods are proposed to improve the converter performance by utilizing the transformer leakage inductance [E4-E10]. The phase-shifted full-bridge [E4] and the active-clamp forward [E5] DC-DC converters are good examples to utilize the transformer leakage inductance to achieve ZVS and further reduce EMI noises.

There are two conventional control schemes for half-bridge DC-DC converters, namely, asymmetric control [E6-E8] and symmetric control [E9-E11]. Symmetric controlled half-bridge DC-DC converter [E9-E13] has simple configuration and operates with symmetric components stresses. However, the two primary switches operate at hard switching condition and there exist leakage-inductance-related ringing losses and problems. To damp such ringing, usually, dissipative snubber circuits are employed across switches, resulting in leakage inductance energy dissipated in the snubber circuits. Consequently, the efficiency is degraded and the power level is limited.

Asymmetric control scheme applies two complementary signals to the two half-bridge switches. Due to the nearly zero dead time between two switches, the primary-side ringing problem is eliminated and ZVS for both switches can be achieved with the help of the transformer leakage inductance [E6-E8]. However, asymmetric half-bridge converter suffers from the asymmetric components stresses distribution in the

corresponding components and a DC bias in the transformer. Therefore, it is not suitable for applications with wide input-voltage range [E6][E8]. Furthermore, the DC gain of the asymmetric-controlled half-bridge converter is nonlinear [E8], resulting in lower duty cycle at high line voltage compared to the symmetric-controlled half-bridge converter, which results in degrading the converter performance at high line input.

An active current clamping method was proposed in [E9-E10] to achieve ZVS of switches and to attenuate the ringing. During the off-time interval (when both switches are turned off), the leakage inductance current freewheels through the auxiliary circuits. Before turning on the main switches, auxiliary switches interrupt the freewheeling path, such that the energy in the leakage inductance is released to create ZVS condition for main switches. However, this method has two main demerits: The first is that the value of the leakage inductance should be high enough, and the other is that high circulating current exists especially at low duty cycle. This means that this scheme is not suited for applications with wide-range of input voltage. In [E11], a DCS controlled ZVS half-bridge topology is proposed. However, it has similar disadvantage, which is that circulating conduction loss increases significantly at high line input.

Fig. 5.6 shows the conventional half-bridge DC-DC converter with current doubler rectification, where L_k is the transformer leakage inductance and C_{j1} and C_{j2} are junction capacitances of MOSFET switches S_1 and S_2, respectively.

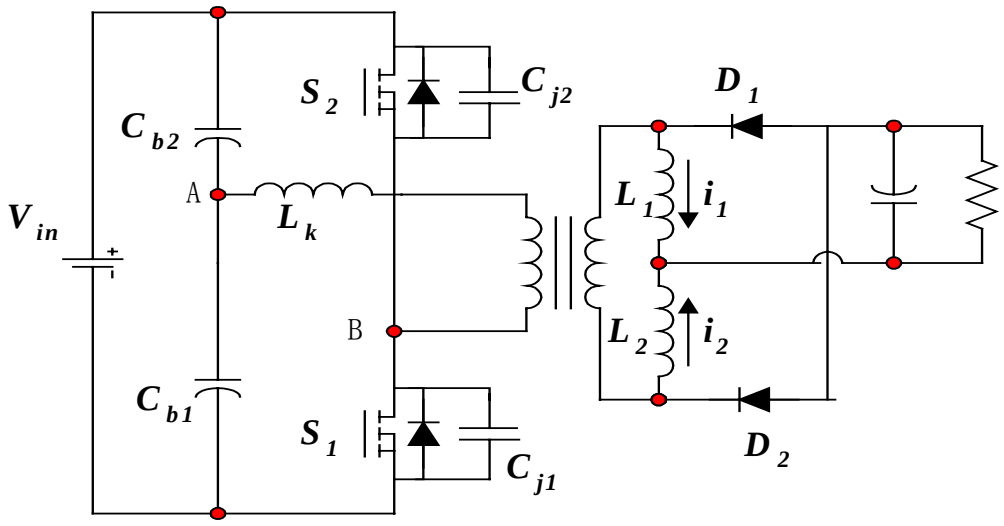


Fig. 5.6 Half-bridge isolated DC-DC converter

During the freewheeling period, when both switches S_1 and S_2 are off, the transformer secondary is shorted by the two conducting diodes. Assuming that the junction capacitances of switches are much smaller than it is for the capacitors C_{b1} and C_{b2}, and neglecting other parasitic capacitances and inductances, if the two body-diodes are ideal, the energy in the leakage inductance will be recycled to the DC bus through the two diodes with undamped oscillation between the transformer leakage inductance and the junction capacitances. The energy involved in the oscillation is determined by the junction capacitances and input voltage as follows:

$$E = \frac{1}{2} C_j V_{in}^{\ 2} \tag{5.2}$$

where C_j is the individual MOSFETs' junction capacitance.

However, body-diodes of the MOSFETs have undesirable reverse-recovery characteristics, especially for high voltage rating MOSFETs, which results in more energy involved in the oscillation. As a result, the ringing is more severe and there are

more reverse-recovery and ringing losses due to the non-ideality of body-diodes. Moreover, the ringing and reverse-recovery may lead to EMI problems.

Usually, snubber circuits are added to damp such ringing. The RC (Resistor-Capacitor) series snubber across a switch or transformer primary windings is the most common snubber circuit. Depending on the size of the snubbers, the energy remained in the leakage inductance may be partly recycled to the DC bus, or totally dissipated in the snubbers. For a small snubber, body diodes conduct to partly recycle the energy with part of energy dissipated in the snubber. For a large snubber, the energy in the leakage inductance may be fully dissipated in the RC snubbers without the involvement of body diodes. In the later case, the power losses increase significantly with the increase of primary-side peak current and switching frequency.

5.3.2 The proposed energy freewheeling clamping on half-bridge topology

The proposed energy freewheeling clamping concept is applied on half-bridge topology as shown in Fig. 5.7.

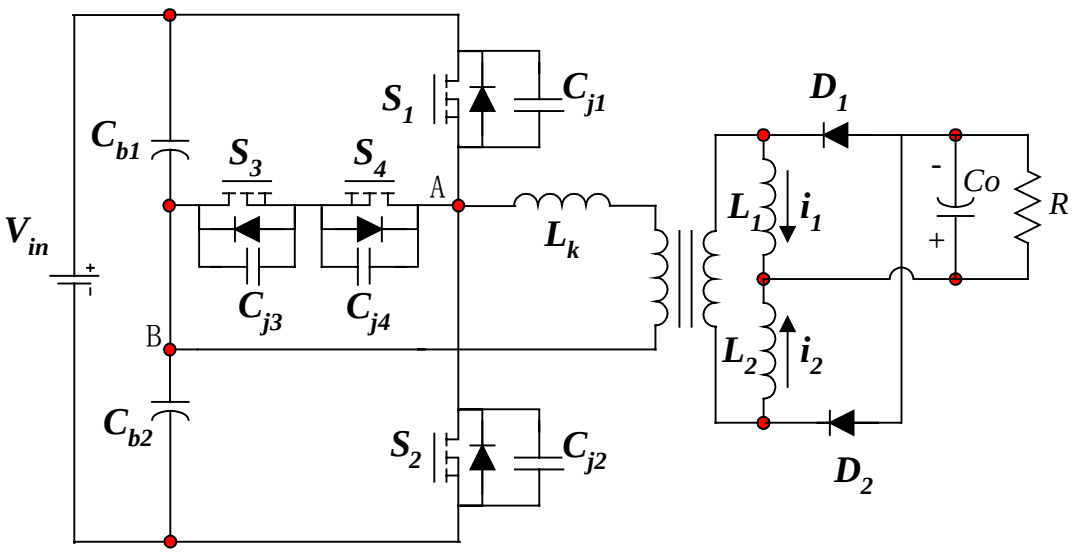


Fig. 5.7 The proposed energy freewheeling concept applied on half-bridge topology

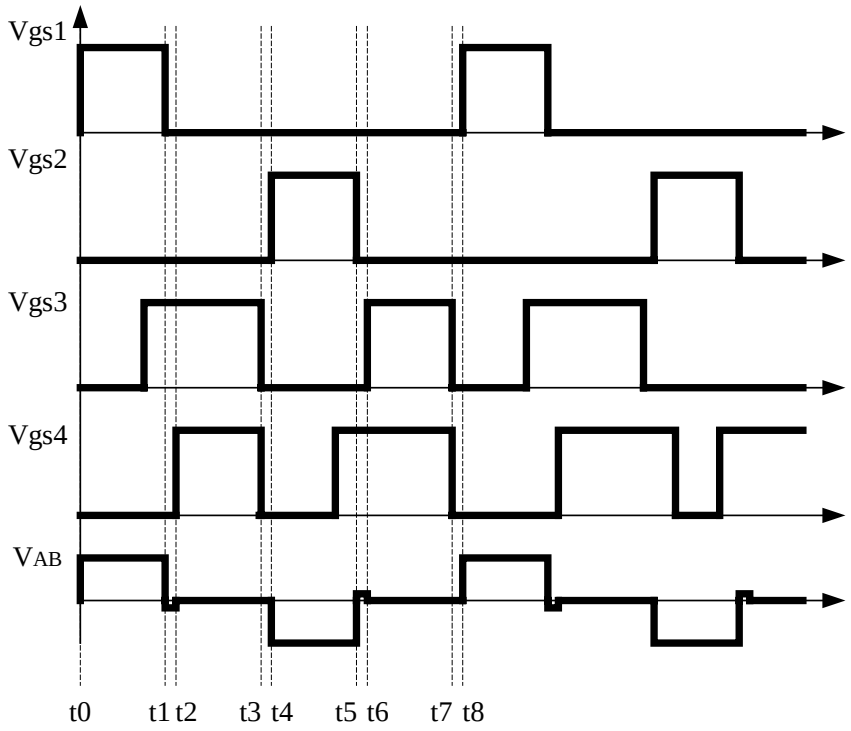


Fig. 5.8 Operation modes description for the proposed half-bridge with the energy freewheeling concept

Before the operation modes analysis, assumptions are made as the following:

A. The primary side two half-bridge capacitors Cb1, Cb2 and the output capacitor Co are big enough so that the voltage across them is constant. L1 and L2 in current doubler are big enough so that $i_{L1} = i_{L2} = 1/2 I_{out}$.

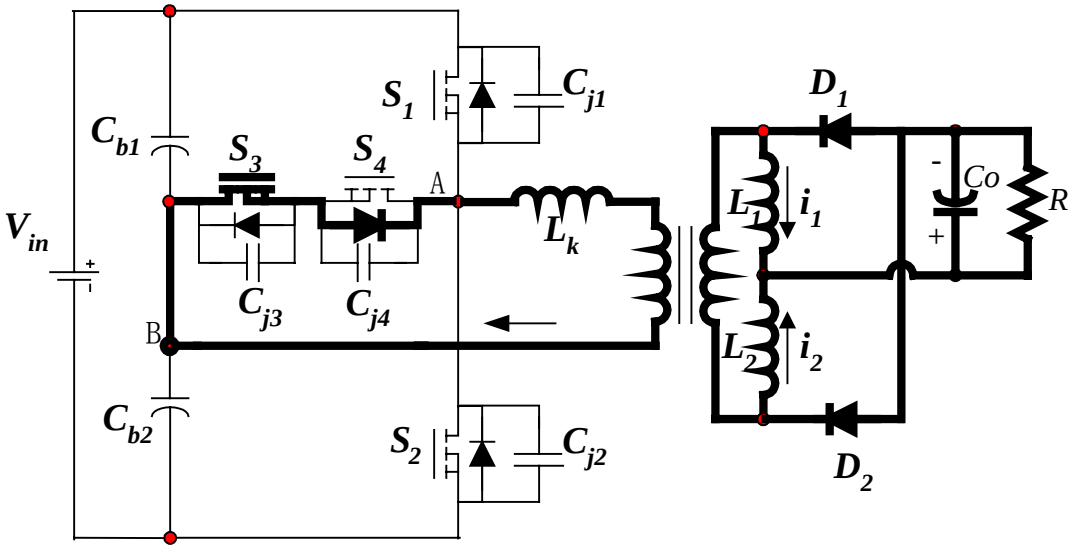
B. The magnetizing inductance is big enough so that the magnetizing current is ignored.

C. The secondary side diode is ideal, the forward voltage drop and reverse recovery is ignored.

D. Ignore all trace parasitics.

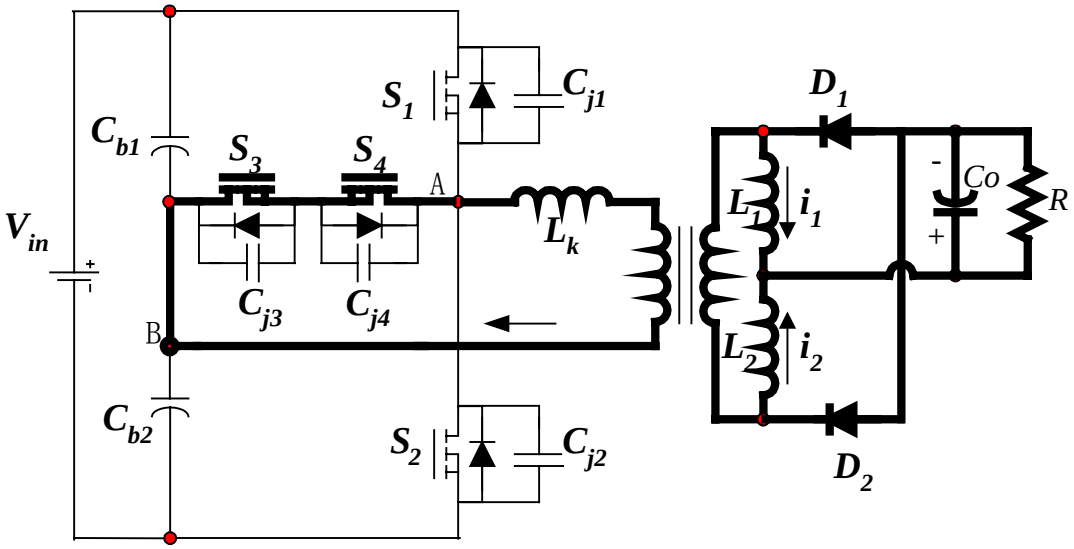
The main equivalent operation modes are shown in Fig. 5.8 and Fig. 5.9. They are described as follows:

Mode 1 *($t_1 < t < t_2$):* Initially, it is assumed that S_1 was conducting and S_3 was turned on with Zero-Current-Switching (ZCS). At $t = t_1$, S_1 is turned off, causing the primary current i_p to charge the junction capacitance C_{j1} and discharge C_{j2}. When the voltage across C_{j1} is charged to half of input voltage V_{in}, the leakage inductance current will flow through S_3 and the body diode of S_4 creating the ZVS condition for S4 to be turned on. Since leakage current does not flow through junction capacitor Cj1 and Cj2 after they are charged/discharge to 1/2Vin, the ringings, which is normally found in conventional half-bridge topology, are not presented in the proposed circuit due to the clamping of S3 and S4 branch. Considering the fact that the transformer is shorted, the leakage current continues to freewheel.



Mode 1

Fig. 5.9 (a)



Mode 2

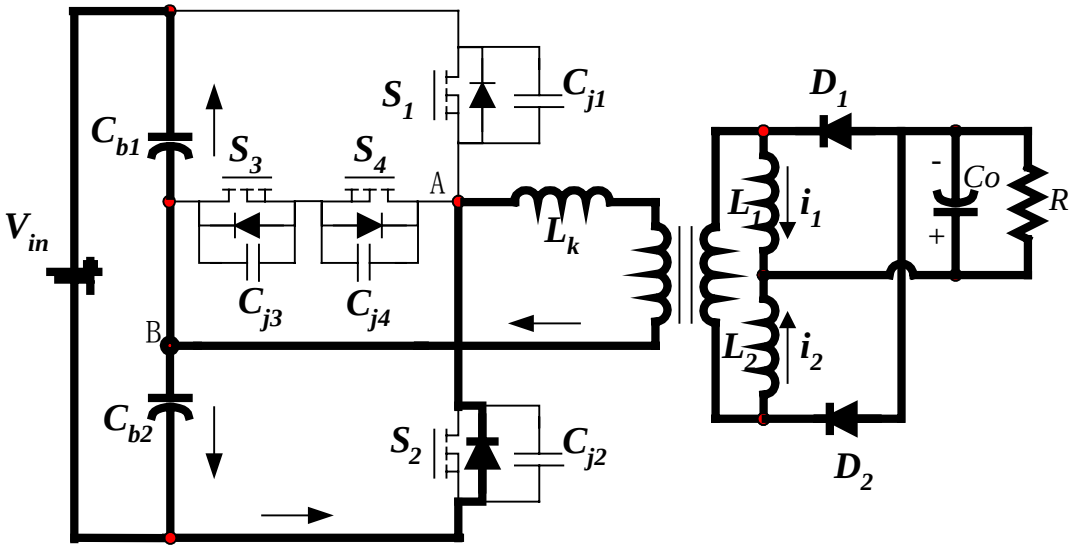
Fig. 5.9 (b)

Mode 2 *(t2<t<t3):* At t2, S4 is turned on with ZVS. Since the transformer is shorted and the voltage across S3 and S4 is negligible, the leakage current keeps freewheeling through S3, S4 and the transformer primary winding. The power dissipation during the freewheeling interval is calculated as:

$$W_{fw} = I_k \cdot (2R_{ds})^2 \cdot (1-D)\frac{T}{2} \qquad (5.3)$$

In which, I_k is the reflected load current and is calculated as: $I_k = \frac{n_s}{2n_p} Io$, where np and ns are transformer primary and secondary turns number respectively, Io is the load current. Rds is the conduction resistance of the MOSFETs S3 and S4. D is duty ratio of the power switches defined as the conduction time over half a switching period. T is the switching period.

From the above expression, it is clear that small Rds can reduce the freewheeling loss during the freewheeling interval. Therefore, MOSFET with low on-resistance is preferred for this application.



Mode 3

Fig. 5.9 (c)

Mode 3 *(t3<t<t4):* At t3, both MOSFETs are off, the current through leakage inductor begins to charge Cj1, Cj3 and Cj4 and discharge Cj2. When Vds of S2 drops to zero, the

body diode of S2 conduct carrying all the leakage current and charging for Cj1, Cj3 and Cj4 is finished. The current though leakage inductor should be big enough so that voltage across S2 is able to drop to zero to obtain ZVS condition for S2 to be turned on. The minimum load current to obtain ZVS for S2 is calculated as follows:

$$\frac{1}{2}L_k \cdot I_k^{\,2} = C_{jc} \cdot (\frac{V_{in}}{2})^2 + C_j \cdot (\frac{V_{in}}{2})^2 \tag{5.4}$$

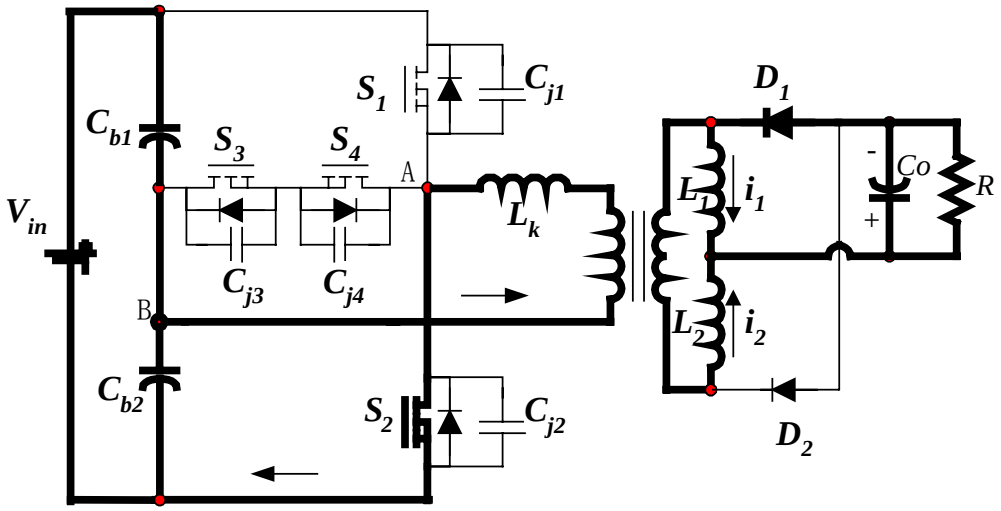
$$Ik = \frac{I_{out}}{2} \cdot \frac{n_p}{n_s} \tag{5.5}$$

$$I_{out} = \sqrt{\frac{(4C_j + C_{jc})}{2L_k}} \cdot V_{in} \cdot \frac{n_p}{n_s} \tag{5.6}$$

Where, Cj is the junction capacitance of the power MOSFET S1 and S2, Cjc is the junction capacitance of the clamping MOSFET S3 and S4. Vin is input voltage, Lk is the leakage inductance, np and ns are primary and secondary transformer turns number respectively. If load current is less than the minimum current Iout, S2 loses soft switching condition and suffers turn-on loss, which hurts the converter efficiency.

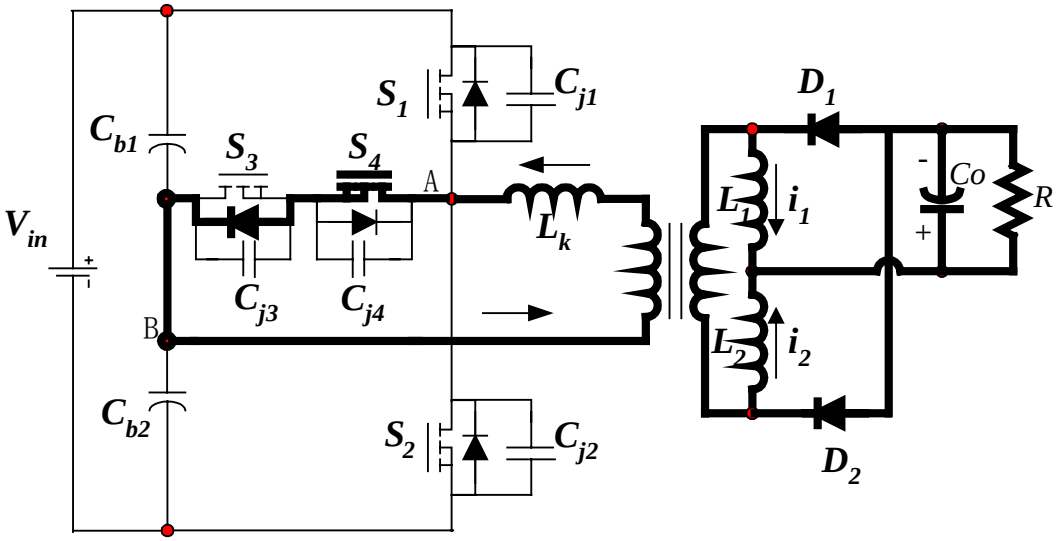
Mode 4 *(t4<t<t5):* At t4, S2 is turned on with ZVS. Power is delivered from primary side to secondary side.

Mode 5 *(t5<t<t6):* Prior to t5, S4 is turned on with ZCS. At t5, S2 is turned off. Similarly, Cj1 and Cj2 is discharged and charged respectively so that Vds of S2 rise to 1/2Vin. Then the leakage current flows through S4, body diode of S3 and transformer. As a result, the ringings are eliminated since no current flows through junction capacitor of the power MOSFET S1 and S2.



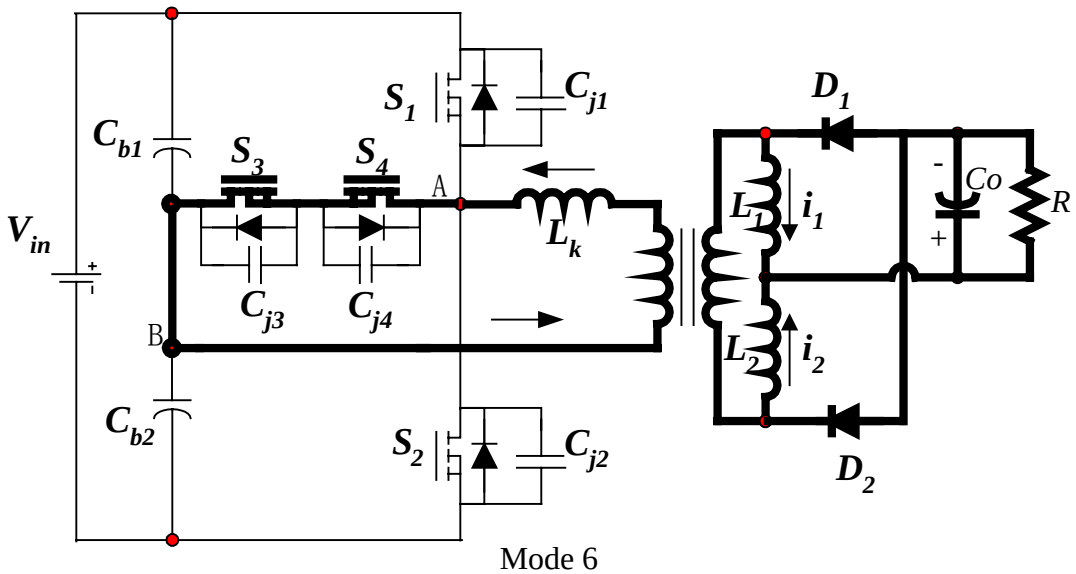
Mode 4

Fig. 5.9 (d)



Mode 5

Fig. 5.9 (e)

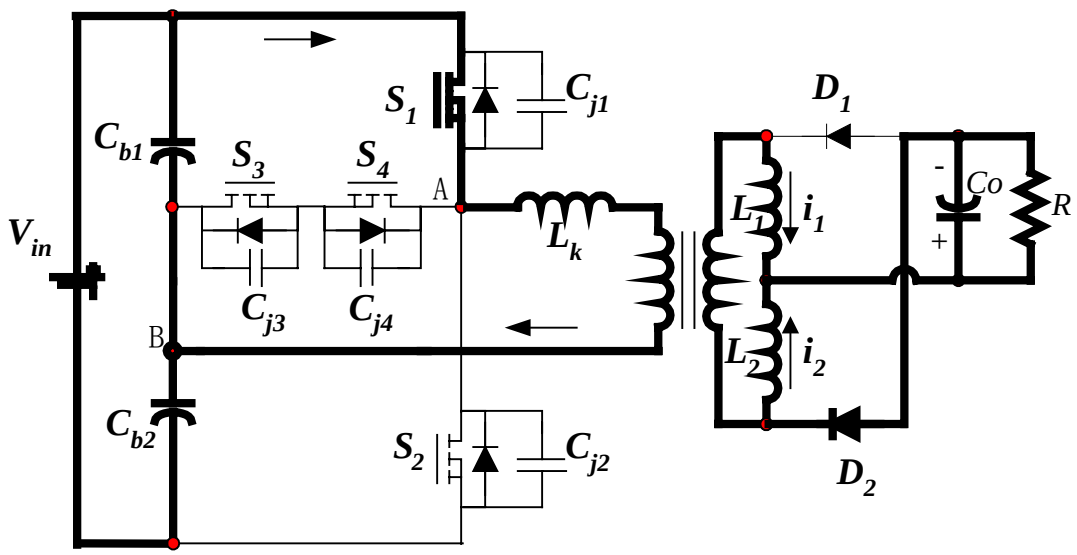


Mode 6

Fig. 5.9 (f)

Mode 6 *(t6<t<t7):* This mode is similar with Mode 2. The leakage current keeps freewheeling through S3, S4 and transformer primary winding. The power dissipation is equal to the one in Mode 2.

Mode 7 *(t7<t<t8):* At t7, both S3 and S4 are turned off, the leakage current charge/discharge S2 and S1. Similarly, there is minimum load current to obtain ZVS condition for S1 to be turned to reduce the switching loss, which is given in the analysis before.



Mode 7

Fig. 5.9 (g)

Fig. 5.9 Operation mode analysis for the proposed clamped half-bridge topology

Mode 8 *(t8<t<t1):* At t8, S1 is turned on with ZVS. The converter delivers power from the primary side to the secondary side. One whole switching period is finished.

5.3.3 Simulation verifications

The proposed clamping scheme is simulated with the following parameters:

Vin=48V, Vout=1V, fs=300kHz, Cb1=Cb2=1uF, D=0.375, np=8, ns=1, L1=l2=600nH, Lk=200nH, Co=470uF.

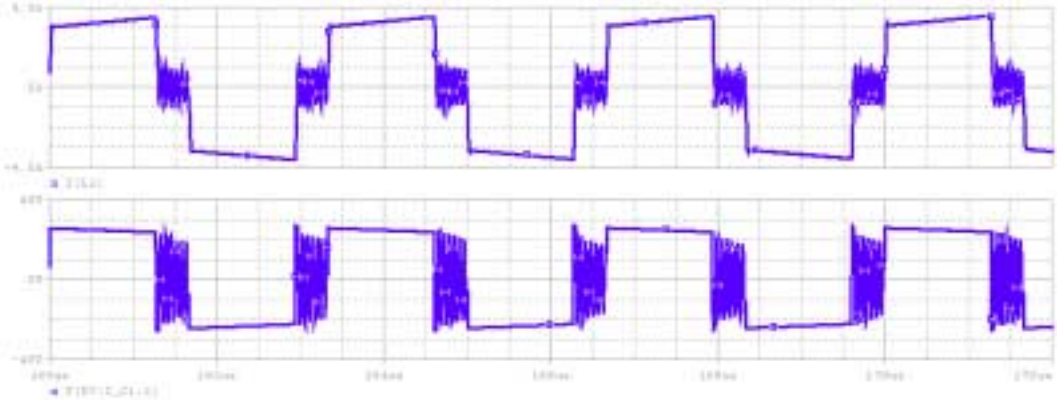


Fig. 5.10 (a) No clamping

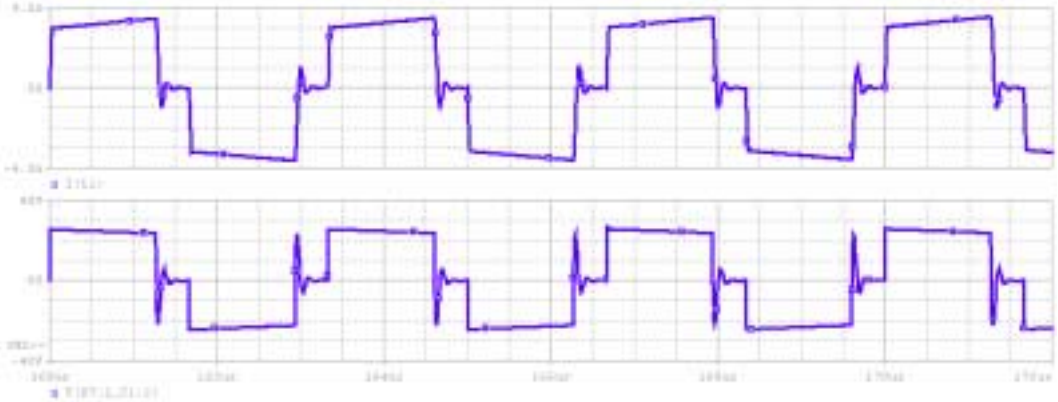


Fig. 5.10 (b) With RC snubber across low side MOSFET (S2). R=10Ohm, C=2nF

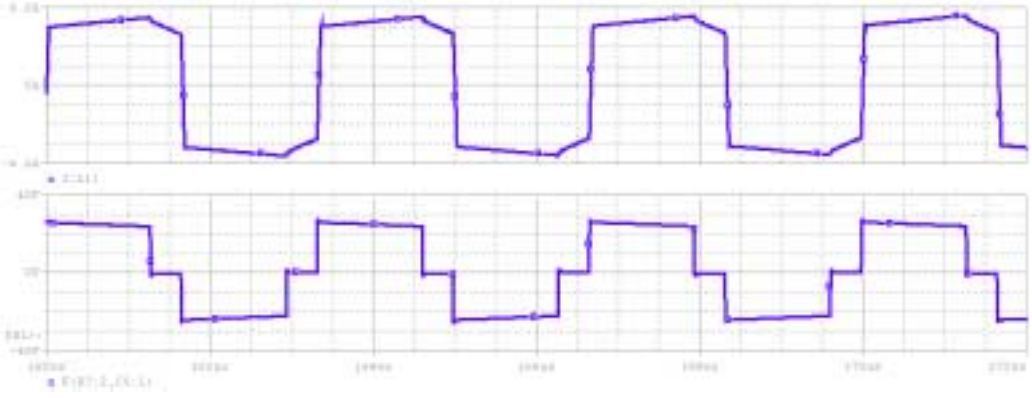


Fig. 5.10 (c) With the proposed active-clamping circuit

Fig. 5.10 Transformer primary side winding current vs. voltage

In Fig. 5.10, the transformer winding current and voltage waveforms in three cases are compared with the same power stage parameters. Fig. 5.10 (a) illustrate the waveform in the conventional half-bridge topology. The serous ringing during the off-time of the two power MOSFETs indicate EMI issues and power losses. With a RC snubber added across the low-side MOSFET of the half-bridge, the ringing is damped significantly. The penalty is the power dissipated on the snubber circuit. With the proposed active-clamping circuit, clean waveforms are observed in Fig. 5.10 (c). Even there is some power loss as analyzed before, it is not as significant as the one in the RC snubber, which is totally dissipated on the resistor. Therefore, the proposed active-clamping circuit is verified and can be applied on half-bridge topology to eliminate the ringing.

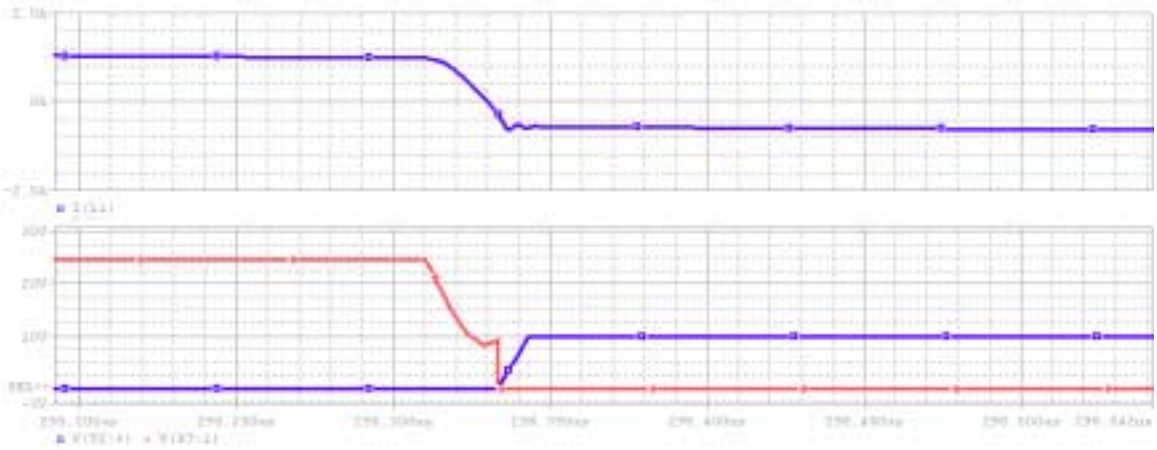


Fig. 5.11 (a) Iout=14A, S2 loses ZVS

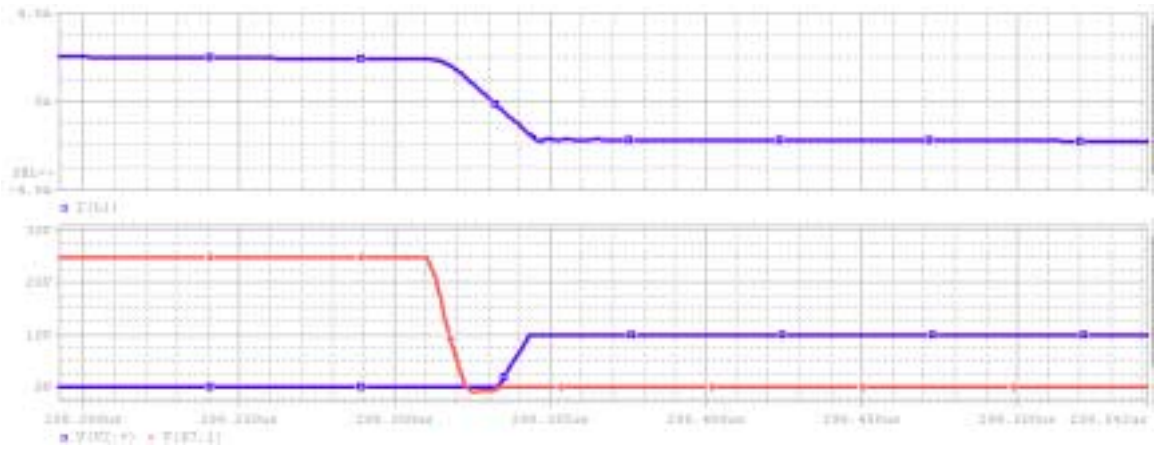


Fig. 5.11 (b) Iout=30A, S2 is turned on with ZVS

Fig. 5.11 ZVS condition vs. load current

(Top trace: leakage current. Bottom trace: Vds of S2 (red) and Vgs of S2 (blue))

Fig. 5.11 shows the ZVS condition for the half-bridge topology employing the proposed active-clamping circuit. When load current is 14A, the energy stored in the leakage inductor is insufficient to discharge the MOSFET junction capacitance, which leads to hard switching for the low-side MOSFET. When the load current increased to 30A, the leakage inductor has enough current to fully discharge the junction capacitance of the MOSFET. ZVS is well illustrated, in which the MOSFET is turned on after its drain to source voltage drops to zero.

5.3.4 Summary

The above analysis and verifications allows the following to be highlighted:

- Due to the oscillation between the MOSFET junction capacitance and the transformer leakage inductance, ringings exist in the conventional symmetrical

half-bridge topology, which brings EMI issue and degraded converter performance.

- The proposed energy freewheeling clamping circuit shorts the transformer primary side during the freewheeling time when two power MOSFETs are both off. Since the leakage current does not flow through the power MOSFET junction capacitor after it is charged to half the input voltage, the ringing is eliminated.
- The proposed clamping scheme is verified by simulation.

5.4 The energy storage concept applied on half-bridge topology

5.4.1 Proposed active-clamping circuit

A clamping concept is proposed as shown in the dashed-line frame of Fig. 5.12 (b). With the proposed clamping snubber, the energy in the leakage inductance can be recycled into the voltage source. It is important to note that the diodes used in the snubber have better characteristics than body-diodes of the MOSFETs. Employing the clamping concept, a variety of practical active-clamp snubber circuits are proposed as shown in Fig. 5.13, where the capacitor Cs is used to absorb the energy in the leakage inductance and damp the ringing. In Fig. 5.13 (a), the diode D_3 and D_4 are external fast-reverse-recovery or schottky diodes, to simplify the circuits, body diodes of switch S_3 and S_4 can act as diodes as shown in Fig. 5.13 (b). Both topologies have the same drive timing and principal of operation. Basically, during the freewheeling period when both switches are off, since the transformer secondary side is shorted, the leakage inductance energy cannot

be delivered to output, and the middle branch provides paths to transfer the leakage inductance energy to the capacitor C_s.

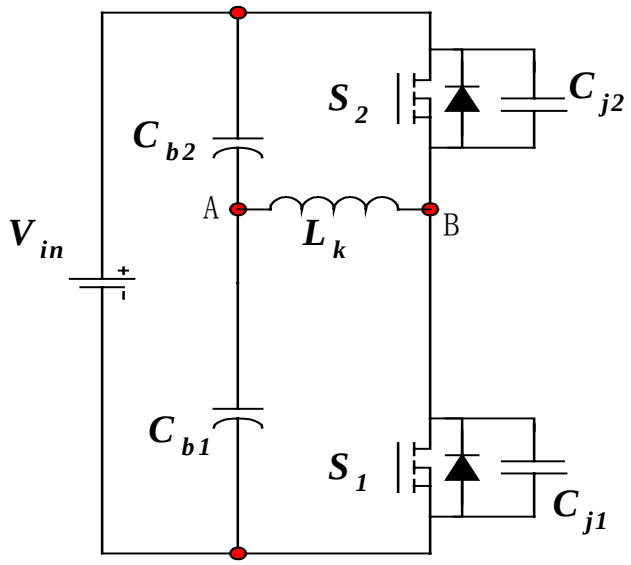


Fig. 5.12 (a) Without snubber

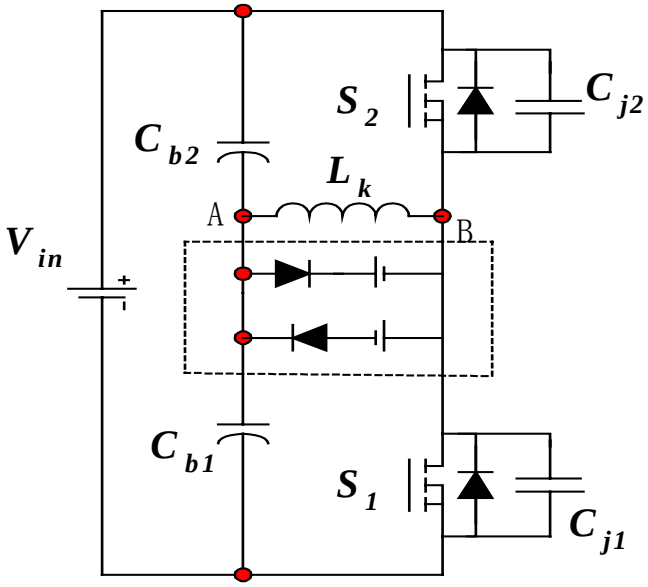


Fig. 5.12 (b) With Clamp-circuit concept

Fig. 5.12 Equivalent circuits during the freewheeling period

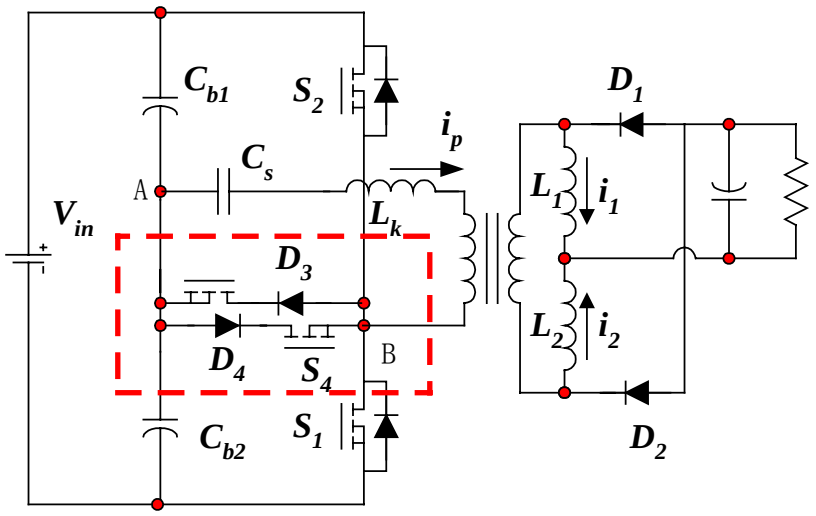


Fig. 5.13 (a) Topology A

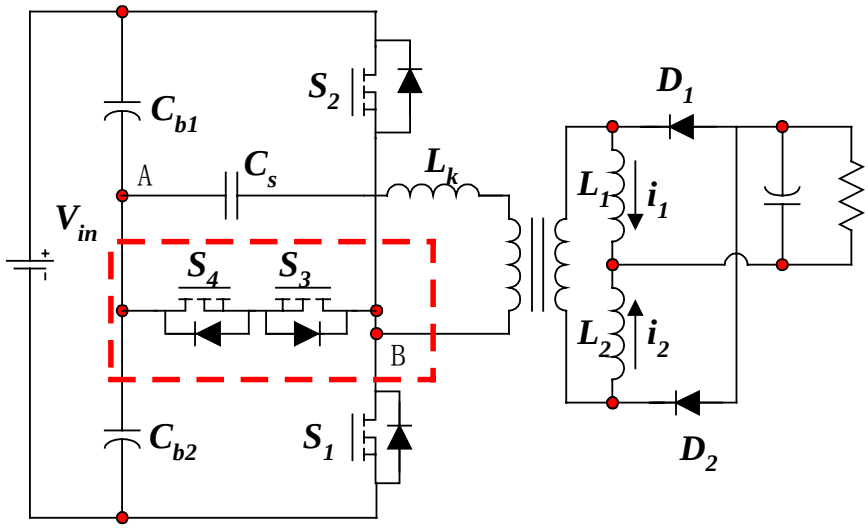


Fig. 5.13 (b) Topology B

Fig. 5.13 Proposed active-clamp snubber circuits in half-bridge DC-DC converter

Taking the topology in Fig. 5.13 (a) as an example for the principle of operation analysis, Fig. 5.14 shows the key operational waveforms. To simplify the analysis of the

operation modes, components are considered ideal except otherwise indicated. The main equivalent operation modes are shown in Fig. 5.15, and described as follows:

Mode 1 *($t_1 < t < t_2$):* Initially, it is assumed that S_1 was conducting and S_3 was turned on with Zero-Current-Switching (ZCS). At $t = t_1$, S_1 is turned off, causing the primary current i_p to charge the junction capacitance C_{j1} and discharge C_{j2}. When the voltage across C_{j1} is charged to -half of input voltage V_{in}, the leakage inductance current will flow through D_3, C_s, and S_3. Considering the fact that the transformer is shorted and there is a DC voltage across C_s, the leakage current continues to charge the capacitor C_s until the current resets to zero at t_2. At the end of this mode, all the energy in the leakage inductance is transferred to the capacitor C_s.

Mode 2 *($t_2 < t < t_4$)*: Since the diode D_3 blocks any potential reverse current in its branch, the reverse oscillation path through S_3 and D_3 is blocked. Considering the possibility to use schottky diode as D_3, the diode reverse recovery current can be eliminated. However, because the voltage $v_{AB} = 0$ is not the steady state, the voltage across C_s will cause the voltage v_{AB} to oscillate until $v_{AB} = V_{cs}$. Since the voltage across Cs is much smaller than half of the input voltage, the MOSFET body-diodes will not be involved in the oscillation, and thus, the ringing is negligible. Therefore, there are no body-diode-related losses and the ringing loss is very small. At $t = t_3$, since both the voltage across and the current through S_3 are zero, S_3 can be turned off with Zero-Voltage Zero-Current Switching (ZVZCS).

Mode 3 ($t_4 < t < t_5$): S_2 is turned on at $t = t_4$ causing the leakage inductance current to start charging from zero at the following slope:

$$\frac{di_{Lk}}{dt} = \frac{0.5V_{in} + V_{cs}(t)}{L_K} \tag{5.7}$$

Where $V_{cs}(t)$ is the voltage across the capacitor Cs. The smaller the leakage inductance is, the faster its current chargeup will be, until it becomes equal to the reflected inductor current, causing the diode D_2 to be blocked and the converter to start transferring energy from the primary-side to the secondary-side. This current will continue to charge at a slope of:

$$\frac{di_{Lk}}{dt} = \frac{0.5V_{in} + V_{cs}(t) - \frac{n_1}{n_2} \cdot V_o}{L_K + (\frac{n_1}{n_2})^2 \cdot L_2} \tag{5.8}$$

Where L_2 is the secondary inductor, n_1 and n_2 are the transformer primary number of turns and secondary number of turns, respectively, and V_o is the output voltage. During this interval, the inductor current is charged and the capacitor Cs is discharged. The polarity of the voltage across the capacitor Cs will reverse during this interval. The auxiliary switch S_4 is turned on with ZVZCS since the diode D_4 block the current.

During this mode, the capacitor Cs is charged linearly with the reflected output current. Assuming the output current is constant during the mode, the reflected current through the capacitor Cs is:

$$I_c = \frac{n_2}{2n_1} I_o \tag{5.9}$$

The capacitor voltage change during the mode is:

$$V_{Csch} = \frac{1}{Cs} \frac{n_2}{2n_1} I_o DT \tag{5.10}$$

Where $DT = t_5 - t_4$; n_1 and n_2 are transformer primary and secondary turns number, respectively. Ignoring the capacitor Cs voltage change due to resetting leakage inductance current, the capacitor Cs voltage can be described as:

$$V_{cs}(t) = \frac{1}{Cs}\frac{n_2}{2n_1} I_o \left[\frac{1}{2} DT - (t - t_4)\right] \tag{5.11}$$

Mode 4 ($t_5 < t < t_6$): This mode is similar to mode 1. S_2 is turned off at $t = t_5$, causing the primary current i_p to charge C_{j2} and to discharge C_{j1}. When the voltage across C_{j2} is charged to half of the input voltage, the leakage inductance current flows through D_4, C_s, and S_4. Considering the fact that the transformer is shorted and there is a DC voltage across C_s, the leakage current continues to charge the capacitor C_s until the current resets to zero at t_6. At the end of this mode, all the energy in the leakage inductance is transferred to the capacitor C_s.

At the end of the Mode 3, the capacitor Cs voltage is:

$$V_{cs}(t_5) = -\frac{1}{4Cs}\frac{n_2}{n_1} I_o DT \tag{5.12}$$

Assuming the capacitor Cs has sufficient large capacitance and the leakage inductance current is linearly reset to zero and the capacitor Cs voltage keeps constant during this mode. The leakage inductance current at $t = t_5$ is equal to reflected output current:

$$I_{Lk}(t_5) = \frac{n_2}{2n_1} I_o \tag{5.13}$$

The duration time of this mode T_R can be obtained:

$$T_R = L_k \frac{I_{L_k}(t_5)}{V_{cs}(t_5)} = \frac{2C_s L_k}{DT} \tag{5.14}$$

Mode 5 *($t_6 < t < t_8$)*: This mode is similar to mode 2. After minor oscillation, this mode will end with:

$$V_{C_{j1}} = \frac{1}{2}V_{in} + V_{Cs}(t_6) \tag{5.15}$$

$$V_{C_{j2}} = \frac{1}{2}V_{in} - V_{Cs}(t_6) \tag{5.16}$$

Where $V_{Cs}(t_6) > 0$. At $t = t_7$, the switch S_4 can be turned off with ZVZCS in the same manner described in mode 2 for S_3. $V_{Cs}(t_6)$ will be derived later.

Mode 6 *($t_8 < t < t_{10}$)*: This mode is similar to mode 3. The switch S_1 is turned on and the converter starts to deliver energy from the primary-side to the secondary-side. At $t = t_9$, the auxiliary switch S_3 is turned on with ZVZCS.

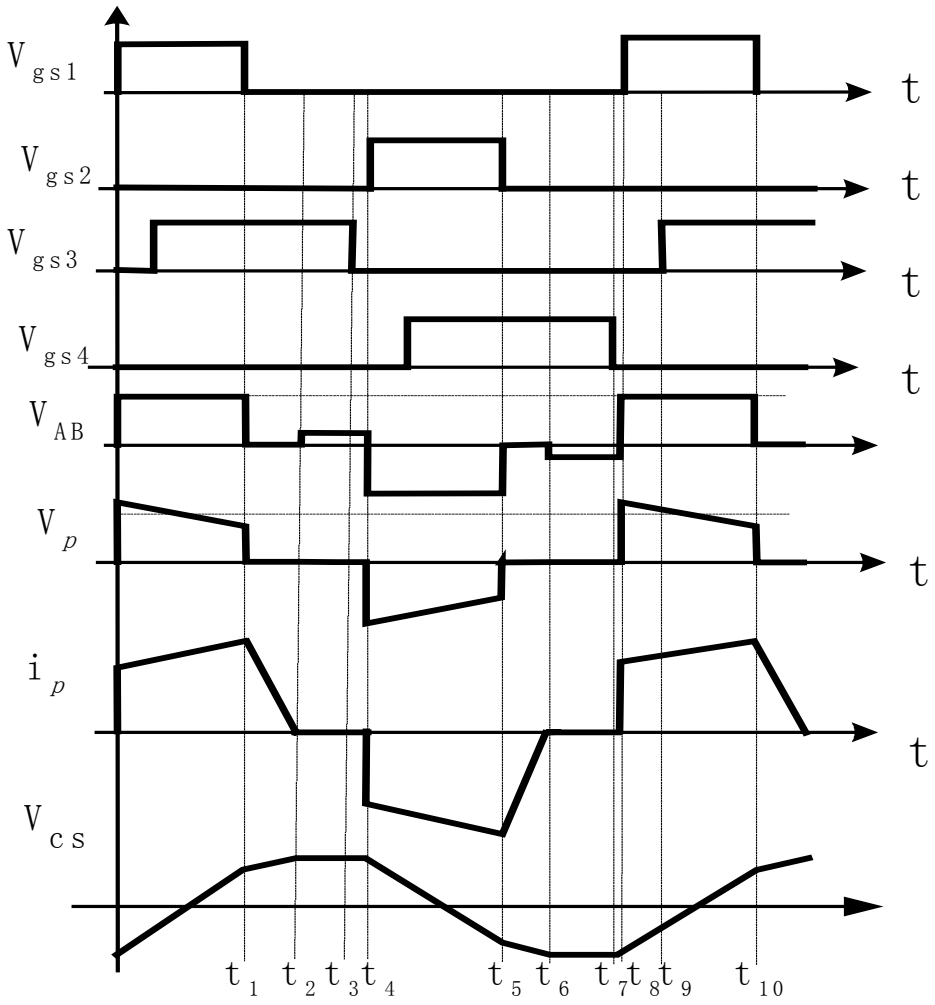


Fig. 5.14 Key theoretical waveforms of the proposed topology

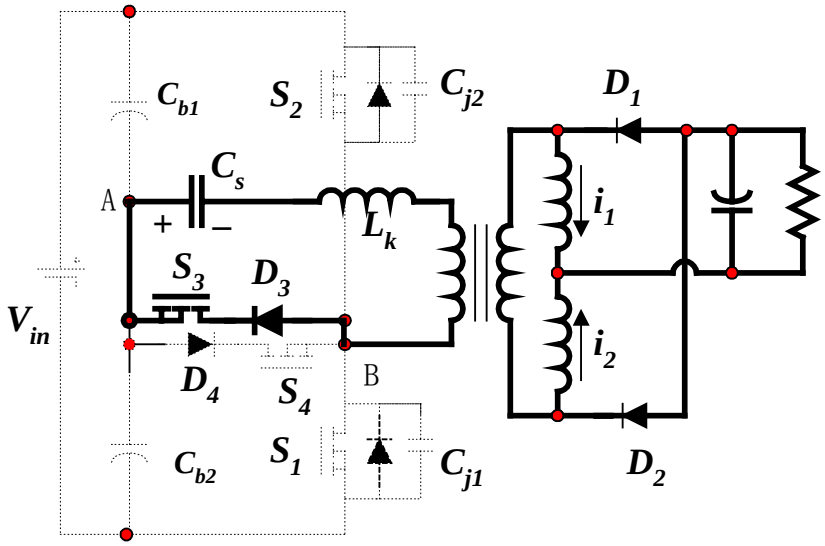


Fig. 5.15 (a) Mode 1

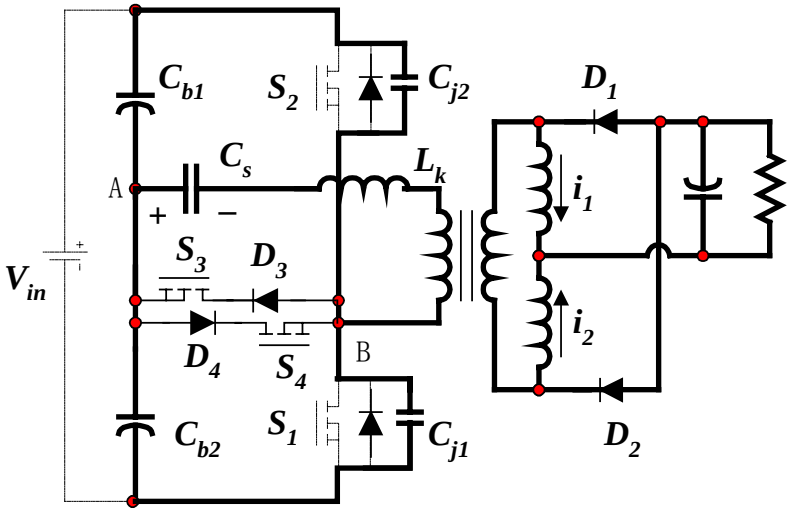


Fig. 5.15 (b) Mode 2

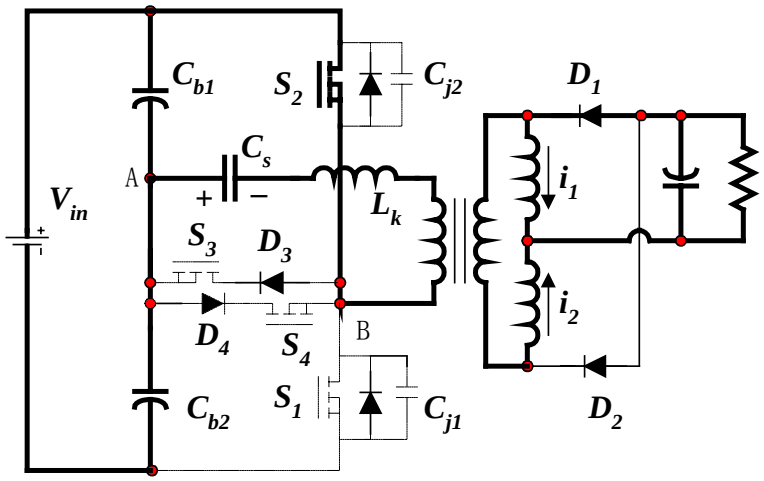


Fig. 5.15 (c) Mode 3

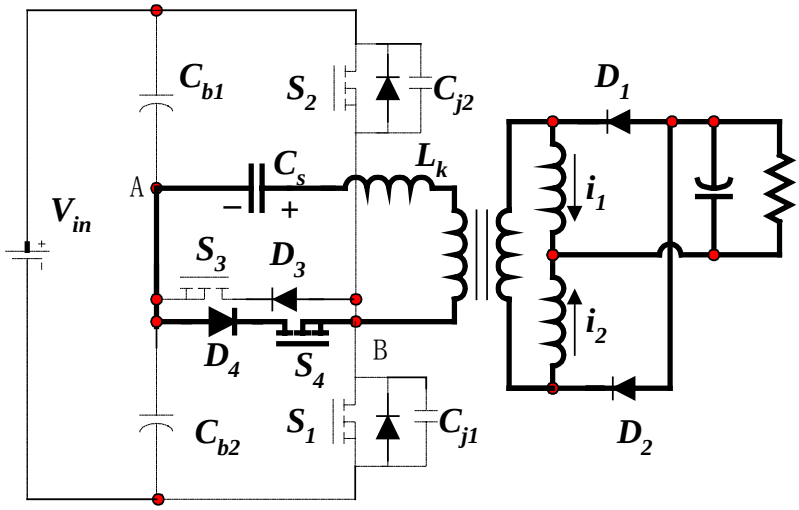


Fig. 5.15 (d) Mode 4

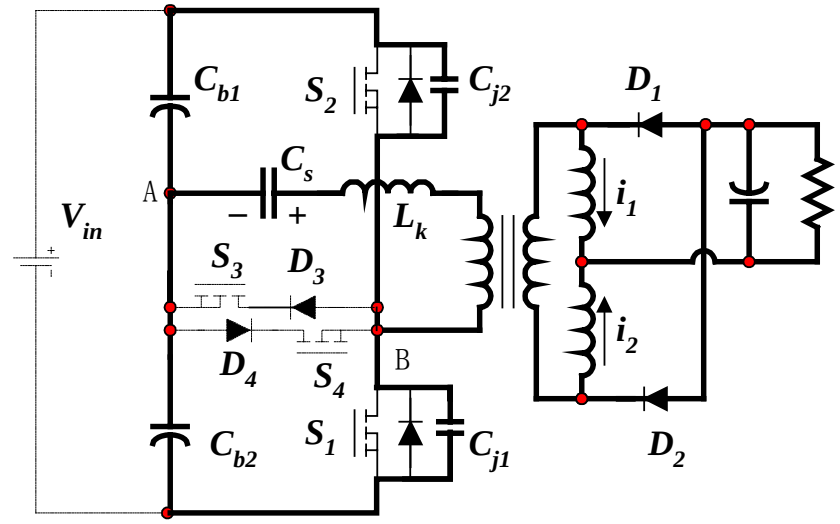


Fig. 5.15 (e) Mode 5

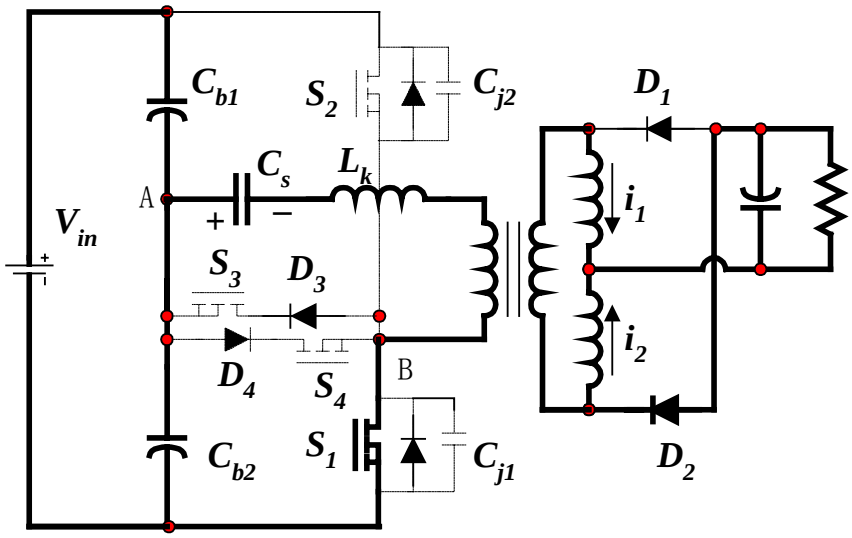


Fig. 5.15 (f) Mode 6

Fig. 5.15 Modes of operation equivalent circuits

5.4.2 Main features and design considerations

5.4.2.1 Main features

As discussed earlier, with the proposed active-clamp snubber, the energy in the leakage inductance is transferred to the capacitor instead of being dissipated in dissipative snubbers. Furthermore, the body diodes of main switches are not involved in the oscillations, such that the switches' body-diodes conduction losses and reverse-recovery losses are eliminated.

The auxiliary switches S_3 and S_4 are turned on with ZVZCS and turned off with ZVZCS. Therefore, the switching losses are minimized. Since the conduction intervals of the auxiliary circuit only account for a very short portion of the whole period, the auxiliary switches and diodes conduction losses are negligible. In addition, all components' voltage stresses in the middle branches are half of the input voltage. Therefore lower voltage and current rated components with lower gate charge can be chosen for auxiliary components. The auxiliary circuits losses are limited compared to the leakage inductance ringing losses.

When the main switches are turned off, the leakage inductance current starts to reset towards zero as shown in Fig. 5.16 (a), where T_R is reset time of leakage inductance current, and T_{on} and T_{off} are the on-time and off-time of the two main switches, respectively. If $T_{off} > T_R$, the operation is the same as described earlier, and the primary voltage and current are as shown in Fig. 5.16 (a). However, if $T_{off} < T_R$, there is not enough time for the leakage inductance to transfer the energy to the capacitor Cs. When the auxiliary switches are turned off, the remained leakage inductance energy is used to

charge/discharge the main switches junction capacitance. In this case, ZVS may be achieved for the main switches, and the corresponding waveforms of the primary voltages and currents are shown in Fig. 5.16 (b).

In other words, depending on the duty cycle width, the proposed snubber topology has two possible operation cases: The small-duty-cycle case, where the converter operates with the active-clamp mode to reduce ringing problem, and the large-duty-cycle case, where the active-clamp interval is reduced, such that the energy in the leakage inductance will be directly used to achieve ZVS for the main switches instead of being transferred into the capacitor Cs. Therefore, this topology is suited for wide input voltage range. At high line, the converter reduces the energy circulation conduction losses, and at low line, the converter reduces the switching losses.

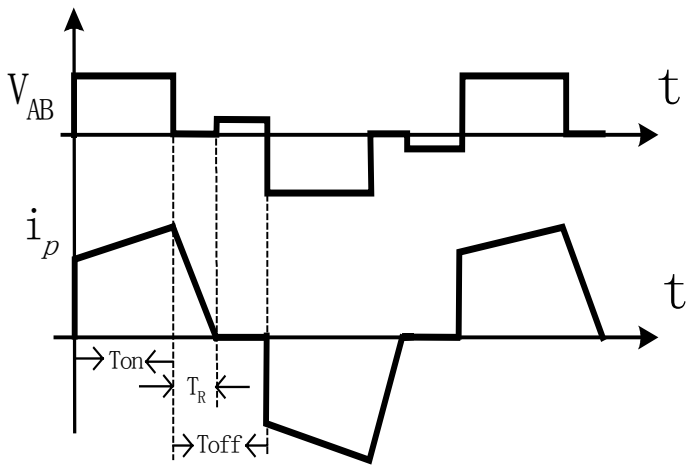


Fig. 5.16 (a) $T_{off} > T_R$

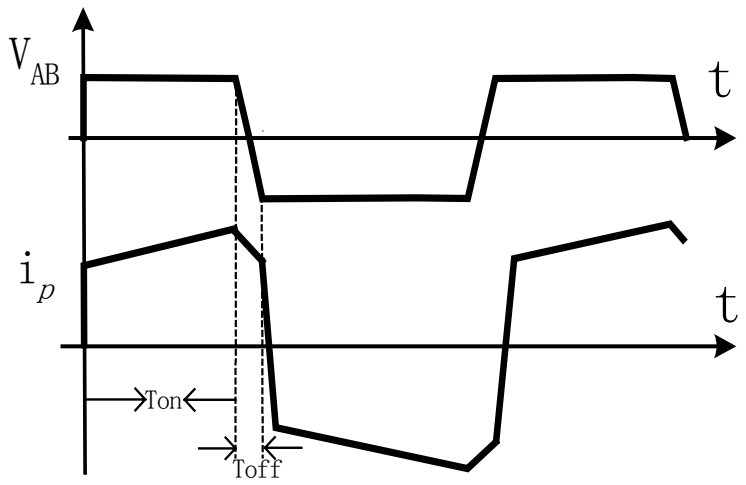


Fig. 5.16 (b) $T_{off} < T_R$

Fig. 5.16 Two possible operation schemes for the proposed converter

The reset time T_R is rewritten as follows:

$$T_R = \frac{2C_s L_k}{DT} \tag{5.17}$$

Where T is the switching period and D is the duty cycle that satisfies $T_{on} = DT$. As shown in Equation (5.17), T_R is independent of the load, which simplifies the design for the capacitance Cs. The voltage stress in Cs is given by:

$$V_{pk} = \frac{DTn_2}{4C_S n_1} I_o \tag{5.18}$$

Where I_o is the converter output current. Cs value can be approximately designed for V_{pk}=10~20%V_{in} at full load.

As matter of fact, capacitor Cs can be removed and the leakage inductance energy is trapped in the middle branch. At the case, the main switches have higher possibilities to achieve ZVS than with capacitor Cs. However, conduction loss may be significant at low

duty cycle operation. In order to determine adding capacitor Cs or not, an appropriate loss comparison can be made based on this following analysis.

For the case without capacitor Cs, assuming the leakage inductance current keeps constant during the freewheeling time (1-D)T, the conduction loss can be estimated as follows:

$$P_{con} = (1-2D)\left[I_{Lk}{}^2 R_{ds(on)} + I_{Lk} V_D \right] \tag{5.19}$$

Where I_{LK} is the leakage inductance current value during the freewheeling mode when two main switches are off. $R_{ds(on)}$ is the on-resistance of Switch S_3 or S_4, V_D is forward voltage drop across body diode of main switches. Substitute Equation (5.13) into Equation (5.19), the conduction loss can be rewrote as:

$$P_{con} = (1-2D)\left[\frac{1}{4}\left(\frac{n_2}{n_1} \right)^2 I_o{}^2 R_{ds(on)} + \frac{n_2}{2n_1} I_o V_D \right] \tag{5.20}$$

In the proposed converter, when Toff > T_R, the main switches operate at hard switching, the switching loss is calculated as:

$$P_{switching} = \frac{1}{T}\int_0^{Ttran} v_{ds} \cdot i_{ds} \cdot dt \tag{5.21}$$

The switching loss of the two switches can be approximated as:

$$P_{switching} = \frac{n_2}{12n_1} V_{in} I_o \frac{T_{on} + T_{off}}{T} \tag{5.22}$$

Depending on Pcon and Pswitching values at certain operating points, the trade-off can be made accordingly. It should be noted that switching loss is hard to estimate accurately. Equations given above are just for a rough estimation.

Compared to the phase-shift full bridge DC-DC converter, the converter switches S_3 and S_4 stand only half of the input voltage versus full input voltage in full-bridge

converter, and switch S_3 and S_4 act as auxiliary switches and stand small current stress. In half-bridge converter, power stress and related switching and conduction loss are mainly put on main switches S_1 and S_2 instead of evenly distributed on 4 main switches in full-bridge DC-DC converters. From this point of view, half bridge DC-DC converter is suitable for lower power level compared to full bridge. Moreover, the proposed active-clamped half-bridge DC-DC converter has options to make trade-off on the capacitance value of Cs or even removing capacitor Cs, which provide design flexibility according to specific applications.

5.4.2.2 Converter DC voltage gain

In the previous analysis, the voltage increase is ignored in Mode 1 and 4, and the converter DC voltage gain is the same as conventional half-bridge DC-DC converter:

$$V_{out} = \frac{n_2 D}{2n_1} V_{in} \qquad (0<D<0.5) \tag{5.23}$$

However, the voltage increases have effect on the converter DC voltage gain. In Mode 4, assuming all the energy in leakage inductance at the end of Mode 3 is transferred in the capacitor Cs without additional loss and voltage change in Mode 4 is ΔV_{cs}, the energy balance equation is expressed as:

$$\frac{1}{2} \cdot Cs \cdot (V_{Cs} + \Delta V_{Cs})^2 - \frac{1}{2} \cdot Cs \cdot V_{Cs}{}^2 = \frac{1}{2} \cdot L_K \cdot (I_o \cdot \frac{n_2}{2n_1})^2 \tag{5.24}$$

where V_{cs} is the voltage value at the end of Mode 3 (t = t_5), which is known from Equation (5.12). Substitute Equation (5.12) into (5.24) and solve Equation (5.24):

$$\Delta V_{Cs} = \frac{n_2 \cdot Io}{4Cs \cdot n_1} (\sqrt{D^2 \cdot T^2 + 4Cs \cdot L_K} - D \cdot T) \tag{5.25}$$

The capacitor voltage value at the end of Mode 4 and 5 are:

$$V_{Cs}(t_8) = V_{Cs}(t_6) = V_{Cs}(t_5) - \Delta V_{Cs} \tag{5.26}$$

Ignoring the duty cycle loss due to leakage inductance, the transformer primary voltage in power delivery modes can be described as:

$$V_{trans\_pri} = \frac{1}{2}V_{in} + V_{Cs} + \Delta V_{Cs} - \frac{V_{Csch}}{DT} \cdot t) \qquad (0 < t < DT) \tag{5.27}$$

where V_{Csch} is the voltage change in power delivery modes that is expressed in Equation (5.10). In power delivery modes, transformer primary voltage is reflected to secondary side to charge an inductor. According to voltage-second balance across an inductor, we have:

$$\int_0^{DT} (V_{trans\_pri} \cdot \frac{n_s}{n_p} - V_{out})dt = V_{out} \cdot (1-D) \cdot T \tag{5.28}$$

Substituting Equation (5.10) and (5.27) into (5.28), solve for Vout:

$$V_{out} = V_{in} \cdot \frac{n_2}{2n_1} \cdot D + \frac{D \cdot Io}{4Cs} \cdot (\frac{n_2}{n_1})^2 \cdot (\sqrt{(D \cdot T)^2 + 4Cs \cdot L_k} - D \cdot T) \tag{5.29}$$

From Equation above, it can be observed that the proposed converter has higher DC gain than the conventional half-bridge DC-DC converter. The increase of DC gain is proportional to the load current. For typical applications, numerical analysis shows the DC addition is ignorable compared with output voltage.

5.4.2.3 Design example

A snubber design procedure is given with an example. The specifications of the converter are Vin: 36V~75V, Vout: 3.3V, Iout: 30A, transformer turn ratio: 4:2, the measured primary-side leakage inductance: 300nH, and switching frequency: 200kHz. At

nominal input voltage Vin = 48V, the corresponding duty cycle is around 0.3 and the off-time is (0.5-0.3) T=1uS. Design T_R=600nS, from Equation (5.14) Cs=1.5uF. According to Equation (5.18), the capacitor Cs voltage stress is 3.75V at D=0.3. At low line input Vin=36V, the corresponding duty cycle is 0.4; capacitor Cs voltage stress is highest, which is 5V. A 16V ceramic compactor is selected capacitor Cs.

5.4.3 Simulation and experimental verifications

The proposed topology with the active-clamp snubber was first simulated with Pspice platform with manufacturer Spice models Si7856 and Si7892 for primary-side and secondary-side MOSFETs, respectively. Experimental prototype were built and tested with the following specifications: V_{in}=36~75V, V_{out}=3.3V, Io=25A, switching frequency of 200kHz, isolation transformer turns ratio of 4:2 with leakage inductance of 220nH as reflected to the primary-side, Cs value of 3uF, and output inductances values of 2.3uH.

In both the simulation and the experimental work, the conventional RC series snubber and the proposed active-clamp snubber were compared with the same specifications and conditions for the half-bridge DC-DC converter. Fig. 5.17 and Fig. 5.18 are simulation waveforms at the operating point of Vin=48V, Vout=3.3V, Iout=25A, fs=200kHz. Fig. 5.17 shows primary voltage V_{AB} and transformer primary current waveforms for different snubber circuit cases. If there is no any snubbers on the primary side, the leakage inductance and MOSFET junction capacitance oscillate during the interval of freewheeling when both switches are off as analyzed before. The oscillation involves body-diode reverse recovery and leads to EMI issues. The corresponding

oscillation waveforms are shown in Fig. 5.17 (a). With series RC snubber across transformer primary side winding, the oscillation is damped as shown in Fig. 5.17 (b), however, leakage inductance energy is dissipated with degraded efficiency. With the proposed active-clamp snubber, the ringing is eliminated and clean waveforms are observed in Fig. 5.17 (c).

As analyzed before, both auxiliary switch S_3 and S_4 turn on and off under ZVZCS conditions. Fig. 5.18 shows both switches' waveforms of drive voltages, drain-source voltages and drain currents. It is clearly observed that both switches turn on with zero voltage and zero current, and turn off with zero voltage and current. Thus the switching loss of the auxiliary switches is nearly zero.

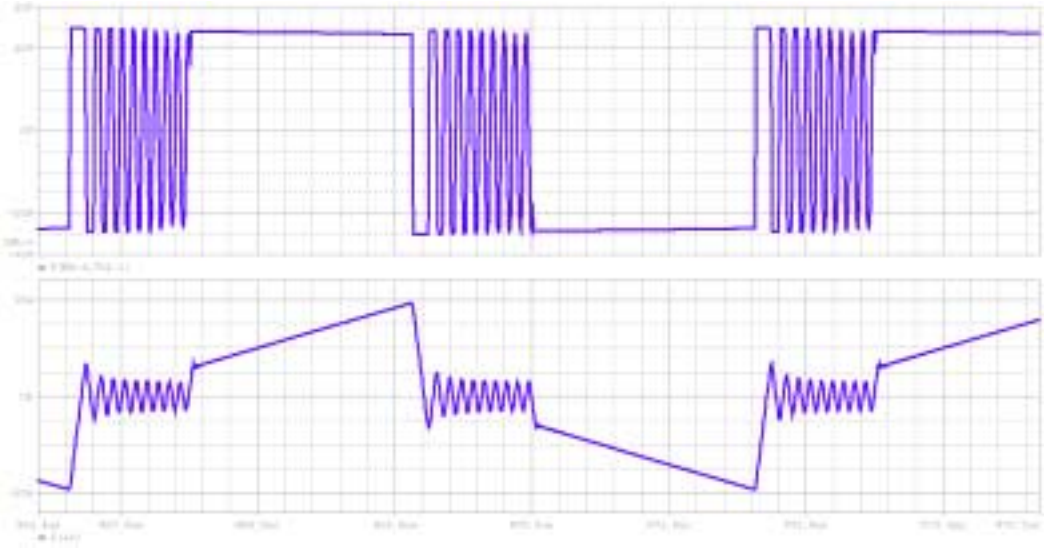


Fig. 5.17 (a) Without snubber

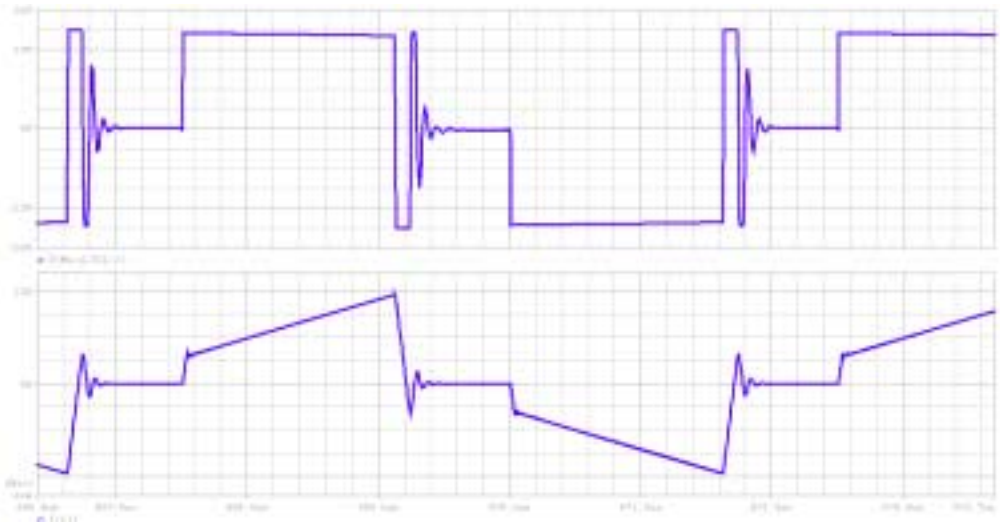


Fig. 5.17 (b) With conventional dissipative RC series snubber (R=30 ohm, C=2nF)

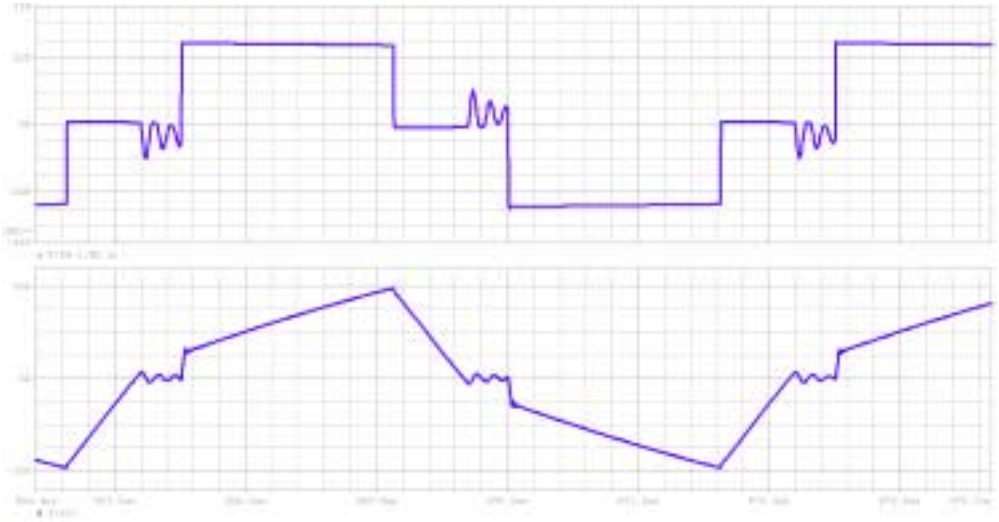


Fig. 5.17 (c) With active-clamp snubber (Cs=3uF)

Fig. 5.17 Simulation waveforms comparison

(Top trace: voltage V_{AB}; Bottom trace: transformer primary current)

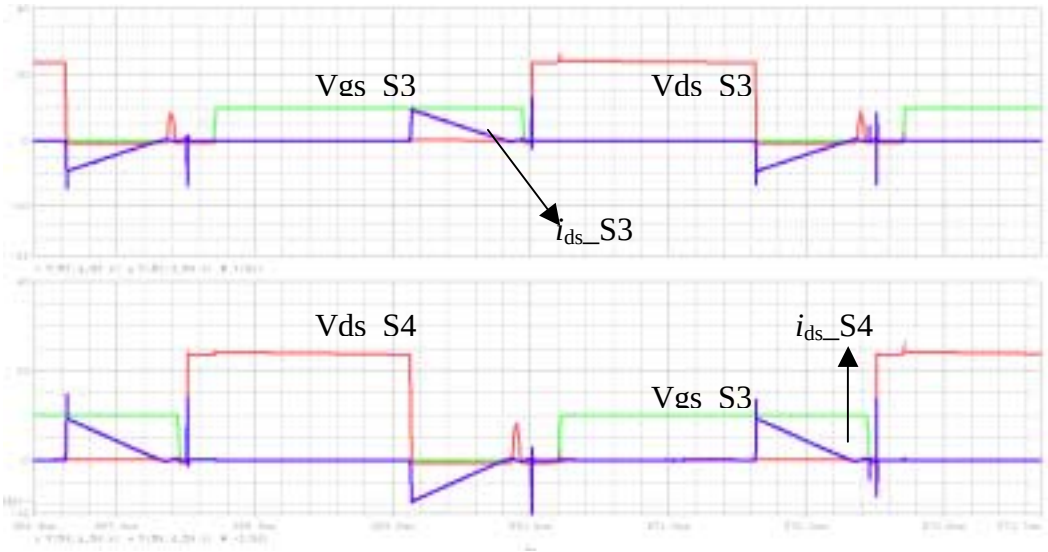


Fig. 5.18 ZVZCS waveforms of auxiliary switches

As analyzed before, at low line input, the duty cycle is maximized and the freewheeling period is minimized such that the energy trapped in the transformer leakage inductance cannot be completely transferred to the capacitor. With the turn-off of auxiliary switch S_3 and S_4, the remained leakage inductance energy will be released to charge/discharge MOSFET junction capacitance, such that ZVS may be achieved for the switch S_1 and S_2, in which case waveforms are shown in Fig. 5.19. The primary voltage V_{AB} and transformer current waveforms are shown in Fig. 5.19 (a), it can be seen that no ringing occurs during the freewheeling time. The ZVS switching waveforms of the switch S_1 and S_2 are shown in Fig. 5.19 (b). S_3 and S_4 switching waveforms are shown in Fig. 5.19 (c), where S_3 and S_4 turn on with ZVZCS.

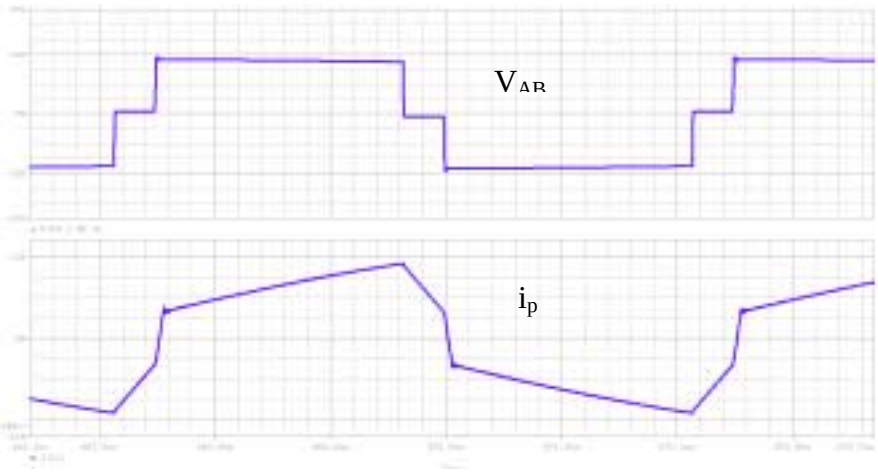


Fig. 5.19 (a) Primary voltage V_{AB} and transformer current

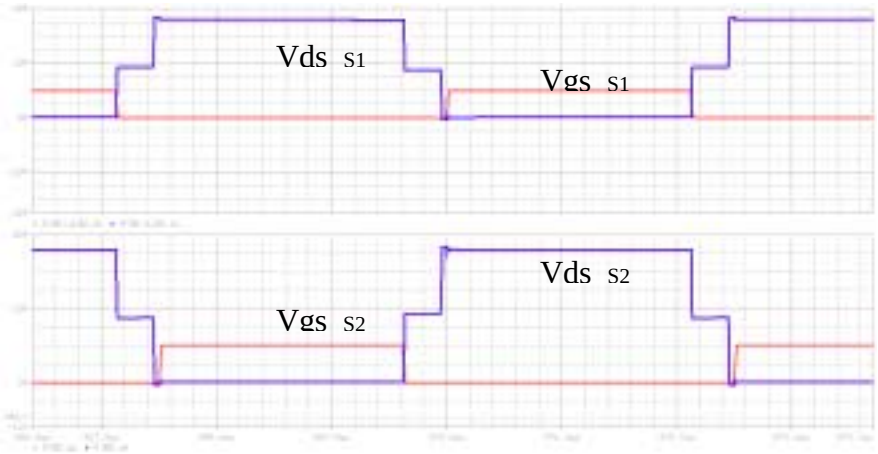


Fig. 5.19 (b) ZVS waveforms of the switch S_1 and S_2

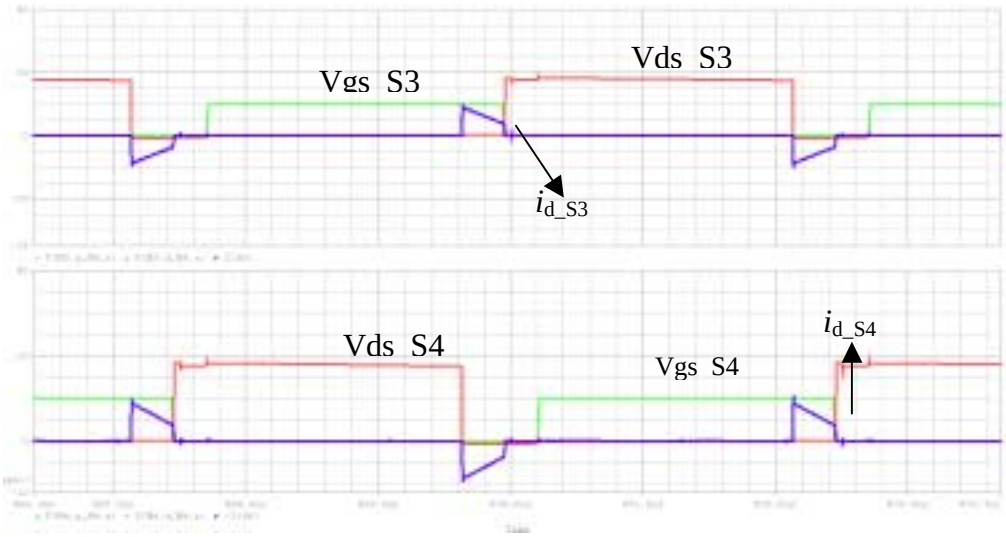


Fig. 5.19 (c) Switching waveforms of the switch S_3 and S_4

Fig. 5.19 Waveforms under the condition of $T_{off} < T_R$

In the experimental prototype, three MOSFETs (Si4420DY) are paralleled in each of the two channels of synchronous rectifiers in the current-doubler secondary side. IRFS59N10D MOSFETs are used for the main primary-side switches S_1 and S_2, 30CTQ060S Schottky diodes are selected for D_3 and D_4, and Si4470EY MOSFETs are used for S_3 and S_4. The MOSFET drive IC HIP2100 is used to drive the switch S_1 and S_2. LTC4440 high-side driver can be used for driving the switch S_3 and S_4. However, as an alternative driving scheme in the prototype, a simple self-driven circuitry based on the transformer windings is used to drive switches S_3 and S_4 without adding additional IC driver.

Experimental waveforms at two different duty cycles are shown in Fig. 5.20 and Fig. 5.21 compared with conventional RC snubber. It can be observed that the ringing is attenuated with the help of the proposed active-clamp snubber circuit and the body diodes of the main switches was not involved in the operation. Compared with the conventional

RC snubber, the body-diodes reverse recovery and RC snubber losses are eliminated. As discussed before, depending on the capacitance value of Cs, the freewheeling time is adjustable. At Cs=6.6uF, the experimental waveforms of transformer voltage and current are shown in Fig. 5.22. Efficiency comparison is shown in Fig. 5.23 with three cases of snubber circuits: RC snubber, active-clamp snubber with Cs=3uF, active-clamp snubber with Cs removed. It is shown that higher overall efficiencies are achieved with the proposed active-clamp converter.

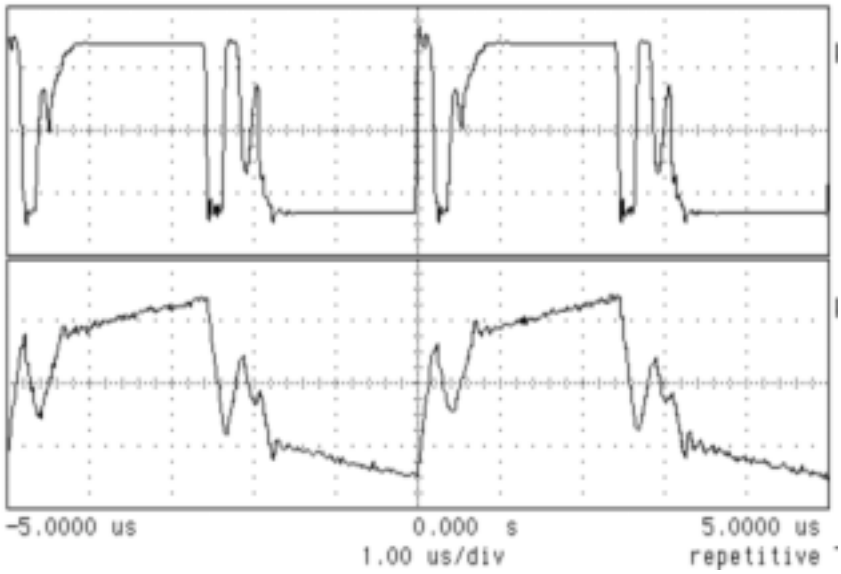


Fig. 5.20 (a) With the conventional RC series snubber

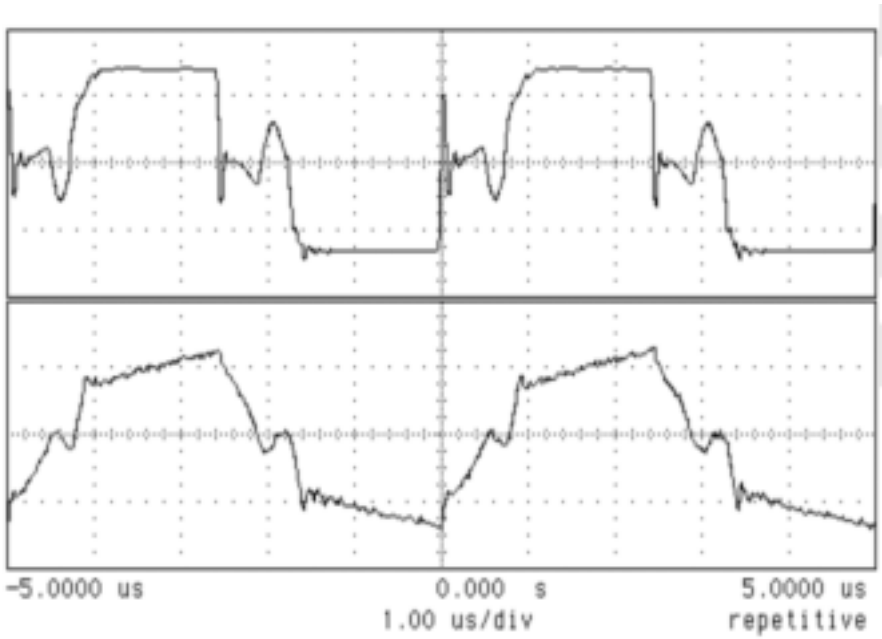


Fig. 5.20 (b) With the proposed active-clamp snubber

Fig. 5.20 Experimental waveforms of transformer primary-side voltage and current (D=0.37, Top trace Vab: 20V/div; Bottom trace i_p: 5A/div)

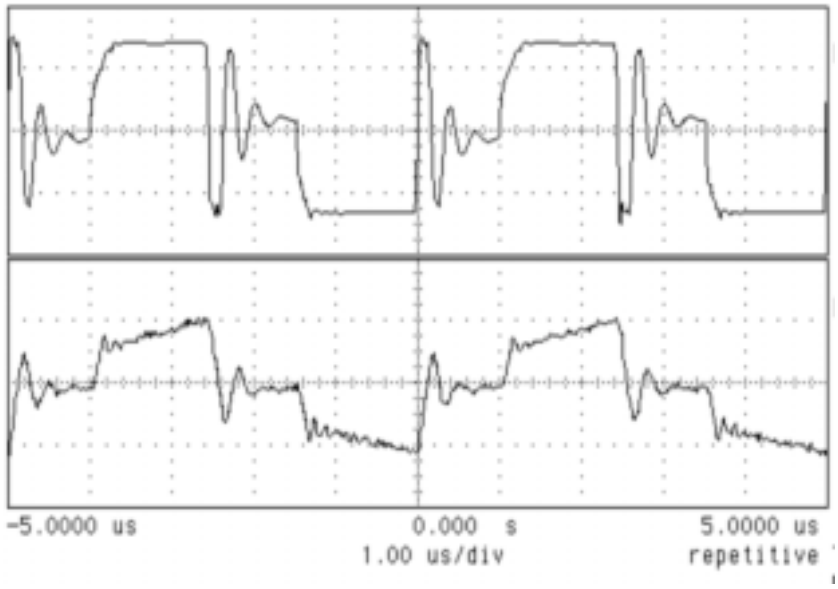


Fig. 5.21 (a) With the conventional R/C series snubber

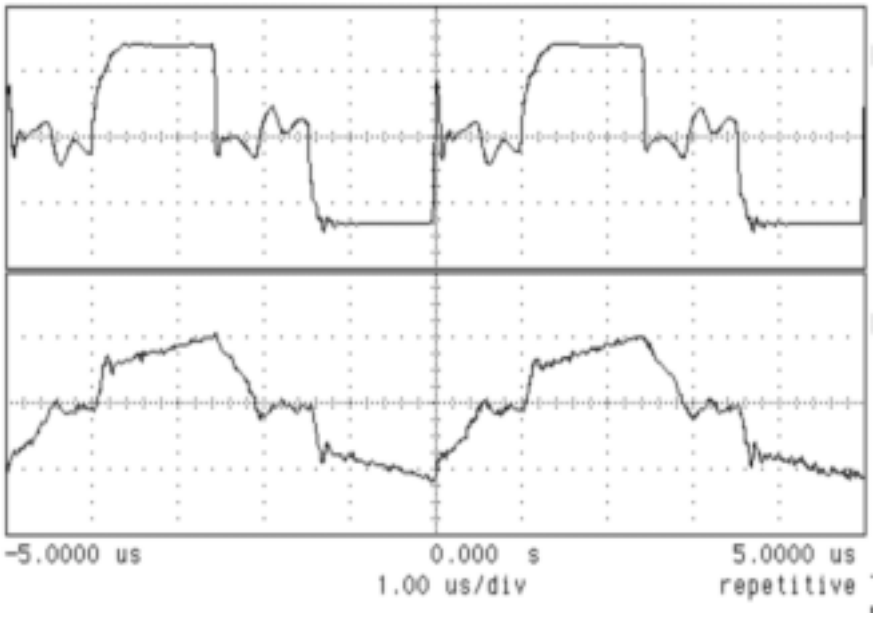


Fig. 5.21 (b) With the active-clamp snubber

Fig. 5.21 Experimental waveforms of transformer primary-side voltage and current

(D=0.28. Top trace Vab: 20V/div; Bottom trace i_p: 5A/div)

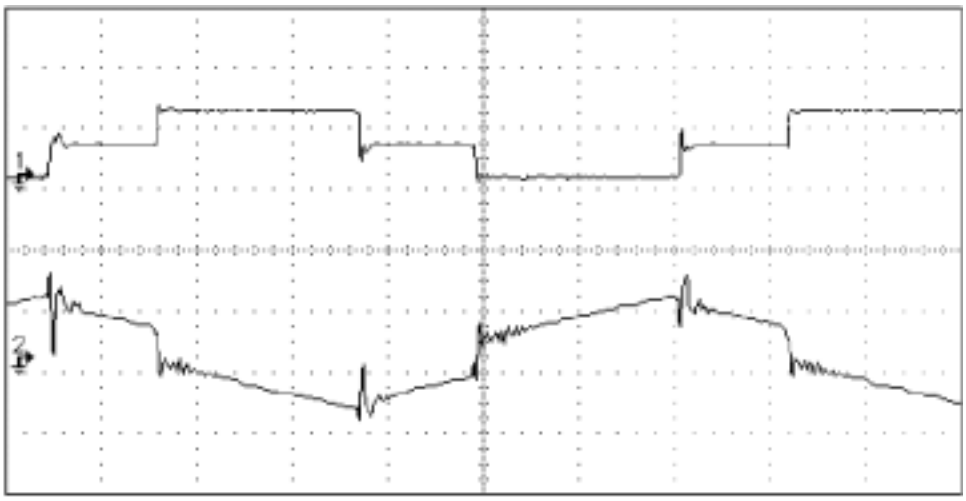


Fig. 5.22 Experimental waveforms of Vds across low-side switch and transformer primary current (Cs=6.6uF)

(Top trace Vab: 40V/div; Bottom trace i_p: 5A/div)

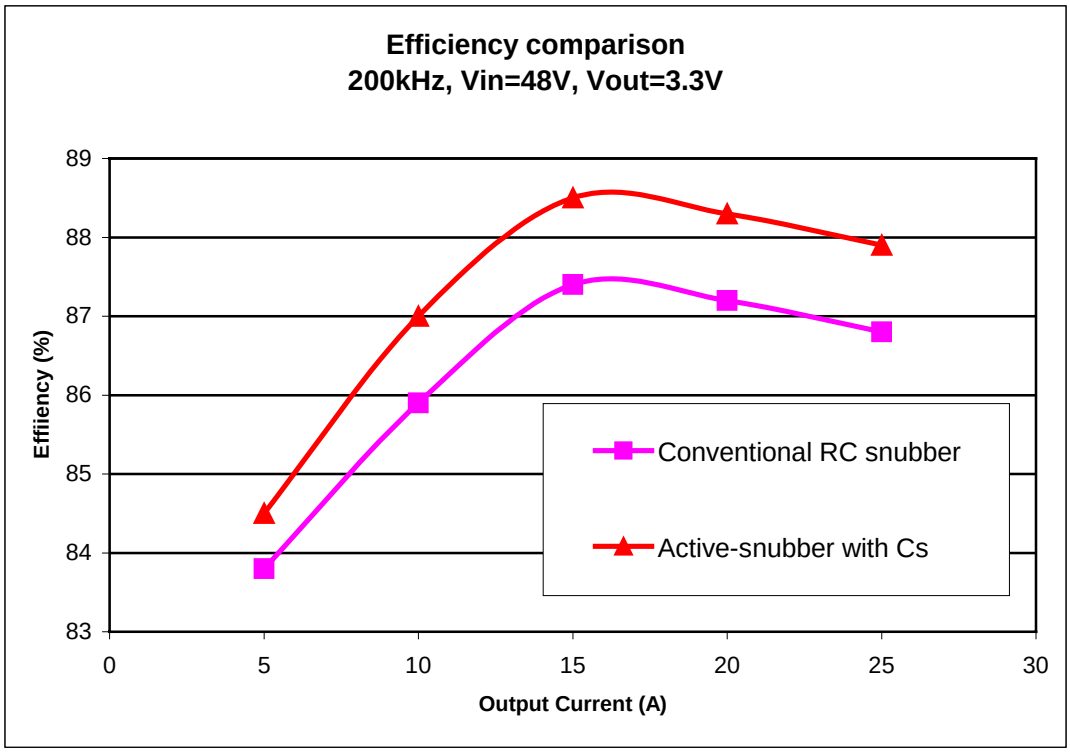


Fig. 5.23 Efficiency comparison between the proposed active-clamp snubber and the conventional RC snubber

5.4.4 Summary

A lossless active-clamp snubber circuit is proposed for the isolated half-bridge DC-DC converter and theoretically analyzed. Simulation and experimental results show that the transformer-leakage-inductance-related ringing is attenuated and the primary side body-diodes reverse recovery is eliminated using the proposed active-clamp snubber. Moreover, the efficiency is improved with the proposed active-clamp snubber compared to the conventional RC series snubber circuit. The half-bridge DC-DC converter with the

proposed active-clamp snubber topology is a strong candidate for applications requiring wide range of input voltage.

5.5 The energy storage and release concept applied on active-clamp forward topology

5.5.1 Introduction

Single-ended active-clamp converters, stemming from designs first documented by Bruce Carsten [E14][E15], have more recently gained widespread acceptance for many medium power off-line and DC-DC converter applications. Due to its simplicity and good performance, the key industry players such as Tyco/Lucent, IBM, NEC hold a big number of patents based on single-ended active-clamp topology. This topology adds an active-clamp network consisting of a small auxiliary switch in series with a capacitor plus the associated drive circuitry to traditional transformer-isolated forward and flyback converters resulting in significant performance enhancements. Theory and operation of these converters have been reported in many recent publications [E16-E24]. Typically, the clamp switch is kept on during the off-time of the main switch. As a result, the clamp capacitor absorbs and returns parasitic energy during every cycle with minimal losses. A large value of the clamp capacitance keeps the associated voltage ripple to a minimum.

The advantage of active-clamp forward topology can be summarized as below.

1) No additional reset winding or dissipative clamps are required for transformer reset.

2) Higher maximum duty cycle allows wider input voltage range or higher turns ratio.
3) The energy stored in parasitic elements is transferred to tank elements and recycled, resulting in higher efficiency and lower noise.
4) Switch voltage is clamped to a controlled level resulting in smaller (lower stress) switching devices.
5) Zero Voltage Switching (ZVS) of the switches is possible, leading to higher efficiency and possible high-frequency operation.
6) The voltage stress across the switches is relatively constant over the full range of input voltage. This feature offers certain design trade-offs which are not available in other single-ended implementations due to the switch voltage stress being proportional to the input voltage.
7) The transformer waveforms allow easy implementation of the synchronous switching technique on the secondary side.

The transformer reset technique is well demonstrated in the active-clamp forward topology. When the main power MOSFET S2 is turned off, the magnetizing current flows through the clamping switch S1. This brings power dissipation on the clamping switch S1 since the current keeps flowing through S1 from positive to negative during the whole period when S2 is off. For high line input when the duty ratio is small, the power loss is especially serious since the main power switch S1 is on at most of the switching period. The high line input voltage also cause the magnetizing current peak-to-peak value the highest, which leads to even more power loss.

5.5.2 Operation modes analysis for the proposed active-clamp forward converter

The proposed active-clamp forward converter is shown in Fig.5.24. The reset circuit is similar with the conventional one, which consists of a clamping capacitor C1 and clamping switch S1. Different with the conventional active-clamp scheme, S1 does not keep on during the whole off-time of S2. Actually when the main power stage switch is off, S1 keeps off and the magnetizing current flows through the body diode of S1. S1 stays off all the way till right before S2 is turned on. Since the magnetizing energy is stored on the clamping capacitor instead of freewheeling during the whole S2 off-time, the conduction loss is reduced.

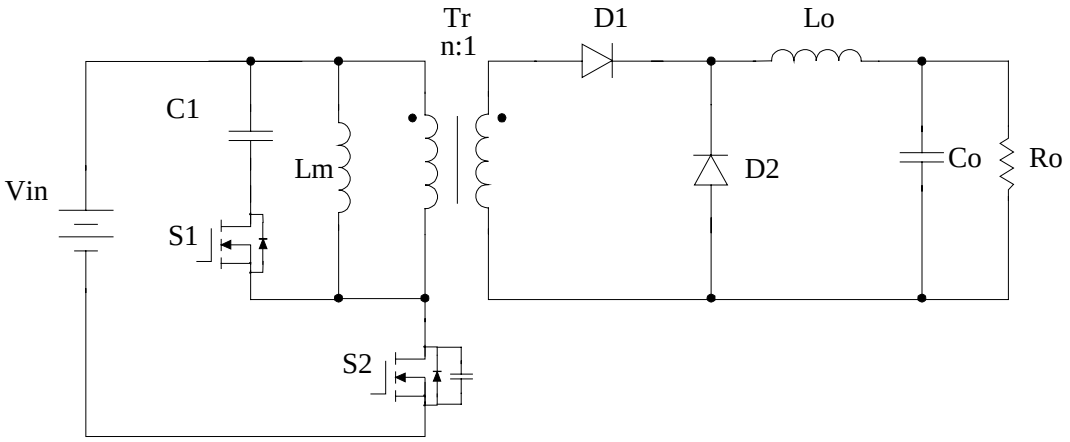


Fig. 5.24 The active-clamp forward topology

Similarly, to simplify the analysis, assumptions are made before the detailed operation modes analysis is carried out.

1) All diodes (including body diodes in MOSFETs) have zero forward voltage drop.
2) Secondary side filter inductor is big enough, the current flows through it is constant and equal to output current Io.

3) Clamping capacitor is big enough, the voltage ripple on it is ignorable.

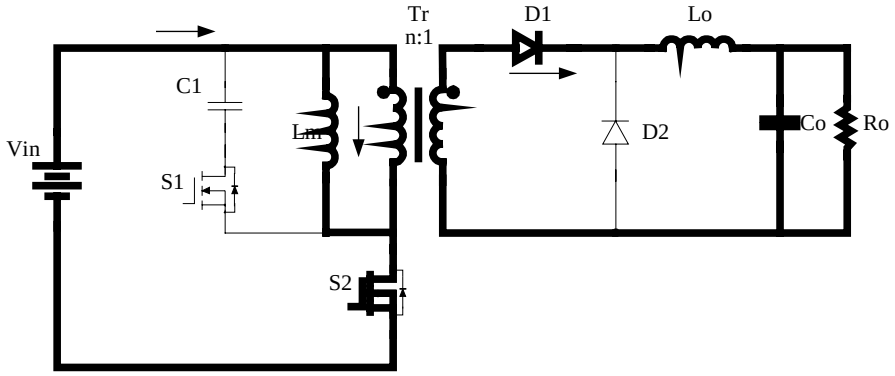


Fig. 5.25 (a) Mode 1

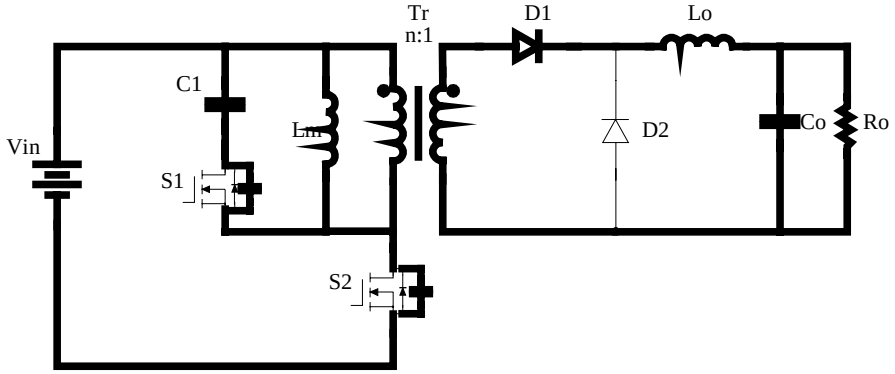


Fig. 5.25 (b) Mode 2

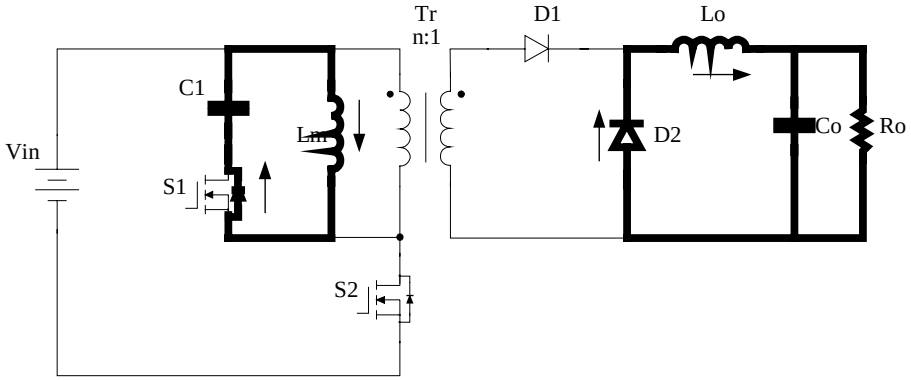


Fig. 5.25 (c) Mode 3

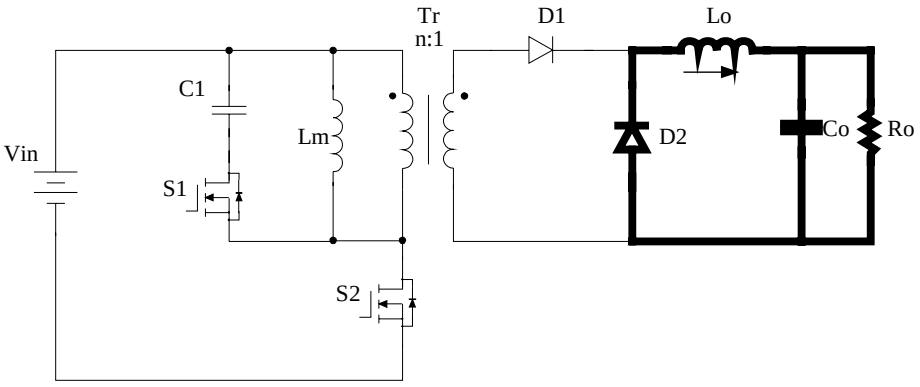


Fig. 5.25 (d) Mode 4

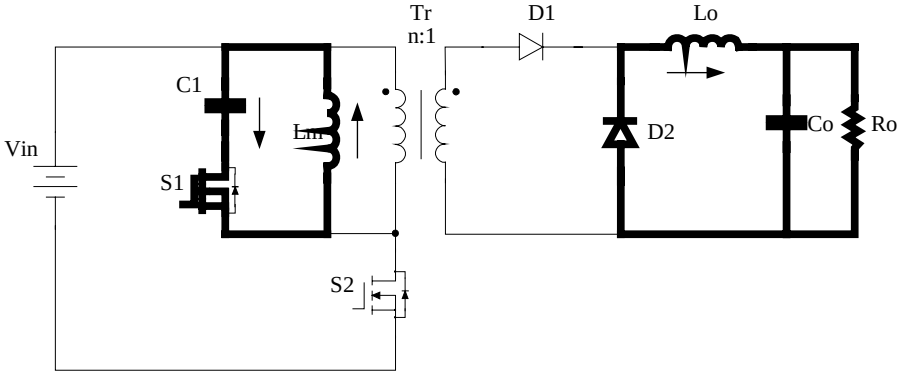


Fig. 5.25 (e) Mode 5

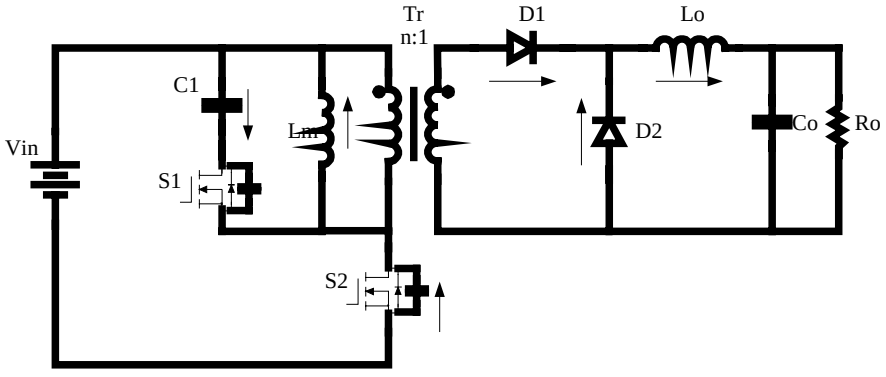


Fig. 5.25 (f) Mode 6

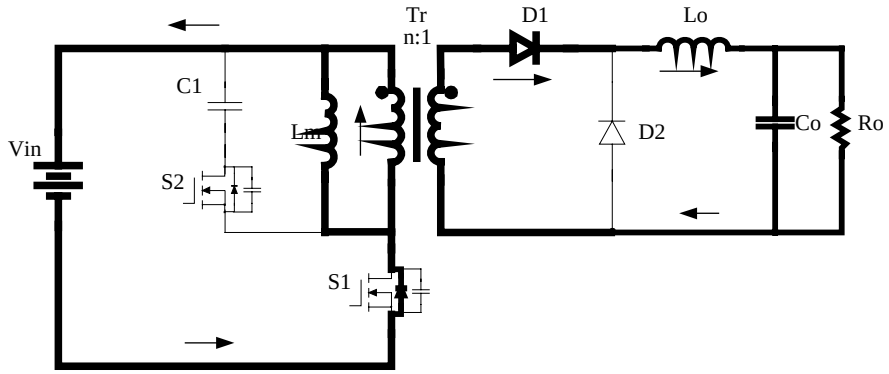


Fig. 5.25 (g) Mode 7

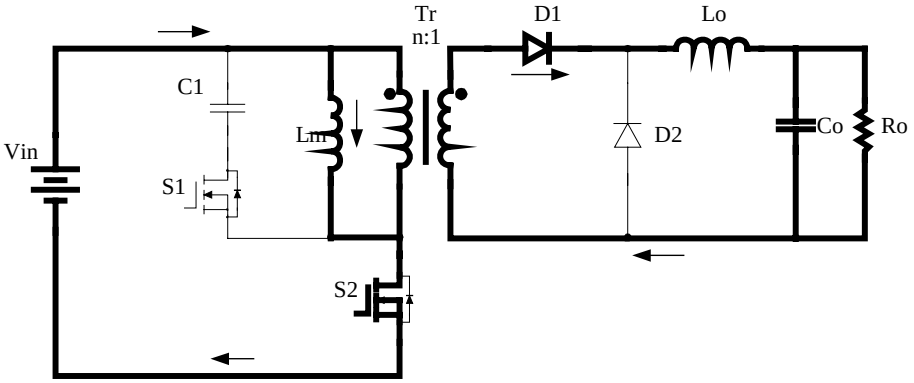


Fig. 5.25 (h) Mode 8

Fig. 5.25 Operation modes of the proposed active-clamp DC-DC converter

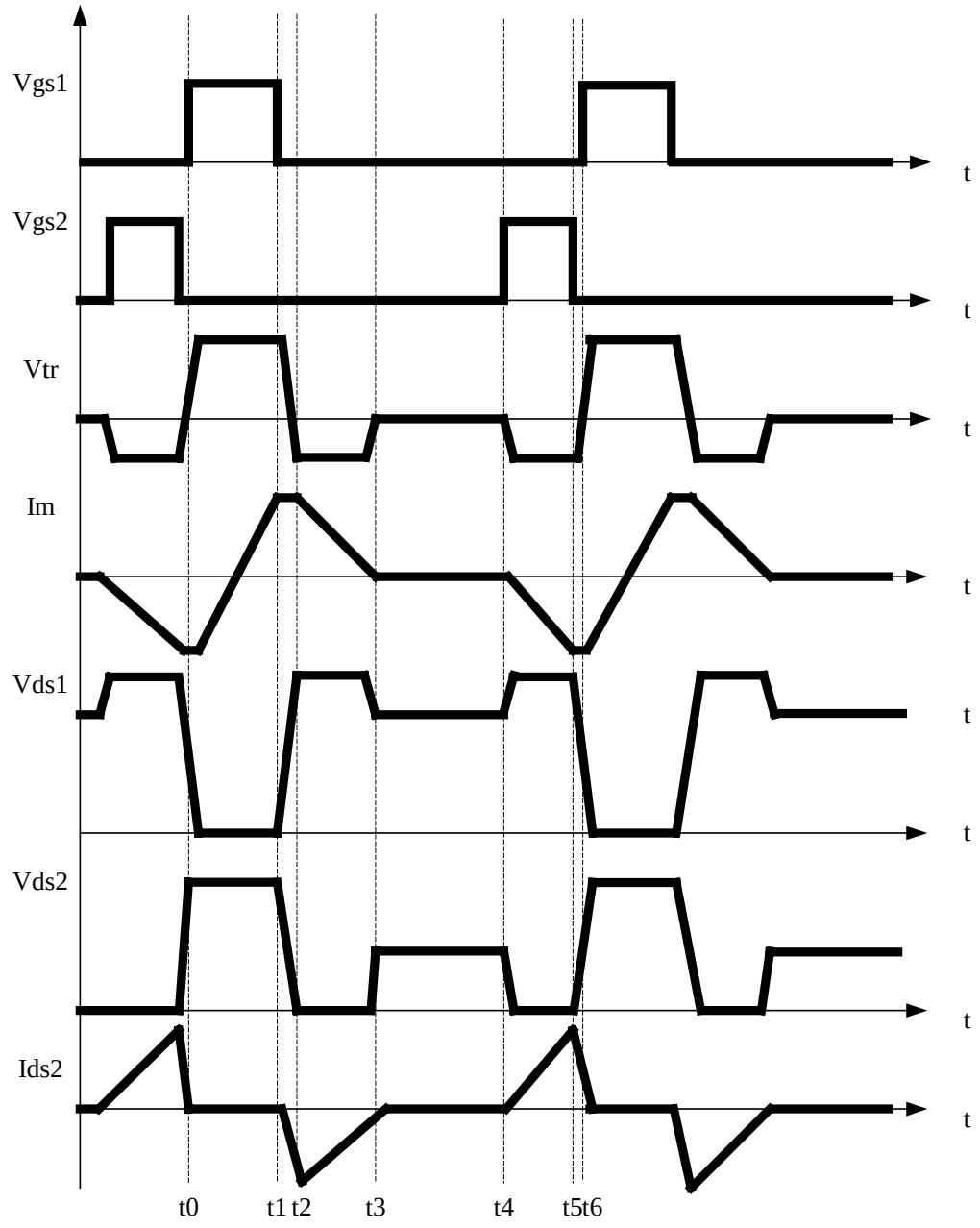


Fig. 5.26 Key waveforms

Mode 1*: (t0≤t<t1)* In this mode, MOSFET S1 is on, Diode D1 conducts and power is delivered from the primary side to the secondary side. The magnetizing current increases with the slope rate as:

$$\frac{d\,\mathrm{Im}}{dt} = \frac{Vin}{Lm} \tag{5.30}$$

Where Vin is the input voltage and Lm is the magnetizing inductance of the transformer. The pk-pk value of the magnetizing current is:

$$\mathrm{Im}\,pp = \frac{Vin \cdot D \cdot Ts}{Lm} \tag{5.31}$$

where D is the duty cycle defined as switch on-time over switching period. Ts is the switching period.

At t1, magnetizing current is equal to:

$$\mathrm{Im}(t1) = \frac{Vin \cdot D \cdot Ts}{2Lm} \tag{5.32}$$

The voltage across MOSFET S2 can be shown as:

$$VdsS2 = Vin + Vc1 \tag{5.33}$$

Where Vc1 is the voltage across clamping capacitor Vc1.

Mode 2: *(t1≤t<t2)* At t1, S1 is turned off, primary side current charges the junction capacitor of S1 causing VdsS1 to increase. At the same time, current flows through the junction capacitor of MOSFET S2 causing VdsS2 to decrease. When VdsS1 reaches Vin+Vc1, VdsS2 drops to zero, the body diode of MOSFET S2 conducts and carries the magnetizing current preparing the ZVS condition for MOSFET S2 to be turned on. The current flows out of transformer primary winding consists of two parts, the magnetizing current Im and the reflected secondary side current Iref. At t2, Iref is equal to:

$$Iref = \frac{n1}{n2} \cdot Io \tag{5.34}$$

In which, n1 is the number of turns for transformer primary winding, n2 is the number of turns for transformer secondary winding. Io is converter output current.

Mode 3: *(t2≤t<t3)* In this mode, diode D1 on the secondary side is off, D2 conducts caring all load current. Transformer secondary side winding is open. Transformer primary side winding current consists of only magnetizing current. Since VdsS2 drops to zero due to body diode conduction, ZVS is obtained. The transformer is directly connected to clamping capacitor with reversed voltage polarity, which puts secondary side diode D1 in reverse bias. The magnetizing current keeps decreasing and finally drops to zero. The time needed to reset the magnetizing can be expressed as follows:

$$T_{res} = \frac{V_{in} \cdot D}{2V_{c1} \cdot fs} \tag{5.35}$$

Where Vc1 is voltage across clamping capacitor C1, fs is switching frequency, D is duty cycle for S1.

Mode 4*: (t3≤t<t4)* In this mode, magnetizing current drops to zero, S1 body diode is off. Since no current flowing through the clamping switch, no power loss suffered during this interval. The energy stored in magnetizing inductor is transferred to clamping capacitor and kept for this interval. Converter primary is hibernating till t4.

Mode 5*: (t4≤t<t5)* At t4, S2 is turned on, clamping capacitor C1 begins to charging the magnetizing inductor causing magnetizing current to increase from zero. It should be noted that MOSFET S2 is turned on under hard switching condition. There is power loss during turn on transient, which is decided by:

$$Ps2 = \frac{1}{2} \cdot Coss\_c2 \cdot Vc1^2 \tag{5.36}$$

The loss is decided by output capacitance of S2 and clamping voltage across C2. Therefore, low output capacitance MOSFET is preferred to reduce the turn-on loss of MOSFET S2.

When S2 is on, transformer primary winding is applied by the clamping capacitor with the equal voltage applied on it. From t4 to t5, the magnetizing current is charged to *1/2Impp*. The time required to accomplish the charging is:

$$T_{chg} = \frac{V_{in} \cdot D_{chg}}{2V_{c1} \cdot f_s} \tag{5.37}$$

Where Dchg is the duty cycle of S2, which is defined as the conduction time over switching period. Since in Mode 3 and Mode 5 the same voltage applied on magnetizing inductor and the changes in magnetizing current are both *1/2Impp*, we may arrive at the conclusion that:

$$T_{chg} = T_{res} \tag{5.38}$$

Solving the equation, we arrive at:

$$V_{c1} = \frac{V_{in} \cdot D}{2 \cdot D_{chg}} \tag{5.39}$$

This is the voltage across the clamping capacitor in steady state.

The expression shows that the voltage across the clamping capacitor is decided by duty cycle ratio between S1 and S2. If small duty ratio Dchg for S2 is used, the clamping capacitor withstands high voltage which increases the voltage stress applied on S1 and S2. However, the small Dchg means the magnetizing inductor is charged and discharged in very short time. Mode d lasts long which reduced the losses existing in conventional active-clamp topology.

***Mode 6**: (t5≤t<t6)*

At t5, S2 is turned off, the current on magnetizing inductor discharge the junction capacitor of S1, causing VdsS1 to decrease. When VdsS1 drops to zero, the body diode conduct, providing ZVS condition for S1 to be turned on.

5.5.3 Simulation verifications

Below parameters are used in simulation:

Vin=48V, Vout=1.8V, Iout=30A, transformer turns ratio is 5:1, leakage inductance is 300nH, magnetizing inductance is 30uH, C1=1uF, fs=100kHz.

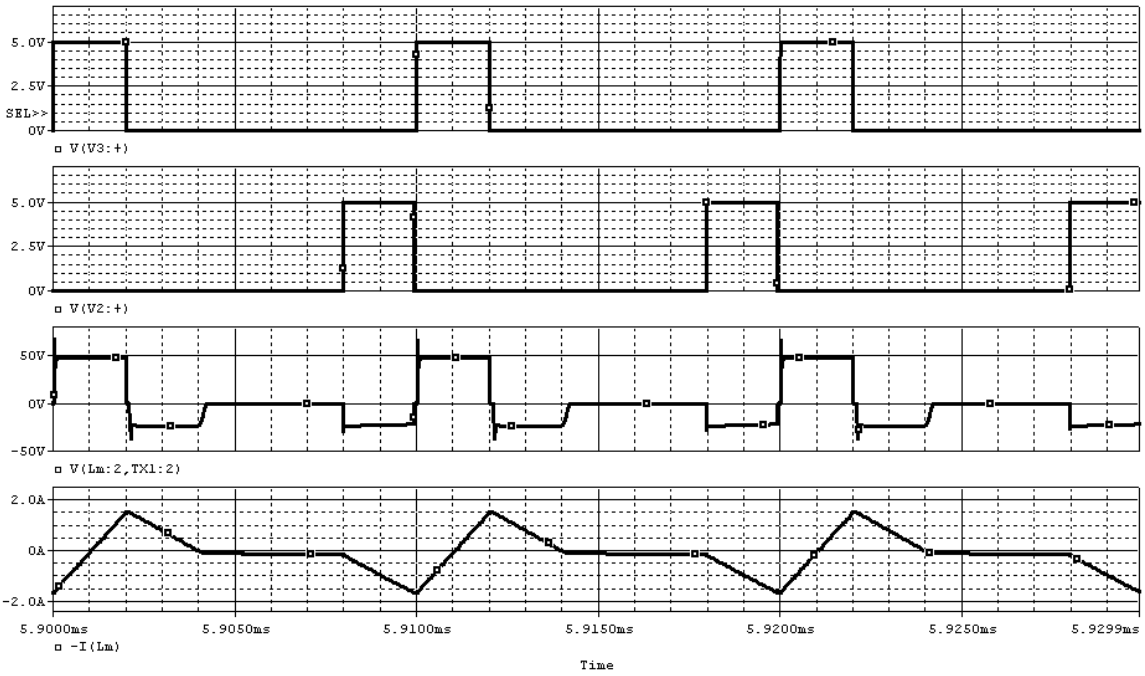


Fig. 5.27 The simulation waveform

(Trace 1: The driving signal for the main power MOSFET S2. Trace 2: The driving signal for the clamping MOSFET S1. Trace 3: The transformer primary winding voltage waveform. Trace 4: The transformer primary winding current waveform.)

The first and second traces are the driving signal applied on the gate of MOSFET S1 and S2 respectively. The third one is the transformer primary winding voltage. The forth trace is the magnetizing current. When S1 is on, Imag increases and goes down to zero when S1 is off. Before S2 conducts, ideally there is no current flowing through clamping

switch and the magnetizing current remains zero. The tiny current in simulation is caused by secondary side diode forward voltage drop. When S2 is on, the clamping capacitor voltage charges the magnetizing inductor causing the magnetizing current goes negative. The spike in the transformer primary winding voltage waveform comes from the reverse recovery of the secondary side diode.

Fig. 5.28 Simulation waveforms

(Trace 1: The voltage across the power switch S2. Trace 2: The voltage across the clamping switch S1. Trace 3: The voltage across the clamping capacitor. Trace 4, 5: The current flowing through transformer primary winding (solid line) and the magnetizing current (dashed line))

The first and second traces are Vds of S1 and Vds of S2 respectively. The third trace is the voltage across the clamping capacitor. The last two are leakage inductor

current (solid trace) and magnetizing current (dashed trace). The simulation waveform agree with the analysis carried out before, which verified the proposed scheme.

5.6 The lossless zener diode concept applied on self-driven circuit

5.6.1. Background introduction

As switching frequencies increase, the need for a low loss or energy saving gate driver circuit is necessary. For high power density designs the gate driver size should also be small. There are many different types of gate drive circuits that fall under two categories, external driven or self-driven. An external gate driver receives its signal from a control circuit, where as, a self-driven circuit receives its signal and power internally from the circuit. Compared with external gate driving circuit, the self-driven has the following features:

- Simplicity. Self-driven scheme generates the driving signal by itself taking advantage of the power stage information such as the transformer winding voltage. Since the primary needs not passing the driving signal to the secondary, the isolation circuitry is saved.
- Reduced power losses. For conventional external driving, the junction capacitance of the MOSFET is charged and discharged during the switching process. The energy stored on the junction capacitance is dissipated in the driving circuitry in each switching period. The power dissipation is proportional to the switching frequency and causes thermal issues for converters with high switching frequency.

For the self-driven circuitry, since the power stage itself provides the driving current for the MOSFETs, the discharging current of the MOSFET when it is turned off flows back to the power stage. The energy stored on the junction capacitance is partly recycled to the power stage instead of fully dissipated in the driving circuitry. Less power dissipation leads to higher efficiency and higher reliability.

- Adaptive driving. One other benefit of self-driven circuits is that the gate drive signal is nearly instantaneous, thus reducing, or even eliminating, the body diode conduction time.

As discussed above, self-driven is suitable for isolated DC-DC converters and has widely applications in on-board DC-DC converters. There exists however, some important issues in self-driven schemes. One of them is the changing driving voltage issue. Fig. 5.29 illustrates a half-bridge DC-DC converter with cross-coupling self-driven circuit, which is used as the first stage in a two-stage on-board converter. Since the regulation is accomplished in the second stage (employing topology like buck), the two MOSFET driving signals both have full duty ratio, which allows self-driven circuitry to be used at the second side.

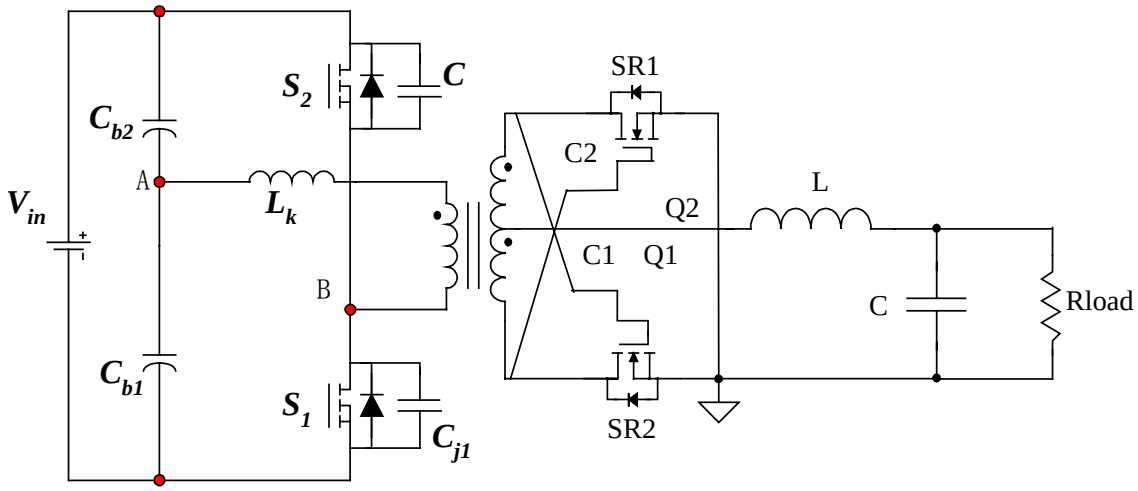


Fig. 5.29 Half-bridge isolated DC-DC converter with self-driven circuitry.

The driving voltage for MOSFET SR1 and SR2 comes from the transformer winding and the voltage level is decided by the voltage applied on the transformer primary winding. Therefore, the input voltage has significant effect on the self-driven voltage for SR1 and SR2. For one design with Vin=36~75V, transformer primary turns number np=5 and secondary turns number ns=1, the driving voltage applied on the MOSFET gate has the range of:

$$Vdrv = \frac{Vin}{2} \cdot \frac{ns}{np} \cdot 2 = 7.2 \sim 15V \tag{5.40}$$

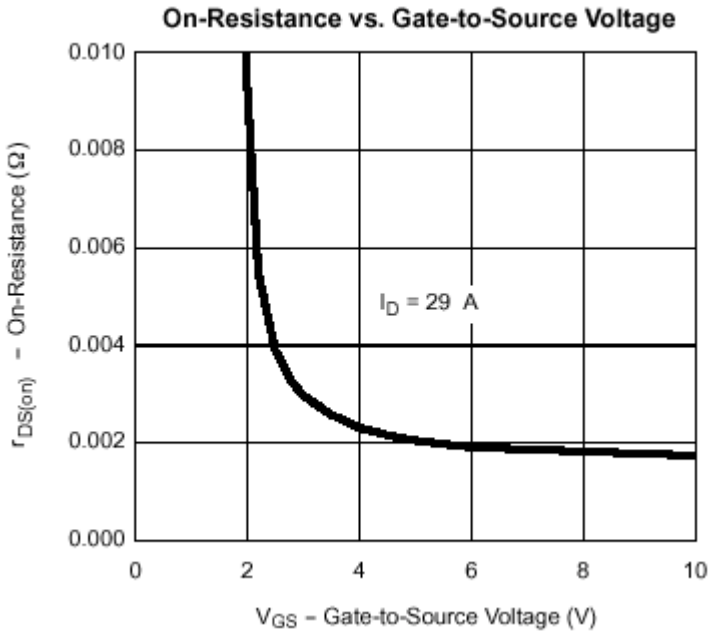


Fig. 5.30 The on-resistance vs. driving voltage for MOSFET Si7868

(Vgsmax=20V, Idmax=18A)

Fig. 5.30 shows the non-linear property of the on-resistance vs. driving voltage for Vishay MOSFET Si7868. It is clear that the driving voltage has a big effect on the on-resistance of the MOSFET. In other words, the driving voltage affects the power dissipation of the MOSFET, especially in high-current applications where the conduction loss amount to be a very big portion of the total power losses the effect is even more significant. Such a big variation of the driving voltage in the self-driven circuit brings big challenges for efficiency optimization of the DC-DC converter.

5.6.2 The proposed lossless zener diode clamping circuit

To stabilize the driving voltage for the MOSFET, the clamping circuit is proposed as shown in Fig. 5.31.

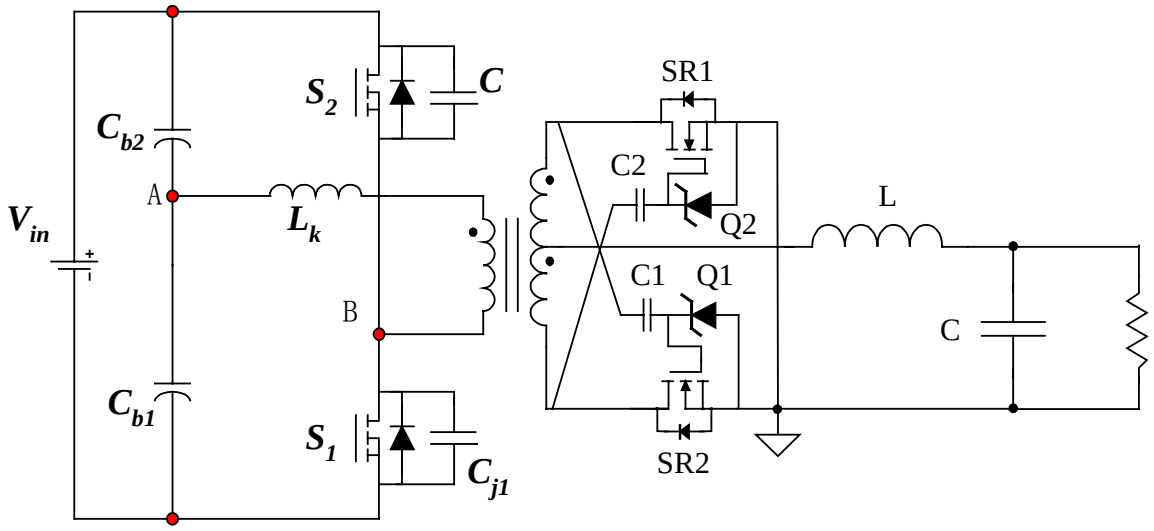


Fig. 5.31 The proposed clamping lossless zener clamping circuit for self-driven scheme

The proposed circuit has the following features:

1) Lossless. Different with the conventional zener diode circuit, one capacitor instead of a resistor is placed in series with the zener diode. Since capacitor is reactive component and does not dissipate power, the proposed circuit has much less power dissipation than the conventional zener diode with a resistor.
2) Strong driving capability. The capacitor serves as a differentiator and has low impedance for the driving current to pass through.
3) Stabilization. The zener diode clamps the driving voltage to its reverse breakdown voltage, which is independent of the transformer winding voltage. It consumes power when there is current flowing through the clamping

capacitor C1 and C2. Since the charging process is very short (10ns~40ns) and the current flowing through C1 and C2 after the charging process is finished.

A. Operation principle analysis and power loss considerations.

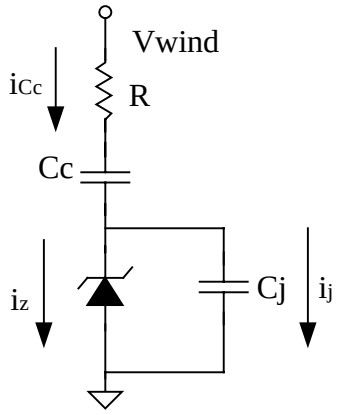


Fig. 5.32 The proposed clamping circuit

Cc is the clamping capacitor placed in series with the clamping zener diode. Cj is the input parasitic capacitance of the MOSFET. One small resistor R is used to damping the oscillation between the capacitance (the clamping capacitor and the junction capacitance of the MOSFET) and the parasitic inductance (the trace inductance and the leakage inductance of the transformer).

Assume the input voltage, which comes from the transformer windings, has the range of Vwind≤Vwind≤Vwindmax. The clamping capacitor is designed at the minimum input voltage, Vwind=Vwindmin. To simplify the analysis, we assume that the driving current ij is constant during the charging process 0≤t≤tc. The current required to charg the MOSFET gate to turn the MOSFET on is calculated as:

$$i_j = \frac{Q_g}{t_c} \tag{5.41}$$

In which, Qg is the total gate charge and tc is the time needed to charge the MOSFET to required driving voltage.

Assume the current flows through the clamping capacitor is also constant, in tc time, the capacitor voltage is charged from zero to Vwind-Vdrv, Vdrv is the reverse voltage of the zener. The current flowing through the clamping capacitor is calculated as:

$$i_{Cc\_\min} = Cc \cdot \frac{V_{wind\min} - V_{drv}}{t_c} \tag{5.42}$$

The critical clamping capacitor value is designed so that the current flowing through the zener diode is zero for Vwind. There are two reasons to design the clamping capacitor at Vwindmin.

1) Voltage clamping consideration. If the capacitor is less than the critical value, there is less current flowing through Cc than flowing through Cj. As a result, the zener diode has to provide negative current, with which the zener diode cannot maintain its voltage Vdrv and leads to insufficient driving voltage at the MOSFET gate.
2) Power loss consideration. The damping resistor R consumes the energy stored in the MOSFET junction capacitor Cj and the clamping capacitor Cc. Large clamping capacitor value leads to big loss on the resistor.

Then we have:

$$i_{Cc\_\min} = i_j \tag{5.43}$$

Solving the equation, the clamping capacitor value is obtained.

$$Cc = \frac{Q_g}{V_{wind\,\min} - V_{drv}} \tag{5.44}$$

Since there is no current flowing through the zener diode (the current is several mA which can be ignored), the power dissipation on the resistor is equal to the energy transferred to the junction capacitance of the MOSFET (the current flowing through the resistor is equal to the current charging the junction capacitor of the MOSFET, which is the same case as self-driving except that the driving voltage is Vdrv instead of Vwind).

The power loss on the damping resistor during the turn on and turn off process of the MOSFET is calculated using the energy reservation rule:

$$P_r = Cc \cdot (V_{wind\,\min} - V_{drv})^2 + Q_g \cdot f_s \cdot V_{drv} \tag{5.45}$$

When the transformer winding voltage is higher than Vwindmin, assume the zener diode clamps the driving voltage to Vdrv. The current charging the MOSFET gate keeps unchanged due to the fixed driving voltage.

The clamping capacitor voltage changes from zero to Vwind-Vdrv in the interval of 0≤t≤tc. The current flows through it is:

$$i_{Cc} = Cc \cdot \frac{V_{wind} - V_{drv}}{t_c} = \frac{Q_g \cdot (V_{wind} - V_{drv})}{(V_{wind\,\min} - V_{drv}) \cdot t_c} \tag{5.46}$$

The current flowing through the zener diode is calculated as:

$$i_z = i_{Cc} - i_j = \frac{Q_g \cdot (V_{wind} - V_{wind\,\min})}{(V_{wind\,\min} - V_{drv}) \cdot t_c} \tag{5.47}$$

The power dissipation on the zener diode during MOSFET turn-on is:

$$P_{z1} = V_{drv} \cdot i_z \cdot t_c \cdot f_s = \frac{V_{drv} \cdot Q_g \cdot (V_{wind} - V_{wind\,\min}) \cdot f_s}{V_{wind\,\min} - V_{drv}} \tag{5.48}$$

During the MOSFET turn-off transition, the circuit changed to Fig. 5.33.

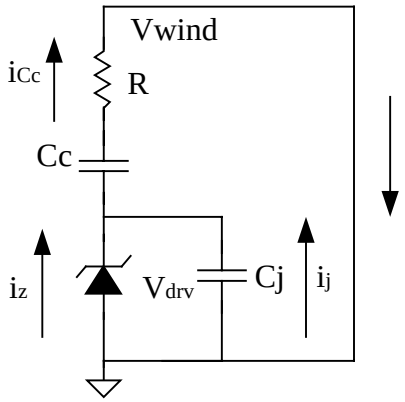


Fig. 5.33 The MOSFET turn-off transition analysis

At first, Cj and Cc is both discharged by current iCc, the voltage across Cj, i.e., Vdrv begins to decrease till it goes to zero. At this interval, no current flows through the zener diode. Then zener diode conducts as a diode with the forward drop Vf across it and begin to carry the current. To simplify the analysis, we assume that during this interval, the current flowing through the zener diode is the difference between iCc and ij in the average point of view and the voltage across it is Vf, the power dissipation during the MOSFET turn-off transition is:

$$P_{z2} = \frac{(V_{wind} - V_{wind\,\min}) \cdot Q_g \cdot V_f \cdot f_s}{V_{wind\,\min} - V_{drv}} \tag{5.49}$$

The total power dissipation on the zener diode for one MOSFET switching period (one turn-on and one turn-off) is:

$$P_z = P_{z1} + P_{z2} = \frac{(V_{wind} - V_{wind\,\min}) \cdot (V_{drv} + V_f) \cdot Q_g \cdot f_s}{V_{wind\,\min} - V_{drv}} \tag{5.50}$$

The power loss on the damping resistor is equal the energy stored in the clamping capacitor and the junction capacitor of the MOSFET, which is shown as:

$$P_r = Cc \cdot (V_{wind} - V_{drv})^2 + V_{drv} \cdot f_s \cdot Q_g = \frac{({V_{wind}}^2 - 2V_{wind} \cdot V_{drv} + V_{drv} \cdot V_{wind\,\min}) \cdot Q_g \cdot f_s}{V_{wind\,\min} - V_{drv}} \tag{5.51}$$

The total loss on the clamping circuit for transformer winding voltage Vin is shown as:

$$P_{total} = \Pr + Pz = \frac{[V_{wind}{}^2 + (V_f - V_{drv}) \cdot V_{wind} - V_{wind\,\min} \cdot V_f] \cdot Q_g \cdot f_s}{V_{wind\,\min} - V_{drv}} \qquad (5.52)$$

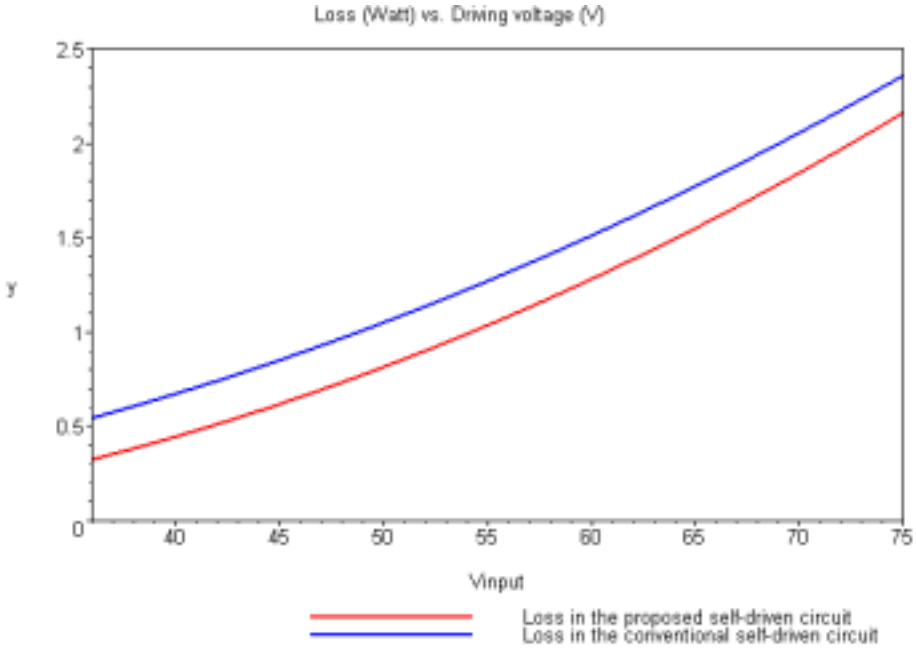


Fig. 5.34 The loss comparison between two self-driven circuits vs. the converter input voltage

One comparison between the proposed self-driven scheme and the conventional one is carried out with the following parameters:

Vwind=7.5~15V, Vdrv=3.6V, fs=300kHz, R=1Ohm, MOSFET used: Si7868 from Vishay (www.vishay.com) with 3 in parallel. Clamping capacitor Cc=41.6nF.

The calculation result shows that, the proposed self-driven circuit has less power loss than the conventional one. A simple explanation can be made by recalling the fact that the clamping capacitor Cc is put in series with the MOSFET junction capacitor so that the equivalent capacitance is reduced, which reduces the energy stored on them, i.e, the power loss is reduced.

The comment above does not take the zener diode loss into consideration. When larger capacitance value is selected (in the case for higher driving voltage Vdrv), the current difference between i_{Cc} and i_j goes up, which means more power dissipated in the zener diode. This case is shown in the following figure.

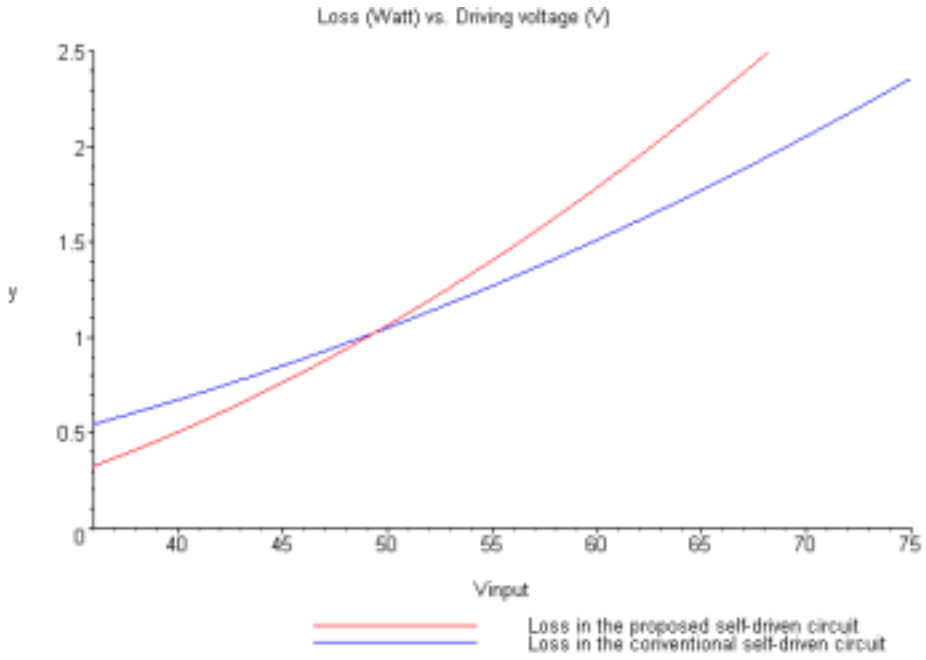


Fig. 5.35 The loss comparison between two self-driven circuits vs. the converter input voltage when higher Vdrv (Vdrv=6V) is aimed

There is an intersection point as shown in Fig.5.35, at which the two power losses are equal. At the left side, the proposed self-driven circuit has less power loss than the conventional one. At the right side, the large capacitor value causes big current flowing through the zener diode, causing big power loss on it. For this case, the proposed self-driven scheme should be carefully analyzed to decide the feasibility for applications.

B. Simulation verifications.

The proposed self-driven scheme with the clamping technique is applied to a half-bridge DC-DC converter with full duty cycle is simulated with the following parameters:

Vin=36V~75V, np=5, ns=1, primary MOSFET: Si7456, secondary side SR MOSFET: Si7868 (3 in parallel for each channel), clamped driving voltage Vdr=3.6V, clamping capacitor Cc=41.6nF, damping resistor R=1Ohm, fs=300kHz. The simulation results are shown in Fig. 5.37 .

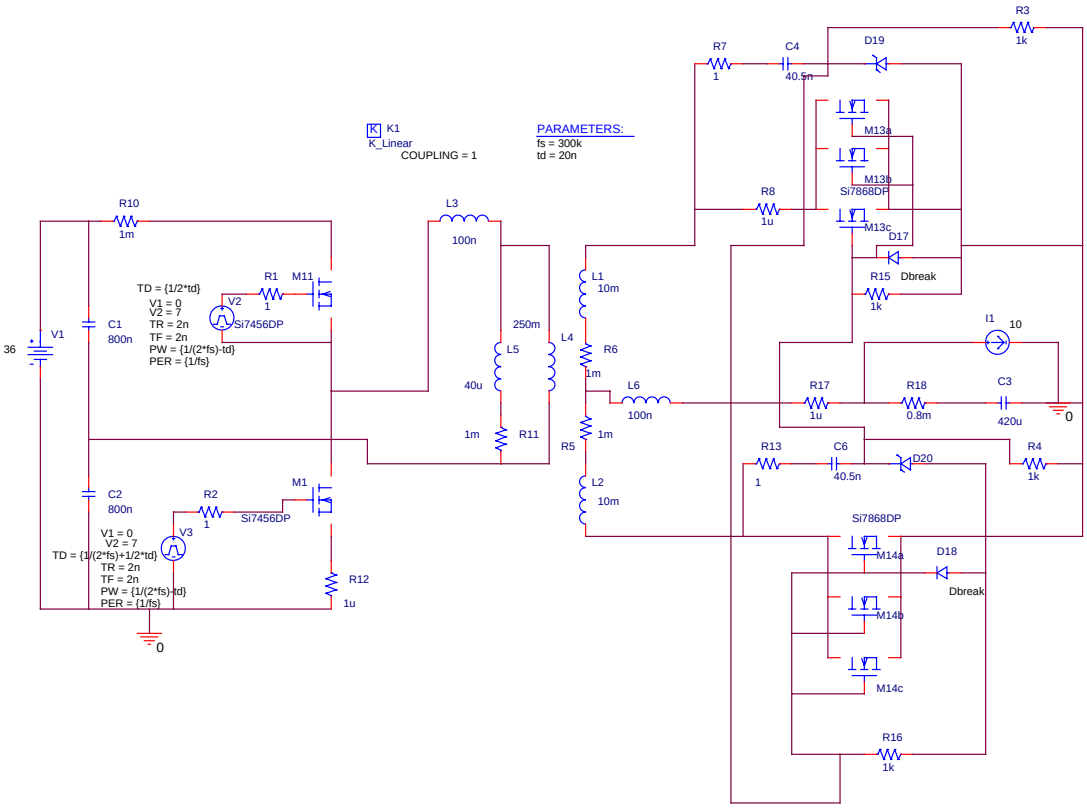


Fig. 5.36 The simulation schematics

Fig. 5.37 (a) 36V converter input voltage

Fig. 5.37 (b) 75V converter input voltage.

Fig. 5.37 Simulation result for the proposed self-driven circuit with clamping

(Top: transformer secondary winding voltage waveform; bottom: clamping circuit input votage, blue: MOSFET gate)

From the simulation results, it is clear that for the wide input voltage range Vin=36V~75V, the proposed self-driven circuit can effectively maintain the driving voltage to 3.5V. The driving voltage optimization is easy to be carried out and the MOSFTE gate is protected from over voltage breakdown.

To verify the calculation result, the simulation is carried out with the parameter shown as below:

Vin=36V~75V, np=5, ns=1, primary MOSFET: Si7456, secondary side SR MOSFET: Si7868 (3 in parallel for each channel), clamped driving voltage Vdr=3.6V, 3.6V/1.5W zener diode 1SMA5914BT3 from On Semeconductor (www.onsemi.com) is chosen as the clamping zener diode.

The difference between the simulation result and the calculation result may come from the assumption, in which the charging/discharing current through the capacitors is taken as constant during the transition.

Table 5.1 Power loss comparison between calculation and simulation.

	Vin=36V	Vin=42V	Vin=48V	Vin=54V	Vin=68V	Vin=75V
Power Loss from simulation (W)	0.53(0.29)*	0.70(0.43)	0.90(0.63)	1.13(0.87)	1.75(1.57)	2.12(2.00)
Power loss from calculation (W)	0.54(0.41)	0.74(0.51)	0.96(0.74)	1.22(1.00)	1.94(1.75)	2.36(2.2)

* The number in the bracket is the power loss from the proposed self-driven circuit.

C. Summary.

From the analysis above, few points may be summarized:

- The proposed self-driven clamping circuit can effectively stabilize the driving voltage, which makes the driving optimization easier. The driving voltage on the MOSFET gate is independent on the converter input voltage, this also help to protect the MOSFET gate form over voltage breakdown for high line input.
- The clamping capacitor is critical for the power loss in the proposed circuit. The value should be carefully designed taking consideration of the driving voltage, MOSFET type and the input line voltage range.
- The proposed circuit is verified by simulation result from a full duty ratio half-bridge with self-driven on the secondary side. The calculation results agree with the simulation results in the power loss point of view except for errors resulting from the analysis assumptions.

6. PHASE-SHIFT CONCEPT APPLIED ON HALF-BRIDGE DC-DC CONVERTERS

6.1 Introduction

Microprocessors and DSPs have experimented a very important development in recent years. As a consequence, nowadays these devices need power supplies with strict voltage and current requirements. One of the main challenges, for designer, is to get a higher current slew rate. In general, the main requirements to feed last generation microprocessors and DSPs are the following [F1-F4]:

- Low output voltage: 1 to 3.3 V.
- Output voltage tolerance: ± 2%.
- High load current: 1 to 60 A.
- High-current slew rate: up to 5 A/ns.
- Reduced converter size & improved converter efficiency.

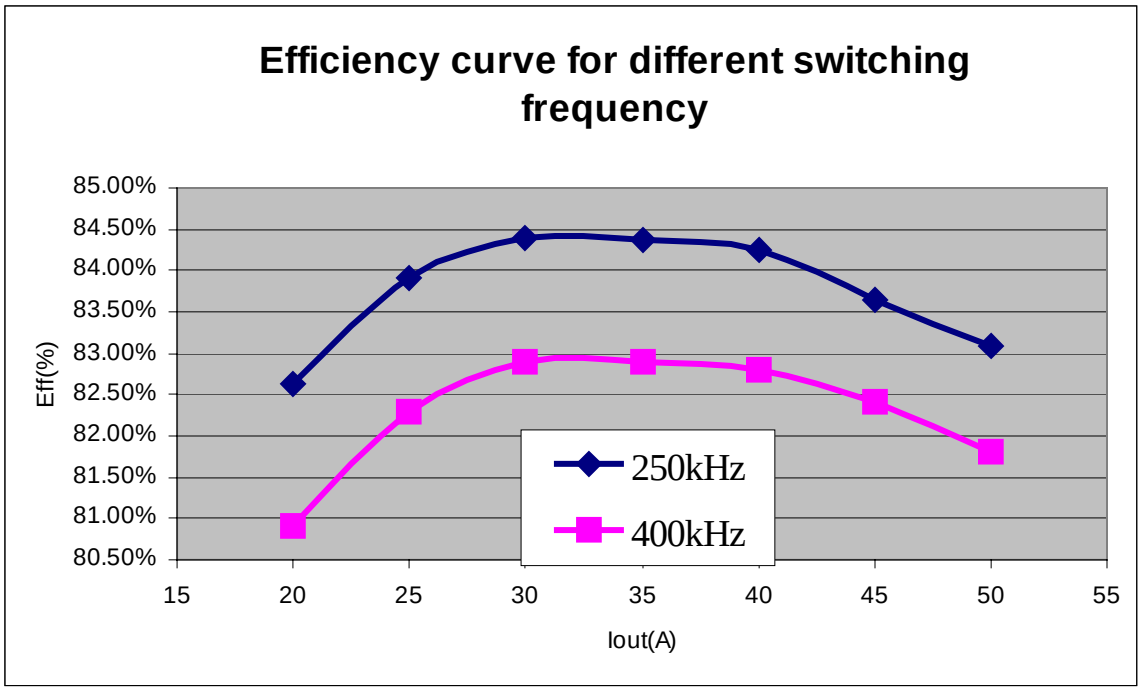


Fig. 6.1 The experimental efficiency curve for one DC-DC converter with different switching frequency

Since microprocessors and DSPs current consumption presents a big number of high load current steps with high slew rate, fast transient response with high bandwidth has long been required for the power supply system.

Increasing switching frequency is probably the most straightforward way to expand the bandwidth. The switching power supply, however, has limited switching frequency due to the switching losses. The switching losses are meaningful for frequencies greater than 500 kHz. Fig. 6.1 shows a DC-DC converter prototype efficiency curve built in lab with 36V~75V input 1V/50A output employing half-bridge topology with current doubler rectification. When frequency goes up, losses in the converter such as the driving

loss, switching loss and transformer AC conduction loss increase significantly. From 250kHz to 400kHz, the efficiency drops by two percent.

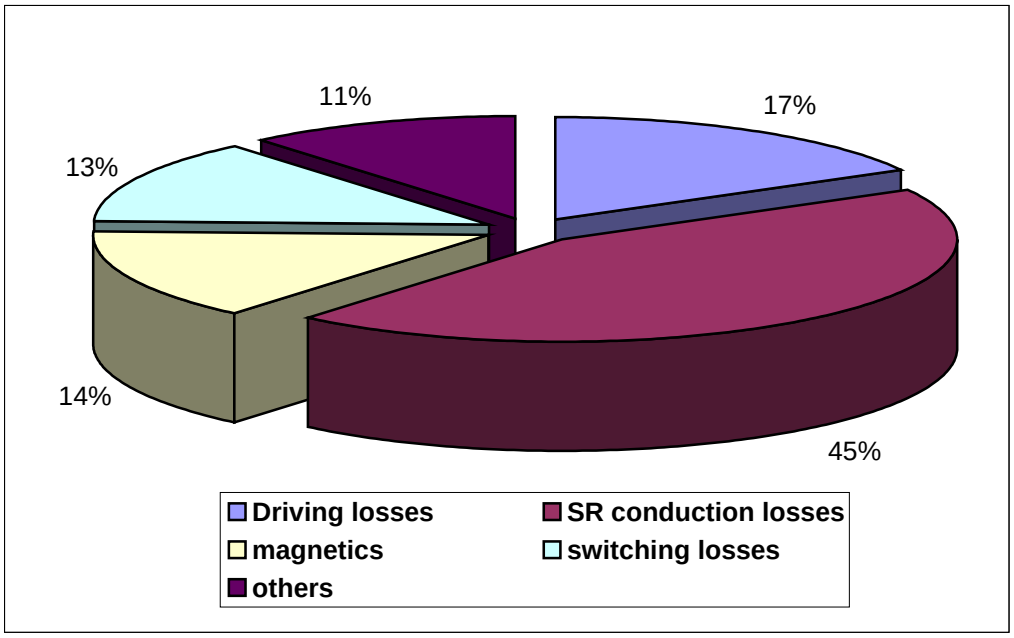
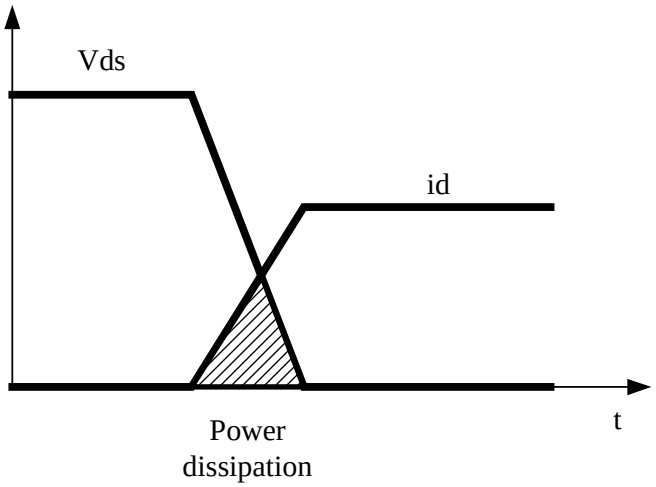
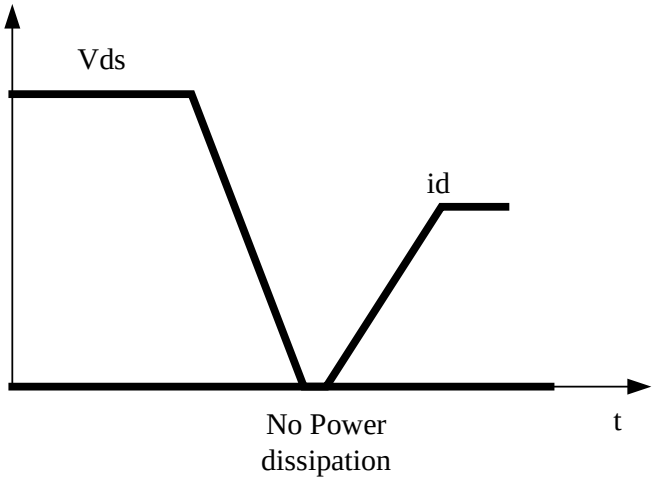


Fig. 6.2 Losses distribution in one DC-DC converter

From Fig. 6.2, we can see that, the driving loss and switching loss on the MOSFET, which increase with the switching frequency, amount to a big part of the total loss (30%). Choosing MOSFET with low total gate charge Qg and reduce the driving voltage can reduce the driving loss on the MOSFET. However, the penalty is that, the conduction loss increase due to the increase of the on-resistance, which does not provide a good solution for high-current applications. For the switching losses, ZVS techniques can help to bring down the switching loss as shown in Fig. 6.3.



(a) Hard switching.



(b) Soft switching.

Fig. 6.3 The ZVS illustration

Before turn on the switch, the drain to source voltage of the MOSFET is brought down to zero. When the MOSFET is turned on, there is no overlap between the drain to source voltage and the current flowing through the MOSFET, which means no power dissipated at the MOSFET turn on process. This technique is widely employed in DC-DC

converters. For bus converter applications, since the power MOSFET has full duty ratio, the two MOSFET can be turned on with ZVS, which significantly reduced the switching loss and the ringing between the leakage inductance and the junction capacitance is eliminated as well, which gives excellent EMI solution. However, for regulated DC-DC converter with variable duty ratio, that is a different story. Asymmetric half-bridge topology has complementary switching between the two power MOSFETs, which provide a way to regulate the output while still maintain ZVS for the two MOSFETs. However, the asymmetrical switching brings uneven stresses for the switches and DC bias in transformer magnetizing current, the gain of the converter is also not linear. All those defaults limit the applications of the asymmetric half-bridge. Another promising topology is the phase-shift full-bridge. The two switches on each bridge leg have 50% duty ratio, one switch turns on right after the other one is turned off. This provides ZVS condition since the body diode of the switch turns on to bring down the voltage across it right before the switch is turned on. However, the phase-shift full-bridge has four MOSFETs and are too complicated for small power applications.

In this Chapter, a novel phase-shift half-bridge topology is proposed. Both MOSFETs of the proposed half-bridge topology obtain the ZVS condition for turns on. The output regulation is carried out by the phase-shift angle. Unlike the asymmetric half-bridge topology, there is no DC bias in the transformer and the stress of the component is even due to the symmetrically switching.

6.2 Proposed phase-shift half-bridge DC-DC topology

Fig. 6.4 shows the phase-shift DC-DC converter block diagram. The bridge cells output square wave with 50% duty ratio. A phase difference described by the phase shift angle α exists between the two square waves, which regulate the output.

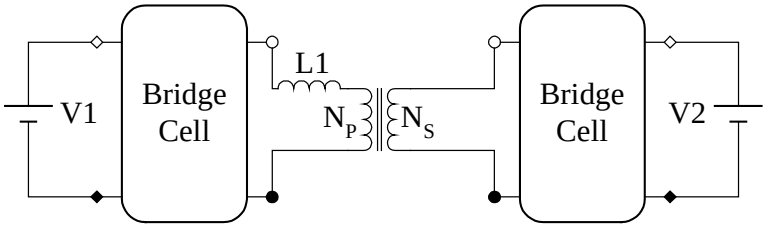


Fig. 6.4 the phase-shift control block diagram

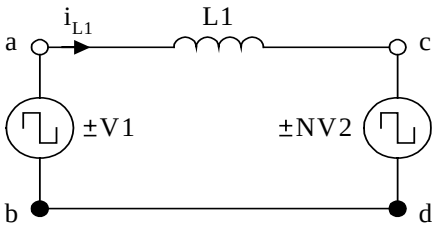


Fig. 6.5 the simplified model for phase-shift control

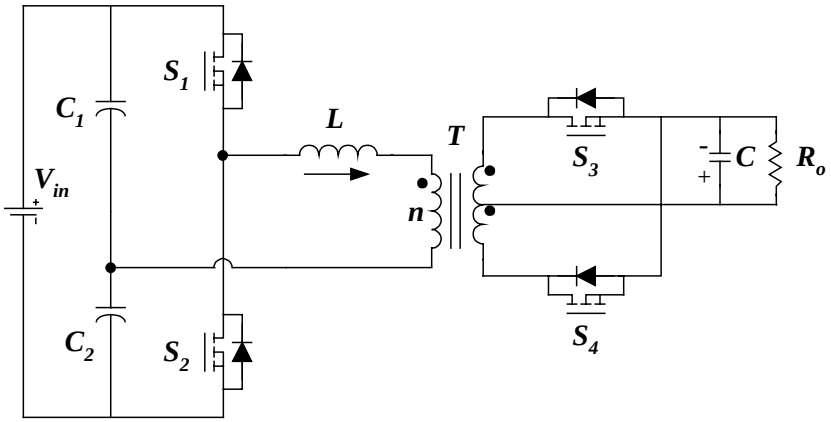


Fig. 6.6 The proposed phase-shift DC-DC converter

The proposed phase-shift DC-DC converter is shown in Fig. 6.6 and has the following features:

1. Both switches are turned on with ZVS. The driving signals for the two MOSFETs have 50% duty ratio, one MOSFET is turned on right after the other turned off. The energy stored in the inductor discharges the junction capacitor, brings down the voltage across it to zero and creates the ZVS condition for the switch to be turned on.
2. No ringing presented. Right after one switch is turned off, the body diode of the other switch conducts carrying the inductor current. As a result, the MOSFET drain to source voltage is clamped and the oscillation between the inductor and the junction capacitor of the MOSFET is eliminated which reduced the power dissipation and provides a good solution for EMI noise.
3. Simple. The proposed topology has the same component counts as the conventional half-bridge topology.

4. Easy to implement. Due to the popularity of the phase-shift full-bridge topology, a large variety of commercial available phase-shift PWM controller such as UC3895 can be used for the proposed phase-shift half-bridge topology.

6.3 Operation modes analysis

The proposed topology is shown in Fig. 6.6. The driving signal is shown in Fig. 6.7. The driving signals of S1, S2 and S3, S4 are complimentary with dead time between them so that the ZVS operation is easy to be obtained. S4 driving signal is phase-shifted with respect to S1. The voltage and current waveform for the inductor is shown in Fig. 6.7. The operation mode is shown from (a) to (f) in Fig. 6.8.

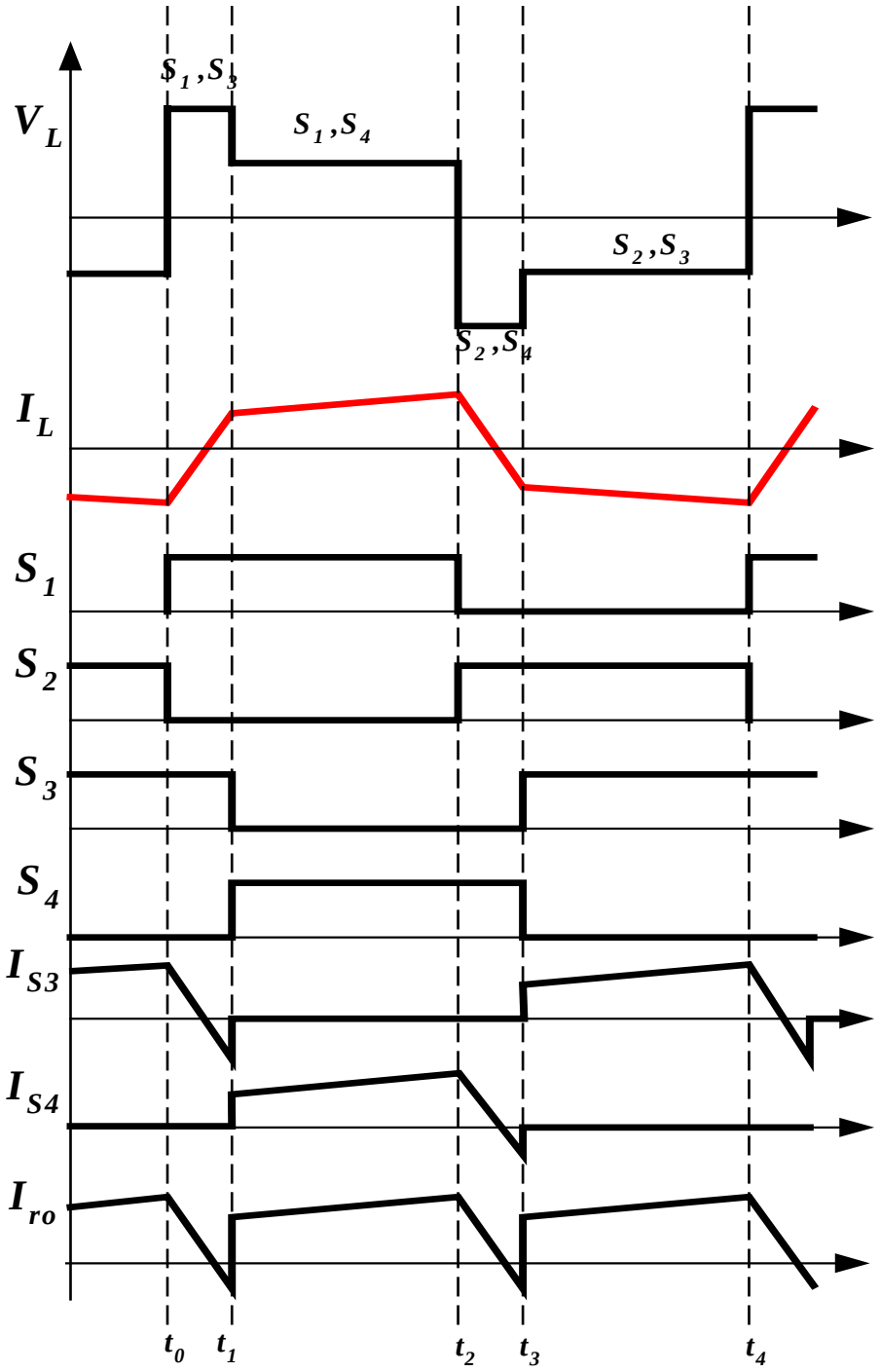


Fig. 6.7 the key waveforms for the phase-shift bi-directional DC-DC converter

The commutation time is decided by the phase-shift angle as below:

$$t_1 = \frac{\alpha}{180} \cdot \frac{Ts}{2},\ t_2 = \frac{Ts}{2},\ t_3 = \frac{Ts}{2} + t_1,\ t_4 = Ts \tag{6.1}$$

Ts is switching period, Ts=1/fs, fs is the switching frequency.

Mode 1 *($t_0<t<t_1$):* For t=t0, inductor current is negative, S1 and S3 are on. The inductor current keeps decreasing and drops to zero. The secondary side current decreases and reaches zero at the same time. Then the primary current goes positive and the secondary current goes negative. For the whole process, voltage applied on the inductor is:

$$V_L = \frac{1}{2}V_{in} + \frac{n_1}{n_2}V_o \tag{6.2}$$

n1 and n2 are the transformer primary and secondary winding turns number respectively.

The current slop is:

$$k_1 = \frac{\frac{1}{2}V_{in} + \frac{n_1}{n_2}V_o}{L} \tag{6.3}$$

The inductor current is:

$$i_{L1} = -i_{P2} + k_1 \cdot t \tag{6.4}$$

i_{P2} is the instant current value at point P2.

Mode 2 *($t_1<t<t_2$):* At t1 moment, S3 is turned off and S4 is turned on. The reflected voltage from the secondary side changes its polarity and the voltage across the inductor changes to:

$$V_L = \frac{1}{2}V_{in} - \frac{n_1}{n_2}V_o \tag{6.5}$$

The current slop is $k_2 = \dfrac{\frac{1}{2}V_{in} - \frac{n_1}{n_2}V_o}{L}$

The inductor current is:

$$i_{L2} = i_{P1} + k_2 \cdot (t - t_1) \tag{6.6}$$

i_{P1} is the instant current value at P1.

Mode 3 *(t_2<t<t_3):* At t2 moment, S1 is turned off and S2 is turned on. The voltage across the inductor is:

$$V_L = -\frac{1}{2}V_{in} - \frac{n_1}{n_2}V_o \tag{6.7}$$

The inductor current is:

$$i_{L3} = i_{P2} - k_1 \cdot (t - t_2) \tag{6.8}$$

Moe 4 *(t_3<t<t_4):* At t3 moment, S4 is turned off and S3 is turned on. The voltage across the inductor is:

$$V_L = -\frac{1}{2}V_{in} + \frac{n_1}{n_2}V_o \tag{6.9}$$

The inductor current is:

$$i_{L4} = -i_{P1} - k_2 \cdot (t - t_3) \tag{6.10}$$

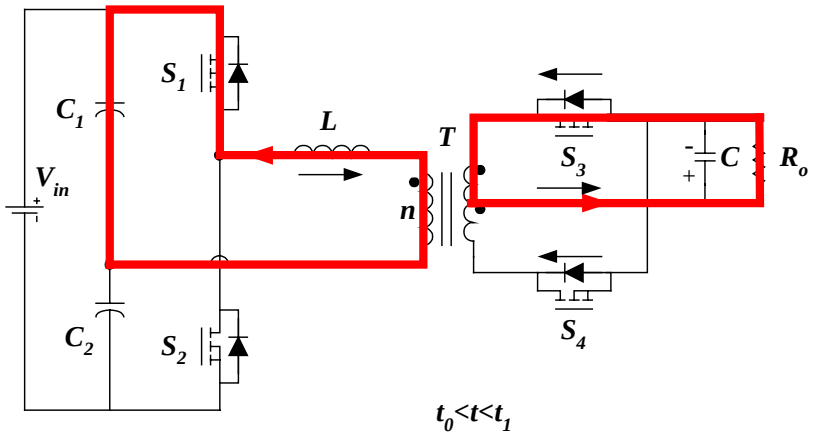


Fig. 6.8 (a)

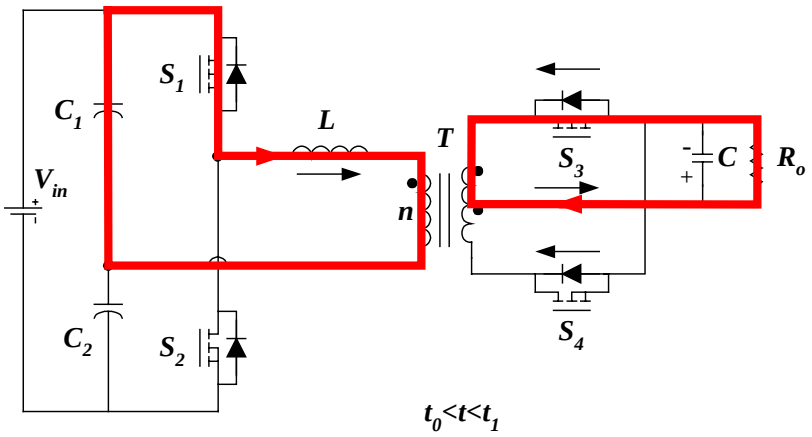


Fig. 6.8 (b)

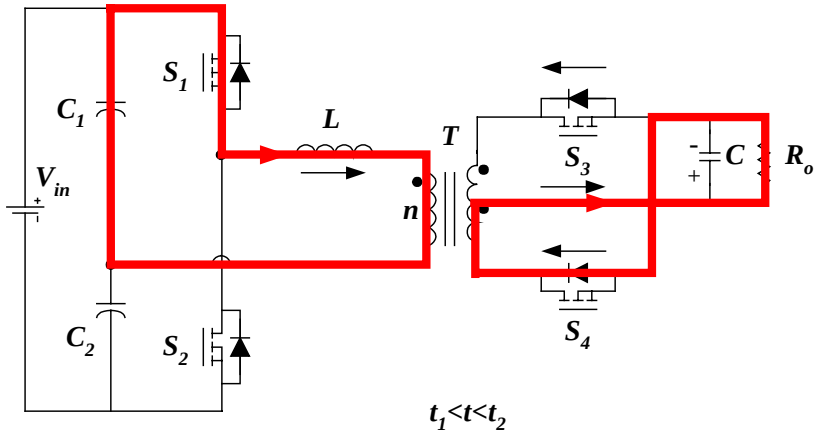


Fig. 6.8 (c)

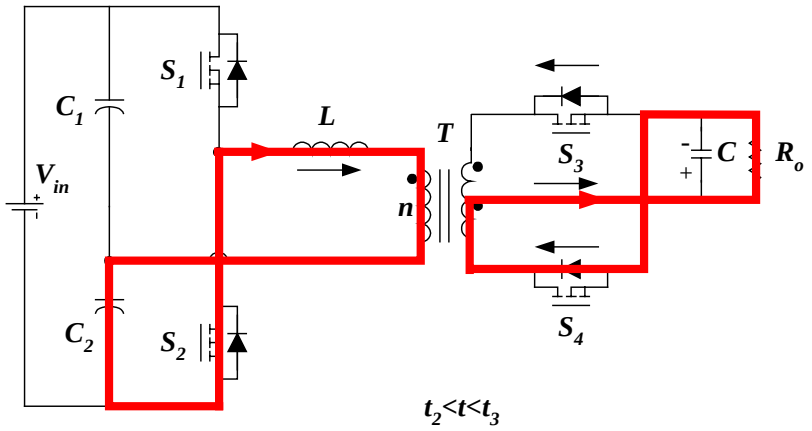


Fig. 6.8 (d)

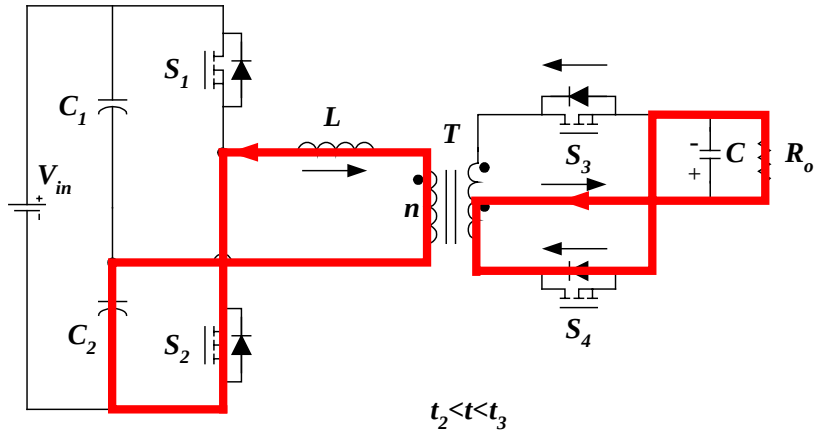


Fig. 6.8 (e)

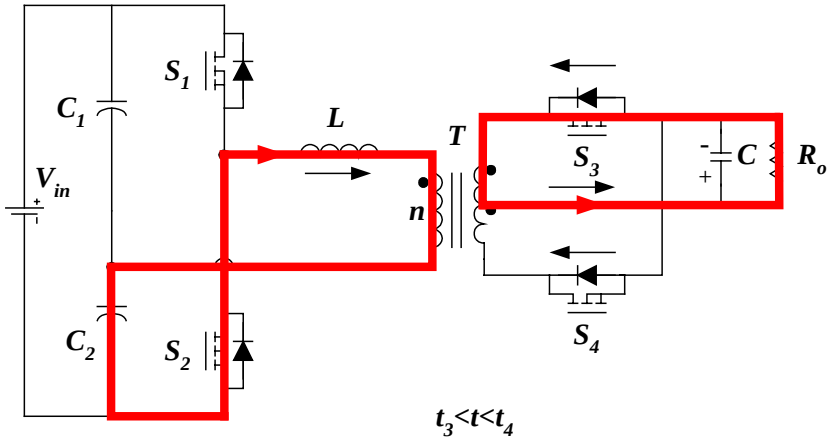


Fig. 6.8 (f)

Fig. 6.8 The operation modes analysis

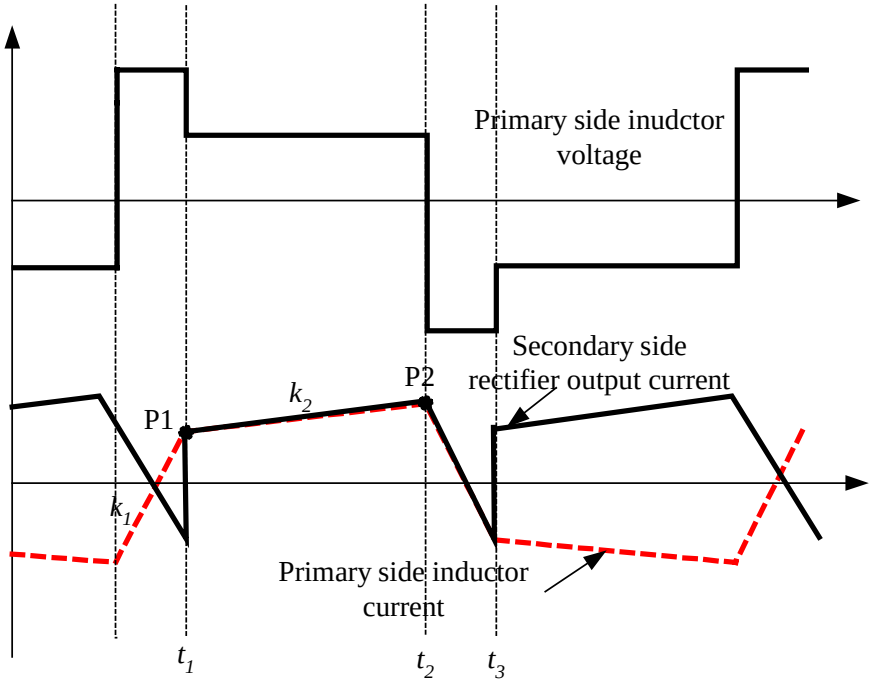


Fig. 6.8 the key waveforms for the phase-shift bi-directional DC-DC converter

From the analysis above, the peak to peak current is calculated as:

$$i_{pp} = k_1 \cdot DT_s + k_2(1-D)T_s \tag{6.11}$$

i_{P2} is obtained as:

$$i_{P2} = \frac{1}{2} i_{pp} \tag{6.12}$$

So we get i_{P1}:

$$i_{P1} = i_{P2} - k_2 \cdot (t_2 - t_1) \tag{6.13}$$

The average rectifier output current is shown below:

$$i_{oavg} = \frac{1}{\frac{1}{2}Ts} \cdot [\int_0^{t1} (-i_{L1}) \cdot \frac{n_1}{n_2} dt + \int_{t1}^{t2} i_{L2} \cdot \frac{n_1}{n_2} dt] \tag{6.14}$$

Since the output capacitor does not take DC current from average point of view, the average filter output current is exactly the load current. The equation is established based on the analysis before:

$$i_{oavg} = \frac{v_{out}}{R_{load}} \tag{6.15}$$

Solve the equation using the expressions 4.14, the output voltage is obtained. The result is so complicated and is omitted here. Curves describing the relationship between parameters are shown below to get a clear picture of the phase-shift bi-directional DC-DC converter.

The design parameters are:

n1=12 turns, n2=1 turns, fs=300kHz, Vin=48V, Ro=0.05Ohm, Lk=3.6uH.

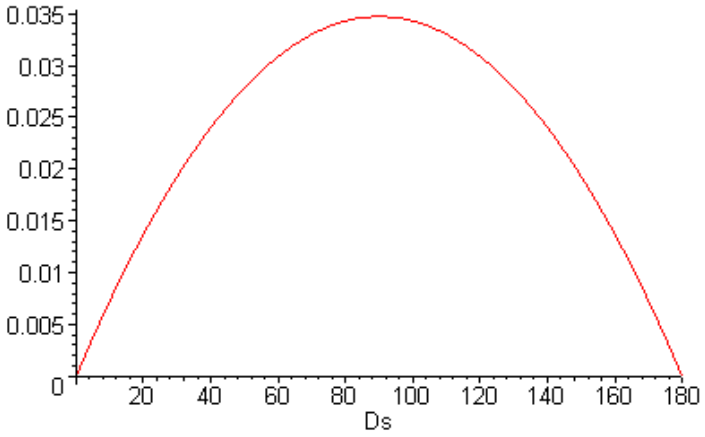


Fig. 6.9 voltage gain vs. phase-shift angle

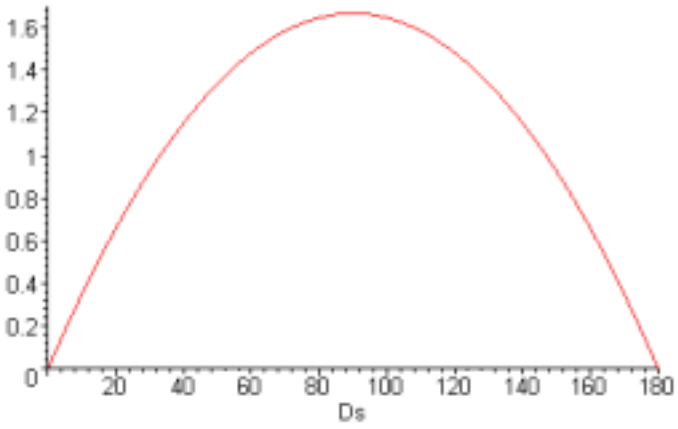


Fig. 6.10 output voltage vs. phase-shift angle

The voltage gain vs. phase-shift angle takes the transformer turns ratio n1/n2 into consideration. The converter gain is not proportional to the phase-shift angle, the maximum gain is obtained at 90^{o}. For zero and 180^{o} phase-shift angle, the gain is very small since the average of the filter output current is zero. The power source does not deliver power to the load.

The reactive power comes from the load is different for different phase-shift angle. It reaches zero for approximately 40 degree phase-shift angle. This is the case for conventional rectifier circuit since no current flows out from the load. For zero or 180 degree phase-shift angle, the current flows out from the load is equal the one to it, the average power is zero.

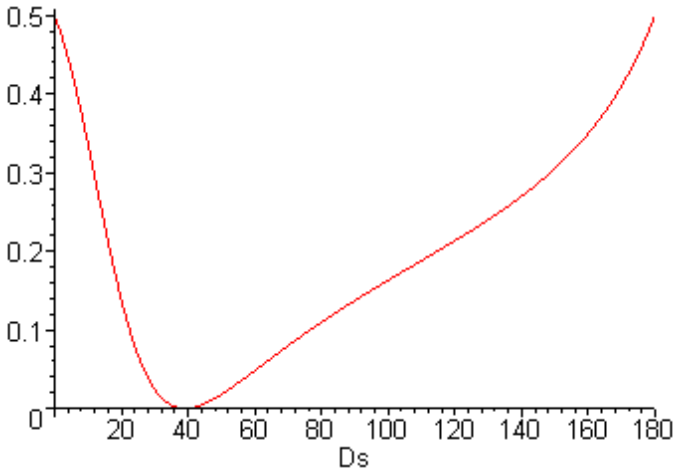
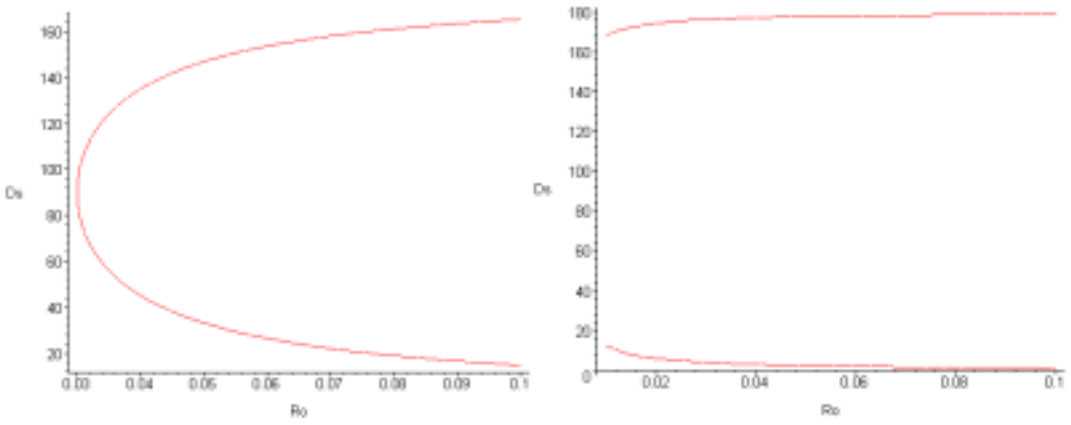


Fig. 6.11 Q/(Q+P) vs. phase-shift angle

(Q: reactive power, P: active power, n1=12; n2=1; fs:=300kHz; Vin=48; Ro=0.05; Lk=3.6uH;)

To keep the output voltage stable, the phase-shift angle varies with the load change. Fig. 6.12 shows for given load, there are two possible phase angle which keep the output stable. The lower curve is preferred since less reactive power induced which reduce the power losses. The power delivery capability of the phase-shift half-bridge DC-DC converter is also shown in Fig. 6.12. If the inductor is too large, for given switching period, the current cannot reach the desired value since slope is inversely proportional to the inductance. This limited the total power delivered to the load. As a result, the inductor should be carefully designed for practical applications.



(a) Lk=3.6uH (b) Lk=200nH

Fig. 6.12 the phase-shift angle vs. different load

(n1=12;n2=1;fs:=300kHz;Vin=48V;Vo=1V;)

For the phase-shift control the power loss is an important issue to be considered. As mentioned before, different phase-angle leads to different reactive power and power losses. For given output voltage, the phase-angle is affected by both the inductor value and the turns ratio selected by designer. Inductor value directly affects the power delivery capability and turns ratio affects the phase-shift angle, which affects the reactive power and power losses. For optimized design, the inductor and turns ratio are carefully selected aimed at the lowest secondary rms value at full load.

Fig. 6.13 shows one optimization example. In the 3D plotting, x-axis is the inductor value and y-axis is the turns ratio. The z-axis is the rms current flows through one channel MOSFET in the secondary side. We can choose Kn=14 and Lk=600nH to obtain minimum power losses for 1V@25A output.

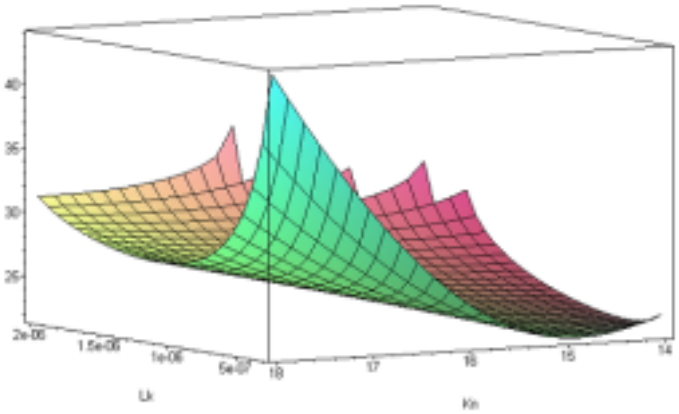


Fig. 6.13 The optimum inductance and turns ratio for minimum rms current in switch

(Vin=30, Ro=0.04, fs=500kHz, Vo=1, Cout=500uF)

6.4 Simulation verifications

One phase-shift bi-directional DC-DC converter simulation model is built in Pspice with the following parameters:

Vin=36V, primary side winding turns number np=10, secondary side winding turns nuber ns=1, L=5uH, C=400uF, load resistor R=0.1ohm.

To disregard the effect from the transformer turns ratio on the converter gain, the converter gain is defined as:

$$gain = \frac{Vout}{Vin \cdot \frac{ns}{2np}} \tag{6.16}$$

The output voltage and gain vs. phase-shift angle is shown in Fig. 6.14.

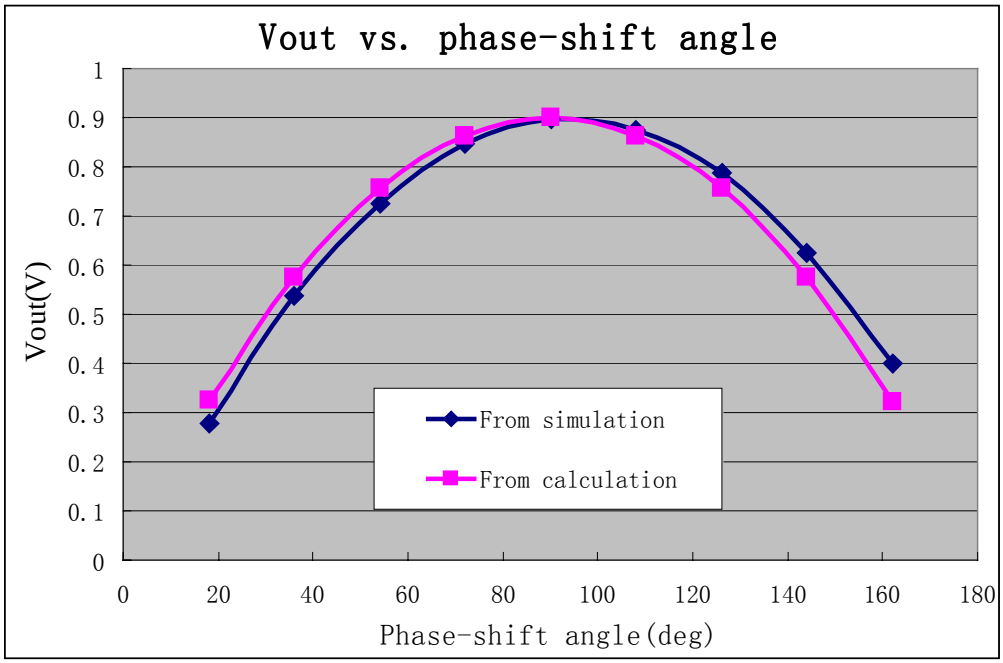


Fig. 6.14(a) The output voltage vs. phase-shift angle.

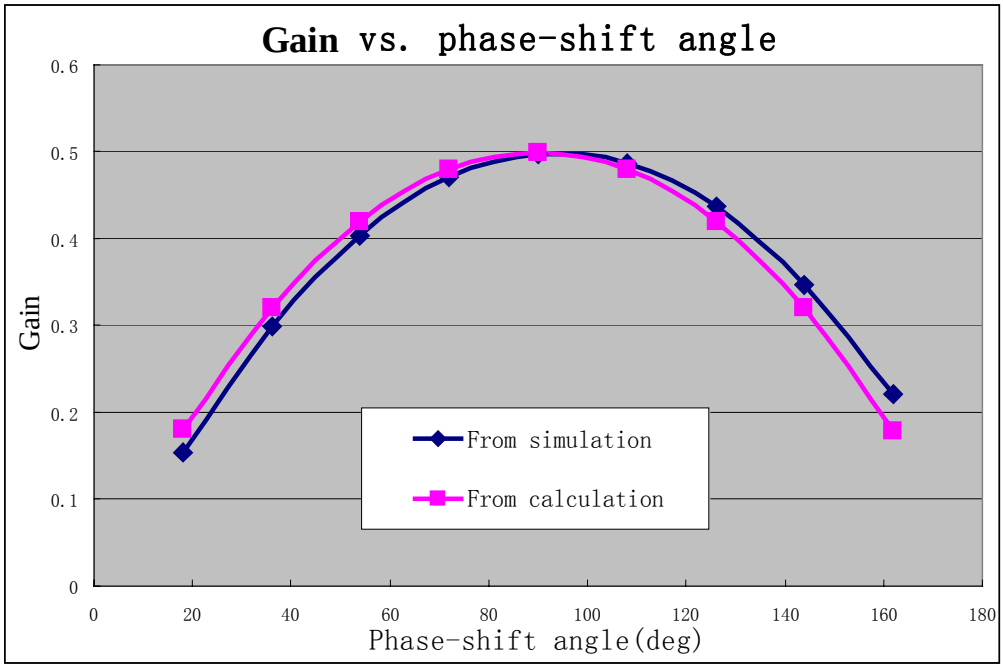


Fig. 6.14(b) The converter gain vs. phase-shift angle

Fig. 6.14 The comparison between calculation results and simulation results

As shown in Fig. 6.14, the output and gain vs. phase-shift angle curve between the simulation results and the calculation results agree with each other very well, which verified the analysis carried out before.

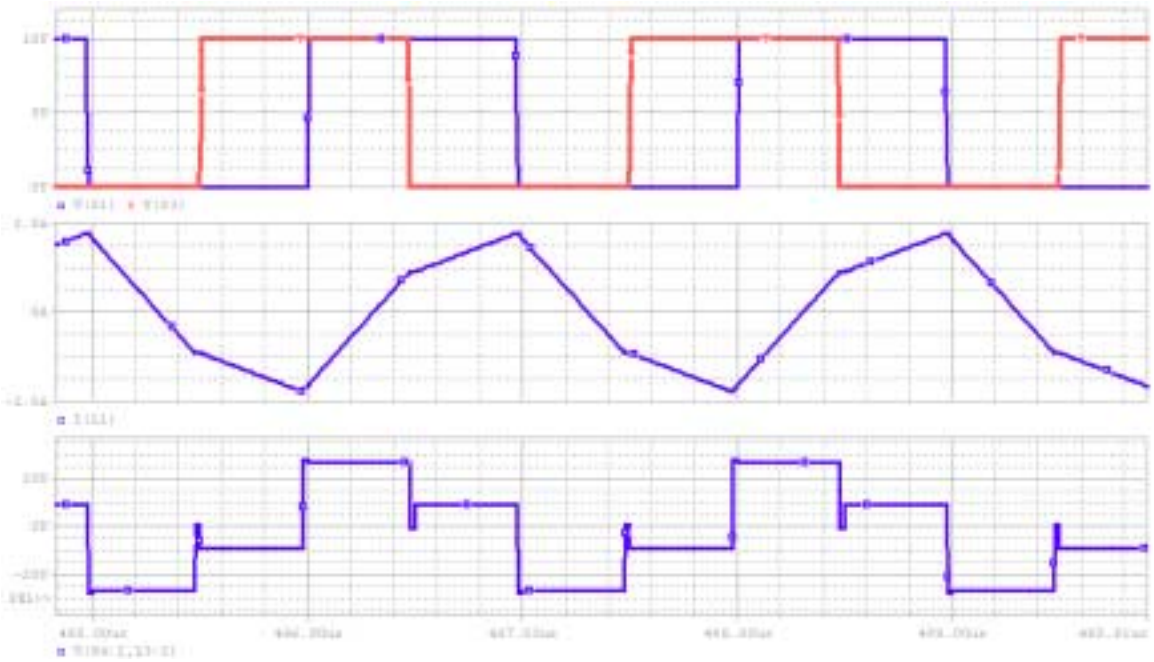


Fig. 6.15 Key simulation waveform

The key simulation waveforms are shown in Fig. 6.15. The top traces are driving signals for S1 and S3 with the overlap decided by the phase-shift angle. The middle trace is the current flowing through the inductor. The bottom one is the voltage applied on the inductor. Different with the one shown in Fig. 6.7, there are glitches in the inductor voltage waveform at the moment when S3 is turned off (turned on). Since the driving signals for S3 and S4 are complimenary with small deadtime between them to prevent short circuit, during the commutation between S3 and S4, that is, when both switches are off, the primary side inductor current keeps flowing through the transformer winding. As

a result, there is current flowing through the body diode of the secondary side SR MOSFETs. Therefore, the voltage applied on the secondary side winding is equal to the sum of output voltage and the body diode forward voltage drop. When the diode forward voltage drop reflected to the primary side, the voltage applied on the inductor is reduced.

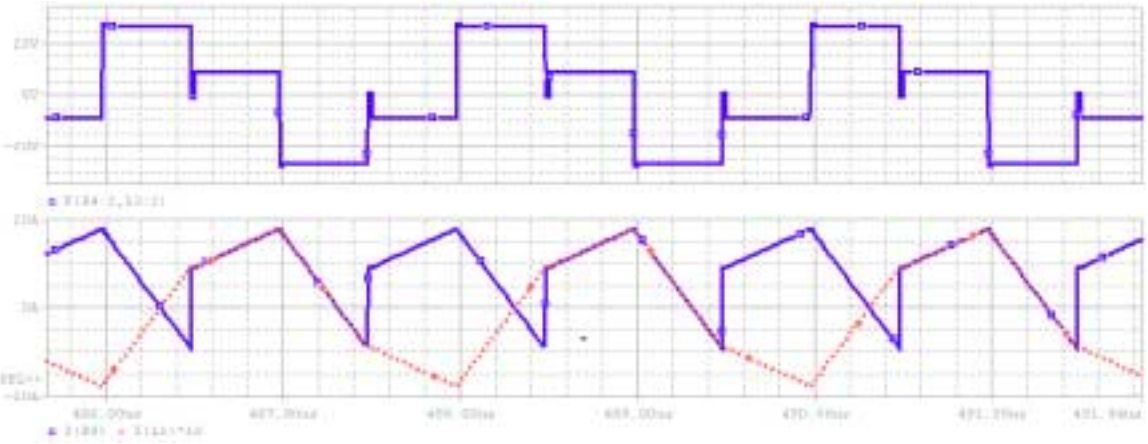


Fig. 6.16 Key simulation waveforms

In Fig. 6.16, the top trace is the primary side inductor voltage waveform. In the bottom traces, the solid line shows the current waveform of the rectifier, which is the sum of the current flowing through the two SR MOSFETs. The dashed line shows the primary inductor current waveform. To compare with the rectifier output current waveform, the inductor current waveform is scaled by the transformer turns ratio np/ns=10.

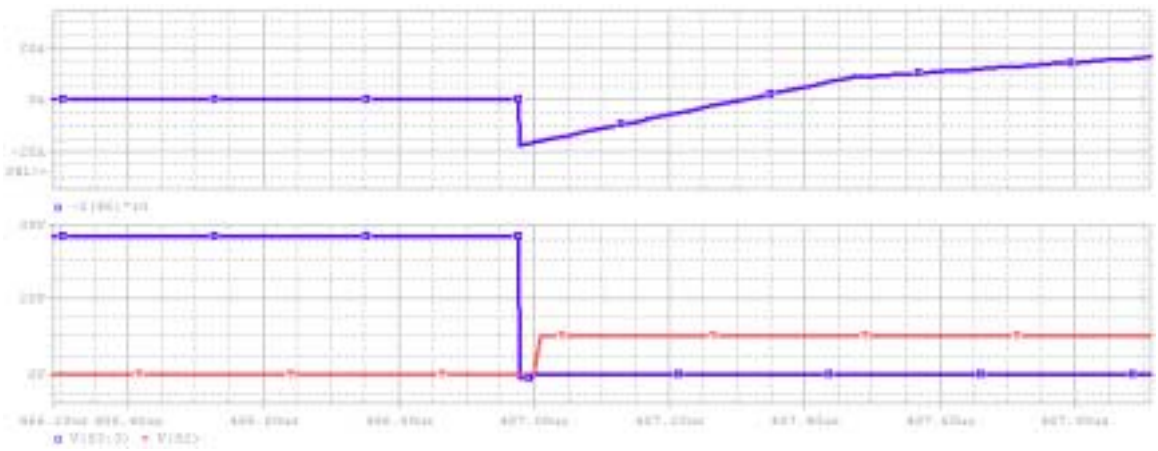


Fig. 6.17 ZVS of the primary power MOSFET

The ZVS of the power MOSFET is illustrated in Fig. 6.17. The top trace is the current flowing through the MOSFET, in the bottom traces, the blue one is the voltage across the MOSFET, the red one is the MOSFET driving signal. When the other MOSFET is turned off, the current of the inductor keeps freewheeling and the junction capacitor of the MOSFET is discharged bringing the voltage across it down to zero. After that, the body diode of the MOSFET conducts, carrying the inductor current and the voltage across the MOSFET is kept at the diode forward voltage. When the MOSFET is turned on, the loss is reduced significantly since the voltage across the MOSFET is equal to the body diode forward voltage, which is ignorable compared with half of the input voltage in the case of conventional half-bridge topology. It should be noted that, since the inductor has larger value compared with the leakage inductance of the transformer and it can store more energy, the MOSFET is easier to obtain the ZVS condition due to the sufficient freewheeling energy in the inductor. For the asymmetric half-bridge and the full-bridge topology, since the leakage inductor is the only component which store the energy to discharge the junction capacitor of the MOSFET and the leakage inductor is

usually small (less than 500nH), the MOSFET may lose ZVS when the load current is insufficient.

6.5 Summary

Switching frequency has very close relationship with the transient response and the converter efficiency. High bandwidth requires high switching frequency. However, switching losses increase significantly when frequency goes high. In this Chapter, a novel phase-shift half-bridge topology is proposed to reduce the switching frequency while has the ability to regulate the output. Since the two power MOSFETs of the primary side half-bridge has both full duty ratio, the ZVS can be obtained, which reduces the switching loss significantly. The ringing existing in the conventional symmetric half-bridge topology is eliminated due to the complementary driving of the primary side MOSFETs. This provides a good solution for the EMI noise. Compared with the phase-shift full-bridge topology, the proposed topology has less switches, which is more suitable for low power applications. The operation modes of the proposed topology are analyzed and the relationship between the converter gain and the phase-shift angle is modeled. The simulation results verified the analysis of the proposed phase-shift half-bridge topology.

7. THE POWER LOSSES ESTIMATION PLATFORM FOR POWER ELECTRONICS CIRCUIT

7.1 Introduction

The importance of accurate and rapid evaluation of the power losses in power electronics is increasing to achieve systems with higher efficiency and reliability. A number of approximation methods for estimating power electronics losses have been presented in the open literature [G1-G5]. However, power losses estimation models with higher accuracy and lower complexity are rare, since higher accuracy models [G2] usually turn out to be complicated and big effort is required to apply the model on the system evaluation. For large power electronics systems, more cost needs to be invested in system evaluation. For simplified models [G4], the approximation results may be obtained in a short time with less investment. However, the results may not satisfy the requirements for some high precision evaluations.

Conducting experiments is a good way to get accurate results. However, big investment in time, effort, and money is required to build the hardware platforms. When there are more than one candidate systematic solutions to be investigated, huge amount of work is expected when all solutions are tried one by one on the hardware experimental platform.

In this paper, virtual system models are built and verified by experimental results. The power losses analysis platform was built by integrating powerful analysis software

including OrCAD Pspice A/D™, Maxwell™ and MathCAD™. The platform can precisely quantify the losses including driving losses, conduction losses and switching losses of semiconductor devices. Moreover, magnetic components losses including core losses and AC copper losses for transformers and inductors are also precisely estimated in the software analysis. Detailed power losses analysis for a selected topology is presented in this paper. The estimated efficiency curves are compared to actual experimental efficiency measurements.

The analysis platform operational block diagram and analysis principle as well as some technical issues are discussed in detail in section II to IV. In section V, a phase-shift half-bridge DC-DC converter is used as an analysis example. The analysis results are compared with the experimental measurement, which verified the validity of the software analysis platform.

7.2 Proposed analysis platform

The platform operation consists of three parts: the Pspice A/D™ [G6] simulation, the data file conversion and data extraction and the MathCAD™ [G7] analysis. The block diagram is shown in Fig. 7.1.

For a given topology, simulation is done in OrCAD Pspice A/D™, and all current and voltage data on all components are stored in data file ‘pp.csd’. Since only part of the data are useful for the analysis, one C-code program is developed to extract the needed data from the simulation output data file and output the important data in a format that can be read by MathCAD™. In MathCAD™, power losses for all the key power components

are calculated using the imported simulation waveform data. The same process repeats, and new data is obtained when the input or output for the converter changes (i.e. different output power). After analysis at all operation conditions is finished, the analysis results are exported to other software in post processing. Statistics graphics are generated, which provided a clear picture for the power dissipation in the topology. Comparisons between solutions can also be easily obtained.

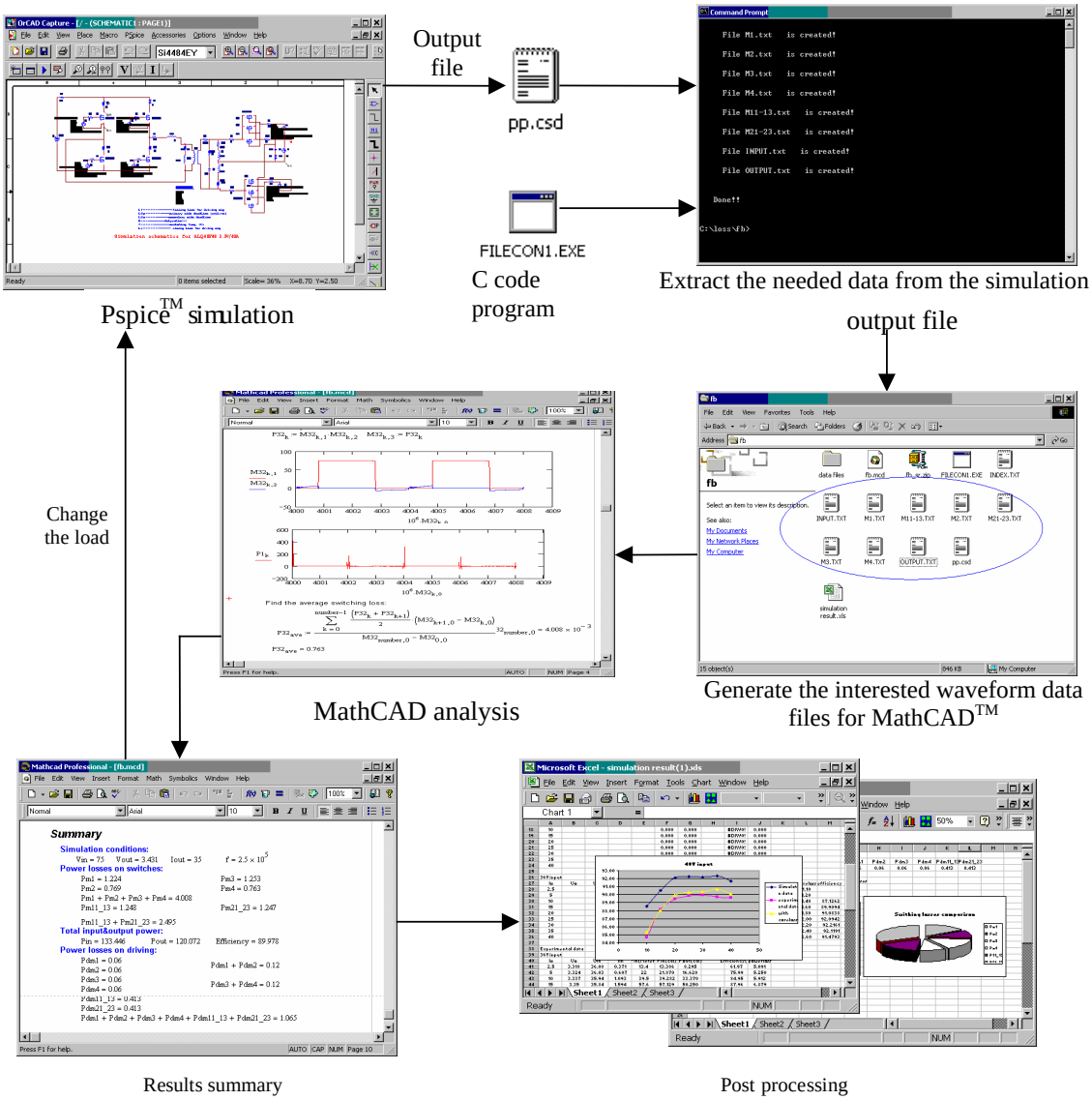


Fig. 7.1 Block diagram for the analysis platform

7.3 Features of the proposed platform

The software analysis platform is fast and easy to use on any topologies. The key features for the proposed platform features include:

- Relatively accurate analysis: the voltage and current data for the key components come from the Pspice simulation. If the Pspice model is accurate enough, the losses analysis is accurate. The power losses calculation uses the output waveform data from the Pspice simulation, and it is different with the approximate calculation and has higher accuracy.
- Fast analysis: All operations are carried out automatically; only simulation parameters configuration needs to be done by human. Time consumed in the analysis comes mainly from the simulation. When simulation is finished, just several simple mouse clicks, the power losses on the key components are displayed on the screen. Based on the analysis results, more processing can be made, such as the statistics analysis, the graphic output and the comparison between different components in the topology. A more straightforward understanding is possible based on the platform.
- Comparative analysis: The comparison for different simulation parameters is feasible using the losses analysis platform. All data files for given simulation conditions are stored on the disk, after all simulations are done, the comparison can be made immediately.

- General analysis: The analysis platform integrates powerful analysis software (Pspice A/D™, Maxwell™ and MathCAD™). Since the software is designed for general purpose, the platform can be used on any topologies.

7.4 Platform operational principles

Some technical issues arise when constructing the analysis platform.

The software interface:

Pspice A/D™ provides two formats for data output, the binary format and the Common Simulation Data File (CSD) format. Simulation data are compressed in the binary format but are not easily read by other software. CSD format enables data stored in an ASCII file and is accessible to other software. Since all waveform data is stored in one single file, a C-code program is developed to extract the ones we are interested in. Files are generated according to the components to be analyzed. The data storage format is also converted by the C-code program so that it can be recognized by MathCAD™. The Ccode program is designed for general purpose, for a different topology, and only the index file for the C code (index.txt) needed to be modified to extract the other specified waveform data.

MathCAD™ analysis:

The losses of the converter consist mainly of two parts, the losses on MOSFETs and the losses on magnetic components, i.e. the transformer and the inductor.

7.4.1 Losses on MOSFETs

The losses on the MOSFET can be divided into three parts: the on-state losses, the transient losses during the turn-on and turn-off transition and the driving losses. For the on-state losses, it is relatively easy to predict given the on-state resistance of the MOSFET. That is,

$$P_{on} = I^2 R_{on} \tag{7.1}$$

In which I is the rms value of the current flows through the MOSFET, and the R_{on} is the on-state resistance between drain and source. For the transient losses, approximate method may be used taking the current and voltage changes linearly. However, no accurate equations are available to calculate due to the complicated process in turning on and turning off of the MOSFET. In the analysis platform, the voltage and the current waveforms in one switching period are obtained using Pspice simulation, and data of all points are imported to the MathCAD to calculate the losses including the on-state losses and the transient losses of the MOSFET accurately.

The power losses for the switches are calculated using the trapezoid rule as shown in Fig. 7.2.

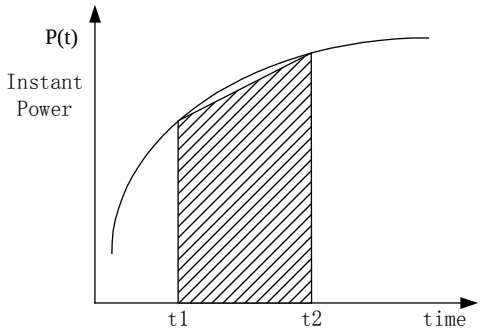


Fig. 7.2 The trapezoid rule for power losses calculation

The instant power is calculated as:

$$P(t) = i(t) \times u(t) \tag{7.2}$$

i(t) and u(t) are the instant current and voltage value for the MOSFET. They are obtained from the Pspice simulation.

Using trapezoid rule, the power dissipated from t1 to t2 is:

$$W(t_1) = \frac{[P(t_1) + P(t_2)] \times (t_2 - t_1)}{2} \tag{7.3}$$

The average power in one switching period is:

$$P_{ave} = \frac{\sum_{k=0}^{n} W(t_k)}{t_n - t_0} \tag{7.4}$$

The accuracy of the analysis relies heavily on the accuracy of the Pspice model. MOSFET models are provided by the Vishay™ Website (www.vishay.com) and are modified to facilitate the simulation.

The driving losses are calculated as follows:

$$P_{drv} = n \cdot V_{gs} \cdot Q_g \cdot f_s \tag{7.5}$$

n is the number of MOSFETs working in parallel. V_{gs} is the voltage applied between the gate and the source to turn on the MOSFET, Q_g is the gate charging provided by the manufacture datasheet and f_s is the switching frequency. For three Si7892DP MOSFETs operated in parallel at 250kHz switching frequency with 10V driving voltage, the driving losses are approximately 0.4W, which matches the experimental data.

7.4.2 Losses on magnetic components

The losses on magnetic components consist of two parts, the copper losses and the core losses. The copper losses for the inductor are relatively easy to calculate since DC losses are dominant.

$$P_{copper} = I^2 R \tag{7.6}$$

I is the rms value of the current flowing through the magnetic components and R is the equivalent resistance of the magnetic components. For the copper losses of the transformer, however, the equation above cannot be directly applied, since AC losses are dominant. Due to the skin effect, the equivalent resistance of the transformer windings is different with its DC counterpart. Maxwell™ is used to calculate the AC equivalent resistance. Fig. 7.3 shows the distribution of the current density on the cross section of the copper, and Table 7.1 shows the resistance comparison between the winding structures with different numbers of copper layers in the planar transformer.

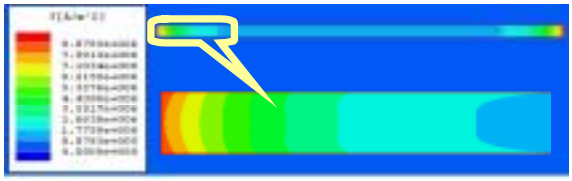


Fig.7.3 (a) One layer

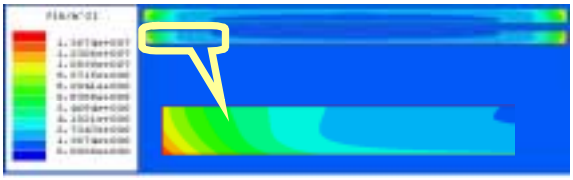


Fig.7.3 (b) Two layers

Fig.7.3 (c) Three layers

Fig. 7.3 The current distribution comparison for transformer structures with different layers

(f=500kHz; length=1m; width=3.5368mm; height=0.1284mm)

Table 7.1 The AC resistance vs. the DC resistance of the copper layer with different transformer winding structure

	DC	Single	Double	Triple
Resistance (ohm)	0.0379	0.0544	0.0768	0.0762

The core losses appear more complicated to calculate due to the nonlinear property of the magnetic material.

For the transformer, from Faraday's law we have:

$$\Delta B = \frac{V \cdot t_{on}}{N_p \cdot A} \tag{7.7}$$

In which, B is the magnetic flux density, V is the voltage applied on the windings of the transformer, for a full-bridge DC-DC converter, t_{on} is the time when the two diagonal MOSFETs are both on. t_{on}=DTs, where D is the duty ratio of the switch and Ts is the switching period. N_p is the turns number of the primary side winding and A is the

intersection area of the core. Power loss density P_v can be found by looking up the table provided by the datasheet of the core. The total loss for the transformer is calculated as:

$$P_{total} = P_{copper} + P_v \cdot V_{core} \tag{7.8}$$

Vcore is the volume of the core.

The core data are stored in software in advance, and all the processing is done by software automatically.

7.5 Simulation and experiment results

Fig. 7.4 is a DC-DC full-bridge converter with current doubler and synchronous rectifier. Simulation parameters are listed in Table 7.2. Simulation results are listed in Table 7.3 and 7.4. Interestingly, the results show that, the losses on M1, M3 and M2, M4 are different. This can be easily explained by the soft switching capability difference between the leading leg and the lagging leg in phase-shift control.

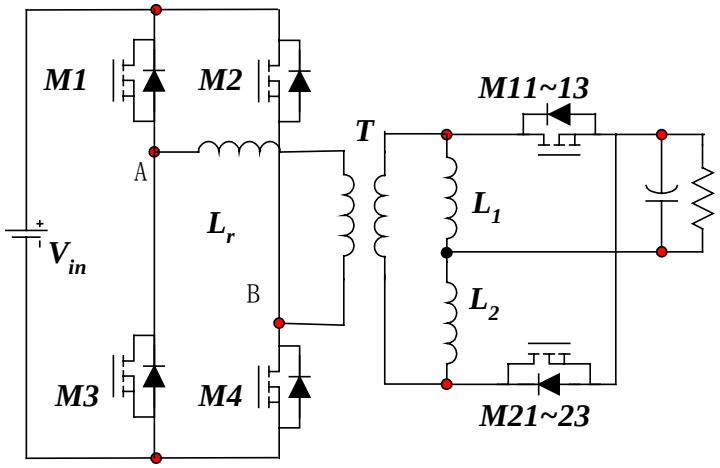


Fig. 7.4 The topology of the DC-DC converter for simulation

Table 7.2 The simulation parameters for key component

M1~M4	M11~13	M21~23	T1 core	L1 core	L2 core	Vin	Vout	Iout	fs
Si7454	Si7892	Si7892	PC44	3C96	3C96	48Vdc	3.3Vdc	30A	300kHz

Table 7.3 Losses on the key components

Component	M1	M2	M3	M4	M11-13	M21-23	T	L1	L2
Losses (W)	0.667	0.605	0.676	0.606	0.819	0.807	1.802	0.364	0.362

Table 7.4 Driving losses on the MOSFETs

Component	M1	M2	M3	M4	M11-13	M21-23
Driving losses	0.060	0.060	0.060	0.060	0.413	0.413

When all simulation points (at all possible load) are finished, the efficiency curve is generated. To verify the validity of the analysis, a full-bridge phase-shift isolated DC-DC converter with current doubler prototype is built with the specification as: Vin=48V, Vout=3.3, fs=300kHz, core material for transformer is PC44 and inductor core material is 3C96. Four Si7454 MOSFETs are used in the primary side full-bridge and six Si7892 MOSFETs are used for the secondary side current doubler. Fig. 7.5 shows the simulation efficiency curve and the measured efficiency curve in the experiment. It is clear that the simulation results are very close to the experimental ones. The difference between the two curves may results from simulation errors and some uncertain parasitic parameters. The unified temperature for the simulation also contributes to the difference between the curves (120^{o} C is used for the simulation).

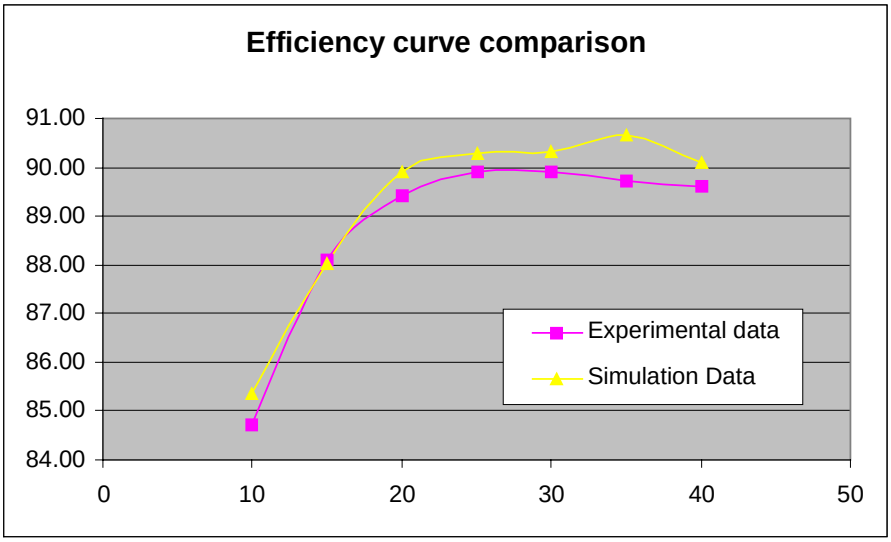


Fig. 7.5 The efficiency curves comparison for DC-DC converter

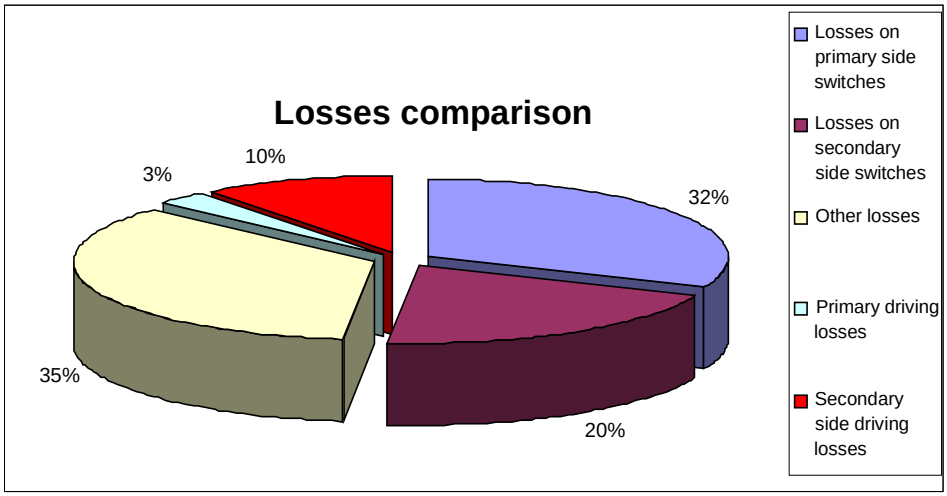


Fig. 7.6 The distribution of the power losses

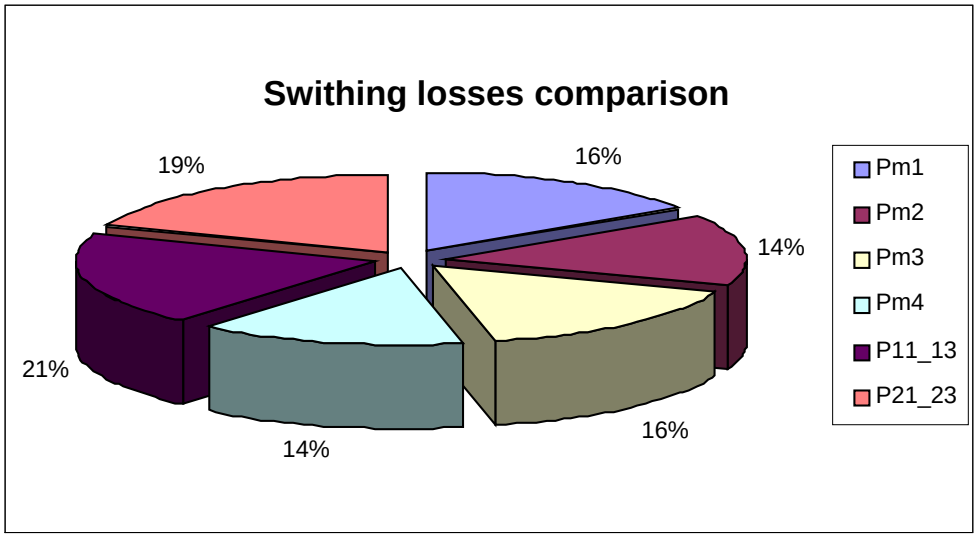


Fig. 7.7 The switching losses comparison for the MOSFETs

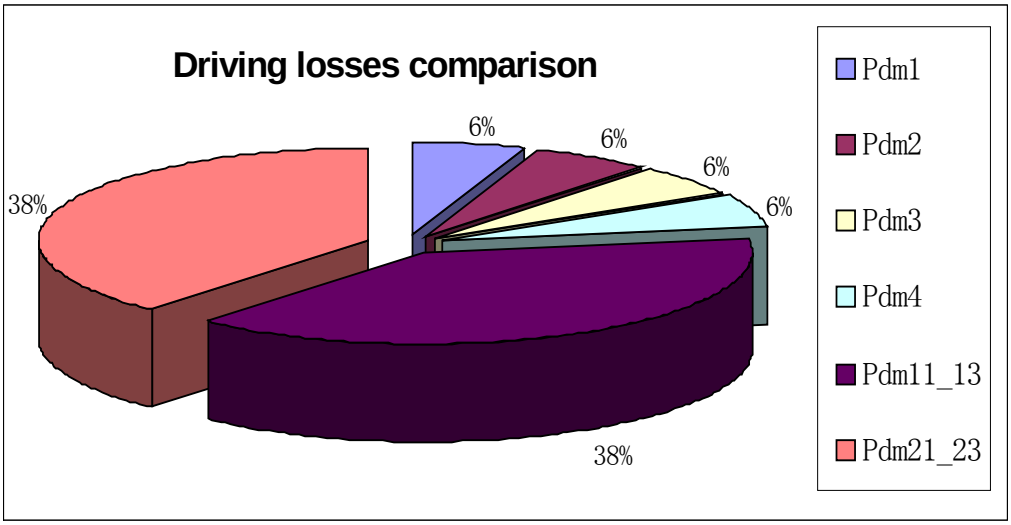


Fig. 7.8 The driving losses comparison for the key MOSFETs

Fig. 7.6 and Fig. 7.7 show the power losses distribution. Fig. 7.8 shows the driving losses comparison between the key MOSFETs. It is clear that driving losses in the secondary side are significant in synchronous rectifier MOSFETs. For a lowvoltage highcurrent DC-DC converter, the conduction losses on the secondary side are large due

to the high-current flow. More MOSFETs working in parallel is an effective way to reduce the conduction losses on the synchronous rectifier. However, the more MOSFETs in parallel, the more driving losses the secondary side are suffered. Therefore, an optimal point needs to be carefully selected to get the best performance for the converter.

7.6 Conclusion

A powerful losses analysis platform for general-purpose application is presented. The block diagram and the detailed analysis principle are introduced and the technical issue for the platform is discussed. A prototype is built and the efficiency curve at different load points is measured and is compared with the simulation result. The validity of the simulation platform analysis is verified by the comparison between the efficiency curves.

8. CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

In this dissertation, the on-board DC-DC converter for Distributed Power System is studied in the topology and control point of view focusing on two main aspects-the efficiency and the transient response, which are two key requirements for on-board DC-DC converters. The main points are summarized as below.

This work focuses on the half-bridge topology due to its popularity, simplicity and adaptability for low-voltage high-current applications. First, the half-bridge topology requires only two MOSFETs, which is only half of the number of full-bridge topology. This helps to reduce the cost for practical applications. Second, the natural step-down facilitates the transformer turns ratio design and makes the half-bridge topology more suitable for applications with low output voltage.

For the efficiency considerations, the power losses mechanism in on-board DC-DC converters are analyzed and the losses distribution are discussed. A big variety of power management concepts and techniques aiming at reduce the power losses in on-board DC-DC converters are proposed in this work and intensive analysis and verifications are carried out respectively.

For the power losses due to the ringings in the circuitry, new energy management concepts are proposed, which diverts the ringing energy so that the ringing is removed. Clear waveforms are obtained in the experimental prototype, which also provides a good solution for EMI issues due to the ringing in the conventional half-bridge topology. In

despite of the elimination of the ringing, the power losses in the additional circuitry are investigated. The results show that, the energy freewheeling concept is suitable for large duty ratio applications. Due to the big variation of the duty ratio when the input line voltage has big range, the freewheeling power losses are big which degrade the performance of the converter. However, the proposed energy storage concept is more suitable for small duty ratio applications since the ringing energy is stored on the clamping capacitor instead of freewheeling during the main power MOSFETs off interval. Experimental results indicate significant efficiency improvement for both proposed concepts, which verified the feasibility for applications.

The energy storage and release concept, on the other hand, makes use of the magnetizing energy while similarly keeping the energy on the clamping capacitor. The application of the concept is well demonstrated in active-clamp forward converter in which, the continuous energy freewheeling is prevented and the related loss is reduced.

Another clamping concept is proposed employing the lossless zener-capacitor block. Different with the conventional application of the zener diode, there is no loss on the capacitor in series with the zener diode. This allows it to be used on the driving optimization for all self-driven circuit so that the driving voltage is independent of the input condition. As a result, it can be used in bus converter in which the driving voltage is affected by the input line change. Calculation and simulation results both concluded that for correct design, the losses in the self-driven circuit with the proposed lossless zener concept are less than the conventional self-driven circuit, which verified the feasibility of the proposed concept and the derived application self-driven circuit.

Employing the phase-shift concept, a phase-shift half-bridge topology for DC-DC converters is proposed and analysis and simulation verifications are carried out aiming at reducing the power dissipations on the power MOSFETs. The results show that, all MOSFETs can obtain ZVS employing the phase-shift concept, which is verified by the simulation results. Unfortunately, the proposed phase-shift half-bridge topology requires careful design and good management of the reactive power flow.

One power losses estimation platform is proposed as a tool to evaluate the power losses of the key components in power electronics systems. It can be used to evaluate the power electronics systems prior to the expensive experiment and provides a simple way to compare different system schemes.

The control scheme study is the other important part of this work. A novel capacitor voltage imbalance correction concept is proposed for peak current mode controller half-bridge topology. This concept provides a control-orientated solution for voltage imbalance correction in symmetric and DCS half-bridge topology, which avoids the modifications on the power stage and gives the possibility for integrating the control concept in ICs. Since half-bridge topology is widely used in industry applications, the proposed concept and the derived implementation circuit have potentially broad applications. Followed by the experimental verifications of the proposed concept, the modeling work is done to provide the analytical insight into the physical behavior of the voltage imbalance in the peak current mode controlled half-bridge topology. The modeling work for the first time explained the failure mechanism of the peak current mode control on the symmetric and DCS half-bridge topology and also answered the question why the proposed voltage compensation concept can balance the capacitor

voltage as verified in the experimental prototype. Based on the work done in this dissertation, the peak current mode control is now ready to be applied on symmetric half-bridge and DCS half-bridge topology for DC-DC converters.

8.2 Summary of the improvements

This dissertation investigated the topology and control schemes in half-bridge DC-DC converters. Concepts for topology and control improvements for DC-DC converters are proposed and implementation is discussed, which verified by simulation and experimental results. The key improvements of this dissertation work can be summarized as the follows.

For the topology improvements, different energy management concepts are proposed aiming at efficiency improvement and are verified by analysis, simulation and experimental results.

- The energy freewheeling concept

  This concept is proposed to reduce the ringings caused by the leakage inductor and the junction capacitor of the power MOSFETs in the half-bridge topology. The energy is freewheeling during the off time of the two power MOSFETs and the ringing is removed due to the freewheeling of the leakage inductor energy.

- The energy storage concept

  This concept uses a clamping capacitor to store the leakage energy during the off time of the power MOSFETs so that the energy is not used in the ringings between the leakage inductor and the junction capacitor.

- The energy store and release concept

  In this concept, the leakage energy is first stored in the clamping capacitor and then released to create the ZVS condition for the power MOSFET. The magnetizing energy in the active-clamp forward topology is fully utilized and the freewheeling losses are reduced especially at small duty ratio condition.

- The lossless zener concept

  This concept is applied on DC-DC converters with self-driven circuit. The resistor is replaced by the capacitor, which reduced the power losses during the steady state. The driving voltage is stabilized at the same time so that the MOSFET driving can be optimized.

- The phase-shift concept

  The phase-shift concept is applied on half-bridge topology without complicating the converter structure. ZVS is obtained for all the switches and the power loss is reduced.

For the control improvements, the peak current mode control for half-bridge topology is proposed and the capacitor voltage imbalance is corrected in the proposed control scheme.

A powerful power losses estimation platform is also proposed as a powerful tool to evaluate the power losses in any power electronics circuit. Since the result is based on the simulation tools, the result is accurate compared with the approximation model.

8.3 Suggestions for future work

8.3.1 Implementation study for the integration of the peak current mode controller

The peak current mode control scheme on half-bridge topology is proposed and verified by the lab experimental prototype. The experimental peak current mode controlled half-bridge DC-DC converter is built with the proposed control schemes implemented on the control boards consist of discrete capacitors, resistors and opams. The bulky size and poor performance of the lab prototype due to the discrete components indicate more work is to be finished aiming at integration all the implementation circuits for the proposed control schemes to be used in commercial products. Circuit could be simplified and optimized in circuit integration point of view. In the lab experimental prototype, two current sensors are used to split the current signal into two channels. Further investigations may improve the current sensing and reduce the sensing circuit cost.

8.3.2 Studies on the clamping techniques

For the proposed energy management concept, the implementation circuit is proposed in Chapter 5 and verified by simulations. More practical issues can be investigated by further experimental work. The efficiency is the key concern to evaluate the performance of the proposed active-clamping snubber. The clamping MOSFET parameters and the leakage inductance of the power transformer can have big effect on

the active-clamping snubber performance. MOSFETs with low conduction resistance are preferred for the proposed energy freewheeling concept application. For the energy storage and release concept, the stress on the power switch is affected by the auxiliary clamping switch. Design guideline can be found in Chapter 5 and optimization work aimed at component stress and efficiency improvement is encouraged to obtain the optimum performance of the converter. For the lossless zener concept, the detailed operation analysis can be found in this dissertation and can also be used as the guideline of the optimization work for specific implementation on the DC-DC converters with self-driven circuit.

8.3.3 Further investigation on the possible applications of the phase-shift concept on other topologies

The phase-shift concept on the half-bridge topology is proposed in Chapter 6. The same concept can be applied on other topologies such as the full-bridge, push-pull. The reactive power is important for the system efficiency and there are more optimization work can be done for future research aimed at minimum reactive power, which reduce the power losses. The switching frequency is also a concern and the ZVS conditions for the power switch for specific applications need to be further investigated.

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