Chapter 5

Isolated Switch-Mode dc-to-dc Converters

INTRODUCTION

The discussion in Chapter 4 showed that the four basic converter topologies have their output conversions determined by the duty ratio, D, and that they consist of a single input and a single output with a common reference point. For applications in which the output voltage does not differ from the input voltage by a large factor, those topologies can be used. However, for many applications the input voltage is normally derived from an off-line half- or full-wave rectifier, and the output voltage is a very small fraction of the rectified dc input voltage. As a result, transformers must be added between the power stage and the output for the purpose of voltage scaling. Unlike line-frequency transformers, these transformers are high frequency and much smaller in size and weight. In addition, transformers are used in switched-mode converters for electrical isolation between the input and output, reduction of

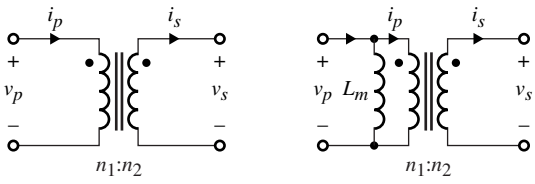
stresses in switching devices, and provision of multi-output connections. With isolation transformers, the output voltage polarity reversal does not become a design restriction. Also, in some applications, system isolation may be required by the regulatory body. However, the benefits obtained by adding isolation transformers come with a price. The major drawbacks include high converter volume and weight, reduced efficiency, and added circuit complexity to limit the effect of leakage inductance and avoid core saturation.

In this chapter, we will discuss some widely used high-frequency switched-mode dc-dc converters: the flyback, forward, push-pull, half-bridge, and full-bridge converters. It will be shown that the flyback converter is based on the boost converter, and the forward converter is based on the buck converter. In analyzing these converters, we will use the transformer model by including the magnetizing inductance. In all the dc-dc converters discussed in Chapter 4, the role of the inductor is to store energy as it comes from the source in one portion of the switching cycle and release it to the load in the other portion of the cycle. As the converter reaches the steady state, the mechanism of energy storage and release reaches equilibrium and the net energy stored in the inductor over one switching cycle is zero. In other words, energy in the inductor does not build up from one cycle to the next. Otherwise, if energy build-up in the inductor were allowed, soon the inductor would reach saturation. The issue of saturation is important not only for the inductor, but also for the transformer. Unlike converter topologies presented in Chapter 4, the topologies in this chapter require more than one switch, since the transformer must be magnetized and demagnetized repeatedly within a switching cycle, to avoid saturation. The conversion can be done unidirectionally, in which the magnetization current is positive, or bidirectionally, in which the magnetization current is positive and negative. Finally, we consider only the continuous conduction mode of operation for the isolated converters, since their dcm analysis is very similar to the dcm analysis presented in the previous chapter.

5.1 TRANSFORMER CIRCUIT CONFIGURATIONS

Transformer Model

An ideal transformer has no leakage inductances, an infinite magnetizing inductance, no copper and core losses, the ability to pass all signal frequencies without any power loss, and the ability to provide any level of current and voltage ratio transformation. Figure 5.1(*a*) shows an ideal transformer with its current and voltage relations. Figure 5.1(*b*) shows the equivalent transformer circuit including only the magnetic inductance, L_m, reflected in the primary side.



$$\frac{v_p}{v_s} = \frac{n_1}{n_2}, \quad \frac{i_p}{i_s} = \frac{n_2}{n_1}$$

Figure 5.1 (*a*) Ideal transformer model. (*b*) Transformer equivalent circuit including the magnetizing inductance.

Circuit Configurations

Throughout this chapter, as far as the primary side is concerned, two configurations of transformers are used: non-center-tap and center-tap. The non-center-tap configuration has three possible connections, known as single-ended, half-bridge, and full-bridge, as shown in Fig. 5.2(*a*), (*b*), and (*c*), respectively. The center-tap configuration is known as *push-pull* and is shown in Fig. 5.3.

As far as the transformer's secondary side is concerned, two configurations of transformer-rectifier connections are normally used: center-tap full-wave and bridge full-wave, as shown in Fig. 5.4(*a*) and (*b*), respectively. The center-tap arrangement results in one diode forward voltage drop, compared to two diode voltage drops for the bridge configuration.

These configurations are the most popular ones used in today's switch-mode power supply design. Since we have a dc source voltage across S_1 and S_2 of Figs. 5.2(*b*) and 5.3, the two switches are not allowed to close simultaneously. Hence, in a normal operation, S_1 and S_2 in these two configurations switch alternately, each having the same duty cycle. This will prevent transformer core saturation. In the full-wave bridge

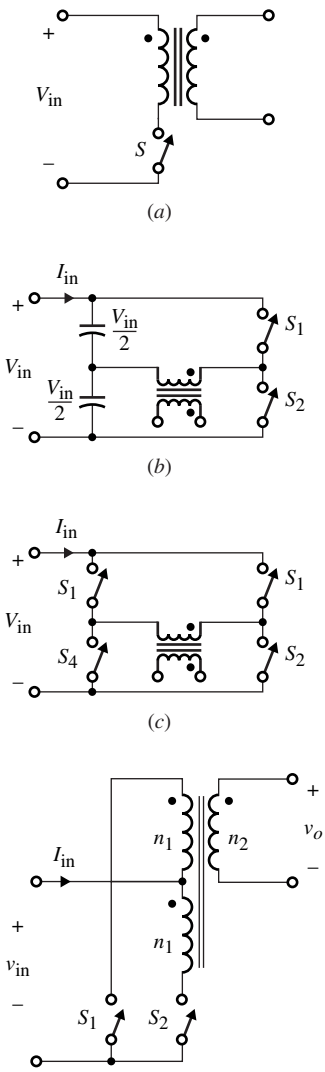


Figure 5.2 Transformer configurations: (*a*) single-ended, (*b*) half-bridge, and (*c*) full-bridge.

Figure 5.3 Push-pull transformer configuration.

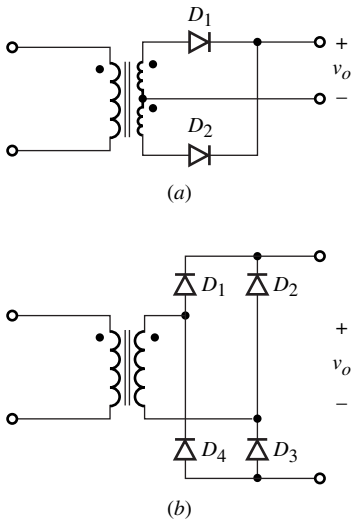


Figure 5.4 Transformer configurations in the secondary (load) side: (*a*) center-tap full-wave, and (*b*) bridge full-wave.

configuration, S_1 and S_3 are closed simultaneously in the first half cycle, and in the second half cycle switches S_2 and S_4 are closed simultaneously.

The difference between the two-switch transformer connections of Fig. 5.2(*b*) and Fig. 5.3 is that the switches in the former connection must be able to sustain a maximum voltage of V_{in} compared to $2V_{in}$ for the latter connection. However, in the push-pull configuration, each switch carries the average input current, I_{in}, whereas in the half-bridge configuration, each switch must carry twice the average input current. This is why the push-pull configuration is chosen when the source voltage is low. In the full-bridge case, each switch must be able to block V_{in} and allow a peak current equal to I_{in}. This makes it attractive for high-power applications. The only disadvantage of the full-bridge configuration is that it requires two floating driving circuits.

EXAMPLE 5.1

Consider the push-pull converter with a current source load shown in Fig. 5.5. If S_1 and S_2 are turned on and off according to the waveforms shown, determine the current and voltage stresses for S_1 and S_2 in terms of the average input current, I_{in}, and voltage V_{in}.

SOLUTION Consider the first half cycle, when S_1 is closed. The input voltage is applied to the upper primary winding of the transformer. An equal amount of voltage is also induced on the lower

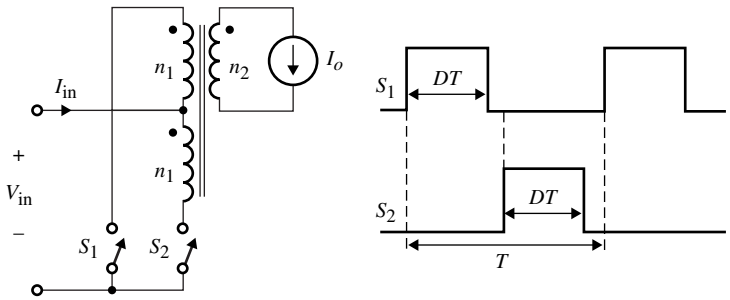


Figure 5.5 Circuit for Example 5.1.

Table 5.1 Comparison between Transformer Configurations

Transformer configuration	Maximum voltage stress across each switch	Maximum current stress through each switch	Core excitation and reset mechanism	Power level applications
Single-ended				
Forward	$\geq 2V_{in}$* $= (1 + n_3/n_1)V_{in}$	$\geq 2I_{in}$* $\geq I_{in}/D$	Unidirectional complex reset circuit	Low power <500 W
Flyback	$\geq 2V_{in}$ $= V_{in}(1 - D)$	$2I_{in}$ $\geq I_{in}/D$	Unidirectional and core reset not necessary	<200 W
Half-bridge	V_{in}	$2I_{in}$ $\geq I_{in}/D$**	Bidirectional and core reset not necessary	High input voltage, medium power with low source current <800 W
Full-bridge	V_{in}	I_{in} $\geq I_{in}/D$**	Bidirectional and core reset simple	High power >800 W
Push-pull	$2V_{in}$	I_{in} $\geq I_{in}/D$**	Bidirectional and core reset simple	Medium power with low source voltage

*I_{in} and V_{in} are average values.
**$D < 0.5$.

primary winding. The polarity of this voltage is in the direction of the input voltage. As a result, S_2 is subjected to twice the input voltage, i.e., $V_{stress} = 2V_{in}$. S_1 is also subjected to the same voltage stress when S_2 is turned on.

Neglecting the transformer's magnetizing current, the maximum switch current can be obtained as $I_{max} = I_{stress} > I_{in,ave}/2D = n_2 I_o/2n_1 D$ $(0 < D < 0.5)$. Depending on the value of D, the current stress on each switch can be much larger than the average input current.

The primary-switch connections for the isolated switched-mode converters are compared in Table 5.1.

5.2 BUCK-DERIVED ISOLATED CONVERTERS

Depending on the location at which the isolation transformer is inserted in the power stage of the basic buck converter, and on the type of isolation transformer configuration, several buck-derived converter topologies are possible. These topologies vary in complexity and features. In this section we will consider some of the more popular buck-derived converters: single-ended forward, half- and full-bridge, push-pull, and Weinberg converters. Other topologies are given as exercises at the end of this chapter.

ac Transformer Insertion

Let us consider isolating the input and output voltages of the buck converter by inserting an ac transformer. Figure 5.6(*a*) shows four places where physical transformer

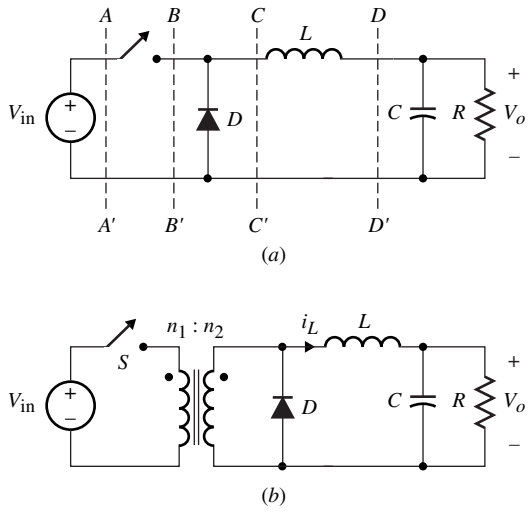


Figure 5.6 (*a*) Buck converter. (*b*) Isolated buck converter.

insertion is possible. Locations AA' and DD' are not possible since the transformer's primary and secondary voltages would be dc V_{in} and V_o, respectively. The obvious location is either BB' or CC' since the voltage at either location is an ac squarewave voltage.

It is clear that the isolated buck-derived converter of Fig. 5.6(*b*) will not function properly in steady state. This is because the average voltage across the transformer is positive (nonzero), which results in a continuous increase in the magnetization current that will eventually lead to transformer saturation. Let us further investigate the problem of transformer magnetizing inductance saturation.

When the switch is turned on at $t = 0$, the diode becomes reverse biased as shown in Fig. 5.7(*a*). The magnetizing and output inductor currents are given by

$$i_{Lm} = \frac{V_{\text{in}}}{L_m} t + I_{Lm}(0)$$

$$i_L(t) = \frac{n_1}{n_2} i_p = \frac{\dfrac{n_2}{n_1} V_{\text{in}} - V_o}{L} t + I_L(0)$$

where $I_L(0)$ and $I_{Lm}(0)$ are the initial output and magnetizing inductor currents, respectively.

At $t = DT$, S is switched off (Fig. 5.7(*b*)), and D turns on. Hence, the magnetizing current stays constant at $I_{Lm}(DT)$, which is given by

$$I_{Lm}(DT) = \frac{DT}{L_m} V_{\text{in}} + I_{Lm}(0)$$

The diode current is given by

$$i_D(t) = i_L(t) + I_{Lm}(DT)$$

The inductor current $i_L(t)$ for $t \geq DT$ is given by

$$i_L(t) = \frac{-V_o}{L}(t - DT) + I_L(DT)$$

where

$$I_L(DT) = \frac{\frac{n_1}{n_2}V_{\text{in}} - V_o}{L}DT + I_L(0)$$

At $t = T$, when the switch is turned on again, it causes i_{Lm} to increase starting at a higher initial value, $I_{Lm}(DT)$, as shown for three cycles in Fig. 5.7(c).

One way to avoid the problem of transformer saturation is to add another diode as shown in Fig. 5.8 to produce a negative voltage across the primary side when the switch is switched off. However, this converter as shown provides a path for the magnetizing current to reset to zero when the switch is open. As a result, a third winding, known as "catch" winding, is added to allow i_{Lm} to discharge to zero, preventing magnetic flux build-up from one cycle to the next. This converter is known as a single-ended forward converter, to be discussed in the next section.

The isolation of the buck-boost converter can be carried out in a similar manner. Figure 5.9(a) shows the buck-boost converter with a transformer insertion as shown in Fig. 5.9(b). Depending on the transformer windings, negative or positive output polarities can be obtained as shown in Fig. 5.9(b) and (c), respectively. Figure 5.9(c) is known as a single-ended flyback converter, which will be discussed later in the chapter.

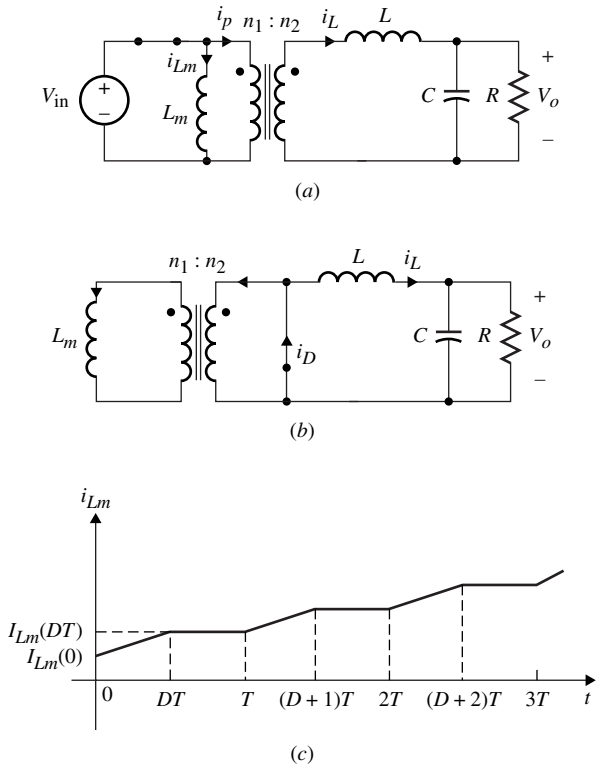


Figure 5.7 Equivalent circuit model. (a) Switch on. (b) Switch off. (c) Magnetizing inductor current.

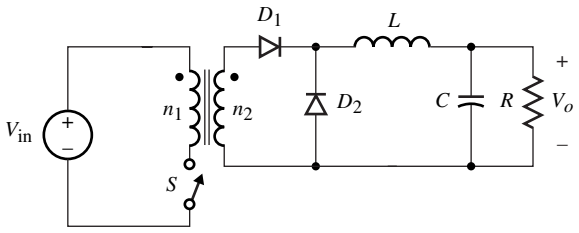


Figure 5.8 Isolated buck-derived converter known as a single-ended forward converter.

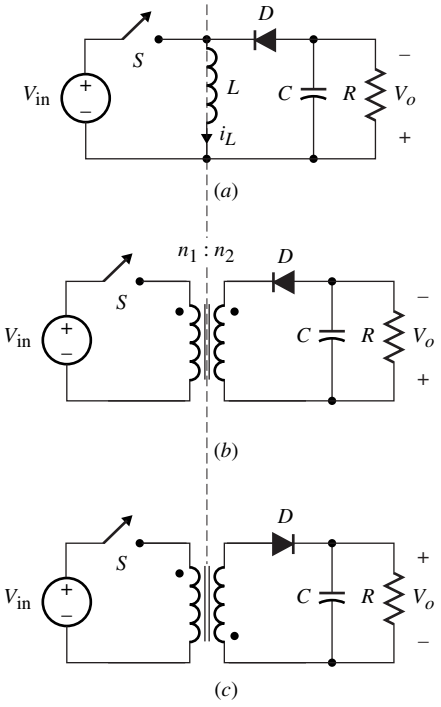


Figure 5.9 (*a*) Buck-boost converter. (*b*) Isolated converter with negative output voltage. (*c*) Isolated converter with positive output voltage.

5.2.1 Single-Ended Forward Converter

In this section we will analyze Fig. 5.8, which shows the simplest isolated dc-to-dc converter utilizing one switch and two diodes. As stated earlier, this circuit is commonly referred to as a *forward converter.* It can be shown that the design of Fig. 5.8 will not work properly since its magnetizing current will not be allowed to reset to zero, causing the magnetizing current to continuously increase linearly until it finally saturates the core. A more practical forward converter must include a transformer core-resetting circuit as shown in Fig. 5.10(*a*). The additional winding n_r is known as *tertiary winding.* Figure 5.10(*b*) and (*c*) shows two alternative ways to draw Fig. 5.10(*a*).

To allow for a zero average voltage across the transformer primary winding, the maximum duty cycle is 50%. However, if the winding ratio $n_r/n_1 < 1$, then it is possible to have a duty cycle that exceeds 50%. This will result in a voltage stress across the switch that exceeds $2V_{in}$.

For illustration purposes, we will analyze the converters of Figs. 5.8 and 5.10(*a*). If an ideal transformer is assumed in Fig. 5.8, then the steady state is quite simple. Assume the switch is turned on for the period DT and off for the period $(1-D)T$, resulting in the two modes of operation shown in Fig. 5.11(*a*) and (*b*), respectively.

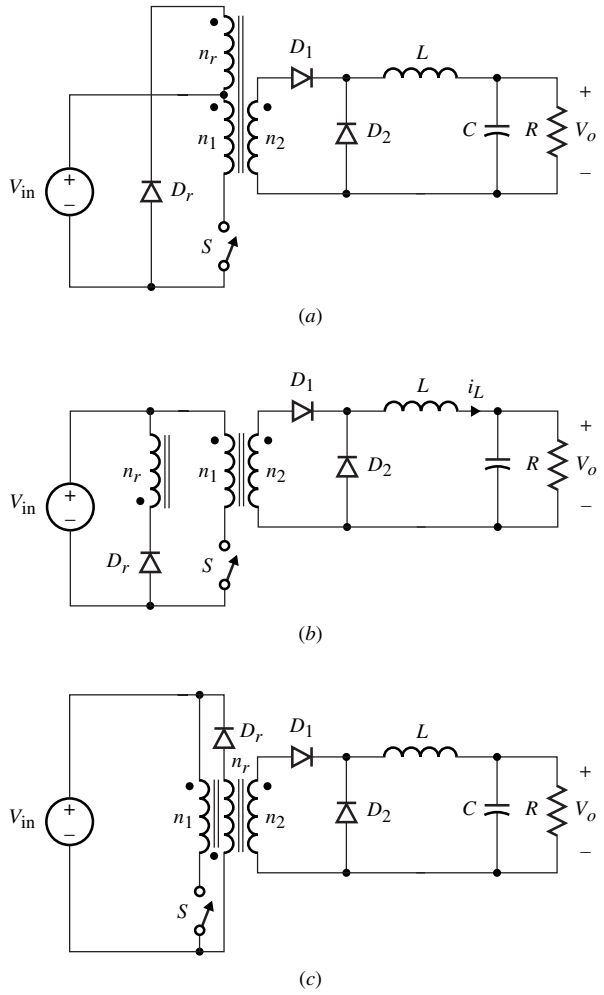


Figure 5.10 Three ways to draw a single-ended forward converter with a core reset circuit.

When the switch is turned on initially at $t = 0$, the initial inductor current is $I_L(0)$, and v_L is given by

$$v_L = \frac{n_2}{n_1} V_{\text{in}} - V_o$$

$$= L\frac{di_L}{dt}$$

The inductor current is given by

$$i_L(t) = \frac{\frac{n_2}{n_1} V_{\text{in}} - V_o}{L} t + I_L(0) \qquad 0 \le t < DT$$

At $t = DT$, the switch turns off, forcing D_1 to reverse-bias and D_2 to become forward biased, resulting in the inductor current given by

$$i_L(t) = \frac{-V_o}{L}(t - DT) + I_L(DT)$$

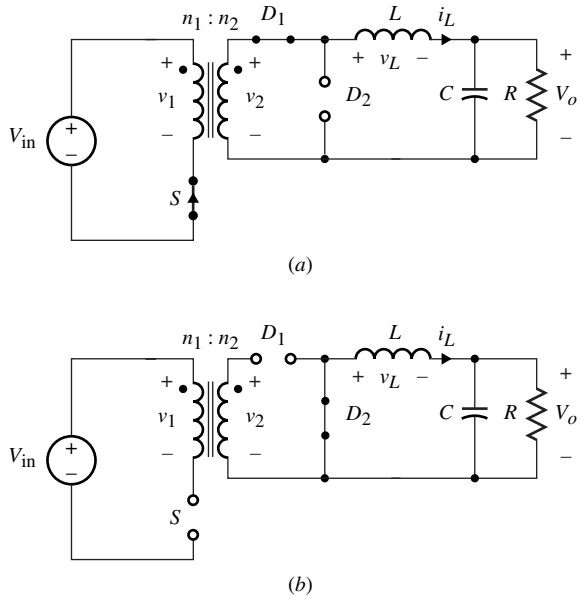


Figure 5.11 Modes of operation. (*a*) Mode 1: *S* is on. (*b*) Mode 2: *S* is off.

where $I_L(DT)$ is the inductor current at $t = DT$, when the switch is turned off. From the above equations, we obtain the following voltage gain relation:

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1} D$$

Sketches of the waveforms for v_1, v_2, v_L, i_L, i_{D1}, and i_{D2} are shown in Fig. 5.12.

For proper operation that will allow the inductor current to reach steady state, the relation $(n_2/n_1)V_{\text{in}} > V_o$ must hold, which provides a step-down operation. The capacitor voltage ripple is similar to that for the nonisolated buck converter.

Next we carry out the analysis by assuming the transformer has a finite magnetizing inductance, L_m, as shown in the equivalent circuit given in Fig. 5.13. With careful investigation of the circuit, it is clear that the magnetizing current $i_m(t)$ has no place to discharge its value when the switch is off. This will cause the converter to fail. As a result, a core-resetting mechanism as mentioned above must be used. Figure 5.14 shows the equivalent circuit for the forward converter by including the core reset circuit given in Fig. 5.10(*b*).

The operation of this converter can be easily explained by assuming that before the switch is turned on again in a new cycle, the magnetizing current, i_m, has reached zero, i.e., the transformer core is being reset. The energy is delivered to the load during the period the switch is on, and the core resetting takes place during the *off* time. It will be shown that $D \le 50\%$ for $n_r \ge n_1$ to allow time for the magnetic core flux to reset during the *off* switch time. In steady state, this converter has three modes of operation, as follows.

The first mode starts when *S* is turned on at $t = 0$, causing voltage across the primary equal to V_{in}. This will force D_1 to turn on and D_2 to reverse-bias. Since the reset winding has the opposite polarity of the primary, the diode D_r becomes reverse biased as shown in Fig. 5.15(*a*).

From Fig. 5.15(*a*), the following voltage equations are obtained:

$$v_L = v_2 - V_o,\ v_1 = V_{\text{in}},\ v_2 = \frac{n_2}{n_1} v_1,\ v_r = \frac{n_r}{n_1} V_{\text{in}},\ v_{Dr} = \left(1 + \frac{n_r}{n_1}\right) V_{\text{in}} \qquad (5.1)$$

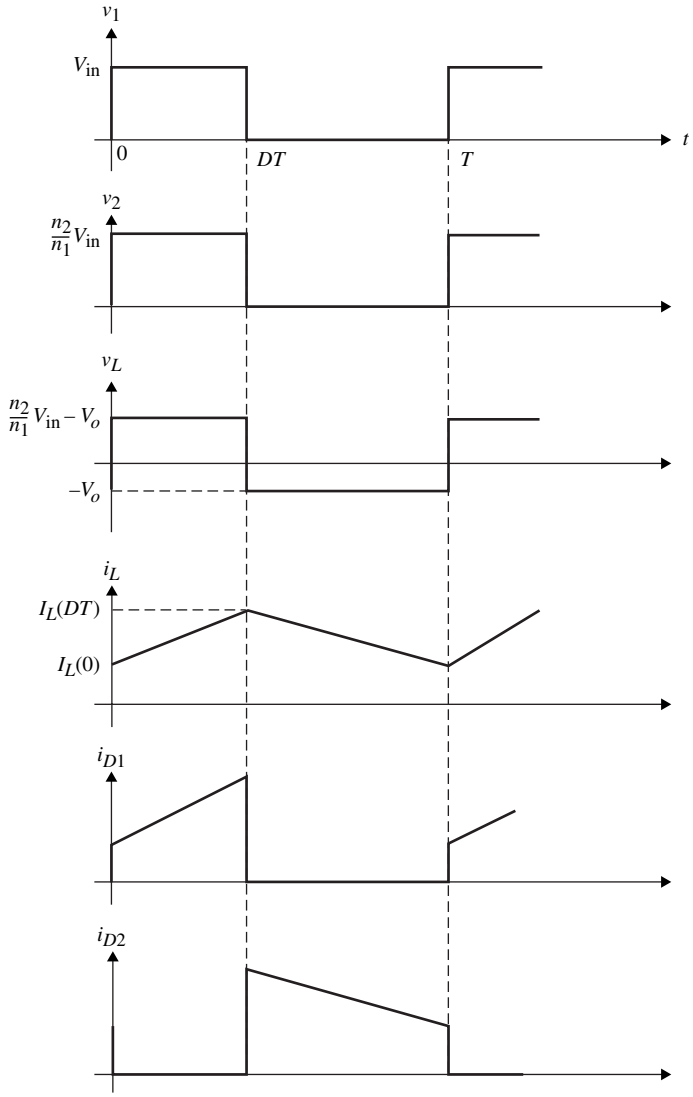


Figure 5.12 Current and voltage waveforms for the forward converter.

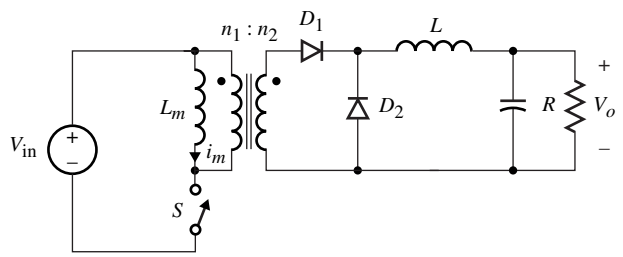


Figure 5.13 Single-ended forward converter with the magnetizing inductance.

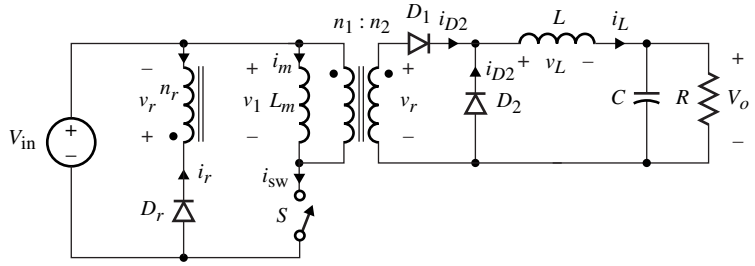


Figure 5.14 Forward converter with core reset circuit n_r–D_r, including the magnetizing inductance.

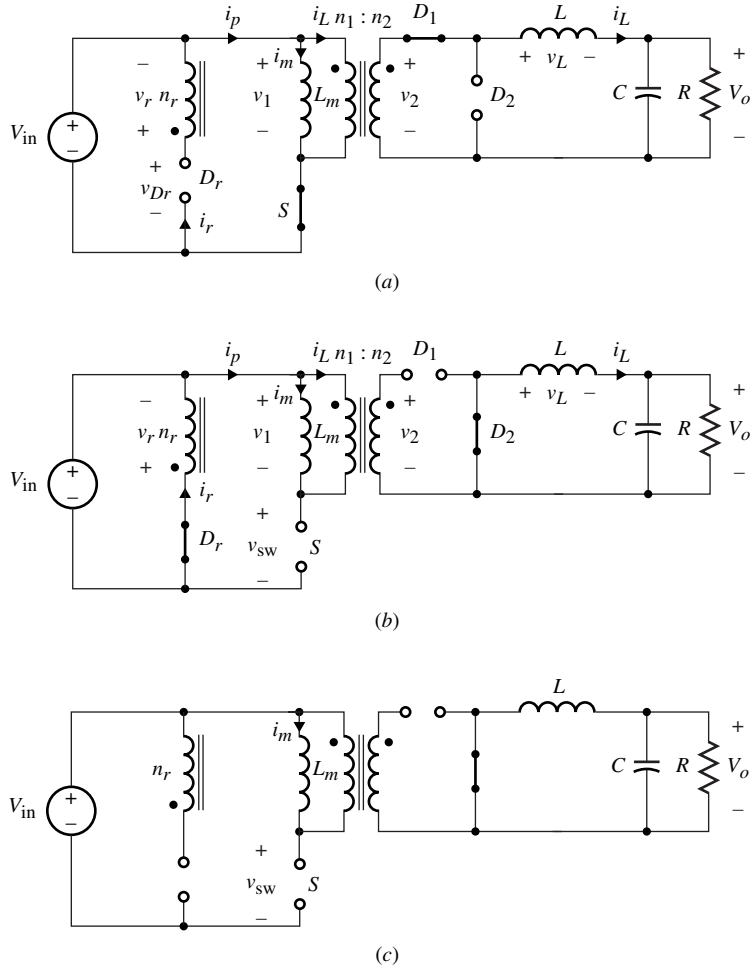


Figure 5.15 Modes of operation. (*a*) Mode 1: $0 \le t < DT$. (*b*) Mode 2: $DT < t < D_1 T$. (*c*) Mode 3: $D_1 T \le t < T$.

The current equations are given by

$$L_m \frac{di_m}{dt} = V_{\text{in}} \tag{5.2a}$$

$$L \frac{di_L}{dt} = \frac{n_2}{n_1} V_{\text{in}} - V_o \tag{5.2b}$$

$$i_r = 0 \tag{5.2c}$$

$$i_1 = \frac{n_2}{n_1} i_L \tag{5.2d}$$

$$i_p = i_m + i_L \tag{5.2e}$$

From Eqs. (5.2*a*) and (5.2*b*), the following relations are obtained:

$$i_m(t) = \frac{V_{\text{in}}}{L_m} t \tag{5.3}$$

$$i_L(t) = \frac{\frac{n_2}{n_1} V_{\text{in}} - V_o}{L} t + I_L(0) \tag{5.4}$$

where $I_L(0)$ is the initial output inductor current and $I_m(0) = 0$ since the core has been reset prior to turning on the switch. Since $L_m >> L$, the slope of the magnetizing current is much smaller than the slope of i_L, as shown in Fig. 5.16. At $t = DT$, the switch is turned off and the circuit enters mode 2, shown in Fig. 5.15(*b*). At the instant *S* opens, the transformer primary current, i_p, becomes zero, turning off D_1 and forcing i_L to go through D_2. At this point, i_m now is forced to flow in the n_1 winding, which forces D_r to turn on to carry the reflected current through n_r.

The voltage equations in this mode are given by

$$v_L = -V_o\,,\; v_r = -V_{\text{in}}\,,\; v_1 = -\frac{n_1}{n_r} V_{\text{in}}\,,\; v_2 = \frac{n_2}{n_1} v_1,\; V_{Dr} = 0\,,\; v_{\text{sw}} = \left(1 + \frac{n_r}{n_1}\right) V_{\text{in}} \tag{5.5}$$

and the current equations are as follows:

$$L_m \frac{di_m}{dt} = -\frac{n_1}{n_r} V_{\text{in}} \tag{5.6a}$$

$$L \frac{di_L}{dt} = -V_o \tag{5.6b}$$

$$i_r = \frac{n_1}{n_r} i_1 \tag{5.6c}$$

$$i_m = -i_L \tag{5.6d}$$

The waveforms are shown in Fig. 5.16. At $t = D_1 T$, the magnetizing inductor current becomes zero, since it represents the smaller portion of i_p. The magnetizing and inductor currents in this time interval are given by

$$i_m(t) = -\frac{n_1}{n_r} \frac{V_{\text{in}}(t - DT)}{L_m} + I_m(DT) \tag{5.7}$$

$$i_L(t) = -\frac{V_o}{L}(t - DT) + I_L(DT) \tag{5.8}$$

where $I_m(DT) = (V_{\text{in}}/L_m)DT$. Setting Eq. (5.7) to zero at $t = D_1$, we obtain

$$D_1 = \left(1 + \frac{n_r}{n_1}\right) D \tag{5.9}$$

At $t = D_1 T$, $i_m = 0$, causing D_r to become reverse biased, as shown in Fig. 5.15(*c*).

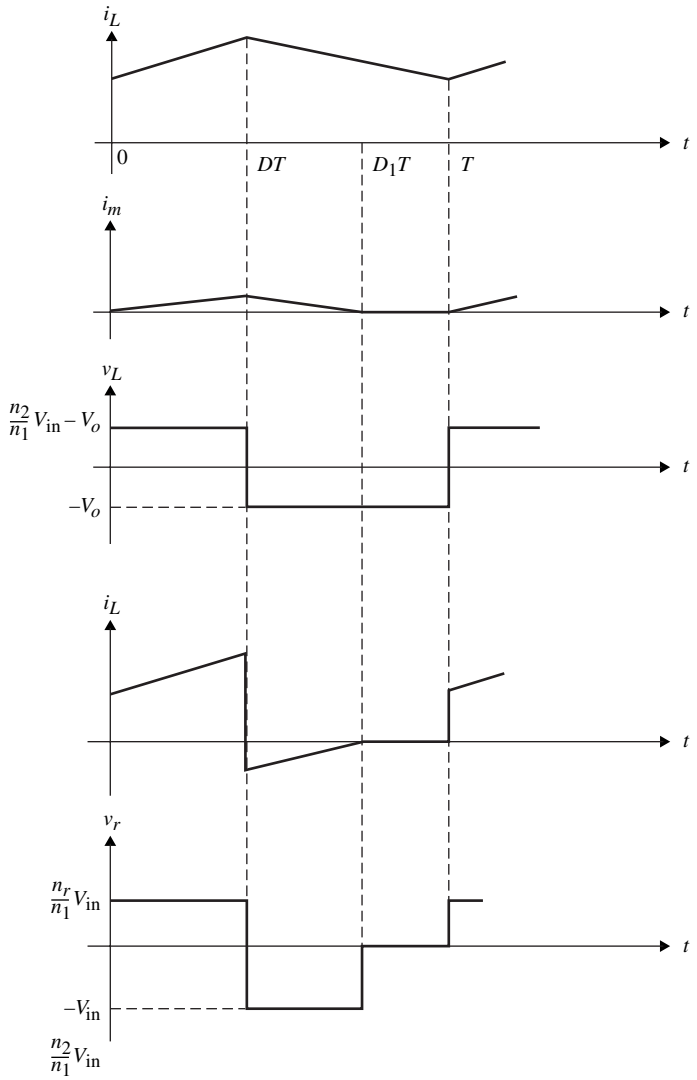


Figure 5.16 Typical voltage and current waveforms.

The voltage and current equations are given by

$$v_L = -V_o\,,\ v_r = v_1 = v_2 = 0\,,\ v_{Dr} = V_{\text{in}}\,,\ v_{\text{sw}} = V_{\text{in}}$$

$$i_m = i_r = i_p = i_L = 0\,,\ \text{and } i_L(t) \text{ is the same as given in Eq. (5.8).}$$

For the core to be fully magnetized, i_m must reach zero; therefore, D_1 must not be greater than 1.

$$D_1 \le 1$$

Hence, from Eq. (5.9) we restrict D by the following relation:

$$D \le \frac{1}{1 + \dfrac{n_r}{n_1}} = \frac{n_1}{n_1 + n_r}$$

The maximum duty cycle of 50% occurs when $n_r = n_1$.

EXAMPLE 5.2

Consider the forward converter of Fig. 5.14 with an input voltage of 50 V, an output voltage of 35 V, and $n_1/n_2 = 1$ and $n_1/n_r = 0.25$. With a frequency of 35 kHz, an inductance of 180 μH, and a minimum inductor current of 1.1 A, calculate the duty cycle and the maximum inductor current in this converter.

SOLUTION The duty cycle is given in the following equation:

$$D = \frac{V_o}{V_{\text{in}}} = \frac{35\text{ V}}{50\text{ V}} = 0.7$$

$$T = \frac{1}{f} = \frac{1}{35\text{ kHz}} = 2.86 \times 10^{-5}\text{s}$$

Calculating for the maximum inductor current,

$$\begin{aligned} i_{L,\max} &= \frac{V_{\text{in}} - V_o}{L} DT + i_{L,\min} \\ &= \frac{50\text{ V} - 35\text{ V}}{180\ \mu\text{H}}(0.7)(2.86 \times 10^{-5}) + 1.1 \\ &= 2.77\text{ A} \end{aligned}$$

EXERCISE 5.1

Figure E5.1 shows a two-switch forward converter.

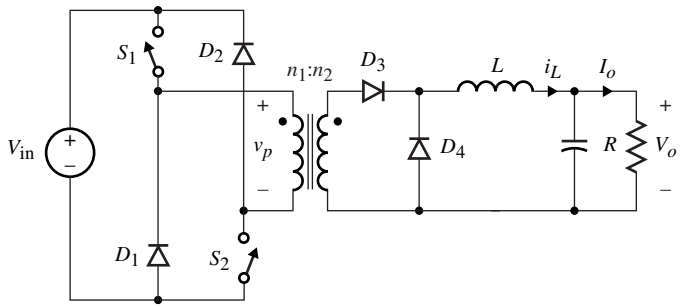


Figure E5.1 Two-switch forward converter.

(a) Show that the voltage gain expression is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1} D$$

S_1 and S_2 are switched simultaneously.

(b) Find the critical inductor value (L_{crit}) to maintain a continuous conduction mode of operation. Assume $n_1 = n_2 = 1$, $V_{\text{in}} = 80$ V, $V_o = 45$ V @ $I_o = 5$ A, $f_s = 50$ kHz.

(c) Compare the one-switch, single-ended topology with this two-switch topology.

ANSWER **(b)** 39.4 μH

EXERCISE 5.2

Find the rms current values for diodes D_3 and D_4 in Fig. E5.1 using the values of part (*b*) of Exercise 5.1 with $L = 10L_{\text{crit}}$.

ANSWER 3.76 A, 3.31 A

EXERCISE 5.3

Determine the efficiency of the converter described in Exercise 5.1 by assuming that the output rectifier diodes have a 1 V forward voltage drop and a 1.5 Ω conduction resistance.

ANSWER 84.1%

EXERCISE 5.4

Determine the rms value of the inductor current i_L for Example 5.2.

ANSWER 1.99 A

5.2.2 Half-Bridge Converter

Another way to avoid the transformer saturation problem is to use half- and full-bridge converter topologies to generate symmetrical ac waveforms at the primary side of the transformer. In this way the core flux is excited bidirectionally, resulting in a better utilization of the core, which in turn results in an increased power rating.

Figure 5.17(*a*) shows the circuit topologies for the half-bridge converter with the center-tap output rectifier configuration. The filtering capacitors are relatively large and used as voltage dividers, resulting in a $V_{\text{in}}/2$ applied voltage across each primary winding. As stated before, in the half-bridge converter, S_1 and S_2 are switched on and off in complementary fashion but with equal conduction periods. Since the input voltage is not allowed to be shorted, S_1 and S_2 are normally designed such that there exists a dead time during which both switches are off. This results in a duty ratio less than 50%. Key current and voltage waveforms are shown in Fig. 5.17(*b*).

The voltage gain for the half-bridge converter is the same as the gain for the push-pull converter, to be discussed in a later section. The filtering capacitors C_1 and C_2 are used to divide the input voltage, so each has $V_{\text{in}}/2$. Unlike the push-pull converter, the maximum blocking voltage for each switch of the half-bridge converter is V_{in}, rather than $2V_{\text{in}}$.

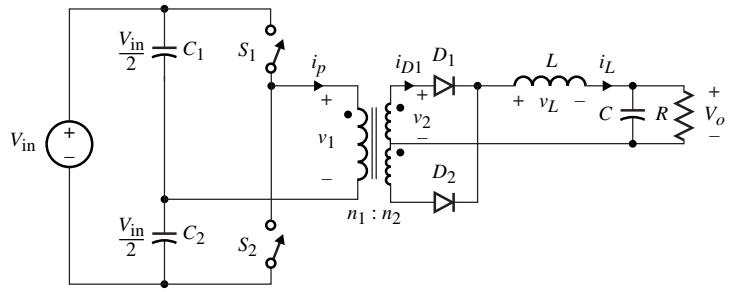
Finally, the switches S_1 and S_2 are implemented using bidirectional semiconductor devices (i.e., MOSFETs with anti-parallel diodes) to provide conduction paths for the inductor leakage currents that exist due to the nonideal transformers.

EXERCISE 5.5

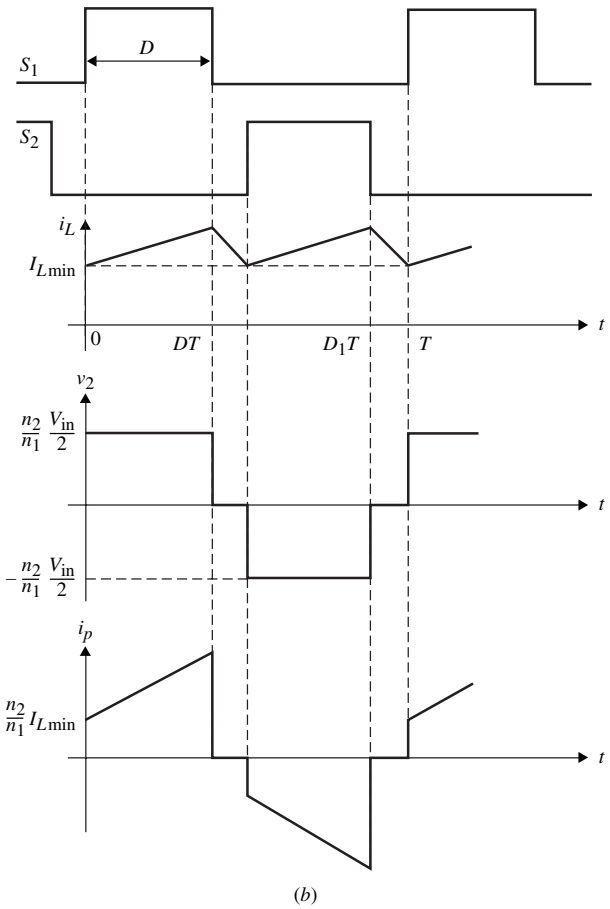
(a) Show that the voltage gain for the half-bridge converter of Fig. 5.17(*a*) is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{2n_1}D$$

(b) Find the expression for the maximum diode current.



(*a*)



(*b*)

Figure 5.17 (*a*) Half-bridge buck-derived converter. (*b*) Current and voltage waveforms.

***ANSWER* (b)** $I_o + \dfrac{V_o(1-D)T_s}{L}$

EXERCISE 5.6

Determine the average load current and the rms inductor current for the half-bridge converter of Fig. 5.17(*a*) with the following specifications:

$$V_{\text{in}} = 135 \text{ V}, \; V_o = 12 \text{ V}, \; f_s = 100 \text{ kHz}, \; R = 2 \; \Omega,$$

$$n_2 = 13, \; n_1 = 39, \; L = 20 \; \mu\text{H}$$

ANSWER 6 A, 6.01 A

5.2.3 Full-Bridge Converter

Figure 5.18 shows the buck-derived full-bridge converter with a full-wave center-tap output transformer.

We must note that the push-pull, half-bridge, and full-bridge converters can use the full-bridge rectifier at the output side. Unlike the half-bridge converter, the full-bridge converter is used in high-input-voltage applications, since the power switching devices are required to block only V_{in}.

EXAMPLE 5.3

Design the full-bridge dc-dc converter with the center-tap output transformer as shown in Fig. 5.18 with the following specifications: $V_{\text{in}} = 480$ V, $V_o = 600$ V @ $I_o = 10$ A, $f_s = 50$ kHz.

SOLUTION The load resistor is obtained from $R = V_o / I_o = 600/10 = 60 \; \Omega$. If we choose $n_2 = 2n_1$, then

$$D = \frac{V_o}{V_{\text{in}}} \frac{n_1}{n_2} = \frac{600}{480} \frac{1}{2} = 0.625$$

Since L_{crit} for the buck converter is expressed as

$$L_{\text{crit}} = \left(\frac{1 - D}{4}\right) RT$$

we have $L_{\text{crit}} = 112.5 \; \mu$H. Choose $L > 10 L_{\text{crit}} = 1.125$ mH. If output ripple is less than 1%, according to

$$\frac{\Delta V_o}{V_o} = \frac{1 - D}{8LC(2f)^2}$$

C can be determined as $C = 0.42 \; \mu$F. We can choose $C = 10 \; \mu$F.

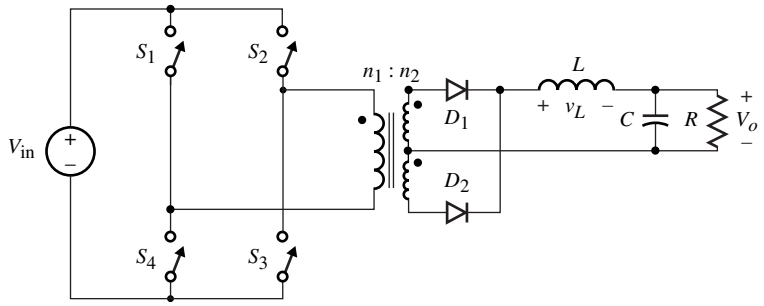


Figure 5.18 Full-bridge converter.

5.2.4 Push-Pull Converter

The circuit configuration for the push-pull converter is shown in Fig. 5.19(*a*). The circuit uses two active switches. It uses the transformer for voltage scaling and electrical isolation, and the output inductor is used for energy storage. Hence, unlike the design of the transformer for the single-ended converter, where care must be taken in selecting the core material and geometry to design for proper magnetizing inductance, in the push-pull the transformer is used as an ideal element. Since S_1 and S_2 share the current, the push-pull converter is used for higher-power applications compared to the single-ended converters. Figure 5.19(*b*) illustrates the switching waveforms for S_1 and S_2 with a dead time during which both switches are open.

During this dead time, the load current is carried by the two output diodes, D_1 and D_2. The maximum duty cycle for both switches is 0.5. As can be noticed, the switching frequency of the converter is twice the switching frequency of each switch acting alone. The converter's basic operation is straightforward and similar to the analysis of the half-bridge converter. When S_1 is on, the possible primary voltage causes D_1 to conduct and D_2 to turn off, resulting in the equivalent circuit shown in Fig. 5.20(*a*).

The converter voltages are given by

$$\begin{aligned} v_{s1} &= v_{s2} = \frac{n_2}{n_1} V_{\text{in}} \\ v_{p1} &= v_{p2} = +V_{\text{in}} \\ v_L &= \frac{n_2}{n_1} V_{\text{in}} - V_o \end{aligned} \tag{5.10}$$

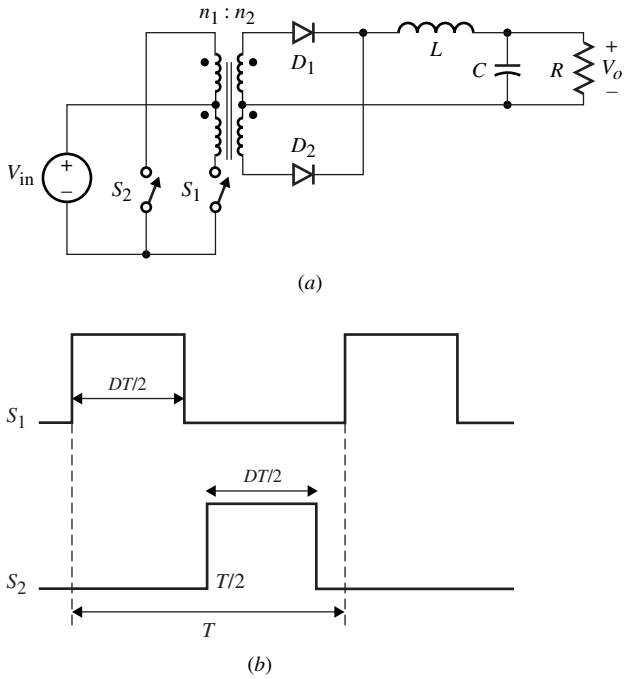


Figure 5.19 (*a*) Push-pull converter. (*b*) Switching waveforms for S_1 and S_2.

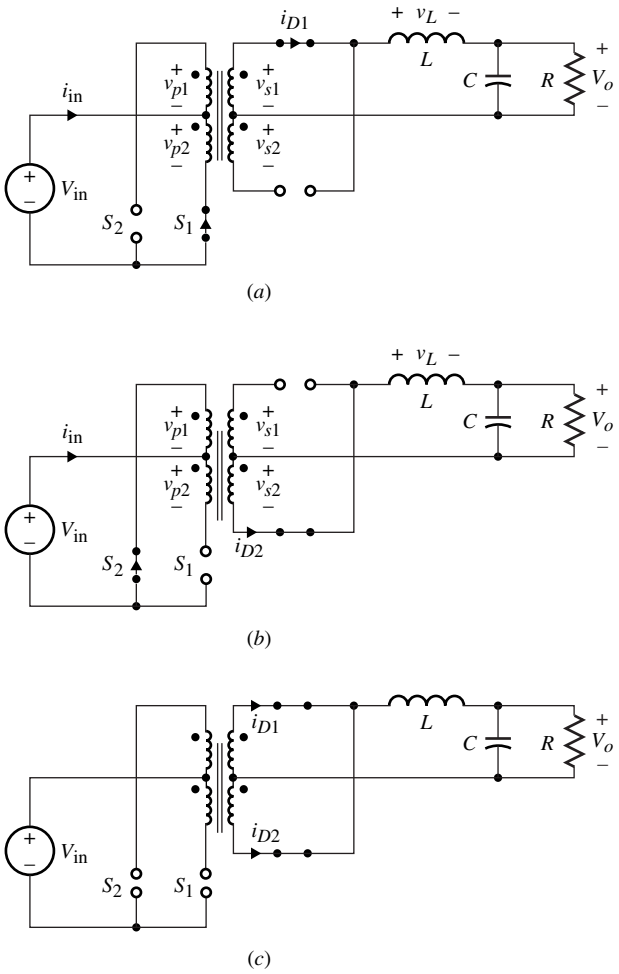


Figure 5.20 (*a*) Equivalent circuit when S_1 is on and S_2 is off. (*b*) Equivalent circuit when S_1 is off and S_2 is on. (*c*) Equivalent circuit when S_1 is off and S_2 is off.

This circuit is equivalent to a buck converter with a dc input of $(n_2/n_1)V_{\text{in}}$. All voltage and current waveforms are similar to those for the buck converter.

Similarly, when S_1 is off and S_2 is on, the equivalent circuit is shown in Fig. 5.20(*b*). The voltages are given by

$$v_{s1} = v_{s2} = -\frac{n_2}{n_1}V_{\text{in}}$$
$$v_{p1} = v_{p2} = -V_{\text{in}} \tag{5.11}$$

The voltage across the inductor is given by

$$v_L = -v_{s2} - V_o = \frac{n_2}{n_1}V_{\text{in}} - V_o \tag{5.12}$$

Notice that for both modes, whether S_1 or S_2 is on, the circuit is similar to the buck converter when the main switch is on.

Finally, consider the case when both S_1 and S_2 are off. The equivalent circuit is shown in Fig. 5.20(c). The voltages v_{s1} and v_{s2} are both zero, and the inductor voltage is $-V_o$. Hence, the inductor current starts discharging with a slope of $-V_o/L$. This mode is similar to the buck converter when the main switch is off. Therefore, the voltage gain of the push-pull converter is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1}D \tag{5.13}$$

where D is the duty cycle for either switch, which ranges between 0 and 0.5.

We observe that because of the presence of the transformer, each of S_1 and S_2 should be able to withstand a reverse voltage of at least $2V_{\text{in}}$. Also, a peak reverse diode voltage for each of D_1 and D_2 is $2(n_2/n_1)V_{\text{in}}$. One disadvantage of the push-pull converter is the imbalance of the voltages applied across the transformer primaries, resulting in unequal switch current. This in turn results in a nonzero magnetizing inductance current at the end of each switching cycle. This eventually will lead to a transformer saturation problem. This problem is caused by a mismatch in the transistor characteristics, such as switching times and voltage drops. To avoid this problem, push-pull converters are designed with not only a voltage control loop (duty cycle control), but also a current loop (current-programmed control) that prevents the transformer from reaching saturation.

Key waveforms for the push-pull converter are shown in Fig. 5.21 with no magnetizing inductance included.

EXAMPLE 5.4

Another boost-derived converter that uses an isolation transformer is the push-pull arrangement shown in Fig. 5.22(a).

The input inductor, L, is very large so that the input current, I_{in}, is assumed constant. These types of converters are useful in high-output-voltage applications. Since I_{in} is continuous, there should be an overlap in the conduction times of S_1 and S_2 as shown in the switching waveforms in Fig. 5.19(b), where δ is the overlapping conduction time. Derive the voltage gain expression for the converter and compare it with the push-pull converter shown earlier. Figure 5.22(c) shows the waveforms for the primary voltage and input current.

SOLUTION Let us assume the first mode begins at $t = 0$, when both S_1 and S_2 are on, resulting in the transformer primary voltage equaling zero since D_1 and D_2 are off. The voltage across L equals the input voltage,

$$\begin{aligned} v_L &= V_{\text{in}} \\ &= L\frac{di_{\text{in}}}{dt} \end{aligned}$$

while i_{in} is given by

$$i_{\text{in}}(t) = \frac{V_{\text{in}}}{L}t + I_{\text{in}}(0)$$

$I_{\text{in}}(0)$ is the initial inductor current value in L.

At $t = t_1$, S_2 is turned off, forcing D_2 to conduct. The voltage across the inductor is given by

$$\begin{aligned} v_L &= V_{\text{in}} - \frac{n_1}{n_2}V_o \\ &= L\frac{di_{\text{in}}}{dt} \end{aligned}$$

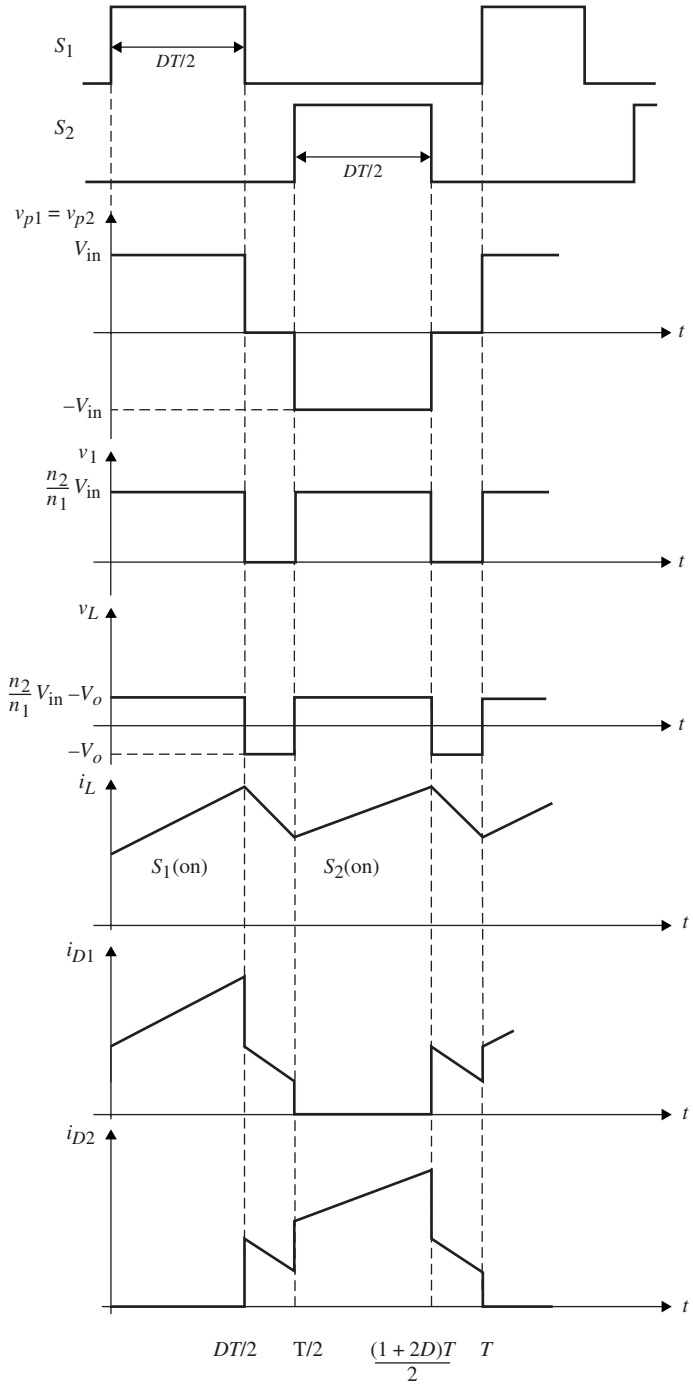


Figure 5.21 Voltage and current waveforms for the push-pull converter of Fig. 5.19(*a*).

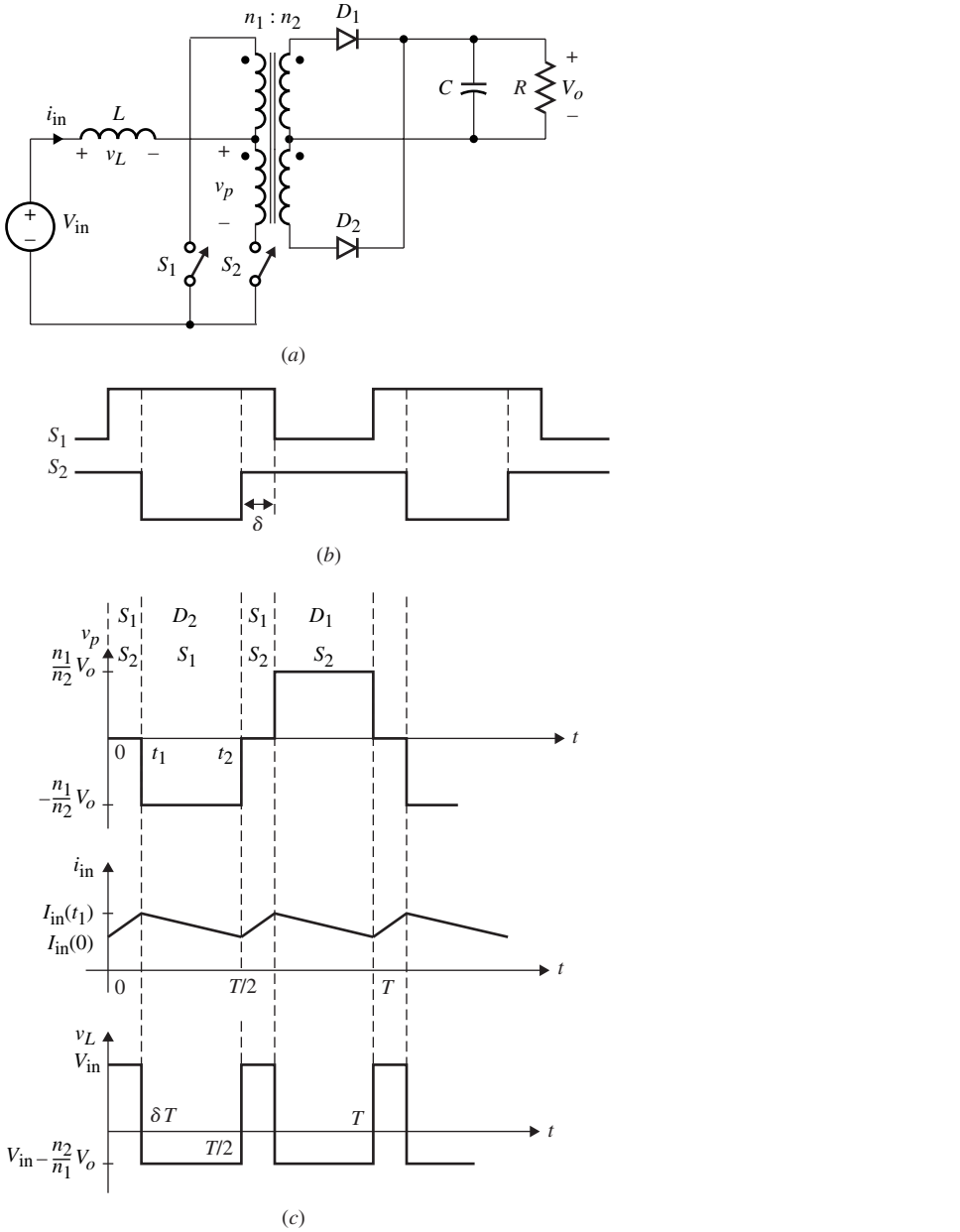


Figure 5.22 (*a*) Current-fed push-pull converter. (*b*) Switching waveforms. (*c*) Converter waveforms.

The inductor current is given by

$$i_{in}(t) = \frac{V_{in} - \dfrac{n_1}{n_2} V_o}{L}(t - t_1) + I_{in}(t_1)$$

The inductor current discharges at a rate of $(V_{in} - (n_1/n_2)V_o)/L$. At $t = t_2$, S_2 turns on again, resulting in $v_p = 0$. The next two modes are similar to the first two modes, except that when S_2 is on, D_1 conducts.

The gain equation is obtained by applying the volt-second balance to L as follows:

$$V_{\text{in}}t_1 = -\left(V_{\text{in}} - \frac{n_1}{n_2}V_o\right)(t_2 - t_1)$$

Since $t_1 = \delta T$ and $t_2 = T/2$,

$$V_{\text{in}}\delta = \left(\frac{n_1}{n_2}V_o - V_{\text{in}}\right)\left(\frac{1}{2} - \delta\right)$$

Solving for V_o/V_{in}, we obtain

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1}\frac{1}{1-2\delta}$$

If we let DT represent the *on* time, $(1-D)T$ is the *off* time of S_1; then we have

$$\delta = D - \frac{1}{2}$$

Hence, the gain is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1}\frac{1}{2(1-D)}$$

EXERCISE 5.7

Calculate the diode rms and average current values for the push-pull converter of Fig. 5.19(*a*) whose current i_L is given in Fig. E5.7. Determine the average output power if the load resistance is 10 Ω.

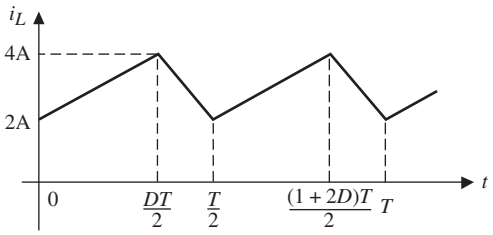


Figure E5.7 Waveform for i_L of Fig. 5.19(*a*).

ANSWER $\sqrt{6D + \frac{13}{4}}$ A, $\frac{3}{4}(1+2D)$, 90 W

5.3 BOOST-DERIVED ISOLATED CONVERTERS

In this section we will discuss several well-known boost-derived isolated converters. All of these converters have the same function of the basic boost converter discussed in Chapter 4. We begin with the simplest: the single-ended one-switch boost-derived converter known as the *flyback converter.*

5.3.1 Single-Ended Flyback Converter

The circuit topology for the flyback converter is shown in Fig. 5.23(*a*). This converter is one of the most common isolated switch-mode converters.

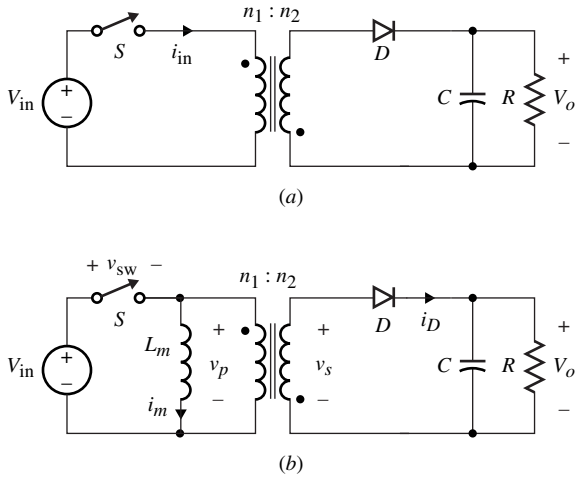


Figure 5.23 (*a*) Single-ended basic flyback converter. (*b*) Flyback converter with magnetizing inductor.

The transformer shown in this topology serves as a step-up/step-down to the input voltage, reverses output voltage polarity, provides electrical isolation, and provides energy storage during the operation. Since all the energy obtained from the source is first stored in the transformer and then passed on to the load, this converter is also known as an energy storage converter. Commercial flyback converters are normally designed with several multicoil output transformers. During the turn-on period, energy is stored in the magnetic inductor and transferred to the output side during the turn-off period. In order for the diode to conduct only during the *off* period in which energy is transferred to the output, the polarities of the transformer windings are reversed, as shown in the figure. One popular application for the flyback converter is in television screens, in which high output voltage is required. This can be obtained by using a high transformer turn ratio, n_2/n_1. Unlike the forward converter, the flyback converter doesn't need an output inductor; it uses only one diode and does not suffer from a core saturation problem. When operated in dcm, it uses a relatively small, magnetizing inductance. To understand the role of the magnetizing inductance, we replace the transformer by a simple model that includes the magnetizing inductor, as shown in Fig. 5.23(*b*).

Typical waveforms for the flyback converter of Fig. 5.23(*b*) operating in the continuous conduction mode are shown in Fig. 5.24. When the transistor is turned on, the primary voltage v_p becomes equal to the source voltage V_{in}, and the diode D is turned off by the negative polarity of $(n_2/n_1)V_{in} + V_o$. The magnetizing inductance, L_m, starts charging linearly with slope V_{in}/L_m. Note that this mode of operation is like the boost converter, in which the inductor L stores energy during the *on* time. When S is turned off, the diode is forced to carry the magnetizing inductor current through the secondary winding. The drawback of this topology is the transformer's primary-side leakage inductance, whose energy must be dissipated when the transistor is turned off. For this reason, in order to reduce the stress on the switching transistor, a snubber circuit is normally added.

The analysis of this circuit consists of two modes of operation as follows.

Mode 1 (S is turned on at $t = 0$ and D is off). The *on*-state equivalent circuit model is shown in Fig. 5.25(*a*). The voltage across L_m is V_{in}, yielding the following equation for $i_m(t)$:

$$i_m(t) = \frac{V_{in}}{L_m}t + I_m(0) \tag{5.14}$$

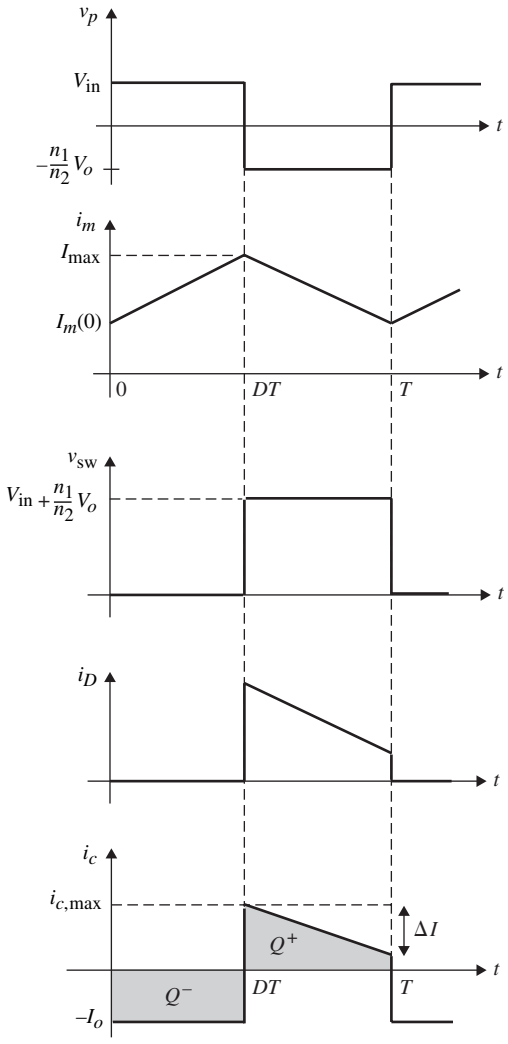


Figure 5.24 Current and voltage waveforms for the flyback converter.

where $I_m(0)$ is the initial value of the magnetizing current when the transistor is turned on. From this equation, we notice that the inductor current, i_m, will linearly charge to $t = DT$ when the transistor is turned off to enter mode 2.

Mode 2 (S is turned off and D is on). This mode of operation starts at $t = DT$, when the transistor is turned off. To maintain the continuity of i_m, the diode D turns on. The equivalent circuit model is shown in Fig. 5.25(*b*).

The voltage across the magnetizing inductance is nV_o, where n is n_1/n_2. In terms of i_m we have

$$v_p = -nV_o = L_m \frac{di_m}{dt}$$

Integrating this equation from DT to t, we obtain

$$i_m(t) = \frac{-V_o n}{L_m}(t - DT) + I_m(DT) \tag{5.15}$$

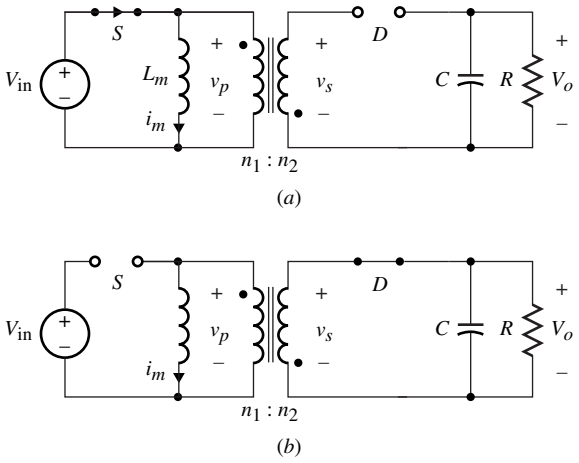


Figure 5.25 Modes of operation. (*a*) Mode 1: *S* is on and *D* is off. (*b*) Mode 2: *S* is off and *D* is on.

where $I_m(DT)$ is the magnetizing current value at $t = DT$, when the diode D starts conducting. Evaluating Eq. (5.15) at $t = DT$ and at $t = T$, respectively, and using $i_m(T) = i_m(0)$, we obtain the following relations:

$$I_m(DT) - I_m(0) = \frac{nV_o}{L_m}(1-D)T \tag{5.16a}$$

$$I_m(DT) - I_m(0) = \frac{V_{\text{in}}}{L_{\text{m}}}DT \tag{5.16b}$$

Equating Eqs. (5.16*a*) and (5.16*b*), we obtain the following conversion ratio:

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{n(1-D)} \tag{5.17}$$

This gain equation is similar to the buck-boost converter gain when $n = 1$. All relevant current and voltage waveforms are shown in Fig. 5.24. The average output current is the same as the average diode current, which is given

$$I_o = \frac{n(I_m(DT) + I_m(0))}{2}(1-D)$$

and the average input current is given by

$$I_{\text{in}} = \frac{I_m(DT) + I_m(0)}{2}D$$

Hence, the current conversion ratio is given by

$$\frac{I_o}{I_{\text{in}}} = \frac{n(1-D)}{D} \tag{5.18}$$

This equation can also be obtained by equating the average input and output powers by replacing $I_o = V_o/R$; thus we obtain the following relation:

$$I_m(DT) + I_m(0) = \frac{2V_o}{nR(1-D)}$$

From the above relation, we obtain the minimum and maximum current values of i_m as follows:

$$I_m(0) = \frac{V_{\text{in}}D}{n^2R(1-D)^2} - \frac{V_{\text{in}}DT}{2L_m} \tag{5.19a}$$

$$I_m(DT) = \frac{V_{\text{in}}D}{n^2R(1-D)^2} + \frac{V_{\text{in}}DT}{2L_m} \tag{5.19b}$$

When setting $I_m(0) = 0$, we obtain the critical value of the magnetizing inductance for the continuous conduction mode of operation.

$$L_{\text{crit}} = \frac{n^2(1-D)^2RT}{2} \tag{5.20}$$

If the inductor current is allowed to reach zero, i.e., $L_m < L_{\text{crit}}$, then the converter will operate in dcm and the core becomes fully demagnetized in each cycle.

EXAMPLE 5.5

Sketch the waveform for i_c and determine the expression for the output voltage ripple for the flyback converter of Fig. 5.23(*b*).

SOLUTION The capacitor current equals the ac ripple in the diode current, i_D. So i_c is the same as the diode current minus the average output current:

$$i_c = i_D - I_o$$

The current i_c is obtained by simply shifting i_D down by I_o as shown in Fig. 5.24. It is clear that the waveform is similar to the buck-boost capacitor current. The total charge, ΔQ, during the DT interval is given by

$$\Delta Q^- = (DT)(I_o)$$

$$C\Delta V_c = (DT)(I_o)$$

$$\therefore \Delta V_c = \frac{DTI_o}{C}$$

$$\frac{\Delta V_c}{V_o} = \frac{D}{RCf}$$

The peak capacitor current is given by

$$I_{c,\max} = I_{Lm}(DT) - I_o$$

Substitute for $I_{Lm}(DT)$ from Eq. (5.19*b*) and simplify to obtain

$$I_{c,\max} = I_o\left[\frac{1-n(1-D)}{n(1-D)} + \frac{nTR(1-D)}{2L_m}\right]$$

EXERCISE 5.8

Determine the voltage gain V_o/V_{in} for the flyback converter operating in the discontinuous conduction mode. Compare this expression with the voltage gain for the continuous conduction mode.

ANSWER $\dfrac{V_o}{V_{\text{in}}} = D\sqrt{\dfrac{RT}{2nL_m}}$

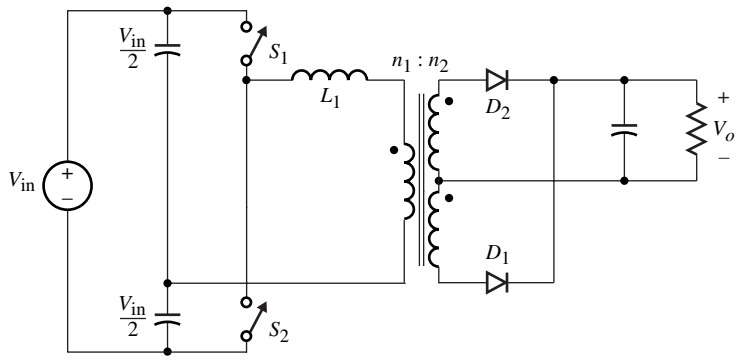
EXERCISE 5.9

Consider the flyback converter of Fig. 5.23(*b*) with $V_o = 48$ V at $I_o = 1$ A, $V_{\text{in}} = 18$ V, $f = 150$ kHz, $n = 0.3$. Find the maximum L_m so that the converter operates in dcm.

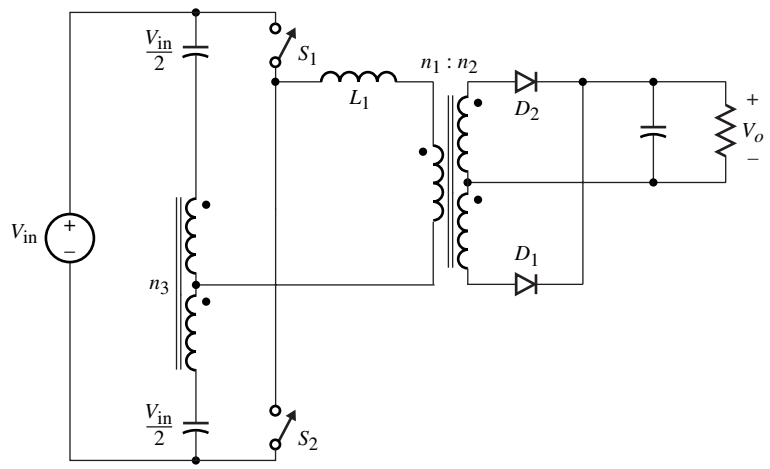
ANSWER 4.44 μH

5.3.2 Half-Bridge Converter

Because of the presence of an input inductance in series with the dc voltage source, the circuit implementation of the half-bridge converter requires a center-tap transformer. Figure 5.26(*a*) and (*b*) shows a discrete inductor and a center-tap transformer implementation of the half-bridge boost-derived converter.



(*a*)



(*b*)

Figure 5.26 Half-bridge boost-derived converter. (*a*) Single-inductor implementation. (*b*) Center-tap transformer implementation.

Because switches S_1 and S_2 are switched alternately, the topology of Fig. 5.26(*a*) is not suitable due to the abrupt change in the primary current. This problem does not exist for Fig. 5.26(*b*), in which a center-tap transformer is added. It can be shown that the voltage gain is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{2}\left(\frac{n_2}{n_1}\right)\frac{1}{1-D} \tag{5.21}$$

5.3.3 Full-Bridge Converter

Figure 5.27 shows the full-bridge boost-derived converter with a full-wave rectifier in the output side. This converter is also known as a double-ended converter.

The main advantage of the full-bridge configuration is that its core material is better utilized compared to the single-ended case, in which the magnetic field density changes from 0 to $+B_{\text{sat}}$. For the full-bridge configuration the core excitation varies between $+B_{\text{sat}}$ and $-B_{\text{sat}}$. There are several switching sequences for Fig. 5.27 that will result in a duty cycle above 50%. Figure 5.28 shows two possible switching sequences.

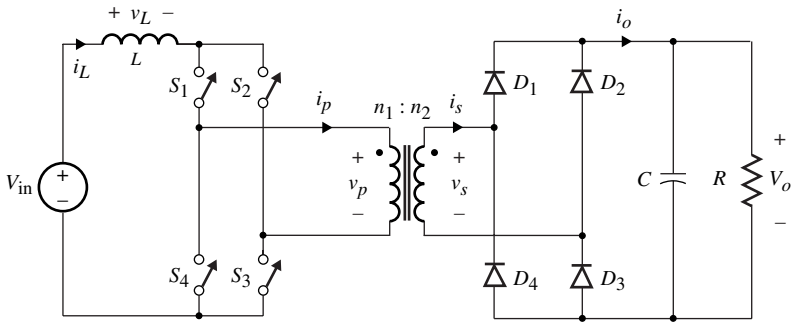
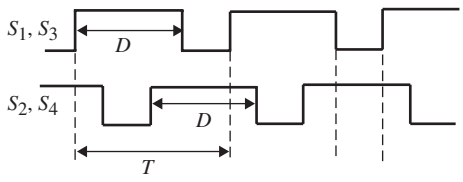
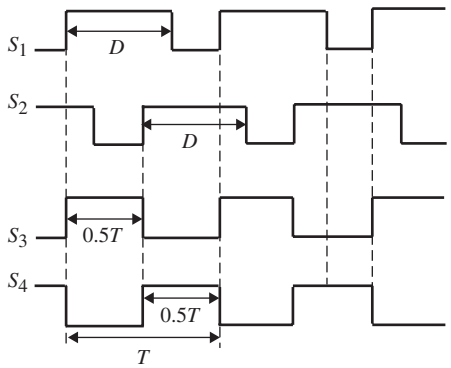


Figure 5.27 Full-bridge boost-derived converter with full-wave output rectifier.



(*a*)



(*b*)

Figure 5.28 Two possible switching sequences for the full-bridge converter of Fig. 5.27.

In Fig. 5.28(*a*), each of the two diagonal pairs of switches are switched simultaneously with $D > 0.5$ for each switch. With this switching sequence, there exist two intervals during which all four switches are on at the same time. During these intervals, the inductor current is divided almost equally between the switch legs S_1-S_4 and S_2-S_3, reducing their rms current values. In the switching sequence of Fig. 5.28(*b*), two of the switches operate with a fixed duty cycle and the other two switches operate with a varying duty cycle. Of course, the driving circuit for Fig. 5.28(*a*) is more complex since unlike Fig. 5.28(*b*), where only two switches are controlled, the switching sequence of Fig. 5.28(*a*) is required to control four switches. Next we consider the analysis of the circuit shown in Fig. 5.27 when operated under the switching sequence of Fig. 5.28(*a*). It can be shown that there are four modes of operation during one switching period, as shown in Fig. 5.29.

The inductor current during mode 1 is given by

$$i_L(t) = \frac{V_{\text{in}}}{L}t + I_L(0) \tag{5.22}$$

where $I_L(0)$ is the initial inductor current when S_1 and S_3 are turned on, while S_2 and S_4 were on initially. This current is divided equally through S_1-S_4 and S_2-S_3, with $v_s = v_p = 0$ and $i_o = 0$.

At $t = t_1$, S_2 and S_4 are turned off simultaneously, forcing $i_L(t)$ to flow through the primary, through diodes D_1 and D_3, and then to the load. The equivalent circuit is shown in Fig. 5.29(*b*).

The inductor current is obtained from v_L:

$$v_L(t) = V_{\text{in}} - \frac{n_1}{n_2}V_o \qquad 0 \le t < t_1$$

Therefore, the inductor current is given by

$$i_L(t) = \frac{V_{\text{in}} - \dfrac{n_1}{n_2}V_o}{L}(t - t_1) + I_L(t_1) \tag{5.23}$$

In this mode v_p and v_s are given by

$$v_s = V_o \qquad v_p = \frac{n_1}{n_2}V_o$$

Mode 3 starts at $t = t_2$, when S_2 and S_4 are turned on again, resulting in a similar equivalent circuit to that in mode 1. The current equation is given by

$$i_L(t) = \frac{V_{\text{in}}}{L}(t - t_2) + I_L(t_2) \tag{5.24}$$

At $t = t_3$, we have

$$I_L(t_3) = \frac{V_{\text{in}}}{L}(t_3 - t_2) + I_L(t_2)$$

Finally, mode 4 starts at $t = t_3$, when S_1 and S_3 are turned off simultaneously. The voltages are given as follows:

$$v_L = V_{\text{in}} + v_p \qquad v_p = \frac{n_1}{n_2}v_s \qquad v_s = -V_o$$

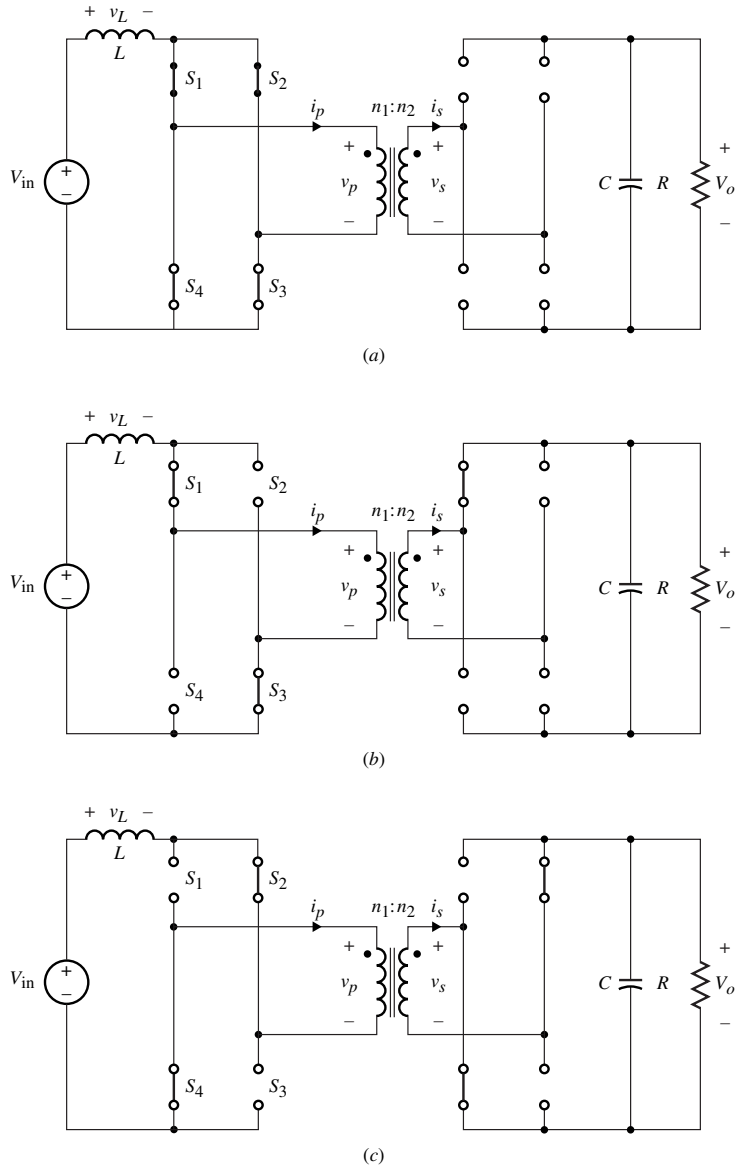


Figure 5.29 Modes of operation. (*a*) Modes 1 and 3: All switches are on. (*b*) Mode 2: S_1 and S_3 are on. (*c*) Mode 4: S_2 and S_4 are on.

Hence, the currents are given as

$$i_L(t) = \frac{V_{\text{in}} - \dfrac{n_1}{n_2}V_o}{L}(t - t_3) + I_L(t_3)$$

$$i_p(t) = -i_L$$

$$i_s(t) = \frac{n_1}{n_2}i_p$$

The current and voltage waveforms are shown in Fig. 5.30.

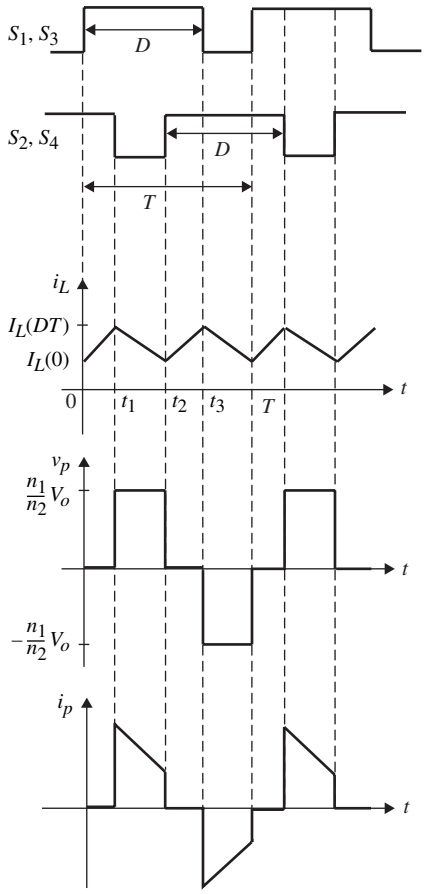


Figure 5.30 Current and voltage waveforms for Fig. 5.27.

From the volt-second principle, we have

$$t_1 V_{\text{in}} = (t_1 - t_2)\left(V_{\text{in}} - \frac{n_1}{n_2}V_o\right)$$

From Fig. 5.29, $t_1 = (D - \frac{1}{2})T$ and $(t_2 - t_1) = (1 - D)T$; hence, we have

$$(D - \tfrac{1}{2})TV_{\text{in}} = -(1 - D)T\left(V_{\text{in}} - \frac{n_1}{n_2}V_o\right) \tag{5.25}$$

Solving Eq. (5.25) for the voltage gain, we obtain

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1}\frac{1}{2(1 - D)} \tag{5.26}$$

EXAMPLE 5.6

(a) Derive the voltage gain expression for Fig. 5.27 by using the switching sequence given in Fig. 5.28(*b*).

(b) What is the rms current in each switch?

SOLUTION

(a) Although there is a change in the switching sequence between Fig. 5.28(*a*) and (*b*) in switches S_3 and S_4, careful investigation of the circuit operation modes indicates that conditions governing the charging and discharging of the inductor are exactly the same for both switching sequences. Therefore, the expression according to the volt-second balance as obtained above also applies here, and the voltage gain expression for the switching sequence given in Fig. 5.28(*b*) is the same as that given in Eq. (5.26).

(b)
$$I_{s,\text{rms}} = \sqrt{\frac{I_L^2}{2} + \frac{\Delta I_L^2}{24}} \tag{5.27}$$

where

$$I_L = \frac{n_2}{n_1}\frac{I_o}{2(1-D)}$$

is the average inductor current and

$$\Delta I_L = \frac{V_{\text{in}}}{L}\left(D - \frac{1}{2}\right)T \tag{5.28}$$

is the inductor current ripple.

EXERCISE 5.10

Derive the expressions for $i_L(0)$ and $i_L(DT)$ in Fig. 5.30 and determine the inductor's critical value, L_{crit}.

ANSWER $I_L(0) = \dfrac{n_2}{n_1}\dfrac{I_o}{2(1-D)} - \dfrac{V_{\text{in}}}{2L}\left(D - \dfrac{1}{2}\right)T$, $I_L(DT) = \dfrac{n_2}{n_1}\dfrac{I_o}{2(1-D)} + \dfrac{V_{\text{in}}}{2L}\left(D - \dfrac{1}{2}\right)T$,

$$L_{\text{crit}} = 2\left(\frac{n_1}{n_2}\right)^2 R(1-D)^2\left(D - \frac{1}{2}\right)T$$

EXERCISE 5.11

Show that the primary rms current of Fig. 5.27 is given by the following equation:

$$I_{p,\text{rms}} = \sqrt{2(1-D)(I_L^2 + \tfrac{1}{12}DI^2)}$$

5.4 OTHER ISOLATED CONVERTERS[1]

In addition to the circuits presented thus far, there are many other isolated converters that are covered in the open literature. Here we will consider two examples: the Cuk and the Weinberg converters.

5.4.1 Isolated Cuk Converter

Figure 5.31 shows the isolated Cuk converter. The converter storage capacitor is split into two series capacitors, C_1 and C_2, as shown. The output voltage remains negative since the transformer's primary and secondary windings have the same polarity. Let

[1]This section may be omitted without loss of continuity.

us derive the expression for the voltage gain. Assume the converter operates in the continuous conduction mode. Like the push-pull and bridge converters, the entire core *B-H* loop is utilized in both directions.

Figure 5.32(*a*) and (*b*) shows the two equivalent circuits for mode 1 when *S* is on and mode 2 when *S* is off.

Mode 1 (during *DT* interval):

$$v_{L1} = V_{\text{in}}$$

$$v_{L2} = -V_o - V_{c2} - \frac{n_2}{n_1} V_{c1}$$

Mode 2 (during $(1-D)T$ interval):

$$v_{L1} = V_{\text{in}} + V_{c1} + \frac{n_1}{n_2} V_{c2}$$

$$v_{L2} = -V_o$$

Applying the volt-second principle to v_{L1} and v_{L2}, we obtain

v_{L1}:

$$DV_{\text{in}} = -(1-D)\left[V_{\text{in}} + V_{c1} + \frac{n_1}{n_2} V_{c2}\right]$$

$$V_{\text{in}} \frac{-D}{1-D} = V_{\text{in}} + V_{c1} + \frac{n_1}{n_2} V_{c2}$$

$$V_{\text{in}} \frac{-1}{1-D} = V_{c1} + \frac{n_1}{n_2} V_{c2} \tag{5.29}$$

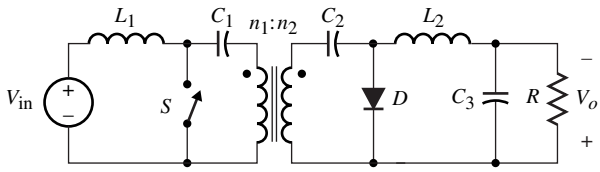
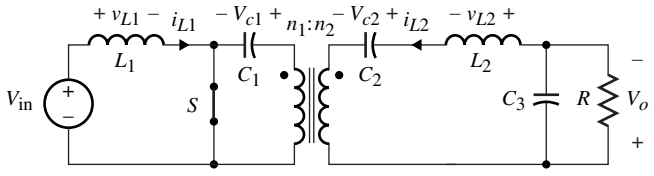
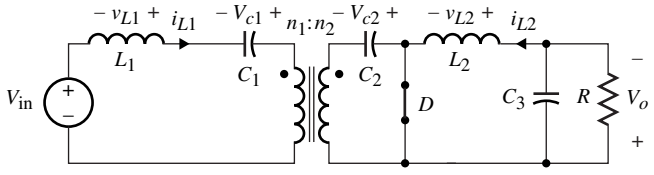


Figure 5.31 Isolated Cuk converter.



(*a*)



(*b*)

Figure 5.32 Isolated Cuk converter. (*a*) Mode 1. (*b*) Mode 2.

v_{L2}:

$$D\left[-V_o - V_{c2} - \frac{n_2}{n_1}V_{c1}\right] = +(1-D)V_o$$

$$-D\left(V_{c2} + \frac{n_2}{n_1}V_{c1}\right) = [+(1-D) - D]V_o$$

$$V_{c2} + \frac{n_2}{n_1}V_{c1} = \frac{-V_o}{D}$$

$$V_{c1} + \frac{n_1}{n_2}V_{c2} = -\frac{n_1}{n_2}\frac{V_o}{D} \tag{5.30}$$

From Eqs. (5.29) and (5.30), we obtain

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{1-D}\frac{n_2}{n_1}$$

EXERCISE 5.12

Consider the Cuk converter shown in Fig. E5.12, which provides a positive output voltage. Assume ideal components to derive the voltage gain equation V_o/V_{in}, and sketch the waveforms for i_{L1}, i_{L2}, i_D, v_{sw}, v_D, and v_{c1}.

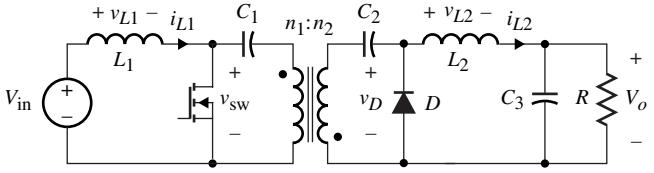


Figure E5.12

5.4.2 Weinberg Converter

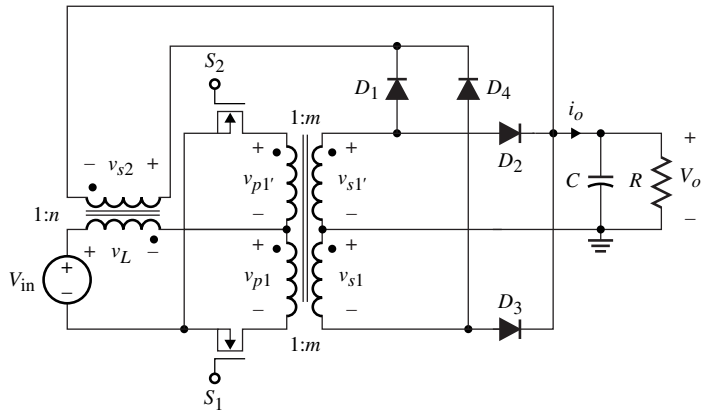
In this section, the basic topology and operation of another buck-derived push-pull converter, known as the Weinberg converter, will be discussed. There are several versions of this topology that perform the same function. The steady-state analysis will be presented in this section for the converter operating in ccm. The original proposed Weinberg dc-to-dc topology is shown in Fig. 5.33(*a*). A more simplified equivalent circuit can be obtained. In this analysis we will assume the *n*-turn-ratio transformer has a magnetizing inductance, L_m, and the *m*-turn-ratio transformer is ideal.

The switching waveforms are similar to those for the push-pull converter and are shown in Fig. 5.33(*b*). When switches S_1 and S_2 are turned on and off alternately, the following cases are investigated:

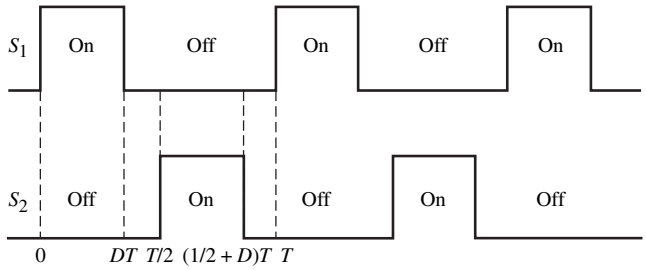
1. Mode 1: S_1 on, S_2 off
2. Mode 2: S_1 off, S_2 on
3. Mode 3: S_1 off, S_2 off

Mode 1: S_1 on, S_2 off ($0 < t \leq DT$)

In this case, the current from V_{in} flows through the magnetizing inductor of the input transformer, causing $v_{s2} > 0$; hence, D_1 and D_4 are turned off. With S_1 on, $v_{s1'} > 0$



(*a*)



(*b*)

Figure 5.33 The Weinberg dc-dc converter. (*a*) Circuit topology. (*b*) Switching waveforms for the power switches S_1 and S_2.

and $v_{s1} < 0$, causing D_3 to reverse-bias and D_2 to be forward biased. The equivalent circuit model is shown in Fig. 5.34(*a*).

From Fig. 5.34 we have $v_L = V_{\text{in}} - V_o/m$, yielding the following equation for i_L:

$$i_L(t) = \frac{V_{\text{in}} - V_o/m}{L} t + I_L(0) \tag{5.31}$$

where $I_L(0) = I_{L\min}$ is the initial inductor current at $t = 0$. Since the center-tap transformer has the same ratio, m, diode D_3 blocks twice the output voltage, i.e.,

$$v_{D3} = -2V_o$$

Mode 2: S_1 off, S_2 on $(T/2 < t \leq (0.5 + D)T)$

At $t = T/2$, S_2 is turned on while S_1 is kept off (S_1 is turned off in the previous interval at $t = DT$). In this case since the current from V_{in} flows through the magnetizing inductor, diodes D_1 and D_4 are turned off. The output diode, D_2, is off because S_2 is on, while D_3 is conducting to carry the inductor current.

From Fig. 5.34(*b*), the inductor voltage is $v_L = V_{\text{in}} - V_o/m$ and i_L is given by

$$i_L(t) = \frac{V_{\text{in}} - V_o/m}{L}(t - T/2) + I_L(T/2) \tag{5.32}$$

The blocking voltage of D_2 is $-2V_o$, and this case is identical to the case in mode 1. Since we have a symmetric circuit operation, these two modes are similar when either switch is on and the other one is off.

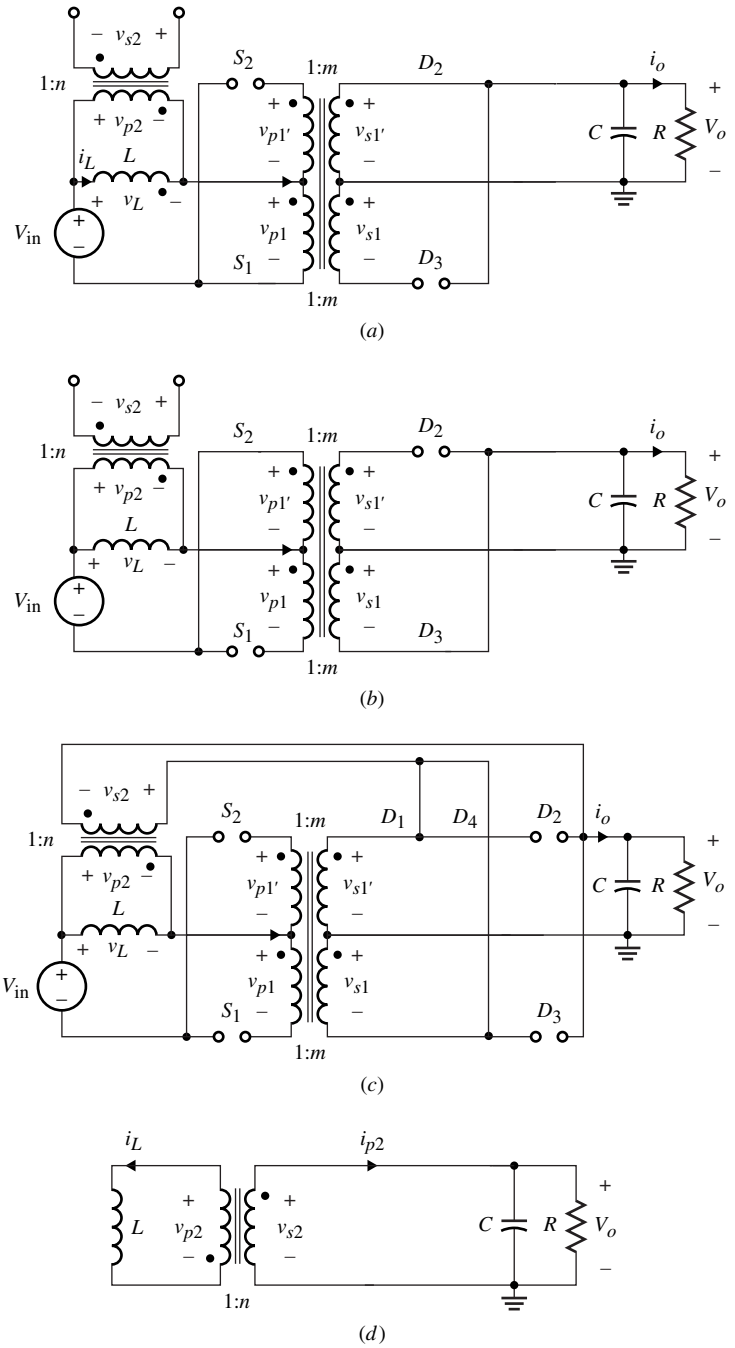


Figure 5.34 Modes of operation. (*a*) Equivalent circuit for mode 1, when S_1 is on and S_2 is off. (*b*) Equivalent circuit for mode 2, when S_2 is on and S_1 is off. (*c*) Equivalent circuit for mode 3, when both S_1 and S_2 are off. (*d*) Simplified equivalent circuit of mode 3.

Mode 3: S_1 off, S_2 off ($DT < t \leq T/2$ and $(0.5 + D)T < t \leq T$)

In this case, since the two switches are turned off, D_1 and D_4 are turned on, while D_2 and D_3 are turned off. The equivalent circuit is shown in Fig. 5.34(*c*), and the simplified equivalent circuit is shown in Fig. 5.34(*d*).

From Fig. 5.34(*d*), the inductor voltage is $-V_o/n$, and the inductor current for the first interval is given by

$$i_L(t) = -\frac{V_o}{nL}(t-(DT)) + I_L(DT) \tag{5.33}$$

where $I_L(DT) = I_{L\max}$ is the initial inductor current at $t = DT$.

EXERCISE 5.13

Show that the average output and input currents for the Weinberg converter of Fig. 5.33(*a*) are given by Eqs. (5.34) and (5.35), respectively.

$$I_{o,\text{ave}} = \frac{(I_{L\max} + I_{L\min})}{2}\left(\frac{D}{m} + \frac{1-D}{n}\right) \tag{5.34}$$

$$I_{\text{in,ave}} = \frac{(I_{L\max} + I_{L\min})D}{2} \tag{5.35}$$

EXAMPLE 5.7

It can be shown that the two-switch Weinberg converter of Fig. 5.33(*a*) can be simplified by using a one-switch equivalent circuit model as shown in Fig. 5.35. Derive the inductor current and voltage gain equation, and draw the key current and voltage waveforms for the simplified converter of Fig. 5.35.

SOLUTION Figure 5.36(*a*) and (*b*) shows the two equivalent circuit modes. Figure 5.36(*c*) shows the switching waveforms for the simplified circuit of Fig. 5.35.

The inductor currents for the two modes are given by

$$i_L(t) = \frac{V_{\text{in}} - V_o/m}{L}t + I_L(0) \qquad 0 < t \le DT \tag{5.36a}$$

$$i_L(t) = -\frac{V_o}{nL}(t-(DT)) + I_L(DT) \qquad DT < t \le T \tag{5.36b}$$

It can be shown that the voltage gain equation is

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{\frac{D}{m} + \frac{1-D}{n}} \tag{5.37}$$

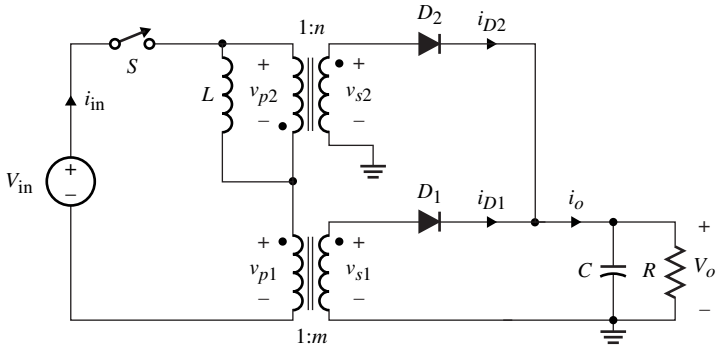


Figure 5.35 Simplified one-switch equivalent circuit model.

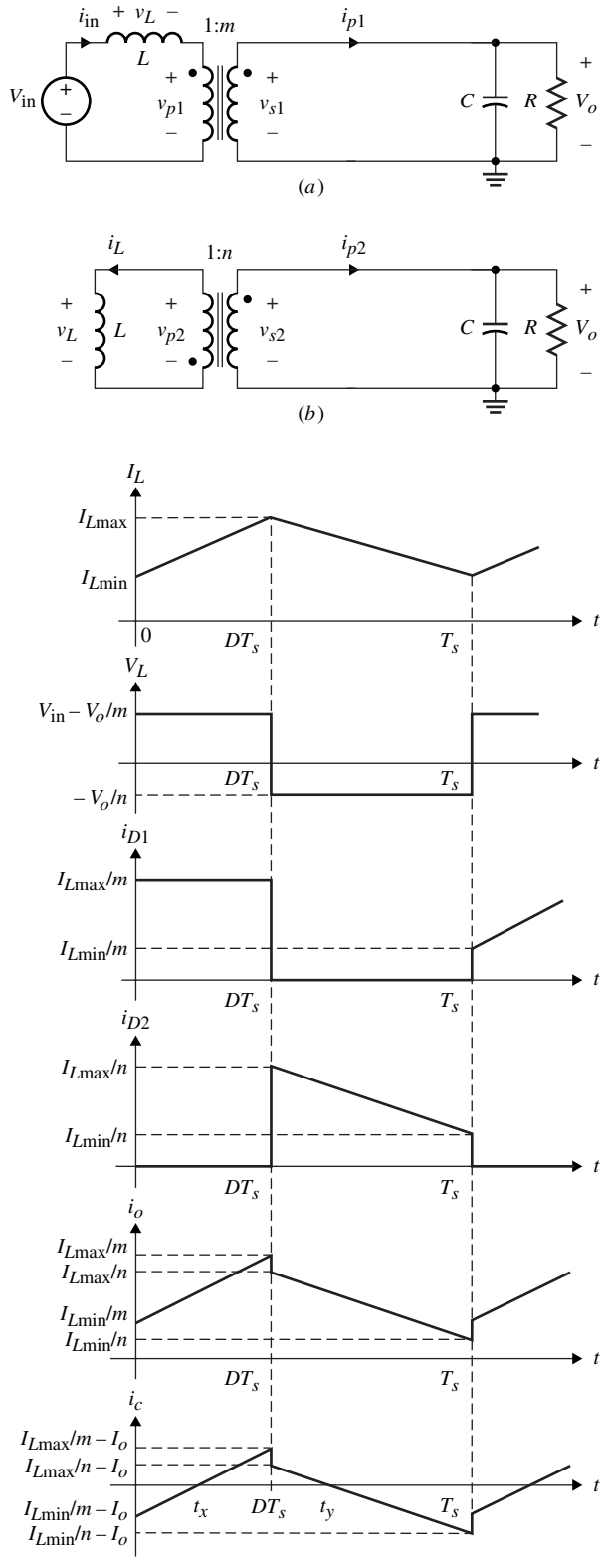


Figure 5.36 Equivalent circuits for Fig. 5. 35. (*a*) Mode 1: The switch is on. (*b*) Mode 2: The switch is off. (*c*) Converter waveforms.

If $m = n$, then the voltage gain becomes the gain of the buck converter. Therefore,

$$\frac{V_o}{V_{\text{in}}} = D \tag{5.38}$$

It can be also shown that $I_{L\max}$ and $I_{L\min}$ are given by

$$I_{L\max} = \frac{V_o^2}{RDV_{\text{in}}} + \frac{V_o}{2nL}(1-D)T \tag{5.39a}$$

$$I_{L\min} = \frac{V_o^2}{RDV_{\text{in}}} - \frac{V_o}{2nL}(1-D)T \tag{5.39b}$$

For ccm operation, $I_{L\min} > 0$, and to obtain the critical inductance set $I_{L\min} = 0$:

$$L_{\text{crit}} > \frac{RDV_{\text{in}}}{2nV_o}(1-D)T \tag{5.40}$$

The normalized output capacitor ripple voltage is given by

$$\Delta V_{nc} = \frac{n^2\tau_n}{2\tau_{nRC}}\left[\left(\frac{I_{n,\max}}{n} - 1\right)^2 + \left(\frac{mD}{n(1-D)}\right)\left(1 - \frac{I_{n,\min}}{m}\right)^2\right] \tag{5.41}$$

where $V_{nc} = V_c/V_{\text{in}}$, $\tau_n = \tau/T = L/RT$, $\tau_{nRC} = RC/T$, $I_{n,\max} = I_{\max}/I_o$, and $I_{n,\min} = I_{\min}/I_o$.

EXAMPLE 5.8

Consider a dc-dc converter unit system that uses the Weinberg converter with an input dc equal to 125 V and an output of 48 V. The design has the following specifications:

Output power $P_o = 2$ kW
Switching frequency $f = 40$ kHz
Output ripple voltage $\Delta V_c/V_o = 0.2\%$

Determine the following:

(a) The value of n where $D = 0.7$ and $m = 0.5$

(b) The critical inductance value

(c) The maximum and minimum inductor currents

(d) The average input and output currents

(e) The capacitor current value

SOLUTION

(a) From the gain relation, we have

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{\frac{D}{m} + \frac{1-D}{n}}$$

$$\frac{48}{125} = \frac{0.7}{\frac{0.7}{0.5} + \frac{1-0.7}{n}}$$

$$n \approx 0.7$$

(b) The critical inductance value is given by

$$L_{\text{crit}} > \frac{RDV_{\text{in}}}{nV_o}(1-D)T_s$$

$R = V_o^2/P = 1.152\ \Omega$ and $T_s = 1/f = 25\ \mu$s; therefore,

$$L_{\text{crit}} = \frac{(1.152)(0.7)(125)}{2(48)(0.7)}(1-0.7)(25\ \mu\text{s})$$

$$L_{\text{crit}} = 11.25\ \mu\text{H}$$

Select $L = 30\ \mu$H.

(c) The maximum inductor current is

$$I_{L\max} = \frac{V_o^2}{RDV_{\text{in}}} + \frac{V_o}{2nL}(1-D)T_s$$

$$I_{L\max} = \frac{(48)^2}{(1.152)(0.7)(125)} + \frac{48}{2(0.7)(30\ \mu\text{H})}(1-0.7)(25\ \mu\text{s})$$

$$I_{L\max} = 31.4\ \text{A}$$

and the minimum value is given by

$$I_{L\min} = \frac{V_o^2}{RDV_{\text{in}}} - \frac{V_o}{2nL}(1-D)T_s$$

$$I_{L\min} = 14.3\ \text{A}$$

(d) From Equation (5.34) we have

$$I_{o,\text{ave}} = \frac{(I_{L\max} + I_{L\min})}{2}\left(\frac{D}{m} + \frac{1-D}{n}\right)$$

$$I_{o,\text{ave}} = \frac{(31.4 + 14.3)}{2}\left(\frac{0.7}{0.5} + \frac{1-0.7}{0.7}\right)$$

$$I_{o,\text{ave}} = 41.78\ \text{A}$$

and from Equation (5.35) we have

$$I_{\text{in,ave}} = \frac{(I_{L\max} + I_{L\min})D}{2}$$

$$I_{\text{in,ave}} = \frac{(31.4 + 14.3)}{2}(0.7)$$

$$I_{\text{in,ave}} = 16\ \text{A}$$

(e) The times at which the capacitor current becomes zero are given by

$$t_x = \frac{(I_o - I_{L\min}/m)}{\frac{1}{L}\left(\frac{V_{\text{in}}}{m} - \frac{V_o}{m^2}\right)}$$

$$t_x = \frac{(41.78 - 14.3/0.5)}{\frac{1}{30\ \mu\text{H}}\left(\frac{125}{0.5} - \frac{48}{0.5^2}\right)}$$

$$t_x = 6.83\ \mu\text{s}$$

and

$$t_y = \frac{nL}{V_o}(I_{L\max} - nI_o) + DT_s$$

$$t_y = \frac{(0.7)(30\ \mu\text{H})}{48}(31.4 - 0.7 \times 41.78) + (0.7)(25\ \mu\text{s})$$

$$t_y = 18.44\ \mu\text{s}$$

Recall

$$\tau_n = \frac{\tau}{T_s} = \frac{L/R}{T_s} = 1.04 \quad \text{and} \quad \tau_{nRC} = \frac{RC}{T_s}$$

Therefore,

$$\Delta V_{nc} = \frac{n^2\tau_n}{2\tau_{nRC}}\left\{\left(\frac{I_{n,\max}}{n} - 1\right)^2 + \left(\frac{mD}{n(1-D)}\right)\left(1 - \frac{I_{n,\min}}{m}\right)^2\right\}$$

$$\frac{0.2}{100} = \frac{(0.7)^2(1.04)(25\ \mu\text{s})}{2(1.152)C}[4.9\times10^{-3} + (0.67)(0.25)]$$

The value for the capacitor is obtained as

$$C = 476.6\ \mu\text{F}$$

5.5 MULTI-OUTPUT CONVERTERS

As stated earlier, one of the advantages of using an isolated transformer is to allow for multiple outputs at the secondary side of the output transformer. This is very common in today's power supplies used in components to provide several voltage levels at different currents and polarities. Figure 5.37(*a*) and (*b*) shows three-output examples of a half-bridge buck-derived converter and a single-ended flyback converter, respectively.

EXERCISE 5.14

Design the half-bridge converter of Fig. 5.37(*a*) to provide three output voltages with $V_{o1} = 5$ V at 6 A, $V_{o2} = 37$ V at 0.5 A, and $V_{o3} = 12$ V at 2 A. Design the transformer turn ratio and the converter components such that the voltage ripple for any output does not exceed 0.1%. Assume $V_{\text{in}} = 160$ VDC and a switching frequency of 100 kHz.

EXERCISE 5.15

Determine the rms currents for the power switches and transformer windings of Example 5.6.

ANSWER 0.877 A, 1.24 A, 3.24 A, 0.534 A, 1.34 A

EXERCISE 5.16

Design the multi-output converter of Fig. 5.37(*b*) for the following output specifications: $V_{o1} = +5$ V at 4 A, $V_{o2} = +12$ V at 0.5 A, $V_{o3} = -12$ V at 0.3 A. The ripple voltage does not exceed 100 mV peak-to-peak for each output. Use $V_{\text{in}} = 185$ V, $f_s = 50$ kHz, and $D = 0.5$.

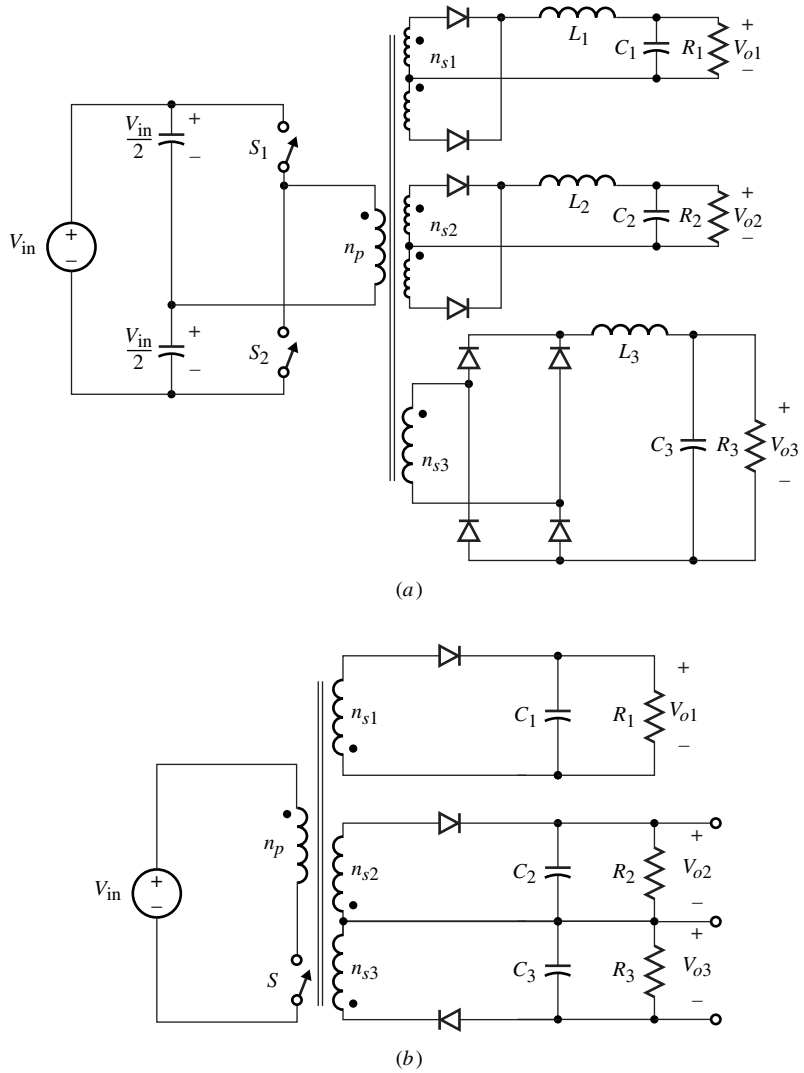


Figure 5.37 (*a*) Three-output half-bridge buck-derived converter. (*b*) Three-output flyback converter.

ANSWER $n_{s1}/n_p = 1/37$, $n_{s2}/n_p = n_{s3}/n_p = 12/185$, $L_m > 2.925$ mH, $C_1 > 400\ \mu$F, $C_2 > 50\ \mu$F, $C_3 > 30\ \mu$F

In practice, normally the output voltage with the highest power is controlled, with the other outputs using linear regulators to stabilize their voltages. This is why the open-loop outputs are designed for a higher voltage than specified.

PROBLEMS

Forward Converter

5.1 Consider the single-ended forward converter of Fig. P5.1 including a leakage inductance of the power transformer. Discuss the effect of L_k on the circuit operation.

D5.2 Design the forward converter of Fig. 5.8 that needs to supply 400 W at 15 A load current. The output ripple should not exceed 1%.

5.3 Derive the expression for the output ripple voltage for the forward converter of Fig. 5.8.

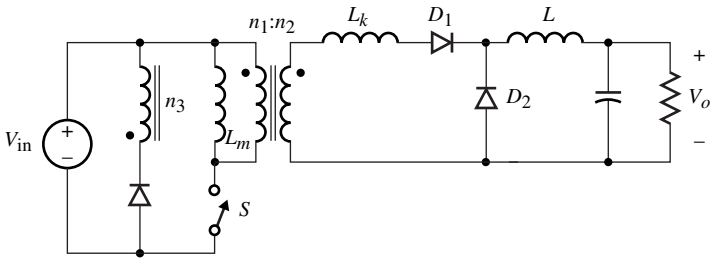


Figure P5.1

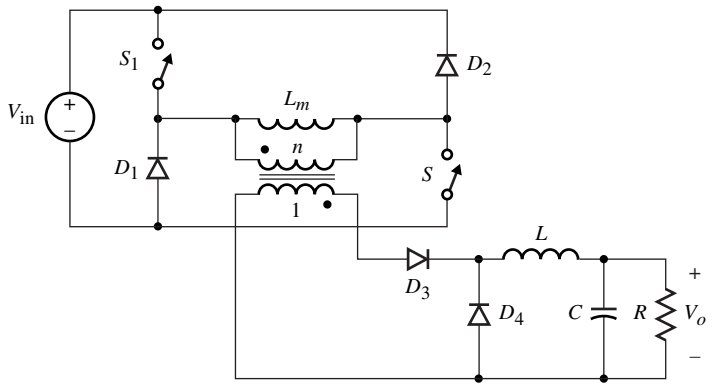


Figure P5.4

5.4 The circuit given in Fig. P5.4 is another type of forward converter. Sketch the primary voltage and diode current waveforms for the circuit.

5.5 Replace D_1 and D_2 by S_3 and S_4, respectively, in Problem 5.4. Derive the voltage gain if the four switches have the switching waveforms in Fig. P5.5.

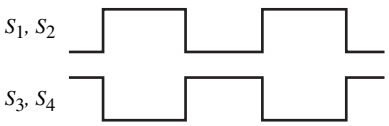


Figure P5.5

5.6 Consider the single-ended forward converter given in Fig. P5.6, which uses a regular and a zener diode to provide a negative voltage damp across the primary in order to reset the core to avoid transformer saturation.

(a) Discuss the operation of the circuit.

(b) Sketch the current waveforms i_{D1}, i_{D2}, i_L, i_{D3}, i_{sw}, and i_p.

Full-Bridge

D5.7 Design a full-bridge dc-dc converter with a center-tap output transformer with the following

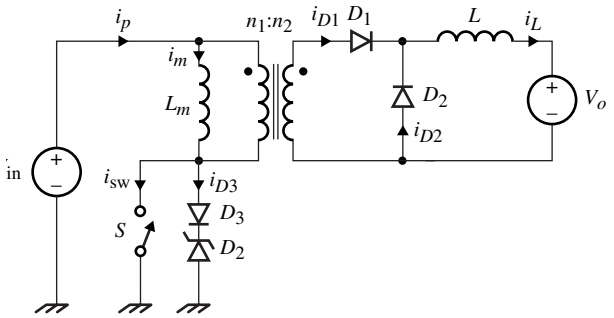


Figure P5.6

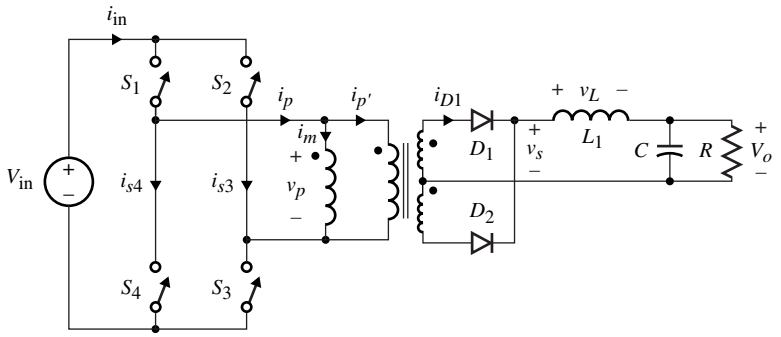


Figure P5.8

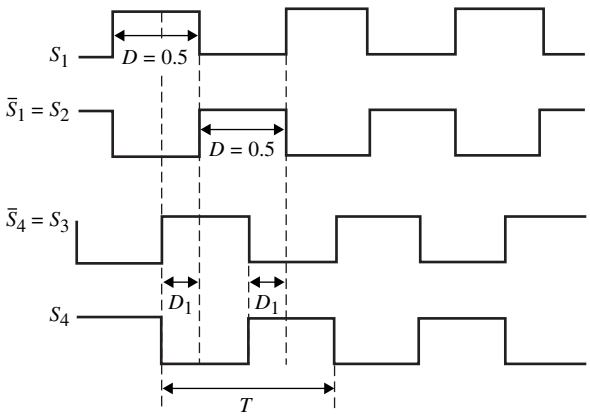


Figure P5.9

specifications: $V_{in} = 480$ V, $V_o = 240$ V at $I_o = 20$ A, $f_s = 75$ kHz.

5.8 Sketch the labeled current and voltage waveforms for the double-ended buck-derived converter shown in Fig. P5.8. Assume the switching sequence for S_1-S_3 and S_2-S_4 is the same as that in Fig. 5.19(*b*). Assume $RC >> T$.

5.9 Repeat Example 5.6 by using the switching sequence in Fig. P5.9. Derive the voltage gain in terms of the phase shift period D_1.

Push-Pull Converter

5.10 Derive the output voltage ripple for the push-pull converter.

Isolated SEPIC and Cuk Converter

5.11 Derive the voltage gain equation for the isolated SEPIC converter shown in Fig. P5.11.

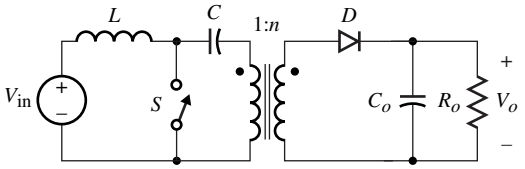


Figure P5.11

5.12 Derive the voltage gain expression for the isolated Cuk converter shown in Fig. P5.12.

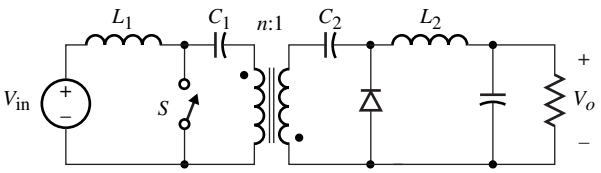


Figure P5.12

Weinberg Converter

5.13 Repeat Problem 5.3 for the Weinberg converter.

5.14 Show that the voltage gain equation for the Weinberg converter of Fig. 5.35 is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{\frac{D}{m} + \frac{1-D}{n}}$$

5.15 Show that t_x and t_y of Fig. 5.36 are given by

$$t_x = \frac{(I_o - I_{L\min}/m)}{\frac{1}{L}\left(\frac{V_{\text{in}}}{m} - \frac{V_o}{m^2}\right)}$$

$$t_y = \frac{nL}{V_o}(I_{L\max} - nI_o) + DT$$

For the special case when $I_{n,\max}/n = 1$, show that $t_y = DT_s$, t_x is the same as above, and ΔV_{nc} is given by

$$\Delta V_{nc} = \frac{n^2\tau_n}{2\tau_{nRC}}\left(\frac{mD}{n(1-D)}\right)\left(1 - \frac{I_{n,\min}}{m}\right)^2$$

Design Problems

Multi-Output Converters

D5.16 Design the four-output buck-boost converter shown in Fig. P5.16 to operate in ccm with the following specifications: $V_{\text{in,min}} = 28$ V, $V_{\text{in,max}} = 48$ V, $V_{\text{in,nom}} = 36$ V, $V_{o1} = 5$ V at $I_o = 10$ A, $V_{o2} = 5$ V at $I_o = 1$ A, $V_{o3} = 12$ V at $I_o = 2$ A, $V_{o4} = -12$ V at $I_o = 3$ A, $f_s = 70$ kHz, and $\Delta V_o/V_o = 1\%$ for each output.

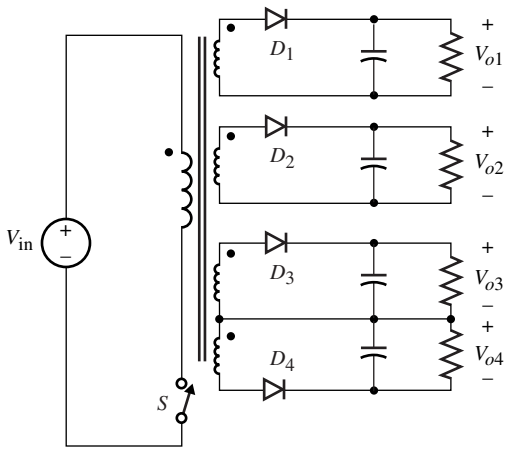


Figure P5.16

D5.17 Design the two-output forward converter shown in Fig. P5.17 to operate in ccm with the following specifications: $V_{\text{in,min}} = 78$ V, $V_{\text{in,max}} = 110$ V, $V_{\text{in,nom}} = 92$ V, $V_{o1} = 5$ V at $I_o = 15$ A, $V_{o2} = 12$ V at $I_o = 5$ A, $f_s = 70$ kHz, and $\Delta V_o/V_o = 1.5\%$ for each output.

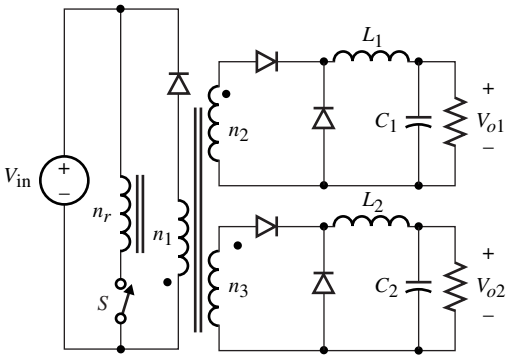


Figure P5.17

D5.18 Design the two-output, two-switch forward converter shown in Fig. P5.18 to operate in ccm with the following specifications: $V_{\text{in,min}} = 210$ V, $V_{\text{in,max}} = 480$ V, $V_{\text{in,nom}} = 370$ V, $V_{o1} = 5$ V at $I_o = 1.5$ A, $V_{o2} = 28$ V at $I_o = 5$ A, $f_s = 85$ kHz, $\Delta V_{o1}/V_{o1} = 0.1\%$, $\Delta V_{o2}/V_{o2} = 0.5\%$, $\Delta I_{o1}/I_{o1} = 15\%$, $\Delta I_{o2}/I_{o2} = 10\%$.

Single-Output Converters

D5.19 Design the simplified Weinberg converter shown in Fig. P5.19 to operate in ccm with the following specifications: $V_{\text{in,nom}} = 48$ V, $V_o = 22$ V at $I_o = 3$ A to 0.3 A, $f_s = 120$ kHz, and $\Delta V_o/V_o = 1\%$.

D5.20 Design the single-ended forward converter of Fig. 5.8 to operate in ccm with the following specifications: $V_{\text{in,nom}} = 28$ V, $V_o = 12$ V at $I_o = 4$ A to 1 A, $f_s = 125$ kHz, and $\Delta V_o/V_o = 1\%$. Assume the diode forward voltage drop is 1 V.

D5.21 Redesign Problem 5.20 using the push-pull converter of Fig. 5.19(*a*).

D5.22 Design the full-bridge converter of Fig. 5.18 to operate in ccm with the following specifications: $V_{\text{in,nom}} = 150$ V, $V_o = 12$ V at $I_o = 2$ A, $f_s = 50$ kHz, $\Delta V_o/V_o = 0.5\%$, $\Delta I_o/I_o = 5\%$.

D5.23 Design the half-bridge converter of Fig. 5.17(*a*) to operate in ccm with the following specifications: $V_{\text{in,nom}} = 185$ V, $V_o = 28$ V at $I_o = 2$ A, $f_s = 100$ kHz, $\Delta V_o/V_o = 0.1\%$, $\Delta I_o/I_o = 5\%$.

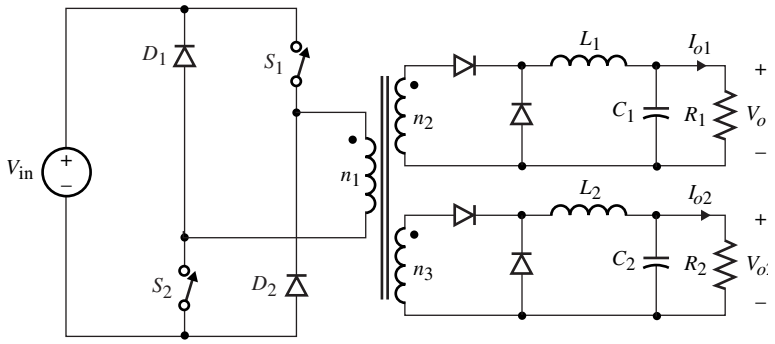


Figure P5.18

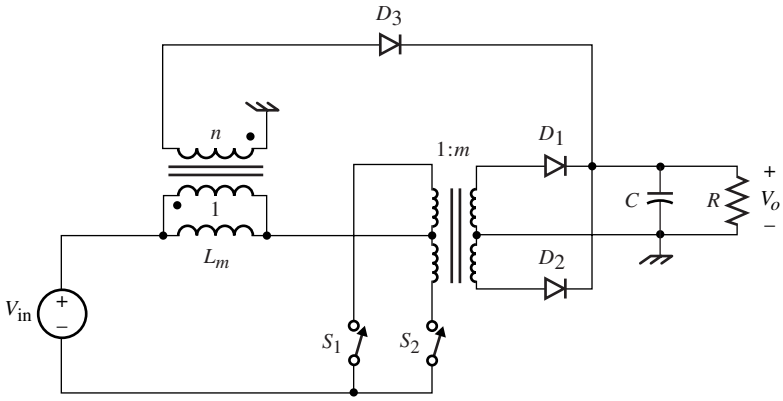


Figure P5.19

D5.24 Design the forward converter that uses a tertiary winding shown in Fig. 5.14 with the following specifications: $V_{\text{in,nom}} = 285\ \text{V} \pm 20\%$, $V_o = 12\ \text{V}$ at $I_o = 2\ \text{A}$ to $200\ \text{mA}$, $f_s = 120\ \text{kHz}$, $\Delta V_o = 100\ \text{mV}$. Determine the diode and transistor voltage and current ratings.

D5.25 Repeat Problem 5.24 with the same specifications except for an additional output voltage with the following specifications: $V_{o2} = 5\ \text{V}$ at 4 A to 500 mA and the output voltage ripple does not exceed 50 mV. The circuit configuration is shown in Fig. P5.25.

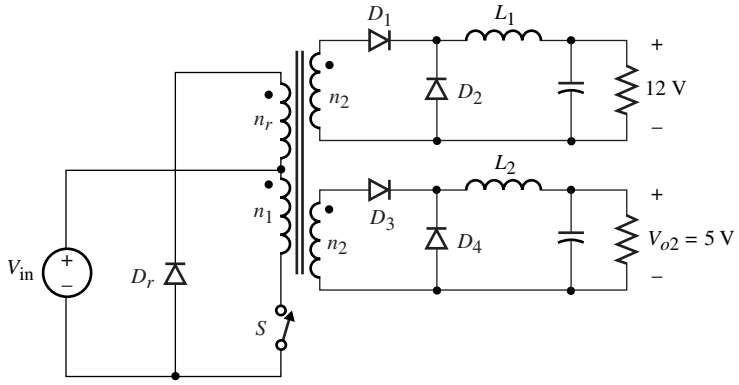


Figure P5.25

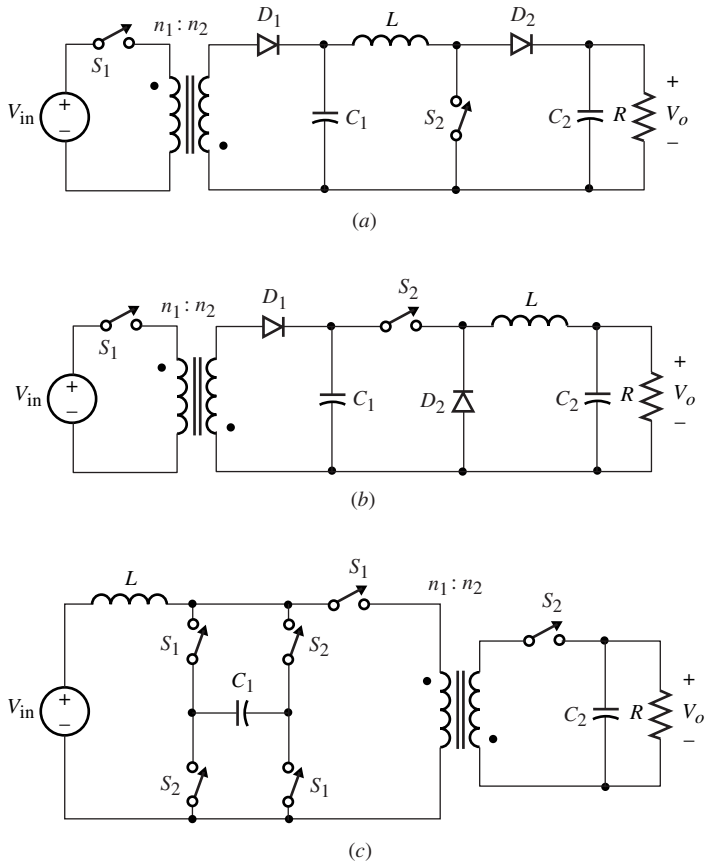


Figure P5.26

Additional Topologies

5.26 For the three circuits given in Fig. P5.26(*a*), (*b*), and (*c*), show that the voltage gains are given by the following equations, respectively. Assume S_1 and S_2 are switched simultaneously for (*a*) and (*b*), and S_1 and S_2 are switched complementarily for (*c*). Assume C_1 and C_2 are very large.

(a) $\dfrac{V_o}{V_{\text{in}}} = \dfrac{D}{(1-D)^2}\dfrac{n_2}{n_1}$

(b) $\dfrac{V_o}{V_{\text{in}}} = \dfrac{D^2}{(1-D)}\dfrac{n_2}{n_1}$

(c) $\dfrac{V_o}{V_{\text{in}}} = \dfrac{-D}{(1-D)(1-2D)}\dfrac{n_2}{n_1}$

5.27 The converter shown in Fig. P5.27(*a*) is another version of the forward converter. Assume ideal diodes. L_m is the transformer magnetizing inductance. The switching waveforms for S_1, S_2, S_3, and S_4 are shown in Fig. P5.27(*b*). Assume $RC >> T$.

(a) Sketch the current and voltage waveforms labeled on the figure.

(b) Derive the voltage gain expression, V_o / V_{in}.

5.28 Draw the waveforms for the branch currents and voltages for the push-pull converter including a finite magnetic inductance as shown in Fig. P5.28.

5.29 Show that if the single-ended flyback converter of Fig. 5.23(*b*) is operating in dcm (magnetizing current is discontinuous), then the voltage conversion ratio is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{n_2}{n_1} D \sqrt{\frac{1}{2\tau}}$$

where $\tau_n = L/RT$.

5.30 Consider the circuit given in Fig. P5.30(*a*) with the switching sequence given in Fig. P5.30(*b*).

(a) Sketch the waveforms for i_L, v_s, i_{D1}, and i_{D4}.

(b) Derive the expression for V_o / V_{in}.

(c) What is the expression for the critical value of L to maintain ccm operation?

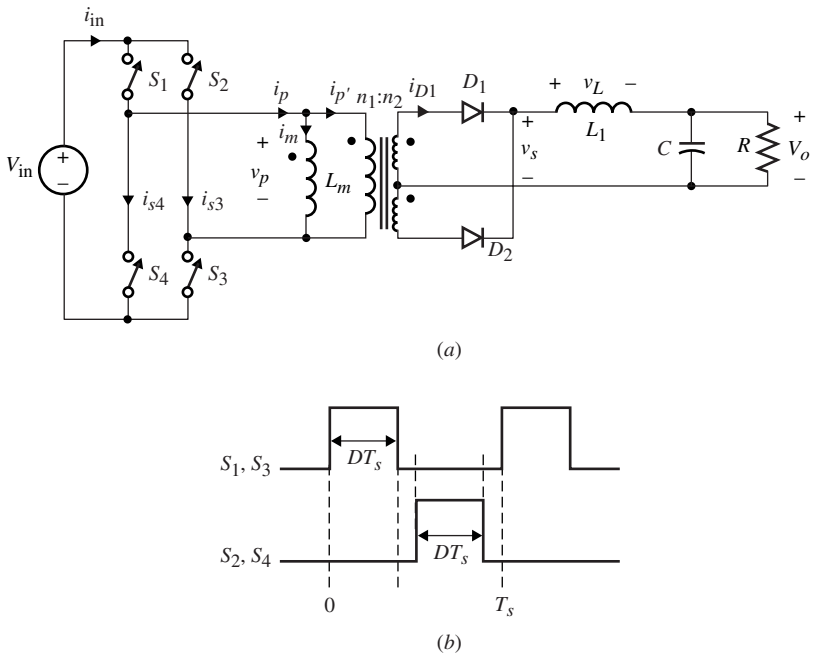


Figure P5.27

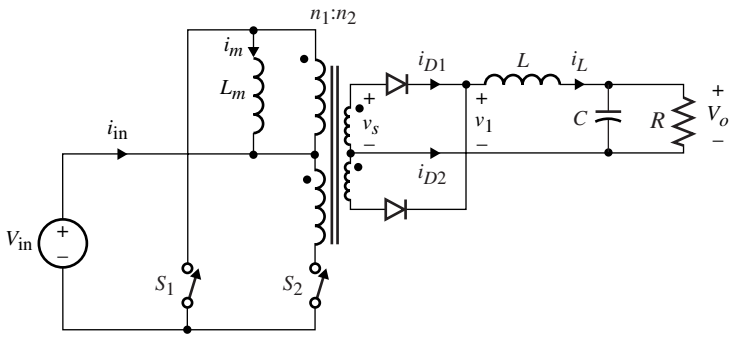


Figure P5.28

5.31 There are several core reset schemes available in today's dc-dc converters. Figure P5.31(*a*) and (*b*) shows two possible core-resetting circuits used in high-power applications. The winding n_r is the reset winding.

(a) Discuss the operation of each of the circuits and compare them to each other.

(b) Draw the waveforms for i_{in}, v_{sw}, i_o, v_o, and i_{D1}.

5.32 Derive the voltage gain equation for the isolated double-switch, single-ended dc-dc converter in Fig. P5.32. S_1 and S_2 are switched simultaneously.

5.33 Consider the current-fed push-pull converter given in Fig. P5.33. Derive the current gain expression I_o / I_{in}.

5.34 The converter shown in Fig. P5.34 is an isolated version of a converter given in Chapter 4. Assume the magnetizing inductance, L_m, is finite. Derive the expression for V_o / V_{in}.

5.35 Figure P5.35 shows the isolated version of the SEPIC converter, where a transformer is inserted in place of L_2. Assume the transformer has a magnetizing inductance, L_m, and a turn ratio of $n_1:n_2$.

(a) Sketch the waveforms for i_{L1}, i_{Lm}(magnetizing inductance), i_{c1}, i_D, v_p, v_s, and v_{sw}.

(b) Show that the voltage gain is given by

$$\frac{V_o}{V_{in}} = \frac{n_2}{n_1}\frac{D}{1-D}$$

where D is the duty cycle of the switch.

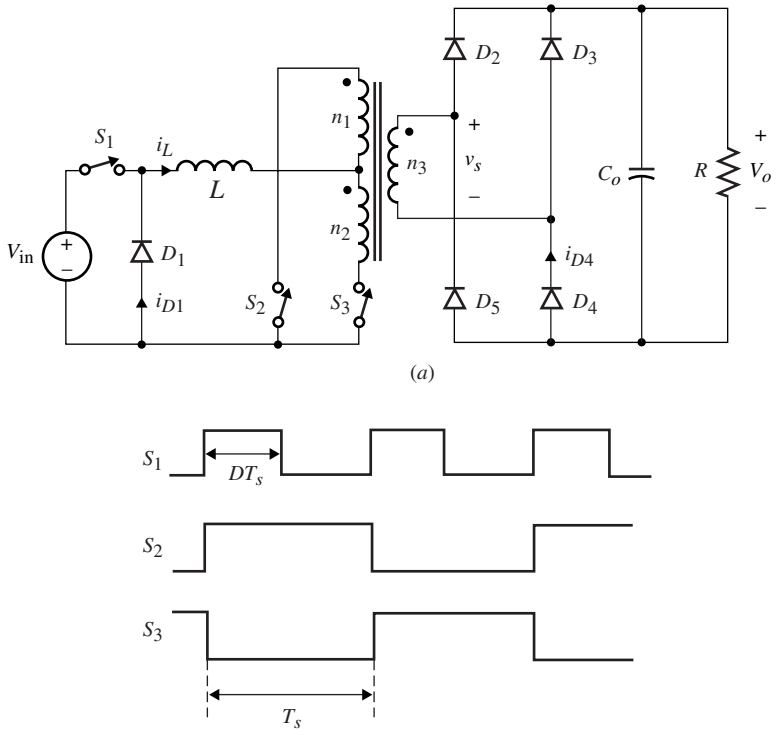


Figure P5.30

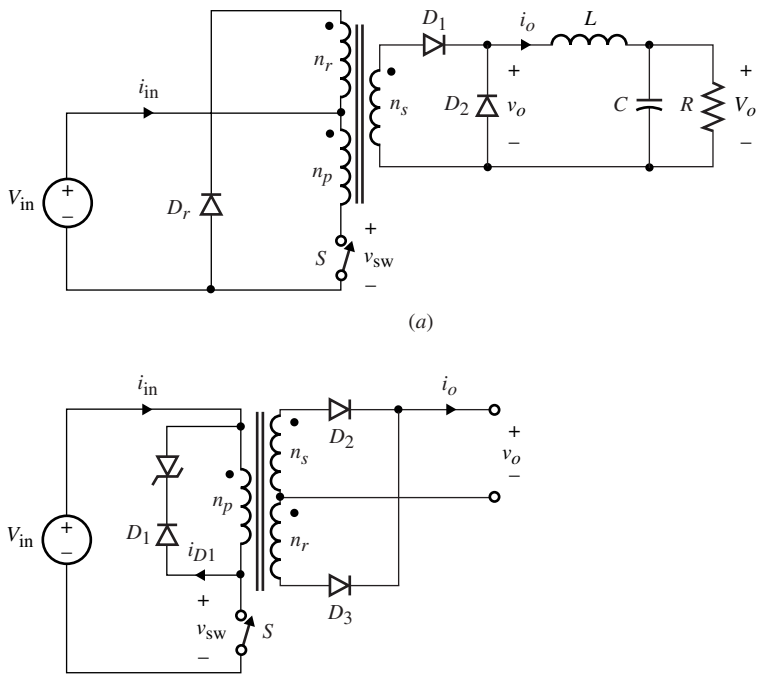


Figure P5.31

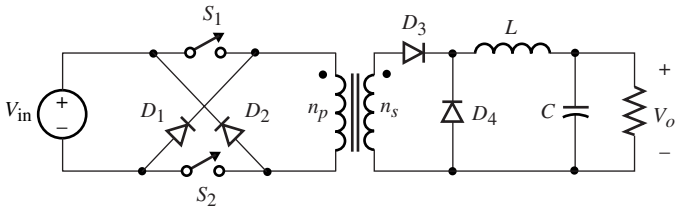


Figure P5.32

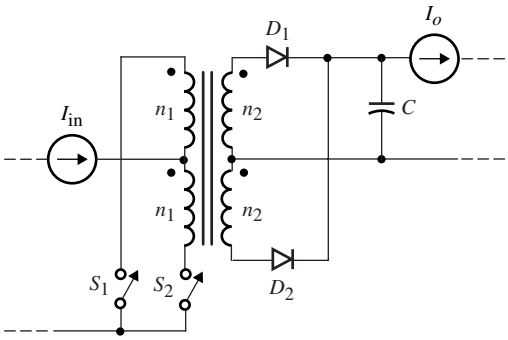


Figure P5.33

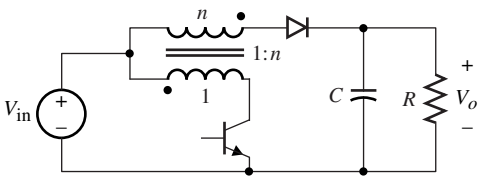


Figure P5.34

5.36 The converter in Fig. P5.36(*a*) and (*b*) is known as the isolated Watkins-Johnson converter. Assume S_1 and S_2 are switched on and off as shown in Fig. P5.36(*c*). Assume finite magnetizing inductance. Derive the expressions for V_o/V_{in} for each converter.

5.37 Draw the waveforms for the voltage and current variables in the push-pull converter shown in Fig. P5.37. Unlike Fig. 5.16(*a*), this converter is assumed to have finite magnetizing inductance.

D5.38 Consider a flyback converter that draws its input current from a dc voltage source varying between 185 V and 275 V and that produces an output voltage of +12 V at an average load current of 10 A.

(a) Determine the value of the transformer ratio and magnetizing inductance L_m.

(b) Determine the range of the duty cycle needed to maintain a constant output voltage. Assume $f = 85$ kHz and a maximum duty cycle of 0.6.

D5.39 Repeat the design in Problem 5.38 by assuming the power switch and diode have 3 V and 0.7 V voltage drops when conducting, respectively.

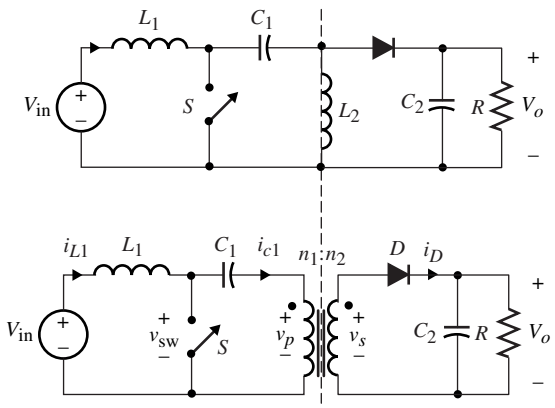


Figure P5.35

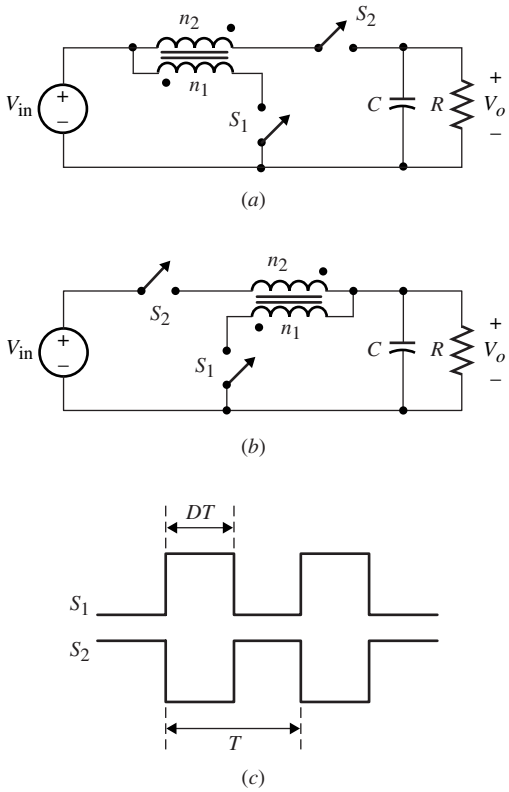


Figure P5.36

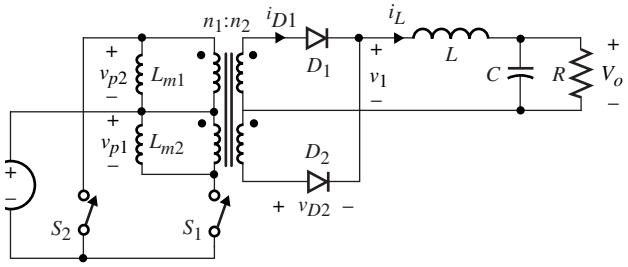


Figure P5.37