Chapter 4

Nonisolated Switch-Mode dc-dc Converters

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INTRODUCTION

In this chapter we discuss converter circuits that are used in power electronic systems to change the system voltages from one dc level to another dc level. Once again, switching devices will be used to process energy from the input to the output. Since the input here is dc, which comes from a post-filtering stage, these devices are normally operated at much higher frequencies than the line frequency, reaching as high as a few hundred kilohertz. This is why such converter circuits are known as high-frequency dc-to-dc switching converters or regulators. The term *regulator* is used since the circuit's main com-

mercial application is in systems that require a stable and *regulated* dc output voltage. Depending on whether or not an output transformer is used, high-frequency dc-to-dc switching converters are classified as isolated or nonisolated. In this chapter and in the next, the emphasis will be on the steady-state analysis and design of several well-known second- and fourth-order dc-to-dc converters, each having its own features and applications. We will consider those topologies that do not use high-frequency isolation transformers as part of their power stage. Moreover, a large number of applications require output electrical isolation and multiple outputs that cannot be achieved using the basic topologies discussed in this chapter. The isolated and magnetically coupled topologies will be discussed in Chapter 5. Such topologies are the most popular in the power supply industry and are used in various types of electronic equipment whose design requires outputs with electrical isolation and multi-outputs.

4.1 POWER SUPPLY APPLICATIONS

4.1.1 Linear Regulators

A typical block diagram of a linear regulator power supply is shown in Fig. 4.1. The front end of the linear regulator is a 60 Hz transformer, T_1, used to provide input electrical isolation and to step up or step down the line voltage, and this is followed by a full-wave bridge rectifier to convert the ac input to a dc input by adding a large filtering capacitor at the input of the linear regulator. This input to the linear regulator, V_{in}, is unregulated dc and cannot be used to drive the load directly. Using a linear circuit that provides a stable dc output regulates the dc voltage at the output, V_o.

For many years, most power supplies available in the market were of the linear regulator type, in which a series-pass active element is used to regulate the output voltage. In general, the active semiconductor element is used as a variable resistance to dissipate unwanted or excess voltage. Such an arrangement results in large amounts of power being dissipated in the active element, which can cause the efficiency to drop to as low as 40%. Because of this low efficiency, linear regulators have not been used

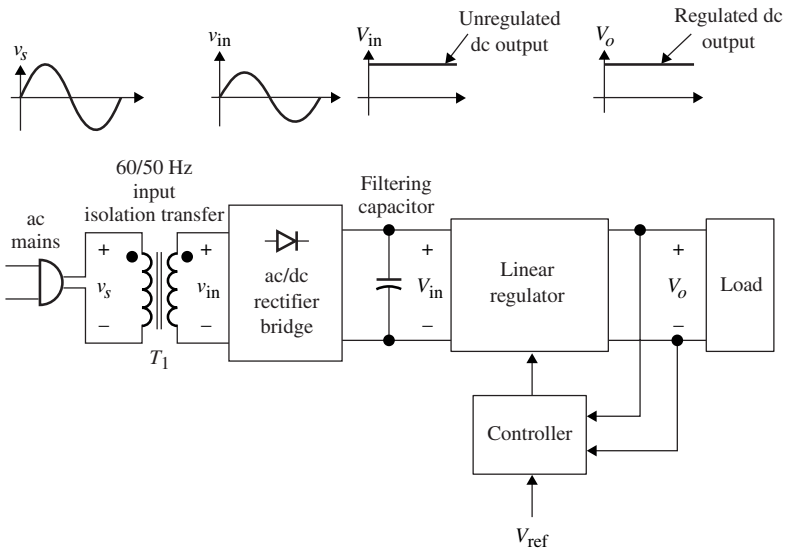


Figure 4.1 Typical block diagram of a linear regulator power supply.

for medium- and high-power applications since the early 1970s, when switched-mode dc-dc converters entered the marketplace. Despite the fact that linear regulators are simple to use and provide tight control, good output voltage ripples, and a low component count, their disadvantages are so numerous that their practical use is limited. Because of their high power losses, they suffer from high thermal dissipation, resulting in low power density and low efficiency.

Figure 4.2 illustrates a simplified circuit to show how the series active element is connected in a linear regulator. V_{in} represents the unregulated input voltage, V_{Excess} is the excess voltage to be dissipated across the linear device, and V_o is the output voltage. V_{Excess}, which is the difference between V_{in} and V_o, must be large enough to keep the transistor in the linear active mode, acting as a variable resistor used only to absorb the difference in the voltage. This is why V_{Excess} is considered one of the key design parameters of linear regulation. To illustrate how the linear resistor works, we present a simplified topology showing the series element regulator in Fig. 4.3, where V_{ref} is generated by a zener diode, and R_1 and R_2 are used as a voltage divider. The magnitude of i_B determines how deeply the transistor is driven in the saturation region. The comparator is used to compare the output voltage with a fixed reference voltage. As the output voltage increases, the base current, i_B, decreases and the excess voltage, v_{CE}, increases, hence reducing the output voltage. Similarly, if the output voltage decreases, the result is a reduced v_{CE} and an increased output.

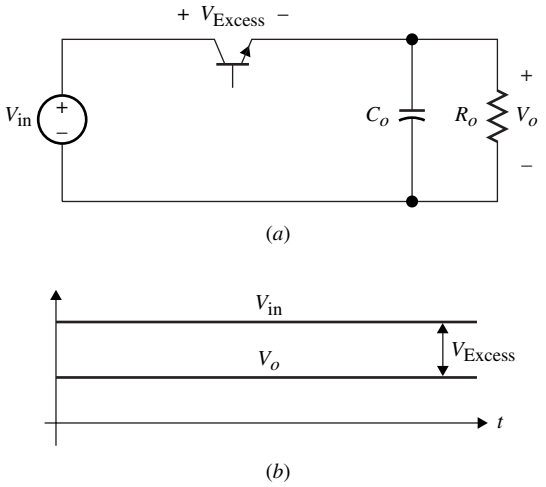


Figure 4.2 (*a*) Typical configuration for a series active element used in a linear regulator. (*b*) Average voltage waveforms.

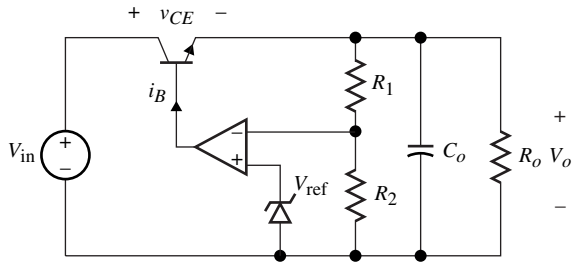


Figure 4.3 Simplified representation of a simple series element regulator.

4.1.2 Switched-Mode Power Supplies

The development of the power semiconductor switch made it possible for power electronics engineers to design power supplies with much higher efficiencies compared with linear regulators. Since transistors are used as switching devices, such power supplies are known as switched-mode power supplies or simply switching converters. In recent years, switching converters have become very popular due to recent advances in semiconductor technology. Today switching devices are available with very high switching speeds and very high power-handling capabilities. It is possible to design switched-mode power supplies with efficiency greater than 90% with low cost and relatively small size and light weight.

Unlike linear regulators, switching converters use power semiconductor devices to operate in either the on-state (saturation or conduction) or the off-state (cutoff or nonconduction). Since either state will lead to low switching voltage or low switching current, it is possible to convert dc to dc with higher efficiency using a switching regulator. Figure 4.4 shows a simplified block diagram for a switched mode ac-to-dc power converter with multi-output application. Compared with the block diagram of Fig. 4.2, a switching network and high-frequency output electrical isolation transformer T_2 are added. The objective is to control the *on* time of the power devices to regulate the dc output voltage. The post-filtering is used to reduce the output voltage ripple. This chapter will discuss the detailed power stage operation of the dc-to-dc block shown in Fig. 4.4 without including the high-frequency isolation transformer. Because of the regulation method used, these converters are known as pulse-width-modulation (PWM) converters.

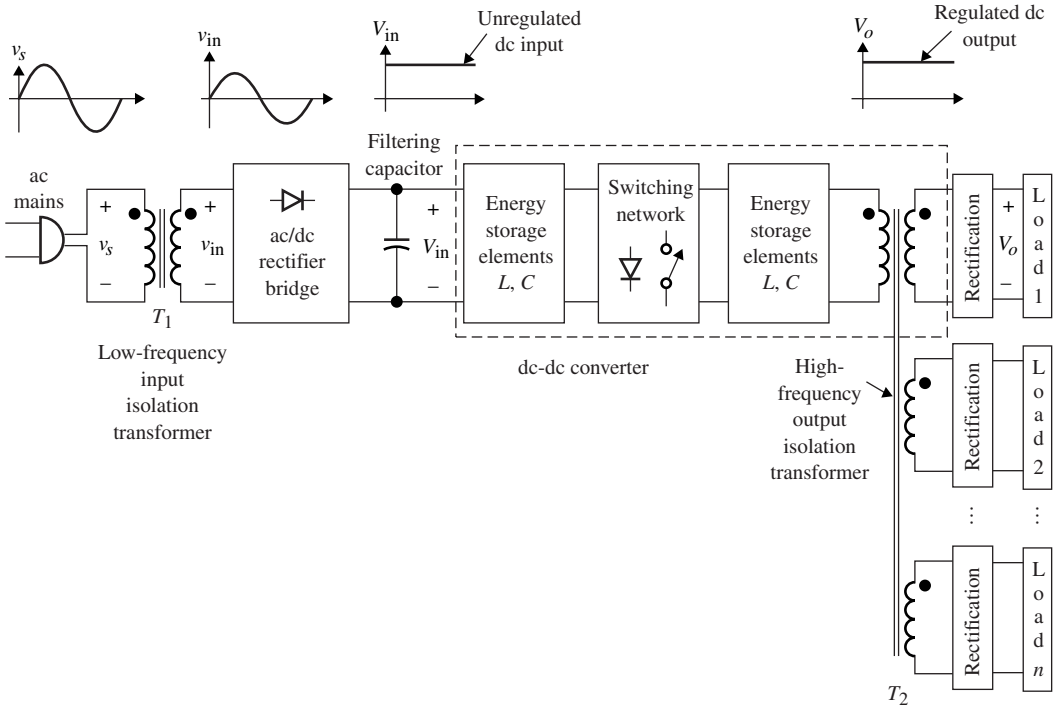


Figure 4.4 Block diagram of a switched-mode power supply with multiple outputs.

4.2 CONTINUOUS CONDUCTION MODE

Steady-state analyses of the basic direct-connected second-order converters such as the buck (step-down), boost (step-up), and buck-boost (step-up/down), and fourth-order converters such as Cuk and SEPIC converters will be presented in this chapter. Both the continuous and discontinuous conduction modes of operation, as well as some nonideal effects will be included in the analysis. The steady-state analysis of isolated or magnetically coupled converters (which are derived from these basic converters) such as the flyback, forward, push-pull, half- and full-bridge, and Weinberg converters will be discussed in Chapter 5.

First, we introduce the basic concept of a switched-mode circuit and the conversion technique in switching converters. Consider the simplest switching voltage converter, shown in Fig. 4.5. We assume that the switch is ideal and it is turned on at $t = t_0$ and turned off at t_1 alternately as shown in Fig. 4.6(*a*), where $f = 1/T$ is the switching frequency.

The waveforms for the output voltage, v_o, and the output current, i_o, are shown in Fig. 4.6(*b*) and (*c*), respectively, where V_{in} is the dc input voltage. The average output voltage is given by

$$\begin{aligned} V_o &= \frac{1}{T}\int_{t_0}^{T+t_0} v_o(t)\, dt \\ &= \frac{1}{T}\int_{t_0}^{t_1} V_{\text{in}}\, dt = \frac{t_1 - t_0}{T} V_{\text{in}} \end{aligned} \tag{4.1}$$

If we let D be defined as the duty ratio or duty cycle,

$$D = \frac{\text{On time}}{\text{Switching period}} = \frac{t_1 - t_0}{T} \tag{4.2}$$

then the average output voltage, V_o, is given by

$$V_o = DV_{\text{in}} \tag{4.3}$$

EXERCISE 4.1

If the output ripple factor $K_{o,\,\text{ripple}}$ is defined by the relation

$$K_{o,\,\text{ripple}} = \frac{\sqrt{V_{o,\text{rms}}^2 - V_o^2}}{V_o}$$

where $V_{o,\text{rms}}$ and V_o are the rms and average values of $v_o(t)$, respectively, determine the output ripple factor for Fig. 4.5.

ANSWER $K_{o,\text{ripple}} = \sqrt{\dfrac{1}{D} - 1}$

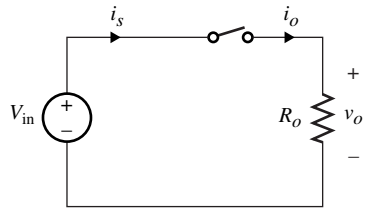


Figure 4.5 A simple switching circuit.

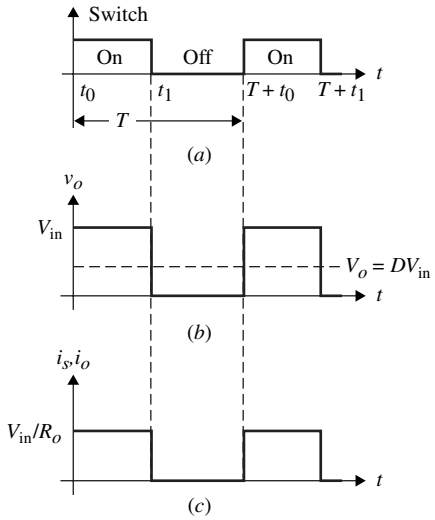


Figure 4.6 Switching waveform for Fig. 4.5.

It is clear from Eq. (4.3) that the average output voltage is less than the applied dc voltage. Assuming an ideal switch, theoretically speaking, the efficiency of this converter is 100%. The drawback of this simple switching circuit is that the output voltage is not constant, but a chopped dc with high ripple voltage. This results in high harmonics being generated at the load. This will not be acceptable for an electronics load when the output must be regulated to a fixed dc level with little ripple. However, in some application where a precise output voltage is not required, such as heating, light dimming, electroplating, and mechanical applications, this simple arrangement might be used, especially if the frequency is very high.

One approach to smooth the output voltage is to use a low-pass filter at the output of the circuit in order to filter the high-switching-frequency components of the output voltage. The filter may consist of a simple capacitor and inductor. The capacitor is used to hold a dc value across the output resistor, and the inductor is used within the circuit to serve as a nondissipative storage element needed to store energy from the input source and deliver it to the load. It can be argued that one single-pole, single-throw switch will not be sufficient to perform energy processing from the input to the output; rather, two switches or a single-pole, double-throw switch is required. This can be easily justified since the inductor current cannot be instantaneously interrupted. When one switch is switched, resulting in a sudden change in the inductor current, a second switch must be switched so that the continuity of the inductor current is maintained. Hence, a practical representation for a switched-mode converter must include either two switches, as shown in Fig. 4.7(*a*), or a single switch, as shown in Fig. 4.7(*b*). The inductor and capacitor elements are used as energy storage components to allow energy transfer from the input to the output. The output capacitor forms a low-pass filter to produce dc output voltage with little ripple. Most topologies, either isolated or nonisolated, will consist of one inductor and one output capacitor—hence the name *second-order* voltage converter. Fourth-order voltage converters consist of two inductors and two capacitors, which are considered series or combinations of second-order converters.

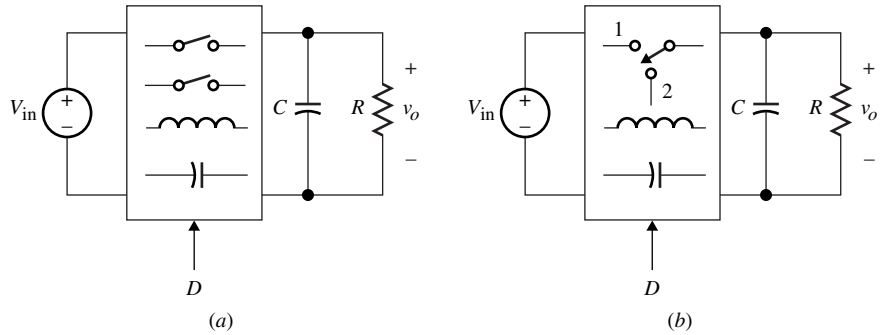


Figure 4.7 Typical block diagram representations for switching converters with (*a*) two independent switches and (*b*) one single-pole, double-throw switch.

In second-order converters, depending on the arrangements of the switches and *L*, three possible topologies can be obtained, namely buck, boost, and buck-boost, as shown in Fig. 4.8. Since these switches cannot be turned on and off simultaneously, single-pole, double-throw switches are used, which can be either on or off. In the following sections these converters will be thoroughly analyzed by deriving their steady-state characteristics. Since all switched-mode converters have pulsating currents and voltages, the dc output voltage can be obtained by adding a low-pass filter. It will be shown that in most of these converters an *LC*-type low-pass filter section is present. In fourth-order circuits like the Cuk and SEPIC, multiple *LC* low-pass filter sections are added.

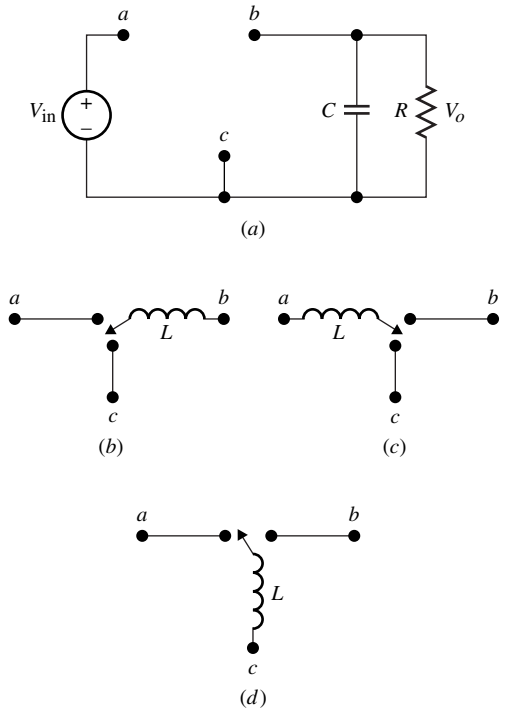


Figure 4.8 (*a*) Three possible ways to insert a low-pass *LC* filter between a dc source and a capacitive load: (*b*) buck converter, (*c*) boost converter, and (*d*) buck-boost converter.

EXAMPLE 4.1

Consider the simple PWM converter of Fig. 4.5 with $V_{\text{in}} = 28$ V and $f_s = 50$ kHz. Assume an ideal switch.

(a) Design for D and R so that the power delivered to the load is 25 W at an average output current of 1.5 A.

(b) Find the output ripple factor.

(c) Find the converter efficiency.

SOLUTION

(a) For 25 W average output power and average output current of 1.5 A, the average output voltage is given by

$$V_o = \frac{P_o}{I_o} = \frac{25}{1.5} = 16.7 \text{ V}$$

The load resistance is

$$R = \frac{16.7}{1.5} = 11.13\ \Omega$$

For $V_o = 16.7$ V and $V_{\text{in}} = 28$ V, the duty cycle is

$$D = \frac{16.7}{28} = 0.6$$

(b) The rms value for the output voltage is

$$V_{o,\text{rms}} = \sqrt{D} V_{\text{in}} = 21.69 \text{ V}$$

The ripple factor is given by

$$K_{o,\text{ripple}} = \sqrt{\frac{21.69^2 - 16.7^2}{16.7^2}} = 0.83$$

This circuit results in 83% output voltage ripple, which is by no means acceptable in many dc power supply applications.

(c) Since the switch is ideal, the converter efficiency is 100%, which can be illustrated as follows.

The average output power is given by

$$\begin{aligned} P_o &= \frac{1}{T_s}\int_0^{T_s} v_o i_o \, dt \\ &= \frac{1}{T_s}\int_0^{T_s} \frac{v_o^2}{R} \, dt = \frac{1}{RT_s}\int_0^{DT_s} V_{\text{in}}^2 dt \\ &= \frac{DV_{\text{in}}^2}{R} \end{aligned}$$

and the average input power is given by

$$\begin{aligned} P_{\text{in}} &= \frac{1}{T_s}\int_0^{T_s} V_{\text{in}} i_{\text{in}} \, dt = \frac{V_{\text{in}}}{T_s}\int_0^{DT_s} i_{\text{in}} \, dt \\ &= \frac{V_{\text{in}}}{T_s}\int_0^{DT_s} i_o \, dt = \frac{V_{\text{in}}}{T_s R}\int_0^{DT_s} v_o \, dt \\ &= \frac{DV_{\text{in}}^2}{R} \end{aligned}$$

As expected, the average input and output powers are equal.

EXERCISE 4.2

Repeat Example 4.1 by assuming the switch has a 1.8 V voltage drop across it when conducting.

ANSWER 0.64, 0.75, 93.6%

4.2.1 The Buck Converter

Topology and Basic Operation

Figure 4.9(*a*) and (*b*) shows the circuit configuration for a buck converter with a single- and two-switch implementation. Figure 4.9(*c*) shows the transistor-diode implementation. This topology is known as a buck converter because it steps down the average output voltage below the input voltage.

Throughout this chapter to obtain the steady-state characteristic equations, we will assume that power switching devices and the converter components are lossless. Moreover, the exact steady-state analysis of these converters requires solving second-order nonlinear systems. Such analysis is complex and because of the nature of the output voltage, it is not necessary. Since these converters' function is to produce dc output, the

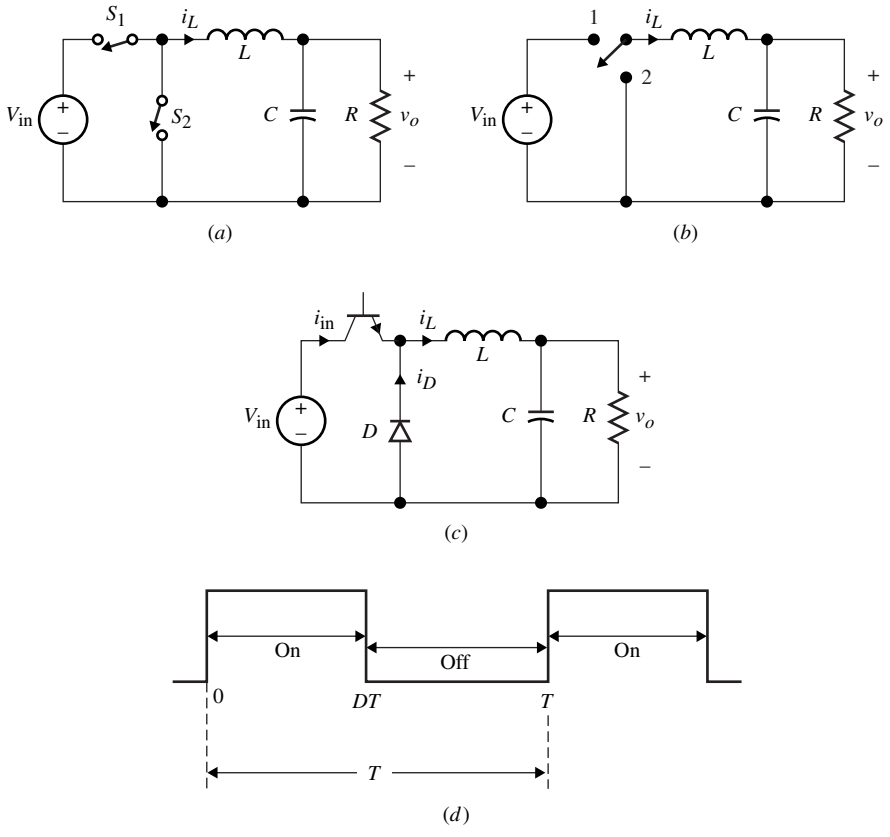


Figure 4.9 The buck (step-down) converter. (*a*) Two-switch implementation. (*b*) Single-pole, double-throw switch implementation. (*c*) Transistor-diode implementation. (*d*) Switching waveform for the power switch.

output voltage $v_o(t)$ consists of the desired dc and the undesired ac components. Practically, the output ripple due to switching is very small (less than 1%) compared to the level of the dc output voltage. As a result, we will assume the output ripple voltage is small and can be neglected when evaluating converter voltage gains, i.e., $v_o = V_o$. In other words, the ripple-free output voltage assumption is made since the output time constant for the filter capacitor and the output resistor, *RC*, is very large. Moreover, the analysis will be based on the converter operating in the steady-state condition, i.e., the converter currents and voltages have reached their steady-state values. These assumptions can be summarized and represented mathematically as follows:

1. Since we assume lossless components and ideal switching devices, the average input power, P_{in}, and the average output power, P_o, are equal:

$$P_{\text{in}} = P_o \tag{4.4}$$

2. Since we assume steady-state operation, the inductor current and the capacitor voltage are periodic over one switching cycle, i.e.,

$$i_L(t_0) = i_L(t_0 + T) \tag{4.5a}$$

$$v_c(t_0) = v_c(t_0 + T) \tag{4.5b}$$

   where t_0 is the initial switching time and T is the switching period.

3. Since we assume ideal capacitors and inductors, the average inductor voltage and the average capacitor current are zero:

$$I_c = \frac{1}{T}\int_{t_0}^{T+t_0} i_c(t)\, dt = 0 \tag{4.6}$$

$$V_L = \frac{1}{T}\int_{t_0}^{T+t_0} v_L(t)\, dt = 0 \tag{4.7}$$

In fact, Eq. (4.7) is a representation of Faraday's law, which states that voltage time during charging equals voltage time during discharging. This is also known as the *volt-second principle*. These two relations suggest that the total energy stored in the capacitor or the inductor over one switching cycle is zero. Finally, throughout the analysis in this chapter, the typical switching waveform for the power devices given in Fig 4.9(*d*) will be used to represent the switching action of the power switch. For simplicity we set the initial switching time to zero, $t_0 = 0$.

Again, *D* is known as the duty ratio or duty cycle, defined in Eq. (4.2). The power transistor is turned on for a period of *DT* and turned off for the remaining time $(1 - D)T$. Depending on whether the switch is turned on or off, the inductor current will be either charging through V_{in} or discharging through the diode, respectively. As a result, there are two modes of operation. We first consider *mode 1,* when the switch is on, shown in Fig. 4.10(*a*).

As shown in the figure, when the switch is on, the input voltage, V_{in}, forces the diode into the reverse bias region. To determine the voltage conversion ratio, the average input and output currents, and the output voltage, we use the inductor current as a state variable in the following equation:

$$\begin{aligned} V_{\text{in}} &= v_L + V_o \\ &= L\frac{di_L}{dt} + V_o \end{aligned} \tag{4.8}$$

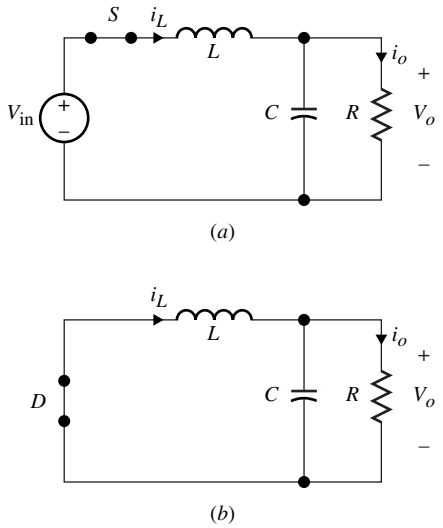


Figure 4.10 Equivalent circuit modes for the buck converter. (*a*) Mode 1: The power switch is on. (*b*) Mode 2: The power switch is off.

Equation (4.8) can be rearranged as follows:

$$\frac{di_L}{dt} = \frac{1}{L}(V_{\text{in}} - V_o) \tag{4.9}$$

Integrating Eq. (4.9) from $t = 0$ to t with $I_L(0)$ as the initial condition, we obtain

$$i_L(t) = \frac{1}{L}(V_{\text{in}} - V_o)t + I_L(0) \tag{4.10}$$

Equation (4.10) suggests that the inductor current charges linearly with a slope of $(V_{\text{in}} - V_o)/L$, where $I_L(0)$ is the initial inductor current value at $t = 0$, when the switch is first turned on. This equation applies as long as the switch is on. However, the equivalent circuit model changes when the power switch is turned off at $t = DT$, resulting in the equivalent circuit of mode 2 shown in Fig. 4.10(*b*), during which the diode is conducting.

As shown in Fig. 4.10(*b*), in order for the inductor current to maintain its continuity, the diode is forced to conduct by becoming forward biased so that the diode "picks up" the current in the direction shown. The diode is known as *flyback* or *free-wheeling* because of the manner in which it is forced to turn on. The resultant equation that describes mode 2 operation is

$$\frac{di_L}{dt} = -\frac{1}{L}V_o \tag{4.11}$$

Integrating both sides of Eq. (4.11) for $t \geq DT$ with $i_L(DT)$ as an initial condition, we obtain

$$i_L(t) = -\frac{V_o}{L}(t - DT) + I_L(DT) \tag{4.12}$$

where $I_L(DT)$ is the initial inductor current when the switch is first turned off.

Equation (4.12) suggests that the inductor current starts discharging at $t = DT$ with the slope of $-V_o/L$, as shown in Fig. 4.11(*a*). In steady-state operation we have

$$I_L(0) = I_L(T) \tag{4.13}$$

Evaluating Eq. (4.10) at $t = DT$ and Eq. (4.12) at $t = T$ and using Eq. (4.13), we obtain the following two relations for $I_L(0)$ and $I_L(DT)$:

$$I_L(DT) = \frac{1}{L}(V_{\text{in}} - V_o)DT + I_L(0) \tag{4.14a}$$

$$I_L(0) = -\frac{V_o}{L}(1 - D)T + I_L(DT) \tag{4.14b}$$

The steady-state current and voltage waveforms are shown in Fig. 4.11. $I_{L\text{max}}$ and $I_{L\text{min}}$ are the inductor current values at the instants the switch is turned off and on, respectively.

Voltage Conversion

Next we use the preceding relations to derive expressions for the voltage conversion, and average input and output currents. From Eqs. (4.14) we obtain

$$\frac{V_o}{V_{\text{in}}} = D \tag{4.15}$$

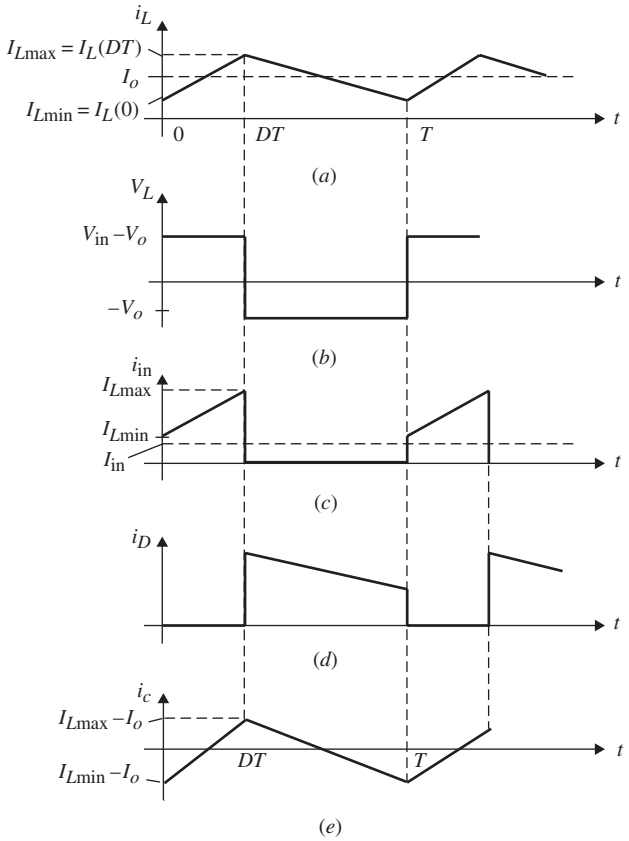


Figure 4.11 Steady-state waveforms for the buck converter: (*a*) inductor current, (*b*) inductor voltage, (*c*) input current, (*d*) diode current, and (*e*) capacitor current.

Hence, the maximum output voltage gain is 1. We should point out that Eq. (4.15) can be obtained easily by using the volt-second principle across the inductor, which is given as follows:

$$\overbrace{(\text{Inductor voltage})(\text{time})}^{\substack{\text{Mode 1}\\(\text{interval } DT)}} + \overbrace{(\text{Inductor voltage})(\text{time})}^{\substack{\text{Mode 2}\\(\text{interval } (1-D)T)}} = 0$$

$$v_L(t)DT + v_L(t)(1-D)T = 0 \tag{4.16}$$

where v_L equals $(V_{\text{in}} - V_o)$ and $-V_o$ during time intervals DT and $(1-D)T$, respectively.

We can make two observations on the buck voltage gain equation $V_o = DV_{\text{in}}$. First, since all the converter components (*L, C, D, Q*) are ideal, they don't dissipate any power, resulting in 100% voltage efficiency. Second, the average input and output voltage ratio has a linear control characteristic curve, as shown in Fig. 4.12. By varying the value of the duty cycle, *D*, we can control the average output voltage to the desired level.

Average Input and Output Currents

The input current, i_{in}, as illustrated in Fig. 4.11(*c*), with an average value of I_{in}, is given by

$$I_{\text{in}} = \frac{1}{T}\int_0^T i_{\text{in}}(t)\, dt \tag{4.17}$$

Since $i_{\text{in}} = i_L$ in mode 1, we substitute for $i_L(t)$ from Eq. (4.10), and by evaluating the integral between $t = 0$ and $t = DT$, we obtain

$$I_{\text{in}} = \frac{1}{2L}(V_{\text{in}} - V_o)D^2T + I_L(0)D \tag{4.18}$$

Using Eq. (4.14*b*), we obtain

$$I_{\text{in}} = \frac{1}{2}(I_{L\max} + I_{L\min})D \tag{4.19}$$

where $I_{L\max}$ and $I_{L\min}$ represent $I_L(DT)$ and $I_L(0)$, respectively.

Similarly, by inspection, the average output current is given by

$$I_o = I_L = \frac{I_{L\min} + I_{L\max}}{2} = \frac{V_o}{R} \tag{4.20}$$

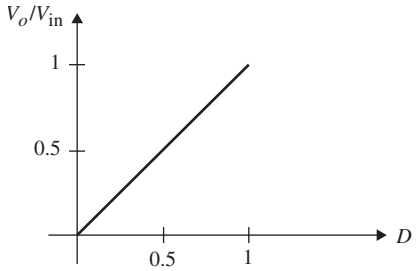


Figure 4.12 Ideal output control characteristic curve for the buck converter.

From Eqs. (4.14) and (4.20) we can solve for the maximum and minimum inductor currents, to obtain

$$I_{L\max} = DV_{\text{in}}\left(\frac{1}{R} + \frac{(1-D)T}{2L}\right) \tag{4.21}$$

$$I_{L\min} = DV_{\text{in}}\left(\frac{1}{R} - \frac{(1-D)T}{2L}\right) \tag{4.22}$$

Substituting these equations in Eqs. (4.19) and (4.20), we obtain

$$I_o = \frac{DV_{\text{in}}}{R}$$

$$I_{\text{in}} = \frac{D^2V_{\text{in}}}{R}$$

Hence, the current gain is given by

$$\frac{I_o}{I_{\text{in}}} = \frac{1}{D} \tag{4.23}$$

This relation can be obtained by equating the average input and output power, to yield

$$I_{\text{in}}V_{\text{in}} = I_oV_o$$

$$\frac{I_{\text{in}}}{I_o} = \frac{V_o}{V_{\text{in}}} = D$$

From Eqs. (4.15) and (4.23), it is clear that the current and voltage relations for the converter are equivalent to a dc transformer model with a ratio of D, as shown in Fig. 4.13. The sinusoidal curve and straight line drawn across the transformer windings indicate that the transformer is capable of transferring ac and dc, respectively.

Critical Inductor Value

It is clear that for $I_{L\min} \neq 0$, the converter will operate in the *continuous conduction mode (ccm).* To find the minimum inductor value that is needed to keep the converter in the ccm, we set $I_{L\min}$ to zero and solve for L:

$$I_{L\min} = DV_{\text{in}}\left(\frac{1}{R} - \frac{(1-D)T}{2L}\right) = 0$$

$$L_{\text{crit}} = \left(\frac{1-D}{2}\right)TR \tag{4.24}$$

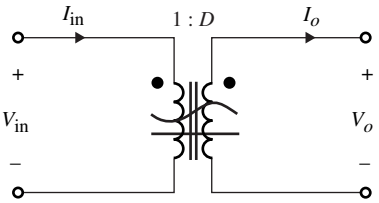


Figure 4.13 Equivalent circuit representation for the buck converter, referred to as a dc-dc transformer.

where L_{crit} is the critical inductance minimum value for a given D, T, and R before the converter enters the discontinuous conduction mode (dcm) of operation.

Output Voltage Ripple

Since we have assumed that the output voltage has no ripple, the entire ac output current from the inductor passes through the parallel capacitor, and only dc current is delivered to the load resistor. In practice, the value of the output capacitor is an important design parameter since it influences the overall size of the dc-to-dc converter and how much of the switching frequency ripple is being removed. Having said that, it is design practice to choose a larger output capacitor in order to limit the ac ripple across V_o. Theoretically speaking, if $C \longrightarrow \infty$, the capacitor acts like a short circuit to the ac ripple, resulting in zero output voltage ripple. If we assume C is finite, then there exists a voltage ripple superimposed on the average output voltage. In order to derive an expression for the capacitor ripple voltage, we first obtain an expression for the capacitor current, which is given by the following relation:

$$i_c(t) = i_L(t) - I_o$$

As a result, the initial capacitor current at $t = 0$ is given by

$$\begin{aligned} I_c(0) &= I_L(0) - I_o \\ &= -\frac{I_{L\max} - I_{L\min}}{2} \end{aligned}$$

and at $t = DT$,

$$\begin{aligned} I_c(DT) &= I_L(DT) - I_o \\ &= +\left(\frac{I_{L\max} - I_{L\min}}{2}\right) \end{aligned}$$

The resultant capacitor current and voltage are shown in Fig. 4.14.

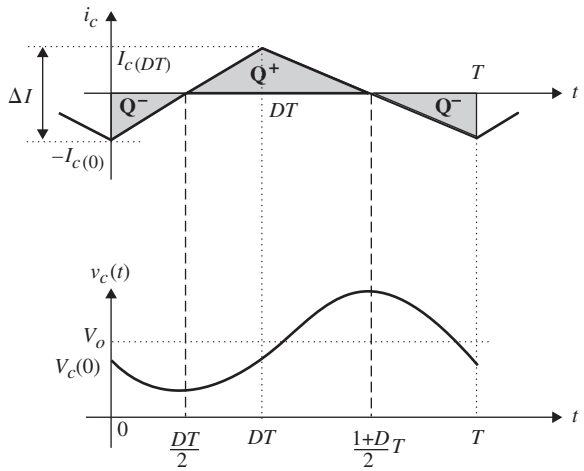


Figure 4.14 Capacitor current and voltage waveforms.

The instantaneous capacitor current can be expressed in terms of ΔI from Eqs. (4.21) and (4.22), as shown in the following equations:

$$i_c(t) = \frac{I_{L\max} - I_{L\min}}{DT}t - \frac{I_{L\max} - I_{L\min}}{2} = \frac{\Delta I}{DT}t - \frac{\Delta I}{2} \qquad 0 \le t < DT \quad (4.25a)$$

$$i_c(t) = -\frac{I_{L\max} - I_{L\min}}{(1-D)T}(t - DT) + \frac{I_{L\max} - I_{L\min}}{2}$$

$$= \frac{-\Delta I}{(1-D)T}(t - DT) + \frac{\Delta I}{2} \qquad 0 \le t < DT \quad (4.25b)$$

where $\Delta I = (V_{\text{in}}(1-D)TD)/L$.

From the capacitor voltage-current relation, $i_c = C(dv_c/dt)$, the capacitor voltage, $v_{c1}(t)$, can be expressed by the following integral for $t \ge 0$:

$$v_{c1}(t) = \frac{1}{C}\int_0^t i_c \, dt + V_c(0)$$

where $V_c(0)$ is the initial capacitor voltage at $t = 0$. Substituting for $i_c(t)$ from Eq. (4.25*a*), we obtain the following equation:

$$v_{c1}(t) = \frac{1}{C}\int_0^t \left(\frac{\Delta I}{DT}t - \frac{\Delta I}{2} \right) dt + V_c(0)$$

Evaluating this integral yields

$$v_{c1}(t) = \frac{1}{C}\frac{\Delta I}{DT}\frac{t^2}{2} - \frac{\Delta I}{2C}t + V_c(0) \qquad 0 \le t < DT \quad (4.26)$$

Similarly, for $t \ge DT$, the capacitor voltage is given by

$$v_{c2}(t) = \frac{1}{C}\int_{DT}^t i_c \, dt + V_c(DT)$$

where $V_c(DT)$ is the initial capacitor voltage when the switch is turned off at $t = DT$. From Eq. (4.27) $v_{c2}(t)$ is given by

$$v_{c2}(t) = \frac{-\Delta I}{C(1-D)T}\frac{(t - DT)^2}{2} + \frac{\Delta I}{2C}(t - DT) + V_c(DT) \qquad DT \le t < T \quad (4.27)$$

Since the capacitor voltage is in the steady state, we have $v_{c1}(t = DT) = v_{c2}(t = DT)$ and $v_{c1}(0) = v_{c2}(T)$, resulting in the following boundary conditions for the capacitor voltage:

$$V_c(T) = V_c(DT) = V_c(0)$$

Since the average capacitor voltage is V_o, then we have in general

$$V_o = \frac{1}{T}\left[\int_0^{DT} v_{c1}(t) \, dt + \int_{DT}^T v_{c2}(t) \, dt \right]$$

Substituting for v_{c1} and v_{c2} from Eqs. (4.26) and (4.27), we obtain

$$V_o = \frac{\Delta I}{12C}(1 - 2D)T + V_c(0) \quad (4.28)$$

Substitute for $\Delta I = (DV_{\text{in}}(1-D)T)/L$ in Eq. (4.28) to yield

$$V_c(0) = DV_{\text{in}}\left[1 - \frac{(1-D)(1-2D)}{12CL}T^2\right] \tag{4.29}$$

Hence, the capacitor initial values at $t = 0$ and $t = DT$ are equal, as expected since the capacitor current is symmetrical. Since the peak capacitor voltage occurs when the inductor current is zero, we have the capacitor minimum voltage occurring at $t = DT/2$, which is obtained from Eq. (4.26):

$$\begin{aligned} V_{c,\min} &= \frac{1}{C}\frac{\Delta I}{2DT}\left(\frac{DT}{2}\right)^2 - \frac{\Delta I}{2C}\left(\frac{DT}{2}\right) + V_c(0) \\ &= -\frac{\Delta I}{8C}DT + V_c(0) \end{aligned} \tag{4.30a}$$

and the maximum capacitor voltage occurring at $t = (1+D)T/2$ as obtained from Eq. (4.27):

$$\begin{aligned} V_{c,\max} &= -\frac{\Delta I}{2C(1-D)T}\left(\frac{(1+D)}{2}T - DT\right)^2 + \frac{\Delta I}{2C}\left(\frac{(1+D)}{2}T - DT\right) + V_c(DT) \\ &= \frac{\Delta I}{8C}(1-D) + V_c(DT) \end{aligned} \tag{4.30b}$$

Substituting for $V_c(0)$ from Eq. (4.29) and using $\Delta I = (DV_{\text{in}}(1-D)T)/L$, it can be shown that $V_{c,\min}$ and $V_{c,\max}$ are expressed as follows:

$$V_{c,\min} = V_o\left[1 - \frac{(1-D)(2-D)}{24CL}T^2\right] \tag{4.31a}$$

$$V_{c,\max} = V_o\left[1 + \frac{(1-D^2)}{24CL}T^2\right] \tag{4.31b}$$

Hence, the variation in the capacitor peak voltage is given by

$$\Delta V_c = V_{c,\max} - V_{c,\min}$$

and from Eqs. (4.31) we obtain

$$\Delta V_c = \frac{V_o}{8LCf^2}(1-D)$$

Sometimes it is useful to express the ratio of the ripple to the output voltage,

$$\frac{\Delta V_c}{V_0} = \frac{1-D}{8LCf^2} \tag{4.32}$$

This term is known as the output voltage ripple and represents the regulation. As expected, when the filtering capacitor and the frequency increase, the voltage ripple decreases.

Using Capacitor Charge to Evaluate ΔV_c

Another useful way to evaluate the expression for ΔV_c without having to obtain the exact expression for $v_c(t)$ is to use the total charge, Q, deposited on the capacitor current interval. Figure 4.14 shows the waveform for i_c and v_c with areas of positive

charge (+) and negative charge (–). Because of waveform symmetry, $t = DT/2$ and $t = (1 + D)T/2$ represent the i_c zero crossing times when the capacitor voltage is minimum, $V_{c,\min}$, and maximum, $V_{c,\max}$, respectively. Hence, the capacitor voltage ripple is ΔV_c. The total charge stored in the capacitor between $t = DT/2$ and $t = (1 + D)T/2$ is obtained from the following equation:

$$\frac{dQ}{dt} = C\frac{dv_c}{dt}$$

So the total charge Q between capacitor current i_c zero crossings $(DT/2 \le t < (1 + D)T/2)$ is given by

$$\Delta Q = C\Delta V_c \tag{4.33}$$

However, since the total charge is related to the current according to the relation

$$i = \frac{dQ}{dt}$$

then we have

$$\begin{aligned}\Delta Q &= \frac{1}{T/2}\int_{DT/2}^{(1+D)T/2} i\,dt = \text{Area under the curve} \\ &= \frac{1}{2}\left(\frac{1+D}{2}T - \frac{D}{2}T\right)\frac{1}{2}\Delta I \\ &= \frac{1}{2}\frac{T}{2}\frac{1}{2}\Delta I\end{aligned} \tag{4.34}$$

From Eqs. (4.33) and (4.34), we obtain

$$\Delta V_c = \frac{T}{8C}\Delta I$$

Substituting for $\Delta I = (DV_{\text{in}}(1 - D)T)/L$, we obtain

$$\begin{aligned}\frac{\Delta V_c}{V_o} &= \frac{1-D}{8LC}T^2 \\ &= \frac{1-D}{8LCf^2}\end{aligned} \tag{4.35}$$

EXAMPLE 4.2

Consider a buck converter with the following circuit parameters: $V_{\text{in}} = 20$ V, $V_o = 15$ V, and $I_o = 5$ A, for $f = 50$ kHz. Determine: (*a*) D, (*b*) L_{crit}, (*c*) maximum and minimum inductor currents for $L = 100L_{\text{crit}}$, (*d*) average input and output power, and (*e*) capacitor voltage ripple for $C = 0.47\ \mu$F.

SOLUTION

(a) $D = 0.75$

(b) Using $R = 3\ \Omega$ and $T = 20\ \mu$s, the critical inductor value is given by

$$L_{\text{crit}} = \left(\frac{1-D}{2}\right)TR = 7.5\ \mu\text{H}$$

(c) For $L = 100L_{\text{crit}} = 750\ \mu\text{H} = 0.75\ \text{mH}$, we have

$$I_{L\min} = DV_{\text{in}}\left(\frac{1}{R} - \frac{(1-D)T}{2L}\right)$$

$$= (0.75)(20)\left(\frac{1}{3} - 3.33\times 10^{-3}\right)$$

$$I_{L\min} = 4.95\ \text{A}$$

$$I_{L\max} = (0.75)(20)\left(\frac{1}{3} + 3.33\times 10^{-3}\right)$$

$$I_{L\max} = 5.05\ \text{A}$$

(d) Since it is an ideal converter, the average output and input powers are given by

$$P_{\text{in}} = P_o = V_o I_o = (15)(5) = 75\ \text{W}$$

(e) The capacitor voltage ripple is given by

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2}$$

$$= \frac{(1-0.75)}{8(0.75\ \text{mH})(0.47\ \mu\text{F})(50\times 10^3)^2}$$

$$\frac{\Delta V_o}{V_o} = 0.035 = 3.5\%$$

EXAMPLE 4.3

Design a buck converter with the following specifications: $\Delta V_0/V_o = 0.5\%$, $V_{\text{in}} = 20\ \text{V}$, $P_o = 12\ \text{W}$, $f = 30\ \text{kHz}$, and $D = 0.4$.

SOLUTION In order to design this converter, we need to calculate the values for *L*, *C*, and *R*. The output voltage is given by

$$V_o = DV_{\text{in}} = 8\,\text{V}$$

Hence, the output current is

$$I_o = \frac{P_o}{V_o} = 1.5\ \text{A}$$

The output resistance is

$$R = \frac{8}{1.5} = 5.33\ \Omega$$

The critical inductance for ccm is given by

$$L_{\text{crit}} = \frac{1-D}{2}TR$$

$$= \left(\frac{1-0.4}{2}\right)\left(\frac{1}{30\times 10^3}\right)5.33$$

$$= 53.3\ \mu\text{H}$$

Let us select $L = 600\ \mu$H. Based on this value, the maximum and minimum inductor currents are given by

$$I_{L\max} = DV_{\text{in}}\left(\frac{1}{R} + \frac{(1-D)T}{2L}\right)$$

$$= (0.4)(20)\left(\frac{1}{5.33} + 0.0167\right)$$

$$= 1.63 \text{ A}$$

$$I_{L\min} = (0.4)(20)\left(\frac{1}{5.33} - 0.0167\right)$$

$$= 1.37 \text{ A}$$

The ripple voltage is given by

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2} = 0.005$$

Solving for C,

$$C = \frac{1-D}{(8Lf^2)0.005}$$

$$C = 27.78\ \mu\text{F}$$

EXERCISE 4.3

Redesign Example 4.2 to achieve an output ripple voltage not to exceed 1% and an inductor current ripple not to exceed 10% at the average load current.

ANSWER 0.15 mH, 8.33 μF, 3 Ω

EXERCISE 4.4

Determine the diode and transistor average and rms current values for Exercise 4.3.

ANSWER 1.25 A, 3.75 A, 2.5 A, 4.33 A

EXERCISE 4.5

Show that the expression for the peak capacitor voltage at $t = (1 + D)T/2$ is as given by Eq. (4.31*b*).

4.2.2 The Boost Converter

Basic Topology and Voltage Gain

Other possible switch and transistor-diode arrangements are shown in Fig. 4.15(*a*) and (*b*), respectively. This topology is known as a boost converter since the output voltage is higher than the input, as will be shown in this section.

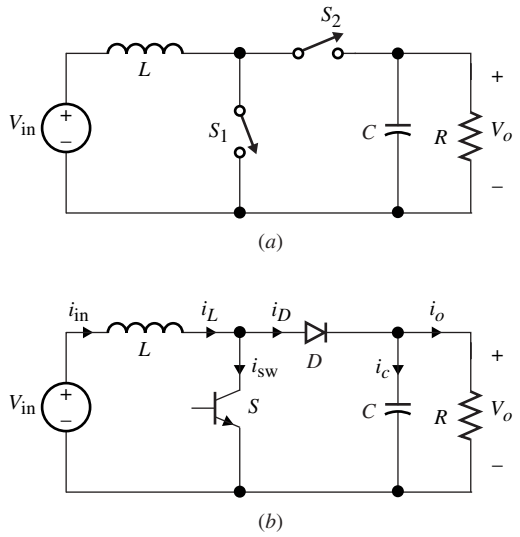


Figure 4.15 Boost converter. (*a*) Two-switch implementation. (*b*) Transistor-diode implementation.

Similar to the case for the buck converter, we assume all the converter components are ideal and the transistor switching waveform is as shown in Fig. 4.9(*d*). When the switch is turned on, the equivalent circuit of mode 1 is shown in Fig. 4.16(*a*). This is a charging interval, and the voltage across the inductor is V_{in}, and $i_L(t)$ is given by

$$i_L(t) = \frac{1}{L}V_{\text{in}}t + I_L(0) \qquad 0 \le t < DT \tag{4.36}$$

where $I_L(0)$ is the initial inductor current value at $t = 0$. When the switch is turned off at $t = DT$, the resultant equivalent mode 2 circuit is shown in Fig. 4.16(*b*).

The inductor voltage is $V_{\text{in}} - V_o$, and $i_L(t)$ is given by

$$i_L(t) = \frac{1}{L}(V_{\text{in}} - V_o)(t - DT) + I_L(DT) \qquad DT \le t < T \tag{4.37}$$

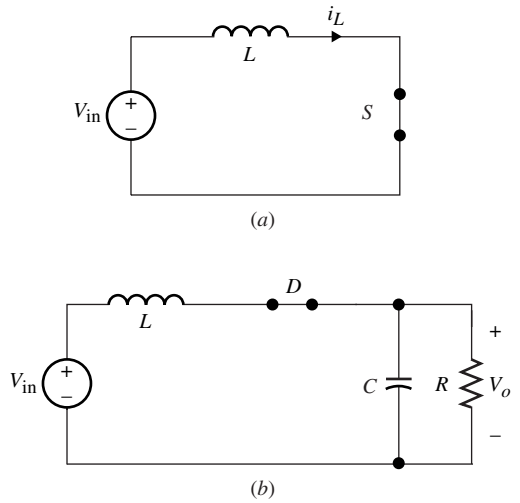


Figure 4.16 Equivalent circuit modes for the boost converter. (*a*) Mode 1: The switch is on. (*b*) Mode 2: The switch is off.

Evaluating Eqs. (4.36) and (4.37) at $t = DT$ and $t = T$, respectively, and using the fact that $I_L(T) = I_L(0)$, we obtain

$$I_L(DT) - I_L(0) = \frac{1}{L} V_{\text{in}}(DT) \tag{4.38a}$$

$$I_L(DT) - I_L(0) = -\frac{1}{L}(V_{\text{in}} - V_o)(1 - D)T \tag{4.38b}$$

From Eqs. (4.38*a*) and (4.38*b*), the resulting voltage conversion is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1 - D} \tag{4.39}$$

Hence, the voltage gain is always greater than 1. Also from Eqs. (4.38), the inductor ripple current is given by

$$\begin{aligned} \Delta I &= I_L(DT) - I_L(0) \\ &= I_{L\max} - I_{L\min} \\ &= \frac{1}{L} V_{\text{in}} DT \end{aligned} \tag{4.40a}$$

Substituting for V_{in} from Eq. (4.39), we obtain

$$\Delta I = \frac{1}{L} V_o D(1 - D)T \tag{4.40b}$$

Key current and voltage waveforms are given in Fig. 4.17.

Average Input and Output Currents

The input current is the same as the inductor current as shown in Fig. 4.17(*a*). Hence, the average input current by inspection is given by

$$I_{\text{in}} = \frac{I_{L\max} + I_{L\min}}{2} \tag{4.41}$$

The average output current is the same as the average diode current and is given by

$$I_o = \left(\frac{I_{L\max} + I_{L\min}}{2}\right)(1 - D) = \frac{V_o}{R} \tag{4.42}$$

Since we assume an ideal converter, the average input and output powers must be equal. Using Eqs. (4.41) and (4.42), we get

$$V_{\text{in}} I_{\text{in}} = V_o I_o$$

resulting in

$$\frac{I_{\text{in}}}{I_o} = \frac{V_o}{V_{\text{in}}} = \frac{1}{1 - D} \tag{4.43}$$

As with the buck converter, the input-output current and voltage ratios are equivalent to a dc transformer with a transformer mode ratio equal to $1/(1 - D)$, as shown in Fig. 4.18.

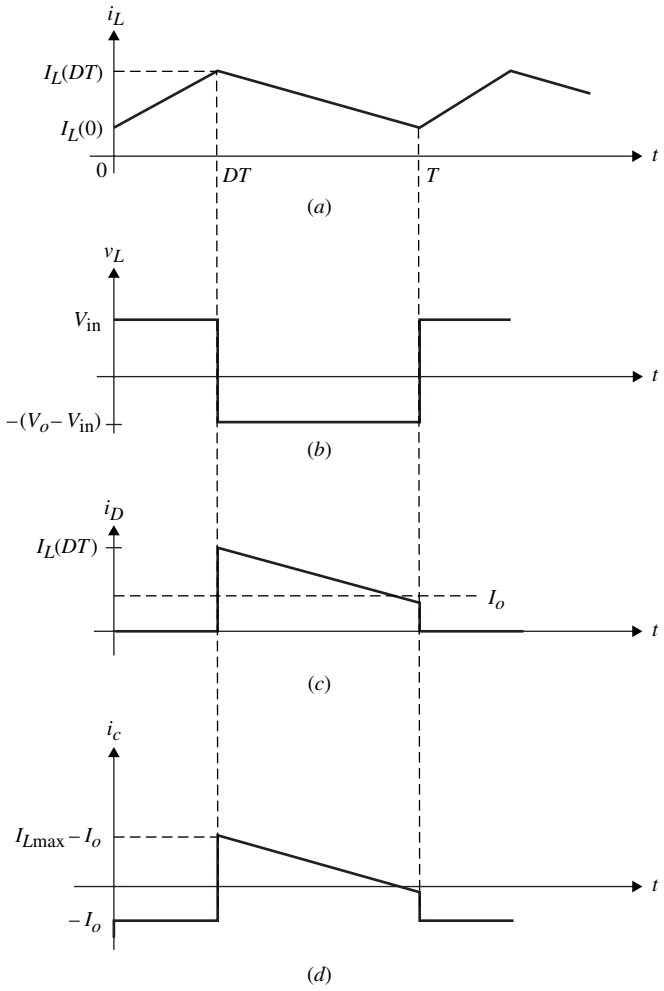


Figure 4.17 Current and voltage waveforms for the boost converter.

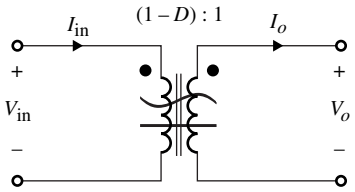


Figure 4.18 Equivalent transformer circuit representation for the boost converter.

Using Eqs. (4.38) and (4.42), we can solve for the maximum and minimum inductor current values:

$$I_L(0) = I_{L\min} = V_{\text{in}}\left(\frac{1}{R(1-D)^2} - \frac{DT}{2L}\right) \tag{4.44a}$$

$$I_L(DT) = I_{L\max} = V_{\text{in}}\left(\frac{1}{R(1-D)^2} + \frac{DT}{2L}\right) \tag{4.44b}$$

For positive values of $I_{L\max}$ and $I_{L\min}$, the converter will operate in the continuous conduction mode. To solve for the minimum critical inductor value that will keep the converter in the ccm, we set $I_{L\min}$ to zero:

$$I_{L\min} = 0$$

Under this boundary condition, the critical inductor value is given by

$$L_{\text{crit}} = \frac{RT}{2}(1-D)^2 D \tag{4.45}$$

Output Ripple Voltage

It is clear from Fig. 4.17 that when the diode is reverse biased, the capacitor current is the same as the load current. Since we assume the load current is purely dc, the capacitor current is given by

$$i_c = -I_o \qquad 0 \le t < DT$$
$$i_c = i_L - I_o \qquad DT \le t < T$$

The capacitor current waveform is shown in Fig. 4.17(*d*) and redrawn in Fig. 4.19 along with the capacitor voltage waveform. Mathematical expressions for i_c can be obtained directly from this figure.

The current $i_c(t)$ is expressed mathematically as

$$i_c(t) = -\frac{\Delta I}{(1-D)T}(t - DT) + I_c(DT) \qquad DT \le t \le T \tag{4.46}$$

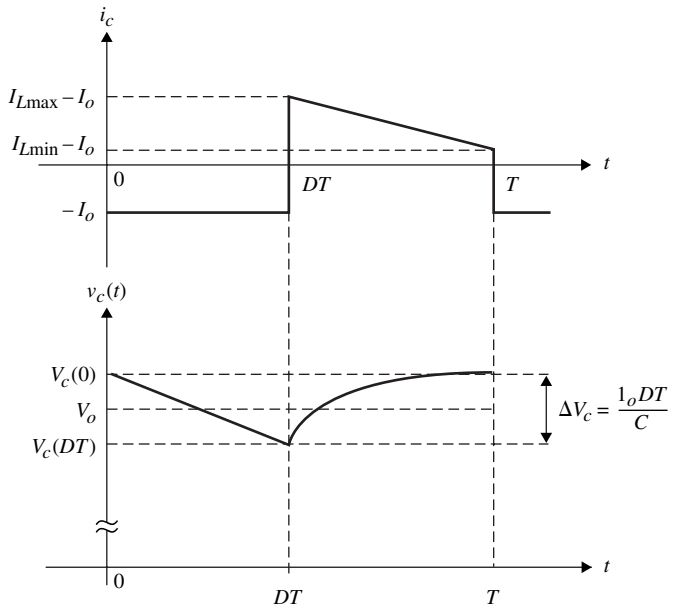


Figure 4.19 Capacitor current and voltage waveforms for the boost converter, assuming $I_{L\min} > I_o$.

where $I_c(DT)$ is the initial $i_c(t)$ at $t = DT$. The capacitor voltage for $0 \le t < DT$ is given by

$$\begin{aligned} v_c(t) &= \frac{1}{C}\int_0^t -I_o\, dt + V_c(0) \\ &= -\frac{I_o}{C}t + V_c(0) \end{aligned} \tag{4.47}$$

where $V_c(0)$ is the initial capacitor voltage at $t = 0$.

At $t = DT$ we have

$$V_c(DT) = -\frac{I_o}{C}DT + V_c(0) \tag{4.48}$$

Since the average capacitor voltage is V_o, we can solve for $V_c(0)$ and $V_c(DT)$ as follows:

$$\begin{aligned} V_c(0) &= V_o + \frac{I_o DT}{2C} \\ V_c(DT) &= V_o - \frac{I_o DT}{2C} \end{aligned} \tag{4.49}$$

and the capacitor voltage variation is given by

$$\Delta V_c = V_c(0) - V_c(DT) = \frac{I_o DT}{C} \tag{4.50}$$

For $DT \le t < T$ the capacitor voltage is given by

$$\begin{aligned} v_c(t) &= \frac{1}{C}\int_{DT}^{T}\left[\frac{-\Delta I}{(1-D)T}(t-DT) + I_c(DT)\right]dt + V_c(DT) \\ &= -\frac{\Delta I}{2C(1-D)T}(t-DT)^2 + \frac{I_c(DT)(1-D)T}{C} + V_c(DT) \end{aligned} \tag{4.51}$$

The output ripple voltage is given by

$$|\Delta V_o| = |\Delta V_c| = I_o\frac{DT}{C} = \frac{V_o DT}{RC}$$

Then the voltage ripple is given by

$$\begin{aligned} \frac{\Delta V_o}{V_o} &= \frac{DT}{RC} \\ &= \frac{D}{RCf} \end{aligned} \tag{4.52}$$

EXAMPLE 4.4

Sketch the current waveforms for i_L, i_{in}, i_D, i_o, and i_c for the boost converter with the following parameters: $L = 1.8$ mH, $V_{\text{in}} = 50$ V, $V_o = 120$ V, $R = 20\ \Omega$, $C = 147\ \mu$F, and $f = 15$ kHz. Also sketch the voltage waveforms for v_L, v_{sw}, v_c, and v_D.

SOLUTION In order to sketch the waveforms, we need to find *D*, the maximum and minimum inductor currents, and the average output current.

The duty cycle is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} = \frac{120}{50}$$

which yields $D = 0.58$

Using $R = 20\ \Omega$ and $T = 66.67\ \mu\text{s}$, the maximum and minimum inductor currents are given by

$$I_{L\max} = V_{\text{in}}\left(\frac{1}{(1-D)^2 R} + \frac{DT}{2L}\right) = 14.94\ \text{A}$$

and

$$I_{L\min} = V_{\text{in}}\left(\frac{1}{(1-D)^2 R} - \frac{DT}{2L}\right) = 13.86\ \text{A}$$

The average input and output currents are given by

$$I_{\text{in}} = \frac{I_{L\max} + I_{L\min}}{2} = 14.4\ \text{A}$$

$$I_o = I_{\text{in}}(1-D) = 6\ \text{A}$$

The capacitor peak currents are given by

$$I_{c\max} = I_{L\max} - I_o = 8.94\ \text{A}$$

$$I_{c\min} = I_{L\min} - I_o = 7.86\ \text{A}$$

Hence,

$$\Delta I_c = (I_{c\max} - I_{c\min}) = 1.074\ \text{A}$$

Notice this value must be equal to ΔI_L.

The capacitor voltage is given by

$$v_c(t)\big|_{t=0} = 120\ \text{V}$$

$$v_c(t)\big|_{t=DT} = \frac{-I_o}{C}DT + 120\ \text{V}$$

$$= \frac{-5.95\ \text{A}}{147\,\mu\text{F}}(0.58)(66.67\,\mu\text{s}) + 120\ \text{V} = 118.43\ \text{V}$$

Hence, the ripple is 1.57 V.

EXAMPLE 4.5

Design a boost converter with the following specifications: $P_o = 27$ W, $V_o = 40$ V, $V_{\text{in}} = 28$ V, $\Delta V_o / V_o = 2\%$, $f_s = 35$ kHz.

SOLUTION First let's determine the duty cycle, *D*:

$$D = 1 - \frac{V_{\text{in}}}{V_o} = 1 - \frac{28}{40} = 0.3$$

For continuous conduction mode, the inductance minimum value is given by

$$L_{\text{crit}} = \frac{RT}{2}(1-D)^2 D$$

where

$$T = 28.57\ \mu\text{s}$$

$$R = \frac{V_o^2}{P_o} = \frac{(40)^2}{27} = 59.26\ \Omega$$

$$L_{\text{crit}} = 124.44\ \mu\text{H}$$

We choose $L = 200\ \mu\text{H}$ since L should be greater than L_{crit} for ccm operation.

The output ripple voltage is

$$\frac{\Delta V_o}{V_0} = \frac{D}{RCf}$$

$$0.02 = \frac{0.3}{(59.26)C(35\ \text{kHz})}$$

$$C = 7.23\ \mu\text{F}$$

EXERCISE 4.6

Determine the average and rms current values for the diode and transistor in Example 4.4.

ANSWER 8.4 A, 11 A, 6 A, 9.28 A

4.2.3 The Buck-Boost Converter

The third possible converter type is obtained by interchanging the diode and the inductor of the buck converter to realize the design of Fig. 4.20. This converter is known as a *buck-boost converter* since its voltage gain can be less than, equal to, or

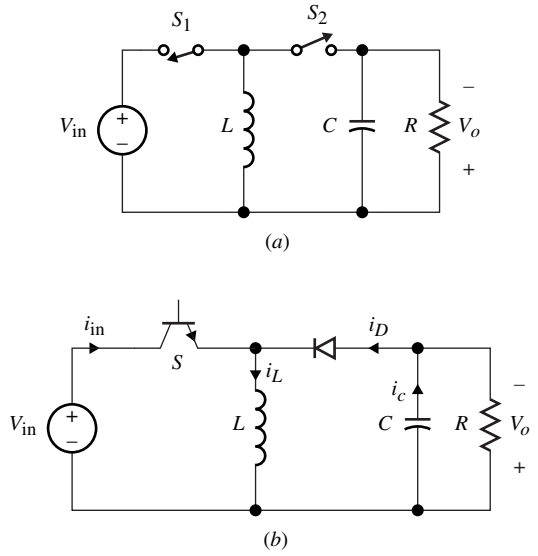


Figure 4.20 Buck-boost converter. (*a*) Switch implementation. (*b*) Transistor-diode implementation.

greater than 1. Unlike the buck and boost converters, this converter gives a negative output voltage when used without isolation.

In this analysis, we follow assumptions made in performing the steady-state analysis for the buck and boost topologies. When the switch is on, the diode is reverse biased with the equivalent circuit of mode 1 as shown in Fig. 4.20(*a*); Fig. 4.21(*b*) gives the equivalent circuit for mode 2 when the transistor is off.

When the transistor is turned on, the inductor current starts charging from the source voltage, V_{in}, while the diode D is reverse biased. The voltage across the inductor is V_{in}, and i_L is given by

$$i_L(t) = \frac{1}{L}V_{\text{in}}(t) + I_L(0) \tag{4.53}$$

where $I_L(0)$ is the initial inductor value that corresponds to the minimum inductor current value. Evaluating Eq. (4.53) at $t = DT$, when the switch is turned off, we obtain the maximum inductor current. This yields the following relation:

$$I_{L\max} - I_{L\min} = \frac{1}{L}V_{\text{in}}DT \tag{4.54}$$

Similarly, in mode 2 the inductor current is given by

$$i_L(t) = -\frac{V_o}{L}(t - DT) + I_L(DT) \tag{4.55}$$

Evaluating Eq. (4.55) at $t = T$, and since we assume steady-state operation, we use $I_L(0) = I_L(T)$ to obtain

$$I_L(0) = \frac{V_o}{L}(T - DT) + I_L(DT) \tag{4.56a}$$

$$I_{L\max} - I_{L\min} = \frac{V_o}{L}(1 - D)T \tag{4.56b}$$

Equating Eqs. (4.54) and (4.56*b*), we obtain the following voltage conversion ratio:

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{1 - D} \tag{4.57}$$

It is clear from this equation that the output voltage can be either smaller or greater than the input voltage:

$D > 0.5$ Boost

$D < 0.5$ Buck

$D = 0.5$ Unity gain

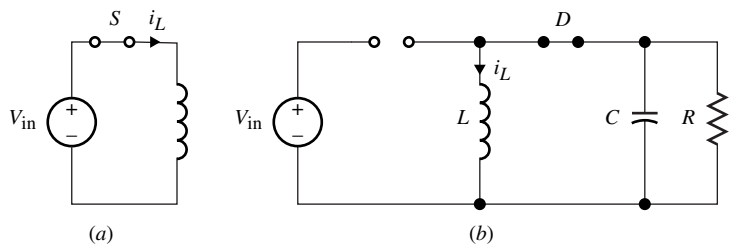


Figure 4.21 Equivalent circuits. (*a*) Mode 1: The transistor is conducting. (*b*) Mode 2: The transistor is not conducting.

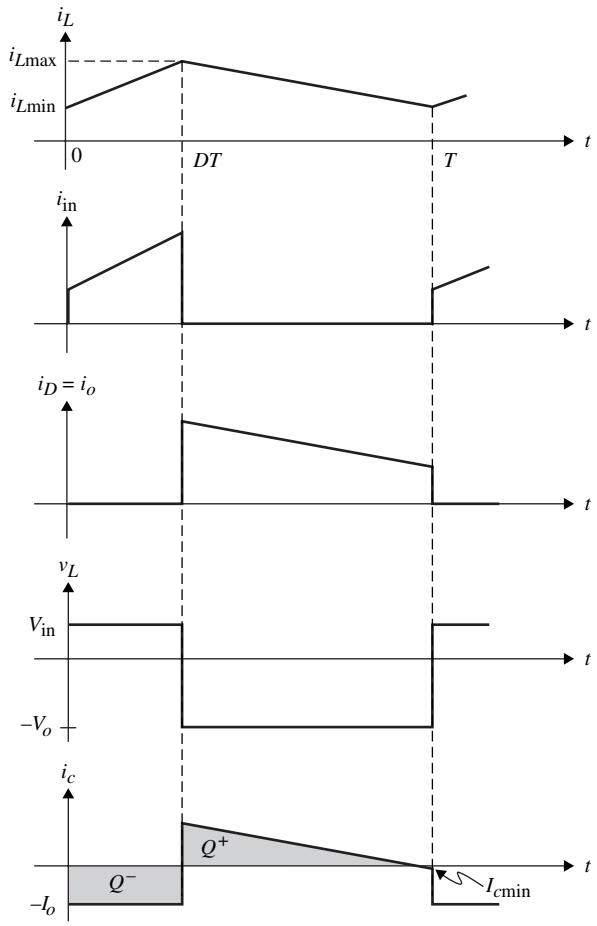


Figure 4.22 Current and voltage waveforms for the buck-boost converter.

Figure 4.22 gives typical current and voltage waveforms for the buck-boost converter. From Fig. 4.22, it is clear that the average input current is given by

$$I_{\text{in}} = \frac{I_{L\max} + I_{L\min}}{2} D \tag{4.58a}$$

and the average output current is given by

$$I_o = \frac{I_{L\max} + I_{L\min}}{2} (1 - D) \tag{4.58b}$$

Since the conservation of power must hold, we use $I_{\text{in}} V_{\text{in}} = I_o V_o$ to obtain

$$\frac{I_{\text{in}}}{I_o} = \frac{V_o}{V_{\text{in}}} = \frac{D}{1 - D} \tag{4.59}$$

To solve for $I_{L\max}$ and $I_{L\min}$ in terms of the converter components, we substitute for $I_o = V_o / R$. Hence, from Eqs. (4.56) and (4.58*b*) we obtain

$$I_{L\max} = V_{\text{in}} \left[\frac{D}{R(1 - D)^2} + \frac{DT}{2L} \right] \tag{4.60a}$$

$$I_{L\min} = V_{\text{in}}\left[\frac{D}{R(1-D)^2} - \frac{DT}{2L}\right] \tag{4.60b}$$

The critical inductor value that keeps the converter in the dcm mode can be obtained by setting $I_{L\min} = 0$ in the above equation to yield

$$L_{\text{crit}} = \frac{RT(1-D)^2}{2} \tag{4.61}$$

We notice that for the same frequency of operation and load resistance, the buck converter has the highest critical inductor limit when compared to the boost and buck-boost, whereas the boost converter has the smallest L_{crit}, resulting in a wider range of inductor design.

Output Voltage Ripple

It can be shown that the capacitor current of the buck-boost converter is the same as that of the boost. Hence, the capacitor voltage is given by

$$\begin{aligned} \Delta V_c(t) &= \frac{V_o DT}{RC} \\ \frac{\Delta V_o}{V_o} &= \frac{DT}{RC} = \frac{D}{RCf} \end{aligned} \tag{4.62}$$

EXAMPLE 4.6

(*a*) Sketch the current and voltage waveforms for a buck-boost converter with the following parameters: $V_{\text{in}} = 40$ V, $V_o = 60$ V, $D = 0.6$, $R = 20\ \Omega$, $L = 750\ \mu$H and $T_s = 200\ \mu$s. (*b*) Find the rms value for i_c.

SOLUTION

(a) Let $T = 200\ \mu$s.

$$D = \frac{1}{1 + \frac{V_{in}}{V_o}} = \frac{1}{1 + \frac{40}{60}} = 0.6$$

$$\begin{aligned} I_{L\max} &= \frac{V_{\text{in}}D}{R(1-D)^2} + \frac{V_{\text{in}}DT}{2L} \\ &= \frac{40(0.6)}{20(1-0.6)^2} + \frac{40(0.6)(200\mu\text{s})}{2(750\mu\text{H})} = 10.7 \text{ A} \end{aligned}$$

$$\begin{aligned} I_{L\min} &= \frac{V_{\text{in}}D}{R(1-D)^2} - \frac{V_{\text{in}}DT}{2L} \\ &= \frac{40(0.6)}{20(1-0.6)^2} - \frac{40(0.6)(200\,\mu\text{s})}{2(750\,\mu\text{H})} = 4.3 \text{ A} \end{aligned}$$

$$\begin{aligned} I_{\text{in}} &= \frac{I_{L\max} + I_{L\min}}{2} D \\ &= \frac{10.7 + 4.3}{2}(0.6) = 4.5 \text{ A} \end{aligned}$$

$$P_o = V_{\text{in}} I_{\text{in}}$$
$$= (40)(4.5) = 180 \text{ W}$$

Having found P_o, we can now solve for the average output current:

$$I_D = I_o = \frac{180 \text{ W}}{60 \text{ V}} = 3 \text{ A}$$

Hence, we can calculate the values for $I_{c\max}$ and $I_{c\min}$:

$$I_{c\max} = I_{L\max} - I_o = 7.7 \text{ A}$$
$$I_{c\min} = I_{L\min} - I_o = 1.3 \text{ A}$$

$$I_{c\text{rms}} = \sqrt{\frac{1}{T}\left[\int_0^{DT} 9\,dt + \int_{DT}^{T}\left(\frac{-V_o}{L}(t - DT) + I_{c\max}\right)dt\right]}$$
$$= 3.856 \text{ A}$$

EXERCISE 4.7

Consider a buck-boost converter that supplies 75 W at $I_o = 5$ A from a 37 V dc source. Let $T = 130\ \mu$s and $L = 250\ \mu$H. Determine: (*a*) the duty ratio, *D*, (*b*) $I_{L\max}$ and $I_{L\min}$, (*c*) average input current, (*d*) average diode and transistor currents, and (*e*) the rms value of the capacitor current.

ANSWER 0.29, 9.8 A, 4.25 A, 2.03 A, 5 A, 3.464 A.

EXERCISE 4.8

Derive the output voltage ripple formula of Eq. (4.62) for a buck-boost converter.

EXERCISE 4.9

Determine *D*, $I_{L\max}$, $I_{L\min}$, I_{in}, I_D, I_{sw}, and $I_{c\text{rms}}$ for a buck-boost converter whose capacitor current waveform is shown in Fig. E4.9. Assume $L = 120\ \mu$H.

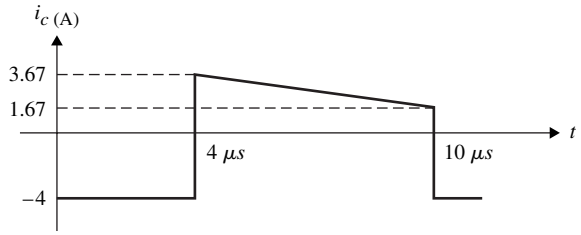


Figure E4.9 Waveform for Exercise 4.9.

ANSWER 0.4, 7.67 A, 5.67 A, 2.67 A, 4 A, 2.67 A, 3.3 A

Under certain input and output voltage conditions, none of the preceding three basic converter topologies is suitable. For example, suppose the input voltage varies between 8 and 18 V while the output voltage is desired to be maintained fixed at +12 V. It is clear that the voltage gain varies between 2/3 and 3/2 while the output is constant at +12 V. Even though the buck-boost converter allows the voltage gain to be less or greater than 1, it provides only a negative output voltage polarity. One topology that is capable of providing a positive output voltage is known as the *Single-Ended Primary Inductance Converter* (SEPIC), shown in Fig. 4.23.

4.2.4 Fourth-Order Converters

It is possible to cascade or cascode more than one of the basic topologies—buck, boost, and buck-boost—to form new topologies that have attractive features that a single topology does not. Figure 4.24(*a*) and (*b*) shows a block diagram of two converters

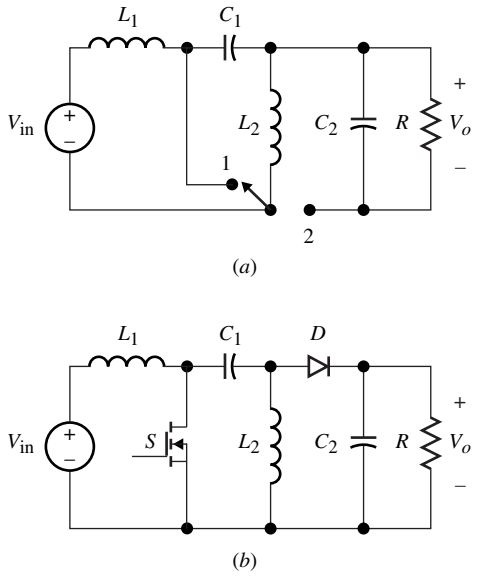


Figure 4.23 Single-ended primary inductance converter (SEPIC). (*a*) Single-switch, double-throw implementation. (*b*) MOSFET-diode implementation.

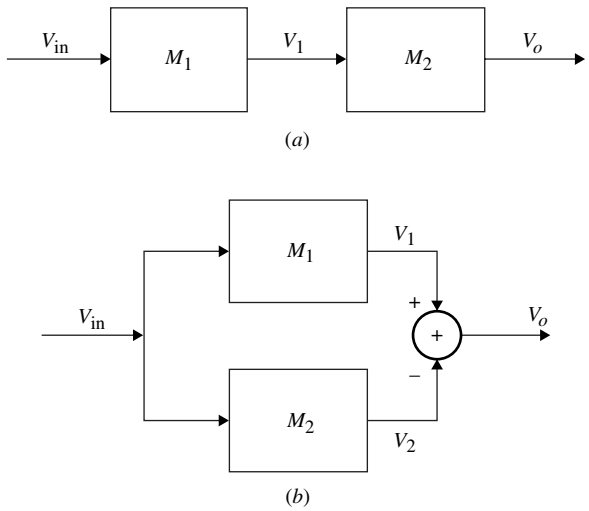


Figure 4.24 Combinations of basic converter topologies. (*a*) Cascade. (*b*) Cascode.

connected in series (cascade) and in parallel (cascode), respectively. The parallel connection is also known as a differential configuration.

The overall voltage gains for the Fig. 4.24(*a*) and (*b*) converter arrangements are given in Eqs. (4.63) and (4.64), respectively.

$$M = \frac{V_o}{V_{\text{in}}} = M_1 M_2 \tag{4.63}$$

$$M = \frac{V_o}{V_{\text{in}}} = M_1 - M_2 \tag{4.64}$$

where, in Fig. 4.24(*a*), M_1 and M_2 are given by

$$M_1 = \frac{V_1}{V_{\text{in}}} \quad M_2 = \frac{V_o}{V_1}$$

and in Fig. 4.24(*b*) we have

$$M_1 = \frac{V_1}{V_{\text{in}}} \quad M_2 = \frac{V_2}{V_{\text{in}}}$$

Figure 4.25(*a*) and (*b*) shows the block diagram and circuit implementation for the two possible series cascadings of the boost converter with a buck converter. Regardless of the sequence, the voltage gain for both converters should be $M_1 M_2 = D/(1-D)$.

The equivalent circuit representation for the cascade of the boost and buck converters is shown in Fig. 4.26(*a*). After careful circuit manipulation, it can be shown that the equivalent one-switch implementation of Fig. 4.26(*a*) is as shown in Fig. 4.26(*b*).

To illustrate how Fig. 4.26(*b*) is obtained from Fig. 4.26(*a*), we assume i_{L1} and i_{L2} are constant current sources as shown in Fig. 4.27(*a*). Figure 4.27(*b*) shows the equivalent circuit when *S* is in positions 1 and 2. Next we redraw the portion of the output circuit as shown in Fig. 4.27(*c*), which is redrawn in Fig. 4.27(*d*). The two modes of Fig. 4.27(*d*) are represented in the equivalent circuit shown in Fig. 4.27(*e*).

Similarly, the buck and boost cascade is shown in Fig. 4.28(*a*). The circuit can be simplified through several straightforward steps as shown in Fig. 4.28(*b*)–(*d*). Notice the capacitor in Fig. 4.28(*a*) is removed since regardless the state of S_1 and S_2, the capacitor average current is always zero. In Fig. 4.28(*c*) we combine L_1 and L_2 in series. Finally, Fig. 4.28(*d*) is obtained using similar steps for the buck-boost cascade.

EXAMPLE 4.7

Figure 4.29(*a*) shows a cascade of a buck and a Cuk converter. Show that the voltage gain is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{D^2}{1-D} \tag{4.65}$$

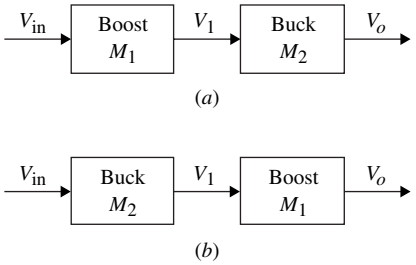


Figure 4.25 Block diagram representation for the cascade of a boost and a buck converter. (*a*) Boost-buck. (*b*) Buck-boost.

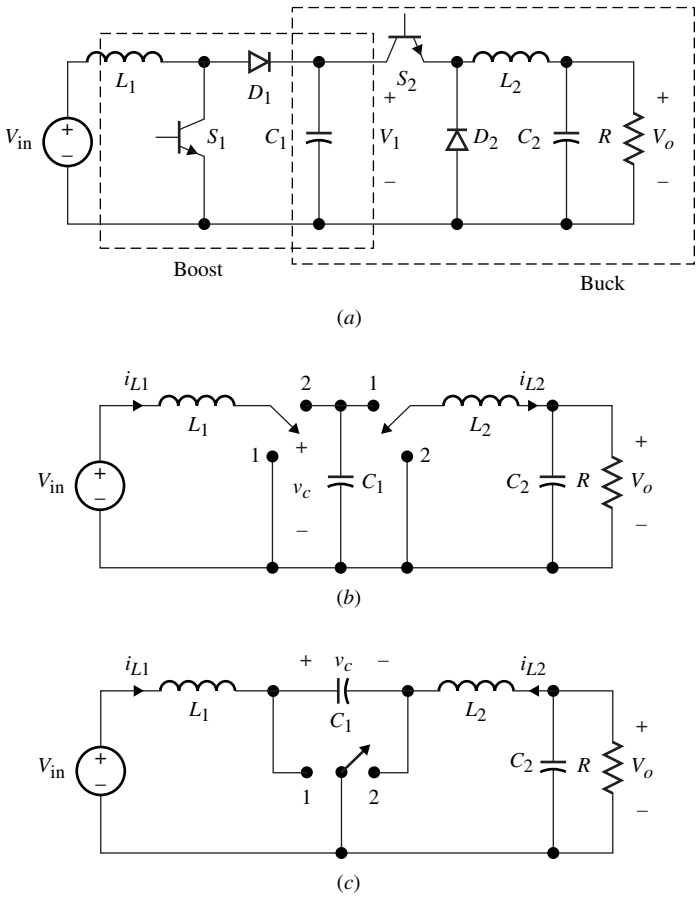


Figure 4.26 (*a*) Boost-buck cascade. (*b*) Two-switch implementation. (*c*) One-switch equivalent circuit implementation.

SOLUTION During mode 1, when S_1 and S_2 are in position 1, and during mode 2, when S_1 and S_2 are in position 2, the inductor voltages are given by

Mode 1 (*DT*):

$$v_{L1} = V_{\text{in}}$$
$$v_{L2} = -V_o + V_c$$

Mode 2 ((1–*D*)*T*):

$$v_{L1} = -V_c$$
$$v_{L2} = -V_o$$

Apply the volt-second balance principle to v_{L1} and v_{L2}, to obtain

$$v_{L1}\colon\ DV_{\text{in}} - (1-D)V_c = 0$$
$$M_1 = \frac{V_c}{V_{\text{in}}} = \frac{D}{1-D}$$

$$V_{L2}\colon\qquad D(-V_o + V_c) - (1-D)V_o = 0$$
$$M_2 = \frac{V_o}{V_c} = D$$

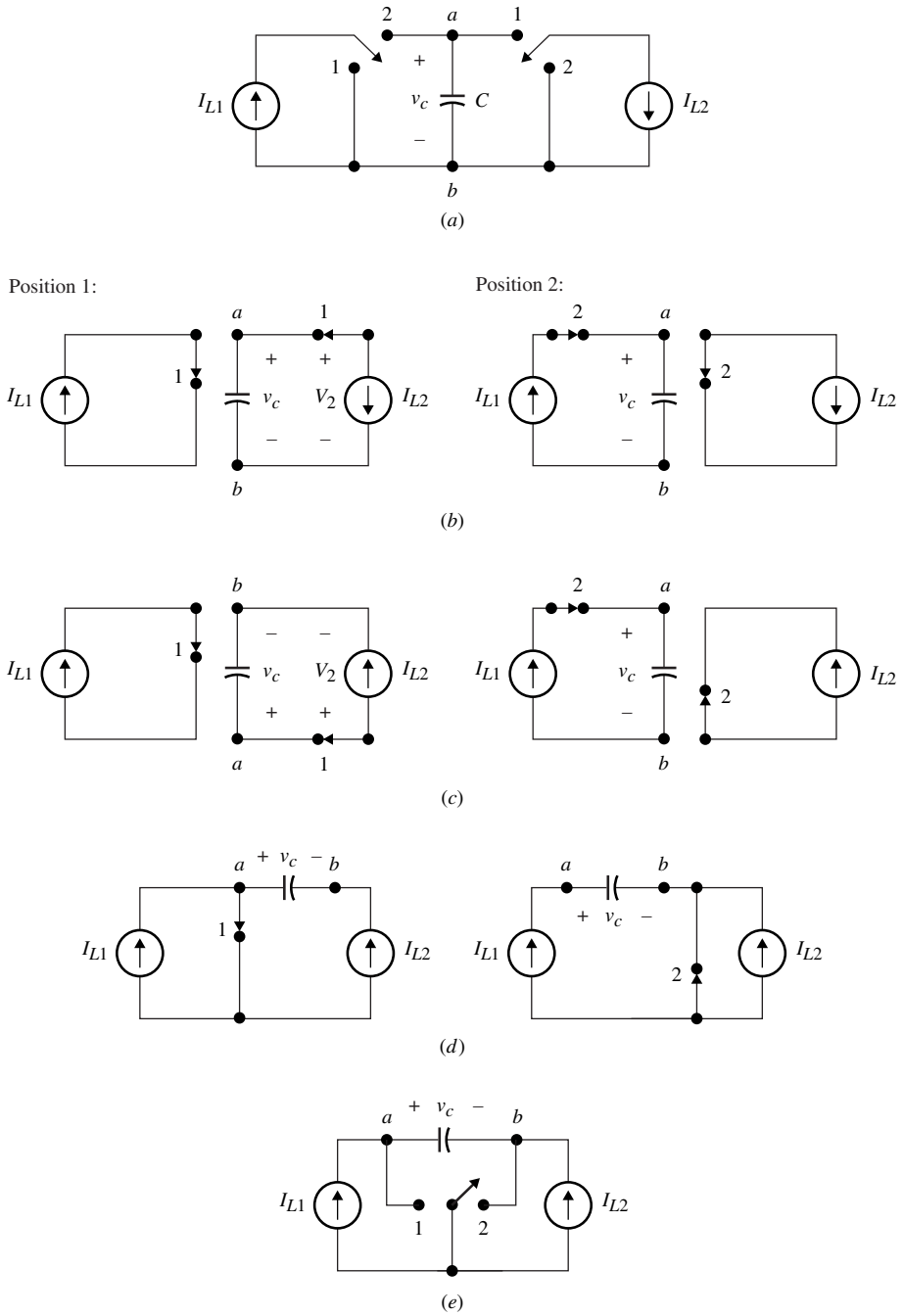


Figure 4.27 Steps illustrating how Fig. 4.26(*b*) is derived.

Therefore, the total voltage gain is

$$\frac{V_o}{V_c} = M_1 M_2 = \frac{D^2}{1-D}$$

Another straightforward way to find the gain equation is to realize that the average voltage between a and a' is DV_{in} and use this voltage as an input to the Cuk converter. The switch implementation for Fig. 4.29(*a*) is shown in Fig. 4.29(*b*).

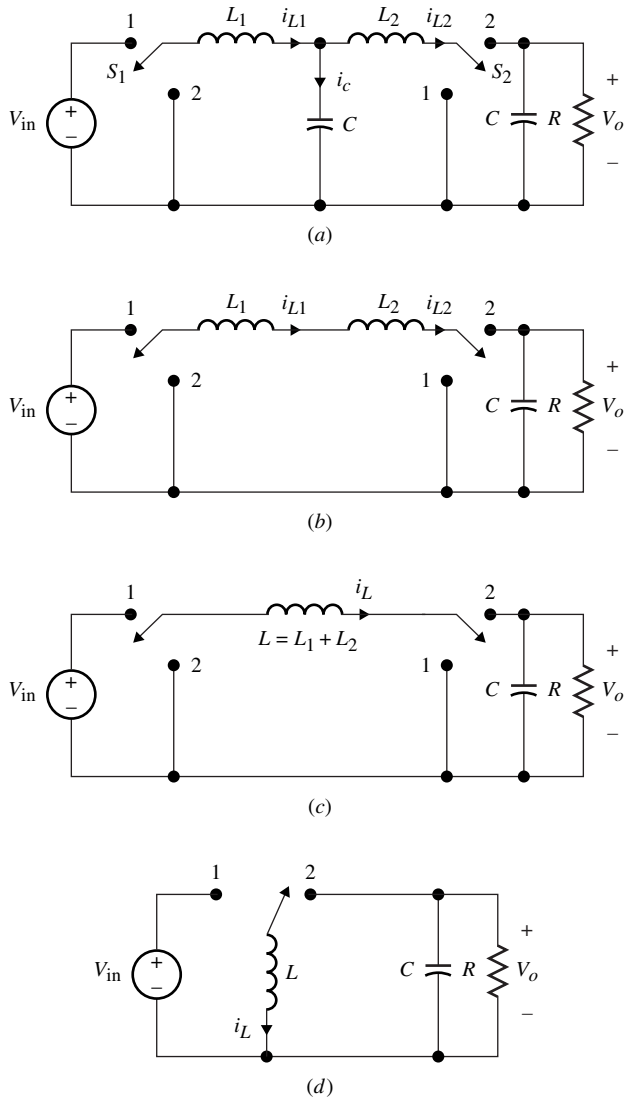
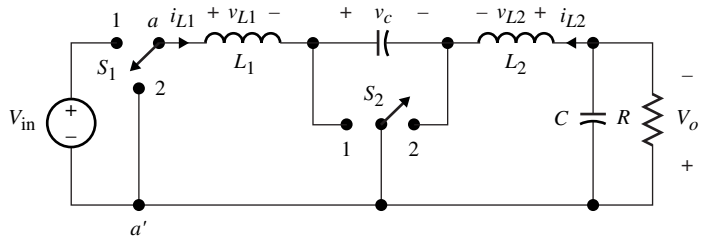


Figure 4.28 Steps illustrating how the buck-boost converter is obtained from the cascade configuration.

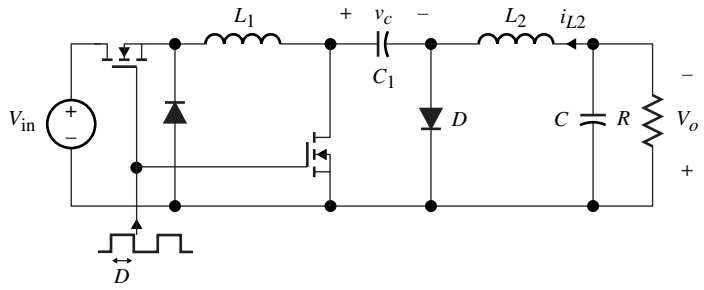
EXERCISE 4.10

Show that the cascaded buck and boost converters of Fig. 4.28(*c*) produce the same voltage gain conversion as that of Fig. 4.28(*a*), i.e., $V_o/V_{in} = D/(1-D)$, when S_1 and S_2 are single-pole, double-through switches; assume S_1 and S_2 are synchronized in position 1 for the DT interval and in position 2 for the $(1-D)T$ interval.

Figure 4.26(*b*) is known as a Cuk converter, whose voltage gain is $D/(1-D)$, as will be discussed in detail shortly. This concept can be extended to other cascaded topologies. The generalized fourth-order switched-mode voltage-to-voltage converter is given in Fig. 4.30. Components 1, 2, 3, 4, and 5 consist of a switch, a diode, two inductors, and one capacitor. By disallowing capacitor loops and inductor cut-sets, the



(*a*)



(*b*)

Figure 4.29 (*a*) Cascade configuration of buck and Cuk converters. (*b*) Diode-switch implementation.

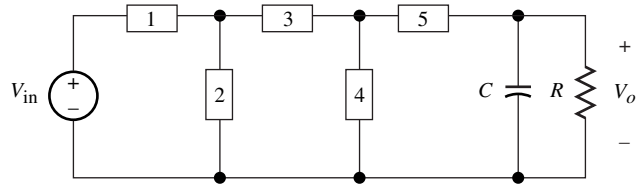


Figure 4.30 Generalized representation of fourth-order voltage-to-voltage converter.

total number of physically realizable topologies can be reduced. For example, all possible topologies with component 1 representing a switch are shown in Fig. 4.31.

The topology of Fig. 4.31(*e*) is a buck converter with an additional output *LC* filter. Figure 4.31(*c*) is a buck-boost converter with an additional output *LC* filter. The topologies in Fig. 4.31(*b*) and (*f*) are physically unrealizable since the average output current in each of the capacitors is zero; hence, no power is delivered to the load. On the other hand, Fig. 4.31(*d*) does not have an average input current.

The Cuk Converter

It has been shown that other converter topologies can be obtained by combining some of the three topologies discussed earlier. One cascade combination of a buck and a boost converter is known as a Cuk converter, given in Fig. 4.26(*b*) and redrawn in Fig. 4.32, named after its inventor, Slobodan Cuk from the California Institute of Technology. Figure 4.32(*c*) shows the Cuk converter with a magnetically coupled inductor representation.

The front end of the converter is a boost, and the back end of it is a buck. Hence, we may refer to the Cuk converter as a boost-buck converter. Unlike the previous converters, this converter requires two switches and uses two inductors, and a capacitor to store and transfer energy from the input to the output, resulting in a higher level of

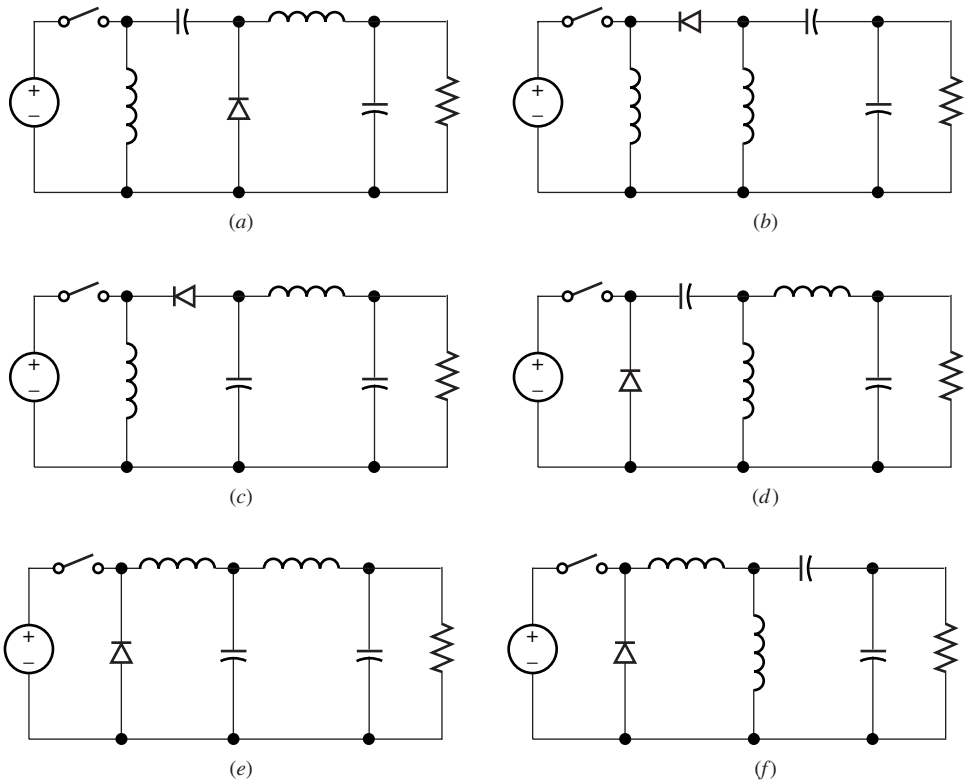


Figure 4.31 All possible fourth-order topologies with a switch used as component 1 in Fig. 4.30.

complexity. Like the buck-boost, the gain of the Cuk converter can be less than, equal to, or greater than 1, with a positive output polarity. The major advantage of this converter is that the input inductor, L_1, and the output inductor, L_2, can be coupled on one magnetic core structure such that with the proper core gap design, the input and output switching currents can be made zero. Other possible combinations of converters are shown in Fig. 4.33(*a*) and (*b*), which represent a boost cascade with an *LC* output filter and a buck cascade with an *LC* input filter, respectively.

The analysis of the Cuk converter can be carried out the same way as for the other converter topologies. There are two modes of operations: mode 1 when the switch is on, and mode 2 when the switch is off.

Mode 1 Mode 1 starts when the transistor is turned on at $t = 0$ (Fig. 4.34(*a*)).

The inductor L_1 voltage is given by

$$\begin{aligned} v_{L1} &= V_{\text{in}} \\ L_1 \frac{di_{L1}}{dt} &= V_{\text{in}} \end{aligned} \tag{4.66}$$

resulting in the following current relation:

$$i_{L1}(t) = \frac{V_{\text{in}}}{L_1} t + I_{L1}(0) \tag{4.67}$$

where $I_{L1}(0)$ is the initial current value.

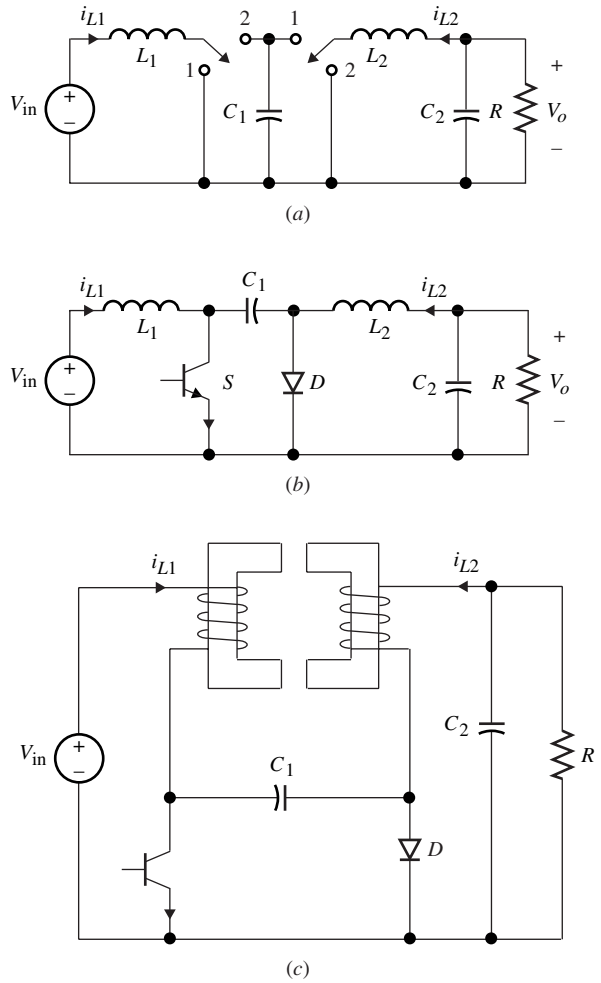


Figure 4.32 Cuk converter with magnetically coupled inductors. (*a*) Two-switch implementation. (*b*) Transistor-diode implementation. (*c*) Core implementation.

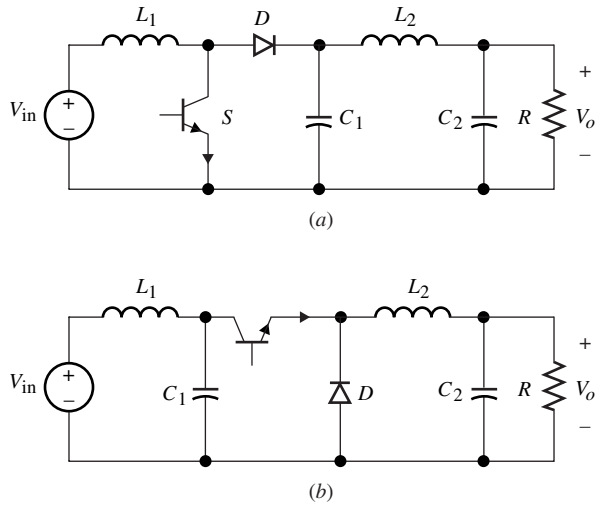


Figure 4.33 (*a*) Boost cascade with *LC* output filter. (*b*) Buck cascade with *LC* input filter.

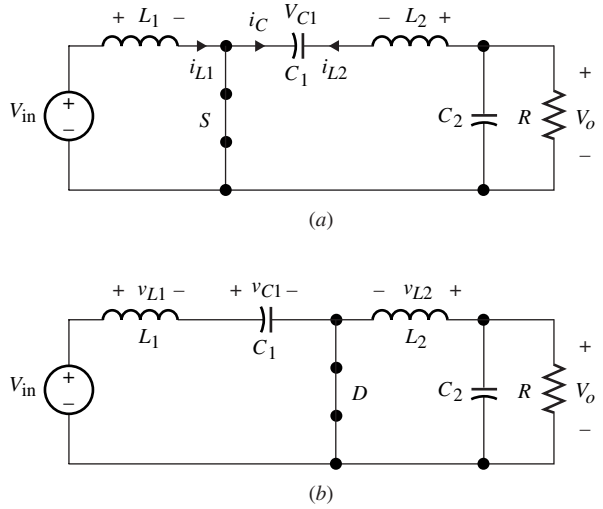


Figure 4.34 (*a*) Mode 1: Transistor is turned on. (*b*) Mode 2: Transistor is turned off.

The voltage across L_2 is given by

$$v_{L2} = v_{c1} + V_o$$
$$= L_2 \frac{di_{L2}}{dt}$$

Since $i_{L2} = -i_{c1} = -C(dv_{c1}/dt)$, the above equation yields

$$L_2 C_1 \frac{d^2 v_{c1}}{dt^2} + v_{c1} = -V_o$$

If we assume the average voltage across C_1 has no ripple, then its average value, V_{c1}, is given by

$$V_{c1} = V_{\text{in}} - V_o \tag{4.68}$$

This equation is obtained by using KVL from the output through C_1, L_1, L_2, and V_{in} and setting the average inductor voltages to zero.

$$v_{L2} = V_{\text{in}}$$

$$i_{L2} = \frac{V_{\text{in}}}{L_2} t + I_{L2}(0)$$

At $t = DT$,

$$I_{L1}(DT) = \frac{V_{\text{in}}}{L_1} DT + I_{L1}(0) \tag{4.69a}$$

Similarly,

$$I_{L2}(DT) = \frac{V_{\text{in}}}{L_2} DT + I_{L2}(0) \tag{4.69b}$$

Mode 2 When the transistor is turned off at $t = DT$, D turns on and the equivalent circuit is given by Fig. 4.34(*b*). Similar analysis shows

$$v_{L1} = V_o$$

and the inductor currents are given by

$$i_{L1}(t) = \frac{V_o}{L_1}(t - DT) + I_{L1}(DT)$$

$$i_{L2}(t) = \frac{V_o}{L_2}(t - DT) + I_{L2}(DT)$$

At $t = T$,

$$i_{L1}(T) = \frac{V_o}{L_1}(1 - D)T + I_{L1}(DT) \tag{4.70a}$$

$$i_{L2}(T) = \frac{V_o}{L_2}(1 - D)T + I_{L2}(DT) \tag{4.70b}$$

Since $I_{L1}(T) = I_{L1}(0)$ and $I_{L2}(T) = I_{L2}(0)$, from Eqs. (4.69) and (4.70), we obtain

$$\frac{-V_{\text{in}}}{L_1}DT = \frac{V_o}{L_1}(1 - D)T$$

$$\frac{V_o}{V_{\text{in}}} = \frac{-D}{1 - D} \tag{4.71}$$

The current and voltage waveforms for the Cuk converter are shown in Fig. 4.35.

The average input current is the same as the average inductor current $i_{L1}(t)$, given by

$$I_{\text{in}} = \frac{I_{L1\max} + I_{L1\min}}{2} \tag{4.72}$$

and the average output current is the same as the average inductor current $i_{L2}(t)$:

$$I_o = \frac{I_{L2\max} + I_{L2\min}}{2} \tag{4.73}$$

Since the average input power and output power are equal, we can obtain from the above equations the following:

$$I_{L2}(DT) = \left[\frac{D}{(1 - D)R} + \frac{DT}{2L_2}\right]V_{\text{in}} \tag{4.74a}$$

$$I_{L2}(0) = \left[\frac{D}{(1 - D)R} - \frac{DT}{2L_2}\right]V_{\text{in}} \tag{4.74b}$$

Similarly, we obtain

$$I_{L1}(DT) = \left[\frac{D^2}{(1 - D)^2R} + \frac{DT}{2L_1}\right]V_{\text{in}} \tag{4.75a}$$

$$I_{L1}(0) = \left[\frac{D^2}{(1 - D)^2R} - \frac{DT}{2L_1}\right]V_{\text{in}} \tag{4.75b}$$

For continuous input current $i_{L1}(t)$, we set $I_{L1}(0) = 0$ to obtain the critical value of L_1 as follows:

$$L_{1\text{crit}} = \frac{(1 - D)^2RT}{2D} \tag{4.76}$$

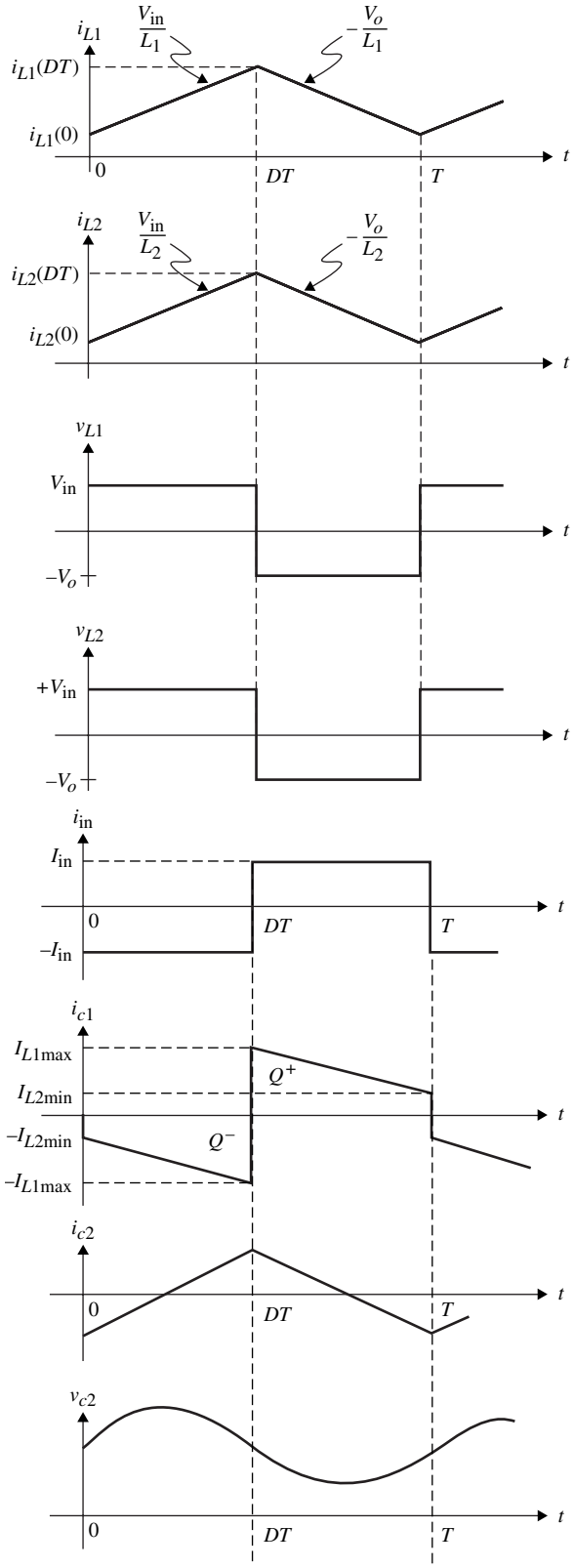


Figure 4.35 Current and voltage waveforms for the Cuk converter.

Similarly, for continuous current in L_2, the minimum value is given by

$$L_{2\text{crit}} = \frac{(1-D)RT}{2} \tag{4.77}$$

The ripple voltage across C_1 and C_2 is given by

$$\frac{\Delta V_{c1}}{V_o} = \frac{D}{RC_1 f}$$

$$\frac{\Delta V_{c2}}{V_o} = \frac{1-D}{8L_2C_2f^2} \tag{4.78}$$

EXERCISE 4.11

The converters shown in Fig. E4.11(*a*) and (*b*) are for a SEPIC and a converter known as a Zeta. Derive the voltage gain expressions for both converters.

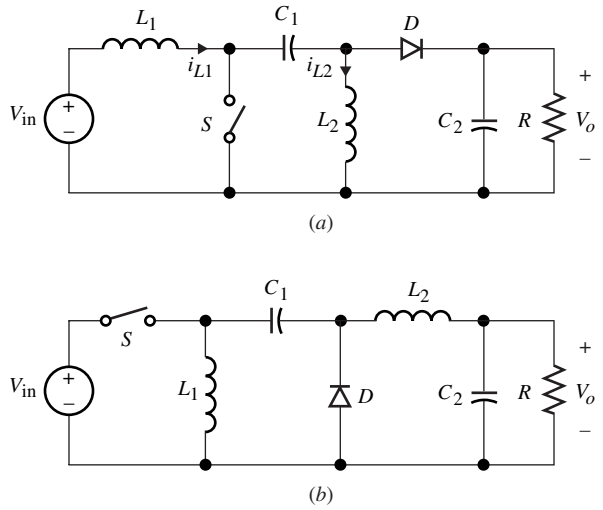


Figure E4.11 (*a*) SEPIC. (*b*) Zeta.

ANSWER $\dfrac{D}{1-D}$

EXERCISE 4.12

Consider the SEPIC converter in Fig. E4.11(*a*) operating in ccm with the following parameters:

$$D = 0.52 \qquad V_{\text{in}} = 112\ \text{V} \qquad f_s = 110\ \text{kHz}$$

$$R = 12\ \Omega \qquad L_1 = L_2 = 50\ \mu\text{H} \qquad C_1 = C_2 = C = 147\mu\text{F}$$

(a) Sketch the waveforms for i_{L1}, i_{L2}, i_D, i_{C1}, and i_{C2}.

(b) Determine the capacitor ripple voltage $|\Delta V_{C1}/V_o|$ and $|\Delta V_{C2}/V_o|$.

ANSWER $\dfrac{\Delta V_{C1}}{V_o} = \dfrac{\Delta V_{C2}}{V_D} = \dfrac{D}{RCf}$

EXERCISE 4.13

Consider the PWM converter shown in Fig. E4.13 with S_1 and S_2 turning on and off simultaneously. Derive the expression for V_o/V_{in}.

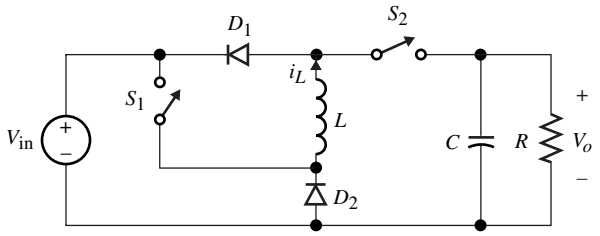


Figure E4.13 PWM converter for Exercise 4.13.

ANSWER $(2D-1)/D$

4.2.5 Bipolar Output Voltage Converters

All single-switch converter topologies discussed so far produce a unipolar average output voltage and a unipolar average output current as shown in Fig. 4.36, resulting in unidirectional average power flow from the source to the load.

In some converter topologies, like bridge converters, the output voltage can be of two polarities, depending on the duty cycle. Figure 4.37(*a*) and (*b*) shows two ways to implement a converter that produces bipolar output voltage.

Furthermore, depending on the switching sequence, the average output voltage and current can be unidirectional. Figure 4.37(*c*) shows the switch-diode implementation of Fig. 4.37(*b*). It can be shown that the voltage gain is given by

$$\frac{V_o}{V_{\text{in}}} = 2D - 1 \tag{4.79}$$

Figure 4.38 shows a plot of *M* vs. *D* for several converters.

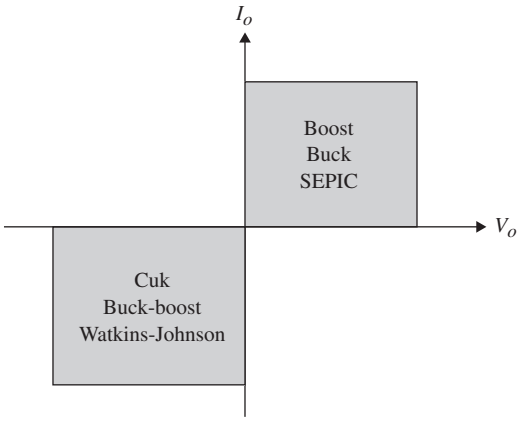


Figure 4.36 Average output current vs. output voltage.

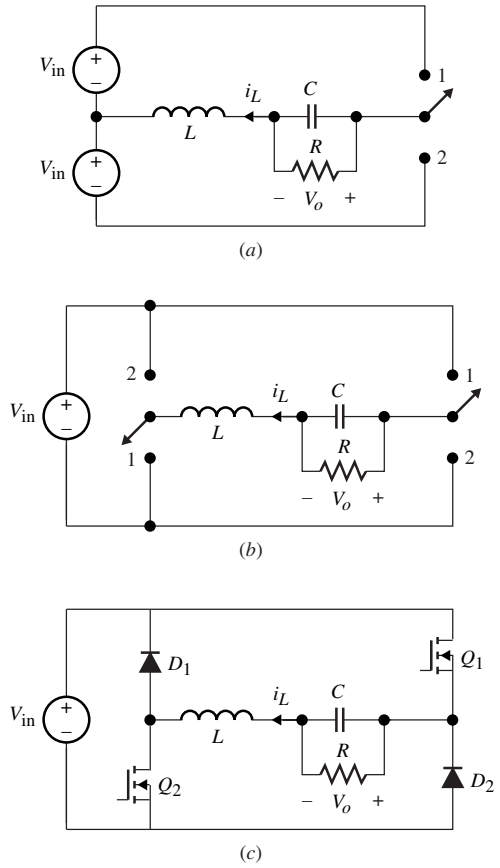


Figure 4.37 Bipolar output voltage converters. (*a*) Half-bridge. (*b*) Full-bridge. (*c*) Diode transistor implementation of (*b*).

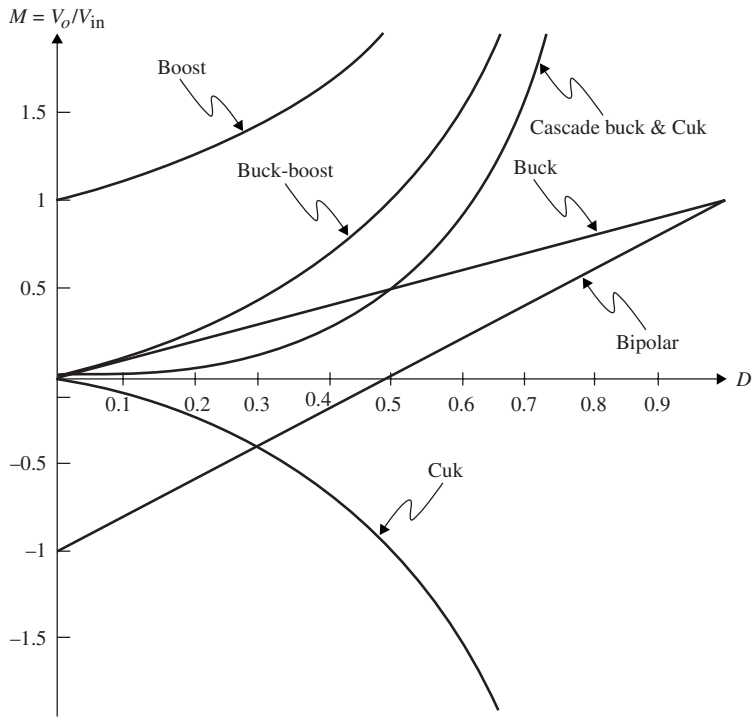


Figure 4.38 *M* vs. *D* for various converters.

EXERCISE 4.14

The converter shown in Fig. E4.14 is known as a Watkins-Johnson converter and is capable of producing a bipolar output voltage. Assume S_1 and S_2 are thrown in positions 1 and 2 simultaneously for the DT and $(1-D)T$ time intervals, respectively. Derive the expression for the voltage gain V_o/V_{in}.

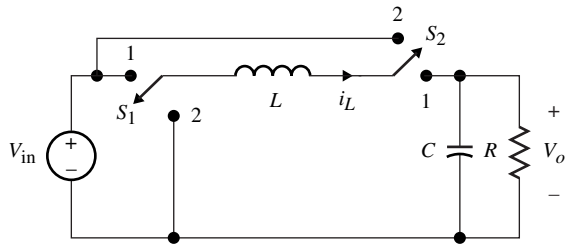


Figure E4.14 Watkins-Johnson converter.

ANSWER $\dfrac{V_o}{V_{\text{in}}} = \dfrac{2D-1}{D}$

4.3 DISCONTINUOUS CONDUCTION MODE

Unlike the continuous conduction mode (ccm), in the discontinuous conduction mode (dcm), the minimum inductor current in each of the three basic topologies is zero. Hence, there exists a short interval in which the inductor current is zero, i.e., discontinuous. dcm operation is frequently encountered in dc-to-dc converters since these converters normally operate under open load conditions. Both the steady-state conversion ratio and the closed-loop dynamic charge significantly change. It will be shown shortly that under dcm the converter voltage gain is a function of not only D, but also the load, switching frequency, and circuit components.

As in the ccm case, the steady-state condition will be assumed when it comes to deriving the expression for the voltage gain. In this section we will present the steady-state analysis for the buck, boost, and buck-boost topologies operated in dcm. Unlike the steady-state analysis in ccm, the analysis for dcm requires solving for the time interval during which the inductor current becomes zero. The basic analysis procedure for each converter is the same.

4.3.1 The Buck Converter

The inductor current waveform under dcm operation is shown in Fig. 4.39. Recall the inductor current equations for the buck converter:

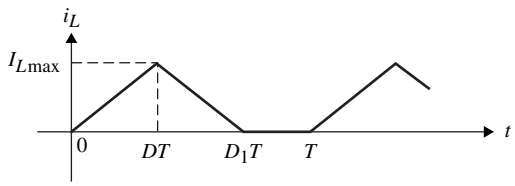


Figure 4.39 Inductor current waveform under dcm operation.

$$i_L(t) = \frac{1}{L}(V_{\text{in}} - V_o)t + i_L(0) \qquad 0 \le t < DT \tag{4.80a}$$

$$i_L(t) = \frac{-1}{L}V_o(t - DT) + i_L(DT) \qquad DT \le t < T \tag{4.80b}$$

The edge of discontinuity occurs when $i_L(T) = i_L(0) = 0$. This value occurs when $L = L_{\text{crit}}$. The waveform for $i_L(t)$ at the edge of discontinuity is shown in Fig. 4.40. These waveforms correspond to the equivalent circuits given in Fig. 4.41(*a*), (*b*), and (*c*) when the switch(es) are on, off, and both off, respectively.

If the converter inductor becomes less than L_{crit}, there exists a dead time greater than zero, as shown in Fig. 4.39. It is shown that D_1 is the duty ratio at which the inductor current becomes zero.

At $t = DT$, Eq. (4.80*a*) gives

$$i_L(DT) = \frac{1}{L}(V_{\text{in}} - V_o)(DT) \tag{4.81}$$

Notice the initial inductor current at $t = 0$ is zero, $i_L(0) = 0$.

At $t = D_1T$, Eq. (4.80*b*) gives

$$i_L(D_1T) = \frac{-1}{L}V_o(D_1T - DT) + i_L(DT) = 0 \tag{4.82}$$

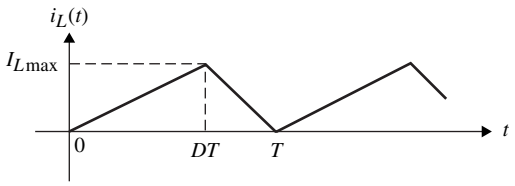


Figure 4.40 Inductor current waveform at the edge of the discontinuity.

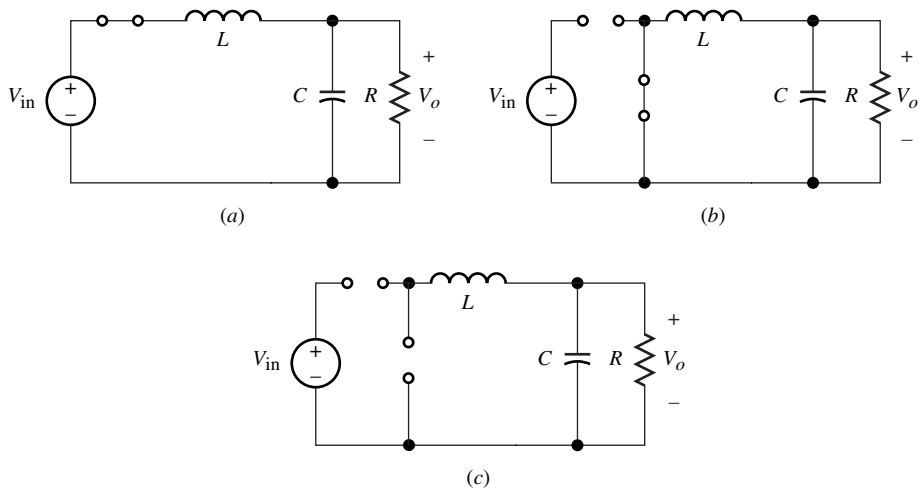


Figure 4.41 Equivalent circuit modes for the buck converter operating in dcm. (*a*) Switch is on. (*b*) Switch is off. (*c*) $i_L = 0$.

From the above two equations, we obtain

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{D_1} \tag{4.83}$$

Using the above equation, we solve for $i_L(DT)$,

$$i_L(DT) = \frac{2V_o^2}{DV_{\text{in}}R} \tag{4.84}$$

Solve for D_1 from Eqs. (4.83) and (4.84) to obtain

$$D_1 = \frac{2V_oL}{DRTV_{\text{in}}} + D \tag{4.85}$$

Thus, the voltage gain in terms of D and the circuit parameters is given by

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{\dfrac{2V_oL}{DRTV_{\text{in}}} + D} \tag{4.86}$$

Let the voltage gain M be equal to V_o/V_{in}. We must solve for the voltage gain in terms of the circuit components. From Eq. (4.86), we solve for M to yield

$$M = \frac{D^2RT}{4L}\left[\sqrt{\frac{8L}{D^2RT} + 1} - 1\right] \tag{4.87}$$

We can also express D_1 as follows:

$$D_1 = \frac{1}{\dfrac{DRT}{4L}\left[\sqrt{\dfrac{8L}{D^2RT} + 1} - 1\right]} \tag{4.88}$$

The voltage conversion characteristics of the buck converter can be expressed in terms of the normalized time constant, τ_n, which is given by

$$\tau_n = \frac{\tau}{T} \tag{4.89}$$

where $\tau = L/R$ and T is the switching period.

The voltage gain can be expressed as

$$M = \frac{D^2}{4\tau_n}\left[\sqrt{\frac{8\tau_n}{D^2} + 1} - 1\right] \tag{4.90}$$

The characteristic curves for M vs. D under different values of the normalized time constant are shown in Fig. 4.42.

The normalized relation for D_1 is given by,

$$D_1 = \frac{1}{\dfrac{D}{4\tau_n}\left[\sqrt{\dfrac{8\tau_n}{D^2} + 1} - 1\right]} \tag{4.91}$$

The characteristic curves for M vs. D_1 under different values of the normalized time constants are shown in Fig. 4.43.

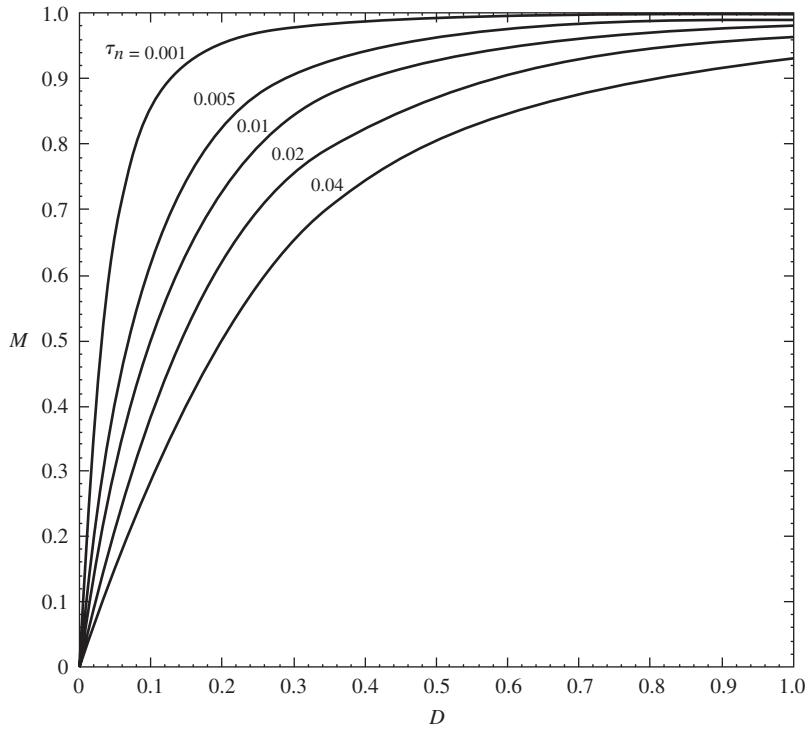


Figure 4.42 Characteristic curves for M vs. D under different normalized time constants.

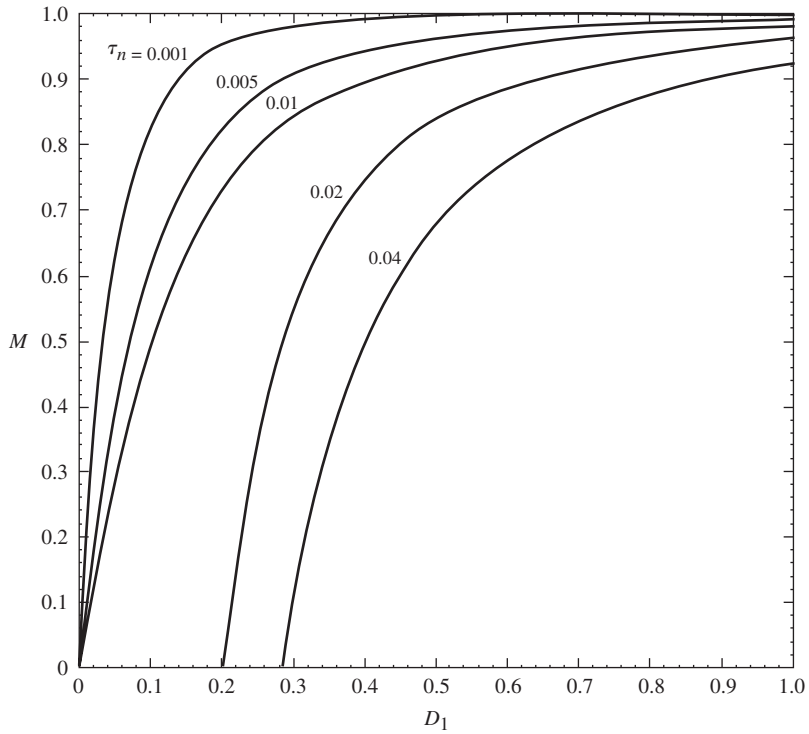


Figure 4.43 Characteristic curves for M vs. D_1 under different normalized time constants.

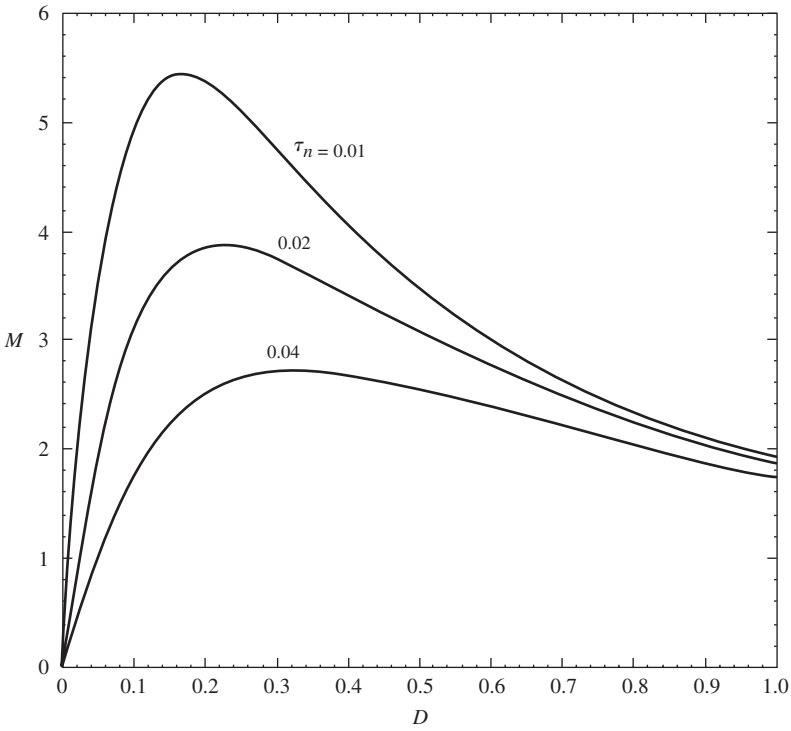


Figure 4.44 Normalized maximum inductor current vs. D under different normalized time constants.

The maximum inductor current of Eq. (4.81) can be expressed in terms of τ_n:

$$I_{L\max} = -\frac{V_{\text{in}}TD}{L}\left[\frac{D^2}{4\tau_n}\left[\sqrt{\frac{8\tau_n}{D^2}+1}-1\right]-1\right] \tag{4.92}$$

Normalizing the current by V_{in}/R,

$$I_{nL\max} = \frac{I_{L\max}R}{V_{\text{in}}}$$

$$I_{nL\max} = -\frac{D^3}{4\tau_n^2}\left[\sqrt{\frac{8\tau_n}{D^2}+1}-1\right]+\frac{D}{\tau_n} \tag{4.93}$$

The plot for $I_{nL\max}$ vs. D under different normalized time constants is given in Fig. 4.44.

EXAMPLE 4.8

Consider a buck converter with a dc voltage source of 80 V and a load resistance equal to 18 Ω. It is required that this converter deliver at least 100 W to the load. Assume the switching frequency is 150 kHz. Determine: (*a*) the inductor critical value, L_{crit}, (*b*) the voltage gain for $L = 0.1L_{\text{crit}}$ and $10L_{\text{crit}}$, (*c*) D_1 for $L = 0.1L_{\text{crit}}$, and (*d*) the maximum inductor current at $t = DT$.

SOLUTION

(a) The output voltage, V_o, is given by

$$V_o = \sqrt{P_oR} = \sqrt{(100)(18)} = 42.43 \text{ V}$$

For the given $V_{in} = 80$ V, the duty ratio under ccm is 0.53. Under this condition, with $T = 6.67$ μs the inductor critical value is

$$L_{crit} = \frac{RT}{2}(1 - D)$$

(b) If the inductor is chosen to be less than $L = 0.1L_{crit} = 2.812$ μH, we have

$$M = \frac{V_o}{V_{in}} = \frac{D^2RT}{4L}\left[\sqrt{\frac{8L}{D^2RT} + 1} - 1\right] = 0.873$$

For $L = 10L_{crit}$,

$$M = \frac{V_o}{V_{in}} = \frac{42.43}{80} = 0.53$$

The new output voltage is $V_o = 0.873(80) = 69.8$ V.

(c) D_1 is given by

$$D_1 = \frac{D}{M} = \frac{0.53}{0.873} = 0.61$$

(d) The maximum inductor current at $t = DT$ is

$$I_{Lmax} = -\frac{V_{in}TD}{L}(M - 1) = 12.73 \text{ A}$$

The time intervals are given as $DT = 3.53$ μs and 4.2 μs with

$$I_o = I_L = \frac{V_o}{R} = \frac{69.8 \text{ V}}{18} = 3.88 \text{ A} \qquad P_o = (3.88)(69.8) = 270.8 \text{ W}$$

$$I_{in} = \frac{I_L(DT)}{2}D = \frac{(12.73)(0.53)}{2} = 3.37 \text{ A} \qquad P_{in} = (3.37)(80) = 269.8 \text{ W}$$

The plot for i_L is shown in Fig. 4.45.

EXAMPLE 4.9

Consider a buck converter with the following parameters: $V_{in} = 80$ V, $R_o = 18$ Ω, $P_o = 100$ W, $L = 0.4$ mH, $f_s = 150$ kHz.

(a) Determine the mode of operation.

(b) Determine the range of R_o for the converter to remain in the ccm.

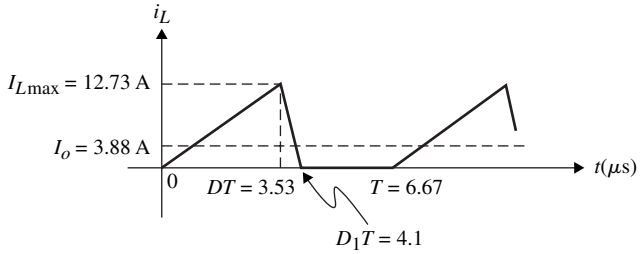


Figure 4.45 Inductor current waveform for Example 4.8 under dcm.

SOLUTION

(a) $V_o = \sqrt{P_o R_o} = 42.43$ V
Assuming continuous mode of operation,

$$D = \frac{V_o}{V_{\text{in}}} = \frac{42.43 \text{ V}}{80 \text{ V}} = 0.53$$

The critical inductor value is given by

$$L_{\text{crit}} = \frac{R_o T}{2}(1 - D) = 28.21 \ \mu\text{H}$$

Since $L > L_{\text{crit}}$, the converter is operating in the ccm.

(b) Notice that the inductor current tends to decrease faster as the load resistance increases.
Recall,

$$I_L(DT) = I_{L\max} = \left[\frac{1}{R} + \frac{(1-D)T}{2L}\right] DV_{\text{in}}$$

$$I_L(0) = I_{L\min} = \left[\frac{1}{R} - \frac{(1-D)T}{2L}\right] DV_{\text{in}}$$

For $I_{L\min} = 0$, we have

$$0 = \left[\frac{1}{R} - \frac{(1-0.53)6.67 \ \mu\text{s}}{2(0.4 \text{ mH})}\right](0.53)(80)$$

$$R = \frac{2(0.4 \ \mu\text{H})}{(1-0.53)(6.67 \ \mu\text{s})} = 255.2 \ \Omega$$

For $R < 255.2 \ \Omega$	ccm (heavy load)
For $R = 255.2 \ \Omega$	dcm (boundary)
For $R > 255.2 \ \Omega$	dcm (light load)

4.3.2 The Boost Converter

The boost converter can also be analyzed to obtain the voltage gain, *M*, the time at which the inductor current reads zero, D_1, and the maximum inductor current, $I_{L\max}$. For the on state in the time interval $0 \le t \le DT$, we have

$$i_L = \frac{V_{\text{in}}}{L} t \tag{4.94}$$

In the dcm $I_L(0)$ equals zero, and the maximum inductor current occurs at $t = DT$, and is given by

$$I_{L\max} = I_L(DT) = \frac{V_{\text{in}}}{L} DT \tag{4.95}$$

For the *off* state in the time interval $DT \le t$, we have

$$i_L(t) = \frac{V_{\text{in}} - V_o}{L}[t - DT] + i_L(DT)$$

In the dcm, $i_L(D_1 T) = 0$; hence,

$$0 = \frac{V_{\text{in}} - V_o}{L}(D_1 - D)T + i_L(DT) \tag{4.96}$$

From Eqs. (4.95) and (4.96), we obtain the voltage gain:

$$\frac{V_o}{V_{\text{in}}} = M = \frac{D_1}{D_1 - D} \tag{4.97}$$

To solve for D_1 in terms of the circuit parameters, we use conservation of power to obtain another relation. The average input power, P_{in}, equals $I_{\text{in}}V_{\text{in}}$, where $I_{\text{in}} = \frac{1}{2}I_{L\max}D_1$; thus,

$$P_{\text{in}} = \tfrac{1}{2}I_{L\max}V_{\text{in}}D_1 \tag{4.98}$$

The average output is given by

$$P_o = \frac{V_o^2}{R} \tag{4.99}$$

Equating P_{in} and P_o, from Eqs. (4.98) and (4.99) we obtain

$$I_{L\max} = \frac{2V_o^2}{RV_{\text{in}}D_1} \tag{4.100}$$

From Eqs. (4.97) and (4.100), and using $I_{\text{in}} = \frac{1}{2}I_{L\max}D_1$, we obtain

$$M = \frac{1}{2}\left[1 + \sqrt{1 + \frac{2RTD^2}{L}}\right] \tag{4.101}$$

In terms of τ_n,

$$M = \frac{1}{2}\left[1 + \sqrt{1 + \frac{2D^2}{\tau_n}}\right] \tag{4.102}$$

The duty ratio D_1 is obtained from Eq. (4.97) in terms of τ_n:

$$D_1 = \frac{\tau_n}{D} + D + \sqrt{\frac{\tau_n^2}{D^2} + 2\tau_n} \tag{4.103}$$

Setting $D_1 = 1$ and solving for L, we obtain

$$L = L_{\text{crit}} = \frac{RTD}{2}(1 - D)^2$$

The normalized maximum inductor current is given by

$$I_{nL\max} = \frac{D}{\tau_n} \tag{4.104}$$

The characteristic curves for M vs. D, M vs. D_1, and D vs. $I_{nL\max}$ under different normalized time constants are shown in Figs. 4.46, 4.47, and 4.48, respectively.

EXAMPLE 4.10

Consider a boost converter that supplies 4 A to an 80 V output with $V_{\text{in}} = 60$ V and $L = 67$ μH. Assume the inductor current is discontinuous and $f_s = 100$ kHz. Determine the operation mode and the maximum inductor that can be used to achieve the dcm mode of operation.

SOLUTION The voltage gain is 1.33 and $\tau = L/R = 3.35 \times 10^{-6}$ s, and $\tau_n = 0.335$. The duty ratio is

$$D = \frac{M - 1}{M} = \frac{1.33 - 1}{1.33} = 0.25$$

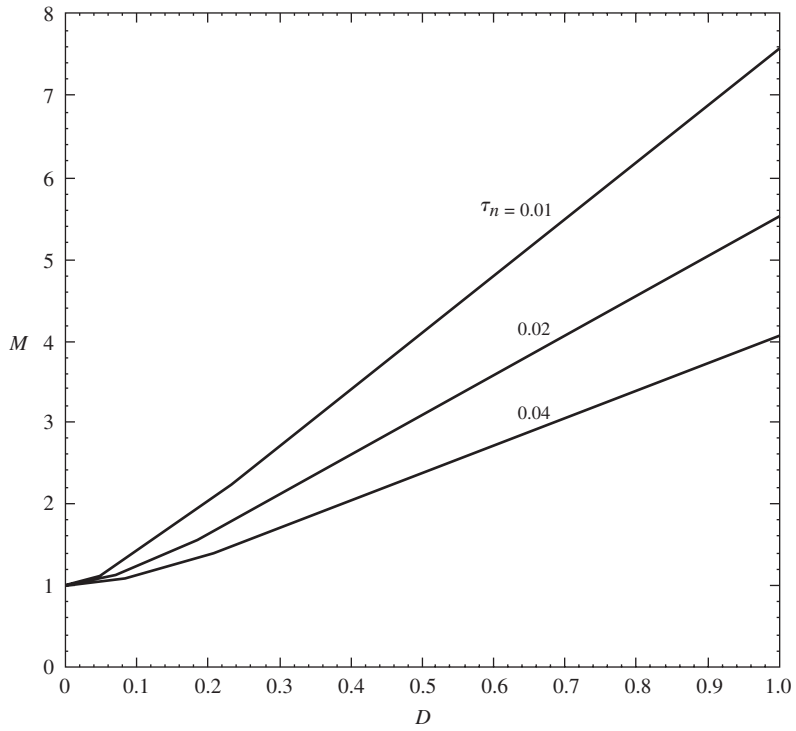


Figure 4.46 *M* vs. *D* under different values of normalized time constant for the boost converter.

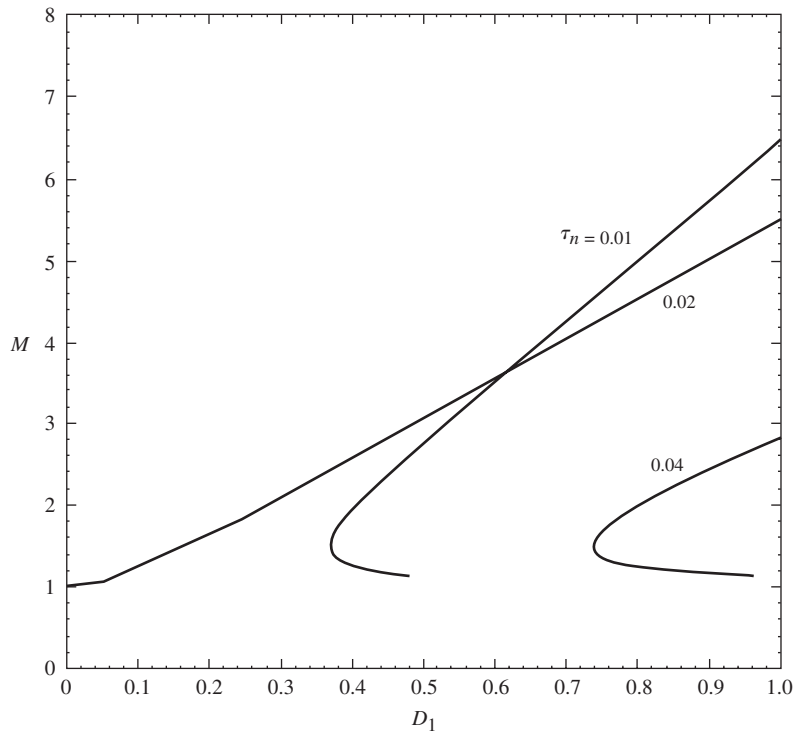


Figure 4.47 *M* vs. D_1 under different values of time constant for the boost converter.

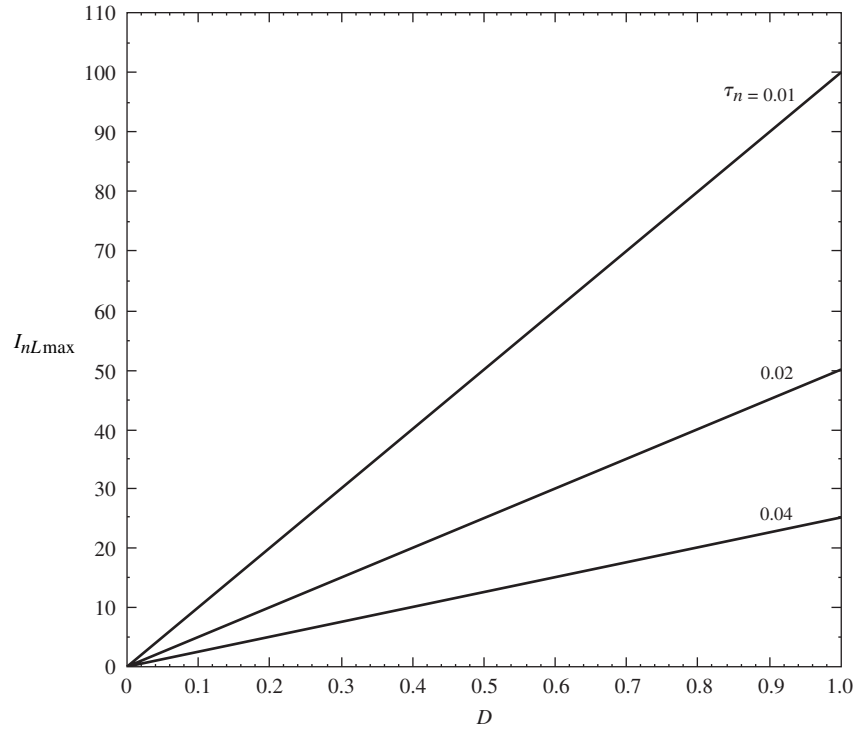


Figure 4.48 $I_{nL\max}$ vs. D under different values of normalized time constant for the boost converter.

Thus, we obtain the value for D_1 as

$$D_1 = \frac{\tau_n}{D} + D + \sqrt{\frac{\tau_n^2}{D^2} + 2\tau_n}$$

$$D_1 = \frac{0.335}{0.248} + 0.248 + \sqrt{\frac{(0.335)^2}{(0.248)^2} + 2(0.335)} = 3.18$$

Since $D_1 > 1$, the converter must be operating in the ccm under the specified values.

The maximum inductor value to maintain is

$$L < L_{\text{crit}} = \frac{RTD}{2}(1-D)^2$$

$$L \leq 0.125 \text{ mH for dcm}$$

4.3.3 The Buck-Boost Converter

As with the other two converters, the derivation of the gain equation for the buck-boost operating in dcm is straightforward. Similar analysis shows the following relations for M and D_1.

$$D_1 = D\left(1 + \frac{1}{M}\right) \tag{4.105}$$

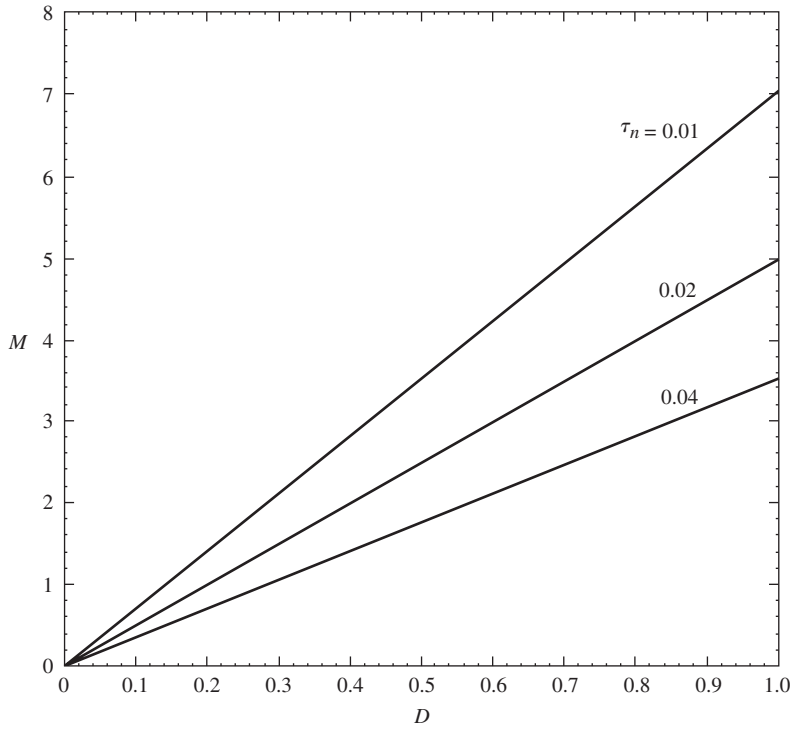


Figure 4.49 *M* vs. *D* under different values of normalized time constant for the buck-boost converter.

$$M = \frac{D}{\sqrt{2\tau_n}} \tag{4.106}$$

The characteristic curves for *M* vs. *D* under different values of normalized time constant are shown in Fig. 4.49. For the *M* vs. D_1 curve, refer to Fig. 4.50.

The normalized maximum inductor current is given by

$$I_{nL\max} = \frac{MD}{\tau_n} \tag{4.107}$$

Figure 4.51 shows $I_{nL\max}$ vs. *D* under different normalized time constants.

EXAMPLE 4.11

Consider a buck-boost converter with the following values: $V_o = 12$ V, $P_o = 25$ W, $V_{\text{in}} = 20$ V, and $f = 100$ kHz .

(a) Design the converter so that it will operate in ccm.

(b) Repeat part (*a*) for dcm.

(c) Find the maximum inductor current under both ccm and dcm.

(d) If the load resistance increases by 50% (i.e., the load current changes from 2.08 A to 1.39 A), determine the mode of operation for the two converters and then the maximum inductor current. Sketch the new inductor currents.

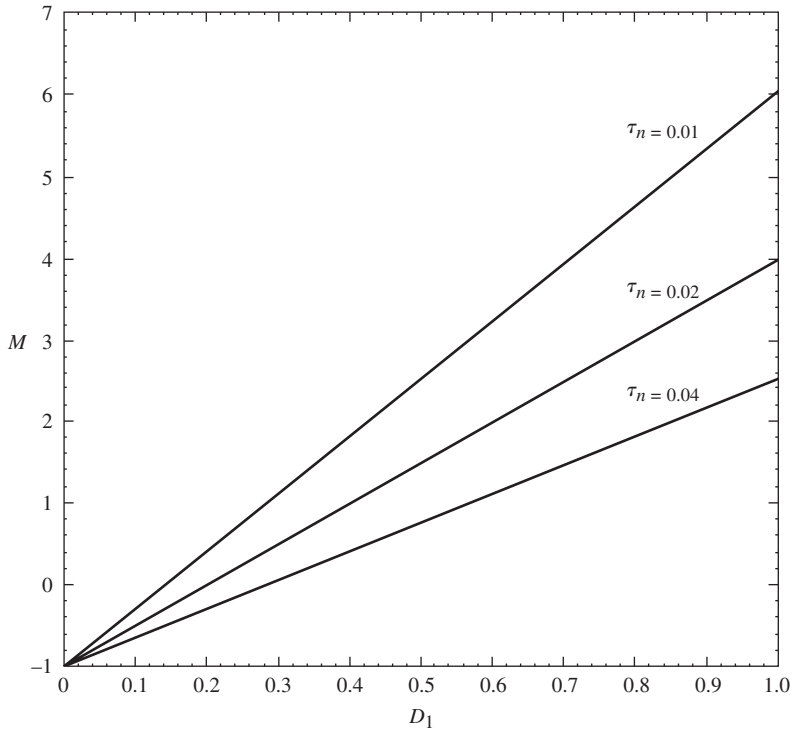


Figure 4.50 M vs. D_1 under different values of normalized time constant for the buck-boost converter.

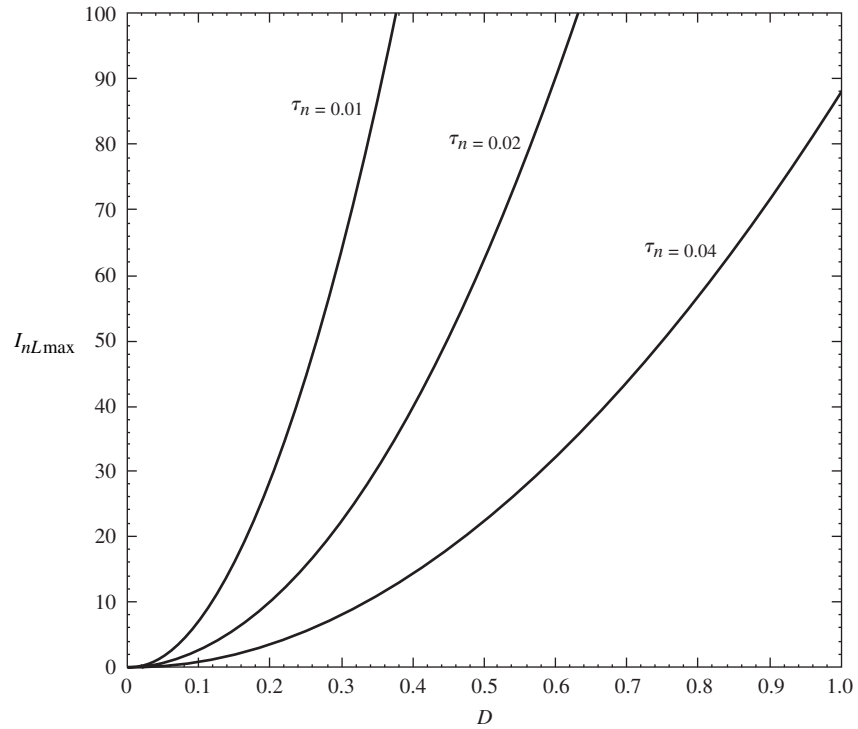


Figure 4.51 $I_{nL\max}$ vs. D under different values of normalized time constant for the buck-boost converter.

SOLUTION

(a) The load resistance at 25 W and 12 V output is given by

$$R = \frac{V_o^2}{P_o} = \frac{12^2}{25} = 5.76\ \Omega$$

The duty ratio, D, under ccm is 0.375.

For ccm, the inductor must be larger than the critical value given by

$$L_{\text{crit}} = \left(\frac{RT}{2}\right)(1-D)^2 = 0.01125\ \text{mH}.$$

For ccm, we choose $L = 0.1$ mH.

(b) For dcm, we choose L smaller than L_{crit}. Let $L = 0.005$ mH.

$$\tau_n = \frac{\tau}{T} = \frac{0.868\ \mu s}{10\ \mu s} = 0.087$$

Hence, for $M = 0.6$ and $\tau_n = 0.087$ we obtain $D = 0.25$. Solve for D_1 to yield $D_1 = 0.67$.

(c) The maximum inductor current for ccm is given by

$$I_{L\max} = \frac{DV_{\text{in}}}{R(1-D)^2} + \frac{V_{\text{in}}DT}{2L} = 3.71\ \text{A}$$

The minimum inductor current is given by

$$I_{L\min} = 3.33 - 0.371 \approx 3\ \text{A}$$

For dcm, we have

$$I_{L\max} = \frac{1}{L}V_{\text{in}}DT = 10\ \text{A}$$

(d) If the load resistance changes by +50% for the designs, the new modes of operations can be obtained by finding the new value of τ_n or determining the new L.

(*i*) For the ccm:

$$R_{\text{new}} = 5.76 + \tfrac{1}{2}(5.76) = 8.64\ \Omega$$

The new L_{crit} is given by

$$L_{\text{crit}} = 0.017\ \text{mH}$$

Hence, the converter will remain in the ccm.

$$I_{L\max} = 2.6\ \text{mA}$$

$$I_{L\min} = 1.85\ \text{mA}$$

(*ii*) For the dcm the new τ is $0.005/8.64 = 0.58\ \mu s$; then the normalized τ_n is given by

$$\tau_n = \frac{\tau}{T} = \frac{0.58}{10} = 0.058$$

For $M = 0.6$ and $\tau_n = 0.058$, we have $D = 0.204$, and D_1 is obtained from

$$D_1 = D + \sqrt{2\tau_n} = 0.544$$

The maximum inductor current is given by

$$I_{L\max} = \frac{1}{L}V_{\text{in}}DT = 8.165\ \text{A}$$

Table 4.1 shows the summary of equations for the three basic converters.

Table 4.1 Summary of ccm Equations

	ccm	dcm		
Converter type	$\frac{V_o}{V_{\text{in}}}$	$\frac{V_o}{V_{\text{in}}}$	D_1	$\frac{V_o}{V_{\text{in}}}$ (in terms of D and τ_n)
Buck	D	$\frac{D}{D_1}$	$\frac{1}{\frac{D}{4\tau_n}\left[\sqrt{\frac{8\tau_n}{D}+1}-1\right]}$	$\frac{D^2}{4\tau_n}\left[\sqrt{\frac{8\tau_n}{D^2}+1}-1\right]$
Boost	$\frac{1}{1-D}$	$\frac{D_1}{D_1-D}$	$D_1=\frac{\tau_n}{D}+D+\sqrt{\frac{\tau_n^2}{D^2}+2\tau_n}$	$\frac{1}{2}\left[1+\sqrt{1+\frac{2D^2}{\tau_n}}\right]$
Buck-boost	$\frac{D}{1-D}$	$\frac{D_1}{D_1-D}$	$D+\sqrt{2\tau_n}$	$D\sqrt{\frac{1}{2\tau_n}}$

EXERCISE 4.15

Consider a boost converter that delivers power to the load with the inductor voltage waveform shown in Fig. E4.15. Assume $R = 176\ \Omega$. Determine L.

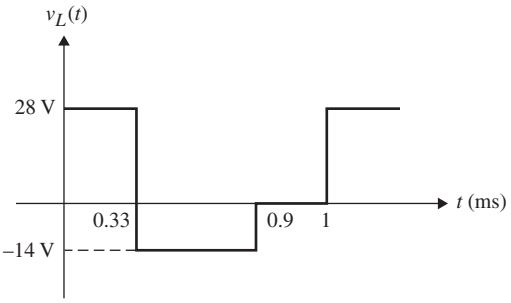


Figure E4.15

ANSWER 10.59 mH

4.4 THE EFFECTS OF CONVERTER NONIDEALITIES

The analysis thus far has been based on the assumption that all components, switching devices, and diodes are ideal. Depending on the application and power levels, the inclusion of some parasitic effects of both components and devices is very important to the design for acceptable performance. In this section, we are going to study the second-order nonideality effects on output voltage and efficiency. The following nonideal characteristics will be investigated:

1. Inductor resistance (r_L)
2. Transistor and diode voltage drops (V_Q, V_D)
3. Switching and conduction losses (r_{sw})

Other nonidealities include the equal series resistance of the output capacitor, r_{ESR}, which is important to include since its presence affects the design of the closed-loop compensator to stabilize the converter.

4.4.1 Inductor Resistance

The Buck Converter

To study the effect of inductor resistance on buck converter performance, we assume the inductor has a finite resistance, r_L, in series as shown in Fig. 4.52. The source of this resistive loss for a practical inductor are the core and copper losses.

When the switch is on, the inductor voltage is given by

$$V_{\text{in}} = r_L i_L + L\frac{di_L}{dt} + V_o$$

The first-order differential equation is obtained as

$$\frac{di_L}{dt} + \frac{i_L}{\tau} = \frac{1}{L}(V_{\text{in}} - V_o)$$

where $\tau = L/r_L$.

The general solution for i_L is given by

$$i_L(t) = (I_i - I_f)e^{-t/\tau} + I_f \tag{4.108}$$

The initial, I_i, and final, I_f, values must be determined in order to solve for $i_L(t)$.

At $t = DT$ we have

$$i_L(DT) = (I_i - I_f)e^{-DT/\tau} + I_f$$

and the final value, I_f, is given by

$$I_f = \frac{V_{\text{in}} - V_o}{r_L}$$

A typical sketch of $i_L(t)$ including inductor resistance is shown in Fig. 4.53.

Let I_i be the minimum inductor current at $t = 0$, $I_{L\min}$, and $I_{L\max}$ be the maximum at $t = DT$. Hence, using the above value for I_f, we obtain the following relation:

$$I_{L\max} = \left[I_{L\min} - \left(\frac{V_{\text{in}} - V_o}{r_L}\right)\right]e^{-DT/\tau} + \frac{V_{\text{in}} - V_o}{r_L} \tag{4.109}$$

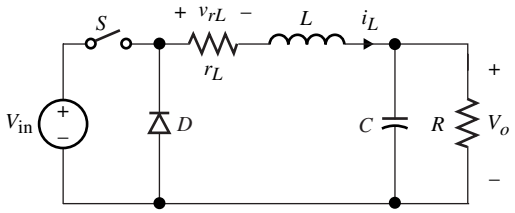


Figure 4.52 Buck converter with inductor resistance.

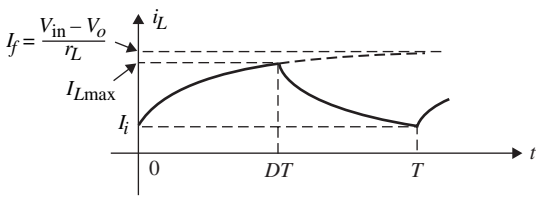


Figure 4.53 Inductor current including r_L.

When the diode is conducting, the inductor equation is given by

$$\frac{di_L}{dt} + \frac{r_L}{L} i_L = -V_o$$

The solution for i_L is given by

$$i_L(t) = (I_i - I_f)e^{(t-DT)/\tau} + I_f$$

The final value, I_f, is given by

$$I_f = \frac{-V_o}{r_L}$$

and the initial value, I_i, is $I_{L\max}$. Hence, $i_L(t)$ is given by

$$I_L(t) = \left(I_{L\max} + \frac{V_o}{r_L}\right)e^{-(t-DT)/\tau} - \frac{V_o}{r_L} \tag{4.110}$$

Evaluating $i_L(t)$ at $t = T$, we obtain

$$I_{L\min} = \left(I_{L\max} + \frac{V_o}{r_L}\right)e^{-T(1-D)/\tau} - \frac{V_o}{r_L} \tag{4.111}$$

where $i_L(t) = I_{L\min}$.

To solve for $i_L(t)$, expressions for $I_{L\min}$ and $I_{L\max}$ must be obtained from Eqs. (4.109) and (4.111) in terms of the circuit components.

By replacing the exponential function by its first two linear terms,

$$e^{-DT/\tau} \approx 1 - \frac{DT}{\tau} \tag{4.112a}$$

$$e^{-T(1-D)/\tau} \approx 1 - \frac{T}{\tau} + \frac{DT}{\tau} \tag{4.112b}$$

Eqs. (4.109) and (4.111) may be written as follows:

$$I_{L\min} = \left(I_{L\max} + \frac{V_o}{r_L}\right)\left(1 - \frac{T}{\tau} + \frac{DT}{\tau}\right) - \frac{V_o}{r_L} \tag{4.113a}$$

$$I_{L\max} = \left(I_{L\min} + \frac{(V_{\text{in}} - V_o)}{r_L}\right)\left(1 - \frac{DT}{\tau}\right) + \frac{V_{\text{in}} - V_o}{r_L} \tag{4.113b}$$

Further, it can be shown that the following equation may be obtained:

$$I_{L\max} \approx I_{L\min} \approx \frac{(V_{\text{in}}D - V_o)}{r_L} \tag{4.114}$$

Equation (4.114) suggests that the inductor ripple is approximated at zero.

Using the relation

$$I_o = \frac{I_{L\min} + I_{L\max}}{2} = \frac{V_o}{R}$$

we obtain

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{1 + \frac{r_L}{R}} \tag{4.115}$$

Notice as $r_L \longrightarrow 0$, the gain becomes D.

Another way to solve for the voltage gain is to assume the time constant τ is very large compared to the switching period, and the voltage across r_L is small compared to the input voltage V_{in}; hence, an approximation V_{rL} is calculated using the average value of inductor current. The plot for M vs. D for different r_L/R values is shown in Fig. 4.54.

The Boost Converter

To study the effect of inductor resistance on the boost converter performance, we again assume the inductor has a finite resistance, r_L, in series as shown in Fig. 4.55. The inductor current waveform is shown in Fig. 4.56.

Similar analysis gives the following inductor current equations:

$$i_L(t) = \left(I_{L\min} + \frac{V_{\text{in}}}{r_L}\right)e^{-t/\tau} - \frac{V_{\text{in}}}{r_L} \qquad 0 \le t < DT$$

$$i_L(t) = \left(I_{L\max} - \frac{V_{\text{in}} - V_o}{r_L}\right)e^{-(t-DT)/\tau} + \frac{V_{\text{in}} - V_o}{r_L} \qquad DT \le t < T$$

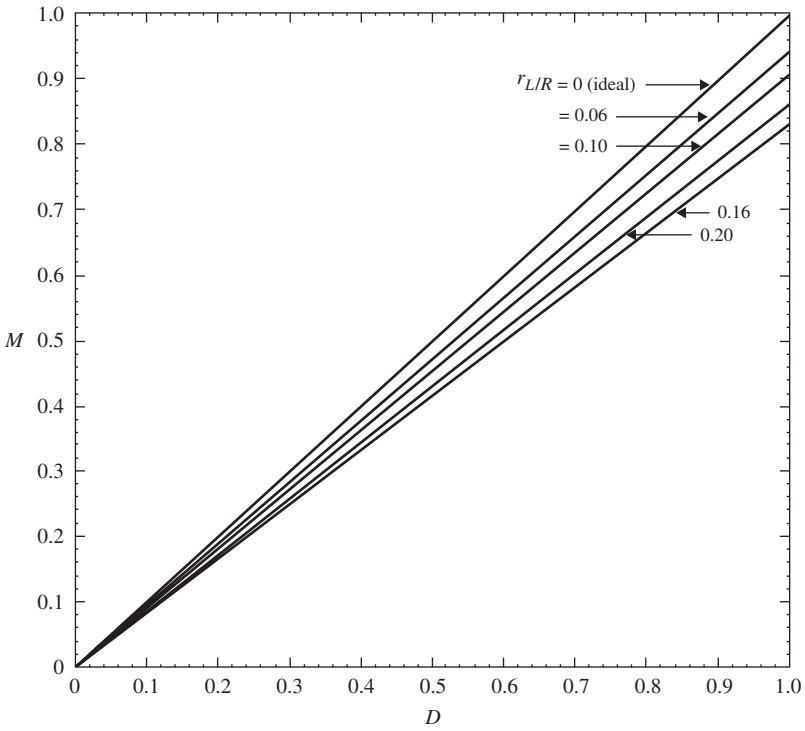


Figure 4.54 M vs. D under different inductor resistance values for the buck converter.

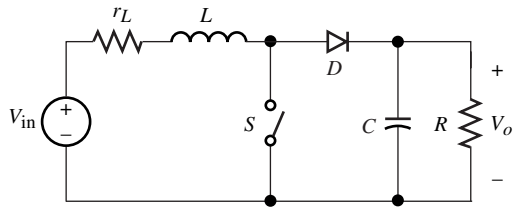


Figure 4.55 Boost converter with inductor resistance.

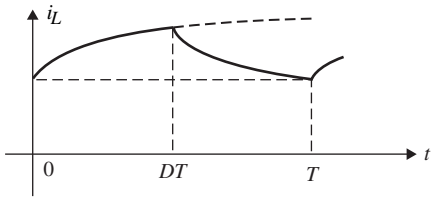


Figure 4.56 Boost inductor current.

where $i_L(0) = I_{L\min}$ and $i_L(DT) = I_{L\max}$. Using the same approximation we have applied to the buck converter, the maximum and minimum inductor currents can be approximated as follows:

$$I_{L\max} \approx I_{L\min} \approx -\frac{1}{r_L}[V_{\text{in}} - (1-D)V_o]$$

Using the average output current, which is given by,

$$I_o = \left(\frac{I_{L\max} + I_{L\min}}{2}\right)(1-D)$$

we obtain the equation for the voltage gain:

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{(1-D) + \dfrac{r_L}{R}\dfrac{1}{1-D}} \tag{4.116}$$

The plot of Eq. (4.116) is shown in Fig. 4.57.

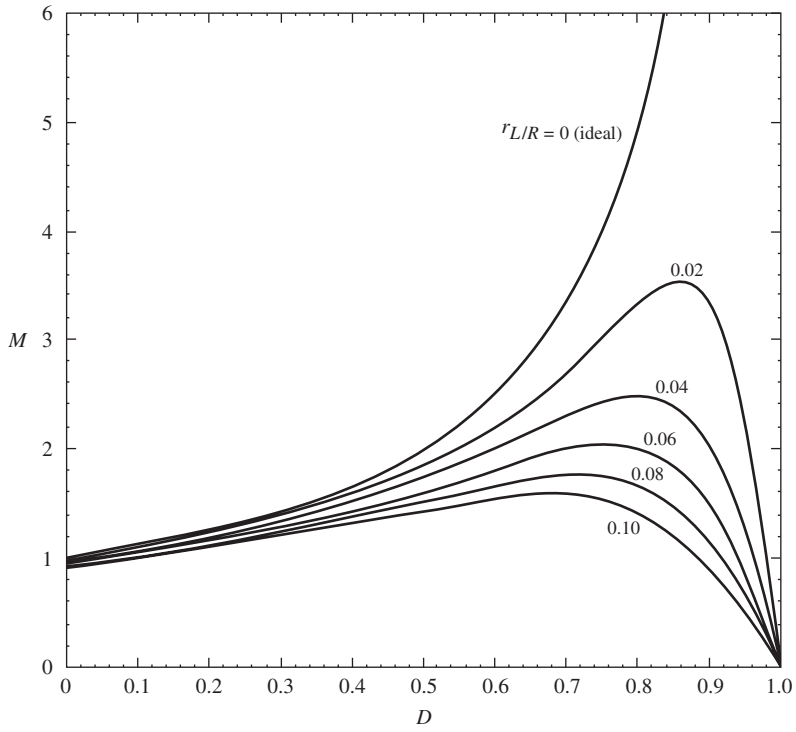


Figure 4.57 *M* vs. *D* under different inductor resistance values for the boost converter.

EXERCISE 4.16

Consider the buck-boost converter with inductor resistance shown in Fig. E4.16. Show that the voltage gain equation can be approximated by the following relation:

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{(1-D) + \dfrac{r_L}{R(1-D)}} \tag{4.117}$$

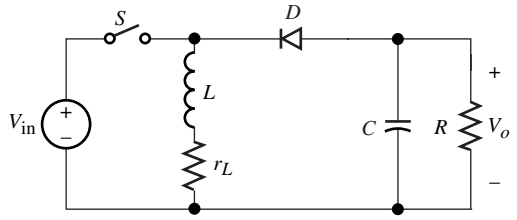


Figure E4.16 Buck-boost converter with inductor resistance.

whose plot is shown in Fig. 4.58.

4.4.2 Transistor and Diode Voltage Drop

As an illustration, let us consider the buck converter. Let us assume that when the transistor is on, a nonzero voltage drop across it, V_Q, is present; and when the diode is

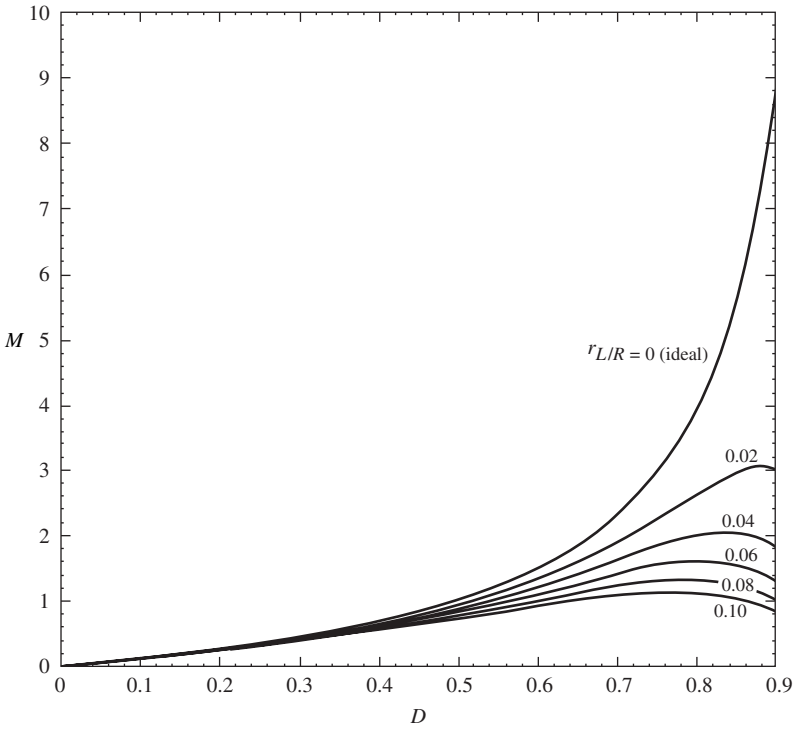


Figure 4.58 *M* vs. *D* under different inductor resistance values for the buck-boost converter.

turned on, a voltage V_D appears across it. Hence, the voltage across the inductor while the transistor and diode are conducting is given by

$$\text{Switch on:} \quad v_L = V_{\text{in}} - V_o - V_Q \qquad 0 \le t < DT$$
$$\text{Switch off:} \quad v_L = -V_o - V_D \qquad DT \le t < T$$

Hence, the inductor currents are given by

$$i_L(t) = \frac{1}{L}(V_{\text{in}} - V_o - V_Q)t + I_{L\min} \qquad 0 \le t \le DT$$

$$i_L(t) = \frac{1}{L}(-V_o - V_D)(t - DT) + I_{L\max} \qquad DT \le t \le T$$

Evaluating the above equations at $t = DT$ and T, we obtain

$$i_{L\max} = \frac{1}{L}(V_{\text{in}} - V_o - V_Q)DT + I_{L\min}$$

$$i_{L\min} = \frac{1}{L}(-V_o - V_D)(1 - D)T + I_{L\max}$$

Using this input and output average power, the voltage conversion is given by

$$\frac{V_o}{V_{\text{in}}} = D - D\frac{V_Q}{V_{\text{in}}} - \frac{V_D}{V_{\text{in}}}(1 - D)$$

If we normalize voltages by V_{in}, we obtain,

$$M = D\left(1 - V_{nQ} - V_{nD}\left(\frac{1}{D} - 1\right)\right) \tag{4.118}$$

where V_{nQ} and V_{nD} are the normalized transistor and diode voltage drops.

EXERCISE 4.17

Derive the normalized voltage gain expression for the boost converter by including V_{nQ} and V_{nD}.

ANSWER $M = 1 - V_{nD} - \dfrac{D}{1 - D}V_{nQ} + \dfrac{D}{1 - D}$

EXERCISE 4.18

Show that gain for the buck-boost converter is given by the following equation when including the diode and switch voltage drops.

$$M = \frac{(1 - V_{nQ})D - (1 - D)V_{nD}}{1 - D} \tag{4.119}$$

4.4.3 Switch Resistance

To study the effect of switching resistance on the converter's performance, we assume the inductor has a finite resistance, r_{sw}, as shown in Fig. 4.59. The resultant inductor current is shown in Fig. 4.60.

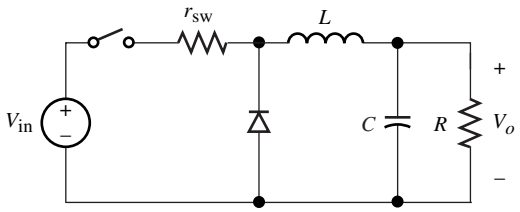


Figure 4.59 Buck converter with switching resistance.

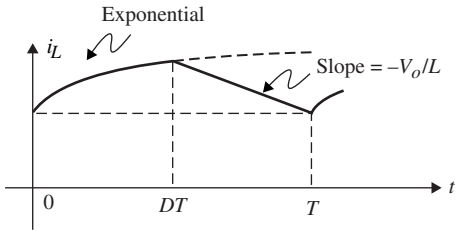


Figure 4.60 Inductor current for Fig. 4.59.

The inductor current equations are given for the *on* and *off* times of the switch as follows:

$$i_L(t) = \left(I_{L\min} - \frac{V_{\text{in}} - V_o}{r_{\text{sw}}}\right)e^{-t/\tau} + \frac{V_{\text{in}} - V_o}{r_{\text{sw}}} \qquad 0 \le t < DT$$

$$i_L(t) = \frac{V_o}{L}(t - DT) + I_{L\max} \qquad DT \le t < T$$

where τ is the time constant and equals L/r_{sw}.

Using the same approximation applied to the inductor resistance, we obtain the following expression for $I_{L\max}$ and $I_{L\min}$:

$$I_{L\max} \approx \frac{1 - DV_{\text{in}} - V_o}{Dr_{\text{sw}}}$$

$$I_{L\min} = -\frac{V_o}{L}(1 - D)T + \frac{DV_{\text{in}} - V_o}{Dr_{\text{sw}}}$$

$$I_o = \frac{V_o}{R} = \frac{I_{L\max} + I_{L\min}}{2}$$

Hence, the voltage gain is given by

$$M = \frac{1}{\dfrac{1}{D} + \dfrac{1 - D}{2\tau/T} + \dfrac{r_{\text{sw}}}{R}} \tag{4.120}$$

Again assuming $\tau/T \gg 1 - D$, we obtain

$$M = \frac{D}{1 + D\dfrac{r_{\text{sw}}}{R}} \tag{4.121}$$

Typically, for a MOSFET, $r_{\text{sw}} = r_{DS(\text{ON})} = 0.15\ \Omega$.

A plot of M vs. D for the buck converter under different values of r_{sw}/R is shown in Fig. 4.61. Figures 4.62 and 4.63 show the plots for M vs. D under different values of r_{sw}/R for the boost and buck-boost, respectively.

EXERCISE 4.19

Show that the gain expressions for the boost and buck-boost converters including the switch resistance, r_{sw}, are

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D + \left(\frac{D}{1-D}\right)\frac{r_{sw}}{R}} \tag{4.122}$$

$$\frac{V_o}{V_{in}} = \frac{D}{1 - D + \left(\frac{D}{1-D}\right)\frac{r_{sw}}{R}} \tag{4.123}$$

EXAMPLE 4.12

A buck converter is modeled by including a switch resistance, r_{sw}, an inductor resistance, r_L, and a diode voltage drop, V_D. Assume $V_{in} = 50$ V, $V_D = 0.9$ V, $V_o = 20$ V, $R = 4\ \Omega$, $r_{sw} = 0.08\ \Omega$, $r_L = 0.06\ \Omega$.

(a) Derive the relation for V_o/V_{in} that includes the above effects.

(b) Find the duty cycle, D.

(c) Find the efficiency, $\eta = P_o/P_{in}$.

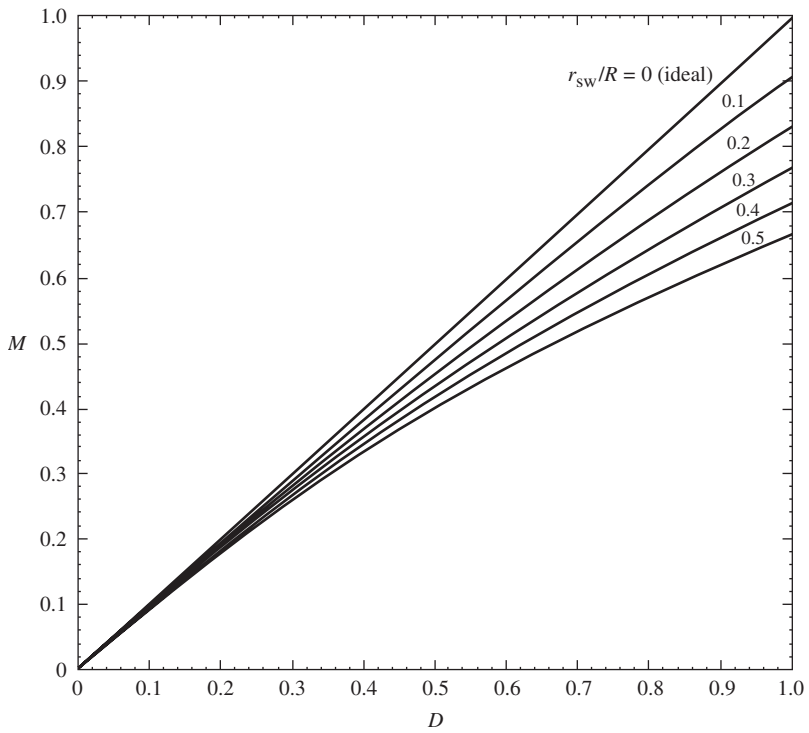


Figure 4.61 M vs. D for the buck converter under different values of r_{sw}/R.

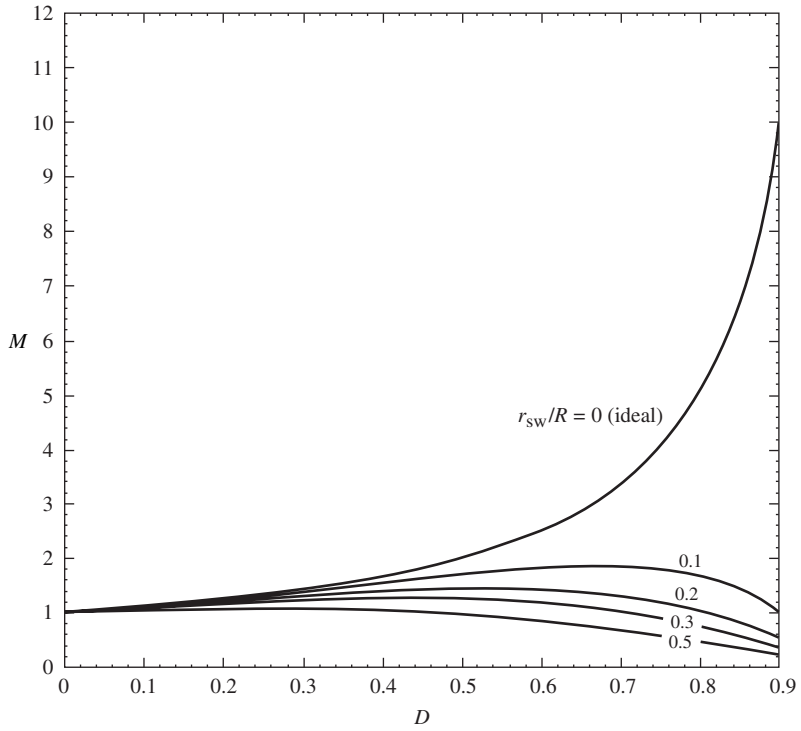


Figure 4.62 M vs. D under different values of r_{sw}/R for the boost converter.

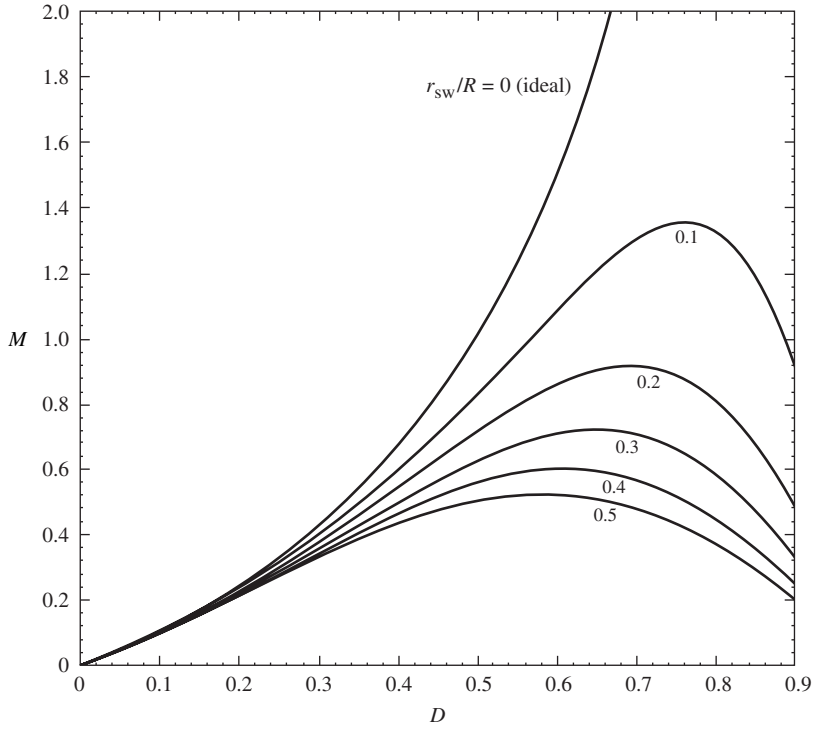


Figure 4.63 M vs. D under different values of r_{sw}/R for the buck-boost converter.

SOLUTION

(a) The inductor current relations are given by

$$I_{L\max} - I_{L\min} = \left(\frac{V_{\text{in}} - I_L(r_L + r_{\text{sw}}) - V_o}{L}\right)DT$$

$$I_{L\min} - I_{L\max} = \left(\frac{V_o - I_L r_L + V_D}{L}\right)(1-D)T$$

$$I_L = \frac{V_o}{R}$$

These result in

$$\frac{V_o}{V_{\text{in}}} = \frac{D\left(1 + \dfrac{V_D}{V_{\text{in}}}\right) - \dfrac{V_D}{V_{\text{in}}}}{1 + \dfrac{r_L}{R} + D\dfrac{r_{\text{sw}}}{R}} \tag{4.124}$$

(b) Substituting for $V_{\text{in}} = 50$ V, $V_D = 0.9$ V, $V_o = 20$ V, $R = 4\ \Omega$, $r_{\text{sw}} = 0.08\ \Omega$, $r_L = 0.06\ \Omega$, we obtain $D = 0.42$.

(c) The power loss in the inductor and switch resistors is given by

$$P_{\text{loss}} = (I_{\text{in}})^2 r_{\text{sw}} + (I_L)^2 r_L$$

$$I_{\text{in}} = DI_o = D\frac{V_o}{R} = (0.42)\frac{20}{4} = 2.1$$

$$I_o = 5 \text{ A}$$

$$P_{\text{loss}} = (2.1)^2(0.08) + (5)^2(0.06) = 0.353 + 1.5 = 1.853 \text{ W}$$

$$P_{\text{in}} = V_{\text{in}} I_{\text{in}} = (50)(2.1) = 105 \text{ W}$$

$$P_o = V_o I_L = (20)(5) = 100 \text{ W}$$

The total loss is 5 W, and the efficiency, η, is given by

$$\eta = \frac{100}{105}100\% = 95.2\%$$

EXERCISE 4.20

Derive the voltage gain equation for the buck-boost converter by including the switch resistance, r_{sw}, and the inductor resistance, r_L.

ANSWER

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{(1-D) + \dfrac{r_L}{R(1-D)} + \left(\dfrac{D}{1-D}\right)\dfrac{r_{\text{sw}}}{R}}$$

---

dc Transformer Model

We can develop the dc transformer equivalent circuit model by including the converter nonidealities discussed above. Such linear circuit models are very useful when it comes to solving for voltage conversion, average current gain, and efficiency. This is because linear circuit analysis techniques that are well understood by design engineers can be employed in solving these models.

By inspection, it can be seen that the dc transformer equivalent circuit for the buck converter of Fig. 4.64 is given in Fig. 4.65. The derivation of the model is quite simple. All we need to do is to write the dc equation relating V_{in}, V_o, I_{in}, D, and I_o during modes 1 and 2. For example, for the buck converter of Fig. 4.64, we have the following relations for $v_L(t)$:

$$v_L(t) = V_{\text{in}} - V_Q - (r_L + r_{\text{on}}D)I_o - V_o \qquad 0 \le t < DT \qquad (4.125a)$$

$$v_L(t) = -V_D - V_o - (r_D(1-D) + r_L)I_o \qquad DT \le t < T \qquad (4.125b)$$

Under dc conditions, the average inductor voltage is zero,

$$\frac{1}{T}\int_0^T v_L(t)dt = 0$$

This integral yields the following dc equation:

$$D[V_{\text{in}} - V_o - V_Q - (r_L + r_{\text{on}}D)I_o] + (1-D)[-V_D - V_o - (r_D(1-D) + r_L)I_o] = 0$$

Rearrange the terms in terms of V_{in}, V_o/D, and DI_o to obtain

$$V_{\text{in}} = \frac{V_o}{D} + V_Q + \frac{1-D}{D}V_D + \left[r_{\text{on}} + \left(\frac{1-D}{D}\right)^2 r_D + \frac{r_L}{D^2}\right]DI_o = 0 \qquad (4.125)$$

It can be easily seen that the above equation can be represented by the dc equivalent model shown in Fig. 4.66(*a*). The simplified equivalent circuit is shown in Fig. 4.66(*b*), where

$$r_{\text{eq}} = r_{\text{on}} + \left(\frac{1-D}{D}\right)^2 r_D + \frac{r_L}{D^2}$$

$$V_{\text{eq}} = V_{\text{in}} - V_Q - \frac{1-D}{D}V_D$$

$$n = D$$

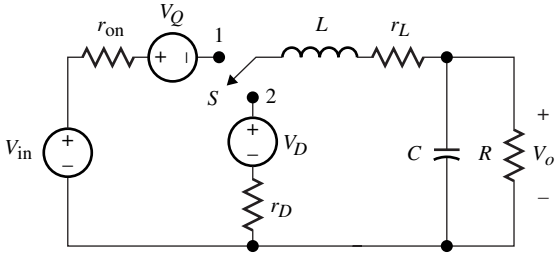


Figure 4.64 Buck converter with component nonidealities.

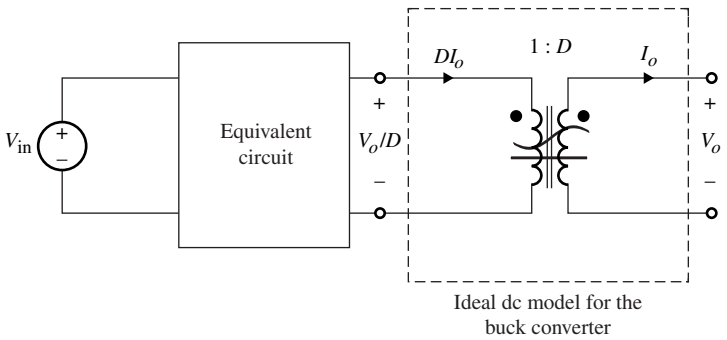


Figure 4.65 Transformer equivalent circuit diagram for a buck converter.

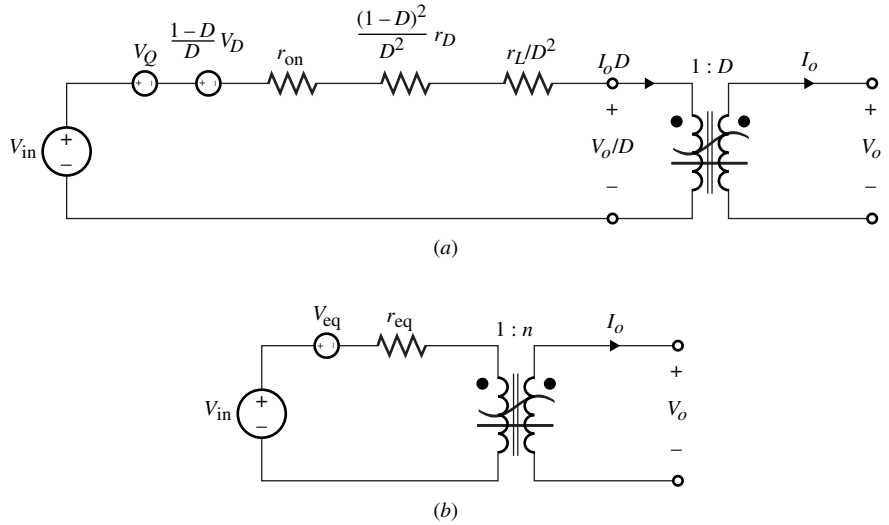
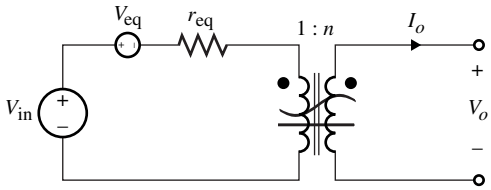


Figure 4.66 (*a*) dc equivalent circuit for the buck converter of Fig. 4.64. (*b*) Simplified equivalent circuit.

Table 4.2 dc Equivalent Circuit Model



	Buck	*Boost*	*Buck-Boost*
n	D	$\frac{1}{1-D}$	$\frac{D}{1-D}$
r_{eq}	$r_{on}+\left(\frac{1-D}{D}\right)^2 r_D+\frac{r_L}{D^2}$	$r_L+D^2r_{on}+(1-D)^2r_D$	$r_{on}+r_D\left(\frac{1-D}{D}\right)^2+r_L\left[1+\left(\frac{1-D}{D}\right)^2\right]$
V_{eq}	$V_Q+\frac{1-D}{D}V_D$	$(1-D)V_D+DV_Q$	$V_Q+\frac{1-D}{D}V_D$

Similarly, we can obtain the dc equivalent circuits for the boost and buck-boost. Table 4.2 shows the values for V_{eq}, r_{eq}, and the transformer ratio for the buck, boost, and buck-boost.

EXERCISE 4.21

Show that the transformer equivalent circuit model for a boost converter that includes r_L, r_{on}, V_D, and V_Q is as shown in Fig. 4.66(*a*) with $n = 1/(1-D)$, $r_{eq} = r_L + D^2 r_{on}$, and $V_{eq} = (1-D)V_D + DV_Q$.

4.5 SWITCH UTILIZATION FACTOR

It is possible to evaluate the use of the power switch in the buck, boost, buck-boost, and Weinberg converters by investigating the average switch power-handling capability with respect to the average power delivered to the load. Figure 4.67 shows a block diagram representation for any switch-mode power converter, where

I_o = average load current

V_o = average load voltage

$I_{\text{sw,max}}$ = maximum current through the switch when turned on

$V_{\text{sw,max}}$ = maximum voltage across the switch when turned off

Let us define the switch maximum power as

$$P_{\text{sw,max}} = V_{\text{sw,max}} I_{\text{sw,max}}$$

and the average output power is given by

$$P_o = V_o I_o$$

Then we define the switch utilization factor (K_{sw}) as the ratio of $P_{\text{sw,max}}$ and P_o:

$$K_{\text{sw}} = \frac{P_o}{P_{\text{sw,max}}} \tag{4.127}$$

EXAMPLE 4.13

Determine K_{sw} for the buck converter.

SOLUTION The maximum switch current and voltage expressions are given by Eqs. (4.128) and (4.129), respectively,

$$I_{\text{sw,max}} = DV_{\text{in}}\left[\frac{1}{R} + \frac{(1-D)T}{2L}\right] \tag{4.128}$$

$$V_{\text{sw,max}} = V_{\text{in}} \tag{4.129}$$

and the maximum switch power is given by

$$P_{\text{sw,max}} = I_{\text{sw,max}} V_{\text{sw,max}}$$

$$= DV_{\text{in}}^2\left[\frac{1}{R} + \frac{(1-D)T}{2L}\right]$$

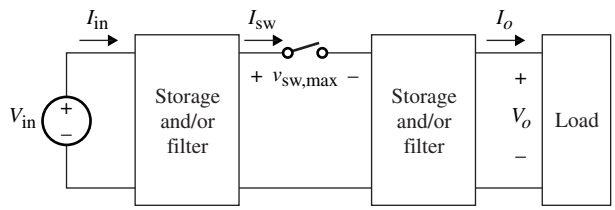


Figure 4.67 Block diagram for switch-mode power converter.

The average output power is given by

$$P_o = \frac{V_o^2}{R}$$

Therefore, the switch utilization factor, K_{sw}, is

$$K_{\text{sw}} = \frac{V_o^2/R}{DV_{\text{in}}^2\left[\frac{1}{R} + \frac{(1-D)T}{2L}\right]}$$

$$= \frac{D}{1 + \frac{(1-D)RT}{2L}}$$

Using the normalized time constant, $\tau_n = L/RT$, K_{sw} can be expressed as

$$K_{\text{sw}} = \frac{D}{1 + \frac{(1-D)}{2\tau_n}}$$

Figure 4.68 shows a plot of K_{sw} vs. D under different values of τ_n for the buck converter.

Similarly, it can be shown that the switch utilization factor for the boost and buck-boost converters are given in Eqs. (4.131) and (4.132), respectively.

$$K_{\text{sw}} = \frac{1}{\frac{1}{1-D} + \frac{(1-D)D}{2\tau_n}} \tag{4.131}$$

$$K_{\text{sw}} = \frac{D}{\frac{1}{1-D} + \frac{(1-D)}{2\tau_n}} \tag{4.132}$$

Figures 4.69 and 4.70 show the plots of K_{sw} vs. D under different values of τ_n for the boost and buck-boost, respectively.

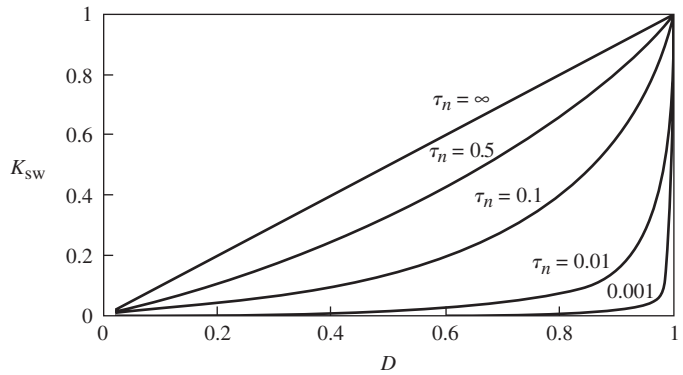


Figure 4.68 K_{sw} vs. D under different values of τ_n for the buck converter.

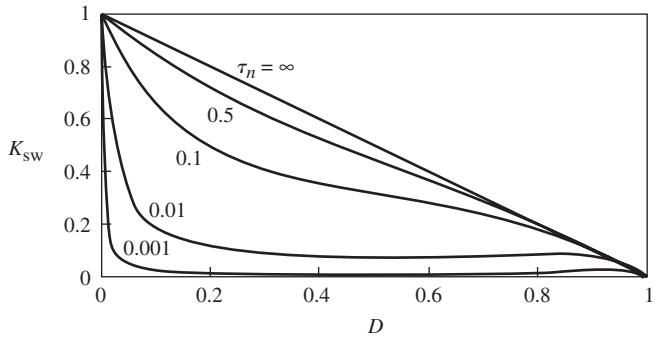


Figure 4.69 K_{sw} vs. D under different values of τ_n for the boost.

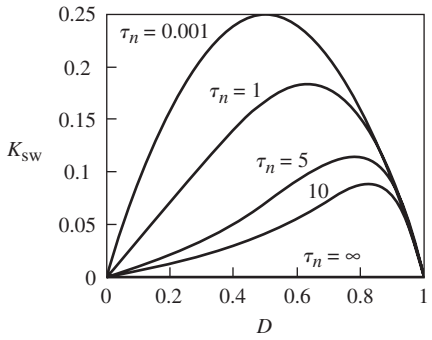


Figure 4.70 K_{sw} vs. D under different values of τ_n for the buck-boost.

EXERCISE 4.22

Show that the switch utilization factor for the boost and the buck-boost are given in Eqs. (4.131) and (4.132).

PROBLEMS

Continuous Conduction Mode

Buck Converter

4.1 Consider the following specifications for a buck converter:

$$V_{in} = 80 \text{ V}$$
$$R_o = 9\ \Omega$$
$$P_o = 100 \text{ W}$$
$$f_s = 150 \text{ kHz}$$

Determine:

(a) The inductor value at the boundary condition (critical value L_{crit})

(b) The maximum inductor current value for $L = 10L_{crit}$

(c) The diode rms and average current values

4.2 Derive the expressions for $v_c(0)$ and $v_c(DT)$ for a buck converter operating in ccm whose current waveform is drawn in Fig. P4.2.

4.3 Consider the buck converter with $V_{in} = 25$ V, $V_o = 12$ V at $I_o = 2$ A, $f_s = 50$ kHz. Determine:

(a) The duty cycle, D

(b) L_{crit}

(c) I_{Lmin}, I_{Lmax}, $I_{o,ave}$, $I_{in,ave}$ for $L = 100L_{crit}$

(d) Output voltage ripple for $C = 0.47\ \mu$F

(e) C for $|V_c| = 2\%$ of V_o

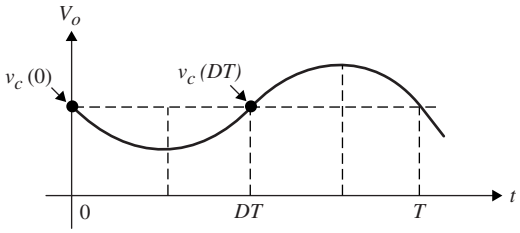


Figure P4.2

4.4 Derive the expressions for the inductor and capacitor rms currents for the buck. Find these values for Problem 4.3.

D4.5 (a) Design a buck converter for the following specifications:

$$\Delta V_o/V_o = 0.1\%, \qquad V_{\text{in}} = 40 \text{ V},$$
$$P_{o,\text{ave}} = 20 \text{ W}, f_s = 75 \text{ kHz}, D = 0.5$$

(b) What is the inductor current's peak-to-peak value?

(c) What are the diode and switch rms current values?

D4.6 Consider a buck converter with $V_{\text{in}} = 48$ V, $V_o = 27$ V at $I_o = 8$ A, and $f_s = 50$ kHz. Design for L and C such that the peak value of the inductor current does not exceed 15% of its average value, and the capacitor peak voltage does not exceed 2% of its average value.

D4.7 Consider the buck converter of Problem 4.6 by assuming the input voltage varies by ±20% and the output current varies from 10 A to 6 A. Redesign for L and C using the same specifications with V_{in}(nominal) = 48 V, $V_o = 27$ V, and $f_s = 50$ kHz.

4.8 Determine the diode and switch rms and peak current and voltage ratings for the design of Problem 4.6.

4.9 Determine the circuit parameters including V_{in}, D, f_s, C, L, and $I_{L\max}$ and $I_{L\min}$ for a buck converter whose capacitor voltage is given in Fig. P4.9.

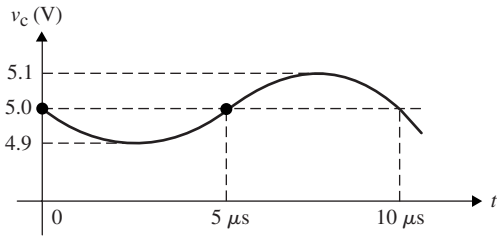


Figure P4.9

D4.10 Design the buck converter to operate in ccm with the following specifications: $V_{\text{in, max}} = 48$ V, $V_{\text{in, nom}} = 32$ V, $V_o = 12$ V, $I_{o,\text{max}} = 4$ A, $I_{o,\text{min}} = 0.5$ A, $f_s = 50$ kHz, and $\Delta V_o = 120$ mV.

Boost Converter

D4.11 Design a boost converter with the following specifications:

$$V_{\text{in}} = 28 \text{ V}, V_o = 48 \text{ V}, P_o = 100 \text{ W},$$
$$f_s = 110 \text{ kHz}, 2\% \text{ output voltage ripple}$$

4.12 Sketch the inductor current for the boost converter shown in Fig. P4.12. Assume ccm operation with $D = 0.4$.

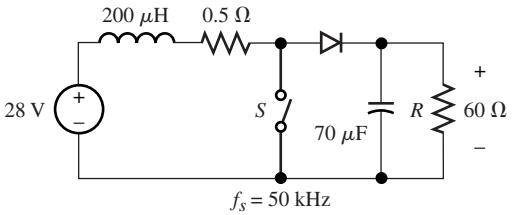


Figure P4.12

D4.13 Design a boost converter to deliver 80 V at 4 A from a 60 V source with an output ripple voltage not to exceed 1%. Assume $f_s = 20$ kHz.

4.14 The source for a boost converter has an internal resistance R_s as shown in Fig. P4.14. Derive expressions for:

(a) V_o/V_{in}

(b) The efficiency, $\eta = \dfrac{P_{o,\text{ave}}}{P_{\text{in, ave}}}$

(c) The duty cycle at which the output voltage is maximized

Your expressions should be given as a function of R/R_s and D.

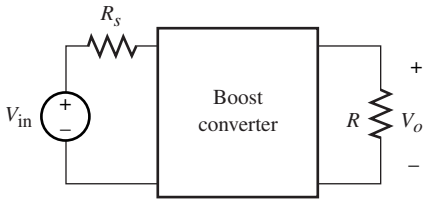


Figure P4.14

D4.15 Design a boost converter for the following requirements: $P_o = 20$ W, $V_{\text{in}} = 20$ V, $D = 0.35$, and 1% output voltage ripple.

4.16 Determine ΔV_o for a boost converter with $V_{\text{in}} = 12$ V, $V_o = 15$ V at $I_o = 250$ mA. Use $L = 150$ μH, $C = 470$ μF, and $f_s = 20$ kHz. Sketch the capacitor voltage and inductor current.

4.17 Derive the capacitor and inductor current rms values for Problem 4.16.

4.18 Derive the expressions for V_o/V_{in} for the boost by including r_L and r_{sw}.

4.19 Derive the expressions for V_o/V_{in} for the boost by including V_D and V_Q.

D4.20 Design a boost converter to operate in ccm with the following specifications:

$$V_{\text{in, min}} = 90 \text{ V}, V_{\text{in, max}} = 150 \text{ V},$$
$$V_{\text{in, nom}} = 120 \text{ V}, V_o = 152 \text{ V}, I_{o,\text{max}} = 2 \text{ A},$$
$$I_{o,\text{min}} = 0.2 \text{ A}, f_s = 50 \text{ kHz}, \Delta V_o/V_o = 1\%$$

Buck-Boost Converter

D4.21 Consider a buck-boost converter with the following specifications:

$$V_o = 12 \text{ V}, P_o = 25 \text{ W}, V_{\text{in}} = 24 \text{ V},$$
$$f_s = 100 \text{ kHz}, \Delta V_o/V_o = 1\%$$

(a) Design the converter so it operates in the ccm.

(b) Find the maximum inductor current under both operating modes.

(c) If the load changes by 50% (lighter load, R increases), determine the new mode of operation.

(d) Sketch $i_c(t)$ and $v_c(t)$ for parts (*a*) and (*b*).

4.22 Consider the following values for a buck-boost converter:

$$V_{\text{in}} = 30 \text{ V}, D = 0.25, R = 2\ \Omega, L = 330\ \mu\text{H},$$
$$f_s = 10 \text{ kHz}$$

(a) Determine the mode of operation.

(b) Sketch i_L.

(c) Determine V_o.

(d) Determine C for a 1% output ripple.

(e) At what value of D does the transition between ccm and dcm occur?

4.23 Consider a buck-boost converter that supplies 100 W to $V_o = 30$ V from a 50–30 V dc source. Let $T = 100$ μs and $L = 800$ μH.

(a) Determine the range of D for the given range of source voltage.

(b) Determine the average input current, diode current, $I_{L\text{max}}$, and $I_{L\text{min}}$, under $V_{\text{in}} = 35$ V.

(c) Determine the rms value of the diode current and the capacitor current under $V_{\text{in}} = 35$ V.

(d) Design for C so that the output ripple voltage is limited to 2% of V_o under $V_{\text{in}} = 30$ V.

(e) If the load resistor is changed so that the converter load current is decreased by 10%, what is the new duty cycle when $V_{\text{in}} = 35$ V?

4.24 For stability considerations, sometimes it is required that the equivalent series resistance (ESR) of the output capacitor be included in modeling the power stage of a PWM converter. Fig. P4.24 shows

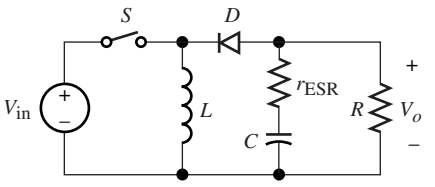


Figure P4.24

a buck-boost converter including r_{ESR}. Derive the expression for the output ripple.

4.25 Repeat Problem 4.4 for a buck-boost converter.

D4.26 Redesign Problem 4.5 for a buck-boost converter.

D4.27 Redesign Problem 4.13 for a buck-boost converter.

4.28 Derive the expression for V_o/V_{in} for the buck-boost converter by including r_L.

4.29 Derive the expression V_o/V_{in} for the buck-boost by including V_D and V_Q.

4.30 Derive the expression for V_o/V_{in} for the buck-boost converter by including r_{sw}.

Fourth-Order Converters

4.31 Derive the expression for V_o/V_{in} for the Zeta converter by including r_L.

4.32 Derive the expression for V_o/V_{in} for the Cuk converter by including V_D and V_Q.

4.33 Derive the expression for V_o/V_{in} for the Cuk converter by including r_{sw}.

4.34 Determine the output voltage ripple equation for the Cuk and Zeta converters.

4.35 Consider the Cuk converter of Fig. P4.35.

(a) Sketch the waveforms for i_{L1}, i_{L2}, i_D, and i_s assuming constant voltages across C_1 and C_2.

(b) Determine the rms current values in the diode and switch.

(c) What is the ripple voltage across C_1 and C_2?

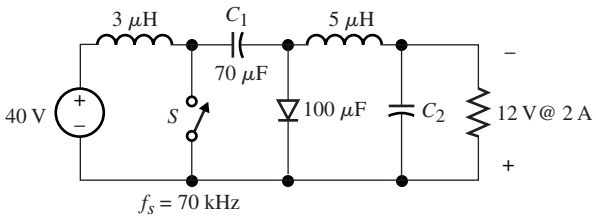


Figure P4.35

4.36 Derive the voltage gain equation for the single-ended primary inductance converter (SEPIC) shown in Fig. E4.11(*a*).

4.37 Derive the rms expressions for the inductor and diode currents for the Cuk converter.

D4.38 (a) Derive the voltage gain expression for the SEPIC converter operating in the dcm.

(b) Design the converter for the following specifications:

$$V_{\text{in}} = 45\text{ V},\ V_o = 15\text{ V},\ P_o = 25\text{ W},$$
$$f_s = 50\text{ kHz}$$

(i) The maximum inductor ripple current should not exceed 15% of its average value.

(ii) The maximum voltage ripple across C_1 should not exceed 5% of its average value.

(iii) The maximum output voltage ripple is less than 0.1%.

4.39 Develop an equivalent circuit for the cascaded boost and buck-boost converters.

4.40 Derive the voltage gain expression for the cascaded arrangement in Problem 4.39.

Discontinuous Conduction Mode

4.41 Consider the buck converter of Problem 4.1.

(a) Determine the voltage gain for $L = 0.1L_{\text{crit}}$.

(b) Determine D_1.

4.42 Derive the ripple voltage for the buck converter operating in the dcm.

4.43 Derive the ripple voltage for the buck-boost converter operating in the dcm.

4.44 Consider a boost converter with $L = 67\ \mu$H, $V_{\text{in}} = 60$ V, $f_s = 20$ kHz, $C = 10\ \mu$F, $V_o = 80$ V at $I_o = 4$ A.

(a) Determine the mode of operation.

(b) Repeat part (*a*) for $I_o = 2$ A.

(c) Sketch i_e, V_D, and V_c for parts (*a*) and (*b*).

(d) Determine D and D_1 for $V_o = 80$ V at (*i*) $I_o = 4$ A and (*ii*) $I_o = 2$ A.

(e) Repeat part (*d*) for $V_{\text{in}} = 65$ V.

4.45 Determine the expressions for the diode and transistor currents of the buck-boost operating in the dcm.

D4.46 Design the buck-boost converter to operate in the dcm with the following specifications:

$$V_{\text{in}} = 18\text{ V},\ V_o = -38\text{ V},\ I_{o,\max} = 2\text{ A},$$
$$I_{o,\min} = 0.2\text{ A}, f_s = 95\text{ kHz}, \Delta V_o = 180\text{ mV}.$$

4.47 Derive the following expressions for the buck-boost converter operating in the dcm:

$$M = \frac{D}{\sqrt{2\tau_n}}$$

$$D_1 = D + \sqrt{2\tau_n}$$

where

$$\tau_n = \frac{\tau}{T}$$

$$\tau = L/R$$

4.48 Derive the expression for the voltage ripple for the boost converter operating in dcm. Also give an expression for the capacitor voltage at $t = 0$ and $t = DT$ in terms of the circuit parameters.

4.49 Repeat Problem 4.21 under dcm operation.

4.50 Derive the voltage gain for the Cuk converter operating in the dcm.

4.51 Derive the expressions for M and D_1 for the Cuk converter when it operates in the dcm. (dcm operation for the Cuk converter is assumed only when both inductor currents are discontinuous.)

4.52 (a) Derive the expression for ΔV_o (peak-to-peak) for a buck converter operating in the dcm.

(b) Determine ΔV_o for a boost converter for $V_{\text{in}} = 12$ V, $V_o = 15$ V, and $I_o = 250$ mA. Use $L = 150\ \mu$H, $C = 470\ \mu$F, and $f_s = 20$ kHz.

Other Converter Topologies

4.53 Derive the expression for the voltage gain for the two-switch PWM converter shown in Fig. P4.53.

S_1 and S_2 are switched simultaneously. Assume $RC >> T$. Compare this converter to the single-switch buck-boost converter.

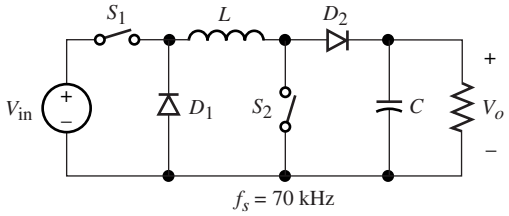


Figure P4.53

4.54 It is possible to develop a basic switched-mode dc converter by using constant input and output current sources. Such converters are called *current inverters.* Figure P4.54 shows the three basic current converters: buck, boost, and buck-boost. Assume L/R is very large compared to the switching frequency so that I_o is assumed constant. Show that the current gains for these topologies are given by, respectively,

$$\textbf{(a)}\ \frac{I_o}{I_{in}} = (1 - D)$$

$$\textbf{(b)}\ \frac{I_o}{I_{in}} = \frac{1}{D}$$

$$\textbf{(c)}\ \frac{I_o}{I_{in}} = \frac{1 - D}{D}$$

4.55 Show that the critical capacitor value that will produce a continuous capacitor voltage for the buck converter in Fig. P4.54(*a*) is given by

$$C_{crit} \geq \frac{D^2 T}{2R}$$

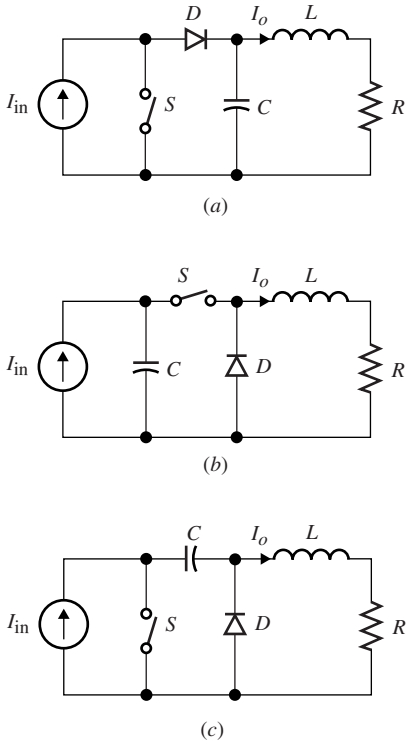


Figure P4.54

4.56 Consider the circuits shown in Fig. P4.56 with V_o and I_o constants, i.e., $RC>>T$ and $L/R>>T$. The input current and voltage squarewaves are as shown. Derive the expressions for the inductor and capacitor ripples in terms of the circuit parameters.

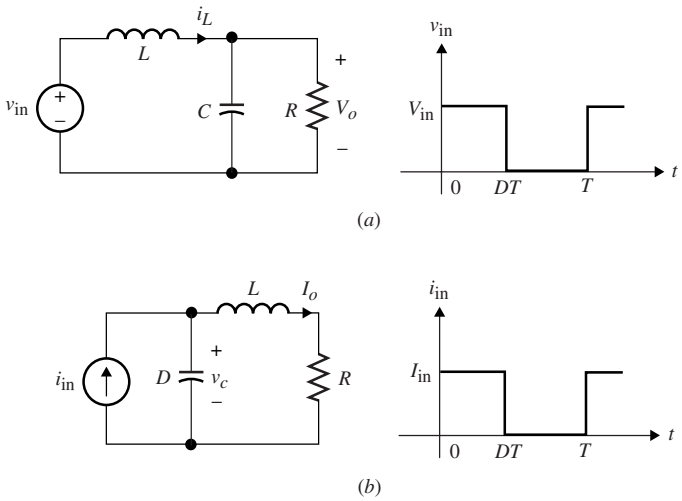


Figure P4.56

4.57 Repeat Problem 4.56 for Fig. P4.57, where $1 \le \beta < 2$.

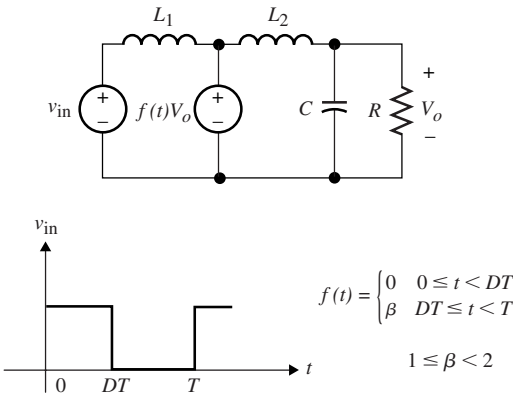


Figure P4.57

4.58 Derive the dc and fundamental components of the Fourier series for the input current in the buck converter.

Additional General Problems

4.59 Derive the rms expressions for the inductor and diode currents for the buck converter.

4.60 Derive the rms expressions for the inductor and diode currents for the boost converter.

4.61 Derive the rms expressions for the inductor and diode currents for the buck-boost converter.

4.62 Consider the bidirectional double-switch buck converter shown in Fig. P4.62. Assume S_1 and S_2 are turned on and off simultaneously at duty ratio D. Show that the voltage gain is given by

$$\frac{V_o}{V_{in}} = 2D - 1$$

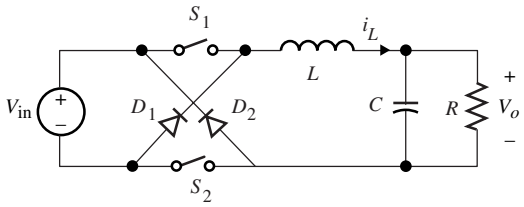


Figure P4.62

4.63 Derive the ripple voltage expression for the bidirectional converter of Problem 4.62.

D4.64 Design the three buck-boost converters needed to be used in the dc distributed power system in Fig. P4.64.

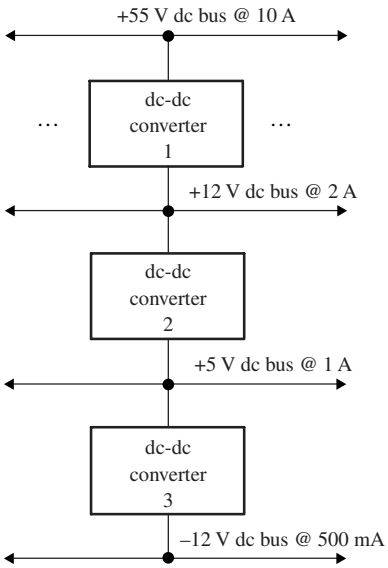


Figure P4.64

4.65 Show that the nth harmonic peak value for the diode voltage of the buck converter is given by

$$v_{D,n} = \frac{V_{in}\sqrt{2}}{n\pi} \sin nD\pi$$

4.66 The converter shown in Fig. P4.66 is known as a noninverting buck-boost converter. Derive the expression for V_o/V_{in}. Assume S_1 and S_2 are turned on and off simultaneously.

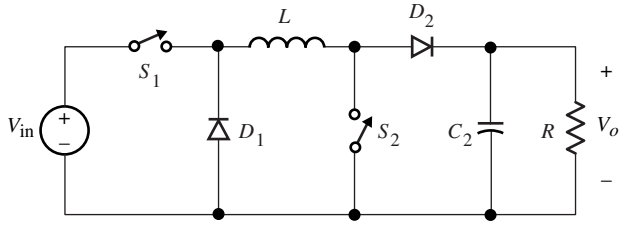


Figure P4.66

D4.67 Design a switched-mode power supply that is capable of supplying +12 V output voltage with an output power of 25 W to 375 W from a 56 V dc source. Assume the dc input comes from a variable dc source supply that changes by ±25%. The converter should not produce more than ±2% output ripple, given the peak and rms rating values for the power devices. Let $f_s = 75$ kHz .

D4.68 Design a switched-mode converter that delivers 25 W output power to a regulated output voltage of +12 V. Assume the dc source is obtained from an ac-dc SCR rectifier whose dc unregulated output vary between 8 V and 18 V. It is desired to limit the output voltage ripple to 1% and the switching frequency to 100 kHz.

4.69 Figure P4.69 shows another way to represent a buck-boost converter using a single-pole, double-through switch. Assume C_1 and C_2 are large enough that their voltages are constant. Derive the expression for V_o/V_{in} and I_o/I_{in}. Assume in steady state the switch is in position 1 for the interval DT and in position 2 for the interval $(1-D)T$.

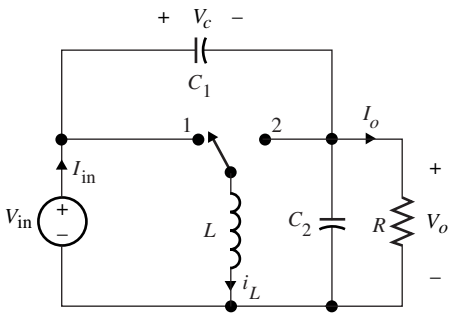


Figure P4.69

4.70 Figure P4.70 shows the circuit representation for cascading a buck-boost and a buck converter. Show that the total voltage gain is $D^2/(1-D)$.

4.71 Determine the voltage gain for the circuit shown in Fig. P4.71. What converters are put in cascade to produce this topology?

4.72 Consider a boost converter with its dc source coming from an unregulated 124 V dc input that varies by ±18% and delivers power to the load between 75 W and 225 W. It is desired to regulate the output voltage to 72 V. Assume the power switch has an on-resistance of 0.5 Ω, and the power diode has a 0.7 V voltage drop with a 0.25 Ω forward resistance. Also assume the inductor loss can be modeled by a discrete resistance of 0.1 Ω. Determine the range of the duty cycle D needed to be employed to maintain a constant output voltage. Assume ccm operation.

4.73 Figure P4.73 shows a two-quadrant boost converter topology that produces bipolar output voltage. Derive the expression for V_o/V_{in} assuming Q_1 and Q_2 are synchronized switches during turn-on for DT and turn-off for $(1-D)T$.

4.74 The circuit shown in Fig. P4.74 is known as an inverse SEPIC converter. Derive the voltage gain equation V_o/V_{in}. The switch is in position 1 during the DT interval and in position 2 during the $(1–D)T$ interval.

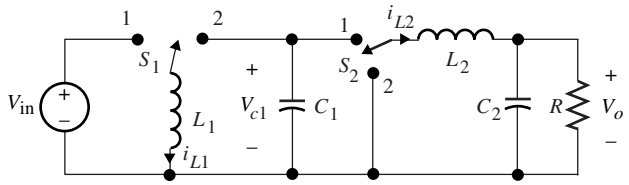


Figure P4.70

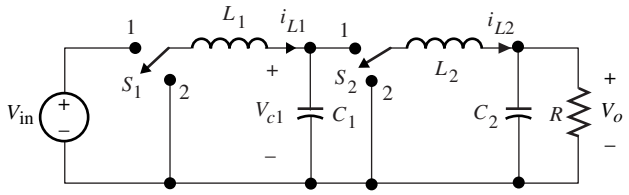


Figure P4.71

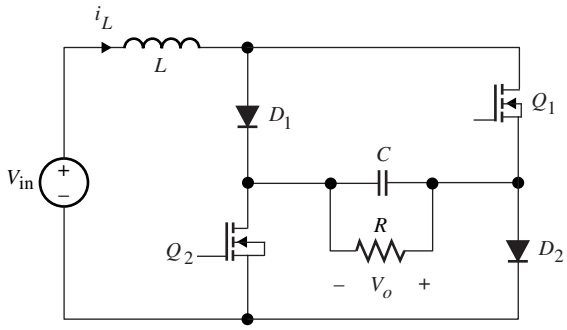
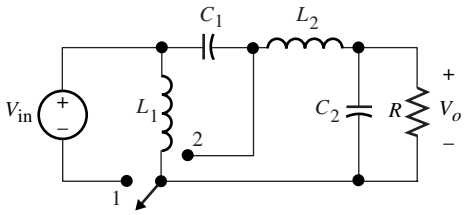


Figure P4.73



Inverse SEPIC

Figure P4.74