Chapter 2

Review of Switching Concepts and Power Semiconductor Devices

INTRODUCTION
2.1 THE NEED FOR SWITCHING IN POWER ELECTRONIC CIRCUITS
2.2 SWITCHING CHARACTERISTICS
2.2.1 The Ideal Switch
2.2.2 The Practical Switch
2.3 SWITCHING FUNCTIONS AND MATRIX REPRESENTATION
2.4 TYPES OF SWITCHES
2.5 AVAILABLE SEMICONDUCTOR SWITCHING DEVICES
2.5.1 Bipolar and Unipolar Devices
2.5.2 Thyristor-Based Devices
2.6 COMPARISON OF SWITCHING DEVICES
2.7 FUTURE TRENDS IN POWER DEVICES
2.8 SNUBBER CIRCUITS
PROBLEMS

INTRODUCTION

In this chapter, an overview of power semiconductor switching devices will be given. Only devices that are available in the market and are currently used in power electronics applications will be considered. These devices include Unipolar and bipolar devices such as the power diode, Bipolar junction transistor (BJT), Metal Oxide semiconductor field-effect transistors (MOSFET), and insulated gate bipolar transistor (IGBT); and thyristor-based devices such as the silicon-controlled rectifier (SCR), gate turn-off (GTO) thyristor, triac, static induction transistor and thyristor, and MOS-controlled thyristor (MCT). Detailed discussion of the physical structure, fabrication, and physical behavior of these devices and their packaging is beyond the scope of this text. The emphasis here will be on the terminal *i-v* switching characteristics of the available devices and their current, voltage, and switching limits. Even though most

of today's available semiconductor power devices are made of silicon or germanium, other materials, such as gallium arsenide, diamond, and silicon carbide, are currently being tested.

As stated in Chapter 1, one of the main contributions to the growth of the power electronics field has been the unprecedented advancement in semiconductor technology, especially with respect to switching speed and power-handling capabilities. The area of power electronics started with the introduction of the SCR in 1958. Since then, the field has grown in parallel with the growth of the power semiconductor device technology. In fact, the history of power electronics is very much connected to the development of switching devices, and it emerged as a separate discipline when high-power BJTs and MOSFET devices were introduced in the 1960s and 1970s. Since then, the introduction of new devices has been accompanied by dramatic improvements in power rating and switching performance.

In the 1980s, the development of power semiconductor devices took an important turn when new processing technology was developed that allowed the integration of MOS and BJT technologies on the same chip. Thus far, two devices using this new technology have been introduced: the IGBT and MCT. Many IC processing methods and types of equipment have been adopted for the development of power devices. However, unlike microelectronic ICs, which process information, power device ICs process power; hence, their packaging and processing techniques are quite different.

Since the development of thyristors in the late 1950s, power semiconductor device technology has been undergoing dynamic evolution, always following the evolution of microelectronics technology, and in the process, introducing many different kinds of devices with wide ranges of power ratings and frequency. Because of their functional importance, drive complexity, fragility, and cost, a power electronics design engineer must be equipped with a thorough understanding of the device's operation, limitations, and drawbacks, and related reliability and efficiency issues.

Power semiconductor devices represent the heart of modern power electronics, with two major desirable characteristics guiding their development:

1. Switching speed (turn-on and turn-off times)
2. Power-handling capabilities (voltage-blocking and current-carrying capabilities)

Improvements in semiconductor processing technology as well as in manufacturing and packaging techniques have allowed the development of power semiconductors for high voltage and high current ratings and fast turn-on and turn-off characteristics. The availability of different devices with different switching speeds, power-handling capabilities, sizes, costs, and other factors makes it possible to cover many power electronics applications, so that trade-offs must be made when it comes to selecting power devices.

2.1 THE NEED FOR SWITCHING IN POWER ELECTRONIC CIRCUITS

Do we have to use switches to perform electrical power conversion from the source to the load? The answer, of course, is no; there are many circuits that can perform energy conversion without switches, such as linear regulators and power amplifiers. However, the need for semiconductor devices to perform conversion functions is very much related to the converter efficiency. In power electronic

circuits, the semiconductor devices are generally operated as switches—either in the *on* state or *off* state. This is unlike the case in power amplifiers and linear regulators, where semiconductor devices operate in the linear mode. As a result, a very large amount of energy is lost within the power circuit before the processed energy reaches the output. The need to use semiconductor switching devices in power electronic circuits is based on their ability to control and manipulate very large amounts of power from the input to the output with relatively very low power dissipation in the switching device, resulting in a very high-efficiency power electronic system.

Efficiency is an important figure of merit and has significant implications on the overall performance of the system. A low-efficiency power system means that large amounts of power are being dissipated in the form of heat, with one or more of the following implications:

1. The cost of energy increases due to increased consumption.
2. Additional design complications might be imposed, especially regarding the design of device heat sinks.
3. Additional components such as heat sinks increase the cost, size, and weight of the system, resulting in low power density.
4. High power dissipation forces the switch to operate at low switching frequencies, resulting in limited bandwidth and slow response, and most important, the size and weight of magnetic components (inductors and transformers) and capacitors remain large. Therefore, it is always desirable to operate switches at very high frequencies. But we will show later that as the switching frequency increases, the average switching power dissipation increases. Hence, a tradeoff must be made between reduced size, weight, and cost of components versus reduced switching power dissipation, which means inexpensive low-switching-frequency devices.
5. Component and device reliability is reduced.

For more than 35 years, it has been shown that switching (mechanical or electrical) is the best possible way to achieve high efficiency. However, electronic switches are superior to mechanical switches because of their speed and power-handling capabilities as well as their reliability.

We should note that the advantages of using switches come at a cost. Because of the nature of switch currents and voltages (square waveforms), high-order harmonics are normally generated in the system. To reduce these harmonics, additional input and output filters are usually added to the system. Moreover, depending on the device type and power electronic circuit topology used, driver circuit control and circuit protection can significantly increase the complexity of the system and its cost.

EXAMPLE 2.1

The purpose of this example is to investigate the efficiency of four different power electronic circuits whose function is to take power from a 24 V dc source and deliver a 12 V dc output to a 6 Ω resistive load. In other words, the task of these circuits is to serve as dc *transformers* with a ratio of 2:1. The four circuits are shown in Fig. 2.1(*a*), (*b*), (*c*), and (*d*), representing a voltage divider circuit, zener regulator, transistor linear regulator, and switching circuit, respectively. The objective is to calculate the efficiency of these four power electronic circuits.

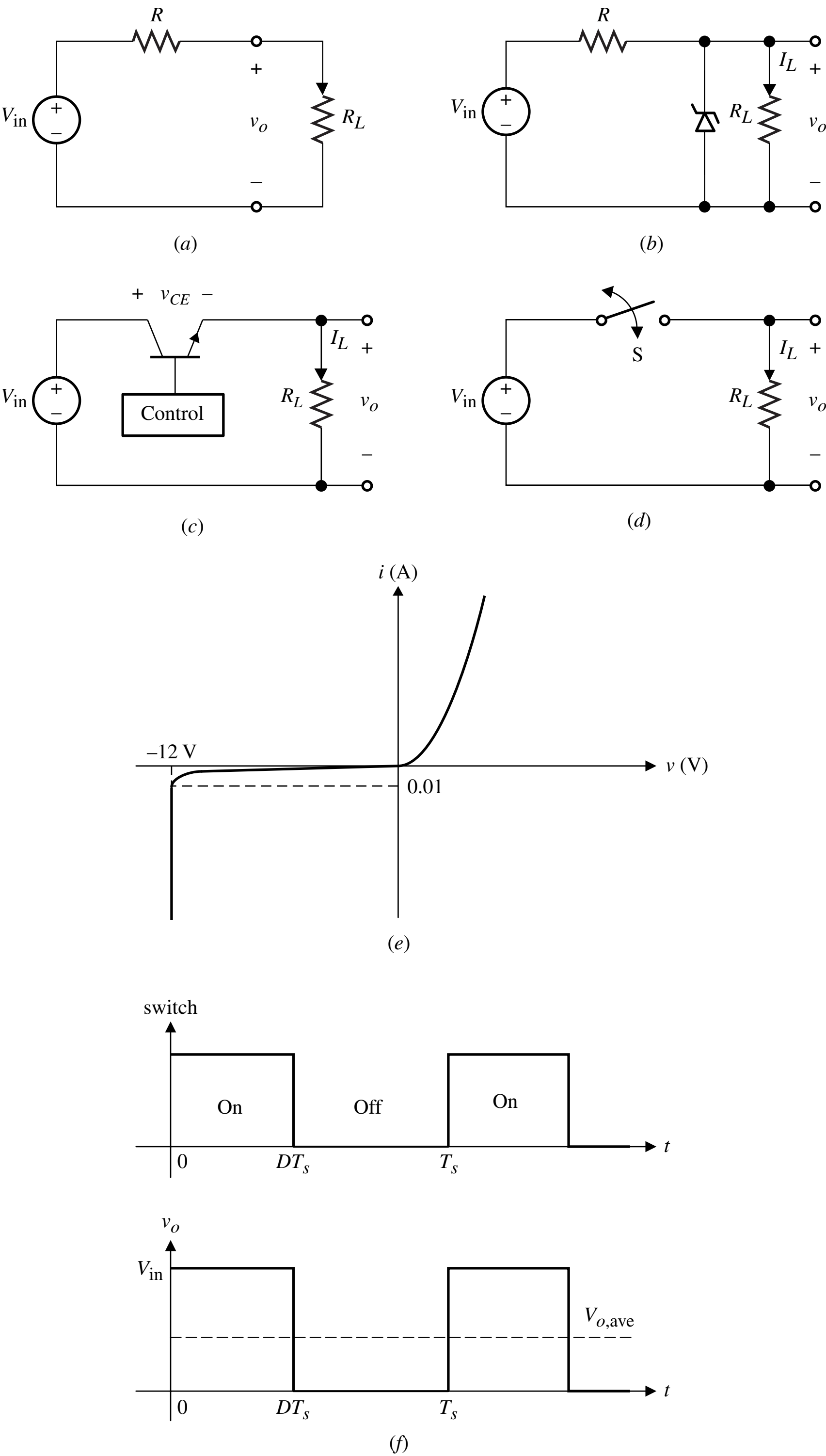


Figure 2.1 (*a*) Voltage divider. (*b*) Zener regulator. (*c*) Transistor regulator. (*d*) Switching circuit. (*e*) Zener diode *i-v* switching characteristics. (*f*) Switching waveforms for circuit (*d*).

SOLUTION

(a) ***Voltage divider dc regulator.*** The first circuit is the simplest, forming a voltage divider with $R = R_L = 6\ \Omega$ and $V_o = 12$ V. The efficiency, defined as the ratio of the average load power, P_L, to the average input power, P_{in}, is

$$\eta = \frac{P_L}{P_{in}}\% = \frac{R_L}{R_L + R}\% = 50\%$$

In fact, the efficiency is simply V_o / V_{in}%. As the output voltage becomes smaller, the efficiency decreases proportionally.

(b) ***Zener dc regulator.*** Since the desired output is 12 V, we select a zener diode with zener breakdown $V_Z = 12$ V. Assume the zener diode has the *i-v* characteristic shown in Fig. 2.1(*e*). Since $R_L = 6\ \Omega$, the load current, I_L, is 2 A. If we calculate R for $I_Z = 0.2$ A (10% of the load current), this results in $R = 5.45\ \Omega$. Since the input power is $P_{in} = 2.2\ \text{A} \times 24\ \text{V} = 52.8$ W and the output power is $P_{out} = 24$ W, the efficiency of the circuit is given by

$$\eta = \frac{24\ \text{W}}{52.8\ \text{W}}\% = 45.5\%$$

(c) ***Transistor dc regulator.*** It is clear from Fig. 2.1(*c*) that for $V_o = 12$ V, the collector emitter voltage must be around 12 V. Hence, the control circuit must provide a base current, I_B, to put the transistor in the active mode with $V_{CE} \approx 12$ V. Since the load current is 2 A, the collector current is approximately 2 A (assume small I_B). The total power dissipated in the transistor can be approximated by the following equation:

$$P_{diss} = V_{CE}I_C + V_{BE}I_B \approx V_{CE}I_C \approx 12 \times 2 = 24\ \text{W}$$

Therefore, the efficiency of the circuit is 50%.

(d) ***Switching dc regulator.*** Let us consider the switching circuit of Fig. 2.1(*d*) by assuming the switch is ideal and periodically turns on and off, as shown in Fig. 2.1(*f*). The output voltage waveform is also shown in Fig. 2.1(*f*). Even though the output voltage is not constant or pure dc, its average value is given by

$$V_{o,ave} = \frac{1}{T_s}\int_0^{T_s D} V_{in}\, dt = V_{in} D$$

where D is the duty ratio, which is the ratio of the *on*-time to the switching period, T_s. For $V_{o,ave} = 12$ V, we set $D = 0.5$, i.e., the switch has a duty cycle of 0.5 or 50%. In this case, the average output power is 48 W and the average input power is also 48 W, resulting in 100% efficiency! This is, of course, because we assumed the switch is ideal. However, let us assume that a BJT switch is used in the circuit with $V_{CE,sat} = 1$ V and I_B is small; then the average power loss in the switch is approximately 2 W, resulting in an overall efficiency of 96%. Of course, the switching circuit given in this example is oversimplified; the switch requires additional driving circuitry that is not shown, which also dissipates some power. Still, the example illustrates the high efficiency that can be achieved by a switching power electronic circuit compared to a linear power electronic circuit. Also, the difference between the linear circuit in Fig. 2.1(*b*) and (*c*) and the switched circuit of Fig. 2.1(*d*) is that the power delivered to the load in the latter case is pulsating between 0 and 96 W. If the application calls for constant power delivery with little output voltage ripple, then an *LC* filter must be added to smooth out the output voltage. This class of dc-dc converters will be studied in Chapters 4 and 5.

A final observation regards what is known as load regulation and line regulation. Line regulation is defined as the ratio between the change in the output voltage, ΔV_o, with respect to the change in the input voltage, ΔV_{in}. This is a very important design parameter in power electronics since the dc input voltage is obtained from a rectified line voltage that normally changes by ±20%. Therefore, any off-line power electronic circuit must have a limited or specified range of line regulation. If the input voltage in Fig. 2.1(*a*) and (*b*) is changed by 2 V, (i.e., $\Delta V_{in} = 2$ V) with R_L unchanged, the corresponding change in the output voltage, ΔV_o, is 1 V and 0.55 V, respectively. This is considered very poor line regulation. The circuits of Fig. 2.1(*c*) and (*d*) have much better line and load regulation since the closed-loop control compensates for the line and load variations.

2.2 SWITCHING CHARACTERISTICS

2.2.1 The Ideal Switch

It is always desirable to have power switches perform as near as possible to the ideal case. For a semiconductor device to operate as an ideal switch, it must possess the following features:

1. No limit on the amount of current (known as forward or reverse current) that the device can carry when in the conduction state (*on*-state)
2. No limit on the amount of device voltage (known as forward or reverse blocking voltage) when the device is in the nonconduction state (*off*-state)
3. Zero *on*-state voltage drop when in the conduction state
4. Infinite *off*-state resistance, i.e., zero leakage current when in the nonconduction state
5. No limit on the operating speed of the device when it changes state, i.e., zero rise and fall times

Typical switching waveforms for an ideal switch are shown in Fig. 2.2, where i_{sw} and v_{sw} are the current through and the voltage across the switch, respectively, and DT_s is the *on* time[1]. During the switching and conduction periods the power loss is zero, resulting in 100% efficiency. With no switching delays, an infinite operating frequency can be achieved. In short, an ideal switch has infinite speed, unlimited power-handling capabilities, and 100% efficiency. Semiconductor switching devices are available that can, for all practical purposes, perform as ideal switches for a number of applications.

2.2.2 The Practical Switch

The practical switch has the following switching and conduction characteristics:

1. Limited power-handling capabilities, i.e., limited conduction current when the switch is in the *on* state, and limited blocking voltage when the switch is in the *off* state
2. Limited switching speed, caused by the finite turn-on and turn-off times, which limits the maximum operating frequency of the device
3. Finite *on*-state and *off*-state resistances, i.e., the existence of forward voltage drop in the *on* state, and reverse current flow (leakage) in the *off* state
4. Because of characteristics 2 and 3, the practical switch experiences power losses in the *on* and *off* states (known as conduction loss) and during switching transitions (known as switching loss)

[1]Only the *on* time is shown since the emphasis is on the *on* and *off* times. The *off* time, $(1 - D)T_s$, has only conduction loss.

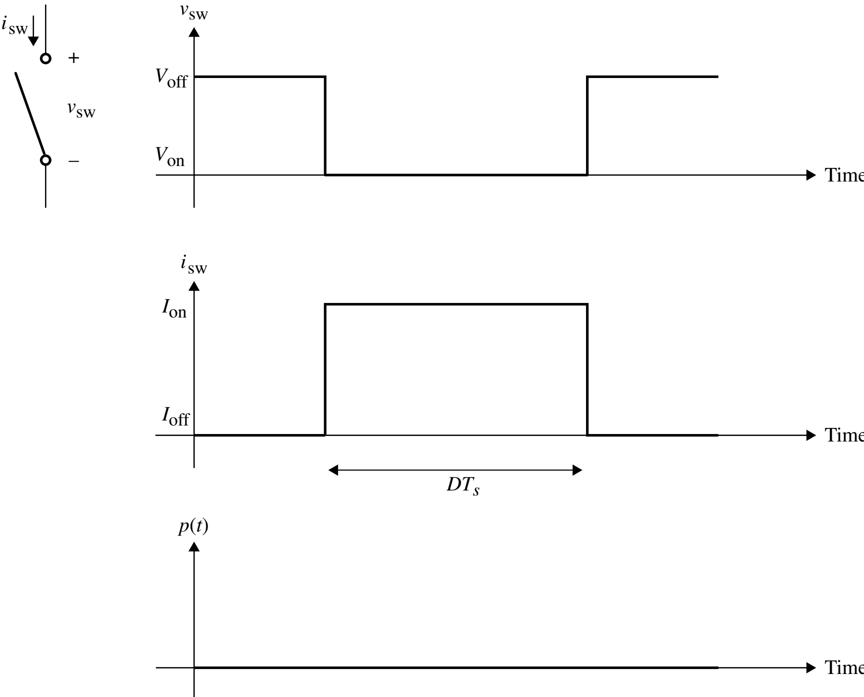


Figure 2.2 Ideal switching voltage, current, and power waveforms.

Typical switching waveforms for a practical switch are shown in Fig. 2.3(a). The average switching power and conduction power losses can be evaluated from these waveforms. The exact switching waveforms vary from one device to another, but Fig. 2.3(a) is a reasonably good representation. For simplicity, DT_s is shown to include the *off*-time and the *on*-time period of the switch. Moreover, other issues such as temperature dependence, power gain, surge capacity, and overvoltage capacity must be considered for specific devices in specific applications. A useful plot that illustrates how switching takes place from *on* to *off* and vice versa is called a *switching trajectory,* which is simply a plot of i_{sw} versus v_{sw}. Figure 2.3(b) shows several switching trajectories for the ideal and practical cases under resistive loads.

The average power dissipation, P_{ave}, over one switching cycle is given by

$$\begin{aligned} P_{ave} &= \frac{1}{T_s}\int_0^{T_s} i_{sw} v_{sw}\, dt \\ &= P_{ave,swit} + P_{ave,cond} \end{aligned}$$

where $P_{ave,swit}$ is the average switching losses and $P_{ave,cond}$ is the average conduction losses, given by

$$P_{ave,swit} = \frac{1}{T_s}\left[\underbrace{\int_0^{t_{on}} i_{sw} v_{sw}\, dt}_{on \text{ switching loss}} + \underbrace{\int_{DT_s - t_{off}}^{DT_s} i_{sw} v_{sw}\, dt}_{off \text{ switching loss}}\right]$$

$$\begin{aligned} P_{ave,cond} &= \frac{1}{T_s}\left[\int_{t_{on}}^{DT_s - t_{off}} I_{on} V_{off}\, dt + \int_{DT_s}^{T_s} I_{off} V_{on}\, dt\right] \\ &= I_{on} V_{off}\left(D - \frac{(t_{on} + t_{off})}{T_s}\right) + I_{off} V_{on} (1 - D) \end{aligned}$$

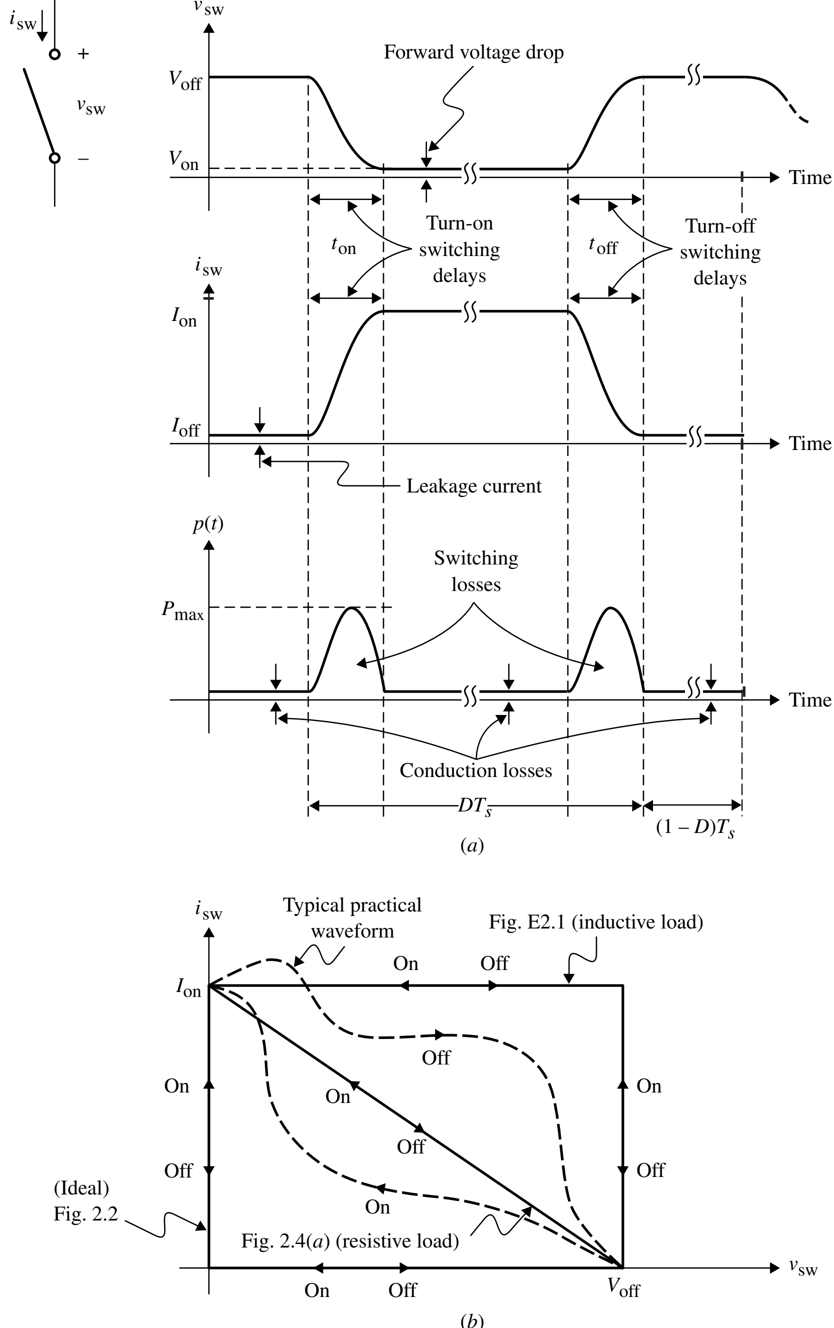


Figure 2.3 (*a*) Practical switch current, voltage, and power waveforms. (*b*) Switching trajectories under different load conditions.

If we assume the *on* and *off* times are small compared to T_s, then we have

$$P_{\text{ave,cond}} \approx \underbrace{I_{\text{on}} V_{\text{off}} D}_{\textit{on}\text{ conduction loss}} + \underbrace{I_{\text{off}} V_{\text{on}} (1 - D)}_{\textit{off}\text{ conduction loss}}$$

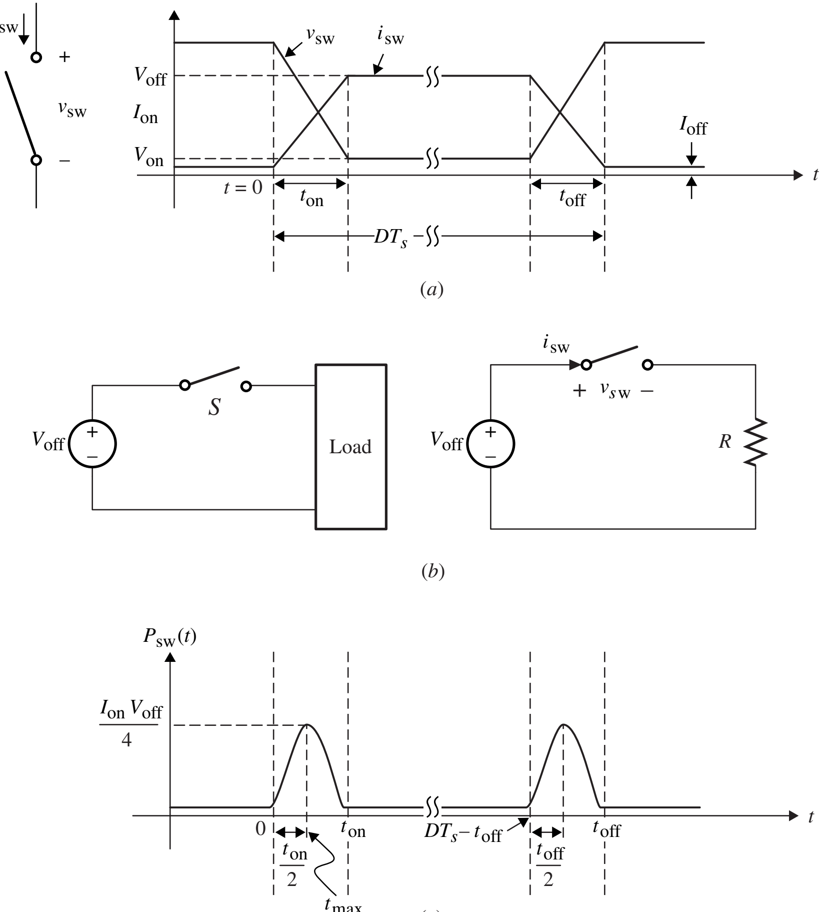


Figure 2.4 (*a*) Linear approximation of typical current and voltage switching waveforms. (*b*) Circuit implementation. (*c*) Instantaneous power waveform.

EXAMPLE 2.2

Consider a linear approximation of Fig. 2.3(*a*) as shown in Fig. 2.4(*a*) with $D = I$ (this assumes that T_s is the *on* time).

(a) Give a possible circuit implementation using a power switch whose switching waveforms are as shown in Fig. 2.4(*a*).

(b) Derive the expressions for the instantaneous switching and conduction power losses and sketch them.

(c) Determine the total average power dissipated in the circuit during one switching period.

(d) Find the maximum power.

SOLUTION

(a) First let us assume that the turn-on time, t_{on}, and turn-off time, t_{off}, the conduction voltage, V_{on}, and the leakage current, I_{off}, are part of the switching characteristics of the device and have nothing to do with the circuit topology.

When the switch is off, the blocking voltage across the switch is V_{off}, which can be represented as a dc voltage source of value V_{off} reflected somehow across the switch during the *off* state. When

the switch is on, the current through the switch equals I_{on}; hence, a dc current is needed in series with the switch when it is in the *on* state. This suggests that when the switch turns off again, the current in series with the switch must be diverted somewhere else (this process is known as *commutation* and will be discussed later). As a result, a second switch is needed to carry the main current from the switch being investigated when it's switched off. However, since i_{sw} and v_{sw} are linearly related as shown in Fig. 2.4(*a*), a resistor will do the trick, and a second switch is not needed. Figure 2.4(*b*) shows a one-switch implementation, where S is the switch and R represents the switched load.

(b) The instantaneous current and voltage waveforms during the transition and conduction times are given as follows:

$$i_{sw}(t) = \begin{cases} \dfrac{t}{t_{on}}(I_{on} - I_{off}) + I_{off} & 0 \le t \le t_{on} \\ I_{on} & t_{on} \le t \le T_s - t_{off} \\ -\dfrac{t - T_s}{t_{off}}(I_{on} - I_{off}) + I_{off} & T_s - t_{off} \le t \le T_s \end{cases}$$

$$v_{sw}(t) = \begin{cases} -\dfrac{V_{off} - V_{on}}{t_{on}}(t - t_{on}) + V_{on} & 0 \le t \le t_{on} \\ V_{on} & t_{on} \le t \le T_s - t_{off} \\ \dfrac{V_{off} - V_{on}}{t_{off}}\Big(t - (T_s - t_{off})\Big) + V_{on} & T_s - t_{off} \le t \le T_s \end{cases}$$

It can be shown that if we assume $I_{on} \gg I_{off}$ and $V_{off} \gg V_{on}$, then the instantaneous power, $p(t) = i_{sw}v_{sw}$ can be given as follows:

$$p(t) = \begin{cases} -\dfrac{V_{off}I_{on}}{t_{on}^2}(t - t_{on})t & 0 \le t \le t_{on} \\ V_{on}I_{on} & t_{on} \le t \le T_s - t_{off} \\ -\dfrac{V_{off}I_{on}}{t_{off}^2}\Big(t - (T_s - t_{off})\Big)(t - T_s) & T_s - t_{off} \le t \le T_s \end{cases}$$

Figure 2.4(*c*) shows a plot of the instantaneous power where the maximum power during turn-on and turn-off is $V_{off}I_{on}/4$.

(c) The total average dissipated power is given by

$$P_{ave} = \frac{1}{T_s}\int_0^{T_s} p(t)\, dt = \frac{1}{T_s}\left[\int_0^{t_{on}} -\frac{V_{off}I_{on}}{t_{on}^2}(t - t_{on})t\, dt + \int_{t_{on}}^{T_s - t_{off}} V_{on}I_{on}\, dt \right.$$
$$\left. + \int_{T_s - t_{off}}^{T_s} -\frac{V_{off}I_{on}}{t_{off}^2}(t - (T_s - t_{off}))(t - T_s)\, dt\right]$$

Evaluation of this integral gives

$$P_{ave} = \frac{V_{off}I_{on}}{T_s}\left(\frac{t_{on} + t_{off}}{6}\right) + \frac{V_{on}I_{on}}{T_s}(T_s - t_{off} - t_{on})$$

The first expression represents the total switching loss, and the second expression represents the total conduction loss over one switching cycle. We notice that as the frequency increases, the average power increases linearly. Also, the power dissipation increases with an increase in the forward conduction current and the reverse blocking voltage.

(d) The maximum power occurs at the time when the first derivative of $p(t)$ during switching is set to zero, i.e.,

$$\left.\frac{dp(t)}{dt}\right|_{t=t_{\max}} = 0$$

Solving this equation for $t_{\max}$, we obtain the following values at turn-on and turn-off, respectively:

$$t_{\max} = \frac{t_{\text{on}}}{2}$$

$$t_{\max} = T_s - \frac{t_{\text{off}}}{2}$$

Solving for the maximum power, we obtain

$$P_{\max} = \frac{V_{\text{off}} I_{\text{on}}}{4}$$

EXERCISE 2.1

Repeat Example 2.2 for the switching waveforms shown in Fig. E2.1.

ANSWER

(c) $$P_{\text{ave}} = \frac{V_{\text{off}} I_{\text{on}}}{2T_s}(2t_d + t_{\text{fall}} + t_{\text{rise}})$$

(d) $$P_{\max} = V_{\text{off}} I_{\text{on}}$$

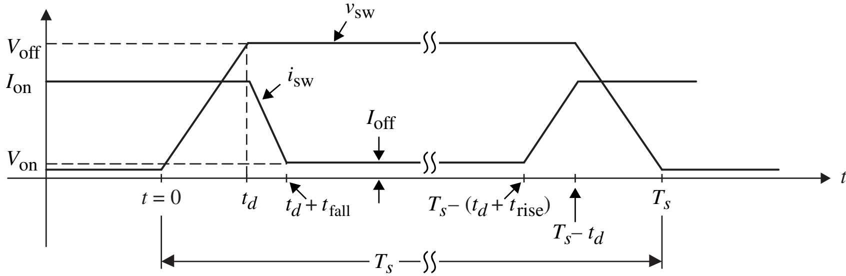


Figure E2.1 Waveforms for Exercise 2.1.

EXERCISE 2.2

Find the efficiency of the circuit in Fig. 2.1(*d*) assuming the switching characteristics for S are as shown in Fig. 2.4(*a*) with $t_{\text{on}} = 100$ ns, $t_{\text{off}} = 150$ ns, $T_s = 1\ \mu$s, $I_{\text{off}} = 0$, $V_{\text{on}} = 0$, and $D = 1.0$.

ANSWER 80%

2.3 SWITCHING FUNCTIONS AND MATRIX REPRESENTATION

Since switches perform the duties of conversion, rectification, inversion, regulation, and so on, it is possible to use the block diagram of Fig. 2.5 as a useful representation of many power electronic circuits. This system has n inputs and m outputs that can be either voltages or currents. There are $n \times m$ switches, where each of the n input lines

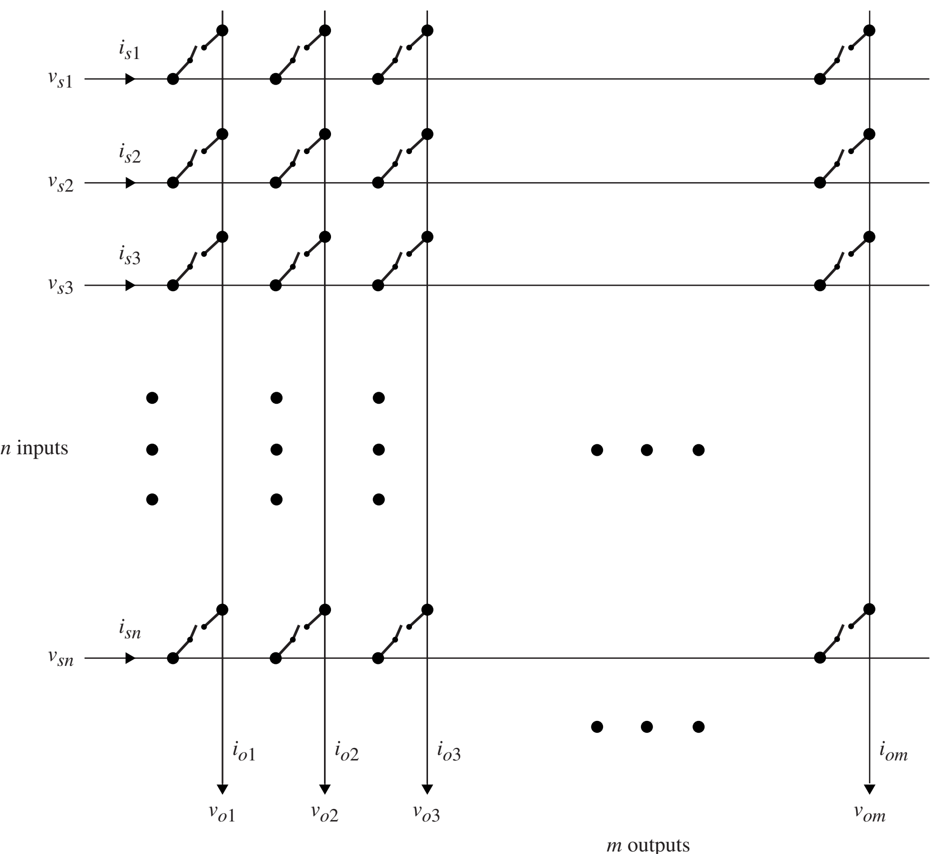
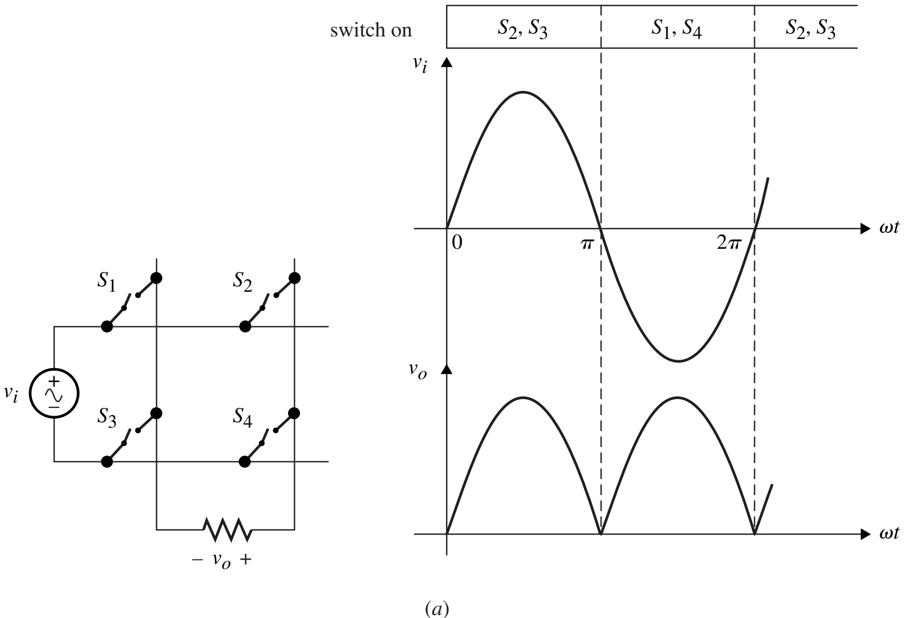


Figure 2.5 Switching matrix representation.

could be connected to any of the m outputs, resulting in what is known as a *switching matrix,* with the control of the switches described by a *switching function*. For illustration purposes, Fig. 2.6(a) and (b) shows the switching matrix representation for the single-phase full-bridge and the three-phase full-bridge, respectively. The switching function is a mathematical model for the switching matrix, describing the operation of the switches in the matrix. The literature is full of different techniques and technologies for the generation of switching functions. The switching function approach provides a compact matrix representation for the power converter and serves as a convenient tool for modeling all kinds of power conversion circuits. Due to the fact that no resistors are included in the structure, there is no power dissipation. In practical systems, additional energy storage elements are present to facilitate energy transfer; however, losses are associated with these components and the parts of the switching devices. If we assume ideal storage elements and ideal switches, then it is conceivable to achieve 100% efficiency in the switch matrix arrangement shown in Fig. 2.5. In order to process power bidirectionally, switches must be able to block voltages of either polarity and conduct current in either direction. One of the most challenging problems in designing and analyzing the system is the design and implementation of the switching network within the storage elements.

Theoretically, since we assume ideal switches and because there are no energy storage elements, the instantaneous input power must be equal to the instantaneous output power. Also, there are no restrictions on the form and frequency of the sources.

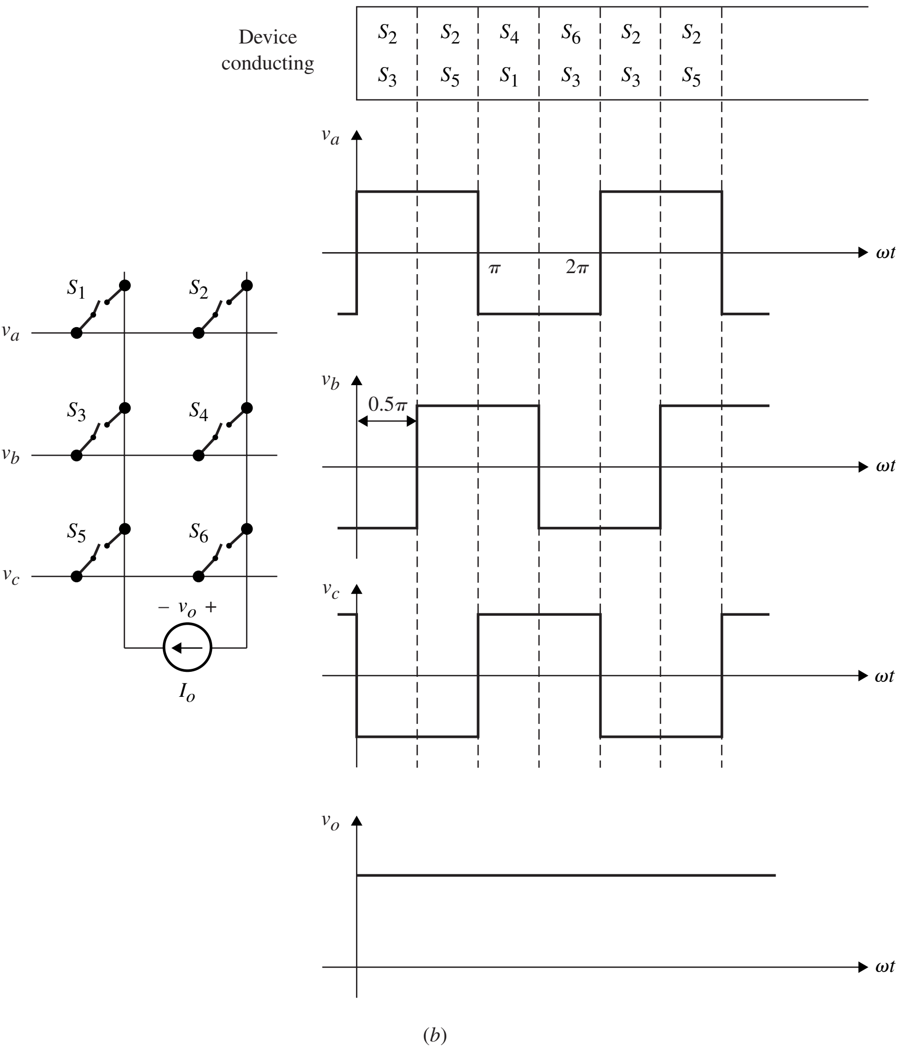


(*a*)

Figure 2.6 Examples of power electronic circuits. (*a*) Single-phase.

However, only one variable at the source terminal can be fixed (either voltage or current) and the corresponding terminal variable is determined by the switching function. For example, if $v_{s1}, v_{s2}, \ldots, v_{sn}$ represent fixed voltage sources, their corresponding currents $i_{s1}, i_{s2}, \ldots, i_{sn}$ are determined by the switching, as will be illustrated in Example 2.3. Similarly, if the output variables are represented by fixed output current sources i_{o1}, $i_{o2}, \ldots, i_{om}$, their corresponding terminal voltages are also determined by the switching functions. The reverse is also true for both the input and output terminals. Even though the switching matrix and its function determine the type of power conversion in a given power-processing circuit, the detailed implementation and terminal characteristics of the source and load sides are also a major part of the power conversion circuit. Normally the energy source is represented by an ideal voltage source that supplies a constant voltage over a wide range of currents. Similarly, the ideal current source can provide a constant current over a wide range of voltages. We will be using both types of energy sources throughout the book. As for the load side, the power conversion circuit must be designed to provide a stable and fixed output that can be represented by either a current source or a voltage source. If the output is to be a current source, the load is connected in series with an inductor; for a voltage source output, a capacitor is used.

Two important design issues need to be addressed in designing a power electronic switching circuit: (1) the "hardware," or physical implementation of the semiconductor switching matrix, and (2) the "software," or logical implementation that guarantees the operation of the switching matrix. The hardware implementation of the switching matrix is restricted by Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL). These circuit laws must be observed at all times. KVL states that the algebraic sum of the voltage drops around a closed loop must be zero. Hence, there should not be a switching sequence that will allow two unequal voltage sources to be connected in parallel, or allow a short circuit across a voltage source (see the reference by Philip Krein). For example, to avoid establishing a short circuit across v_i in Fig. 2.6(*a*), S_1 and S_3 or S_2 and S_4 are not allowed to close simultaneously. Similarly, S_1 and S_3 of Fig. 2.6(*b*) cannot be closed simultaneously in order that two unequal voltage sources, v_a and v_b, are not connected in parallel.



(*b*)

Figure 2.6 (*continued*) Examples of power electronic circuits. (*b*) Three-phase.

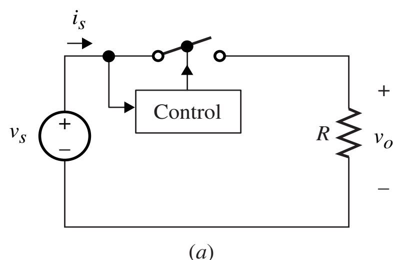
Because KCL guarantees that the algebraic sum of the currents entering a node is zero, no switching sequence should allow two unequal current sources to be connected in series. For example, to avoid establishing an open circuit in series with a current source in Fig. 2.6(*b*), KCL dictates that neither S_1, S_3, and S_5 nor S_2, S_4, and S_6 be opened simultaneously. For more discussion about switching matrices and their associated switching functions, see the reference by Peter Wood.

EXAMPLE 2.3

Consider the single-switch, single-input power-processing circuit given in Fig. 2.7. Assume the source voltage, $v_s(t)$, is a triangular waveform with a peak voltage V_p and frequency $f = 1/T$, as shown in Fig. 2.7(*b*). Assume the switch is ideal and initially off, and its control works in such a way that it toggles every time $v_s(t)$ crosses zero. Use $V_p = 12$ V, R $= 10\ \Omega$ and $T = 1$ ms.

(a) Sketch the waveforms for i_s and v_o.

(b) Calculate the average and rms values for the output voltage.



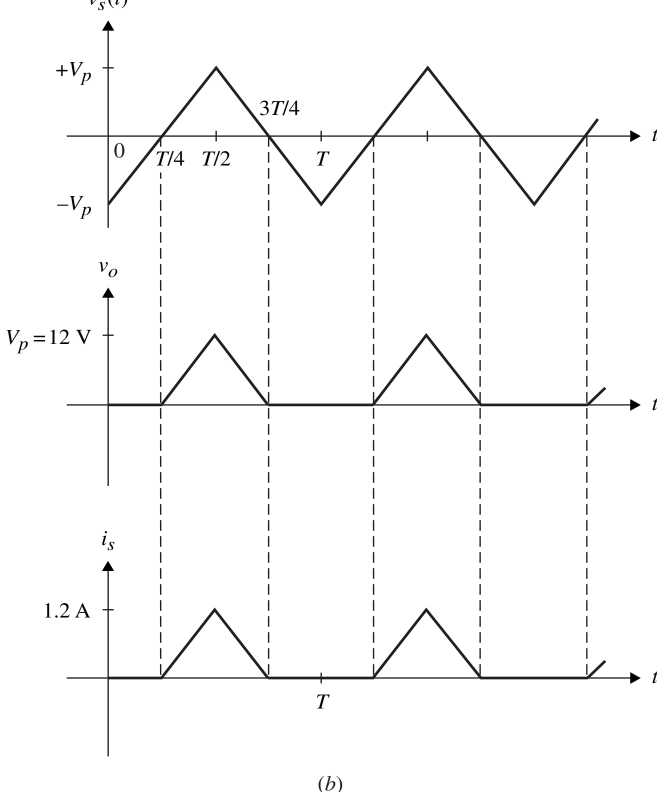


Figure 2.7 (*a*) Circuit and (*b*) waveforms for Example 2.3.

(c) Calculate the average input power, average output power, and efficiency.

(d) Repeat parts (a)–(c) by assuming T = 1 μs.

(e) Repeat parts (a)–(d) by assuming the switch has 1 V voltage drop when closed.

SOLUTION

(a) The output voltage and the source current waveform are shown in Fig. 2.7(*b*).

(b) The average output voltage is given by

$$V_o = \frac{1}{T}\int_0^T v_o(t)\,dt = \frac{1}{T}\left(\frac{1}{2}\frac{T}{2}V_p\right) = \frac{V_p}{4} = 3 \text{ V}$$

The rms is given by

$$V_{o,\text{rms}} = \sqrt{\frac{1}{T}\int_0^T v_o^2(t)\,dt} = \sqrt{\frac{1}{T}\left(\int_{T/4}^{T/2}\left(\frac{4V_p}{T}t - V_p\right)^2 dt + \int_{T/2}^{3T/4}\left(-\frac{4V_p}{T}t + 3V_p\right)^2 dt\right)}$$
$$= \frac{V_p}{\sqrt{6}} \approx 4.9\ \text{V}$$

(c) The average input power is calculated from

$$P_{\text{in}} = \frac{1}{T}\int_0^T i_s(t)v_s(t)\,dt = \frac{1}{T}\left(\frac{1}{R}\int_{T/4}^{T/2}\left(\frac{4V_p}{T}t - V_p\right)^2 dt + \int_{T/2}^{3T/4}\frac{1}{R}\left(-\frac{4V_p}{T}t + 3V_p\right)^2 dt\right)$$
$$= \frac{1}{4RV_p}\left(\frac{2V_p^3}{3}\right) = \frac{V_p^2}{6R} = 2.4\ \text{W}$$

and the average output power,

$$P_{\text{out}} = \frac{1}{T}\int_0^T i_o(t)v_o(t)\,dt = \frac{V_p^2}{6R} = 2.4\ \text{W}$$

The efficiency is

$$\eta = P_{\text{out}}/P_{\text{in}} = 100\%$$

(d) Same as above (because the results are independent of T).

(e) The average output voltage can be approximated by the following integration:

$$V_{o,\text{ave}} = \frac{1}{T}\int_0^T v_o(t)\,dt = \frac{1}{T}\left(\int_{T/4}^{T/2}\left(\frac{4V_p}{T}t - V_p - 1\right)dt + \int_{T/2}^{3T/4}\left(\frac{-4V_p}{T}t + 3V_p - 1\right)dt\right)$$
$$= \frac{1}{4}(V_p - 2) = 2.5\ \text{V}$$

The rms voltage is

$$V_{o,\text{rms}} = \sqrt{\frac{1}{T}\int_0^T v_o^2(t)\,dt} = \sqrt{\frac{1}{T}\left(\int_{T/4}^{T/2}\left(\frac{4V_p}{T}t - V_p - 1\right)^2 dt + \int_{T/2}^{3T/4}\left(\frac{-4V_p}{T}t + 3V_p - 1\right)^2 dt\right)}$$
$$= \sqrt{\frac{1}{6V_p}\left((V_p - 1)^3 + 1\right)} \approx 4.3\ \text{V}$$

It can be shown that the average input power is

$$P_{\text{in}} = \frac{1}{T}\int_0^T i_s(t)v_s(t)\,dt$$
$$= \frac{1}{T}\left[\int_{T/4}^{T/2}\left(\frac{4V_p}{T}t - V_p\right)\frac{1}{R}\left(\frac{4V_p}{T}t - V_p - 1\right)dt + \int_{T/2}^{3T/4}\left(\frac{-4V_p}{T}t + 3V_p\right)\frac{1}{R}\left(\frac{-4V_p}{T}t + 3V_p - 1\right)dt\right]$$
$$= \frac{V_p(2V_p - 3)}{12R} = 2.1\ \text{W}$$

and the average output power,

$$P_{\text{out}} = \frac{1}{T}\int_0^T i_o(t)v_o(t)\,dt$$
$$= \frac{1}{T}\left(\frac{1}{R}\int_{T/4}^{T/2}\left(\frac{4V_p}{T}t - V_p - 1\right)^2 dt + \int_{T/2}^{3T/4}\frac{1}{R}\left(\frac{-4V_p}{T}t + 3V_p - 1\right)^2 dt\right)$$
$$= \frac{1}{6RV_p}\left((V_p - 1)^3 + 1\right) \approx 1.85\ \text{W}$$

resulting in efficiency of $\eta = P_{\text{out}}/P_{\text{in}} \times 100\% = 1.85/2.1 \times 100\% \approx 88.2\%$.

EXERCISE 2.3

Repeat Example 2.3 for (*a*) $v_s = 12 \sin \omega t$ and (*b*) v_s a squarewave with peak-to-peak voltage equal to ±12 V.

ANSWER

(a) –3.82 V, 6 V, 3.6 W, 3.6, 100%; same; –3.32 V, 5.37 V, 3.22 W, 2.89 W, 89.7%

(b) –6 V, 8.5 V, 7.2 W, 100%; same; –5.5 V, 7.8 V, 6.6 W, 6.05 W, 91.7%

2.4 TYPES OF SWITCHES

To implement a given switching function, the ideal switches in the switching matrix must be realized by practical power devices. Functionally speaking, any switch must have the ability to conduct current and/or the ability to block voltage by means of control signals. In the *on* state, the current conduction state is the task under consideration, and in the *off* state, the voltage blocking state is what we are considering. Practical switches have limitations in their conduction current and in their voltage blocking. Since the switch current can flow in the forward, reverse, or both directions and the voltage can be blocked in the forward, reverse, and both directions, there are nine different combinations of current carrying and voltage blocking directions. Four of these combinations are duplicates of another four, i.e., forward current carrying and reverse voltage blocking is the same as reverse current carrying and forward voltage blocking. As a result, switches are classified into five general types of restricted switches, as shown in Table 2.1 (for more details see the reference by Philip Krein).

1. *Forward current carrying and reverse voltage blocking.* This is an uncontrolled device with unidirectional current flow. Uncontrolled device means that turn-on and turn-off are not controlled by an external control signal but rather by the power circuit itself. An example of this type of switch is the diode since it carries the cur-

Table 2.1 Types of Semiconductor Switches, Their Controllability Features, and Their Possible Switch Implementations

Type	Current flow	Voltage blocking	Switch implementation
1	Forward	Reverse	Diode
2	Forward	Forward	Transistor
3	Forward	Bidirectional	SCR
4	Bidirectional	Forward	Transistor with flyback diode
5	Bidirectional	Bidirectional	Triac

rent only in the forward direction when the anode-cathode voltage is positive. The diode is an uncontrolled device since no external control signal can be applied to initiate *carrying* the forward current or to initiate *blocking* the reverse voltage. The controlling voltage is derived from either the source or the load or both.

2. *Forward current carrying and forward voltage blocking.* This is a controlled device with unidirectional current flow. Such a switch should be able to carry the current in the forward direction and block voltage in the forward direction. Of course, the diode is unable to block a forward voltage across it. Another type of switch is needed with an external control signal that allows the device to decide whether the forward current is to flow or not even when a forward voltage is applied. This is the same as implying that the switch performs a current conduction delay function. An example of such a switch is the transistor, which is able to block voltage in the forward direction when the base (gate) current is absent.
3. *Forward current carrying and bidirectional voltage blocking*. This switch can block current flow in both directions (i.e., supports forward and reverse voltage blocking) but carries the current only in the forward direction. An example is the silicon-controlled rectifier (SCR), to be studied later in this chapter.
4. *Bidirectional current carrying and forward voltage blocking.* This switch is similar to type 2, except the current can flow bidirectionally. Hence, the implementation is a transistor with a diode connected as shown in Table 2.1 to allow reverse current flow. The diode is known as a flyback or body diode since it picks the current in the reverse direction. This switch can carry the current in the forward direction through the transistor and in the reverse direction through the flyback diode. The base (gate) signal is used to allow the switch to determine whether to carry the current in the forward direction or to be in the voltage blocking state; because of the presence of the diode, the switch is unable to block reverse voltage.
5. *Bidirectional current carrying and bidirectional voltage blocking.* This switch is the most general power electronic switch and is similar to type 3 with additional characteristics that allow it to support current flow in both directions. Unlike type 4, where a flyback diode is added to allow reverse current flow, here the forward and reverse current flow must be controlled. An example of this type is the triac (*tri*ode *ac*), which is simply two SCRs connected in parallel and in opposite directions, as shown in Table 2.1.

2.5 AVAILABLE SEMICONDUCTOR SWITCHING DEVICES

In this section, the emphasis will be on the *i-v* switching characteristics of devices and their corresponding power ratings and possible applications. Selecting the most appropriate device for a given application is not an easy task, requiring knowledge about the device's characteristics and unique features, innovation, and engineering design experience. Unlike low-power (signal) devices, power devices are more complicated in structure, driver design, and operational *i-v* characteristics. This knowledge is very important for enabling power electronics engineers to design circuits that will make these devices close to ideal. In this section, we will briefly discuss two broad families of power devices:

Bipolar and Unipolar Devices

1. Power diodes
2. Bipolar junction transistors
3. Insulated gate bipolar transistors (IGBTs)
4. Metal oxide semiconductor field-effect transistors (MOSFETs)

Thyristor-Based Devices

1. Silicon-controlled rectifiers (SCRs)
2. Gate turn-off (GTO) thyristors
3. Triode ac switches (triacs)
4. Static induction transistors (SITs) and thyristors (SITHs)
5. MOS-controlled thyristors (MCTs)

2.5.1 Bipolar and Unipolar Devices

The Power Diode

The power diode is a two-terminal device composed of a *pn* junction and whose turn-on state cannot be controlled (uncontrolled switch). The diode turn-on and turn-off is decided by the external circuitry: A positive voltage imposed across it will turn it on and a negative current through it turns it off.

The symbol and the practical and ideal *i-v* characteristic curves of the power diode are shown in Fig. 2.8(*a*), (*b*), and (*c*), respectively. In the conduction state, the forward voltage drop, V_F, is typically 1 V or less. The diode current increases exponentially with the voltage across it; i.e., a small increase in V_F produces a large increase in I_F (see Problem 2.5). In the reverse-bias region, the device is in the *off* state and only a reverse saturation current, I_s, exists in the diode (also known as leakage current). The breakdown voltage, V_{BR}, is the maximum inverse voltage the diode is capable of blocking. V_{BR} is a diode-rated parameter with values up to a few kilovolts, and in normal operation the reverse voltage should not reach V_{BR}. Zener diodes are special diodes in which the breakdown voltage is approximately 6–12 V, controlled by the doping process.

In power circuits, power diodes have two important features:

1. Power-handling capabilities, including forward current carrying and reverse voltage blocking
2. Reverse recovery time (t_{rr}) at turn-off

The parameter t_{rr} is very significant because the speed of turning off the diode could be large enough to affect the operation of the circuit. At turn-on, the delay time is normally insignificant compared to the transient time in power electronic circuits.

Broadly speaking, two types of power diodes are available:

1. The bipolar diode, which is based on the *pn* semiconductor junction. Depending on the applications, a bipolar diode can be either the standard line-frequency

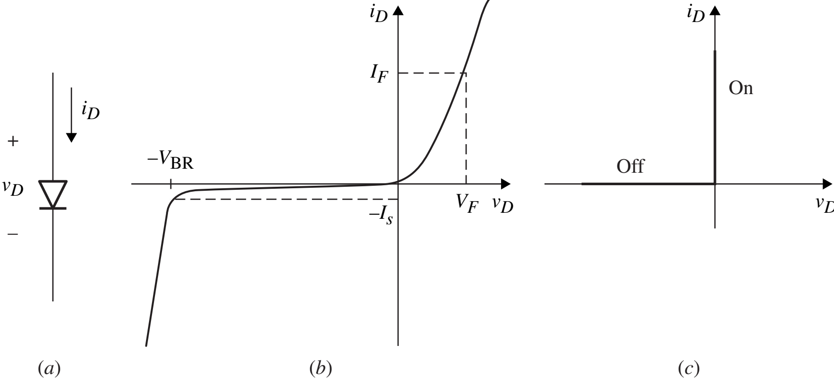


Figure 2.8 Power diode. (*a*) Circuit symbol. (*b*) Practical and (*c*) ideal switching characteristics.

type or the fast-recovery high-frequency type, with its t_{rr} varying between 50 ns and 50 μs. Typical voltage drop is 0.7–1.3 V, with reverse voltage blocking of 3 kV and forward current of 3.5 kA.

2. The Schottky diode, which is based on the metal-semiconductor junction. It has a lower forward voltage drop than the bipolar (about 0.5 V or less). Unlike the bipolar diode, whose current conduction depends on the minority and majority carriers, the Schottky diode current depends mainly on the majority carriers. Finally, the *i-v* characteristics of the Schottky diode are similar to the *i-v* characteristics of the bipolar diode. Unlike bipolar diodes, Schottky diodes generate fewer excess minority carriers than majority carriers; hence its current is primarily generated due to the drift of majority carriers. Due to its large-leakage circuit, it is normally used in low-voltage, high-current dc power supplies.

To study the reverse recovery characteristics of the diode, we consider the circuit of Fig. 2.9(*a*), which has a typical diode current waveform during turn-off as shown in Fig. 2.9(*b*). For simplicity we assume the switch is ideal. Such a circuit arrangement is normally encountered in switch-mode dc-to-dc converters with the switch replaced by either a BJT or a MOSFET. Initially we assume the diode is conducting with forward current I_0. At $t = t_0$, the switch is turned on, forcing the diode to turn off due to the dc input voltage V_{in}. The turn-on characteristics of the diode are simpler to deal with since turn-on only involves charging the diode depletion capacitor. The diode's forward conduction begins when its depletion capacitor has been charged. At turn-on, the diode voltage drop is larger than the normal forward drop during conduction. This transient voltage exists due to the large value of diode resistance at turn-on. This is why during the diode's turn-on time the power dissipation is much larger than when it is in the steady conduction state. The diode turn-off characteristics are more complex since significant stored charges exist in the body of the *pn* junction and at the junction.

As shown in Fig. 2.9(*b*), during turn-off, the diode current linearly decreases from its forward value, I_0, at $t = t_0$ to zero at $t = t_1$ and then continues to go negative until it reaches a negative peak value at $t = t_2$, known as the *reverse recovery current*, I_{RR}, at which the current starts to rise exponentially to zero at $t = t_3$. The time intervals can be broken down as follows: Between t_0 and t_1, the diode current is positive and the diode forward voltage is small. Hence, we assume the rate of change of diode current is constant and is determined by the total circuit inductance in series with the diode. In our example, since the switch is ideal, di_D/dt and I_{RR} are limited by the diode's and lead's parasitic inductances. At $t = t_1$, the current becomes zero and the diode should begin turning off by supporting reverse voltage. But because of the excess minority carriers in

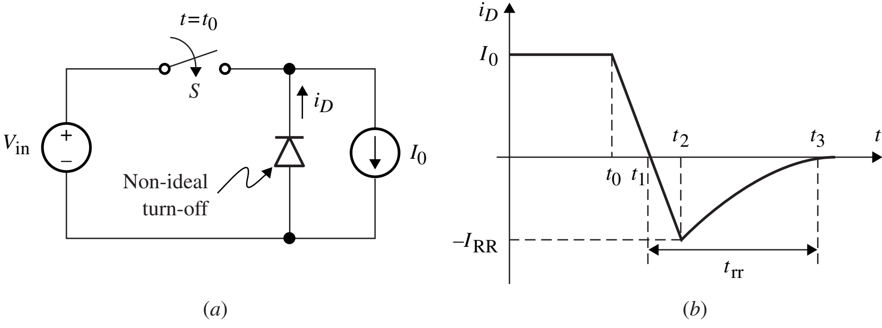


Figure 2.9 Typical diode switching characteristics. (*a*) Switching circuit with *S* closed at $t = t_0$. (*b*) Diode current.

the *pn* junction that need to be removed before the diode's reverse voltage begins to rise, the diode remains in the conduction state for longer time, i.e., until $t = t_2$.

The delay from t_1 to t_2 is due to the minority carriers in the depletion region, whereas the delay from t_2 to t_3 is caused by the charge stored in the bulk of the semiconductor material. At $t = t_3$, all charge carriers are removed, causing the device to be fully switched off. The time it takes from the moment the diode current becomes negative until it becomes zero is the reverse recovery time, t_{rr}, as shown in Fig. 2.9(*b*).

Between t_2 and t_3, the junction behaves like a capacitor whose voltage goes from zero to the reverse voltage via a charging current in this interval. The total charge carriers that cause a negative diode current flow when it is turned off constitute the *reverse recovery charge*, Q_{rr}, and can be expressed in terms of I_{RR} and t_{rr}.

The time between t_2 and t_3 may be very short compared to t_{rr}, resulting in high di/dt. The ratio between $(t_3 - t_2)$ and t_{rr} is a parameter that defines what is known as *diode snappiness*. The smaller this ratio, the quicker the diode recovers its reverse blocking voltage, resulting in what is known as a *fast-recovery* or *hard-recovery* diode. Meanwhile, a diode with a high ratio of $(t_3 - t_2)$ to t_{rr} takes a relatively long time to bring its forward current to zero from its negative peak value. These diodes are known as *soft-recovery* diodes. The fast-recovery diodes have high di/dt and normally experience oscillation at turn-off. Standard or general-purpose diodes have soft recovery time and are used in low-speed applications where the frequency is less than a few kHz.

In general, an attempt to reduce either t_{rr} or I_{RR} will result in an increase in the other. The forward recovery voltage limits the efficiency because of device stresses and higher switching losses, and t_{rr} limits the frequency of operation. Power electronics engineers should keep in mind that the transient voltage at turn-on and the transient current at turn-off might affect the external circuitry and cause unwanted stresses. External snubber circuits are added to suppress these transient values.

EXAMPLE 2.4

Consider the switching circuit shown in Fig. 2.10 by modeling the circuit parasitic inductance as a lumped discrete value, L_s. Assume the switch was open for a long time before being turned on at $t = t_0$. Assume the same diode switching characteristics of Fig. 2.9(*b*), except that it is a fast-recovery diode with $t_3 - t_2 \approx 0$. Derive the expressions for I_{RR} and the peak switch current in terms of the diode reverse recovery time.

SOLUTION While the diode is in the conduction state, its forward current is I_0. When the switch is closed at $t = t_0$, the diode voltage remains zero and its current is given by

$$i_D = I_0 - i_s$$

and i_s for $t \geq t_0$ is given by

$$i_s(t) = \frac{V_{in}}{L_s}(t - t_0) \quad t_0 \leq t \leq t_2$$

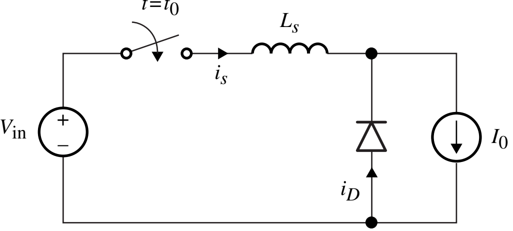


Figure 2.10 Diode switching circuit with parasitic inductor.

At $t = t_1$ the diode current becomes zero and i_s becomes I_0. Hence, the interval $t_1 - t_0$ is given by

$$t_1 - t_0 = \frac{I_0 L_s}{V_{\text{in}}}$$

Since $t_3 - t_2 \approx 0$, then $t_2 - t_1 \approx t_{\text{rr}}$ and I_{RR} is given by

$$I_{\text{RR}} = \frac{V_{\text{in}}}{L_s} t_{\text{rr}}$$

The peak switch current occurs at $t = t_2$ when $i_D = -I_{\text{RR}}$ and is given by

$$I_{s,\text{peak}} = \frac{V_{\text{in}}}{L_s} t_{\text{rr}} + I_0$$

At this point the diode is turned off and the peak inductor current is higher than the load current I_0. Since the load is highly inductive, its value cannot increase suddenly by the amount $V_{\text{in}} t_{\text{rr}} / L_s$ without creating high reverse voltage across the diode. As a result, a snubber circuit must be added across the diode to dissipate excess stored energy in the inductor.

Another important point is that when L_s becomes very small, a very large reverse recovery current occurs that could damage the diode and cause large switching losses.

The peak value of the reverse current, $-I_{\text{RR}}$, is a very important parameter and it can be less than, equal to, or larger than the forward current I_0, depending on the external circuitry connected to the diode, and the diode parasitic inductance. The fast-recovery diodes have low recovery time, normally less than 50 ns, and are used in applications such as high-frequency dc-dc converters, where the speed of recovery is critical.

The Bipolar Junction Transistors (BJT)

The schematic symbol and *i-v* characteristics for the bipolar junction transistors (BJT) are shown in Fig. 2.11(*a*), (*b*), and (*c*), respectively. It is a two-junction, three-terminal device with the minority carriers being the main conducting charges. The switching speed of the BJT is much faster than that of thyristor-type devices. A major drawback is the *second breakdown* problem.[2]

Unlike the SCR, the BJT is turned on by constantly applying a base signal. Power BJTs have two different properties from the low-power BJT and logic transistor: large blocking voltage in the *off* state and high forward current-carrying capabilities in the *on* state. BJT power ratings reach up to 1200 V and 500 A. These high rating values suggest that the power BJT's driving circuits are more complicated.

Because the BJT is a current-driven device, the larger the base current, the smaller β_{forced}[3] and the deeper the transistor is driven into saturation. In saturation, the collector-emitter voltage is almost constant and the collector current is determined largely by the external circuit to the switch. It is sometimes useful to define what is known as an *overdrive factor*, which gives a measure to how deep in saturation the transistor is. For example, if the transistor is at the edge of saturation with given base current I_B, then with an overdrive factor of 10 the base current becomes $10I_B$ and the transistor becomes deeper in saturation.

---

[2]Normally, the first breakdown voltage refers to the avalanche breakdown caused by the increase in the reverse bias voltage, which can be nondestructive. The second breakdown voltage is a destructive phenomenon caused by localized overheating spots in the device.

[3]β_{forced} is defined as the ratio I_C / I_B when the transistor is operating in the saturation mode.

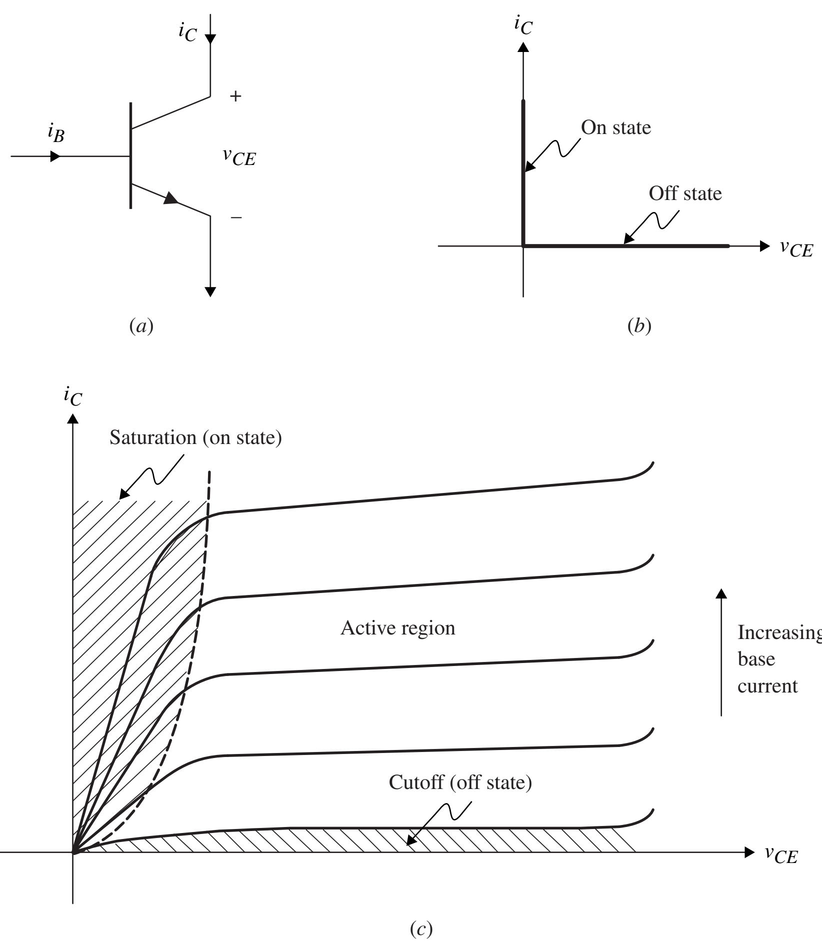


Figure 2.11 BJT switching characteristics. (*a*) *npn* transistor. (*b*) Ideal *i-v* characteristics. (*c*) Practical *i-v* characteristics.

Since the base thickness is inversely proportional to the current gain β, Darlington-connected BJT pairs have been developed in which the collectors of two devices are joined and the base of the first is connected to the emitter of the second, as shown in Fig. 2.12. This arrangement results in an overall gain that approximately equals the product of the individual β's of the two transistors. Transistor Q_1 serves as an auxiliary transistor, which provides the base current necessary to turn on Q_2. Because there is a high current gain, a smaller base current to Q_2 is needed to drive the power Darlington pair. Darlington power transistors are widely used in UPSs and various ac and dc motor drives up to hundreds of kilowatts and tens of kilohertz. A modern Darlington pair has ratings up to 1.2 kV with current up to 800 A and operating frequency up to several kilohertz.

Triple Darlingtons are also available, in which the current gain becomes proportional to the product of the three individual currents gains of the transistors. To turn off the Darlington switch, all base currents must become zero, resulting in slower switching speed compared to a single transistor. Also, the overall collector-emitter saturation voltage, $V_{CE,\text{sat}}$ is higher than for a single transistor, as will be illustrated in Exercise 2.5.

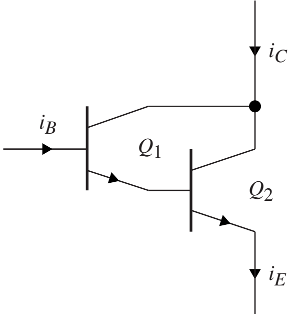


Figure 2.12 Darlington-connected BJT.

There are three regions of operation: saturation, active, and cutoff. As a power switch, the BJT must operate either in the saturation region (*on* state) or in the cutoff region (*off* state). The third state is when the transistor is in the linear region and is used as an analog amplifier.

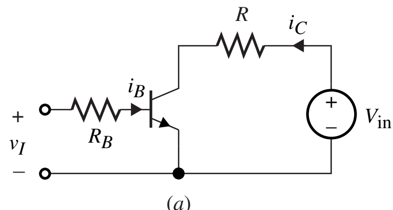
To investigate the turn-on and turn-off processes, we consider a simple inverter circuit shown in Fig. 2.13(*a*) with its switching waveforms as shown in Fig. 2.13(*b*). The voltage v_I is the base driving voltage with positive polarity, V_1, to push positive current into the base, $I_{B1} = (V_I - V_{BE})/R_B$, and a negative polarity, V_2, to quickly discharge the base current, $I_{B2} = -(V_2 + V_{BE})/R_B$. At time $t = t_0$, V_1 is applied with positive dc voltage, $+V_1$. Because it takes time to charge the internal depletion capacitor to turn the junction on at $V_{BE} = 0.7$ V, a delay time, t_d, elapses before the collector current starts flowing. After the junction is turned on, the collector starts flowing exponentially through R_B and the emitter-base junction capacitor. During this period, the minority carriers are being stored in the transistor base region. The collector current increases until it reaches its maximum saturated value, I_{on}, determined by

$$I_{\text{on}} = \frac{V_{\text{in}} - V_{CE,\text{sat}}}{R}$$

The time it takes for the collector current to rise from 10% to 90% of its maximum value, I_{on}, is called the *rise time*. For simplicity, Fig. 2.13(*b*) shows the rise time from $I_C = 0$ to I_{on}. The total switching *on* time is given by $t_{\text{on}} = t_d + t_r$. To turn off the transistor, a negative (or zero) base voltage is normally applied, resulting in a base current I_{B2} being *pulled out* of the base as shown in Fig. 2.13(*b*). The collector current does not start decreasing until sometime later after the stored saturation charge in the base has been removed. This time is called the storage time, t_s; it is normally longer than the delay time, t_d, and usually determines the limiting range of the switching speed. If the base voltage is not negative (i.e., in the absence of I_{B2}), the entire base current must be removed through the process of recombination.

To turn on the BJT, a large current must be pushed to the base. This base current must be large enough to saturate the transistor. In the saturation region, both base-emitter and base-collector junctions are forward biased. This is why the BJT is known as a current-driven device. When it is operated in the saturation region, $I_B > I_C/\beta$, where β is the dc current gain. In this region a new dc current gain β is defined to indicate the depth of the transistor saturation. The saturation collector-emitter voltage is given as $V_{CE,\text{sat}}$, and β_{forced} is defined as

$$\beta_{\text{forced}} = \frac{I_C}{I_B}$$



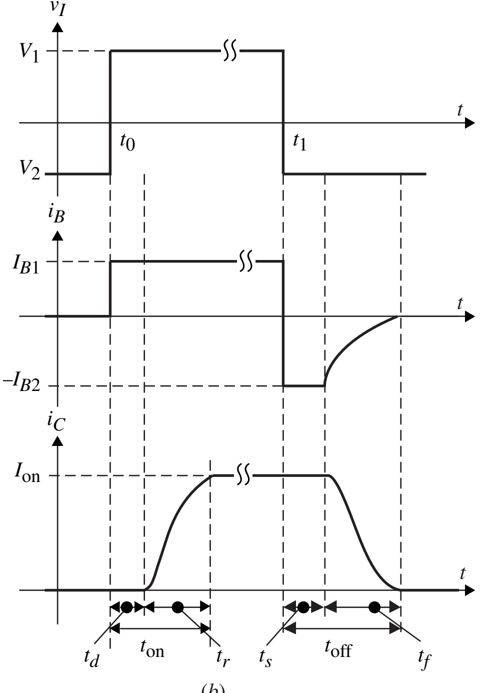


Figure 2.13 Switching characteristics for the BJT. (*a*) Circuit. (*b*) Switching waveforms.

where I_C and I_B are the collector and base currents in saturation, respectively, and $\beta_{\text{forced}} < \beta$. The smaller β_{forced}, the deeper the transistor is driven into saturation. Typically, β_{forced} can be as low as 1. Ideally, $V_{CE,\text{sat}} = 0$, but in practice this value varies between 0.1 and 0.6 V, depending on how deep in saturation the device is driven. The new ratio of collector to emitter current is much smaller than the case when the transistor is operated in the active mode. At the edge of saturation, $\beta_{\text{forced}} = \beta$.

The total power dissipation in the transistor is obtained by adding the input power supplied by the collector current and the input power supplied by the base current; hence, the total power dissipation is defined as follows:

$$P_{\text{diss}} = V_{CE}I_C + V_{BE}I_B$$

EXERCISE 2.4

Consider the transistor circuit shown in Fig. E2.4. Assume the transistor is operating in the saturation region with $V_{CE,\text{sat}} = 0.5$ V, $V_{BE} = 0.75$ V, $V_D = 0.7$ V, and $D = 0.5$. Sketch i_B, v_{CE}, and i_D. Determine the overall efficiency of the circuit (neglect the power supplied through the base).

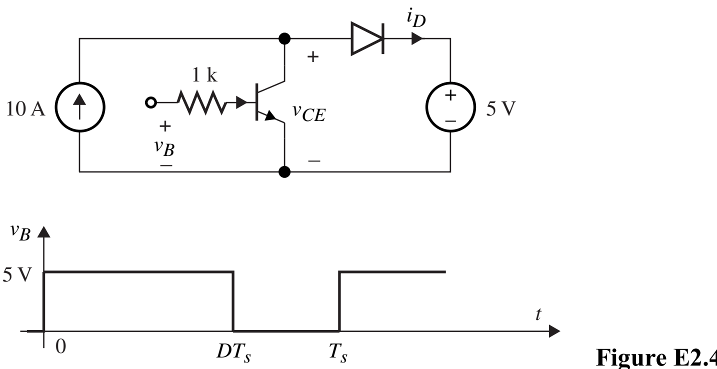


Figure E2.4

ANSWER $\eta = 80.6\%$

To determine the voltage, current, and power operational limits, normally a plot of *i-v* characteristics is given, as shown in Fig. 2.14. It gives the region in which the transistor can operate within its limits, the region is known as the safe operation area (SOA). It represents the permissible range of current, voltage, and power of the device in operation. The locus of switch voltage versus switch current during turn-on and turn-off must lie within the SOA.

EXERCISE 2.5

(a) Show that the current gain of the triple Darlington transistors shown in Fig. E2.5 is given by

$$\frac{i_C}{i_B} \approx \beta_1 \beta_2 \beta_3$$

(b) Assume transistor Q_1 has collector-emitter saturation voltage $V_{CE1,\text{sat}}$. Show that $V_{CE3,\text{sat}}$ for transistor Q_3 is given by

$$V_{CE3,\text{sat}} = V_{CE1,\text{sat}} + 2V_{BE}$$

Assume identical V_{BE} for the three transistors.

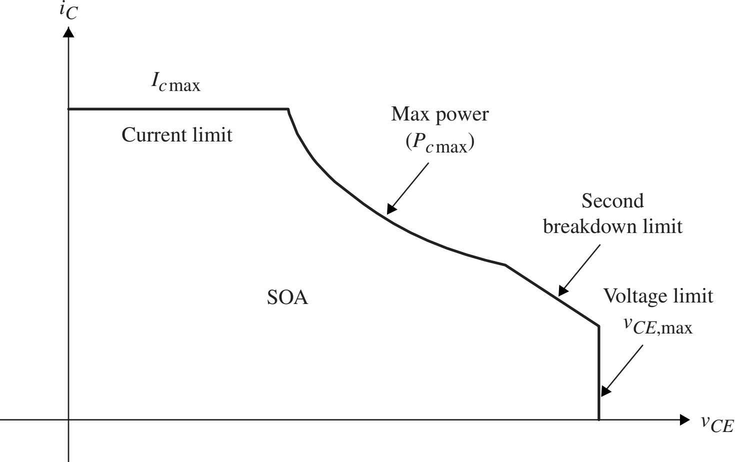


Figure 2.14 Safe Operation Area (SOA) for a BJT.

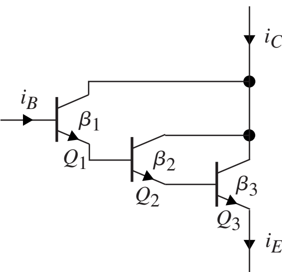


Figure E2.5

EXERCISE 2.6

Consider the simple BJT switch shown in Fig. E2.6. Determine β_{forced} for $R_B = 1\ \text{k}\Omega$, $R_B = 10\ \text{k}\Omega$, $R_B = 20\ \text{k}\Omega$. Use $V_{BE} = 0.7$ V, $V_{CE,\text{sat}} = 0.3$ V and assume an ideal diode.

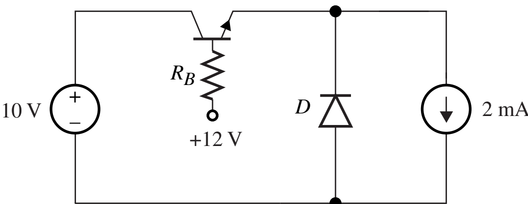


Figure E2.6

ANSWER 1.25, 12.5, 25

Initially, the BJT was developed to be used in linear audio output amplifiers. Soon BJT devices were used in switch-mode and high-frequency converters for aerospace applications to reduce the size and weight of magnetic components and filter capacitors. In applications where self-turn-off devices are needed, such as dc choppers and inverters, BJTs quickly replaced thyristors.

The Power MOSFET

In this section, an overview of power MOSFET semiconductor switching devices will be given. A detailed discussion of the physical structure, fabrication, and physical behavior of the device and its packaging is beyond the scope of this chapter. The emphasis here will be on the device's regions of operation and its terminal *i-v* switching characteristics.

Unlike the bipolar junction transistor, the metal oxide semiconductor field-effect transistor (MOSFET) device belongs to the *unipolar device* family, since it uses only the majority carriers in conduction. The development of metal oxide semiconductor technology for microelectronic circuits opened the way for the power MOSFET device in 1975. Selecting the most appropriate device for a given application is not an easy task, requiring knowledge about the device characteristics, and unique features, as well as innovation and engineering design experience. Unlike low-power (signal) devices, power devices are more complicated in structure, driver design, and operational *i-v* characteristics. This knowledge is very important in enabling a power electronics engineer to design circuits that will make these devices close to ideal.

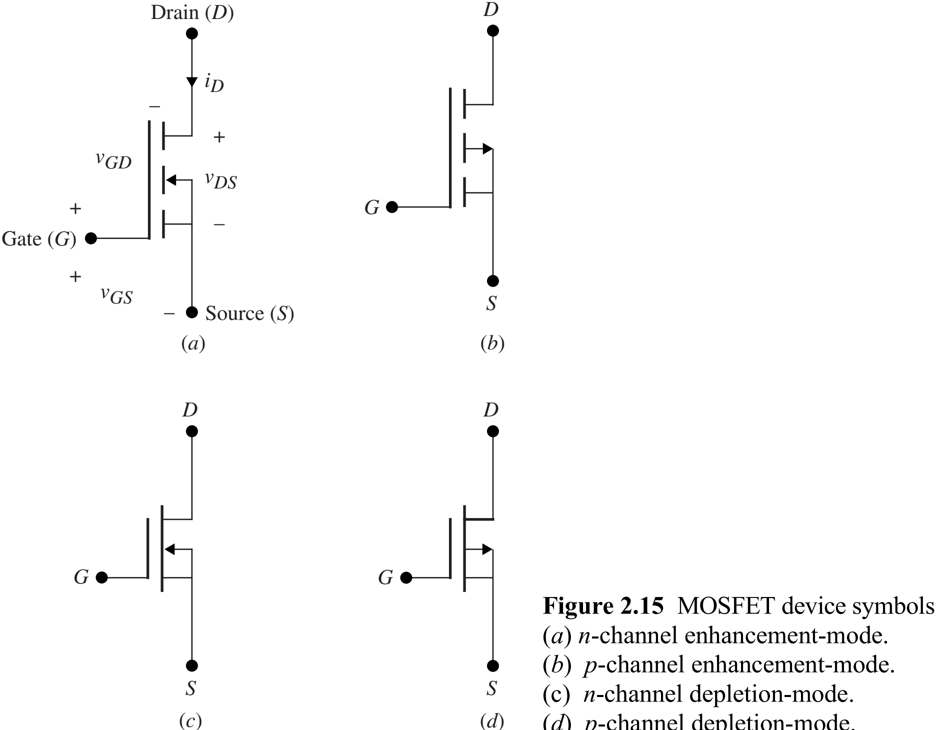


Figure 2.15 MOSFET device symbols.
(*a*) *n*-channel enhancement-mode.
(*b*) *p*-channel enhancement-mode.
(c) *n*-channel depletion-mode.
(*d*) *p*-channel depletion-mode.

The device symbols for *p*- and *n*-channel enhancement and depletion types are shown in Fig. 2.15. Figure 2.16 shows the *i*-*v* characteristics for the *n*-channel enhancement-type MOSFET. It is the fastest power switching device, with a switching frequency of more than 1 MHz, a voltage power rating up to 600 V, and a current rating as high as 40 A. MOSFET regions of operations will be studied shortly.

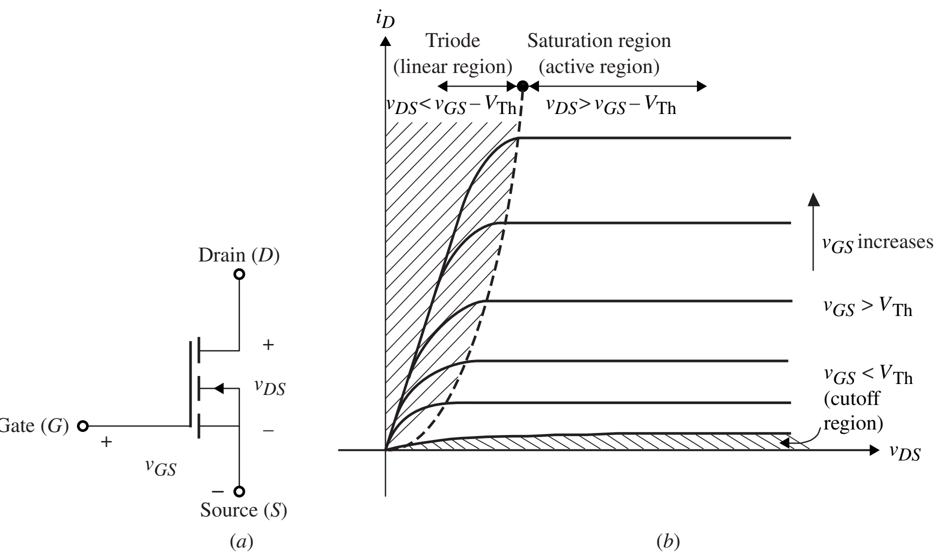


Figure 2.16 (*a*) *n*-channel enhancement-mode MOSFET and (*b*) its i_D vs. v_{DS} characteristics.

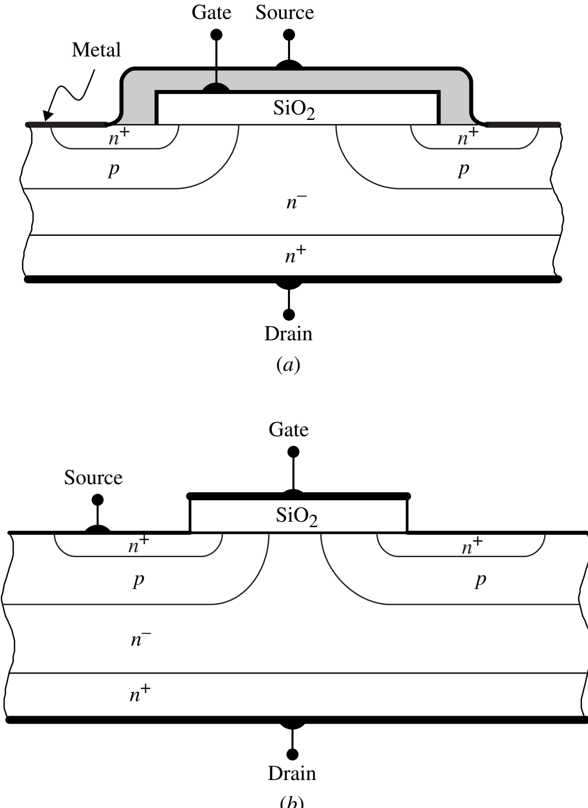


Figure 2.17 (*a*) Vertical cross-sectional view of a power MOSFET. (*b*) Simplified representation.

MOSFET Structure Unlike the lateral-channel MOSET devices used in many IC technologies, in which the gate, source, and drain terminals are located on the same surface of the silicon wafer, power MOSFETs use a vertical channel structure to increase the device's power rating. In the vertical channel structure, the source and drain are on opposite sides of the silicon wafer. Figure 2.17(*a*) shows a vertical cross-sectional view of a power MOSFET. Figure 2.17(*b*) shows a simplified representation. There are several discrete types of the vertical-structure power MOSFET available commercially today, such as the V-MOSFET, U-MOSFET, D-MOSFET, and S-MOSFET. The *pn* junction between the *p*-base region (also referred to as the body or bulk region) and the *n*-drift region provides the forward voltage blocking capabilities. The source metal contact is connected directly to the *p*-base region through a break in the n^+ source region to allow for a fixed potential to the *p*-base region during normal device operation. When the gate and source terminals are set at the same potential ($V_{GS} = 0$), no channel is established in the *p*-base region (i.e., the channel region remains unmodulated). The lower doping in the *n*-drift region is needed to achieve higher drain voltage blocking capabilities. For the drain-source current, i_D, to flow, a conductive path must be established between the n^+ and n^- regions through the *p*-base diffusion region.

On-State Resistance When the MOSFET is in the *on* state (triode region), the channel of the device behaves like a constant resistance, $R_{DS(\text{on})}$, that is linearly proportional to the change between v_{DS} and i_D, as given by the following relation:

$$R_{DS(\text{on})} = \left.\frac{\partial v_{DS}}{\partial i_D}\right|_{V_{GS=\text{constant}}}$$

The total conduction (*on*-state) power loss for a given MOSFET with forward current I_D and *on*-resistance $R_{DS(\text{on})}$ is given by

$$P_{\text{on,diss}} = I_D^2 R_{DS(\text{on})}$$

The value of $R_{DS(\text{on})}$ can be significant and varies between tens of milliohms and a few ohms for low-voltage and high-voltage MOSFET, respectively. The *on*-state resistance is an important data sheet parameter, since it determines the forward voltage drop across the device and its total power losses.

Unlike the current-controlled bipolar device, which requires base current to allow the current to flow in the collector, the power MOSFET is a voltage-controlled unipolar device and requires only a small amount of input (gate) current. As a result, it requires less drive power than the BJT. However, it is a nonlatching current like that of the BJT; i.e., a gate-source voltage must be maintained. Moreover, since only majority carriers contribute to the current flow, MOSFETs surpass all other devices in switching speed, with speeds exceeding a few megahertz. Comparing the BJT and the MOSFET, the BJT has higher power-handling capabilities and lower switching speed, while the MOSFET device has lower power-handling capabilities and relatively fast switching speed. The MOSFET device has a higher *on*-state resistance than the bipolar transistor. Another difference is that the BJT parameters are more sensitive to junction temperature compared to the MOSFET parameters. Unlike the BJT, MOSFET devices don't suffer from second breakdown voltages, and sharing current in parallel devices is possible.

Internal Body Diode The modern power MOSFET has an internal diode called a *body diode* connected between the source and the drain, as shown in Fig. 2.18(*a*). This diode provides a reverse direction for the drain current, allowing a bidirectional switch implementation. Even though the MOSFET's body diode has adequate current and switching speed ratings, in some power electronic applications that require the use of ultra-fast diodes, an external fast-recovery diode is added in an anti-parallel fashion, with the body diode blocked by a slow-recovery diode, as shown in Fig. 2.18(*b*).

Internal Capacitors Another important parameter that affects the MOSFET's switching behavior is the parasitic capacitances between the device's three terminals, namely, the gate-to-source (C_{gs}), gate-to-drain (C_{gd}), and drain-to-source (C_{ds}) capacitances, shown in Fig. 2.19(*a*). The values of these capacitances are nonlinear and a function of the device's structure, geometry, and bias voltages. During turn-on, capacitors C_{gd} and C_{gs} must be charged through the gate; hence, the design of the gate control circuit must take into consideration the variation in these capacitances. The largest variation occurs in the gate-to-drain capacitance as the drain-to-gate voltage varies. The MOSFET parasitic capacitances are given in terms of the device's data sheet parameters C_{iss}, C_{oss}, and C_{rss} as follows,

$$C_{gd} = C_{\text{rss}}$$

$$C_{gs} = C_{\text{iss}} - C_{\text{rss}}$$

$$C_{ds} = C_{\text{oss}} - C_{\text{rss}}$$

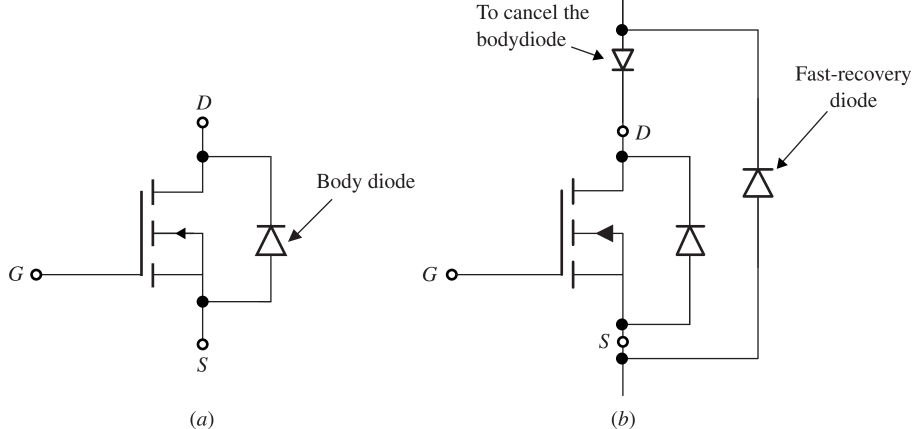


Figure 2.18 (*a*) MOSFET internal body diode. (*b*) Implementation of a fast body diode.

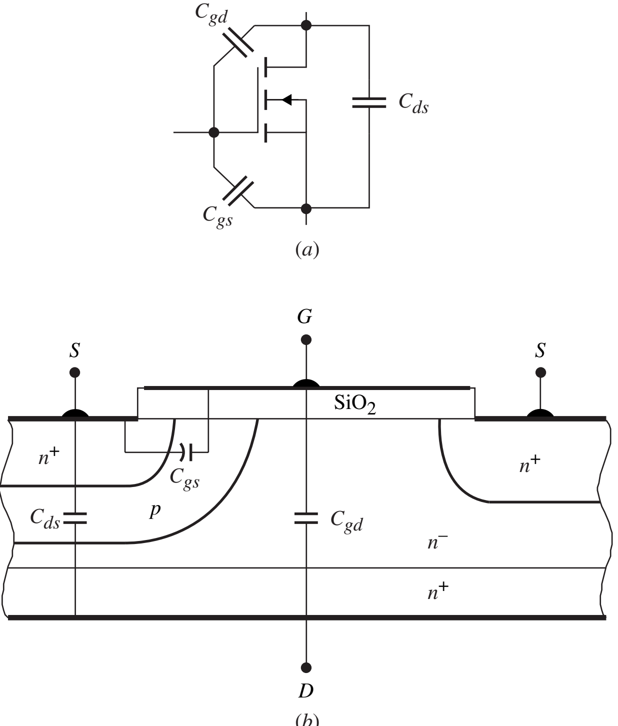


Figure 2.19 (*a*) Equivalent MOSFET representation including junction capacitances. (*b*) Representation of this physical location.

where

C_{rss} = small-signal reverse transfer capacitance
C_{iss} = small-signal input capacitance with the drain and source terminals shorted
C_{oss} = small-signal output capacitance with the gate and source terminals shorted.

The MOSFET capacitances C_{gs}, C_{gd}, and C_{ds} are nonlinear and are a function of the dc bias voltage. The variations in C_{oss} and C_{iss} are significant as the drain-to-source and gate-to-source voltages cross zero, respectively. The objective of the drive circuit is to

charge and discharge the gate-to-source and gate-to-drain parasitic capacitances to turn the device on and off, respectively.

In power electronics, the aim is to use power switching devices to operate at higher and higher frequencies. Hence, the size and weight associated with the output transformer, inductors, and filter capacitors will decrease. As a result, MOSFETs are used extensively in power supply designs that require high switching frequencies, including switching and resonant-mode power supplies and brushless dc motor drives. Because of the device's large conduction losses, its power rating is limited to a few kilowatts. Because of its many advantages over BJT devices, modern MOSFET devices have received high market acceptance.

Regions of Operation Most MOSFET devices used in power electronics applications are of the *n*-channel, enhancement type, like that shown in Fig. 2.16(*a*). For the MOSFET to carry drain current, a channel between the drain and the source must be created. This occurs when the gate-to-source voltage exceeds the device threshold voltage, V_{Th}. For $v_{GS} > V_{\mathrm{Th}}$, the device can be either in the triode region, which is also called "constant resistance" region, or in the saturation region, depending on the value of v_{DS}. For a given v_{GS}, with a small v_{DS} ($v_{DS} < v_{GS} - V_{\mathrm{Th}}$) the device operates in the triode region (saturation region in the BJT), and with a large v_{DS} ($v_{DS} > v_{GS} - V_{\mathrm{Th}}$), the device enters the saturation region (active region in the BJT). For $v_{GS} < V_{\mathrm{Th}}$, the device turns off, with the drain current almost equal to zero. Under both regions of operation, the gate current is almost zero. This is why the MOSFET is known as a voltage-driven device and, therefore, requires a simple gate control circuit.

The characteristic curves in Fig. 2.16(*b*) show that there are three distinct regions of operation, labeled as triode region, saturation region, and cutoff region. When used as a switching device, only the triode and cutoff regions are used; when it is used as an amplifier, the MOSFET must operate in the saturation region, which corresponds to the active region in the BJT.

The device operates in the cutoff region (*off* state) when $v_{GS} < v_{\mathrm{Th}}$, resulting in no induced channel. In order to operate the MOSFET in either the triode or saturation region, a channel must first be induced. This can be accomplished by applying a gate-to-source voltage that exceeds v_{Th}, i.e.,

$$v_{GS} > V_{\mathrm{Th}}$$

Once the channel is induced, the MOSFET can operate either in the triode region (when the channel is continuous with no pinch-off, resulting in the drain current being proportional to the channel resistance) or in the saturation region (the channel pinches off, resulting in constant I_D). The gate-to-drain bias voltage (v_{GD}) determines whether the induced channel undergoes pinch-off or not. This is subject to the following restrictions.

For the triode mode of operation, we have

$$v_{GD} > V_{\mathrm{Th}}$$

and for the saturation region of operation, we have

$$v_{GD} < V_{\mathrm{Th}}$$

Pinch-off occurs when $v_{GD} = V_{\mathrm{Th}}$.

In terms of v_{DS}, the preceding inequalities may be expressed as follows:

1. For the triode region of operation,

$$v_{DS} < v_{GS} - V_{\mathrm{Th}} \qquad v_{GS} > V_{\mathrm{Th}}$$

2. For the saturation region of operation,

$$v_{DS} > v_{GS} - V_{\text{Th}} \qquad v_{GS} > V_{\text{Th}}$$

3. For the cutoff region of operation

$$v_{GS} < V_{\text{Th}}$$

It can be shown that the drain current, i_D, can be mathematically approximated as follows:

$$i_D = k[2(v_{GS} - V_{\text{Th}})v_{DS} - v_{DS}^2] \qquad \text{(triode region)}$$

$$i_D = k(v_{GS} - V_{\text{Th}})^2 \qquad \text{(saturation region)}$$

$$k = \frac{1}{2}\mu_n C_{\text{ox}}\left(\frac{W}{L}\right)$$

where

μ_n = electron mobility
C_{ox} = oxide capacitance per unit area
L = length of the channel
W = width of the channel

Typical values for these parameters are given in the PSPICE model discussed later. At the boundary between the saturation (active) and triode regions, we have

$$v_{DS} = v_{GS} - V_{\text{Th}}$$

resulting in the following equation for i_D:

$$i_D = kv_{DS}^2$$

The input transfer characteristic curve for i_D vs. v_{GS} when the device is operating in the saturation region is shown in Fig. 2.20.

The large-signal equivalent circuit model for an n-channel enhancement-type MOSFET operating in the saturation mode is shown in Fig. 2.21. The drain current is represented by a current source as a function of V_{Th} and v_{GS}.

If we assume the channel is pinched off, the drain-source current will no longer be constant but rather will depend on the value of v_{DS} as shown in Fig. 2.22. The increased

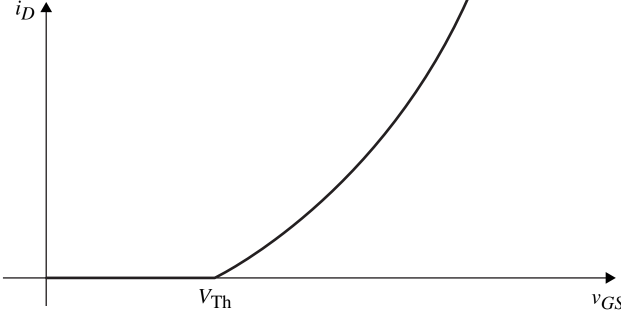


Figure 2.20 Input transfer characteristics for a MOSFET device operating in the saturation region.

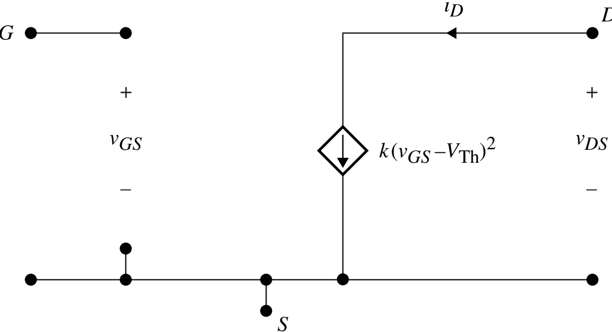


Figure 2.21 Large-signal equivalent circuit model.

value of v_{DS} results in reduced channel length, resulting in a phenomenon known as channel length modulation. If the v_{DS}-i_D lines are extended as shown in Fig. 2.22, they all intercept the v_{DS} axis at a single point labeled $-1/\lambda$, where λ is a positive constant MOSFET parameter. The term $(1 + \lambda v_{DS})$ is added to the i_D equation to account for the increase in i_D due to the channel length modulation. i_D is thus given by

$$i_D = k(v_{GS} - V_{Th})^2(1 + \lambda v_{DS}) \quad \text{(saturation region)}$$

From the definition of r_o given, it is easy to show that the MOSFET output resistance can be expressed as follows:

$$r_o = \frac{1}{\lambda k(v_{GS} - V_{Th})}$$

If we assume the MOSFET is operating under small-signal conditions, i.e., the variation in v_{GS} on the i_D vs. v_{GS} characteristic curve is in the neighborhood of the dc operating point Q at I_D and V_{GS}, as shown in Fig. 2.23, the i_D current source can be represented as the product of the slope g_m and v_{GS}, as shown in Fig. 2.24.

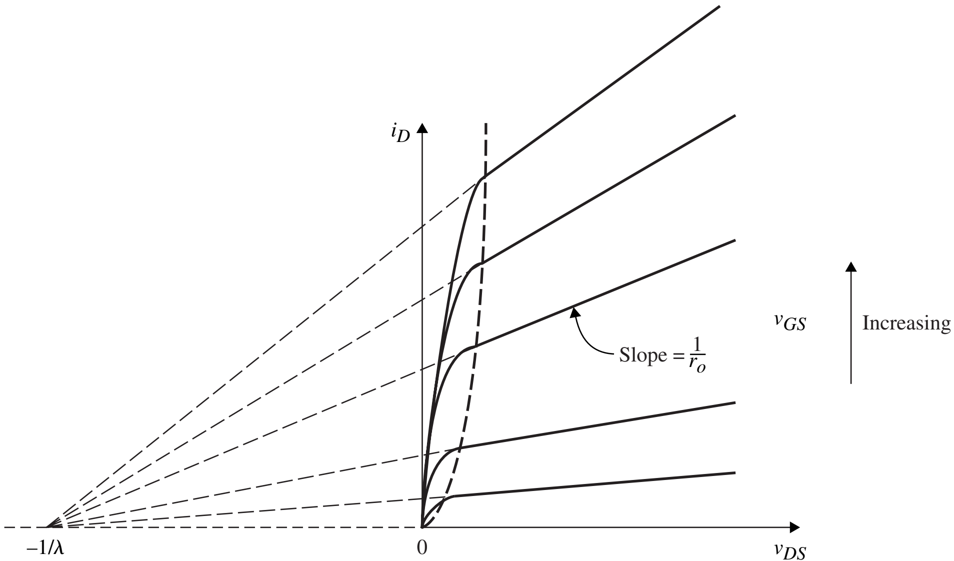


Figure 2.22 MOSFET characteristic curve including output resistance.

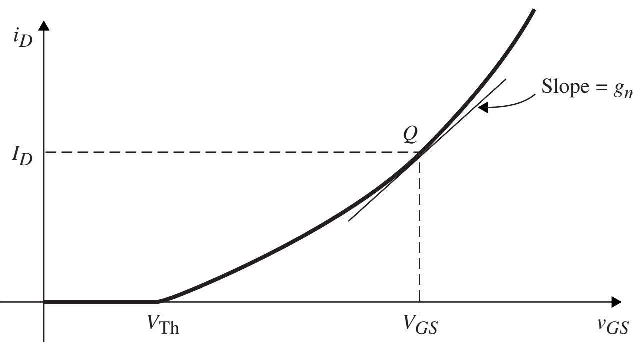


Figure 2.23 Linearized i_D vs. v_{GS} curve with operating dc point (Q).

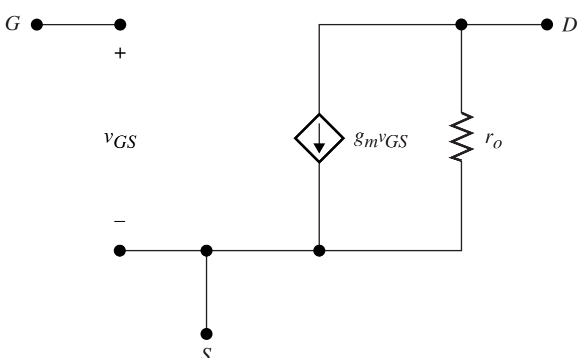


Figure 2.24 Small-signal equivalent circuit including MOSFET output resistance.

Input Capacitance Because the MOSFET is a majority-carrier transport device, it is inherently capable of high-frequency operation. Still, the MOSFET has two limitations:

1. High input gate capacitances
2. Transient/delay due to carrier transport through the drift region

As stated earlier, the input capacitance consists of two components: the gate-to-source and gate-to-drain capacitances. The input capacitances can be expressed in terms of the device junction capacitances by applying the Miller theorem to Fig. 2.25(a). Using the Miller theorem, the total input capacitance, C_{in}, between the gate and source is given by

$$C_{\text{in}} = C_{gs} + (1 + g_m r_o) C_{gd}$$

The frequency response of the MOSFET circuit is limited by the charging and discharging times of C_{in}. Miller effect is inherent in any feedback transistor circuit with resistive load that exhibits a feedback capacitance from the input to the output. The objective is to reduce the feedback gate-to-drain resistance. The output capacitance between the drain and source, C_{ds}, does not affect the turn-on and turn-off MOSFET switching characteristics. Figure 2.26 shows how C_{gd} and C_{gs} vary under increased drain-source voltage, v_{DS}.

In power electronics applications, power MOSFETs are operated at high frequencies in order to reduce the size of the magnetic components. To reduce the switching

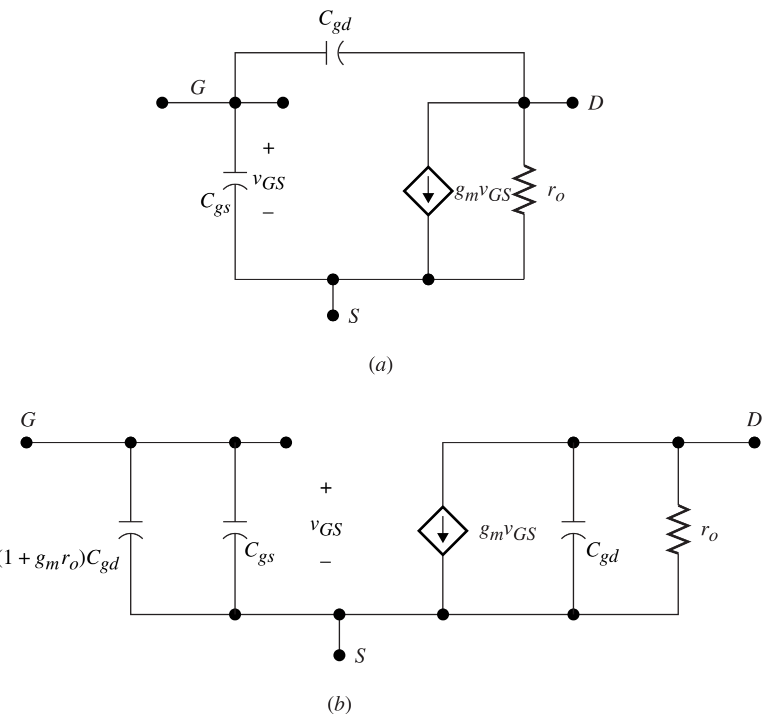


Figure 2.25 (*a*) Small-signal equivalent circuit including parasitic capacitances. (*b*) Applying the Miller theorem.

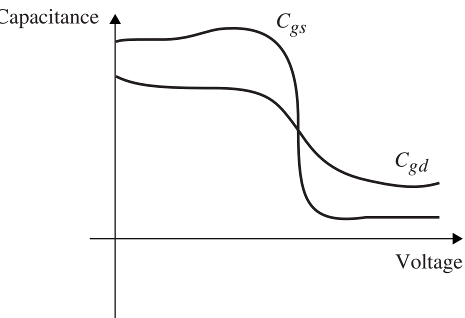


Figure 2.26 Variation of C_{gd} and C_{gs} as a function of v_{DS}.

losses, power MOSFETs are maintained in either the *on* state (conduction state) or *off* state (forward blocking state).

Safe Operation Area The safe operation area (SOA) of a device provides the current and voltage limits the device must handle to avoid destructive failure. The typical SOA for a MOSFET device is shown in Fig. 2.27. The maximum current limit while the device is on is determined by the maximum power dissipation.

$$P_{\text{diss,on}} = I_{DS(\text{on})} R_{DS(\text{on})}$$

As the drain-source voltage starts increasing, the device starts leaving the *on* state and enters the saturation (linear) region. During the transition time the device exhibits

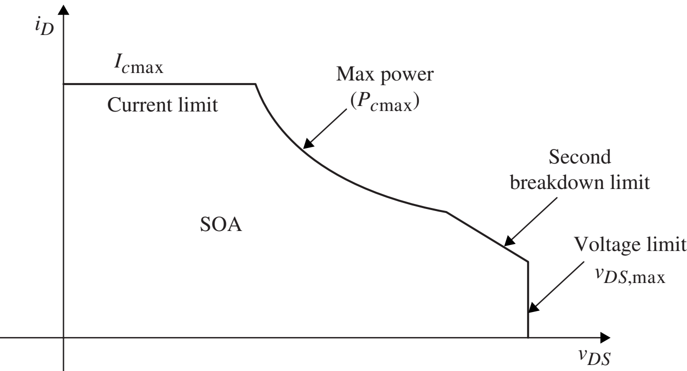


Figure 2.27 Safe operation area for a MOSFET.

large voltage and current simultaneously. At higher drain-source voltage values that approach the avalanche breakdown, it is observed that a power MOSFET suffers from a second breakdown phenomenon. The second breakdown occurs when the MOSFET is in the blocking state (off), and a further increase in v_{DS} will cause a sudden drop in the blocking voltage. The source of this phenomenon in MOSFETs is the presence of a parasitic *n*-type bipolar transistor, as shown in Fig. 2.28. The inherent presence of the body diode in the MOSFET structure makes the device attractive to applications in which bidirectional current flow is needed in the power switches.

Temperature Effect Today's commercial MOSFET devices have excellent response for high operating temperatures. The effect of temperature is more prominent on the *on*-state resistance, as shown in Fig. 2.29. As the *on*-state resistance increases, the conduc-

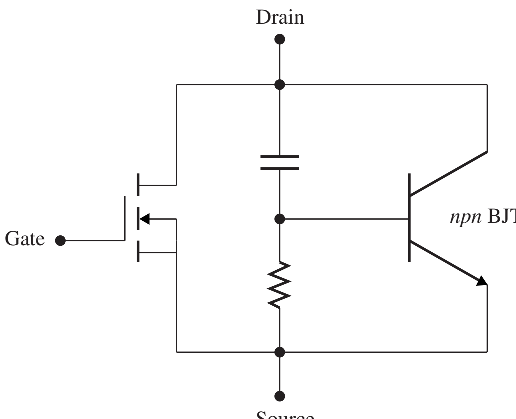


Figure 2.28 MOSFET equivalent circuit including the parasitic BJT.

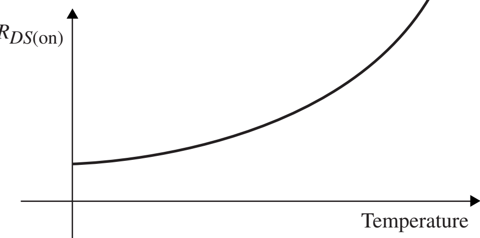


Figure 2.29 The *on*-state resistance as a function of temperature.

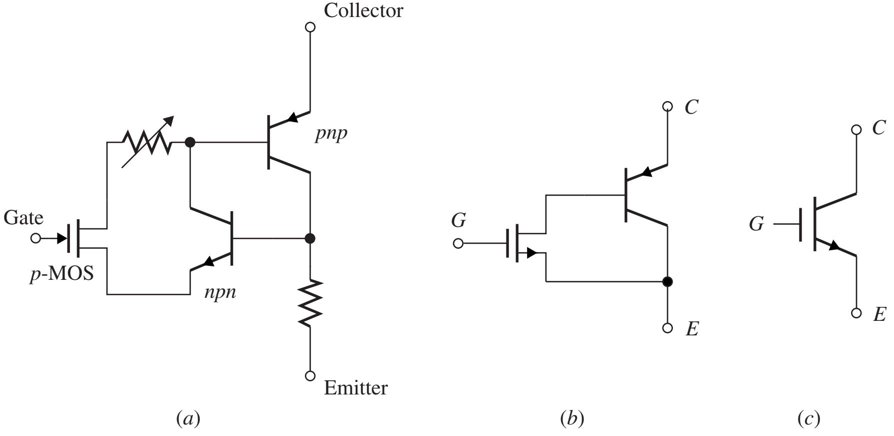


Figure 2.30 (*a*) IGBT equivalent circuit, (*b*) simplified equivalent circuit, and (*c*) symbol.

tion losses also increase. This large $v_{DS(\text{on})}$ limits the use of the MOSFET in high-voltage applications. The use of silicon carbide instead of silicon has reduced $v_{DS(\text{on})}$ manifold.

As the device technology keeps improving in terms of switch speeds and power-handling capabilities, it is expected that the MOSFET will continue to replace the BJT in all types of power electronic systems.

The Insulated Gate Bipolar Transistor (IGBT)

The detailed equivalent circuit model, the simplified two-transistor circuit model, and the schematic symbol for the insulated gate bipolar transistors (IGBT) are shown in Fig. 2.30(*a*), (*b*) and (*c*), respectively. Its *i-v* characteristic is similar to the MOSFET device and is not shown here. Since the IGBT architecture consists of a MOSFET and a BJT as shown in Fig. 2.30(*b*), it is clear that the IGBT has the high input impedance of the MOSFET along with the high current gain and small *on*-state conduction voltage of the BJT. The device was commercially introduced in 1983 and combines the advantages of MOSFETs, BJTs, and thyristor devices: the high current density allowed in BJT devices and the low-power gate drive needed in MOSFET devices.

The device is turned off by zero gate voltage, which removes the conducting channel. However, a negative base cannot turn off the *pnp* transistor current. As a result the turn-off time is higher in the IGBT than in the bipolar transistor. However, like the GTO (to be discussed shortly), the IGBT has a tail current at turn-off due to the recombination of carriers from the base region. At turn-on, a positive gate voltage is applied with respect to the emitter of the *npn* transistor, creating an *n*-channel in the MOS device that causes the *pnp* transistor to start conducting.

Its input capacitance is significantly smaller than that of the MOSFET device, and the device does not exhibit the second-breakdown phenomenon. It is faster than the BJT and can operate up to 20 kHz in medium-power applications. Currently, it is available at ratings as high as 1.2 kV and 400 A. The improvement in its fabrication is promising, and it is expected that it will replace the BJT in the majority of power electronics applications.

2.5.2 Thyristor-Based Devices

The generic term *thyristor* refers to the family of power semiconductor devices made of three *pn* junctions (four layers of *pnpn*) that can be latched into the *on* state through an external gate signal that causes a regeneration mechanism in the device. In this section, we will discuss four main members of the thyristor family that are currently used in power electronic circuits: The silicon-controlled rectifier (SCR), gate turn-off thyristor (GTO), triode ac switch (triac), static induction transistor (SIT), static induction thyristor (SITH), and MOS-controlled thyristor (MCT).

The Silicon-Controlled Rectifier

The silicon-controlled rectifier (SCR) is the oldest power controllable device utilized in power electronic circuits, introduced in 1958. Unlike the diode, the SCR can block voltages bidirectionally and carry current unidirectionally. Until the 1970s, when power transistors were presented, the conventional thyristor had been used extensively in various industrial applications. The SCR is a three-terminal device composed of a four-semiconductor *pn* junction. Unlike the diode, the SCR has a third terminal called the "gate" used for control purposes.

The symbol and *i*-*v* characteristics for the SCR are shown in Fig. 2.31(*a*) and (*b*), respectively. The ideal switching characteristic curves are shown in Fig. 2.31(*c*), where v_{AK} and i_A are the voltage across the anode-cathode terminals and the current through the anode, respectively.

The *latching current* is always less than the minimum trigger current specified in the device's data sheet. The *holding current* is the minimum forward current the SCR can carry in the absence of a gate drive. The *forward breakover voltage*, V_{BO}, is the voltage across the anode-cathode terminal that causes the SCR to turn on without the application of a gate current. *Reverse avalanche* (breakdown) occurs when v_{AK} is negatively large.

The normal operation of the SCR occurs when its gate is used to control the turn-on process by injecting a gate current i_G to allow the forward current to flow; v_{AK} is positive and can be turned off by applying a negative v_{AK} across it.

It must be noted that once the SCR is turned on, the gate signal can be removed. For this reason, this device is also known as a *latch device*. The gate current must be applied for a very short time and normally can go up to 100 mA. Once the SCR is turned on, it has a 0.5–2 V forward voltage.

The physical structure of the SCR consists of three *pn* junctions, as shown in Fig. 2.32. The different doping levels shown are used to help sustain a large block voltage and speed the breakdown process. Under no external bias voltage, the majority carriers diffuse across the junctions and recombine with the minority carriers, resulting in zero net current.

The Off State Generally speaking, thyristor turn-off can be carried out by reversing the anode-cathode voltage (i.e., through natural ac commutation), or it can be turned off through forced commutation by switching a previously negatively charged capacitor across the SCR or by the insertion of a series impedance to reduce the forward current below the device's holding current.

In order to turn off the SCR, v_{AK} must be negative ($v_{AK} < 0$); of course, the triggering gate signal is immaterial (the presence of i_G only increases electron movement across the junction J_2). Under this condition, junctions J_1 and J_3 are reverse biased and

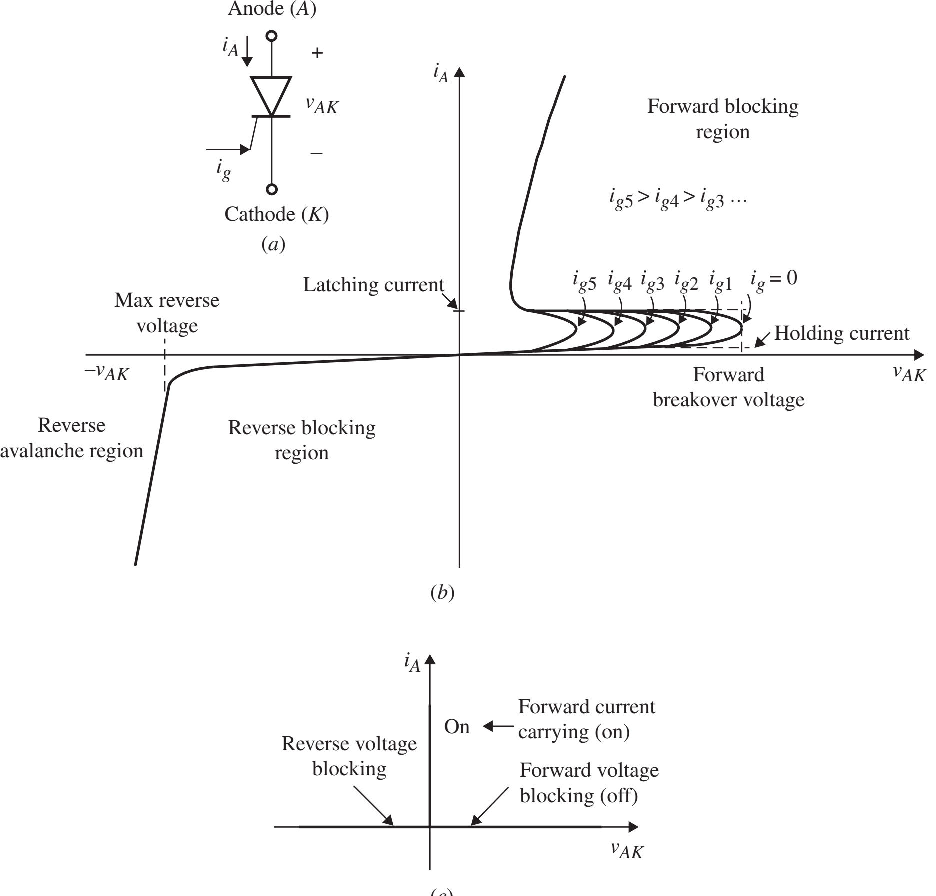


Figure 2.31 SCR switching characteristics. (*a*) Symbol. (*b*) *i-v* characteristics. (*c*) Ideal switching characteristics.

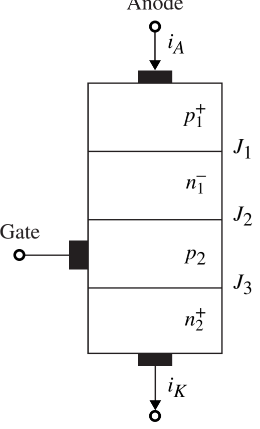


Figure 2.32 Simplified physical structure of the SCR: no biasing.

junction J_2 is forward biased. Like two reverse-bias diodes, the only currents that flow through the device are the leakage currents, I_{s1} and I_{s3}, of junctions J_1 and J_3, respectively. Notice that the larger the depletion region driven to the low doping level of n_1 compared to p_1, as shown in Fig. 2.33(a), the larger the reverse voltage and the wider the depletion regions of J_1 and J_3 become. Junction J_2 is forward biased with forward current, I_{F2}, equal to $(I_{s1} = I_{s3})$. The junction J_3 breaks down at lower voltages than J_1 due to different doping levels, and the large reverse blocking voltage is sustained by junction J_1.

Typical turn-off times for the SCR range from a few microseconds to 100 μs for low and high voltage ratings, respectively.

The On State To turn on the SCR in the conduction state, a positive anode-cathode voltage must be applied ($v_{AK} > 0$) *and* a gate current must be injected to initiate the *on*-state regeneration process. For $v_{AK} > 0$ and $i_G = 0$, junctions J_1 and J_3 are in the forward-bias states and J_2 is in the reverse-bias state. Since n_1 is less doped than the p_2 region, the depletion region grows mostly into the n_1 region, as shown in Fig. 2.33(b).

Without a trigger current ($i_G = 0$), the junction J_2 is in the forward-blocking condition, and the only current that flows in the device is the small leakage current, I_{s2}, through J_2 since it is reverse biased. The forward current remains small until the critical forward breakover voltage, V_{BO}, is exceeded. At this point, the potential energy of the barrier at junction J_2 increases, accelerating the electron-hole pair generation until avalanche breakdown occurs, resulting in the thyristor being switched rapidly into the conduction state. This trigger mechanism should be avoided unless specified as safe by the manufacturer.

Gate triggering is achieved when a small pulse current, i_G, is injected at the gate, introducing an avalanche condition across J_2 and forward currents, I_{F1} and I_{F3}, that flow through J_1 and J_3, respectively. In order to explain the thyristor gate firing mechanism, normally the SCR is replaced by the model of two interconnected complementary *pnp* and *npn* transistors Q_1 and Q_2, respectively, as shown in Fig. 2.34.

We consider only the forward blocking and forward conducting states, since in the reverse blocking state the only current that flows is the leakage current of Q_1 and Q_2.

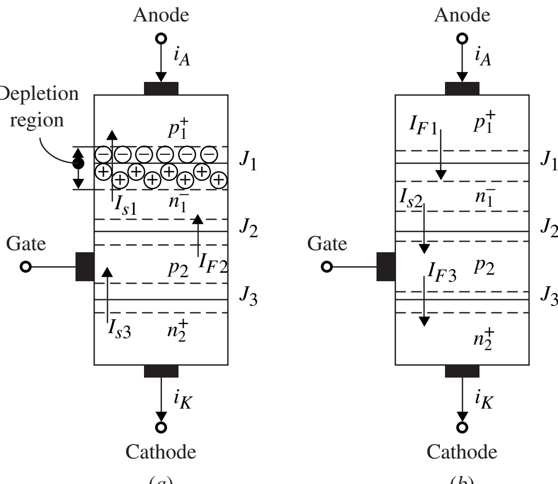


Figure 2.33 Depletion layer (a) under reverse bias ($v_{AK} < 0$) and (b) under forward bias ($v_{AK} > 0$).

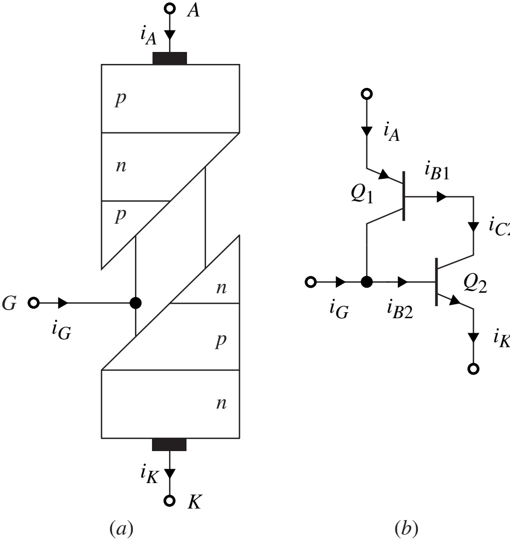


Figure 2.34 Two-transistor analogy model for the SCR. (*a*) *pn* junction representation. (*b*) Transistor circuit representation.

To derive the terminal current relation for the SCR, we turn to the large-signal model of the transistor, called the Ebers-Moll (EM) model, which is used for both transistor junctions, the *npn* and the *pnp*. Figure 2.35(*a*) and (*b*) shows the EM models for the *npn* and *pnp* transistors, respectively. Here α_{F1}[4] and α_{F2} denote the forward α, which is close to unity, and α_{R1} and α_{R2} denote the reverse α, which is normally very small (0.02). For simplicity we will assume α_{R1} and α_{R2} are zero. The currents $I_{D,BC}$ and $I_{D,CB}$ represent the diode leakage currents for the base-collector diode of Q_2 and the collector-base diode of Q_1 when both transistors are in the active mode. These currents are also known as the collector-to-base saturation current while the emitter is open-circuit, I_{CBO2}, for the *npn* transistor, and base-to-collector current, I_{BCO1}, for the *pnp* transistor. The direction of I_{CBO2} and I_{BCO1} are opposite to the direction of the leakage currents as shown in Fig. 2.35(*a*) and (*b*). Recall that, in the active region, the base-emitter junction is forward biased and the base-collector junction is reverse biased.

First, let us assume there's no gate triggering ($i_G = 0$). Replacing the equivalent EM models of Fig. 2.35(*a*) and (*b*) into Fig. 2.35(*c*), we obtain the two-transistor equivalent circuit model. With simple algebraic manipulation, we can show that

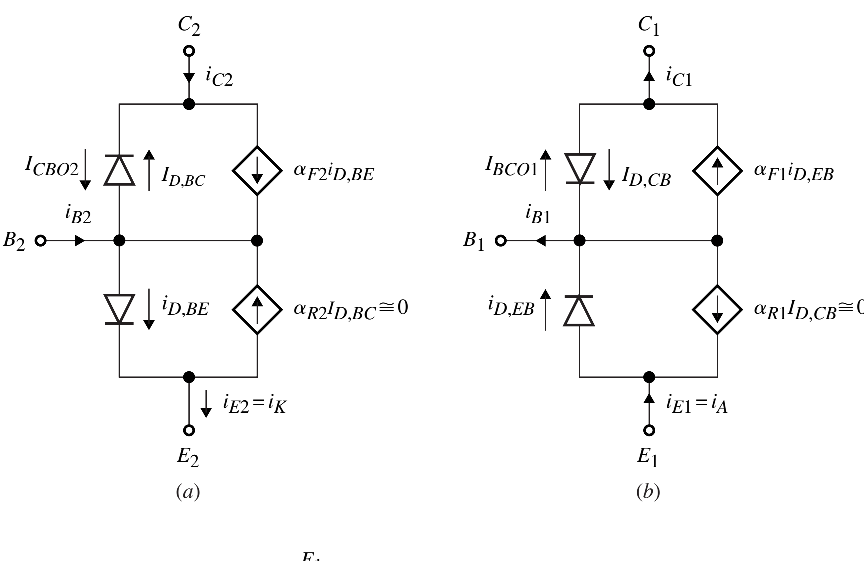
$$i_K = i_A = \frac{I_{CBO1} + I_{BCO2}}{1 - (\alpha_1 + \alpha_2)}$$

With $i_G = 0$, the only current that will flow is the leakage current (α_1 and α_2 are small). Normally $\alpha_1 + \alpha_2 \ll 1$ to keep it off. If $\alpha_1 + \alpha_2 = 1$, the SCR will enter a sustained breakdown, with the anode current limited only by the external circuitry.

To avoid entering the breakdown region, a gate signal is injected, resulting in the following forward current:

$$i_A = \frac{i_G\alpha_2 + I_{CBO1} + I_{BCO2}}{1 - (\alpha_1 + \alpha_2)} \tag{2.1}$$

[4]Forward α (α_F) is the same as the single transistor's α when operating in the active region, given by $\alpha = \beta/(1+\beta)$, where β is the transistor current gain, $\beta = I_C/I_B$.



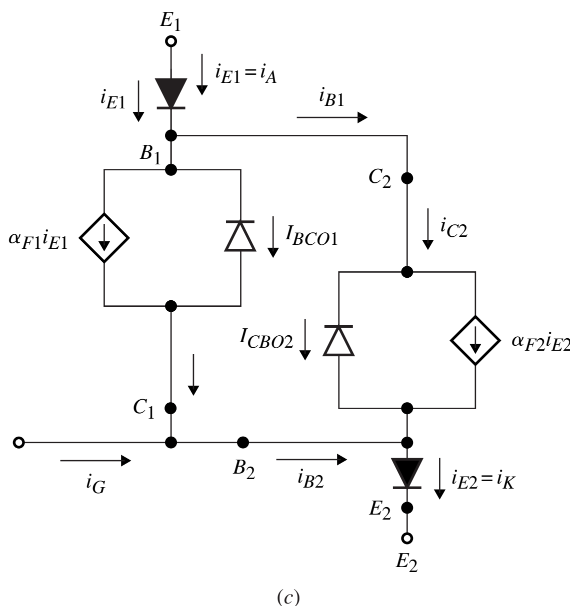


Figure 2.35 Complete Ebers-Moll model for (*a*) the *npn* transistor and (*b*) the *pnp* transistor. (*c*) Equivalent circuit model for Fig. 2.34(*b*).

$$i_K = \frac{(1-\alpha_1)i_G + I_{CBO1} + I_{BCO2}}{1-(\alpha_1+\alpha_2)} \tag{2.2}$$

For the generation process to start, we design the SCR for $\alpha_1 + \alpha_2 \approx 1$.

EXERCISE 2.7

Show that for the generation process to start, the following relation must be satisfied:

$$\beta_1\beta_2 \leq 1$$

When the thyristor was invented, all the schemes for force-commutating mercury-arc rectifiers of the 1930s soon became thyristor-based circuits with expanded applications to include ac drives and UPSs. However, because of their cost and low efficiency, thyristor circuits did not penetrate the adjustable-speed-drive application area. Today's applications range from single phase-controlled rectifier circuits to static var compensation in utility systems. Because of its limited frequency of operation, the application of the thyristor has reached saturation.

The Gate Turn-off Thyristor (GTO)

The schematic symbol and the practical and ideal switching *i-v* characteristics for the gate turn-off thyristor (GTO) are shown in Fig. 2.36(*a*), (*b*), and (*c*), respectively. The device is as old as the SCR and was introduced commercially in 1962. Like the SCR, it can be turned on with a positive gate signal, but unlike the SCR, applying a negative gate signal, as shown in Fig. 2.36(*b*), turns off the GTO. Once the GTO is turned on or off, the gate signal can be removed. The device has a higher *on*-state voltage than the SCR at comparable currents. The GTO is normally an *off* device; it has a very poor turn-off current gain and it exhibits a second-breakdown problem at turn-off.

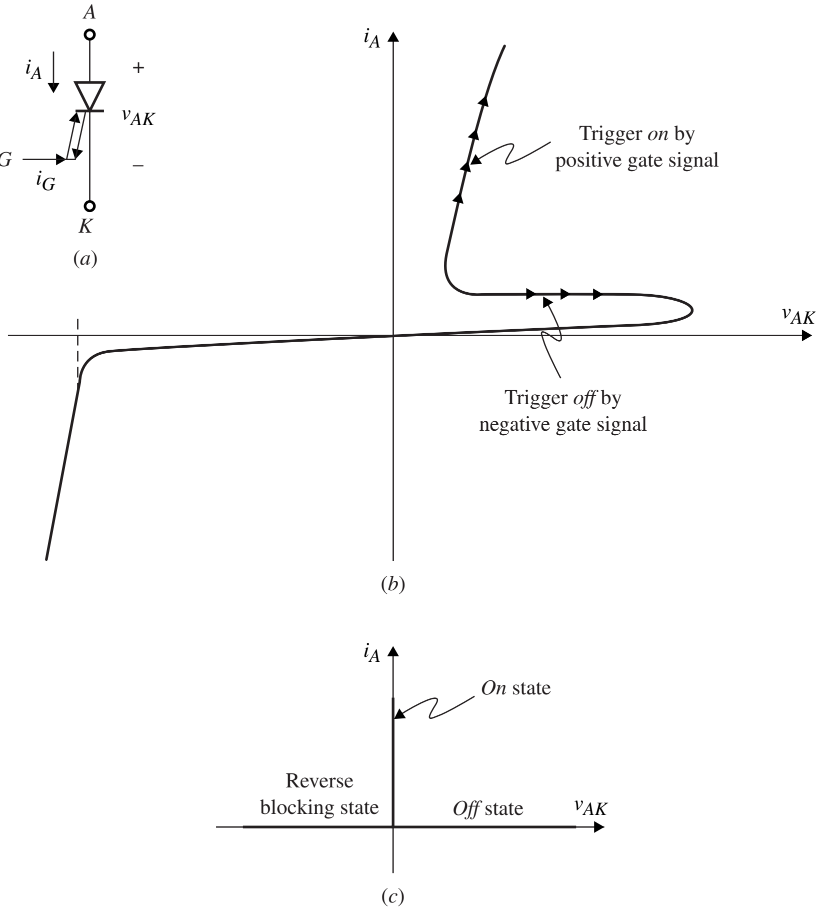


Figure 2.36 GTO switching characteristics. (*a*) Symbol. (*b*) *i-v* characteristics. (*c*) Ideal switching characteristics.

Because of its high switching power dissipation, the GTO's frequency of operation is limited to less than 1 kHz, and modern GTO devices are rated at 4.5 kV and at currents as high as 3 kA. The GTO is used in high current and voltage applications, such as voltage-fed inverters and induction heating resonant converters.

The Triode AC Switch (Triac)

Like the GTO, the *tri*ode *ac* (triac) switching device was introduced immediately after the SCR. In fact, the triac is nothing but a pair of SCRs connected in reverse-parallel on one integrated chip, as shown in Fig. 2.37. It is also known as a bidirectional SCR. The triac's equivalent circuit and the circuit schematic symbol are shown in Fig. 2.37(*a*) and (*b*), respectively. The device can be triggered in the positive and negative half-cycle of the ac voltage source by applying a positive or a negative gate signal, respectively. Today's triac ratings are up to 800 V at 40 A. The *i-v* characteristics and the ideal switching characteristics are shown in Fig. 2.37(*c*) and (*d*). Use of the triac is considerably limited due to its low rates of rise of voltage and current. Applications include light dimming, heating control, and various home appliances.

The Diac

Finally, we should mention another power device known as the diac, which is essentially a gateless triac constructed to break down at low forward and reverse voltages. The diac is mainly used as a triggering device for the triac.

Static Induction Transistors and Thyristors

In 1987 a device known as the static induction transistor (SIT) was introduced. One year later, the static induction thyristor (SITH) was introduced. The symbols for the SIT and SITH are shown in Fig. 2.38(*a*) and (*b*), respectively.

The SIT is a high-power and high-frequency device. The device is almost identical to the JFET, but with its special gate construction it has a lower channel resistance compared to the JFET.

The SIT and SITH are normally *on* devices and have no reverse voltage blocking capabilities. The SITH device turns off in the same way as the GTO, by applying a negative gate current, but it has a higher conduction drop than the GTO. Finally, both devices are majority-carrier devices with positive temperature coefficients, allowing device paralleling.

Among the SIT's major applications are audio and VHF/UHF amplifiers, microwaves, AM/FM transmitters, induction heating, and high-voltage, low-current power supplies. It has a large forward voltage drop compared to the MOSFET; hence, it is not normally used in power electronic converter applications. The applications of the SITH include static var compensators and induction heating.

The MOS-Controlled Thyristor

The simplified equivalent circuit model and the schematic symbol for a *p*-type MOS-controlled thyristor (MCT) are shown in Fig. 2.39(*a*) and (*b*), respectively. Its ideal *i-v* switching characteristic is similar to that of the GTO, as shown in Fig. 2.39(*c*). The device was commercially introduced in 1988. Like the GTO device, it has a high turn-off current gain.

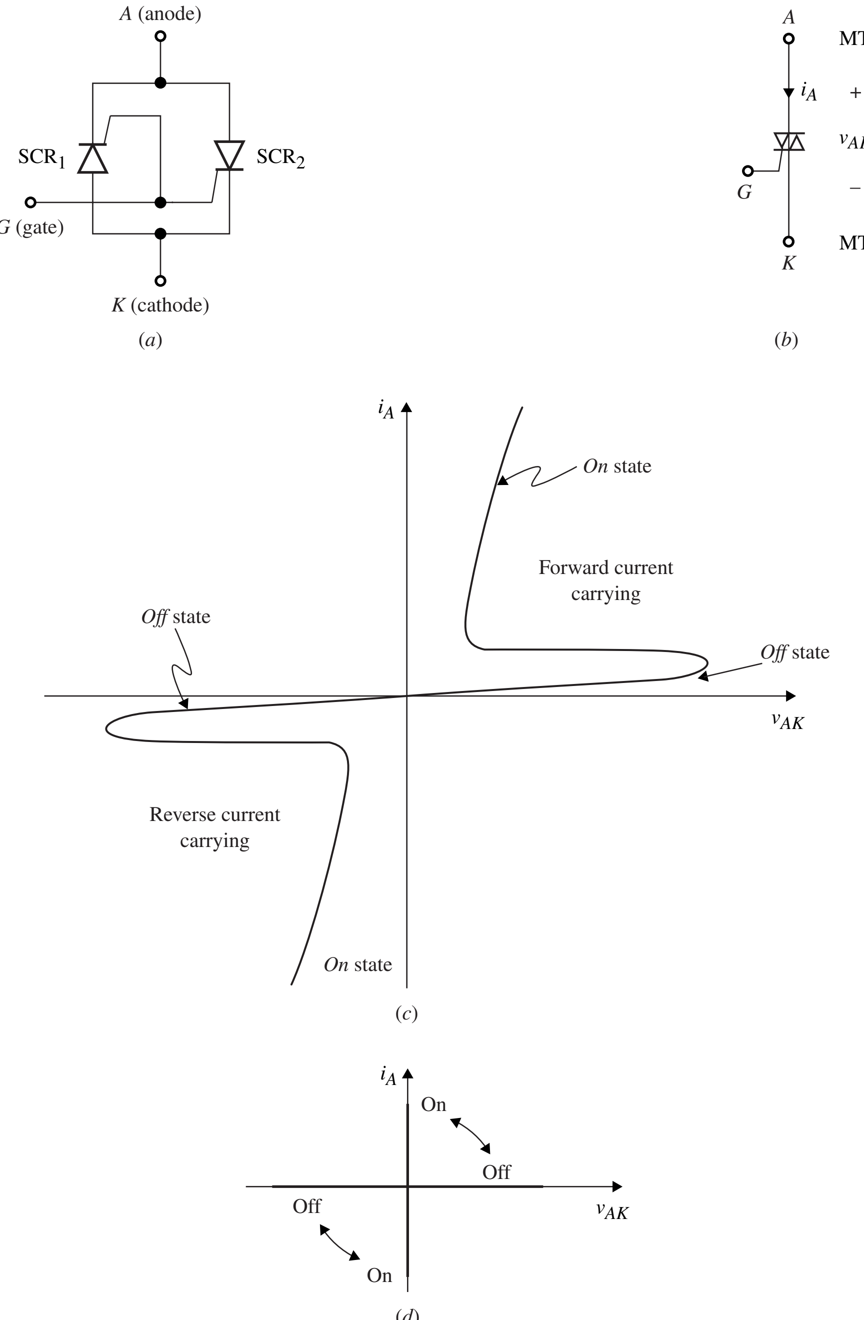


Figure 2.37 Triac switching characteristics. (*a*) Equivalent representation using two SCRs. (*b*) Symbol. (*c*) *i*-*v* characteristics. (*d*) Ideal switching characteristics.

The *p*-MCT is turned on by applying a negative gate voltage (less than –5 V) with respect to the cathode, turning on the *p*-FET and turning off the *n*-FET, initiating the regenerative mechanism in the SCR connected *npn* and *pnp* transistors. Similarly, applying a positive gate signal with respect to the cathode initiates the turn-off. The *n*-MCT has the same device structure, except that the *p*-FET and *n*-FET are

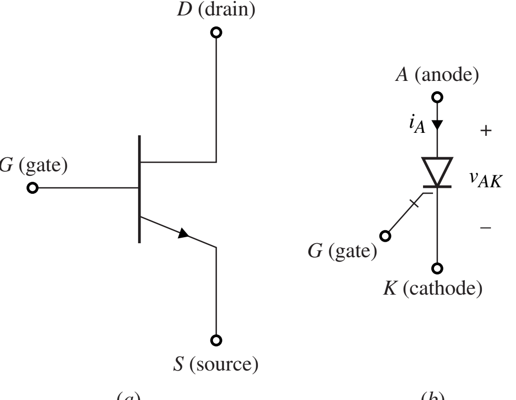


Figure 2.38 (*a*) SIT symbol. (*b*) SITH symbol.

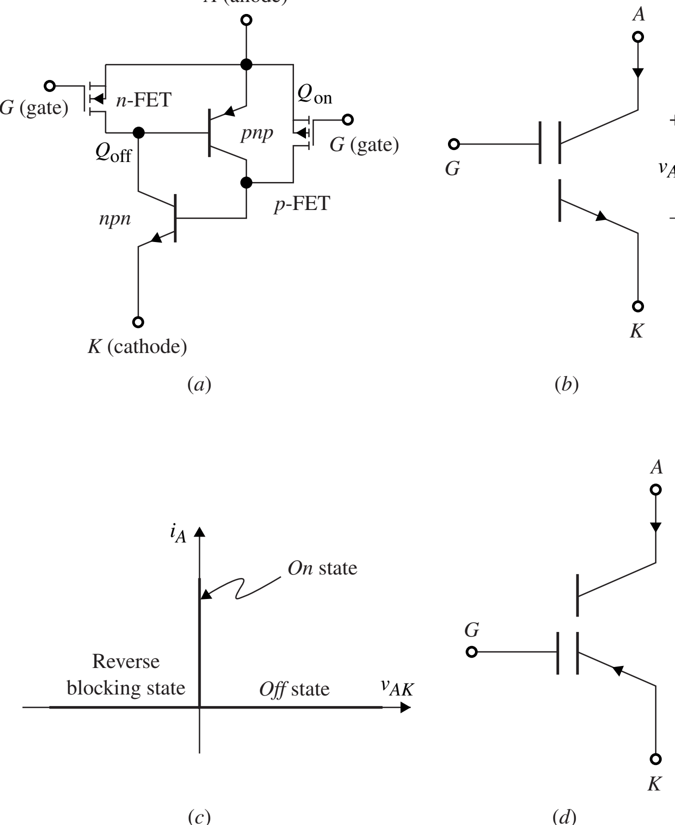


Figure 2.39 MCT switching characteristics. (*a*) Equivalent circuit. (*b*) *p*-MCT symbol. (*c*) Ideal switching characteristics. (*d*) *n*-MCT symbol.

interchanged; hence, a positive and a negative gate signal turns the *n*-MCT on and off, respectively. The schematic symbol for the *n*-MCT is shown in Fig. 2.39(*d*).

The MCT's current and voltage ratings exceed 1 kV and 100 A and are continuously being improved. The device can be easily connected in series and in parallel combinations to boost power rating.

This device is serious competition for the IGBT. It has the same frequency of operation as the IGBT but with a smaller voltage drop and a higher operating temperature. Intensive efforts are under way to introduce a new improvement in the device, and it is expected to receive wider acceptance in medium- and high-power applications.

Other Power Devices

Other devices of the thyristor family include the reverse-conducting thyristor (RCT), which is nothing but a built-in anti-parallel body diode connected across the SCR to allow current to flow in the opposite direction, and the light-activated SCR (LASCR), which is used in high-voltage and high-current applications such as HVDC systems. Their power ratings go up to hundreds of kilovolts and hundreds of kiloamperes, and they provide complete electrical isolation between the power and control circuits.

2.6 COMPARISON OF POWER DEVICES

Depending on the applications, the power range processed in power electronics is very wide—from hundreds of milliwatts to hundreds of megawatts. Therefore, it is very difficult to find a single switching device type to cover all power electronics applications. Today's available power devices have tremendous power and frequency rating ranges as well as diversity. Their forward current ratings range from a few amperes to a few kiloamperes, their blocking voltage rating ranges from a few volts to a few kilovolts, and their switching frequency ranges from a few hundred hertz to a few megahertz, as illustrated in Table 2.2. This table gives only relative comparison between available power semiconductor devices because there is no straightforward technique that gives a ranking for these devices. Devices are still being developed very rapidly with higher current, voltage, and switching frequency ratings. Figure 2.40 shows a plot of frequency versus power, illustrating these rating ranges for various available power devices.

2.7 FUTURE TRENDS IN POWER DEVICES

It is expected that improvements in power-handling capabilities and increases in the frequency of operation of power devices will continue to drive the research and developments in semiconductor technology. From power MOSFETs to power MOS-IGBTs

Table 2.2 Comparison of Power Semiconductor Devices

Device type	Year made available	Rated voltage	Rated current	Rated frequency	Rated power	Forward voltage
Thyristor (SCR)	1957	6 kV	3.5 kA	500 Hz	100s MW	1.5–2.5 V
Triac	1958	1 kV	100 A	500 Hz	100s kW	1.5–2 V
GTO	1962	4.5 kV	3 kA	2 kHz	10s MW	3–4 V
BJT (Darlington)	1960s	1.2 kV	800 A	10 kHz	1 MW	1.5–3 V
MOSFET	1976	500 V	50 A	1 MHz	100 kW	3–4 V
IGBT	1983	1.2 kV	400 A	20 kHz	100s kW	3–4 V
SIT	1987	4 kV	600 A	100 kHz	10s kW	10–20 V
SITH	1975	4 kV	600 A	10 kHz	10s kW	2–4 V
MCT	1988	3 kV	2 kV	20–100 kHz	10s MW	1–2 V

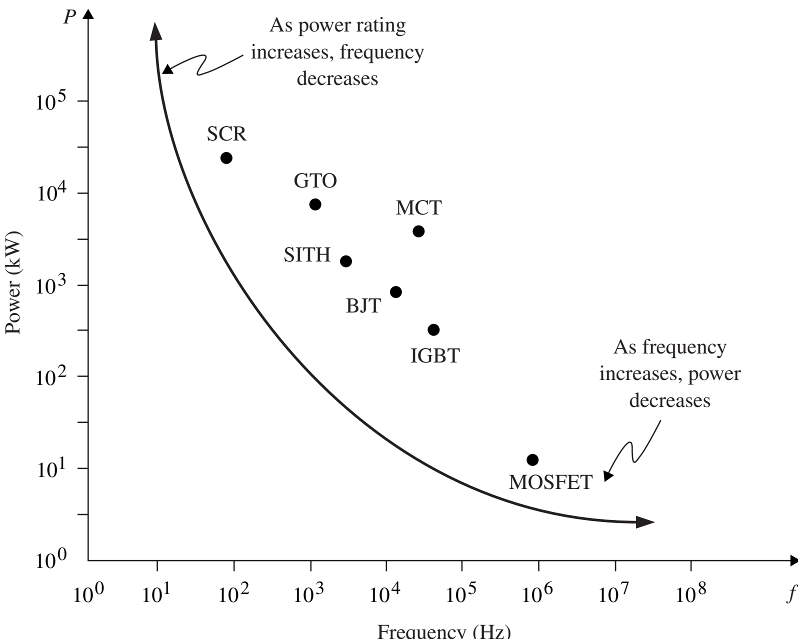


Figure 2.40 Frequency versus power rating ranges for various power devices.

to power MOS-controlled thyristors, the power rating has consistently increased by a factor of 5 from one type to another. Major research activities will focus on obtaining new device structures based on the MOS-BJT technology integration to rapidly increase power ratings. It is expected that the power MOS-BJT technology will capture more than 90% of the total power transistor market.

The continuing development of power semiconductor technology has resulted in power systems with driver circuits, logic and control, device protection, and switching devices designed and fabricated on a single chip. Such power IC modules are called "smart power" devices. For example, some of today's power supplies are available as ICs for use in low-power applications. There is no doubt that the development of smart power devices will continue in the near future, addressing more power electronics applications.

2.8 SNUBBER CIRCUITS

To relieve switches from overstress during switching, switching aid circuits, known as *snubber circuits*, are normally added to the power switching device. The objectives of snubber circuits may be summarized as (1) reducing the switching power losses in the main power device in the power electronic circuit, (2) avoiding second breakdowns, and (3) controlling the device's dv/dt or di/dt in order to avoid latching in *pnpn* devices. There are a wide range of turn-on and turn-off snubber circuits available in today's power electronic circuits. These include dissipative and nondissipative passive snubber circuits, and nondissipative active snubber circuits. In dissipative snubber circuits a capacitor is used to slow the device's voltage rise during turn-off, or an inductor to slow the device's current rise during turn-on. Figure 2.41(a) and (b) shows popular turn-off and turn-on snubber circuits, respectively. In Fig. 2.41(a), a capacitor is used to reduce the voltage rise dv_{sw}/dt across the switch during turn-off. In Fig. 2.41(b), a snubber inductor, L_s, is used to slow down the rise of the inductor current

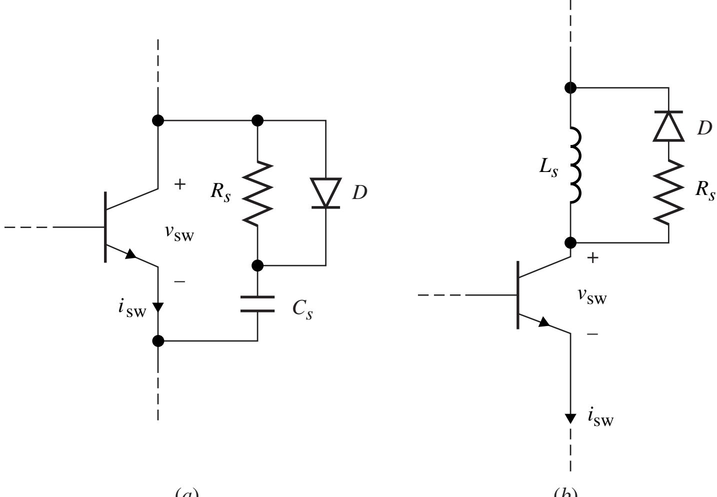


Figure 2.41 Passive snubber circuits: (*a*) turn-off and (*b*) turn-on snubber circuits.

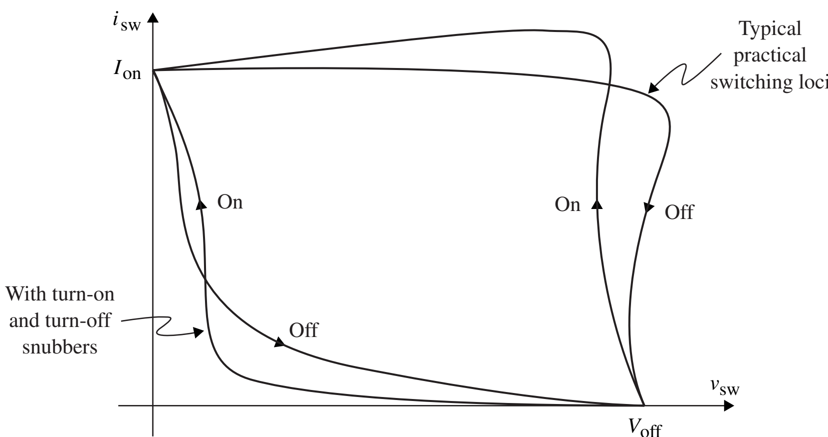


Figure 2.42 i_{sw} versus v_{sw} switching loci.

di_{sw}/dt (the inductor current equals the switch current, i_{sw}). Figure 2.42 shows the switching loci for a practical switch (transistor) with and without snubber circuits. For a detailed discussion on all types of snubber circuits and their design methods, refer to the references at the end of the textbook.

PROBLEMS

Ideal Switch Characteristics

2.1 Consider the switching circuit shown in Fig. P2.1 with a resistive load. Assume the switch is ideal and operating at a duty ratio of 40%.

(a) Sketch the waveforms for i_{sw} and v_{sw}.

(b) Determine the average output voltage.

(c) Determine the average output power delivered to the load.

(d) Determine the average output power supplied by the dc source.

(e) Determine the efficiency of the circuit.

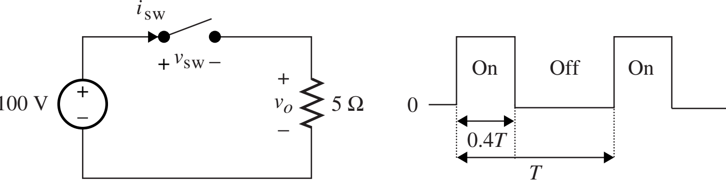


Figure P2.1

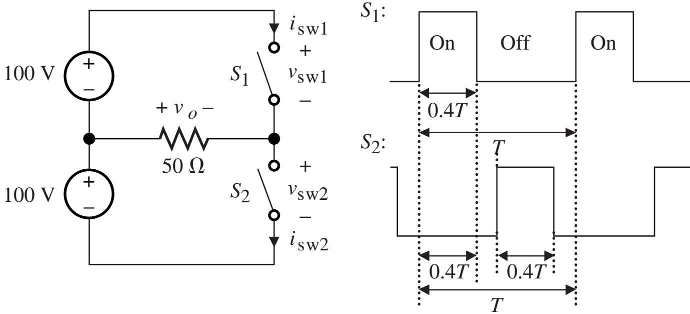


Figure P2.2

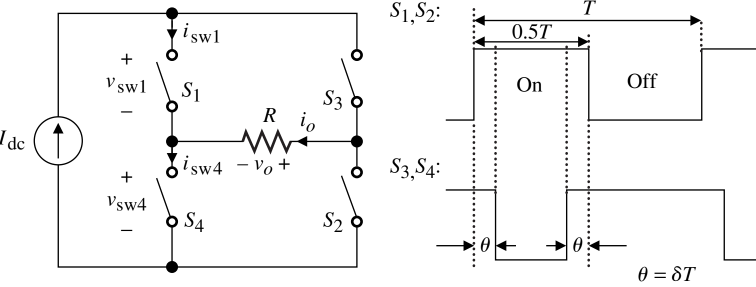


Figure P2.3

2.2 Consider the two-switch circuit given in Fig. P2.2. Assume ideal S_1 and S_2 with the shown switching sequence. Sketch i_{sw1}, v_{sw1}, i_{sw2}, and v_{sw2}. Determine (*a*) the average output voltage, (*b*) the average power delivered to the load, and (*c*) the efficiency.

2.3 The circuit shown in Fig. P2.3 is known as a current-driven full-bridge inverter. Assume S_1, S_2, S_3, and S_4 are ideal, with their switching waveforms as shown. Sketch the waveforms for i_o, v_o, v_{sw1}, i_{sw1}, v_{sw4}, and i_{sw4}, and derive the expression for the average output voltage.

Nonideal Switching Characteristics

2.4 Use Fig. E2.1 and by assuming that the switching waveform has the following parameters,

$I_{on} = 1$ A, $V_{off} = 150$ V, $I_{off} = 10$ μA, $V_{on} = 2$ V, $T_s = 10^{-4}$ s, $t_d = 90$ ns, $t_{fall} = 120$ ns, $t_{rise} = 100$ ns

determine the equation for the instantaneous power and find P_{ave}.

2.5 Repeat Problem 2.1 by assuming the switch has a 0.2 Ω *on*-state resistance and a 2 V forward drop during conduction.

2.6 Repeat Problem 2.3 by assuming each switch has a 0.2 Ω *on*-state resistance and a 2 V forward voltage drop during conduction.

2.7 Consider the circuit of Fig. P2.3 by assuming each switch has a forward voltage drop, V_F, and an *on*-state resistance r_{on}. Derive the expression for the circuit's efficiency in terms of I_{dc}, R, δ, V_F, and r_{on}. Determine δ for maximum efficiency.

2.8 Determine the conduction and switching average power dissipation for Example 2.2 by using $t_{on} = 5$ μs, $t_{off} = 8$ μs, $T_s = 150$ μs, $V_{off} = 150$ V, $V_{on} = 0.7$ V, and $I_{on} = 15$ A.

Figure P2.10

2.9 Repeat Problem 2.8 for Fig. E2.1 with $t_d = 4\ \mu s$.

2.10 Consider a power switching device whose current and voltage waveforms are as shown in Fig. P2.10.

(a) Derive the expression for the instantaneous power and sketch it.

(b) Determine the average power dissipation.

(c) Calculate part (*b*) for $t_r = 120$ ns, $t_f = 180$ ns, $t_d = 90$ ns, $f_s = 100$ kHz, $V_{\text{off}} = 150$ V, and $I_{\text{on}} = 15$ A.

(d) Repeat parts (*a*)–(*c*) by assuming $V_{\text{on}} = 2$ V and $I_{\text{off}} = 10\ \mu$A.

2.11 Use the linear approximated switching current and voltage given in Fig. 2.4 with zero forward voltage and zero leakage (reverse) current.

(a) Calculate the average power for $t_{\text{on}} = 5\ \mu$s, $t_{\text{off}} = 8\ \mu$s, $T_s = 150\ \mu$s, $V_{\text{off}} = 150$ V, and $I_{\text{on}} = 15$ A.

(b) Repeat part (*a*) by assuming the t_{on} is measured from 10% to 90% of I_{on}, and t_{off} is 10% to 90% of V_{off}.

2.12 The switching current and voltage waveforms of Fig. 2.3 at turn-on are represented mathematically as follows:

$$i_{\text{sw}} = I_{\text{on}}(1 - e^{-t/\tau})$$

$$v_{\text{sw}} = V_{\text{off}}\, e^{-t/\tau}$$

where τ represents the time constant, which is a function of the *on*-state resistance of the device and its capacitance. Assume negligible I_{off} and V_{on}. Show that the switching power dissipation at turn-on is given by

$$P_{\text{diss}} = \frac{V_{\text{off}} I_{\text{on}}}{2T_s}\tau$$

Assume $t_{\text{on}} \gg \tau$ and $t_{\text{off}} \gg \tau$.

2.13 Assume the switching current and voltage of Fig. E2.1 at the turn-off interval ($0 \le t \le t_d + t_{\text{off}}$) are represented as follows:

$$v_{\text{sw}}(t) = V_{\text{off}}$$

$$i_{\text{sw}}(t) = I_{\text{on}} e^{-t/\tau}$$

Derive the expression for the average switching power dissipation during the *off* time. Assume $t_d + t_f \approx 5\tau$.

2.14 The diode *i-v* characteristic curve in the forward region can be mathematically represented by

$$i_D = I_s e^{v_D/nV_T}$$

where

I_s = reverse saturation current

V_T = thermal voltage, equal to 25 mV at 20°C

n = empirical constant whose value depends on the semiconductor material and the physical construction of the device (normally between 1 and 2)

(a) Show that a decade change in the forward diode current results in a $2.3nV_T$ change in the forward voltage, mathematically expressed as follows:

$$V_{F2} - V_{F1} = 2.3nV_T \log\frac{I_{F2}}{I_{F1}}$$

(b) Consider the circuit of Fig. P2.14. Assume the diode has $I_F = 5$ A at $V_F = 1$ V with $n = 1.5$. Determine i_D and v_D for (i) $R = 10\ \Omega$ and (ii) $R = 5\ \Omega$.

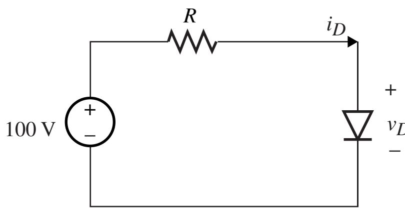


Figure P2.14

General Device Switching Problems

2.15 Consider Fig. P2.15, which shows an approximated reverse recovery turn-off characteristic for a power diode. Show that the following relation can express the total reverse recovery charge, Q_{rr}.

$$Q_{rr} = \frac{1}{2} t_{rr} t_{s1} \frac{di_1}{dt} = \frac{1}{2} t_{rr} t_{s2} \frac{di_2}{dt}$$

where di_1/dt and di_2/dt are the slopes of the diode current during t_{s1} and t_{s2}, respectively.

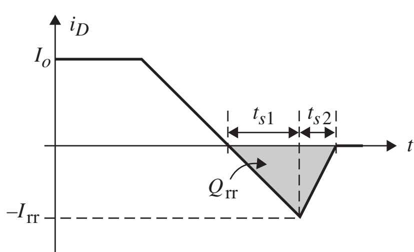
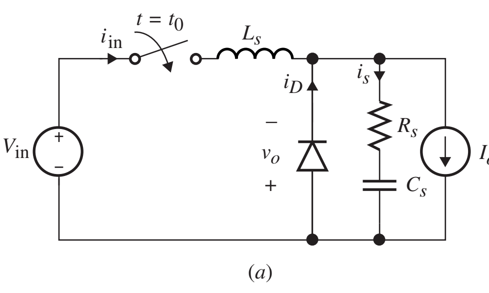


Figure P2.15

2.16 Consider the switching circuit with the series snubber R_s-C_s network connected across the diode as shown in Fig. P2.16. Assume the diode switching characteristic curve is given by Fig. P2.16(*b*) and the switch is ideal.



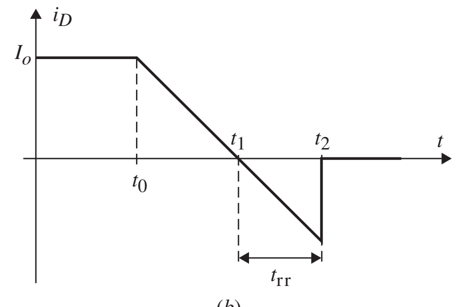


Figure P2.16

(a) Derive the expression for all the branch currents and v_D, and sketch them.

(b) Derive the expression for the capacitor C_s that is needed.

2.17 One way to speed the turn-off time of the Darlington connection is to include a diode between the bases of the two transistors as shown in Fig. P2.17. Discuss how the turn-off speed is improved by adding the diode *D*.

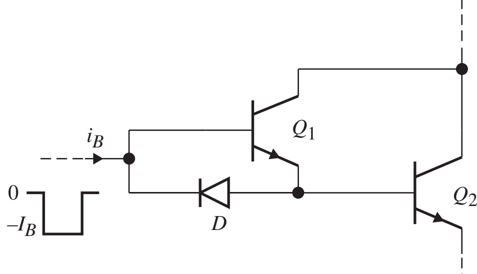


Figure P2.17

2.18 Consider the transistor switching circuit and its switching waveforms in Fig. P2.18(*a*) and (*b*), respectively.

(a) Sketch the waveforms for i_D and v_D.

(b) Calculate the average power dissipated in the transistor.

Use $f_s = 10$ kHz, $t_d = 150$ ns, $t_r = 100$ ns, $t_s = 100$ ns, and $t_f = 250$ ns.

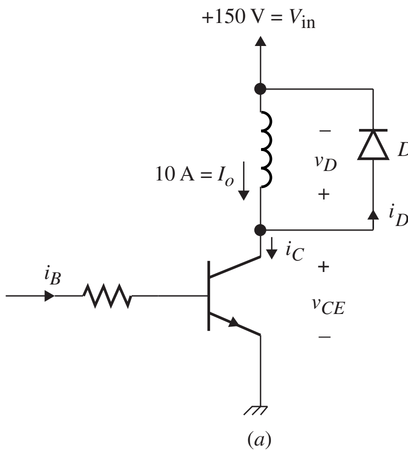


Figure P2.18(*a*)

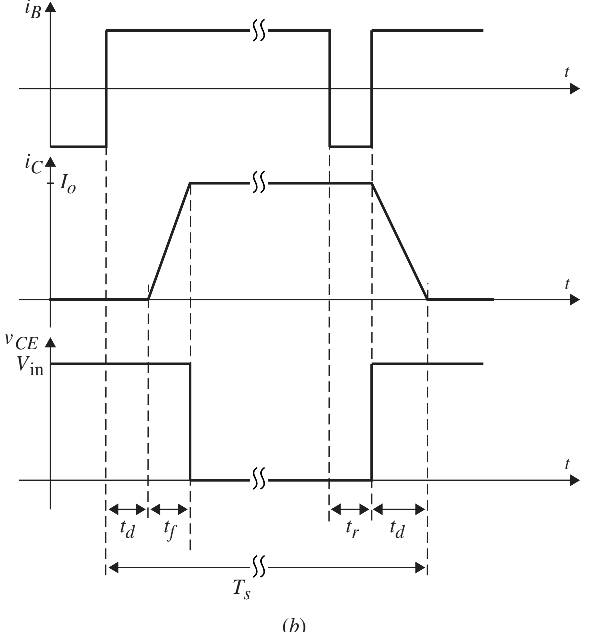


Figure P2.18(*b*)

Figure P2.19

2.19 Figure P2.19 shows a BJT switching circuit known as the Baker clamp, whose objective is to limit how deep in saturation the transistor is permitted to go. Show that if we assume $v_D = V_{BE}$, then the minimum V_{CE} is clamped to V_Z. If the collector is connected to a 15 V power supply through a collector resistor, R_C, and the base is connected to a 5 V power supply through a base resistor, R_B, design for V_Z, R_C, and R_B so that the transistor is driven into saturation with $V_{CE,\text{sat}} = 1.8$ V and $\beta_{\text{forced}} = 10$.

2.20 Derive the SCR forward current relation given in Eqs. (2.1) and (2.2).

2.21 Consider the half-bridge inverter circuits with the unidirectional MOSFET switching a resistive load given in Fig. P2.21. Use $R = 10\ \Omega$.

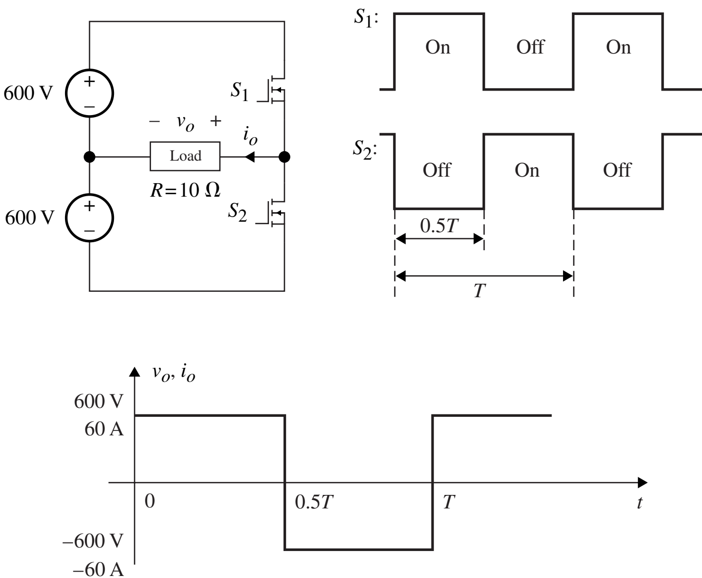


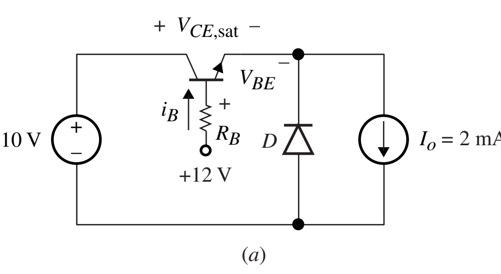
Figure P2.21

(a) Determine the average power delivered to the load when S_1 and S_2 are assumed ideal.

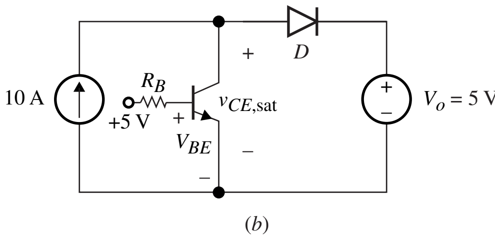
(b) Repeat part (*a*) for $R_{DS(\text{on})} = 0.2\ \Omega$ for each MOSFET.

(c) Find the efficiency of the circuit in part (*b*).

2.22 Calculate β_{forced} in Fig. P2.22(*a*) and (*b*) for $R_B = 1\ \text{k}\Omega$ and $R_B = 10\ \text{k}\Omega$. Assume $V_{BE} = 0.75$ V and $V_{CE,\text{sat}} = 0.4$ V.



(*a*)



(*b*)

Figure P2.22

2.23 Consider the Darlington transistor pair given in Fig. P2.23. Assume transistor Q_1 is driven into saturation with $V_{CE1,\text{sat}} = 0.3$ V and $\beta_{1,\text{forced}} = 0.4$. Calculate $\beta_{2,\text{forced}}$ and $V_{CE2,\text{sat}}$. Use $V_{BE1} = V_{BE2} = 0.7$ V, and $V_B = +5$ V.

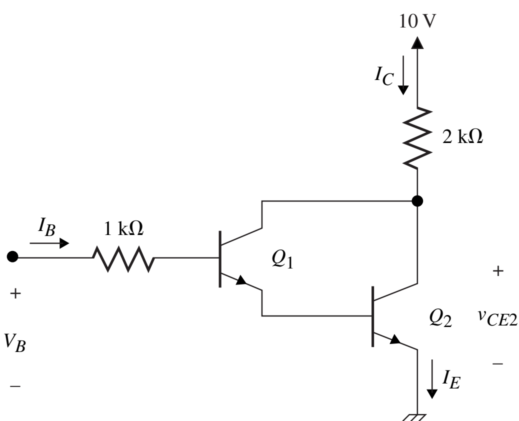


Figure P2.23