HIGH-DENSITY HIGH-CURRENT FAST-TRANSIENT LOW-VOLTAGE DC-DC CONVERTERS

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To my parents

ABSTRACT

Powering requirements of new and future high-performance, high-speed and high-integration density load of DSPs and microprocessors are continuously and increasingly becoming more stringent. More devices are being packaged on a single chip with increased integration density, causing higher load current demands and forcing their operating voltages to drop to levels below one volt. Moreover, such load speeds (operating frequency) are increasing at a fast pace, and they switch the current they draw with increasingly higher slew rates (faster) causing larger voltage deviation during their transients, which should be limited to a very small value especially at low voltages to guarantee safe and high performance operation.

To avoid distribution line parasitics and losses, such loads are not being powered by a DC voltage and current from a centralized power supply as used to be done in the past. Instead, a Distributed Power System (DPS) with a DC-DC converter at its near-load end is placed close to the load. These specially designed DC-DC converters are usually called Voltage Regulator Modules (VRMs) or Point-Of-Load (POL) Converters, and they must satisfy their stringent load requirements of low-voltage, high-current and fast-transient. At the same time, they should maintain high-efficiency and high power density (smaller size) as their loads integration densities becomes higher also. Converter optimizations include power stage and control loop optimization.

The scope of this work is the POL and VRM DC-DC converters requirements, design and optimization. Topologies and control techniques for DC-DC converters are presented after reviewing loads powering requirements and DC-DC converters steady-state and transients design challenges and theoretical analysis.

Non-isolated multiphase voltage-mode hysteretic controlled DC-DC converter control scheme and topology with current sharing is presented and supported by theoretical analysis with output voltage ripple, switching frequency and stability condition equations along with experimental results. This method combines the advantages of the interleaving technique and hysteretic control while achieving current sharing, which results in advantages that include fast transient response and equal current sharing between converter phases.

Then, after reviewing selected isolated topologies, a control method for isolated half-bridge DC-DC converter topology, namely, Duty-Cycle-Shifted (DCS) control, is presented. This method allows soft-switching operation for half-bridge for higher efficiency at higher switching frequency and allows for reduced switching and isolation transformer-leakage inductance-related losses without the penalty of asymmetric components stresses and isolation transformer DC bias. Theoretical discussion and experimental results are presented and compared to other half-bridge control methods.

Another general control method for half-bridge topology, called Alternated Duty Cycle (ADC) control, is also presented. This method can achieve soft switching for half-bridge switches alternatively, if not for the two switches, and can do so without the penalty of asymmetric components stresses and isolation transformer DC bias, while

improving efficiency and maintaining thermal balance of the half-bridge switches. Theoretical discussion and experimental results are presented.

Also presented is the interleaving method for isolated topologies, where the secondary side switches operate at lower switching frequency than the primary side switches to improve efficiency and to improve transient response. Meanwhile, both primary and secondary sides of the isolation transformers are connected in parallel, allowing sharing of currents at both primary and secondary sides. This method resulted in a family of interleaved isolated topologies. Theoretical description and experimental results are also presented.

A Coupled-Inductors Currenr-Doubler (CICD) topology is then presented to allow further output voltage step-down by coupled inductors and to reduce the secondary side current-doubler input current. This is followed by a presentation of a non-isolated Half-Bridge-Buck (HBB) topology, where CICD topology can be also used, resulting in advantages including larger output voltage step-down and better self current sharing, especially when compared to non-isolated, two-phase buck topology. Theoretical analysis and experimental results are presented.

The presentation of control methods and topology for isolated and non-isolated DC-DC converters is followed by initial candidate concepts and work for control and topology techniques as well as programmable digital control. Digital control is discussed as a candidate for future DC-DC converters, while digital system structure, advantages, disadvantages and initial experimental setup are presented also. Moreover, an initial concept for future work on digital control is discussed, namely, the Maximum Efficiency Point Tracking (MEPT) method, which can be used to optimize a switche's dead time

control issue by using adaptive control to achieve better efficiency and converter performance.

Finally, the work is summarized and concluded and future research directions are presented.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Over the last few years, and at a fast pace, many DC loads powering requirements have become increasingly stringent [1-31]. These loads are mainly Digital Signal Processing (DSP) Integrated Circuits (ICs), including those used in communication systems and computers' microprocessors. On one hand, such loads, especially microprocessors, are becoming current hungry, while more functions are integrated in these ICs, which means larger number of transistors. On the other hand, their operating voltages are becoming much lower as the IC integration density increases. Moreover, the speed of these ICs is dramatically increasing, which causes the slew rate (current step change per unit time) of supply current to increase, causing larger supply voltage deviation during these transients at the same time where lower required supply voltages become smaller, and hence, the allowed deviation becomes tighter.

As a result, the steady state and dynamic requirements are becoming stricter, and the dynamic power dissipation reduction becomes important, which makes the power supply design process a difficult task. Moreover, these requirements, i.e., higher currents,

lower voltages, lower allowed voltage deviation and faster current slew rate, can no longer be satisfied from the centralized power supply.

In addition, the required power/current density (smaller size) is continuously increasing, and therefore thermal problems arise, resulting in a high converter efficiency requirement.

In this chapter, powering requirements specifications and issues will be discussed.

1.2 How High is High and How Low is Low: Demands, Growth and Roadmap

In 1995, shipments of the 3.3V microprocessor and memory ICs exceeded the 5V shipment for the first time [21]. Since then, the demand for lower-output-voltage DC-DC converters starts to grow at a larger rate. According to the International Technology Roadmap for Semiconductors (ITRS), the Semiconductor Industry Association (SIA) roadmap, and Intel's Roadmap, the operating voltages for the new and future generation of microprocessors and ICs are in the range of lower than 1.5V and are expected to decrease below 1V while increasing the drawn current from the power supply from range of 50A to break the 100 amperes limit. All this while increasing the load (IC or microprocessor) current slew rate (change of current at faster rate or speed) and deceasing the allowed supply voltage deviation.

Table 1.1 shows example specifications for Intel microprocessors over the past few years [17-20], Table 1.2 shows example specifications from the ITRS-1999 Roadmap [31], while Table 1.3 shows the 2000/2001 Semiconductor Industry Association (SIA) roadmap summary [25,26]. It can be noticed from Table 1.1 that the required supply voltages dropped from 2.8V to lower than 1.6V from Pentium® II

processor to 1.7GHz Pentium® 4 processor. In addition, from Table 1.1, the required supply currents increased from about 14A to above 50A as we go from the Pentium® II processor to the 1.7GHz Pentium® 4 processor.

Table 1.1: Example Specifications for Intel Microprocessors Over the Past Few Years

Parameter/Processor	Pentium® II	Pentium® III	Pentium® 4
Clock Speed (Hz)	233M 2866M 300M	600M 550M 450M	1.4G 1.5G 1.7G
Core Voltage (V) min./max.	2.8	2.05 2.00	1.56/1.7 1.555/1.7 1.53/1.7
Converter Voltage (V) min./max.	-	-	1.627/1.7 1.625/1.7 1.61/1.7
Core Current (A)	11.8 12.7 14.2	17.8 17.0 14.5	-
Converter Current (A)	-	-	40.6 43.0 52.7
Core Current Slew Rate ($A/\mu s$)	30	20	-
Converter Current Slew Rate ($A/\mu s$)	-	-	50

Table 1.2: Example Specifications from the ITRS-1999 Roadmap

Parameter/Year		2002	2003	2004	2005
Supply Voltage (V)	Max.	1.5	1.5	1.2	1.2
	Min.	1.2	1.2	0.9	0.9
Maximum Power with Heat Sink (W)		130	140	150	160
Current (A)		87	93	125	133
Peak-to-Peak Voltage Tolerance (±3%) mV		<90	<90	<72	<72
Chip Frequency (GHz)		2.1	2.49	2.952	3.5

Table 1.3: Example Specifications from the 2000/2001 Semiconductor Industry Association (SIA) Roadmap Summary

Parameter/ Year	**1993**	**1995**	**1999**	**2001**	**2003**	**2005**	**2008**	**2011**	**2014**	**2016**
Feature Size	0.50 microns	0.35 microns	180 nm	130 nm	100 nm	80 nm	70 nm	50 nm	34 nm	22 nm
Internal Clock Frequency	0.20 GHz	0.30 GHz	0.75 GHz	1.68 GHz	2.31 GHz	5.17 GHz	6.74 GHz	11.5 GHz	19.3 GHz	28.7 GHz
Logic Transistors Density	2 $\frac{10^6}{cm^2}$	4 $\frac{10^6}{cm^2}$	6.6 $\frac{10^6}{cm^2}$	13 $\frac{10^6}{cm^2}$	24 $\frac{10^6}{cm^2}$	44 $\frac{10^6}{cm^2}$	109 $\frac{10^6}{cm^2}$	269 $\frac{10^6}{cm^2}$	664 $\frac{10^6}{cm^2}$	—
Voltage	5 Volts	3.3 Volts	2.5 Volts	1.2 Volts	1.0 Volts	0.9 Volts	0.7 Volts	0.6 Volts	0.5 Volts	0.4 Volts

It must be noted that the output current slew required at the converter output is lower than the actual slew rate of the processors. For example, for Pentium® 4 processor, the processor current slow rate is $510A/\mu s$, which is translated to $50A/\mu s$ at the converter output after sufficient capacitive decoupling [20]. This can be explained as shown in Figure 1.1, which shows a simplified general power delivery system model between a DC-DC converter and its load, such as a microprocessor load. In Figure 1.1,

the power delivery system is modeled in three loops constructed by bulk capacitance stage, decoupling capacitance stage, packaging capacitance stage, capacitors and distribution prasatics and die capacitance and parasitics [1,17-20,60], which cause the current slew rate to be reduced as it approaches the converter output. Such model parameters are sometimes given, as in the case of the Pentium® processor design Guidelines [17-20]. The current slew rates at the processor output are expected to increase to approximately double or more of what it is now for Pentium® 4 processor ($510A/\mu s$) in the near future, which will impose a current slew rate at the converter output of about double or more of $50A/\mu s$.

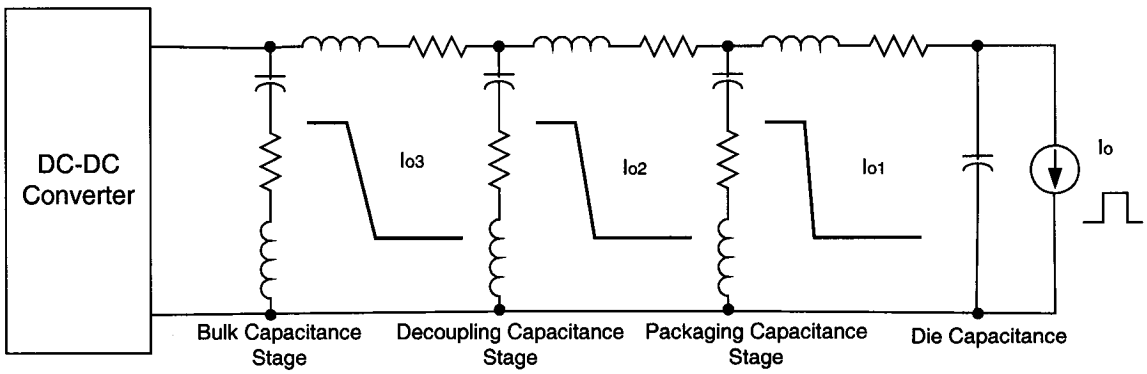


Figure 1.1: Simplified General Power Delivery System Model

Low supply voltage deviation during both steady-state and large-magnitude high-slew-rate current transients is essential, and it is usually required to be less than 3 percent which becomes stricter as the supply voltages become lower. This means that lower than 30mV deviation will be required at voltages of about 1V or lower. The deviation can be undershot (lower than the nominal voltage) when there is a low-to-high (step-up) load transient, or can be overshot (higher than the nominal voltage) when there is a high-to-

low (step-down) load transient. Undershot deviation will decrease the logic transistors speed and affect the signal-timing requirements [23], which will cause IC malfunctioning. Overshot deviation will affect the transistor junctions resulting in a transistor junction breakdown and causing IC destruction [23].

Another important specification is the power/current densities required for the converters that are used in ICs for communication devices and processors to reduce the converter size as it is the case for their loads. This imposes another requirement, which is higher efficiency, especially to reduce the heat generated from the losses and prevent thermal problems. Of course, the reduced cost will also keep playing an important role in such designs.

From Table 1.2 and Table 1.3, it can be noticed how low the future required voltages and how high the output supply currents are projected to be. As shown in Table 1.3 of the SIA 2000/2001 roadmap, output voltages are projected to be below 0.6V by year 2010, and below 0.4V by year 2016, all at increased current levels that are breaking the 100 amperes limit.

1.3 Distributed Power Systems and the New Wave of On-Board DC-DC Converters

The strict requirements for powering new generations of ICs cannot be achieved directly from a centralized power supply because of distributed bus parasitics and losses. Therefore, Distributed Power System (DPS) is used to satisfy these requirements by using On-Board DC-DC converter located near the load [4,8,22,23]. Such DPS system block diagram is shown in Figure 1.2.

In recent years, DPS architectures have been extensively used in mainframe computer and communication systems. However, the basic concepts and design philosophies can be tailored for developing future computer system power supplies.

The off-board silver box is still kept to interface with the utility. An internal DC bus generally can be found in the bulk power supplies. The functions of this bulk power supply are to generate proper bus voltage for the on-board converters and to directly support some regular loads where the specs are relatively looser. To comply with the present standards, some low power level, low-cost AC-DC converters with power factor correction (PFC) and electrical isolation can be considered as options [32-39]. Normally, the on-board converter should be placed close to or packaged on the units that need strict regulated supplies to minimize the effects of parasitic parameters. If the load is far from its supply, the distribution wire or trace impedance will delay the ability to deliver the transient load current, forcing the supply voltage to deviate outside its upper or lower limits, and will result in large distribution losses especially at high currents. Hence, on-board converters take advantage of their closeness to their loads.

Another reason of adapting the DPS architectures is to realize modular open-architecture systems, which require modular distributed power supplies for applications such as hubs, routers and signal and data processing in general [22]. Improved reliability and redundancy are also advantages of DPS architectures [22].

Several names are used for the on-board DC-DC converters, usually indicating the application it is used for. In communications applications for example, they are usually called Point-Of-Load (POL) converters, while Voltage-Regulator-Modules (VRMs) name is used in computers' microprocessor applications.

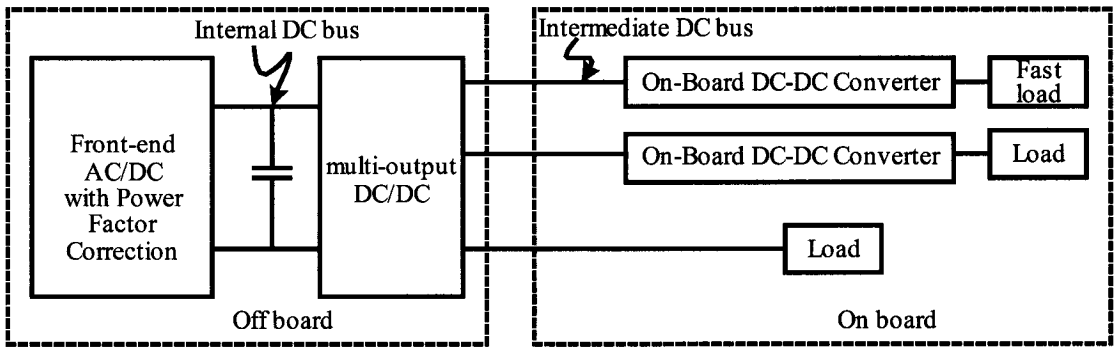


Figure 1.2: Example of Distributed Power System (DPS) Architecture Block Diagram

The on-board DC-DC converters can be isolated or non-isolated depending on the application they are used for. Isolated converters have an isolation transformer that is used to help in stepping the voltage down from its primary-side to its secondary-side, in addition to the electrical isolation it provides. Such isolated converters are usually used in communication system applications that, for example, have an input voltage range of 36V~75V (48V nominal). They are usually referred to as POL converters in such applications and they are such as symmetrical and asymmetrical half-bridge, full-bridge, active clamped forward, flyback forward and push-pull [4,7,40-52]. The secondary side of the isolated topology can have different schemes such as forward, center-tapped or current-doubler as discussed in [4]. Non-isolated converters have no isolation transformer and they are usually buck topology derived [4,6,7,10,15,53-56]. Such converters are used in computer's VRM applications with an input voltage range of 5V ~ 12V. However, future VRMs may be isolated and non-isolated.

Moreover, DC-DC converters can be hard-switched or soft-switched [51,52,56-61]. The idea behind the concept of soft-switching is to shape the voltage or the current

waveform by creating a resonant condition to force the voltage across the switching device to drop to zero before turning it ON or to force the current through the switching device to drop to zero before turning it OFF. By doing this, a Zero-Voltage Switching (ZVS) or a Zero Current Switching (ZCS) can be achieved. While in hard-switching, non of the both parameters, i.e., the voltage cross and the current through the switch, are zero, causing power losses during switching ON and OFF, i.e., switching losses. These switching losses become more significant as the switching frequency increases.

1.4 Driving Market Applications and Research Driving Forces

On-board converter applications include any IC that needs special powering requirements in terms of voltage, current, current slew rate, voltage deviation, etc. Such applications, which were discussed earlier in this chapter and are summarized here, include:

1. New generation of microprocessors.
2. Communication systems and equipment.
3. High-speed Integrated Circuits (ICs) especially those used in consumer electronics and hand-held electronic devices.

Moreover, as a summary, the future on-board DC-DC converters main design and research driving forces include:

1. Lower voltages.
2. Higher currents.

3. Faster transient response to high load current slew rates with larger magnitudes.
4. Lower output voltage deviation.
5. Higher power/current density (smaller size).
6. Higher efficiency and better thermal management with no heatsink.
7. Improved Electromagnetic Compatibility (EMC) and reliability.
8. Lower cost.

1.5 Dissertation Outlines

The next chapter briefly discuses the steady-state and transient analysis and design equations of low-voltage, high-current, fast-transient DC-DC on-board DC-DC converters. Chapter 3 presents an interleaved (multiphase) parallel-connected converters control method for a multiphase voltage-mode hysteretic controlled VRM with current sharing technique. Chapter 4 reviews some common isolated topologies and presents a control method for the half-bridge DC-DC converter, namely, Duty-Cycle-Shifted (DCS) control. Chapter 5 presents a control method for half-bridge topology, to be called Alternated Duty Cycle (ADC) control. Chapter 6 presents an interleaving method for isolated topologies where the secondary side switches operate at lower switching frequency than the primary side switches to improve the efficiency and the transient response. Meanwhile, both primary and secondary sides of the isolation transformers are connected in parallel allowing sharing of currents at both primary and secondary sides. Chapter 7 presents a Coupled-Inductors Current-Doubler (CICD) topology. Chapter 8 presents a non-isolated Half-Bridge-Buck (HBB) topology. In Chapter 9, a brief review comparison between major control methods will be provided, followed by a presentation

for initial work on a control method concept and technique. Chapter 10 discusses digital control as a candidate for future DC-DC converters and presents digital system structure, advantages, disadvantages and initial experimental setup. Moreover, an initial concept for future work on digital control is presented, namely, the Maximum Efficiency Point Tracking (MEPT) method, which can be used to optimize the switch's dead time control issue by using adaptive control to achieve better efficiency and converter performance. Finally, Chapter 11 summarizes this work and presents future research directions.

CHAPTER 2

DESIGN AND ANALYSIS OF ON-BOARD DC-DC CONVERTERS

2.1 Introduction

As mentioned in the previous chapter, the on-board DC-DC converters can be isolated and non-isolated. The non-isolated buck topology is the simplest DC-DC topology and the most common used, especially nowadays in VRM applications where the input voltage is 5V or 12V. Studying the behavior and analysis of buck topology at both steady-state and transient conditions is usually sufficient to understand and to have a general feeling about isolated and non-isolated topologies, especially that most of the isolated and non-isolated DC-DC topologies are either buck derived, behave like buck topology, and/or can be equivalently transformed to buck topology format.

In this chapter, steady-state and transient analysis and design equations will be presented for a better understanding of the parameters' effect on such low-voltage, high-current, fast-transient DC-DC on-board DC-DC converters including parasitics. Non-isolated buck topology is used as example.

2.2 Ideal DC-DC Buck Topology

Figure 2.1(a) shows the ideal buck DC-DC converter used along with the main switching waveforms shown in Figure 2.1(b) and 2.1(c) for different types of operation.

In the conventional buck topology, the upper-side switch S_1 is a MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor), while the low-side switch S_2 is a diode. However, the low-side switch is replaced by a MOSFET in low-voltage, high-current applications because the current available MOSFETS have lower ON-state resistance to reduce the conduction loss. At this case, when both S_1 and S_2 are MOSFETS, the topology is called Synchronous Buck and S_1 and S_2 are called Synchronous Rectifiers (SRs).

In the conventional buck topology, where S_2 is a diode, depending on the value of the output inductor L_o as will be shown later, the converter may operate in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) as shown in Figure 2.1(b). When the inductor value is smaller than a certain limit, the inductor current will discharge quickly when S_2 is ON, before turning ON S_1 to start charging up., and since the diode can conduct in one direction, a discontinuity will occur when the inductor current drops to zero and goes negative, then DCM mode occurs. When L_o value is large enough, the current will be always larger than zero and the converter will operate in CCM.

However, when SRs are used for both buck topology switches, there is no real DCM mode since the MOSFET body-diode will carry the inductor current when it goes

negative, resulting in what is called the Quasi-Square-Wave (QSW) buck topology as in [7].

In the QSW buck converter, a dead time delay is designed between the control signals of the two switches as shown in Figure 2.1(c). This delay results in both switches having soft-switching operation. Note that the body diode of the high-side switch is ON in the first delay period after turning S_2 OFF, while the body diode of the low-side switch is ON in the second delay period after turning S_1 OFF. As discussed in [7], faster transient response is achieved using QSW buck, since the used output inductor value is smaller. However, this causes the converter to have higher output current ripple and lower efficiency compared to the synchronous buck operating in CCM mode.

2.3 Basic Design Equations and Considerations

The design of a low-output-voltage converter requires detailed knowledge and understanding of the system as well as careful selection of the design parameters such as the output inductor, the output capacitor and the switching frequency.

In this section, steady-state and transient equations and considerations are discussed, taking the buck topology as an example, since this topology behavior represents most or all of the topologies used for this application, as mentioned earlier in this chapter. Some basic equations, assuming ideal components, are as follows:

1. Rate of the output inductor current change during step-up transient:

$$\frac{di_{L_o}}{dt} \approx \frac{V_{in} - V_o}{L_o} \tag{2.3.1}$$

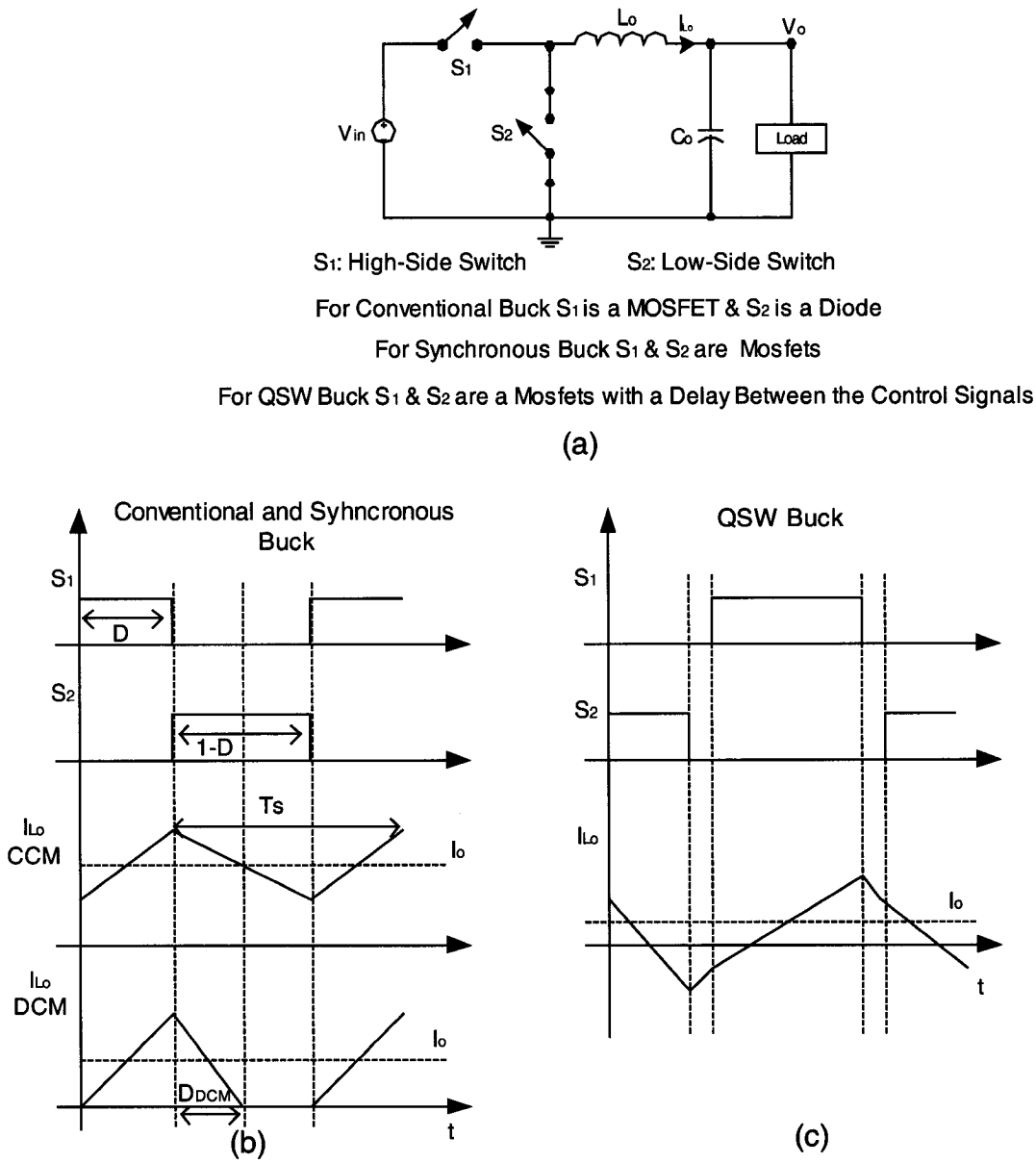


Figure 2.1: (a) Ideal Buck topology, (b) Switches Drive and Output Inductor Current Waveforms for CCM and DCM Operations and (c) Switches Drive and Output Inductor Current Waveforms for QSW Buck

where:

$\frac{di_{L_o}}{dt}$ is the output inductor current rate of change (A/s).

V_{in} is the average input voltage (V).

V_o is the average output voltage (V).

L_o is the output inductor value (H).

2. Rate of the output inductor current change during step-down transient:

$$\frac{di_{L_o}}{dt} \approx \frac{-V_o}{L_o} \tag{2.3.2}$$

3. Output Voltage Gain/Current Gain:

$$D \approx \frac{V_o}{V_{in}} = \frac{I_{in}}{I_o} \tag{2.3.3}$$

where:

D is the switching duty ratio or duty cycle.

I_{in} is the average input current.

I_o is the average output current.

4. The critical (must be larger than this value) output inductor value to operate in CCM:

$$L_{o,crit.} \approx \frac{V_o \max(D, 1-D)}{2 I_o f_s} \tag{2.3.4}$$

where: I_o is the output load current.

5. Output current ripple (inductor current ripple):

$$\Delta I_{Lo,ripple} \approx \frac{V_o \max(D,1-D)}{L_o f_s} \tag{2.3.5}$$

where: $\Delta I_{Lo,ripple}$ is the output inductor current ripple (A).

6. Output ripple voltage:

$$\Delta V_o \approx \frac{V_o \max(D,1-D)}{8 L_o C_o f_s^2} \tag{2.3.6}$$

where: C_o is the output capacitance.

7. Critical output capacitor value required to satisfy the required output voltage deviation ΔV_o during the transient from [7] assuming ideal power stage and control:

$$C_{o,crit.} \geq \frac{1}{2}\frac{\Delta I_o}{\Delta V_o}\left(\frac{L_o}{V_o} - \frac{1}{di_o/dt}\right) \tag{2.3.7}$$

where:

ΔI_o is the maximum load current transient magnitude.

$\frac{di_o}{dt}$ is the output load current slew rate.

8. Critical input capacitor value required to satisfy the required input current slew rate [7]:

$$C_{in,crit.} \geq \frac{1}{2} \frac{P_o^{\,2}}{\left(di_{in}/dt\right)(\Delta V_{in})(V_{in})^2} \tag{2.3.8}$$

where:

P_o is the output power.

$\frac{di_{in}}{dt}$ is the input current slew rate.

As mentioned before, one of the strict requirements of the POL and VRM on-board DC-DC converters is the fast transient response at a very high output current slew rate. This requires that the output inductor L_o to be is designed as small as possible, as noted from Equations (2.3.1), (2.3.2) and (2.3.7), at both step-up and step-down transients, assuming that the closed loop controller has sufficient bandwidth (fast enough).

Unfortunately, using small L_o to achieve faster transient response will cause the output voltage ripple to increase as shown in Equation (2.3.5) and will push the converter operation towered the DCM mode as in Equation (2.3.4), leading to lower efficiency because of increased conduction losses caused by the increased *rms* (root-mean-square) current value. Therefore, lower L_o will require the switching frequency to be increased.

Here, the trade off with efficiency comes out to the picture. The higher the switching frequency, the lower the efficiency is, since the switching devices have higher switching losses as the switching frequency is increased. Therefore, the selection of the switching devices and the advancement made in switching devices technology are very important. Increasing the switching frequency will improve the transient response, and

the compensated control loop bandwidth can be increased and also will reduce the output voltage ripple.

Another way to decrease the output voltage ripple is to increase the converter output capacitor (C_o) as in Equation (2.3.6). However, this capacitor will be very large, especially for future requirements, which is not preferred in the practical designs especially for the VRM and POL applications where the space is limited.

In practical designs, the loop gain crossover frequency is usually selected to be less or in the range of $0.15f_s \sim 0.3f_s$. Therefore, the higher the switching frequency, the faster the closed loop, the smaller the required value of C_o to keep the output voltage ripple within the required limits and the smaller $L_{o,crit.}$ required to operate in CCM to achieve less output current ripple.

Another conclusion that can be drawn from Equations (2.3.1) and (2.3.2) is that in low voltage output converters, the inductor current slew rate during step-down transients is much lower than it is for step-up transients since the voltage across the inductor is much lower (V_o compared to $V_{in} - V_o$), causing the voltage deviation during step-down transients to be larger than it is during step-up transients, resulting in asymmetric transients responses, that becomes more sever as the output voltage becomes smaller.

Another requirement is the high converter input current slew rate, which requires a large converter input capacitor (C_{in}) to be used. From Equation (2.3.8), it can be noted that in order to decrease the size of C_{in}, the input voltage, V_{in}, must be increased. This means that a DPS with high-voltage bus will require lower C_{in}, which is an advantage for the isolated converters over the non-isolated ones. Another advantage of isolated

converters is that an isolation transformer can be used to step-down the voltage, resulting in a larger duty cycle as compared to the non-isolated converters. In non-isolated converters, the duty cycle becomes smaller as the output voltage becomes smaller as given by Equation (2.3.3). The smaller the duty cycle, the larger the input peak current, which increases the conduction losses because the *rms* current value increase and the more asymmetric the transient response is.

It must be noted that high power density is an important requirement and must be taken into consideration during the design, which place a restriction on the component value selection such as C_o and C_{in} and on the topology selection.

As can be seen from the above analysis, the design of POL and VRM encounters many requirements and restrictions, all of which need to be taken into consideration.

2.4 Load Transients and Converter Response

As mentioned before, on-board converters loads, such as microprocessors, can switch from one load level (output current) to another with large magnitude and at fast transient slew rate. These load transients cause large converter output voltage deviation. Since the converter's output voltage is small, this voltage deviation percentage can be large and unacceptable. Current levels are also too high and small component's resistances can cause large I^2R power losses. Moreover, the converter, its component, and closed-loop control cannot be considered ideal anymore.

Figure 2.2 shows a buck converter with main component parasitics consideration, where:

R_{on} is the MOSFET ON-state resistance (Ω).

DCR is the output inductor equivalent DC Resistance (Ω).

ESR is the Equivalent Series Resistance of the output capacitors (Ω).

ESL is the Equivalent Series Inductance of the output capacitors (H).

t_{delay} is the total closed loop controller delay time until the appropriate switch is turned ON or OFF (s).

V_{sense} and I_{sense} are the voltage(s) and current(s) sensed signals for control and protection.

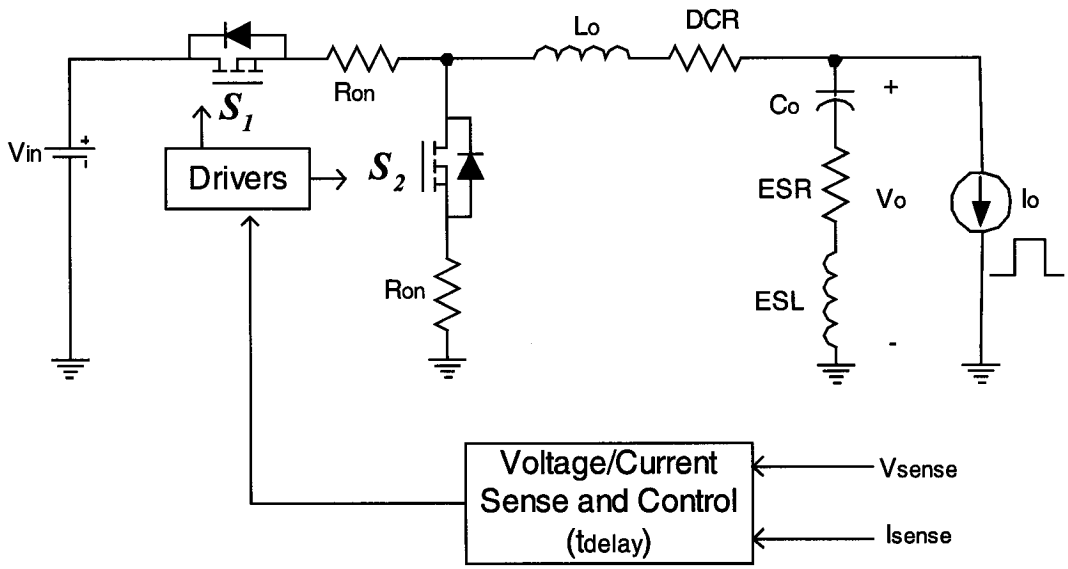


Figure 2.2: Buck Converter with Main Components Parasitics Consideration

Because of the ESR and ESL of the output capacitance, the output voltage is given by:

$$v_o(t) = v_{C_o}(t) + v_{ESR}(t) + v_{ESL}(t) \tag{2.4.1}$$

Equation (2.4.1) should be considered especially for transient analysis since the average voltages drop across the ESR and the ESL are not zero during transients.

Figure 2.3 shows a load step-up transient output current and voltage waveforms as an example. The output current switches up by $\Delta I_o = I_a - I_b, I_b > I_a$ magnitudes during Δt_{trans} time causing output voltage deviation ΔV_o.

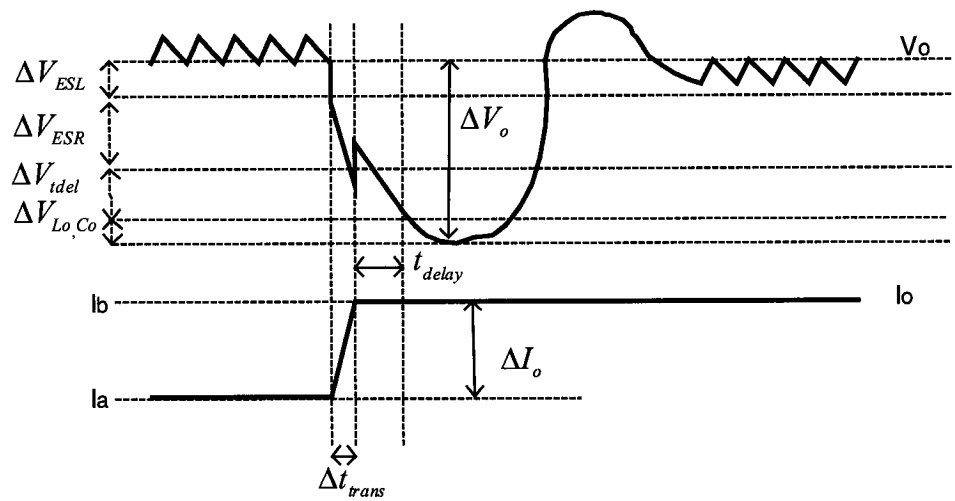


Figure 2.3: Example of Step-Up Load Transient Output Current and Voltage Waveforms

From Figure 2.3, the output voltage transient response waveform can be divided into four transitions or parts before it settles back to its nominal value, as follows:

1. The ESL voltage transition ΔV_{ESL}:

This voltage drop across the output capacitor ESL occurs because of the output load current rate of change and is given by:

$$\Delta V_{ESL} \approx ESL \cdot \frac{di_o}{dt_{trans}} = ESL \cdot \frac{\Delta I_o}{\Delta t_{trans}} \qquad (2.4.2)$$

Equation (2.4.2) shows that this voltage increases as the output current slew rate and magnitude increase, and of course it increases as the ESL value increases. This fast, high-frequency voltage spike usually can be ignored, since it will be filtered out by the high frequency decoupling capacitors before the load.

2. The ESR voltage transition ΔV_{ESR}:

This is the second transition that occurs because of the ESR instantaneous resistive voltage drop and is given by:

$$\Delta V_{ESR} = ESR \cdot \Delta I_o \tag{2.4.3}$$

Equation (2.4.3) shows that this voltage is directly proportional to the ESR value and the transient current magnitude. This voltage deviation part is important and cannot be ignored.

3. The closed loop control delay transition voltage: ΔV_{tdel}

This voltage is caused by the closed loop control delay time, which is the total delay time because of the controller bandwidth delay and control logic component delays until the time when the appropriate switch is turned ON or OFF. This voltage is proportional to parameters including the total loop delays time t_{delay}, the load current step magnitude ΔI_o and the output filter characteristics L_o/C_o.

t_{delay} is a function of the switching frequency, controller bandwidth and controller and drivers logic speed. Larger controller bandwidth, which means smaller t_{delay}, will result in smaller ΔV_{tdel}. The other option to reduce ΔV_{tdel} is to increase C_o, which is not a practical solution because of the space limitations, cost and the amount of C_o to be used are usually restricted to a certain maximum amount for each application.

4. The power stage output filter transition voltage $\Delta V_{Lo,Co}$:

This voltage deviation is mainly a function of the power stage output filter consisting of L_o and C_o. It is directly proportional to L_o and inversely proportional to C_o, which means either smaller L_o or/and larger C_o will result in smaller deviation. This deviation is also directly proportional to ΔI_o^2 and inversely proportional to the voltage across L_o.

If the converter were open loop, this voltage deviation will be equal to the multiplication of the current magnitude change by the output filter characteristics impedance as follows [27]:

$$\Delta V_{Lo,Co,OL} = \Delta I_o \cdot Z_o = \Delta I_o \cdot \sqrt{\frac{L_o}{C_o}} \tag{2.4.4}$$

Assuming ideal components and neglecting the current and voltage ripples, it can be shown that the maximum output voltage $\Delta V_{Lo,Co}$ deviations at both step-down and step-up load transients are given by [27]:

$$\Delta V_{Lo,Co} = \frac{L_o}{C_o} \cdot \frac{\Delta I_o^{\,2}}{2V_{Lo}} \tag{2.4.5}$$

Where: V_{Lo} is the voltage across the output inductor L_o, and it is ideally equal to $V_{in} - V_o$ at load step-up transients and equal to $-V_o$ at load step-down transients.

From equation (2.4.5), it is evident that reducing the ratio L_o/C_o will result in lower $\Delta V_{Lo,Co}$. However, the second transition $\Delta V_{ESR} = ESR \cdot \Delta I_o$ is still there and has to be

considered. Reducing the L_o/C_o ratio by deceasing L_o, for example, will lower $\Delta V_{Lo,Co}$ at the expense of increasing the current ripple and lowering the efficiency, and it may not lower ΔV_{ESR}. Therefore, there is a minimum critical ratio $(L_o/C_o)_{crit.}$ where ΔV_{ESR} is equal and starts to be larger than $\Delta V_{Lo,Co}$. This is given by:

$$\left[\frac{L_o}{C_o}\right]_{crit.} = \frac{ESR \cdot V_{Lo}}{\Delta I_o} \tag{2.4.6}$$

The critical ratio from Equation (2.4.6) is smaller, which means smaller L_o or/and larger C_o is required, as ΔI_o is getting larger. This means that the larger transient current magnitude change will strongly affect future designs. For $L_o/C_o < (L_o/C_o)_{crit.}$, the voltage deviation will not be reduced further, while the current ripple will increase and the efficiency will decrease, resulting in bad design. Hence, L_o/C_o should be selected to be equal, as much as possible, to $(L_o/C_o)_{crit.}$. This behavior can be described as shown in Figure 2.4.

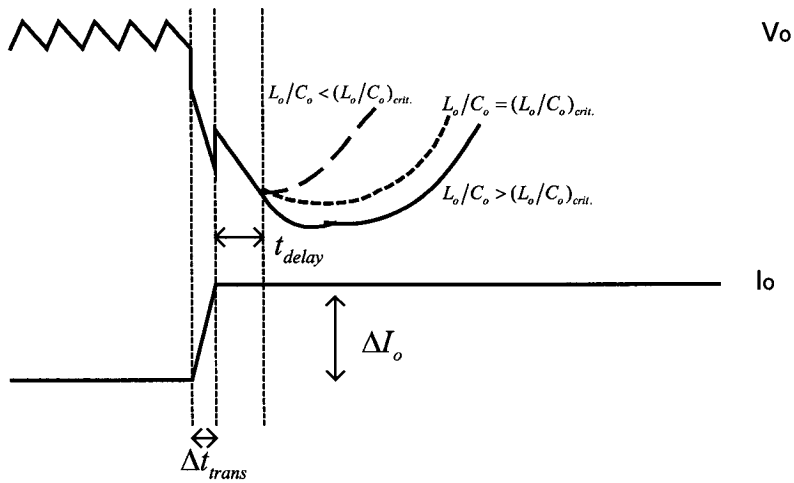


Figure 2.4: Example of Step-Up Load Transient Output Current and Voltage Waveforms at Different L_o/C_o Ratios

CHAPTER 3

MULTIPHASE VOLTAGE-MODE HYSTERETIC CONTROLLED DC-DC CONVERTER WITH CURRENT SHARING

3.1 Introduction

In this chapter, the interleaved (multiphase) parallel-connected converters method will be reviewed, followed by a presentation for a multiphase voltage-mode hysteretic controlled VRM with new current sharing [28,30,54]. Detailed theoretical analysis is provided and supported by simulation and experimental results for a specific design example.

3.2 Interleaving Versus High Switching Frequency and Smaller Output Inductor

A way to reduce the output current and voltage ripples and to improve the transient response is to increase the switching frequency. Unfortunately, increasing the switching frequency will lower the converter's efficiency. Another way to reduce the output current and voltage ripples is to decrease the output inductor value, which unfortunately will result in slower transient response.

Here it comes the interleaving or multiphase technique [7,28,30,54,59,60]. This technique is implemented by paralleling several out-of-phase driven modules, as shown

in Figure 3.1 as an example for the synchronous buck topology with four phases. Figure 3.2 shows main waveforms of Figure 3.1.

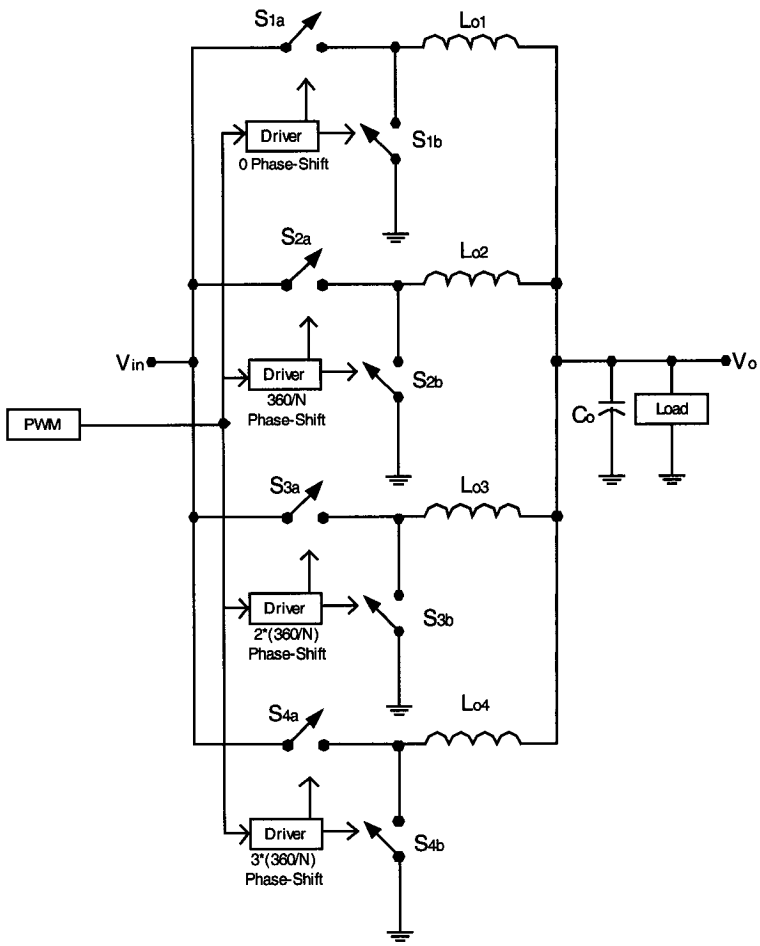


Figure 3.1: Four Interleaved (Multi-Phase) Synchronous Buck Converters

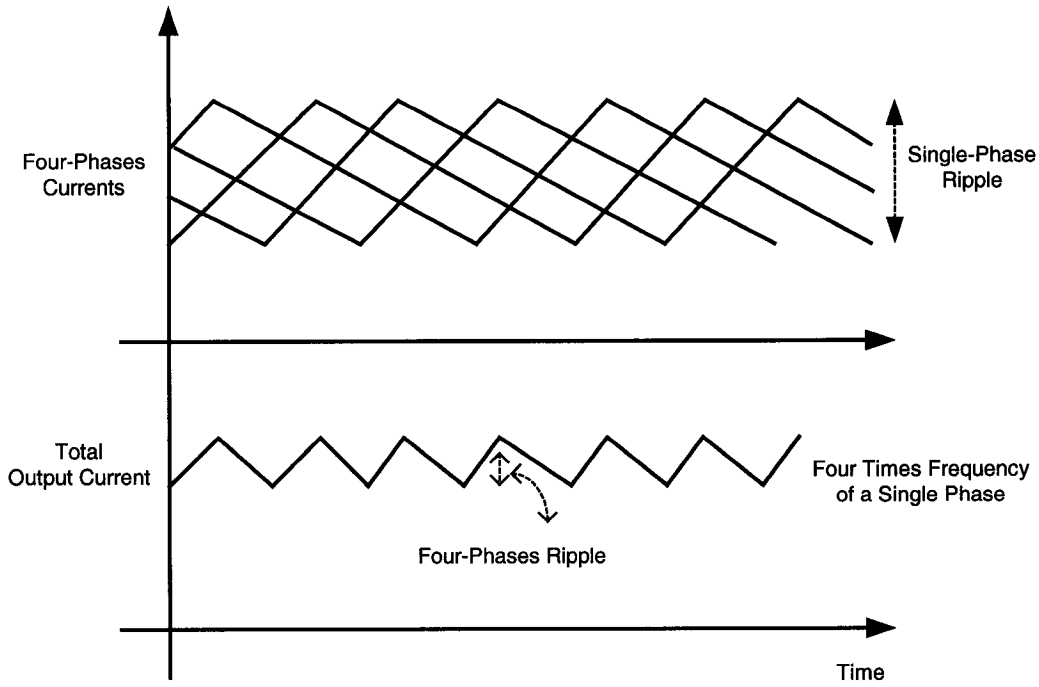


Figure 3.2: Main Waveforms for Four Interleaved Buck Converters (90° Phase Shift Between the Phases)

The phase shift between the phases is $360^{O}/N$, where N is the number of the interleaved modules and the phase switch duty cycle is a function of the V_o/V_{in} ratio. The effective output inductor will be reduced as a result of paralleling. The effective output inductor, assuming all output inductors are equal with a value L_o, is given by:

$$L_{o,eff} = \frac{L_o}{N} \tag{3.2.1}$$

From Equation (3.2.1), $L_{o,eff}$ is lower than the output inductor per phase, which results in a faster transient response as provided in Equations (2.3.1) and (2.3.2).

Moreover, the effective output current and ripple frequency $f_{o,ripple}$ is N times the switching frequency of each of the phase shifted modules (f_s). This yields:

$$f_s = \frac{f_{o,ripple}}{N} \tag{3.2.2}$$

Equation (3.2.2) shows that each interleaved phase is switched at lower switching frequency compared to a single-phase (non-interleaved) module for the same output ripple frequency and magnitude. Therefore, higher output ripple frequency can be achieved by interleaving while switching each phase at a lower frequency. This will result in a faster transient response and lower output current and voltage ripples as from Equations (2.3.5) and (2.3.6).

From the above, several design options are available to satisfy certain requirements. For example, to improve the transient response or to decease output ripple, instead of decreasing the inductor or increasing the ripple frequency, the number of phases can be increased. This results in lower effective output inductance and higher output ripple frequency as from Equations (3.2.1) and (3.2.2). However, it must be noted that the output capacitor value must still be able to maintain the maximum allowed output voltage deviation requirements during transients. Another important advantage of the interleaving technique is that the load current is shared (divided) between the interleaved phases.

However, the feedback control loop is still a constraint that limits the speed of the transient response in interleaved converters, especially that the compensated feedback loop bandwidth is usually limited to the range of 20 percent ~ 30 percent of the switching frequency.

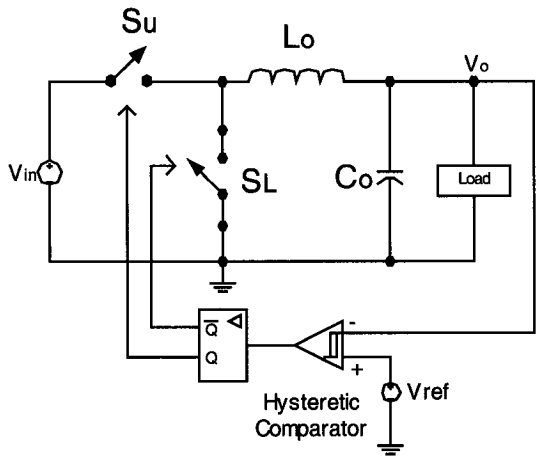
3.3 The Voltage-Mode Hysteretic Control Concept

The Voltage-Mode Hysteretic Control [58,61] is to directly track the output voltage of the converter between an upper limit (V_H) and a lower limit (V_L) around a reference voltage ($V_{ref} = V_o$) to turn ON or OFF the appropriate switches, with no feedback compensation.

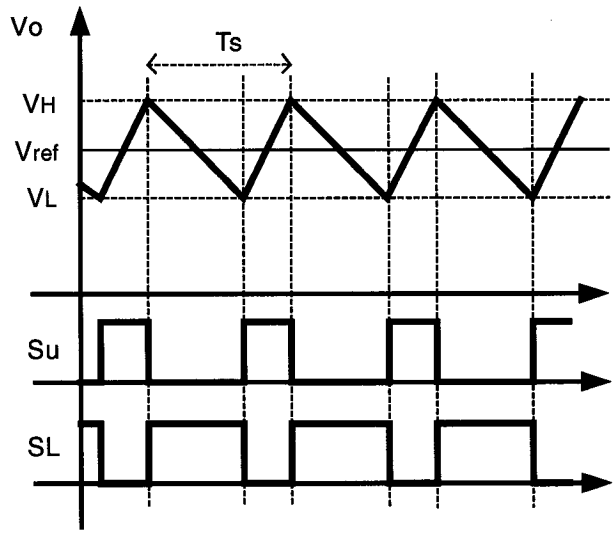
Figure 3.3 shows a simplified schematics and waveforms for a hysteretic controlled buck converter. The controller will turn the high-side switch ON and turn the low-side switch OFF if the output voltage drops bellow V_L, and it will turn the high-side switch OFF and turn the low-side switch ON if the output voltage exceeds V_H, keeping the output voltage regulated around $V_{ref} = V_o$.

The hysteretic controller keeps following the output voltage to produce the required control signals for the switches. If output-current or input-voltage transients occur, the hysteretic controller will keep the appropriate switches ON and OFF until it corrects the output voltage.

The feedback comparator and logic delays cause the actual output voltage waveform to be as illustrated in Figure 3.4. The extra small ripple caused by the delay must be considered in the design.



(a)



(b)

Figure 3.3: A Simplified Schematics and Waveforms for a Voltage-Mode Hysteretic-Controlled Buck Converter

In addition to its advantage of controlling the ripple, the hysteretic control also does not need loop compensation, and the output voltage ripple becomes relatively independent of the output capacitor value. In fact, both the capacitor and the inductor

values can be selected more freely now to satisfy only the transient requirements without taking into consideration the output voltage ripple requirements since the operation of the hysteretic control can take care of it.

Also, the response of this type of controller is fast, since the switches' control signals are derived directly from the output voltage ripple waveform. This allows the controller to respond within one switching cycle.

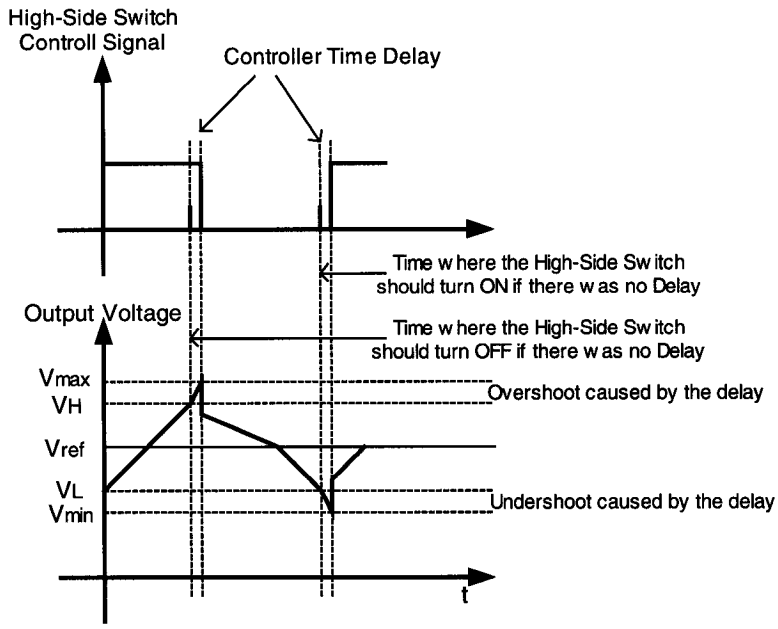


Figure 3.4: Actual Output Voltage Ripple Waveforms for a Voltage-Mode Hysteretic-Controlled Converter

3.4 Multiphase Voltage-Mode Hysteretic Controlled DC-DC Converter with Current Sharing

Both the interleaving (multiphase) and the single-phase voltage-mode hysteretic control techniques can reduce the output voltage ripple. However, the overshoot and

undershoot requirements during large magnitude transients still have to be investigated. It is known that to obtain low output overshoot, the multiphase on-board converters require a design of high-performance feedback control that can also provide current sharing [7, 59,60]. Hence, even though the interleaving technique reduces the output voltage ripple and helps in achieving faster current transient response, a careful control design and/or increase in the output capacitance size will be needed to satisfy the maximum overshoot and undershoot limits during large load transients.

In the single-phase hysteretic voltage-mode control technique, the hysteretic window can be set to a certain level such that the controller will respond quickly to load transients and will correct the voltage before deviating from the maximum allowed overshoot and undershoot. Even though the output capacitor size still plays an important role here, its size is reduced significantly because of the hysteretic window.

On one hand, voltage-mode hysteretic control has many advantages over several other control techniques including simplicity, no feedback loop compensation is needed, near instantaneous response to load transients and no limitations on the switches' conduction time. On the other hand, the interleave technique has several advantages such as the high frequency output voltage ripple with lower switching frequency, ripple cancellation, current division (sharing) between the phases, which allows higher current carrying capability, and also fast transient response which is limited by the feedback control loop. From this summary of advantages, it is clear that combining the voltage-mode hysteretic control technique with the interleave technique will result in a VRM that has the advantages of both techniques [28,30,54].

However, multiphase converters are required to have high-performance current-sharing functionality in order to keep an almost equal division of the load current between the phases at all load conditions in addition to the voltage regulation [4,7,28,30, 54,59,60].

A multiphase voltage-mode hysteretic-controlled DC-DC converter with current sharing is presented with theoretical and experimental verification. In the next section, the multiphase voltage-mode hysteretic control method will be discussed. Section 3.6 presents the concept of the proposed current sharing method and how it is applied to a two-phase interleaved voltage-mode hysteretic controlled DC-DC converter. In Section 3.7, the proposed method will be generalized for N interleaved phases. The theoretical analysis with key design equations is discussed in Section 3.8. The simulation and experimental results are given in Sections 3.9 and 3.10. Finally, the conclusion is given in Section 3.11.

3.5 Multiphase Voltage-Mode Hysteretic Control

When applying the hysteretic voltage-mode control to interleaved buck converters, one must note that: 1) the derived control signal from the output ripple (hysteretic control) must be frequency divided while keeping the same control-signal ON-time (interleaving) and 2) during transients, multiphase control operation must be disabled so that all the phases' switches will switch ON and OFF at the same time. The first note is to keep the switching frequency low for the same output voltage ripple so that the interleaving can be achieved, whereas, the second note is to achieve faster transient response and synchronization between the phases during transients.

Figure 3.5 shows the basic block diagram of N interleaved synchronous buck phases with voltage-mode hysteretic control, while Figure 3.6 shows an example of control signals for two interleaved phases (N = 2) for illustration purposes. It must be noted that the voltage waveform V_o of Figure 3.6 is true only when the voltage ripples across the output capacitor and its Equivalent Series Inductance (ESL) are zero.

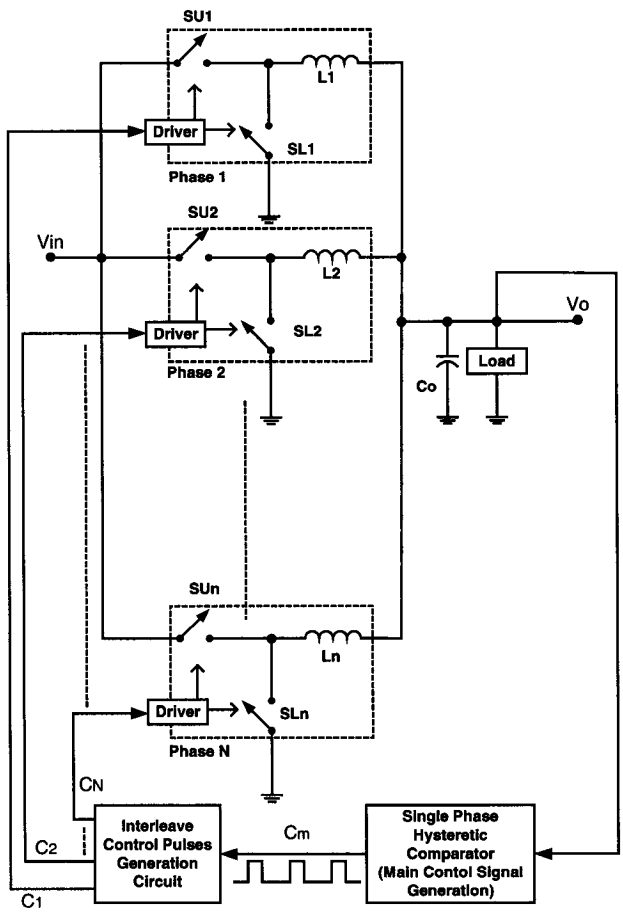


Figure 3.5: Block Diagram of N Interleaved Buck Converters with Voltage-Mode Hysteretic Control

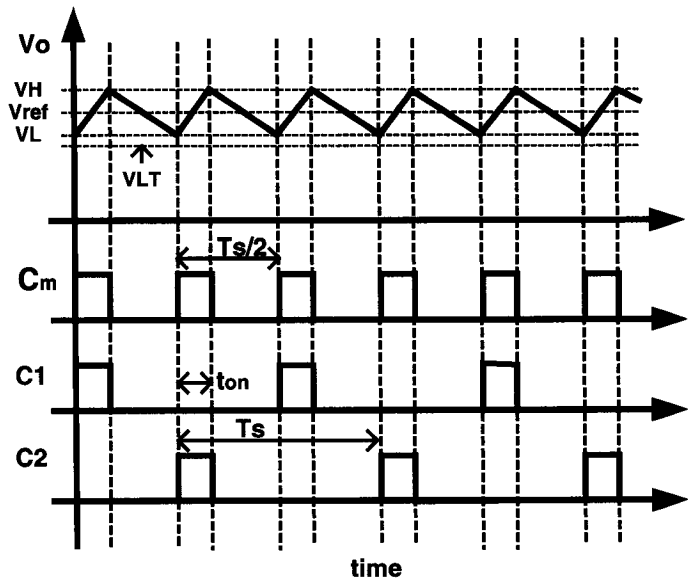


Figure 3.6: Example of Control Signals for Two Interleaved Phases (N=2)

The main control signal (C_m) is generated by comparing the output voltage to a minimum value (V_L) and a maximum value (V_H), forming a hysteretic window. Then, the generated pulses are distributed between the phases interchangeably so that only one phase high-side switch is ON at a time and all the other switches are OFF at that time. This will generate the required multiphase control-signals C_1, C_2, ..., C_N.

At transients, another comparator with threshold of $V_{LT} < V_L$ turns ON all the high-side switches (MOSFETS) and turns OFF all the low-side switches at low-to-high load transients (which cause voltage undershoot). This new threshold (V_{LT}) is added to make the transient response faster and maintain equal current sharing even at transients. Otherwise, if this threshold is not added, only one phase switch will be turned ON at low-to-high load transients when $V_o < V_L$, resulting in slower transient response. However, at

high-to-low load transients (which cause voltage overshoot), all the high-side switches are turned OFF by the hysteretic comparator without the need of another comparator with another threshold larger than V_H.

Figure 3.7 shows how the multiphase control signals can be generated from the main control signal using discrete components for two phases and four phases along with their corresponding waveforms.

3.6 Multiphase Voltage-Mode Hysteretic Control with Current Sharing

It is very important that the current be distributed almost equally between the interleaved phases in the multiphase converter. Unfortunately, components, connections and layout differences from phase, to phase, to the load and other non-idealities may cause the current distribution (sharing) to be unequal, especially at large load transients [7,59]. Hence, current sharing functionality is necessary for the multiphase voltage-mode hysteretic control described in the previous section.

Current sharing between the interleaved converters is usually achieved by controlling the ON-time of each converter phase, such that the ON-time of the phase that carries larger current from the other phases is smaller than the ON-time of the other phases, and the phase that carries the smallest current has the largest ON-time, i.e., the current sharing regulation is performed by shortening (changing) the ON period of the phases' switches [7,59,60]. In this case, the current sharing function is dependent on the control method being used in the voltage regulation. These current sharing methods require some kind of reference to achieve current sharing.

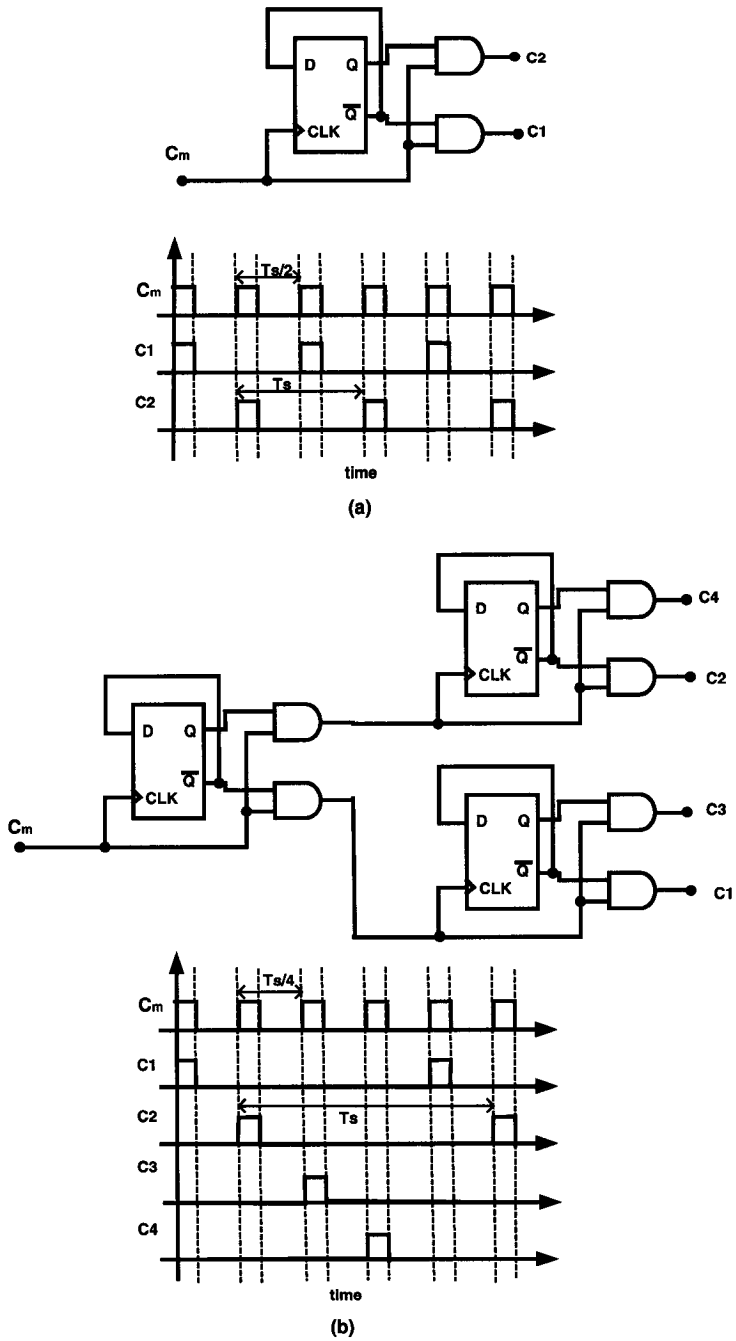


Figure 3.7: Multiphase Logic Circuits to Generate Multiphase Control Signals:

(a) Two Phase and (b) Four Phase

Moreover, the current sharing functionality, in addition to the control loop, adds complexity to the closed loop design (current control loop with compensation is needed). In addition, the ON-time of the switches in the voltage-mode hysteretic control is directly derived from the output voltage ripple by toggling the switches OFF and ON as the output voltage hits the upper and lower limits of the hysteretic comparator (comparator hysteretic window). Hence, changing the ON time of a phase switch means changing the hysteretic window if another switch is not directly turned ON. If another switch is directly turned ON, this may cause several turn ON's within one comparator switching period, causing higher switching frequency for each phase.

Figure 3.8 shows the basic block diagram of the proposed current sharing method. In this method, the instantaneous currents in each phase are sensed (I_1, I_2,..., I_N) and each current is compared relative to the other phases' instantaneous currents generating a comparison digital code (D_1, D_2,..., D_N), without the need for a reference, to find the phase that carries the smallest current. When the main regulation control loop that has no current sharing functionality decides that it is the time to turn a switch ON, the high-side switch in the buck converter, for example, to deliver energy to the converter output, the phase that carries the smallest current at that time will be turned ON by producing a turn ON rising edge signal (C_{Main}), while the other phases are turned OFF by producing the final control signals (C_1, C_2,..., C_N). In simple terms, only one switch will be turned ON at a given time, and this switch will be chosen by monitoring which phase is carrying the smallest instantaneous current at the instant when a switch needed to be turned ON.

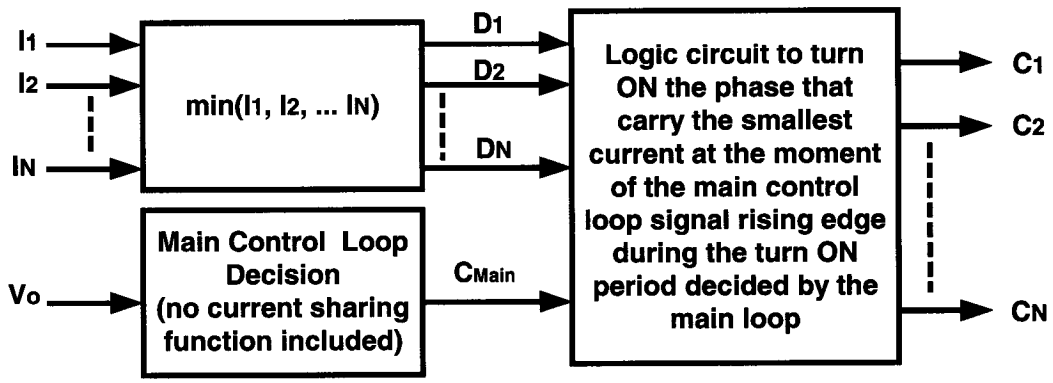


Figure 3.8: Basic Block Diagram of the Proposed Current Sharing Method

It must be noted that even though the instantaneous current in each phase is being compared relative to the other phases continuously, the decision of this comparison is taking effect only at the rising edge of the main control signal C_{Main} and is turning ON the appropriate phase. Hence, the instantaneous point value of each phase current, just before turning ON a phase switch, is the only value that will affect the current sharing process. Figure 3.9 shows the current sharing part for two-phase buck DC-DC converter as an example.

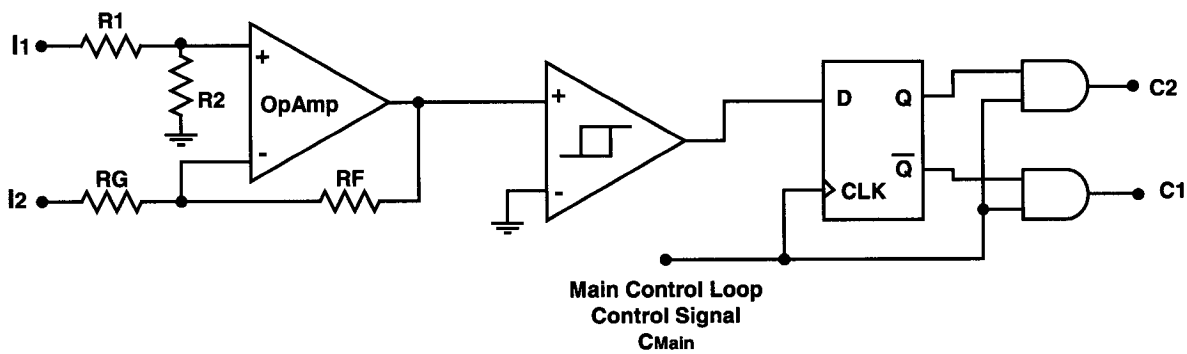


Figure 3.9: Current Sharing Part for Two-Phase Buck DC-DC Converter

The instantaneous currents can be sensed by several methods. For example, it can be sensed by the conventional method directly through the inductors, by placing a small

series resistor with the inductors. Unfortunately, even though this sensing method is simple and relatively accurate, it degrades the efficiency due to the loss in the current sense resistor especially in high current applications. Another way to sense the instantaneous current is to sense the voltage across the low-side switches at the switches junctions. This is possible because: 1) the instantaneous current information for a buck converter is available while the low-side switch is ON and the high-side switch is OFF, 2) the instantaneous current information, just before turning ON one high-side switch, is what is required for the current-sharing process of the presented method and 3) before turning ON one high-side switch, all the low-side switches will be ON and hence the current information is available.

The above proposed current sharing can be applied to the multiphase voltage-mode hysteretic control of the previous section, resulting in a new controller. Figure 3.10 shows the basic controller diagram for the multiphase voltage mode hysteretic controller with the proposed current sharing, while Figure 3.11 illustrates a general waveforms sample for the current sharing process in steady and symmetric condition. The basic operation of the circuit is shown in Figure 3.10, with its related waveforms in Figure 3.11, can be summarized as follows: The main control signal (C_{Main}) is generated by comparing the output voltage to a minimum value (V_L) and a maximum value (V_H) around a reference voltage (V_{ref}) using the hysteretic comparator Comp2. When the time comes to turn ON one high-side switch when the output voltage hits the limit V_L, the rising edge of the turn ON signal of C_{Main}, which is used as a clock for a D-type flip flop cause the current sharing decision of Comp1 to be activated, turning ON the phase that carries the smallest current at that time. Comp3 has a lower limit $V_{LT} < V_L$. This

comparator output is logic zero (low) during the steady state operation when $V_o > V_{LT}$, and is logic one (high) during startup and during the low-to-high load transients when $V_o < V_{LT}$, which causes the phases to switch together (no interleaving) during these transients. This process will generate the require phases' control signals C_1 and C_2 to achieve voltage regulation with current sharing.

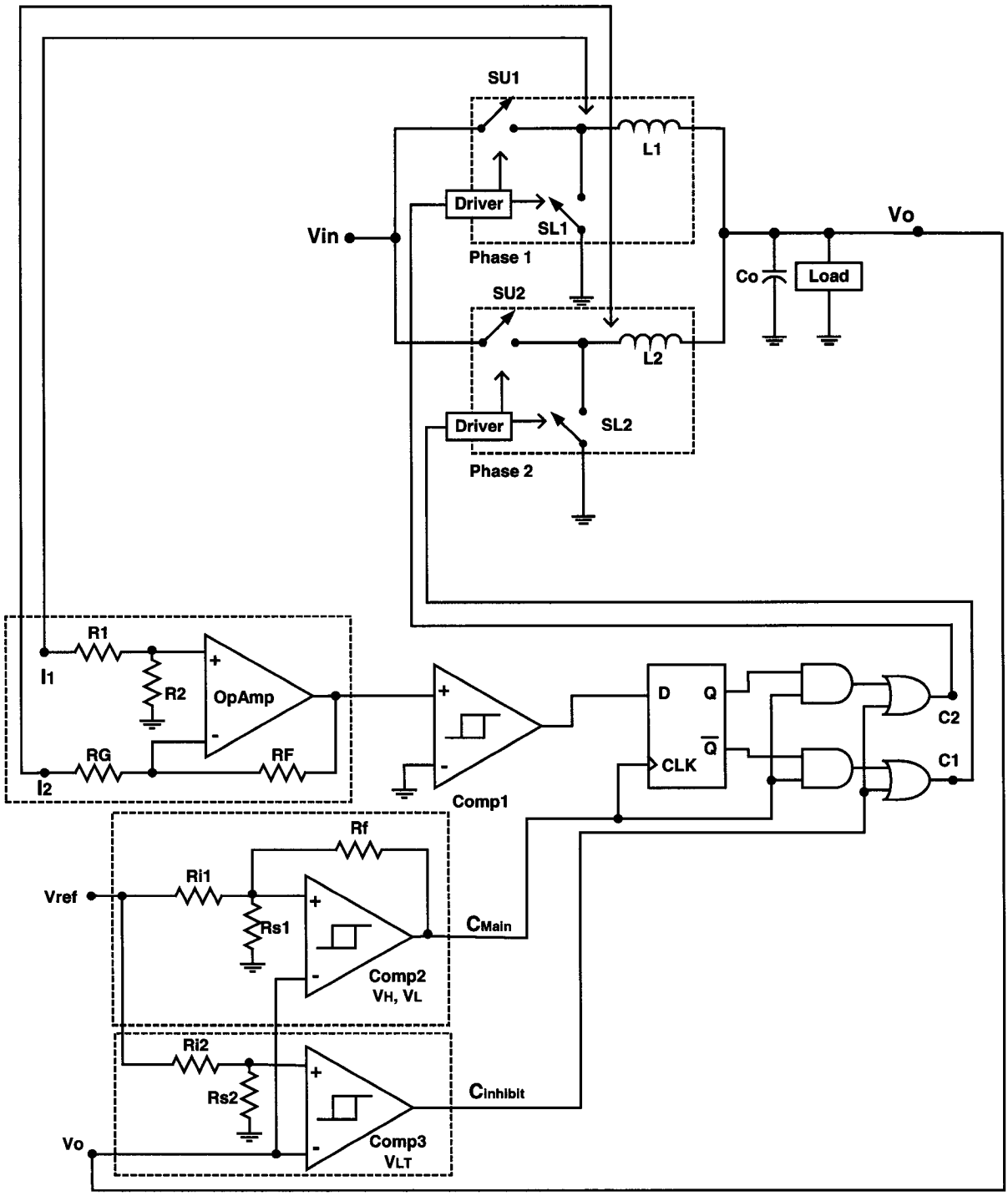


Figure 3.10: Proposed Control Method Applied to a Two-Phase Converter

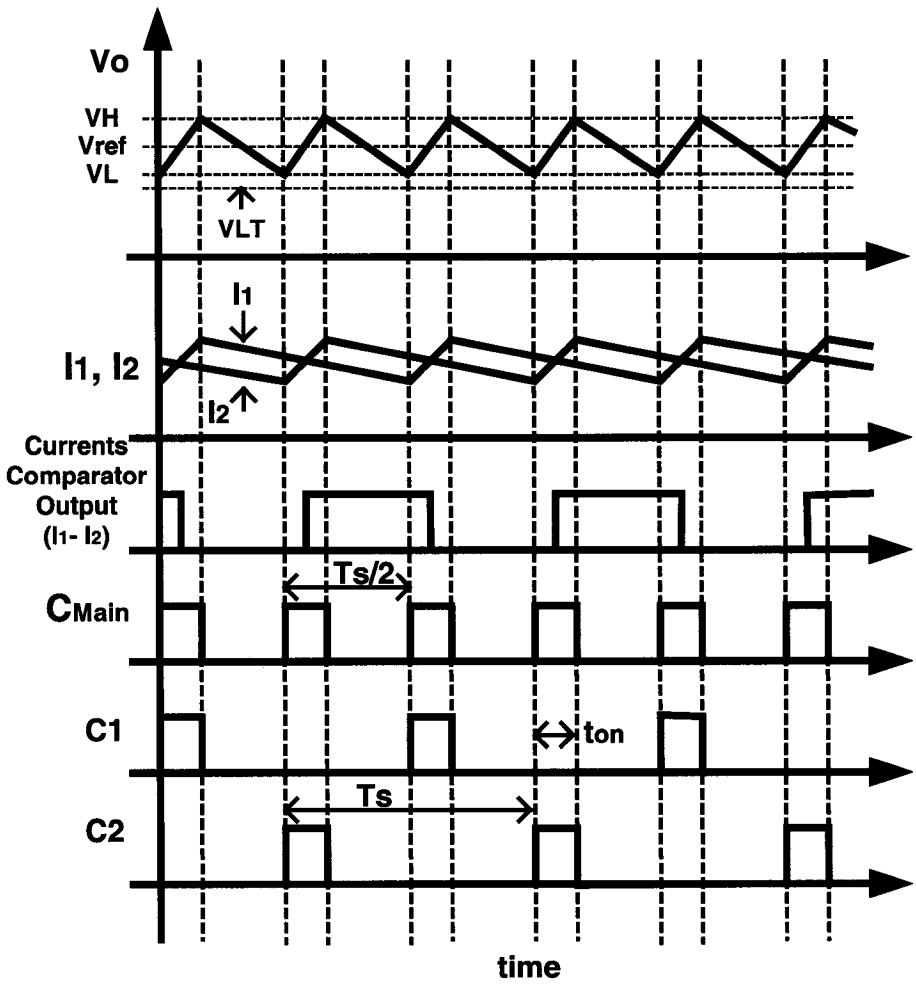


Figure 3.11: General Waveforms Sample for the Current Sharing Process

3.7 Method Generalization for "N" Interleaved Phases

Figure 3.12 shows a basic controller generalized diagram for N multiphase voltage-mode hysteretic controlled current-shared converters. In Figure 3.12, only one of the outputs D_1, D_2,..., D_N of the current comparison circuit can be logic high at a time, causing the phase that carries the smallest instantaneous current to be turned ON at the rising edge of the voltage mode loop as described in the previous section for the two-phase case.

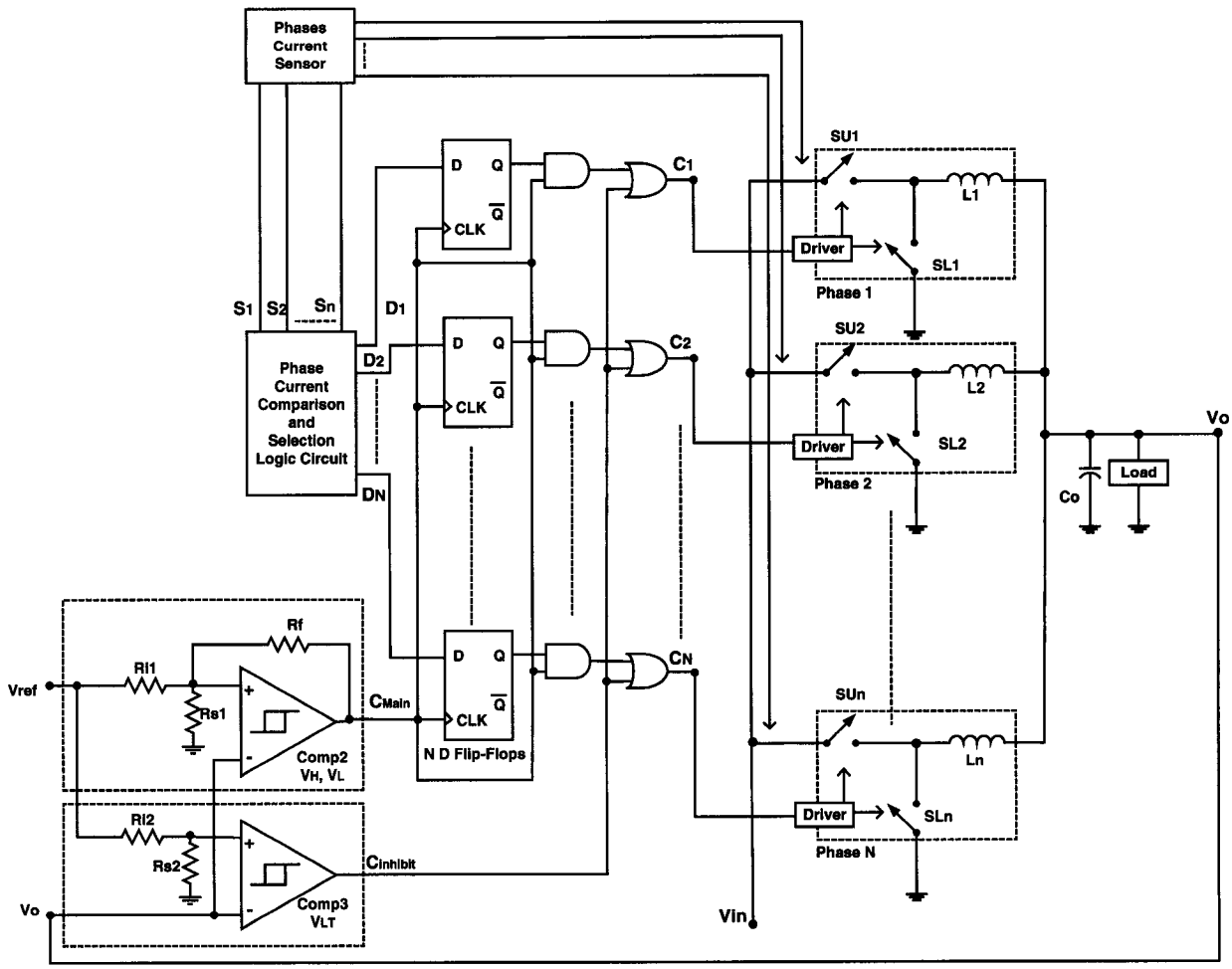


Figure 3.12: Basic Controller Generalized Diagram for N Multiphase Voltage-Mode Hysteretic Controlled Current-Shared Converters

Figure 3.13 shows one possible arrangement for the current sharing circuit by using a set of comparators to find the phase that carries the smallest current for N interleaved phases. The logic circuit after the comparators generate signals D_1, D_2,..., D_N from the comparators' outputs X_1, X_2,..., X_m, so that one of the D-type flip-flops

can be logic high at a time. If this arrangement is to be used, the required number of comparators (m) for N interleaved phases is:

$$m = \frac{N(N-1)}{2} \tag{3.7.1}$$

The circuit shown in Figure 3.13 can use the main control signal input from the voltage loop (C_{Main}) of any type of controller and is not limited to the voltage-mode hysteretic control.

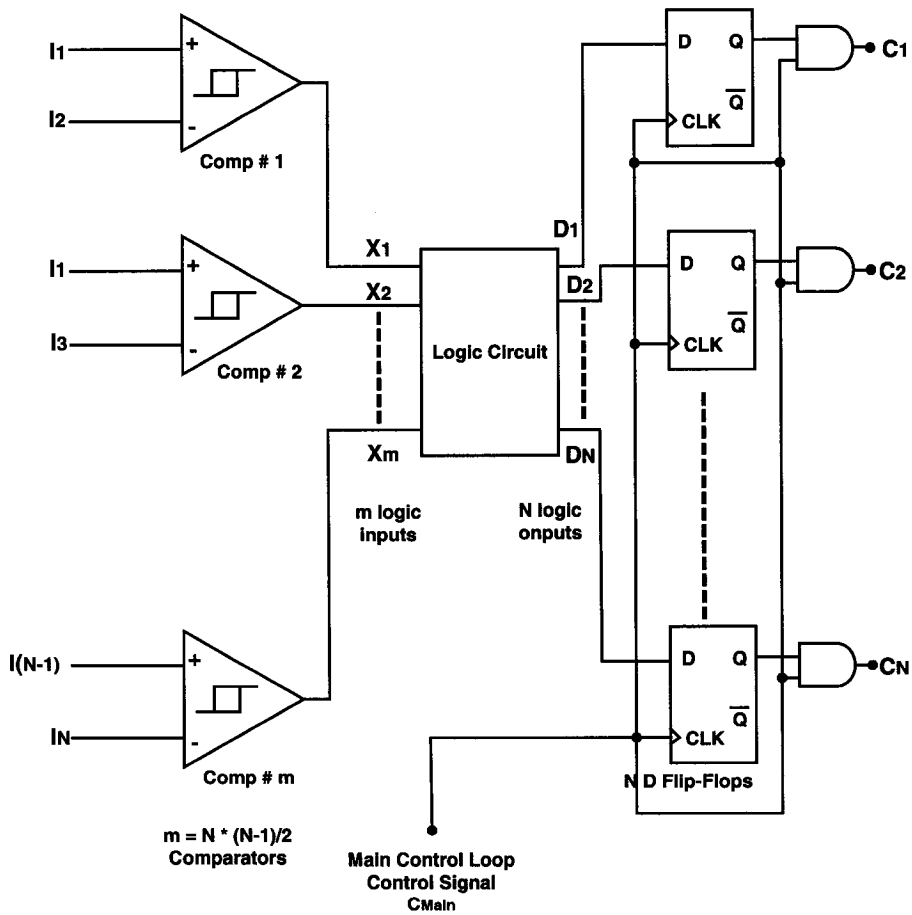


Figure 3.13: Possible Arrangement for Current Sharing Circuit

3.8 Theoretical Analysis

In this section, multiphase voltage-mode hysteretic controlled buck converter is analyzed, and the frequency equation is derived. It is assumed during this analysis, that the converter is operating in steady-state and that all components are ideal except the following non-idealities: the output Capacitor has Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), the switches have ON resistance, and the inductor and its traces also have resistance. In addition, it is assumed that the input voltage is constant with no ripple and the control loop has finite delay time.

Figure 3.14 shows the voltage across the output capacitor in steady-state considering the ESR and the ESL of the output capacitor. In steady-state, the voltage ripple across the output capacitor considering the ESR and the ESL is given by:

$$v_{ripple}(t) = v_C(t) + v_{ESR}(t) + v_{ESL}(t) \tag{3.8.1}$$

where:

$v_{ripple}(t)$: The output voltage ripple across the output capacitor as shown in Figure 3.13.

$v_C(t)$: The voltage across the ideal output capacitor.

$v_{ESR}(t)$: The voltage across the output capacitor ESR.

$v_{ESL}(t)$: The voltage across the output capacitor ESL.

There are two modes of operation in steady state. During Mode 1, when one of the high-side switches is ON, Equation (3.8.1) becomes:

$$v_{ripple\_ON}(t) = \left(\frac{\Delta I_{Lo,ripple} \times t^2}{2 \times C_O \times D \times T_S} - \frac{\Delta I_{Lo,ripple} \times t}{2 \times C_O}\right) + \left(ESR \times \left(\frac{\Delta I_{Lo,ripple} \times t}{D \times T_S} - \frac{\Delta I_{Lo,ripple}}{2}\right)\right) + \left(ESL \times \frac{\Delta I_{Lo,ripple}}{D \times T_S}\right)$$

$$t_0 \le t \le DT_S \quad (3.8.2)$$

During Mode 2 when all high-side switches are OFF, Equation (3.8.1) is given by:

$$v_{ripple\_OFF}(t) = \left(-\frac{\Delta I_{Lo,ripple} \times t^2}{2 \times C_O \times (1-D) \times T_S} + \frac{\Delta I_{Lo,ripple} \times t}{2 \times C_O}\right) + \left(ESR \times \left(\frac{\Delta I_{Lo,ripple}}{2} - \frac{\Delta I_{Lo,ripple} \times t}{(1-D) \times T_S}\right)\right) + \left(-\frac{ESL \times \Delta I_{Lo,ripple}}{(1-D) \times T_S}\right)$$

$$DT_S \le t \le T_S + t_0 \quad (3.8.3)$$

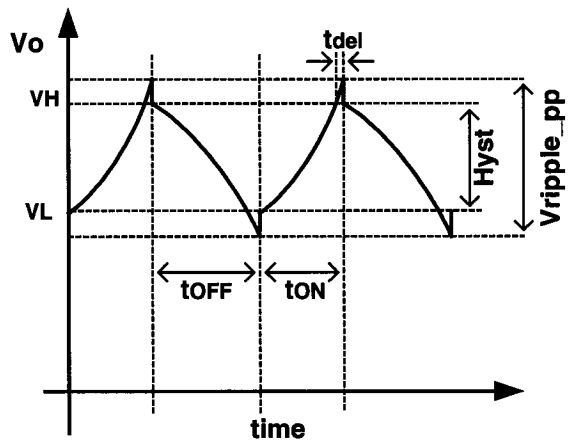


Figure 3.14: Output Voltage with Its Ripple when the Equivalent Series Resistance (ESR), the Equivalent Series Inductance (ESL) and Feedback Loop Delay Time (t_{del}) are Considered

where:

$\Delta I_{Lo,ripple}$: The total inductor(s) ripple for N phases.

T_s : The switching period for N phases.

D: The duty cycle defined as the ratio between the ON time of high-side switch and the switching period T_s.

C_o: The total output capacitance of N phases.

The hysteresis window is then given by:

$$Hyst = v_{ripple\_ON}(t_{ON} - t_{del}) - v_{ripple\_OFF}(t_{OFF} - t_{del}) \tag{3.8.4}$$

where:

$Hyst$: The hysteresis window.

t_{ON} The time duration when one of the high side switches is ON where $t_{ON} = DT_S$.

t_{OFF}: The time duration when all the high-side switches are OFF where $t_{OFF} = (1-D)T_S$.

t_{del}: The total delay time of the feedback loop from time the voltage hits one of the hysteresis window limits until the time the appropriate switches are actually turned ON and OFF.

Equations (3.8.1) through (3.8.4) can be solved to find steady-state output voltage ripple for different topologies after determining the output current ripple $\Delta I_{Lo,ripple}$ for that specific topology. In this case of N interleaved buck converters and assuming that all the phases are identical and have the same output inductors, the total inductor(s) current ripple of N phases is given by:

$$\Delta I_{Lo,ripple} = \frac{V_{in} - I_o R_{eq} - NV_O}{L} \times D \times T_S \tag{3.8.5}$$

where:

V_{in} : The input voltage.

V_o : The output voltage.

R_{eq} : The total path resistance including the ON resistance of the switch and the inductor resistance.

L_o : The output inductor of one phase assuming that all phases have equal output inductors.

And:

$$D = \frac{t_{ON}}{T_S} = \frac{V_o + \frac{I_o}{N} R_{eq}}{V_{in}} \tag{3.8.6}$$

By substituting Equations (3.8.2) and (3.8.3) in Equation (3.8.4), and using Equations (3.8.5) and (3.8.6), the phase switching frequency ($f_S = 1/T_S$) is given by:

$$f_s = \frac{2V_o(N \times V_o + I_o \times R_{eq} - N \times V_{in})(V_{in} - N \times V_o - I_o \times R_{eq}) \times e}{NV_{in}(a \times I_o + b \times (t_{del})^2 + c \times t_{del} + d \times C_o)} \tag{3.8.7}$$

where:

$$a = (2 \times N \times V_{in} \times R_{eq} \times ESR \times t_{del} - 2 \times N \times V_{in} \times R_{eq} \times ESL + 2 \times Hyst \times L \times R_{eq})(C_o) - N \times V_{in} \times R_{eq} \times (t_{del})^2$$

$$b = N \times (V_{in})^2 - N^2 \times V_{in} \times V_o$$

$$c = (N^2 \times V_{in} - N \times (V_{in})^2)(2 \times V_o \times ESR \times C_o)$$

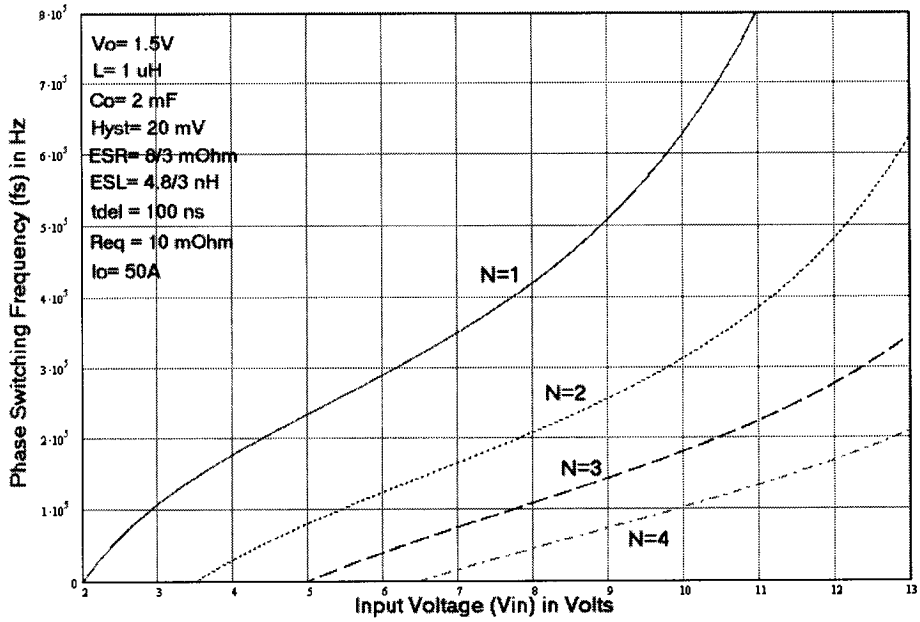
$$d = (2 \times N \times Hyst \times L)(V_o - V_{in}) + (N \times (V_{in})^2 - N^2 \times V_{in})(2 \times ESL)$$

$$e = N \times V_o \times ESR \times C_o + I_o \times R_{eq} \times ESR \times C_o - N \times V_o \times t_{del} - I_o \times R_{eq} \times t_{del}$$

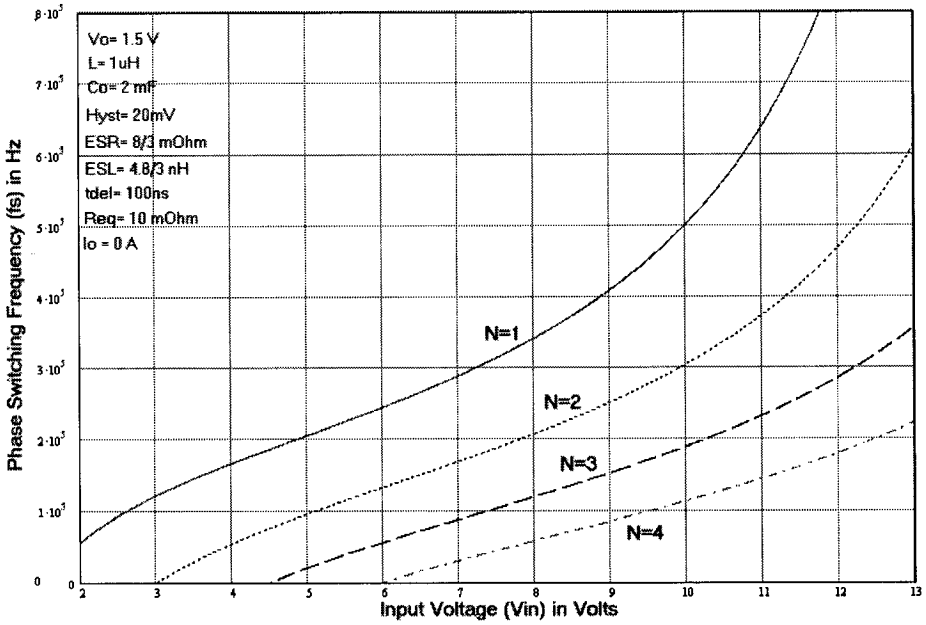
Even though Equation (3.8.7) shows that the switching frequency depends on the load current, this dependency is very small since synchronous rectifiers have the same equivalent circuit over the switching period. This will be shown by plotting curves at different loads later in this section. This load current dependency appears since the switches' ON resistances and the inductors' resistances have been considered in the mathematical derivation. Moreover, since synchronous rectifiers were used, there is no discontinuous mode of operation even at light loads.

Figure 3.15 shows the phase switching frequency f_S versus the input voltage in the case of 1, 2, 3 and 4 phases being used at no-load and full-load conditions for the following parameters: $V_o = 1.5V$, $L_o = 1\mu H$ per phase, $2mF$ output capacitance with $ESR = 8m\Omega/3$ and $ESL = 4.8nH/3$, assuming three paralleled capacitors with a total of $2mF$, $t_{del} = 100ns$ and $Hyst = 20mV$ for full load $I_o = 50A$. Figure 3.15 shows that the phase switching frequency is decreased with the number of phases increased for the same hysteresis window. Of course, if the switching frequency of each phase for N phases is kept the same as the original switching frequency for one phase converter, the output voltage will have a smaller ripple.

It must be noted that the maximum output voltage for N interleaved phases cannot ideally exceed $1/N$ of the input voltage (assuming $R_{eq} = 0\Omega$, i.e., no voltage drop across components and traces) because of the restriction that only one high-side switch can be ON at anytime in steady-state conditions. Therefore, larger minimum input voltage is required when the number of phases increases for the same output voltage. This explains the switching frequency zero crossing of Figure 3.15.



(a)



(b)

Figure 3.15: Theoretical Phase Switching Frequency Versus Input Voltage for N Interleaved Phases at: (a) Full load Condition and (b) No Load Condition

Equation (3.8.7) denominator has a zero that puts a condition on the maximum value of ESL. For the voltage across the ESL not to exceed the hysteresis window and cause the frequency to be very high and uncontrollable, the following condition must be satisfied:

$$ESL < \frac{a \times Hyst + b \times ESR + c}{2 \times N \times V_{in} \times C_o \times (V_{in} - I_o \times R_{eq} - N \times V_o)} \tag{3.8.8}$$

where:

$$a = (2 \times L \times C_o)(N \times V_{in} - I_o \times R_{eq} - N \times V_o)$$

$$b = (2 \times N \times V_{in} \times C_o \times t_{del})(V_{in} - I_o \times R_{eq} - N \times V_o)$$

$$c = (N \times V_{in} \times (t_{del})^2)(-V_{in} + N \times V_o + I_o \times R_{eq})$$

Figure 3.16 shows the maximum allowable ESL value versus hysteresis window for 1, 2, 3 and 4 phases at no-load condition for the same parameters of Figure 3.15, since from Equation (3.8.8) the worst-case design for ESL is at no load because the maximum allowable ESL decreases as the load decreases. From Figure 3.16, it is apparent that the maximum allowable ESL increases as the number of phases increase.

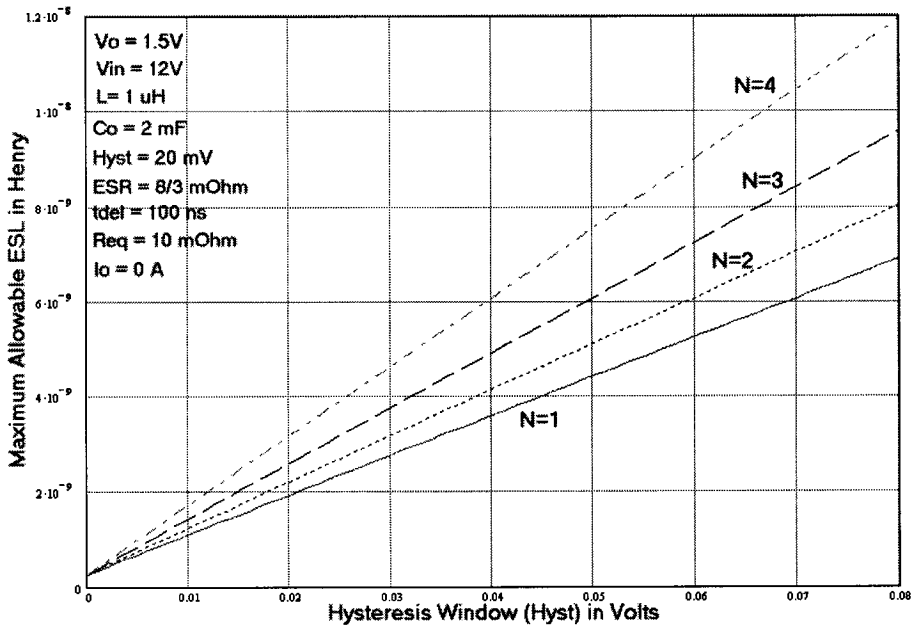


Figure 3.16: Maximum Allowable ESL Versus Hysteresis Window for N Interleaved Phases

3.9 Simulation Results

A two-phase DC-DC buck converter with the presented current sharing method and voltage-mode hysteretic control was simulated using Pspice/Orcad software package with the following design parameters: $V_{in} = 12V$, $V_o = 1.5V$, 50 Amps full load, $L_{phase1} = L_{phase2} = 1\mu H$, and $C_o = 2mF$, with a steady-state hysteretic band of ±10mV and transient hysteretic band of 30mV. It is assumed that three capacitors were paralleled with $ESR = 8m\Omega$ and $ESL = 4.8nH$ for each. Other simulation parameters were $t_{del} = 100ns$ and $R_{eq} = 10m\Omega$.

Figures 3.17 through 3.21 show the simulation results at different conditions, where:

- $V(V_o)$ is the output voltage waveform.

- *I(LAo)* and *I(LBo)* are the output inductor currents waveforms for Phase A and Phase B, respectively.
- *MCS* is the hysteretic comparator output waveform derived directly from the output voltage ripple.
- *V(Current_Comp)* is the current comparison waveform, which is logic high when Phase A is smaller than Phase B, and logic low when Phase B is smaller than Phase A.
- *V(MCSA)* and *V(MCSB)* are the final high-side switches driving waveforms for Phase A and Phase B, respectively.

Figure 3.17 shows the simulation results in steady-state condition. Figures 3.18 and 3.19 show the simulation results at high-to-low load transient condition from 50A to 20A and at low-to-high load transient condition from 20A to 50A, respectively.

Figure 3.20 shows the simulation results when the current sharing function is disabled and the two phase currents are made different deliberately so that Phase A carries twice the current of Phase B. Figure 3.21 shows the simulation results when the current sharing function is enabled for the case of Figure 3.20, where Figure 3.21(a) shows a sample waveform when the controller did not have to take a correction pulse to maintain the current sharing, while Figure 3.21(b) shows a sample waveform when the controller had to take a correction pulse to maintain equal current sharing. It is apparent that the current sharing is maintained regardless of the large differences in the phase construction.

The simulations show that the switching frequency of the simulation results agrees with the theoretical results of Figure 3.15.

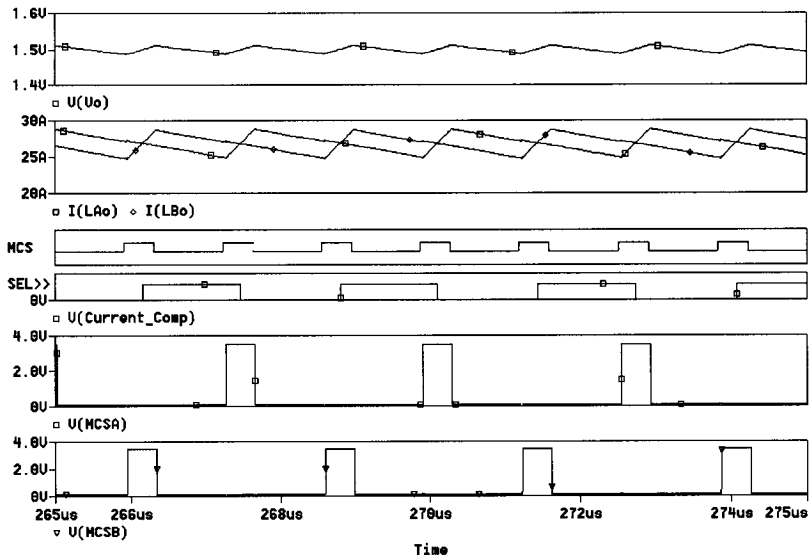


Figure 3.17: Simulation Results in Steady-State Condition

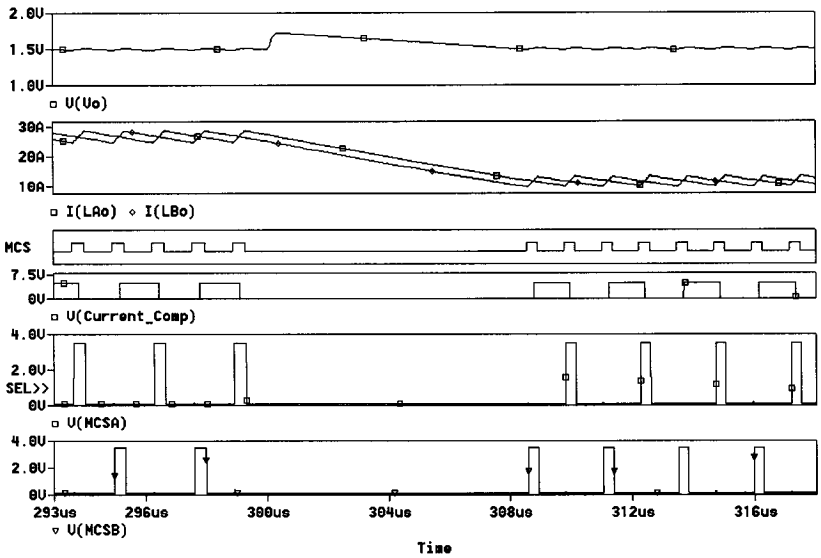


Figure 3.18: Simulation Results in a High-to-Low Load Transient Condition

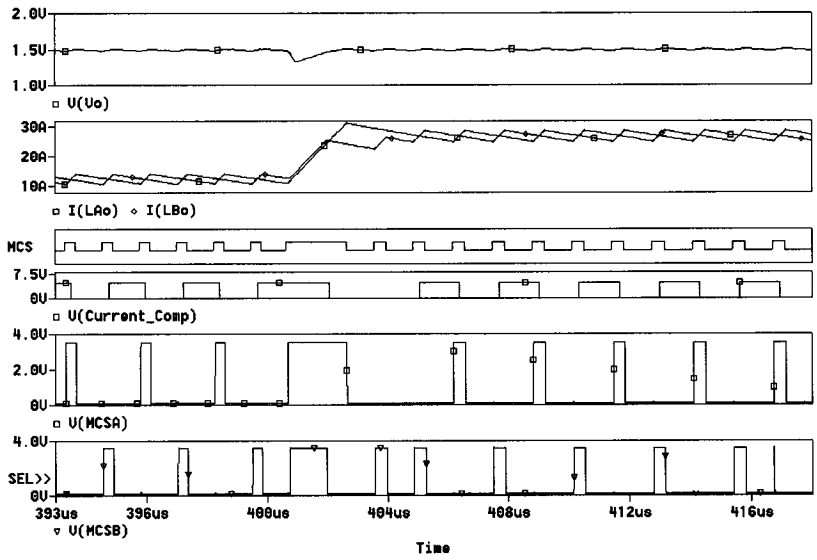


Figure 3.19: Simulation Results in a Low-to-High Load Transient Condition

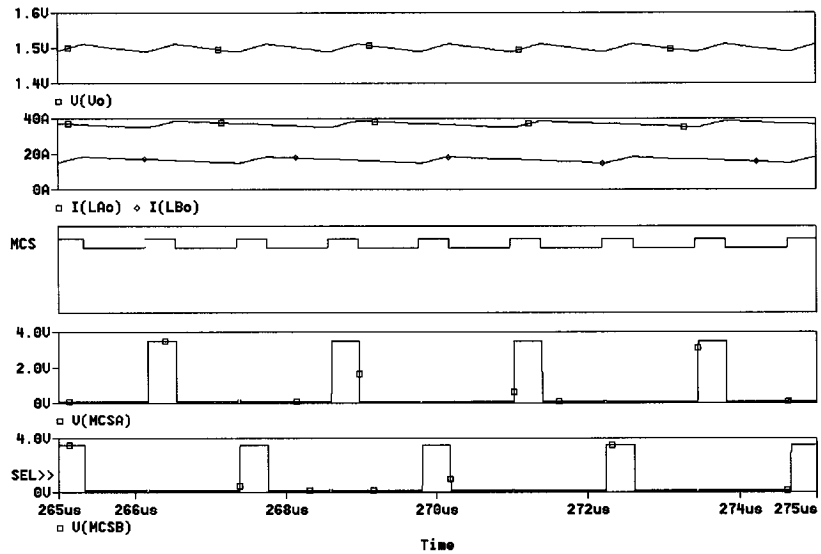
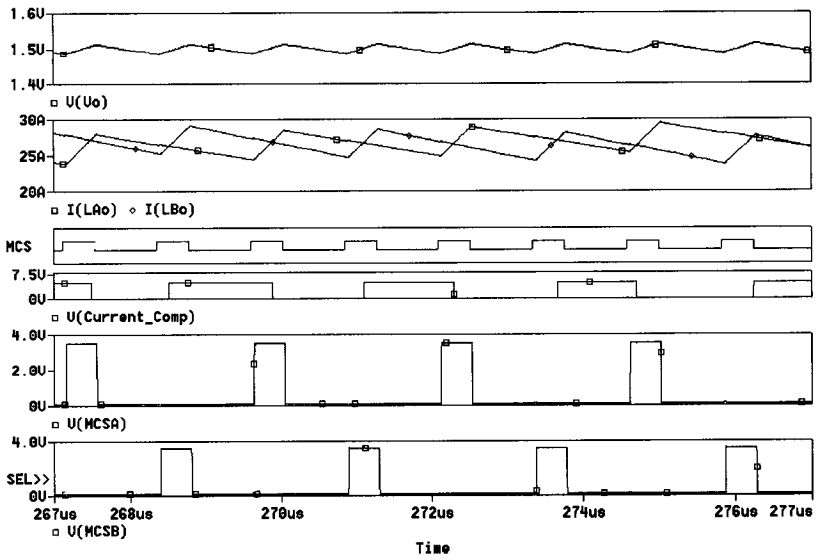
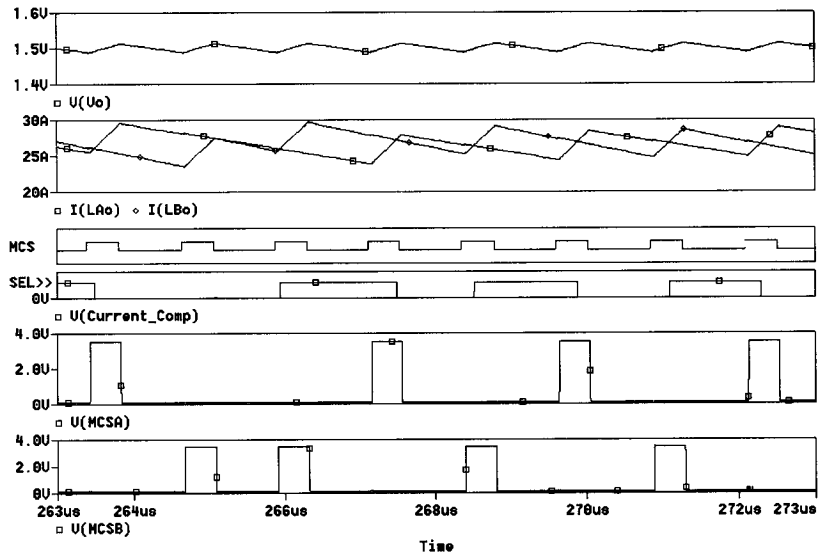


Figure 3.20: Simulation Results When the Two Phases are Deliberately Made Un-Identical so that Phase A Carries Twice the Current of Phase B when the Current Sharing Function is Disabled



(a)



(b)

Figure 3.21: Simulation Results for the Same Case of Figure 3.20 but when the Current Sharing Function is Enabled. Two Waveform Samples are Shown: (a) with No Current Correction Pulse and (b) with Current Correction Pulse

3.10 Experimental Study

A two-phase DC-DC buck converter experimental prototype with input voltage of 5V and output voltage of 1.5V and a maximum load current of 50A was built in the laboratory for verification purposes.

Figure 3.22 shows the experimental waveforms in steady-state for the output voltage, the high-side MOSFETs driving signals and the output inductors currents when the current sharing function is enabled. Figure 3.23 shows experimental output inductors currents of the two phases at load transients when the current sharing function is disabled and the two phases are deliberately made un-identical so that phase A carries more than three times the current of phase B. Meanwhile Figure 3.24 shows the results when the current sharing is enabled for the same case as Figure 3.23. Figure 3.25 shows the experimental waveforms when the controller had to take a corrective action to maintain equal current sharing.

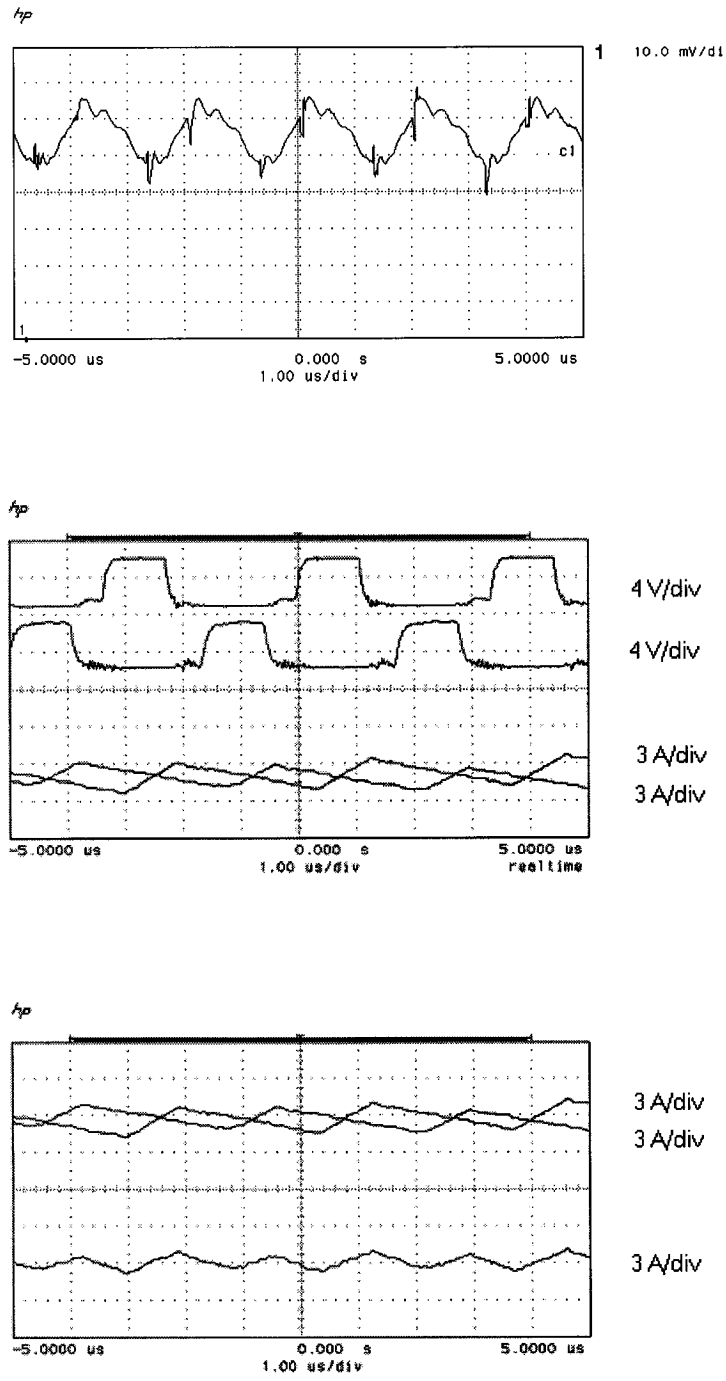


Figure 3.22: Experimental Waveforms in Steady-State Condition when the Current Sharing Function is Enabled: Output Voltage Waveform, High-Side MOSFETs Driving Signals, Inductor Currents and Total Current, Respectively

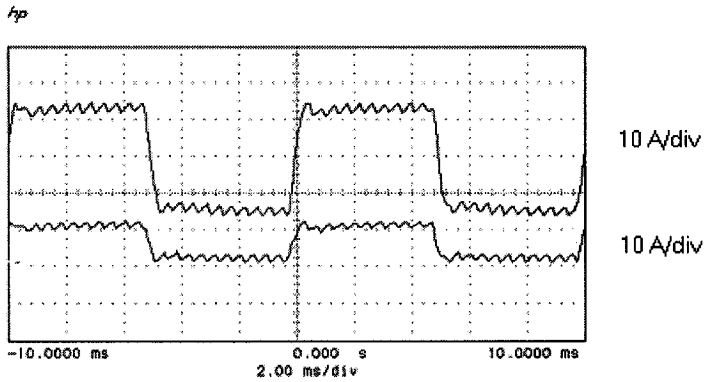


Figure 3.23: Experimental Output Inductor Currents of the Two Phases at Load Transients when the Current Sharing Function is Disabled and the Two Phases are Deliberately Made Un-Identical so that Phase A Carries More Than Three Times the Current of Phase B

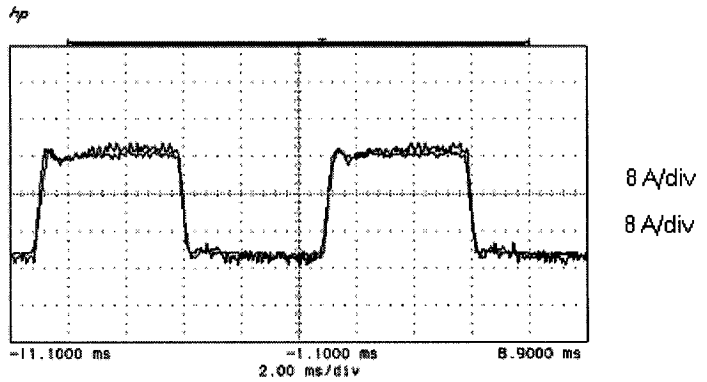


Figure 3.24: Experimental Output Inductors Currents for the Same Case as Figure 3.23 but when the Current Sharing Function is Enabled

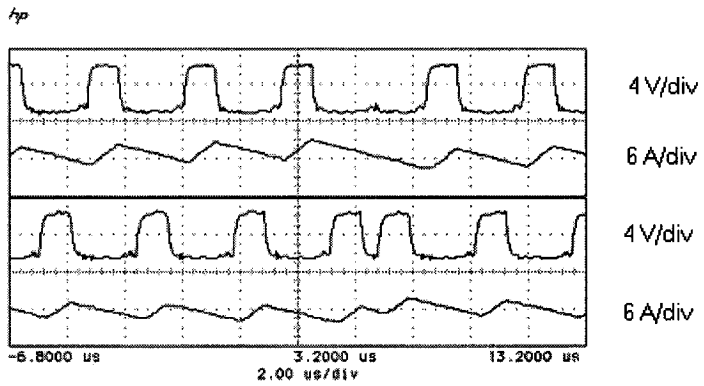


Figure 3.25: Experimental Results for the Case of Figure 3.23 when the Controller Had to Take Corrective Action to Maintain Equal Current Sharing

It is clear that equal current sharing was achieved at all conditions, i.e., during full load steady-state, during low load steady-state and during transients with small and large differences in the phases' layouts.

The frequency of each phase was around 330KHz even though the input is 5V because of the total ESR and ESL. This matches the frequency Equation (3.8.7) for the following parameters: $V_{in} = 5V$, $V_o = 1.5V$, $L_o = 1\mu H$ per phase, $C_o = 2mF$, $ESR = 10m\Omega$ and $ESL = 3nH$, $t_{del} = 100ns$, and $Hyst = 20mV$, $R_{eq} = 10m\Omega$ and $I_o = 50A$.

3.11 Summary

Multiphase voltage-mode hysteretic control for DC-DC converters with current-sharing method is presented in this chapter. This current-sharing method results in several advantages that include: simple to apply to any control method, independent of the main

control method used in the voltage regulation controller closed loop, no need for current reference, good equal current sharing accuracy at all load conditions in steady-state and transients, no need for compensation and hence, does not affect the controller speed. In addition, this sharing approach may be applied to any control method, even those that have no loop compensation or ripple dependent such as multiphase hysteretic control. The application of the presented method is generalized for N interleaved phases.

Moreover, the presented current sharing method was applied to a multiphase voltage-mode hysteretic-controlled DC-DC converter, which resulted in a new and simple control technique with low output voltage ripple and fast transient response.

The frequency equation was derived for N interleaved phases by considering ESR, ESL and the path resistance with the output current effect. Another equation that shows the maximum allowable ESL to keep the controller stable was also derived. Design curves were plotted and compared to simulation results. An experimental prototype was then built in the laboratory to verify the presented method.

CHAPTER 4

REVIEW OF SELECTED ISOLATED TOPOLOGIES AND DUTY-CYCLE-SHIFTED CONTROLLED HALF-BRIDGE

4.1 Introduction

As mentioned earlier, on-board DC-DC converters can be isolated or non-isolated. Isolated DC-DC converters may be a strong candidate for future on-board converters, including VRM, over non-isolated converters because of their high-input bus voltage. High bus voltage has several advantages including low distribution losses, ease of design, lower and smaller on-board converters input filter including capacitance and load transients has less effect on the bus voltage and on other loads [2, 43].

In this chapter, a review of some common isolated topologies will be given briefly, and a control method for half-bridge DC-DC converter, namely the Duty-Cycle-Shifted (DCS) control [51,52], will be presented.

4.2 Review of Selected Isolated DC-DC Converter Topologies

DC-DC isolated topologies utilize additional isolation transformer between a primary-side topology and a secondary-side rectification topology [4,40,42,44-47,49,51, 52,62-65]. This transformer can be used for electrical isolation between the source and the load and/or for additional voltage step-down (in low output voltage applications)

provided by its turns ratio. Figure 4.1 shows a block diagram of isolated topologies, where the transformer turns ratio (n) is equal to the ratio between the primary winding turns' number and the secondary winding turns' number as follows:

$$n = \frac{n_p}{n_s} \tag{4.2.1}$$

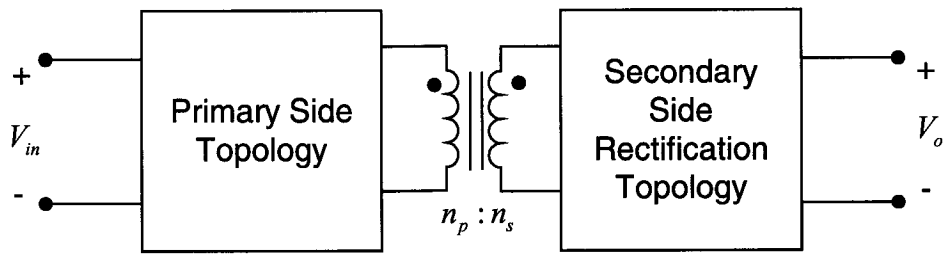


Figure 4.1: A Block Diagram of DC-DC Isolated Topologies

The primary-side topology, in an isolated DC-DC converter, usually inverts the DC input voltage to an AC voltage with certain amplitude and duration applied across the isolation transformer primary side. This AC voltage can be of different waveforms including square waveform and sinusoidal waveform. Then, the isolation transformer steps down (or up) the amplitude of the AC voltage (it usually steps down on low-output-voltage applications) at the secondary side. Thereafter, the stepped AC voltage is rectified by the secondary-side topology converting it back to DC voltage with large ripple, before it is filtered out by an output filter yielding to a DC output voltage with smaller ripple.

As shown in Figure 4.2, the primary-side topology, for example, can be phase-shifted full-bridge [7,40,42], symmetrical half-bridge [4,43,51,52], asymmetrical half-bridge [44-47], push-pull [43,48] or active clamp [43,48-50]. While the secondary-side rectification topology, for example, can be forward [4,49,64], center-tapped [4] or current

doubler [4,7,48,51,52], as shown in Figure 4.3. It must be noted that diodes in Figure 4.3 can be replaced by active switches.

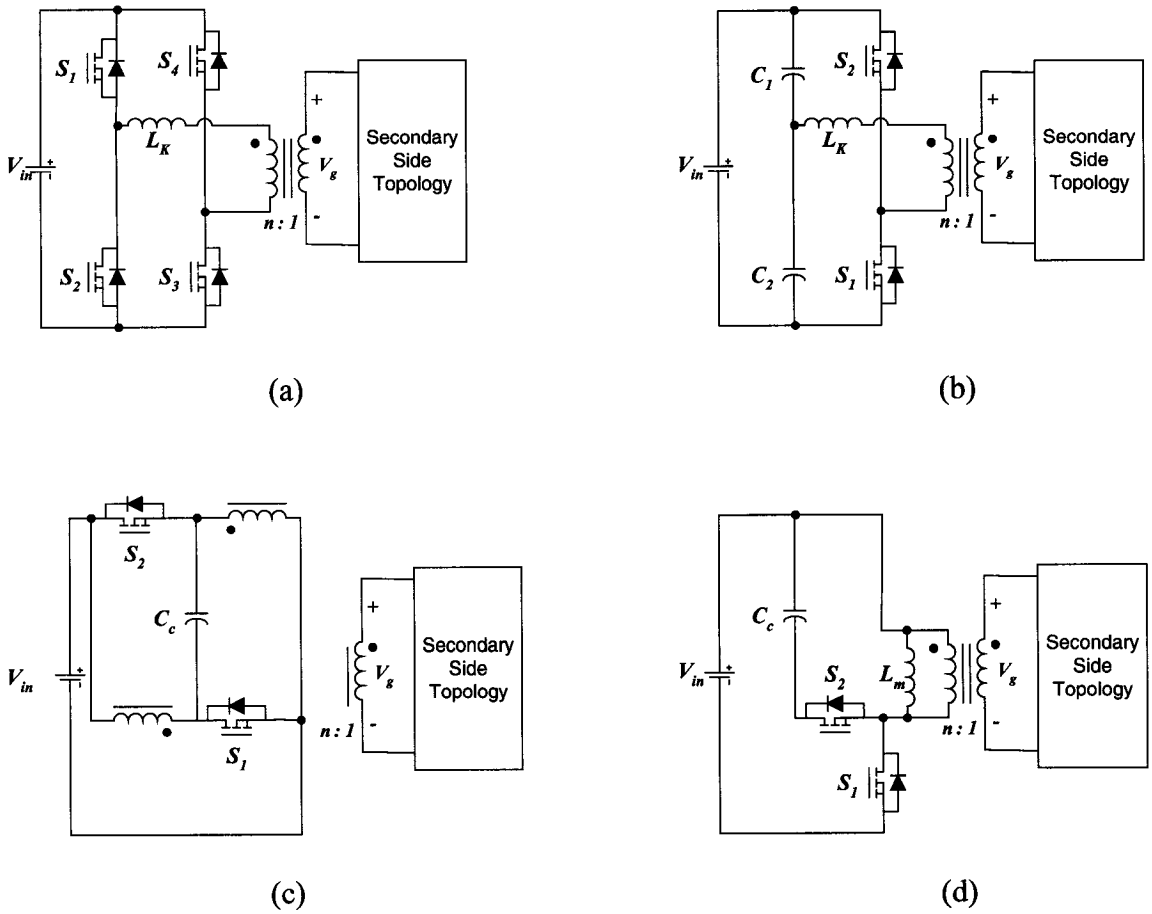


Figure 4.2: Example of Primary Side Topologies in Isolated DC-DC Converters: (a) Full-Bridge, (b) Half-Bridge, (c) Push-Pull and (d) Active-Clamp

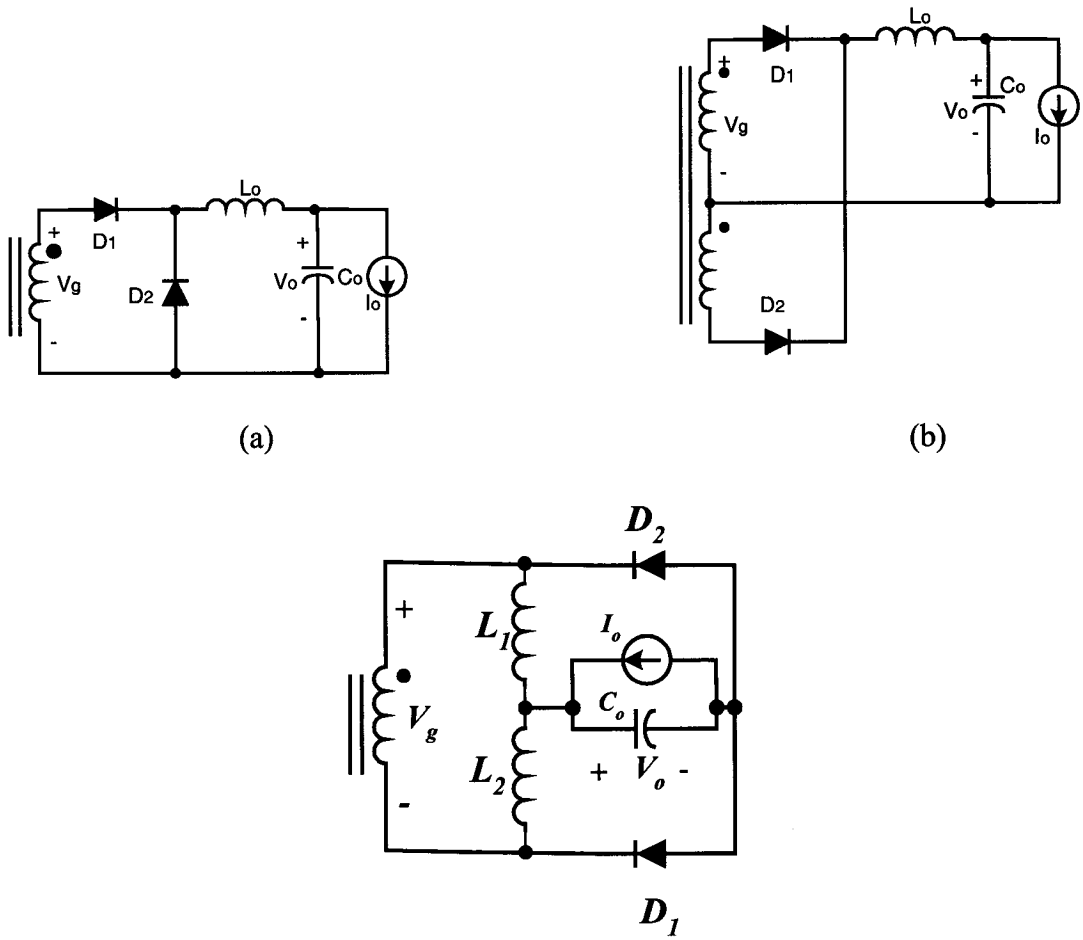


Figure 4.3: Example of Secondary Side Rectification Topologies in Isolated DC-DC Converters: (a) Forward, (b) Center-Taped and (c) Current Doubler

At the secondary side, even thought the secondary-side forward scheme has the simplest structure, it has large rectification and conduction loss, and it has larger conduction loss for the switches compared with the center-tapped scheme. Moreover, the forward topology requires larger output inductance than the other two schemes, which is not preferred in the fast-transient converters. The center-tapped scheme requires small

inductance, since the frequency of the output inductor voltage is twice the switching frequency [4]. Current-doubler is one of the best candidates for high-output current, low-output voltage applications because the current in each secondary side inductors is half compared to the other two schemes. In addition, the effective output inductance is reduced (less than it is for the forward scheme), since there is a partial current ripple cancellation in the output capacitor.

At the primary side, the full-bridge topology can achieve ZVS for its switches that have a voltage stress equal to half of the input voltage and a current stress equal to half of the input current at the expense of larger switches count with their drivers. The push-pull topology switches can achieve ZVS but have the same current stress and twice the voltage stress compared to the full-bridge switches. Push-pull topology also has a large induced voltage spike when the switch is turned OFF because of the transformer-leakage inductance, which causes switch turn OFF loss [43]. This voltage spike causes switches with larger voltage ratings to be used, which means switches with larger ON-state resistance, causing larger conduction losses. Active-clamp (forward-flyback) topology can also achieve ZVS for its switches, but it causes large conduction losses for the secondary side, turn OFF losses and transformer core losses because of the current generated to support the secondary side during the OFF time [43,50]. The half-bridge topology has the same switches' voltage stress and twice the current stress of the full-bridge topology, and it has less component count compared, simpler configuration and driving schemes, and its transformer-required turns ratio is smaller for low output voltage. Half-bridge topology can also achieve ZVS when its switches are driven by a ZVS control scheme, which will be discussed in the following sections.

From the above discussion, half-bridge topology with current-doubler secondary side rectification is a suitable topology for low-output voltage, high-output current applications with medium power levels.

The next section will review two conventional control schemes for half bridge, namely, hard-switching symmetric control and soft-switching asymmetric (or complementary) control schemes followed by another section that presents a symmetric soft-switching control scheme.

4.3 Half-Bridge Topology's Two Conventional Control Schemes

Figure 4.4 shows half-bridge topology with current-doubler secondary side. There are two conventional schemes to control switches S_1 and S_2 of the half-bridge, namely symmetric control scheme and asymmetric (complementary) control scheme [4, 43,44,47,51,52]. Figure 4.5 shows main switching waveforms of the half-bridge topology of Figure 4.4 for each of the two conventional control schemes.

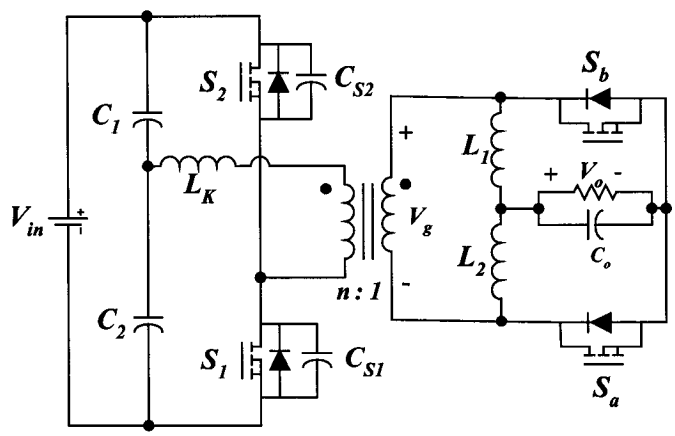
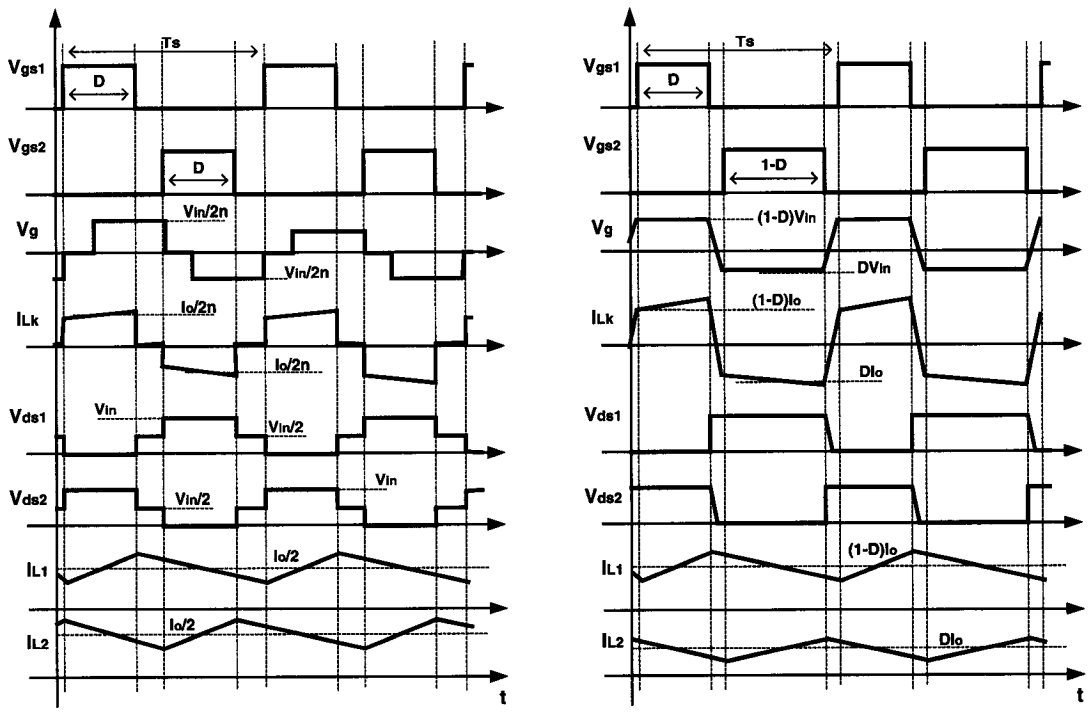


Figure 4.4: Half-Bridge Topology with Current-Doubler Secondary Side



(a) (b)

Figure 4.5: Main Switching Waveforms of Half-Bridge Topology of Figure 4.4 with: (a) Symmetric Control Scheme and (b) Asymmetric Control Scheme

When asymmetric control scheme is used, where S_1 and S_2 control signals are complementary, the dead time between turning OFF a switch and turning ON the other switch is very small. This will allow ZVS operation for both switches by utilizing a resonant behavior between the transformer-leakage inductance (L_k) and the switches junction capacitances (C_{s1} and C_{s2}) during the small dead time forcing the voltage across the other switch to drop to almost zero before turning it ON. In symmetric control, since this dead time is relatively large, ZVS can not be achieved, except at one point where the switches duty cycles are close to 50 percent, which is usually not the case since the

converter design should consider the input voltage and load variations that cause the duty cycle to be designed far from 50 percent at nominal input voltage and load.

In symmetric control, however, the two switches duty cycles are complementary and not equal in time duration. This results in unequal voltages across the half-bridge's two capacitors (C_1 and C_2), and hence the components' voltages and currents are asymmetric. For example, the voltages across secondary-side rectifier switches are not equal. Moreover, asymmetric control has a nonlinear DC gain, which means that larger duty cycle variation range is needed for the same input voltage and load variation, resulting in converter performance degradation. This is not the case for symmetric control where the components' stresses are symmetric since the switches duty cycles are symmetric.

From the above information, the asymmetric-controlled half-bridge is not suitable for applications where the input voltage and load have a wide variation range because of the stresses' asymmetry, even though it can achieve ZVS that is suitable for high switching frequency where switching and transformer-leakage inductance-related losses [100] can be reduced by ZVS. The case is exactly the opposite for the symmetric-controlled half-bridge.

Therefore, a new control for half-bridge that can achieve ZVS without creating asymmetry will be of advantage. To achieve this, next section presents the Duty-Cycle-Shifted (DCS) control for half-bridge topology, that was first reported in [51,52].

4.4 Duty-Cycle-Shifted Control for Half-Bridge

The Duty-Cycle-Shifted (DCS) control scheme [51,52] is based on a symmetric duty cycle for both half-bridge switches shown in Figure 4.4 as follows: By shifting the S_2 driving signal left close to the driving signal of S_1, the dead time between S_1 control signal falling edge and S_2 control signal rising edge becomes very small, resulting in ZVS turn ON condition for S_2. Or, if S_1 driving signal is shifted left and close to the driving signal of S_2, ZVS will be achieved for S_1. The first case main switching waveforms are shown in Figure 4.6.

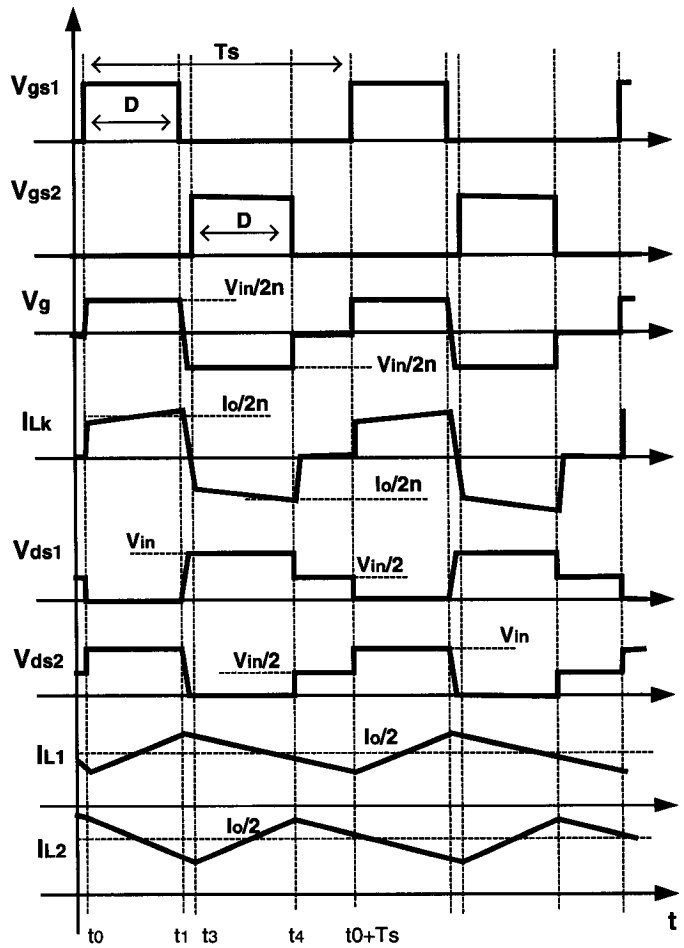


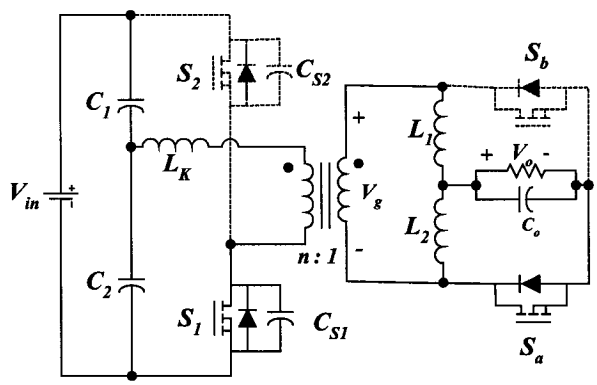
Figure 4.6: Main Switching Waveforms of Half-Bridge Topology with DCS Control

In Figure 4.6, when S_1 is turned OFF, the transformer-leakage inductor current and reflected inductor current charge or discharge switches junction capacitors. After the voltage across drain-to-source of S_2 drops to zero, the body diode of S_2 conducts to carry current. During the body diode conduction period, S_2 may be turned ON with ZVS. No ringing occurs during the transition period.

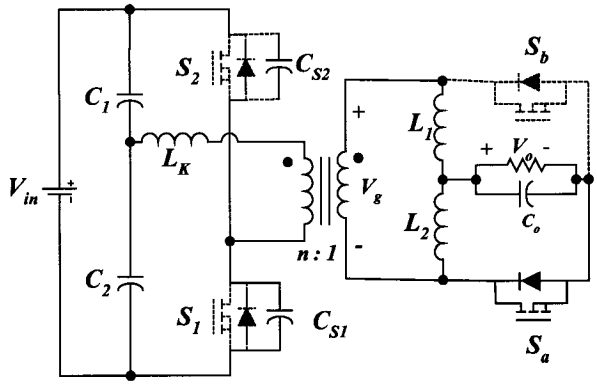
Therefore, using DCS control, ZVS turn ON is achieved for one of the two half-bridge switches, resulting in reduced switching losses and leakage inductance ringing and related losses. Such loss reduction becomes more significant as the switching frequency increases, since the switching losses are directly proportional to the switching frequency. Moreover, using DCS control, no asymmetric components penalties are generated such as those discussed earlier.

4.5 DCS-Controlled Half-Bridge Modes of Operation

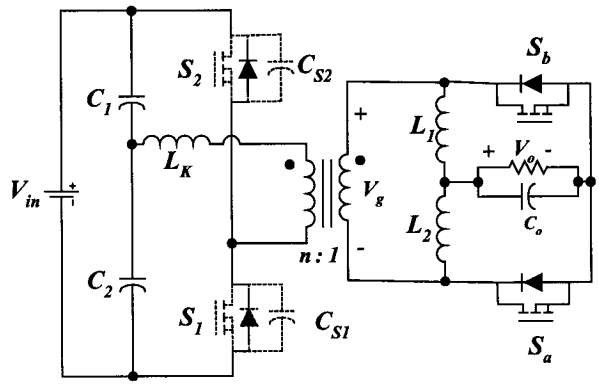
The DCS-controlled half-bridge modes of operation equivalent circuits are shown in Figure 4.7 and their description, assuming all components are idea except otherwise indicated and C_1 and C_2 are large enough to be able to keep constant voltage, can be summarized as follows:



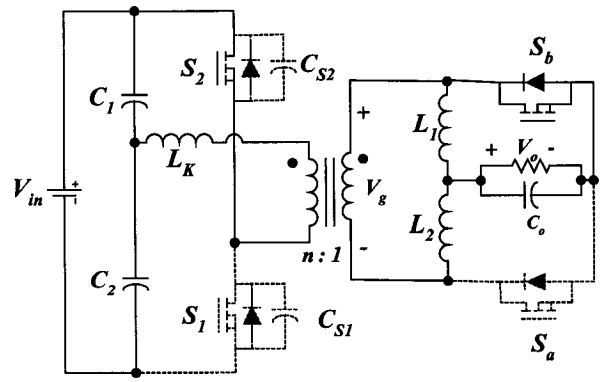
(a)



(b)



(c)



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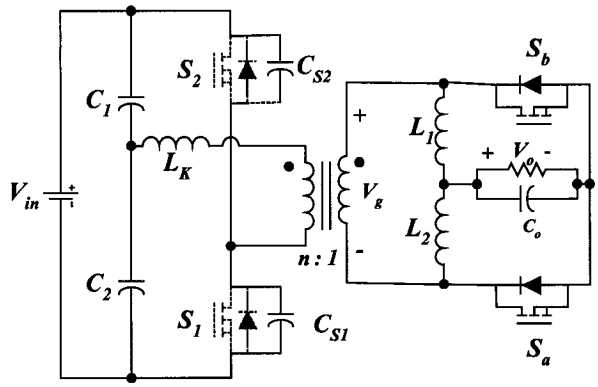
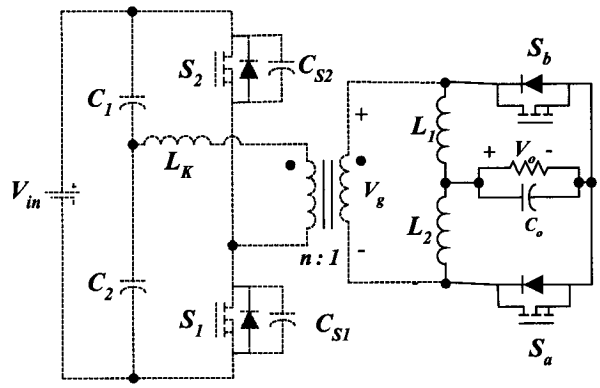


(e)



(f)

Figure 4.7: DCS-Controlled Half-Bridge Modes of Operation Equivalent Circuits: (a) through (f) Equivalent Circuits for Modes 1 through 6

Mode 1: $t_0 \le t < t_1$

During this mode, S_1 is ON while S_2 is OFF. The voltage V_g applied to the transformer secondary side is positive, and therefore the secondary side switch S_a should be turned ON while S_b is OFF. Output inductor L_a carries the output current (charge up through S_a) while output inductor L_b freewheels (discharges).

Mode 2: $t_1 \le t < t_2$

At $t = t_1$, S_1 is turned OFF. The transformer-leakage inductance resonates with the junction capacitances C_{s1} and C_{s2}. At the end of this mode, the voltage across C_{s1} charges up to V_{in}, while the voltage across C_{s2} drops to zero.

Mode 3: $t_2 \le t < t_3$

The drop of the voltage across C_{s2} to zero at $t = t_2$ causes S_2 body diode to conduct and carry the current. This provides ZVS condition for S_2. During this mode, the current doubler rectifiers S_a and S_b are turned ON and the output inductors currents freewheels through them.

Mode 4: $t_3 \le t < t_4$

At $t = t_3$, S_2 is turned ON at ZVS. The voltage V_g applied to the transformer secondary side is negative, and hence the secondary side switch S_b should be turned ON, while S_a is OFF. Output inductor L_b carries the output current (charge up through S_b), while output inductor L_a freewheels.

Mode 5: $t_4 \le t < t_5$

After S_2 turn ON time duration equal to S_1 turn ON time duration of Mode 1 (equal duty cycle), S_2 is turned OFF at $t = t_4$. The transformer-leakage inductance oscillates with the junction capacitances C_{s1} and C_{s2}, while the output inductor currents start to freewheel through S_a and S_b.

Mode 6: $t_5 \le t < t_0 + T_s$

At $t = t_5$, the voltages across each of C_{s1} and C_{s2} are equal to half of the input voltage. The output inductor currents continue to freewheel through S_a and S_b until S_1 is turned ON at $t = t_0 + T_s$ starting Mode 1 again.

4.6 Experimental Study

A half-bridge experimental prototype with 3.3V/25A output and 36V~75V input voltage range was built in the laboratory to evaluate the proposed control method. Current-doubler with synchronous rectifiers is used at the secondary side. IRFS59N10D is used for switch S_1 and S_2, and Si4420DY is used for synchronous rectifiers S_a and S_b. For the purpose of comparing, both symmetric control and DCS control are applied to the same power stage.

When DCS control is used, an extra capacitor is paralleled with S_2 to reduce the turn OFF losses. RC snubber is paralleled with S_1 to damp the oscillation between leakage inductance and capacitance when S_2 is turned OFF. When symmetric control is used, RC snubbers are used in parallel with both S_1 and S_2.

Figure 4.8 shows the experimental waveforms of gate signals for switch S_1 and S_2 when DCS control is used. Figure 4.9 shows the DCS ZVS waveforms of switch S_2. Figure 4.10(a) shows the transformer primary voltage and current at full load with 48V nominal input voltage when symmetric control is used, while Figure 4.10(b) shows the same waveforms when DCS control is used. Comparing Figure 4.10(a) and Figure 4.10(b), it can be observed that the ringing is reduced when DCS control is used.

The converter efficiency was recorded for both control schemes at different loads. Figures 4.11, 4.12, 4.13 and 4.14 compare the efficiency of two control schemes at 100kHz, 200kHz, 300kHz and 400kHz respectively. It is clear that the improvement in efficiency increases with the increase of the switching frequency, and at 400kHz, efficiency improvement was up to 1.6 percent. This is because switching losses and transformer-leakage inductance-related losses are positively proportional to the switching frequency as mentioned earlier.

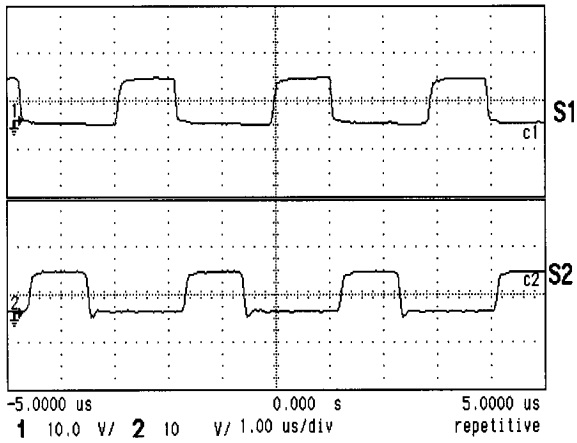


Figure 4.8: Gate Drive Signals of S_1 and S_2

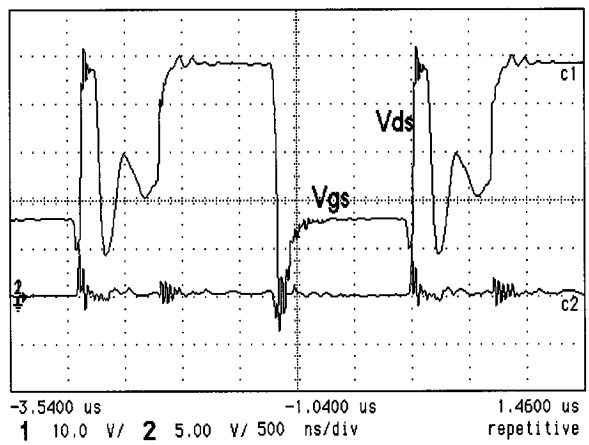
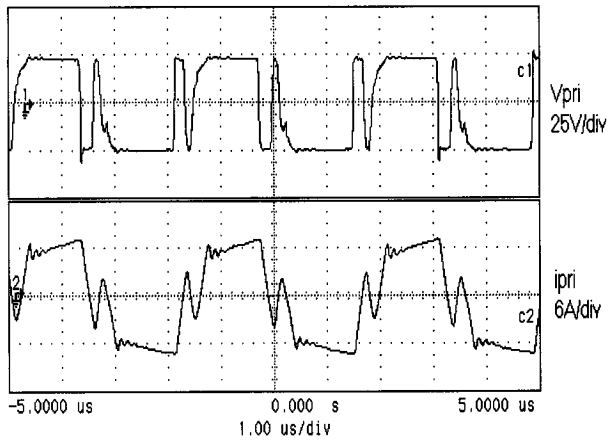
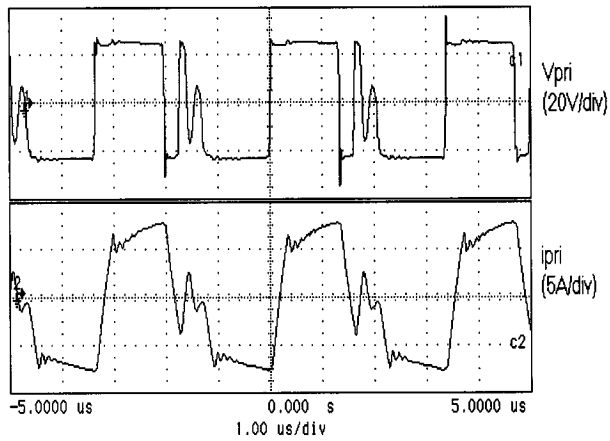


Figure 4.9: Zero-Voltage-Switching of S_2 : Drain-to-Source Voltage of S_2 with Its Gate Drive Signal Shown



(a)



(b)

Figure 4.10: Transformer Primary Voltage and Current for: (a) Conventional Symmetric Control and (b) Duty-Cycle-Shifted Control

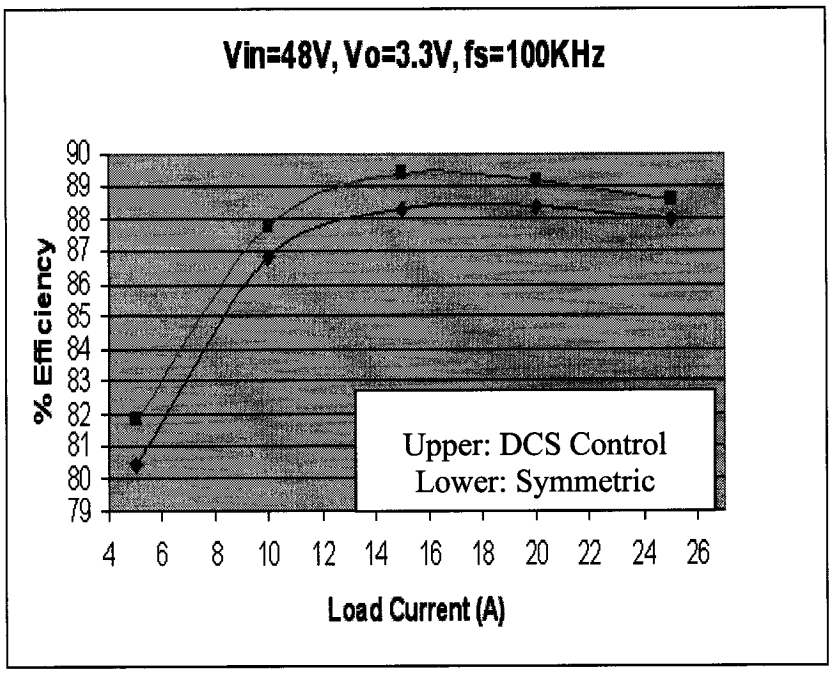


Figure 4.11: Efficiency Comparison at 100KHz

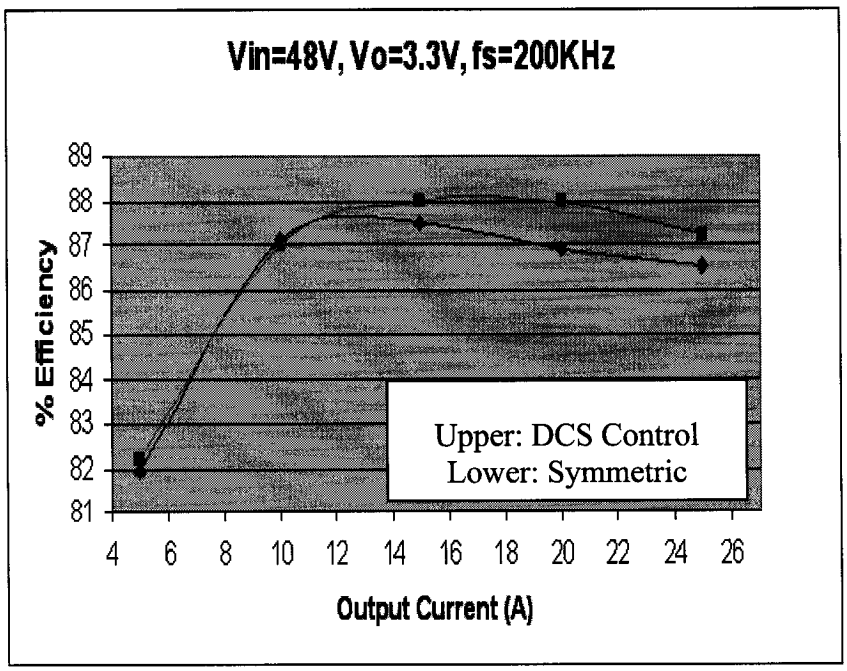


Figure 4.12: Efficiency Comparison at 200KHz

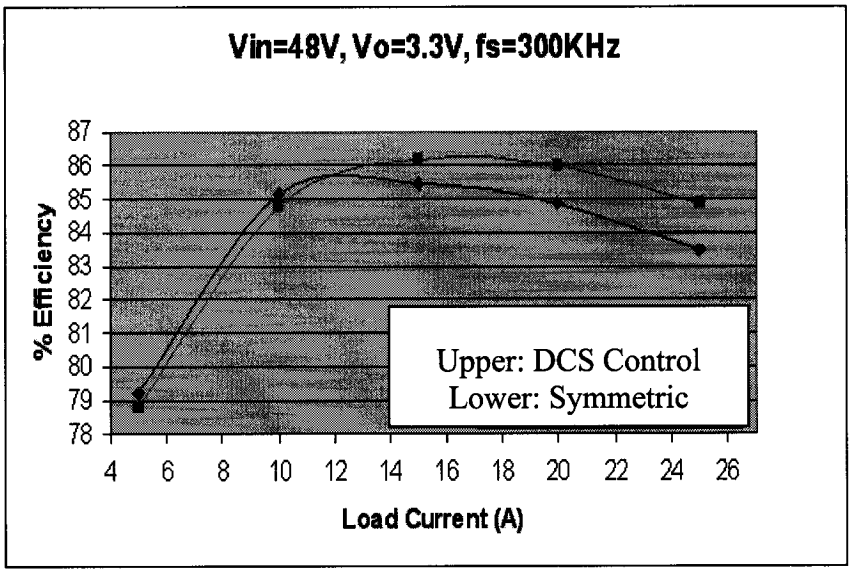


Figure 4.13: Efficiency Comparison at 300KHz

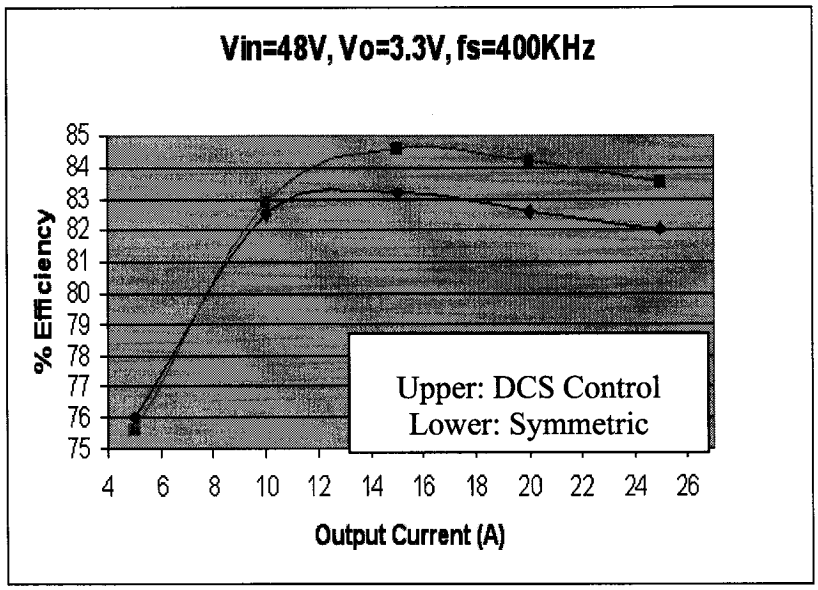


Figure 4.14: Efficiency Comparison at 400KHz

4.7 Summary

Isolated DC-DC converters were reviewed and compared briefly at the beginning of this chapter. Then, a simple and effective PWM control method known as Duty-Cycle-Shifted control method was presented to reduce switching losses and transformer-leakage inductance-related losses in the half-bridge DC-DC converter topology. Using the presented scheme, by shifting one of the symmetric PWM driving signals, Zero-Voltage-Switching (ZVS) is achieved for one of the switches without adding extra components and without adding asymmetric penalties of the complementary duty cycle control. This control concept reduces the switching losses and transformer-leakage inductance-related losses. These losses significantly degrade efficiency, especially when operating in high-switching frequencies.

Experimental results showed that the proposed control scheme improves efficiency up to 1.6 percent at 400kHz switching frequency when compared to the conventional symmetric PWM control. Better efficiency improvement is expected at higher switching frequency.

CHAPTER 5

ALTERNATED DUTY-CYCLE CONTROL METHOD FOR HALF-BRIDGE DC-DC CONVERTER

5.1 Introduction

Half-bridge topology [44,47,51] can be a good candidate for high-power density DC-DC conversion especially in applications that use Point-Of-Load (POL) DC-DC converters for present and future generation of Integrated Circuits (ICs) for communication systems and microprocessors. This is due to several reasons, including structural simplicity, a lower number of switches, a lower isolation transformer primary side turns since half of the input voltage is applied to the transformer windings and the possibility of achieving soft-switching with the appropriate control [44,47,51]. As mentioned in the previous chapter, there are two main conventional control schemes used in half-bridge topology. One is the conventional symmetric PWM control and the other is the asymmetric (complimentary) control [44,47], where two driving signals are generated complimentarily. Another control scheme, the Duty-Cycle-Shifted (DCS) control also was proposed [3] and presented in the previous chapter.

The switching frequency continues to increase mainly to reduce the size and cost of passive components and to improve dynamic performance [4,30,51]. Hence, soft-switching techniques become more desirable in order to reduce the increased switching

losses and switches body diode reverse recovery losses at these increased switching frequencies [42,44,47,51,62,99].

When the conventional symmetric control is used for half-bridge, its two switches operate at hard-switching; when the asymmetric (complimentary) control is used, the two half-bridge switches operate at soft-switching, but unfortunately cause asymmetric stresses on the converter components that are not desirable especially for a wide input voltage range of say 35V ~ 75V or 300V ~ 400V [44,47,51]. Moreover, the DC gain is not linear, which degrades the converter performance. The DCS control uses symmetric (equal) duty cycle and was able to achieve soft-switching for one switch out of two switches without adding extra components and without causing asymmetric components stresses.

In this chapter, a control method called Alternated Duty Cycle (ADC) control is presented. The ADC method can achieve soft-switching for at least one switch of the two half-bridge switches without adding additional components or switches. When soft-switching can be only achieved for one switch, ADC control alternates the soft-switching realization between the two switches so that each switch will be soft-switched half of the time and hard-switched during the other half, keeping equal power losses distribution between the switches. Moreover, any asymmetry in the duty cycle will not cause asymmetric components stresses when ADC control is used.

5.2 Alternated Duty Cycle Control

This section will discuss what the Alternated Duty Cycle (ADC) control means before going into the details and its configurations when applied to the half-bridge converter as shown in Figure 5.1.

Assume two arbitrary waveforms, C_a and C_b, generated from the PWM controller for the half-bridge as shown in Figure 5.2, where: T_s is the switching cycle period, D is the switching duty cycle, or ratio, and m is a real number (can be a floating number), when $m=1$, C_a and C_b become the control signals of asymmetric control and when $m=(1-D)/D$, C_a and C_b become the control signals of symmetric control.

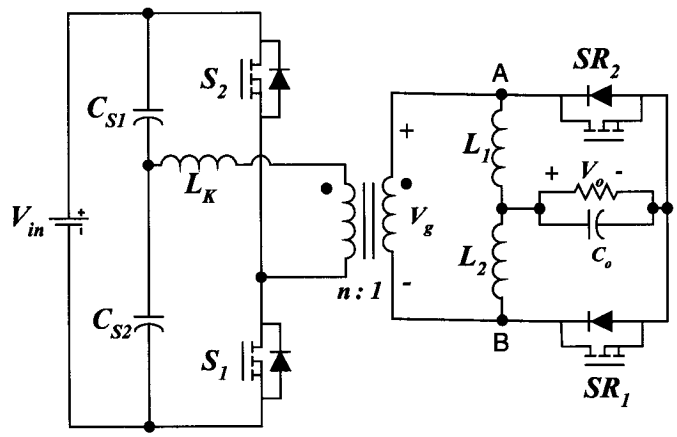


Figure 5.1: Half-Bridge Topology with Current Doubler Secondary Side

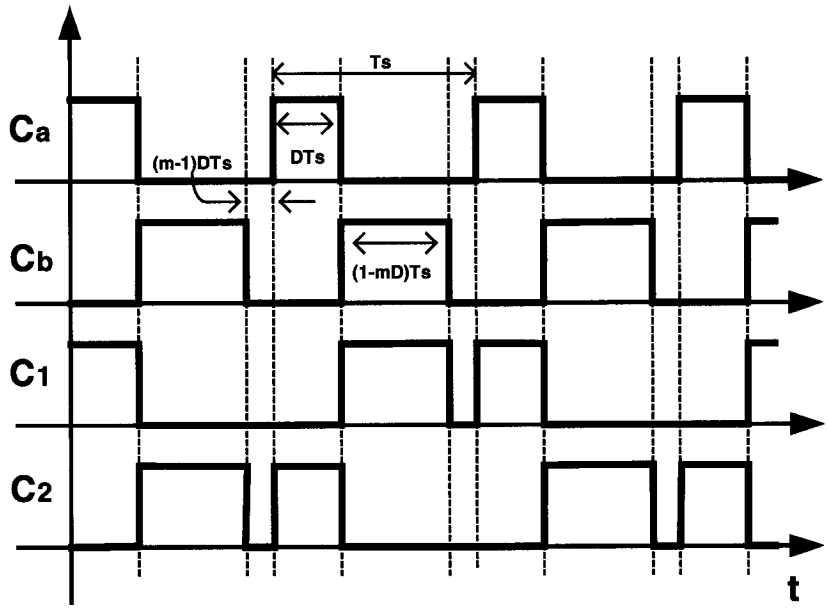


Figure 5.2: Generalized Alternated Duty Cycle (ADC) Control Waveforms

C_1 and C_2 in Figure 5.2 are the ADC control waveforms to drive S_1 and S_2 respectively, where C_a and C_b ON duration times are alternated between S_1 and S_2 so that S_1 will be turned ON by C_a in the first switching cycle and by C_b in the following switching cycle and vise versa for S_2, resulting in C_1 and C_2.

When C_a and C_b are the asymmetric control signals (when $m=1$), the resulting ADC control signals C_1 and C_2 will result in symmetric voltages across the half-bridge capacitors C_{S1} and C_{S2} even though the duty cycle is asymmetric because the average duty cycles of C_1 and C_2 are symmetric. This will result in a converter that works but unfortunately lacks the ability to be regulated for the output voltage at different input and output conditions. The reason for this phenomena is that in order to have the regulation ability in half-bridge converter, a switching dead time period is required as in the

symmetric control or asymmetry is required as in the asymmetric control, which is lost at this case.

Therefore, m will be larger than one, resulting in the loss of the soft-switching operation for one switch. However, it is interesting to note that the soft-switching will be "alternated" between the two half-bridge switches, i.e., S_1 will be soft-switched in the first cycle and hard switched in the following cycle and so on, and vise versa for S_2.

When $m=(1-D)/D$, symmetric (equal) duty cycles are achieved for C_a and C_b and therefore for C_1 and C_2. However, in the ADC control, equal duty cycle is not required since it will not affect the symmetry of the converter and because soft switching is achieved alternatively between the switches.

5.2.1 Gain Equation and Theoretical Analysis:

It can be shown simply by applying the volt-second-balance across the output inductors that the voltage gain equation for the ADC controlled half-bridge is given by:

$$\frac{V_o}{V_g}=\frac{1-D(m-1)}{2} \text{ or } \frac{V_o}{V_{in}}=\frac{1}{4n}\cdot[1-D(m-1)], \quad 1<m<\frac{1}{D} \tag{5.2.1}$$

which means that:

$$D=\frac{V_g-2V_o}{V_g(m-1)} \tag{5.2.2}$$

Figure 5.3 shows the voltage gain versus duty cycle for different values of m.

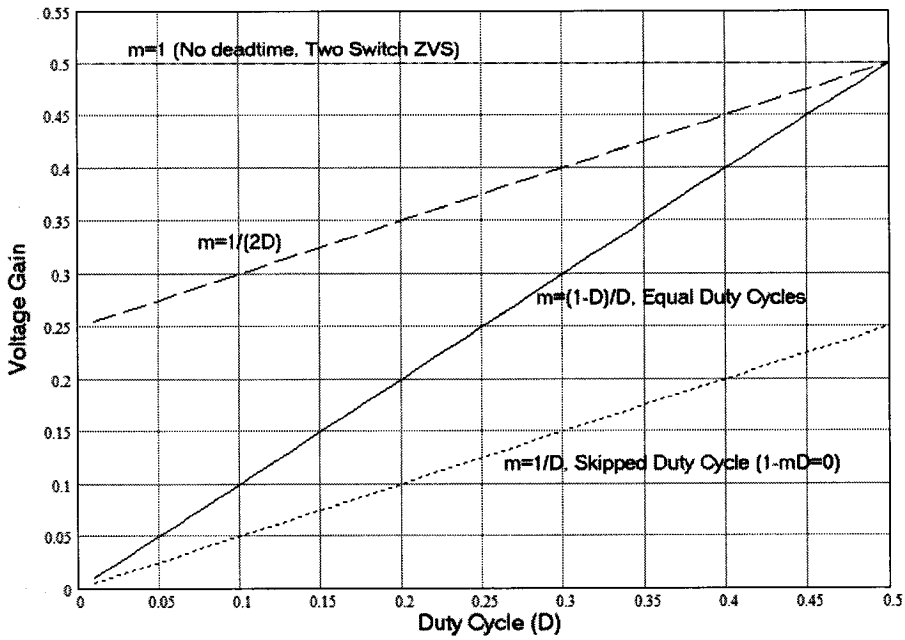


Figure 5.3: Voltage Gain Versus Duty Cycle for Different Values of m

The output current ripple equation for ADC controlled half-bridge is given by:

$$\Delta I_o = \frac{2D(m-1)}{L \cdot f_s} \cdot V_o = \frac{2V_o}{V_g} \frac{V_g - 2V_o}{L \cdot f_s}, \; V_g = \frac{V_{in}}{2n} \tag{5.2.3}$$

Figure 5.4 shows the output current ripple versus duty cycle from Equation (5.2.3) for $V_o = 3.3V$, $L = 2\mu H$ and $f_s = 400kHz$ at different m values.

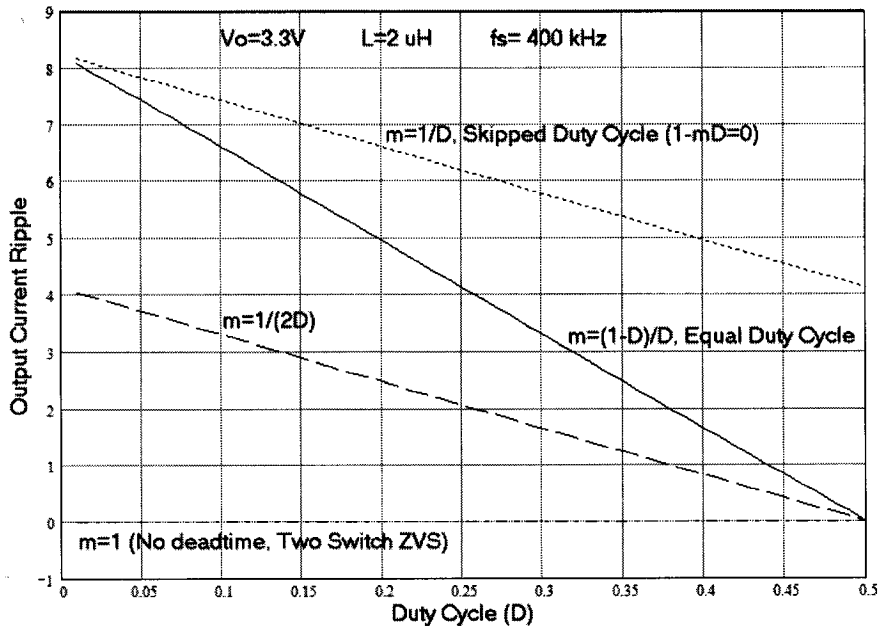


Figure 5.4: Output Current Ripple versus Duty Cycle at Different m Values for $V_o = 3.3V$, $L = 2\mu H$ and $f_s = 400kHz$

5.2.2 Implementation:

Figure 5.5 shows a simple circuit that can be used to implement ADC control by generating the ADC signals C_1 and C_2 shown in Figure 5.2 from a given C_a and C_b that were generated from the regular modulator.

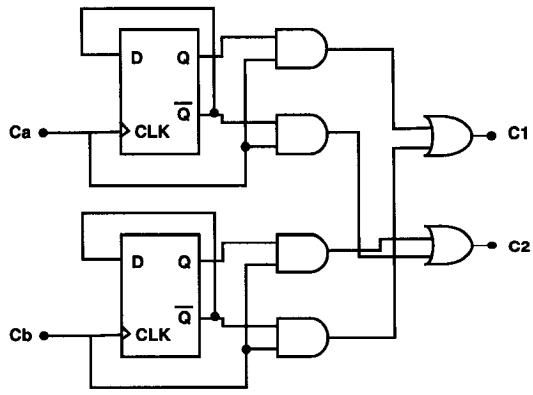
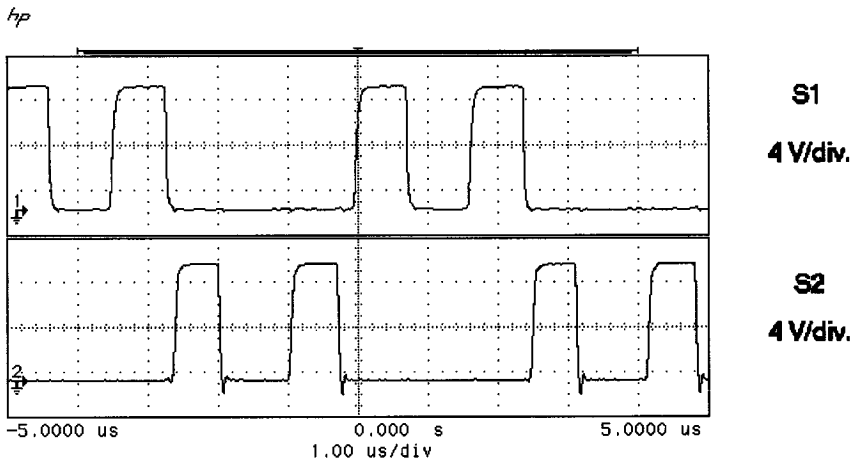


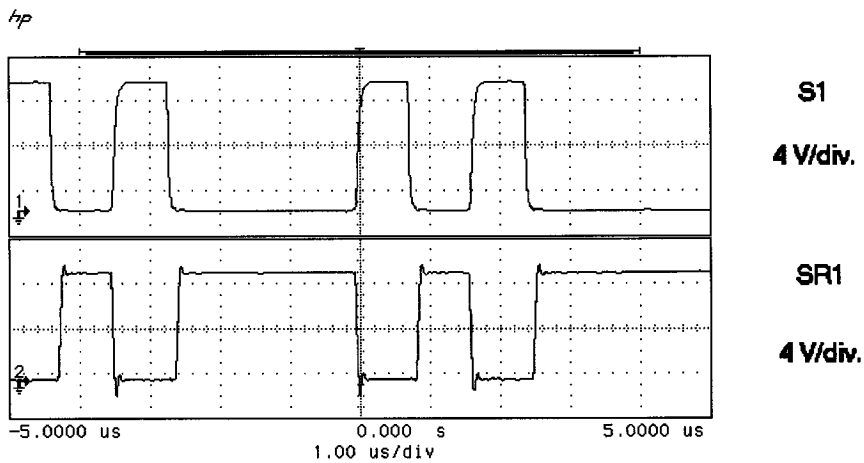
Figure 5.5: Simple ADC Signals Generation Circuitry Implementation

5.3 Experimental Study

A 100W half-bridge prototype with nominal input voltage $V_{in} = 48V$ and output voltage $V_o = 3.3V$ was built in the laboratory for verification and evaluation. The switching frequency per switch was $400kHz$ and with output inductors $L_1 = L_2 = 500nH$. The primary side switches S_1 and S_2 were Si7456DP each. At the secondary side, synchronous rectifiers (SRs) were used, two Si7892DP paralleled in each of the two current doubler channels. The prototype was ADC controlled with equal duty cycles ($m = (1-D)/D$). Figure 5.6 shows some experimental waveforms while Figure 5.7 shows the prototype measured efficiency curve. It can be noticed from Figure 5.6(c) that zero-voltage switching was achieved alternatively between S_1 and S_2.



(a)



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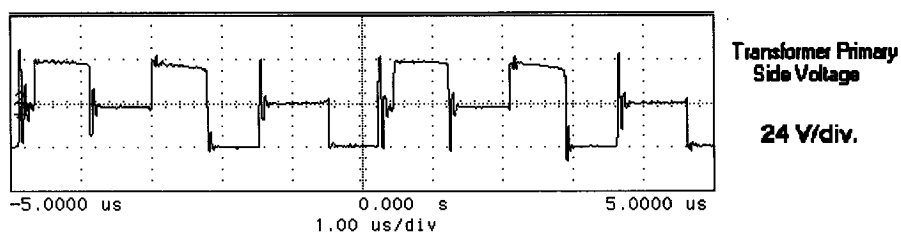

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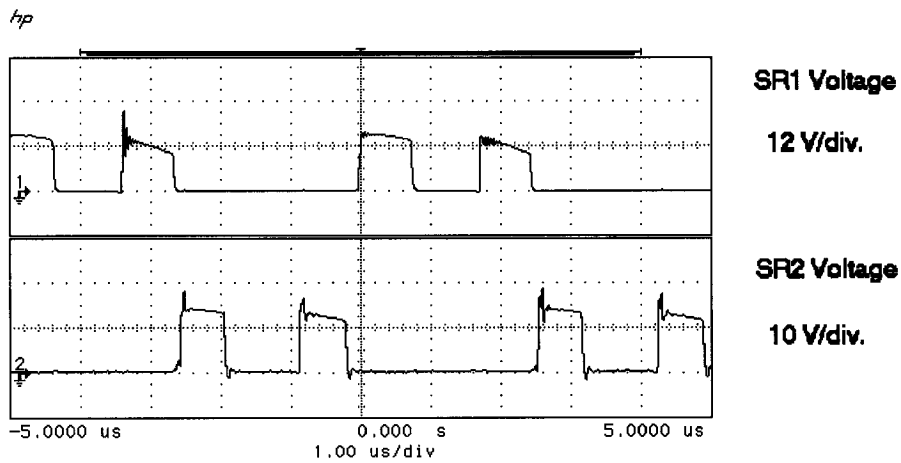


(d)

Figure 5.6: Experimental Waveforms: (a) S_1 and S_2 Driving Signals, (b) S_1 and S_{R1} Driving Signals, (c) Isolation Transformer Primary Voltage and (d) S_{R1} and S_{R2} Voltages.

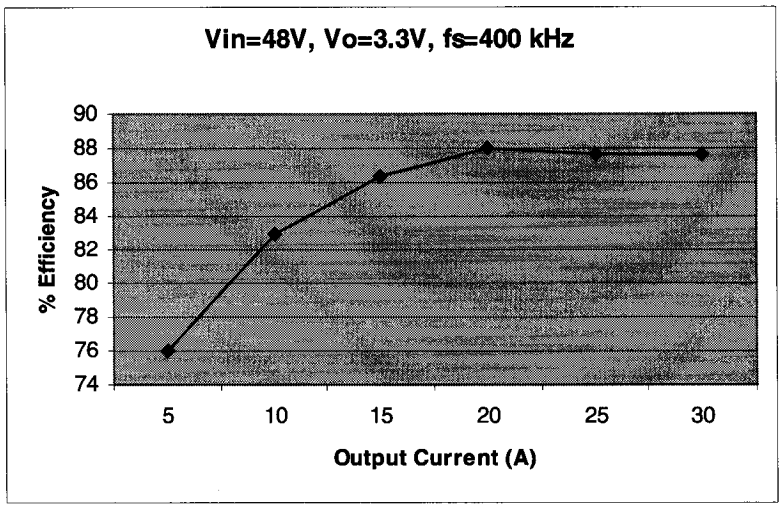


Figure 5.7: Experimental Efficiency Curve

5.4 Summary

A control method, Alternated Duty Cycle (ADC) control, was presented in this chapter. This method can achieve soft-switching for at least one switch of the two half-bridge switches. When soft-switching can be achieved only for one switch, ADC control alternates the soft-switching realization between the two switches so that each switch will be soft-switched for half of the time and hard-switched during the other half, keeping equal power loss distribution between the switches. Moreover, any asymmetry in the duty cycle will not cause asymmetric components stress when ADC control is used.

CHAPTER 6

INTERLEAVED CURRENT DOUBLERS WITH PARALLEL CONNECTED TRANSFORMERS

6.1 Introduction

To improve the transient response, the switching frequency has to be increased and the output inductor has to be decreased, which results in lower converter efficiency and thermal problems.

For both isolated and non-isolated topologies, paralleled synchronous rectifiers are usually used for high-current low-voltage converters. These paralleled rectifiers switch ON and OFF at the same time, which limits the ability to increase the frequency. The interleaving technique uses the same number of rectifiers working at a lower switching frequency in a number of phase-shifted paralleled converter phases, resulting in higher output-ripple frequency and smaller effective output inductance, which improve the transient response and the thermal management.

Interleaved non-isolated buck topology is widely used in 5V - 12V input POL converters or Voltage Regulator Modules (VRMs) where both the input and the output are paralleled [30]. The same method can be applied to isolated topologies where an isolation transformer is used to step-down the high input voltage.

In this chapter, interleaving method for isolated topologies [66] is presented where the secondary side switches operate at a lower switching frequency than the primary side switches to improve the efficiency, since most of the losses are on the secondary side, and to improve transient response. Moreover, in the presented interleaving method, both primary and secondary sides of the isolation transformers are connected in parallel allowing the sharing of currents at both primary and secondary sides [66].

6.2 Transformer's Primary and Secondary Sides Connection Configurations

Given two transformers, there are four possible connection configurations for primary and secondary windings as follows: series-primary series-secondary, parallel-primary series-secondary, series-primary parallel-secondary, and parallel-primary parallel-secondary.

It is clear that to achieve interleaving for the output switches and inductors, the secondary sides have to be connected in parallel, which eliminates the first two connection configurations mentioned above. The third configuration, series-primary parallel-secondary, can be used as presented in [67], resulting in sharing the output current between the transformers' secondary sides but not sharing the primary current at the transformers' primary sides, since primary sides are connected in series and each carries the same current as in the non-interleaved case.

Because as the output load current increases, the input current also increases, it may be more efficient and may attain better thermal management to connect the primary

sides in parallel, as the secondary sides, so that they share the current, which is the fourth connection configuration mentioned above.

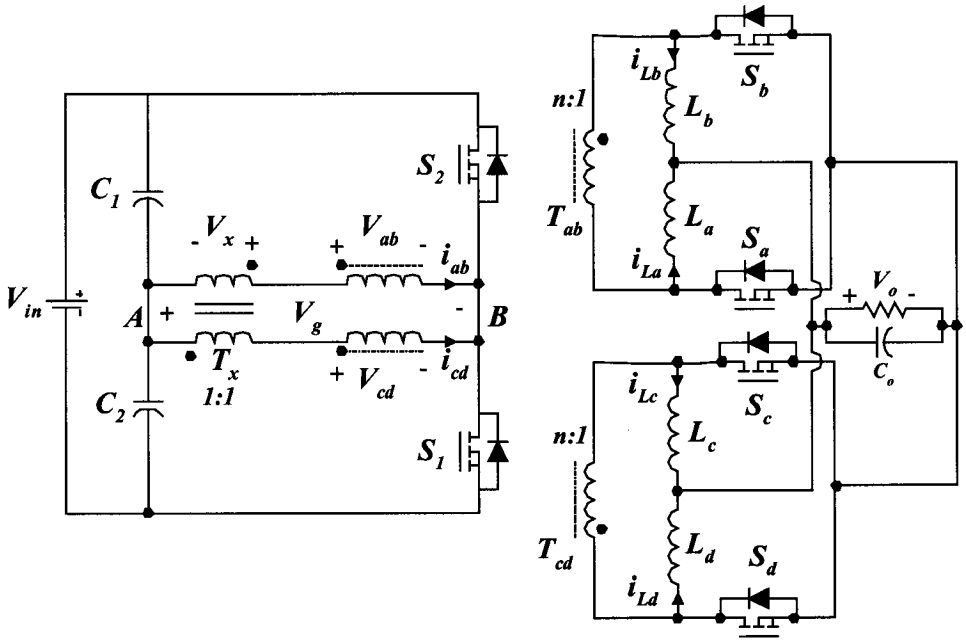
The challenge in the fourth configuration, parallel-primary parallel-secondary, is that when the primary sides are connected in parallel, shorting one primary side will cause the other primary and secondary sides to be shorted also, blocking the interleaving from being achieved for the switches at the output.

This chapter presents how interleaving can be achieved, even when primary sides are connected in parallel, as the secondary sides, resulting in a family of interleaved converters with parallel-connected transformers for both primary and secondary sides.

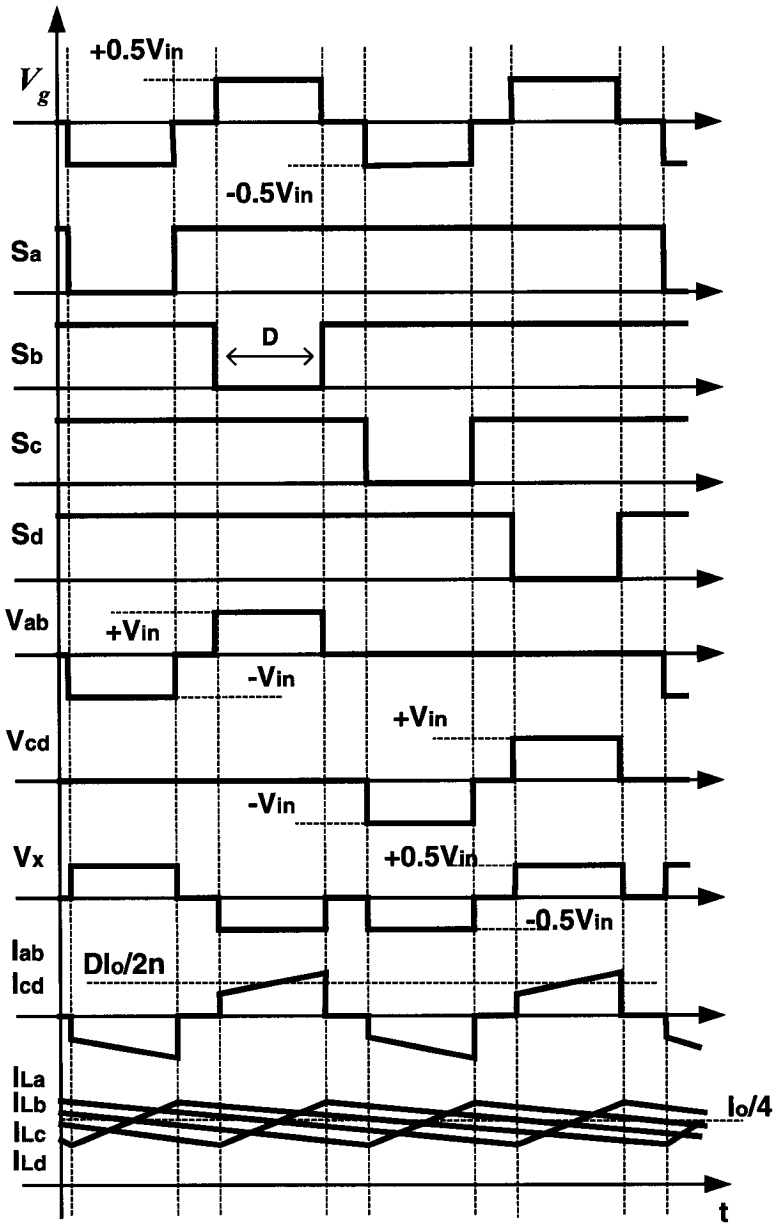
6.3 Topology Configuration

Figure 6.1(a) shows two interleaved current doublers with a half-bridge primary side and with the proposed parallel connected transformers primary and secondary sides. As shown in the figure, a small transformer (T_x) with inverse coupled windings has been added at the primary side to realize the interleaving between the current doublers by transferring the energy between the two paralleled branches. Without T_x, the two paralleled transformers will be shorted together when one current doubler's two channels switches are turned ON at the same time during the freewheeling period.

Figure 6.1(b) shows the main theoretical switching waveforms of the topology of Figure 6.1(a) when conventional symmetric control is used, for example not limitation, since any other control method, hard-switched or soft-switched, can be used. It can be noted that the primary sides currents, i_{ab} and i_{cd}, are half compared to the non-interleaved topology and the series connected primary sides presented in [67].



(a)



(b)

Figure 6.1: (a) Two Interleaved Current Doublers with Half-Bridge Primary Side and Proposed Parallel Connected Transformers Primary and Secondary Sides and (b) Main Theoretical Switching Waveforms

The additional magnetic T_x with 1:1 turns ratio is small and is simple to design for several reasons including: both its windings carry small current (equal to half of the current in its non-interleaved topology), isolation between the two winding is not critical since they are not connected to the secondary side and there is no difficulty in achieving the number of turns since the turns ratio is 1:1.

In addition to the half-bridge primary side, any primary-side topology can be used, including phase-shifted full-bridge and active-clamp, resulting in a new family of converters. Figure 6.2 shows the interleaved topology where any primary side topology can be connected between nodes A and B.

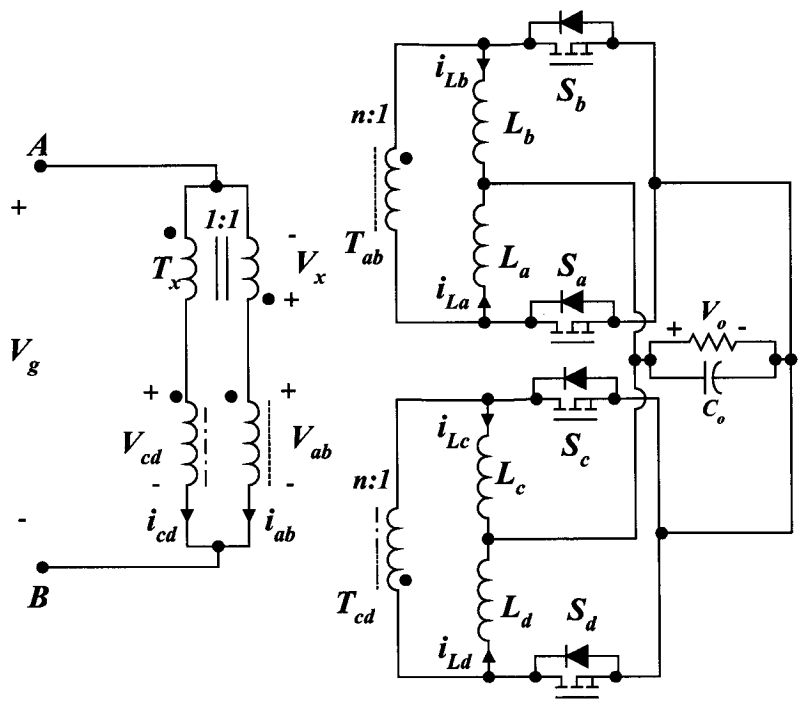


Figure 6.2: Two Interleaved Current Doublers where Any Primary Side can Be Used Including Half-Bridge, Phase-Shifted Full-Bridge and Active-Clamp

6.4 Brief Theoretical Comparison

Both the interleaving and non-interleaving topologies have the same number of switches. However, the switching and reverse recovery body diode losses for the interleaved topology are reduced compared to the non-interleaved topology case especially at higher switching frequencies. This is because the secondary side switching is N times smaller for N interleaved current doublers, which can improve the efficiency [7,67].

In the presented topology of this chapter, the currents at both primary side and secondary side of the isolation transformers are shared, allowing better thermal management as is the case for output inductors.

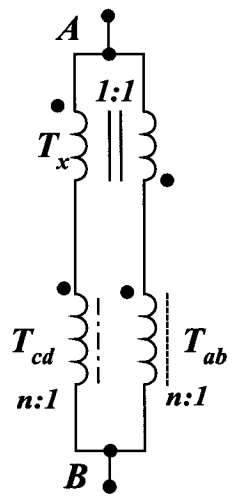
The inductors' output currents are phase shifted (interleaved) by $360°/M$, where $M = 2N$ is the number of output channels. Hence, the current ripple cancels at the output capacitance, which allows smaller capacitance to be used. Moreover, since the effective output inductance is much smaller, the transient performance is improved for the interleaving topology.

6.5 Method Extension for More Interleaved Phases

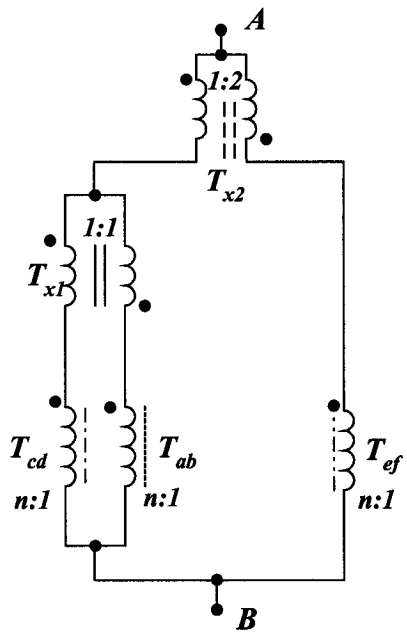
The interleaving method presented in this chapter can be extended to interleave more output channels or current doublers as it was extended for any primary side topology, maintaining shared current at both primary sides and secondary sides of the interleaved transformers.

Considering only the primary side of Figure 6.2 as shown in Figure 6.3(a) for simplicity, the interleaving method can be further extended by adding additional inverse-

coupled transformers or inductors as necessary. For example, Figure 6.3(b) shows the primary side for three interleaved current doublers at the secondary side. Figure 6.3(c) shows the primary side for four interleaved current doublers at the secondary side, where T_{ab}, T_{cd}, T_{ef} and T_{gh} are the isolation transformers, each for one current doubler of the four current doublers (not shown in the figure) where the primary side is only shown and T_{x1}, T_{x2}, and T_{x3} are the inverse coupled transformers for parallel primary and secondary sides' transformers interleaving realization. It is clear that for N interleaved current doublers (2N output channels), N-1 inverse coupled transformers are required. Note that all the inverse coupled transformers have a 1:1 turns ratio when an even number of isolation transformers are interleaved. In the case when an odd number of isolation transformers are interleaved, one inverse coupled transformer turns ratio should be 2:1, as it is the case in T_{x2} of Figure 6.3(b), in order to maintain equal current sharing between the transformers.



(a)



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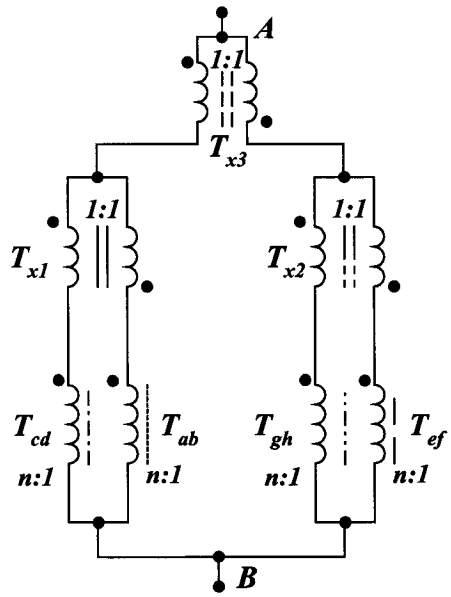


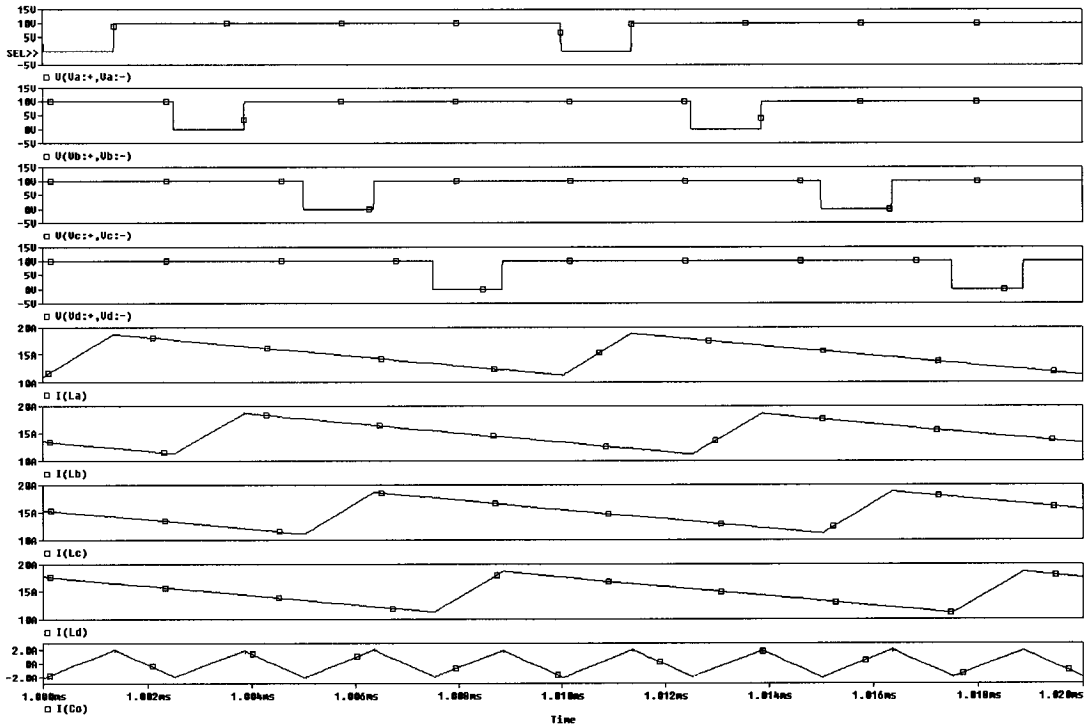
(c)

Figure 6.3: (a) Primary Side for Two Interleaved Current Doublers (Four Output Channels), (b) Primary Side for Three Interleaved Current Doublers (Six Output Channels) and (c) Primary Side for Four Interleaved Current Doublers (Eight Output Channels)

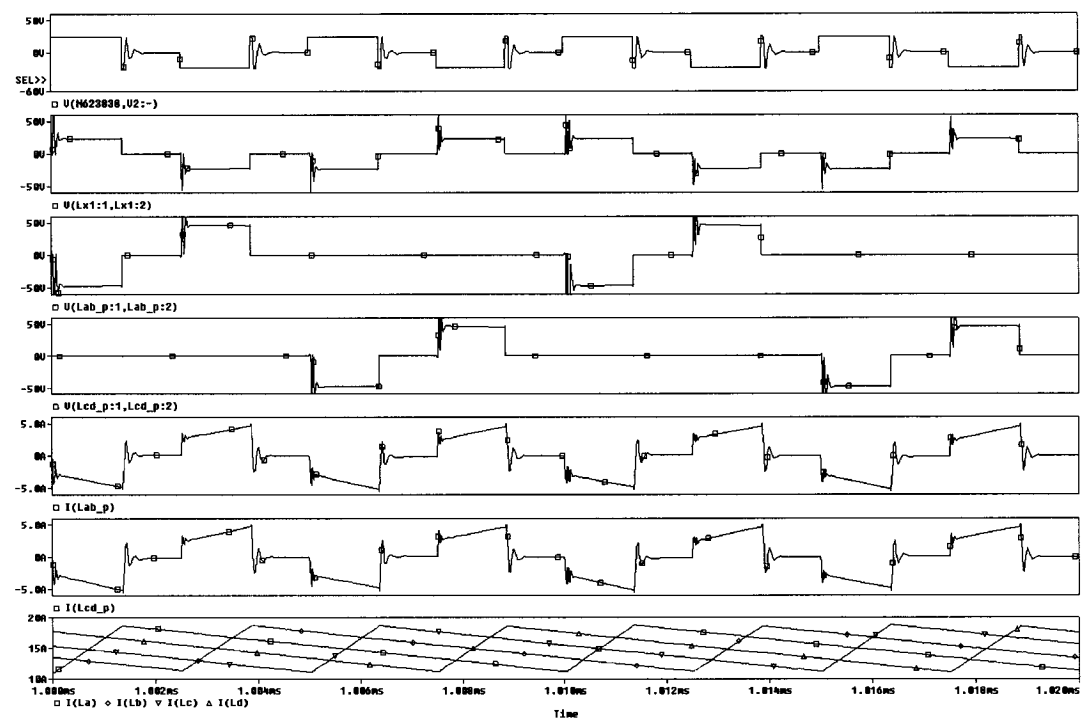
6.6 Simulation Results

An interleaved four-channel (two current doublers) with symmetrically controlled half-bridge, as shown in Figure 5.1, was simulated with 48V input and 1.5V/60A output at 400kHz. The output inductors were $1.8\mu H$ each and the isolation transformers' turns ratio was 4:1. The simulation results are shown in Figures 6.4(a) and 6.4(b). Other simulation results for non-interleaved symmetrically controlled half-bridge with two-channels (one current doubler) also were simulated with the same specifications of 48V input, 1.5V/60A output at 400kHz and$1.8\mu H$ each output inductor, as shown in Figure 6.4(c).

It can be noticed from Figure 6.4 that for the same output ripple frequency, 400kHz, or in other words, the primary side switching frequency (200kHz), the secondary side switches' switching frequency for the two interleaved current doublers, 100kHz, is half compared the non-interleaved single current doubler, 200kHz. It can be noted also that even at the transformers' primary side windings, as is the case at the secondary side windings, the current is half for the interleaved topology compared to the non-interleaved topology because of the parallel connection. Moreover, the current in each inductor is also half compared to the non-interleaved topology, or in other words, it is quarter of the total output current.



(a)



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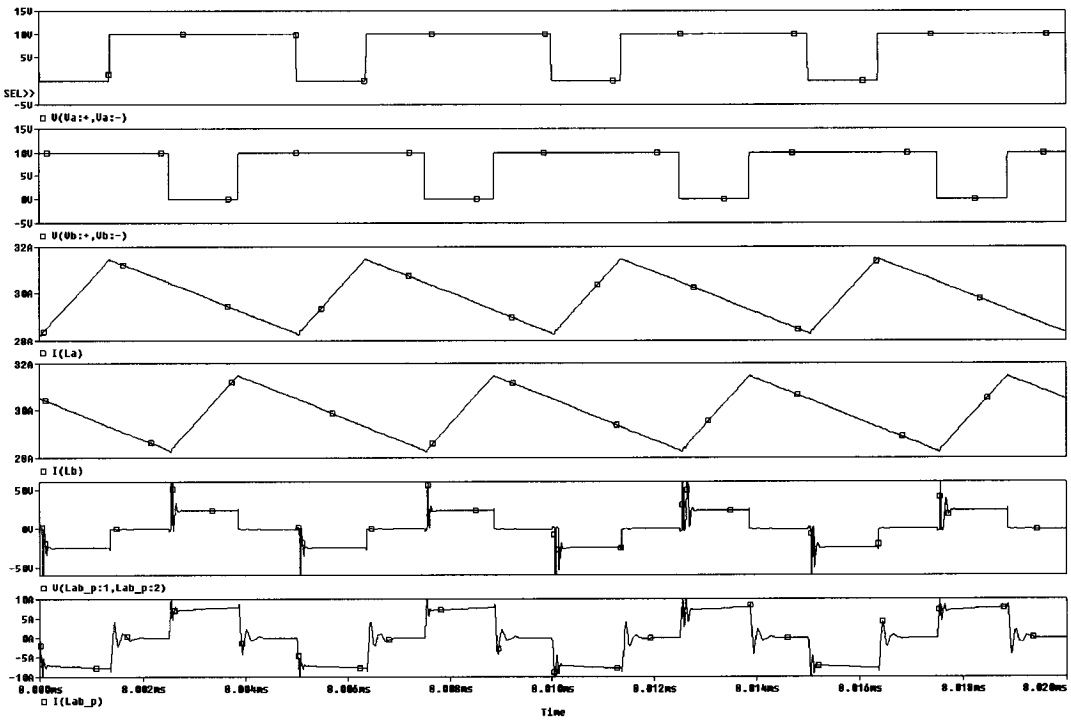


(c)

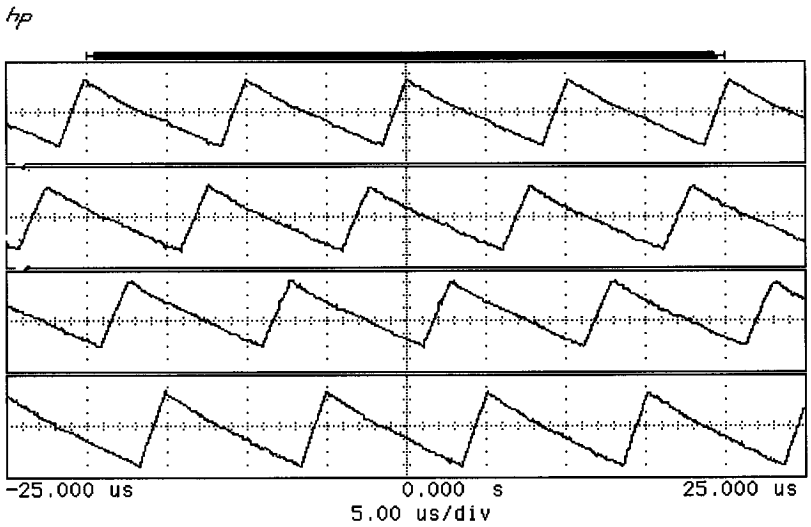
Figure 6.4: Simulation Results: (a) and (b) for Interleaved Topology with Two Current Doublers Secondary Side and Half-Bridge Primary Side and (c) for Non-Interleaved Topology with One Current Doubler Secondary Side and Half-Bridge Primary Side

6.7 Experimental Work

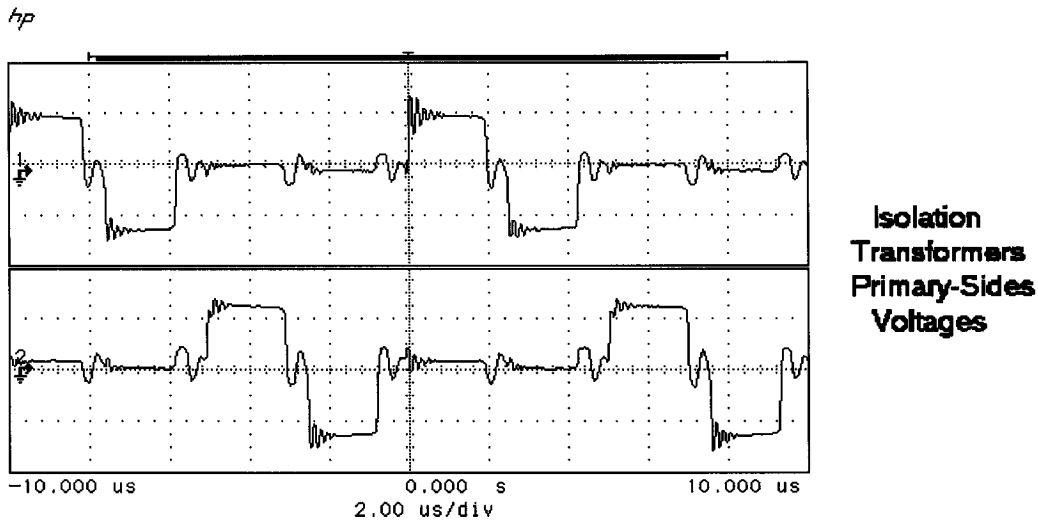
An interleaved four-channel (two current doublers) with symmetrically controlled half-bridge (primary) prototype, as in Figure 6.1, was built in the laboratory for experimental verification with 48V input and 1.5V/60A output at 400kHz. The output inductors where $1.8\mu H$ each and the isolation transformers' turns ratio was 4:1.

Figure 6.5(a) shows the experimental results for four interleaved inductors currents, Figure 6.5(b) shows the two isolation transformers' primary side voltages, Figure 6.5(c) shows one isolation transformer primary side voltage and one side voltage

of the inverse coupled transformer, while Figure 6.5(d) shows the primary side isolation transformers' winding currents. It can be noted that the experimental results of Figure 6.5 agree with the theoretical and simulation results.



(a)



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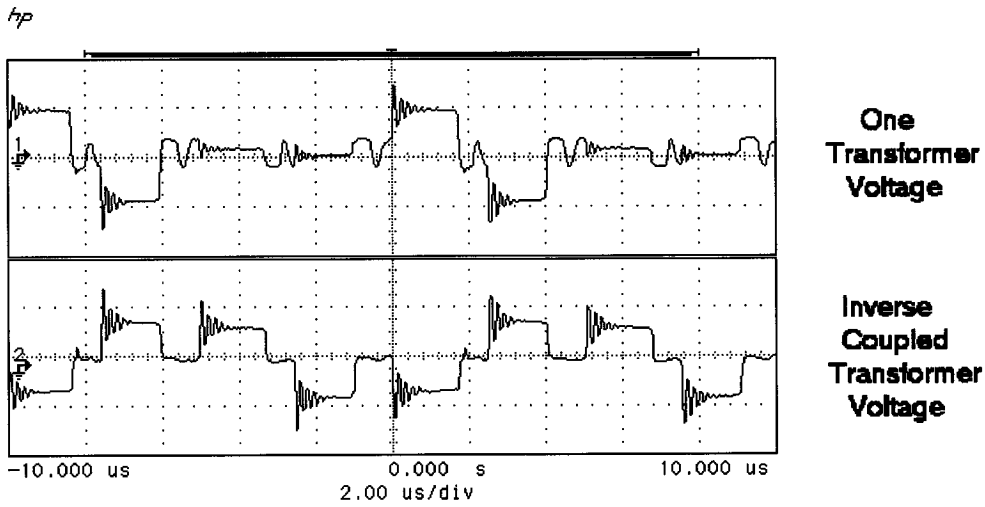

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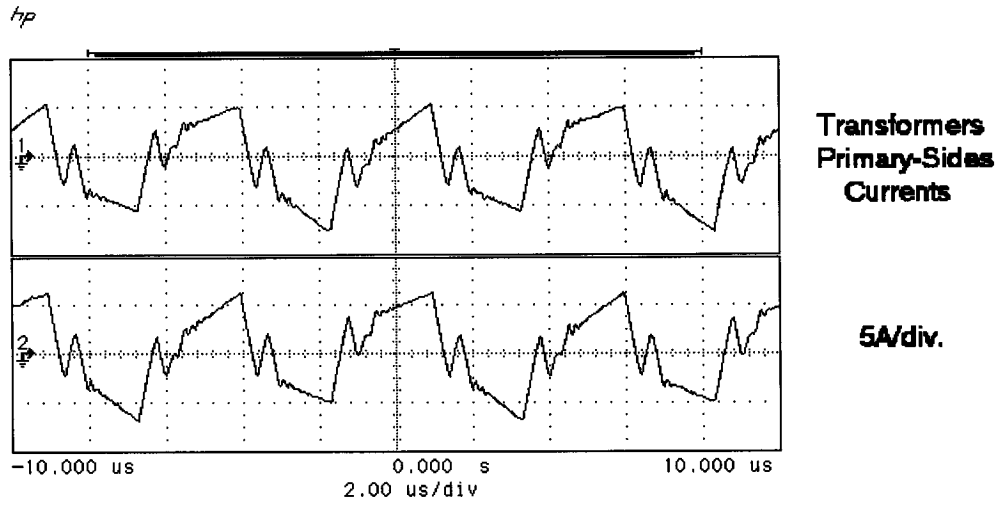


(d)

Figure 6.5: Experimental Waveforms for: (a) Four Interleaved Inductors Currents, (b) Four Two Isolation Transformers Primary Side Voltages, (c) One Isolation Transformer Primary Side Voltage and One Side Voltage of the Inverse Coupled Transformer and (d) the Primary Side Isolation Transformers Two Winding Currents

6.8 Summary

Interleaving method for isolated topologies was presented in this chapter, where the secondary side switches operate at a lower switching frequency than the primary side switches to improve the efficiency and to improve transient response. Moreover, in the proposed interleaving method, both primary and secondary sides of the isolation transformers are connected in parallel, which allows the sharing of currents at both primary and secondary sides. Principle of operation and potential advantages of the presented method were discussed, and simulation and experimental results were presented.

CHAPTER 7

COUPLED-INDUCTORS CURRENT-DOUBLER DC-DC CONVERTER TOPOLOGY

7.1 Introduction

As the required output voltages become smaller and the input voltages become larger, the voltage step-down ratio becomes larger, which means larger isolation transformer turns ratio in isolated converters or smaller switching duty cycle in non-isolated converters. A smaller duty cycle results in higher input peak current (higher input *rms* current) and larger asymmetric transient response. Moreover, lower output voltage converters require tight regulation, which necessitates lower output current and voltage ripples.

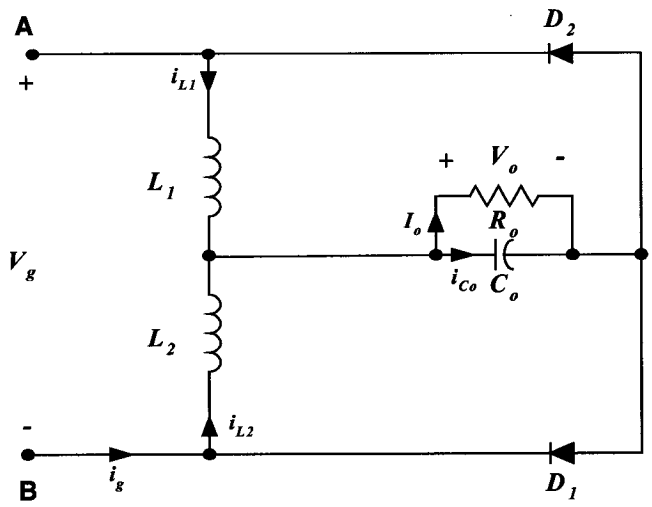
As the required output current increases, the isolation transformer secondary winding current becomes larger, which increases the winding losses and results in a thermal problem that may block the ability to reduce the transformer size required to achieve higher density.

Current-doubler secondary side scheme is preferred in many applications, owing to its advantages including current ripple cancellation, higher current capability, doubled output current and voltage ripple frequency compared to its switches' switching frequency and lower rectification and conduction losses [4].

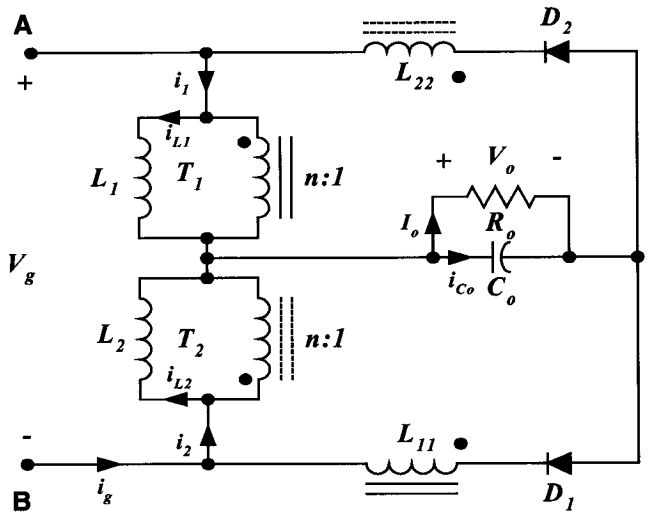
However, there are other characteristics that are preferred for the current-doubler to have when used in low-output voltage, high-output current DC-DC converters with higher input voltages. These characteristics include: lower output current ripple without greatly increasing the switching frequency to achieve lower output voltage ripple with the smallest output capacitance, lower output voltage without decreasing the duty cycle or increasing the isolation transformer turns ratio (larger step-down capability), lower input current, and can be designed to achieve symmetric transient response at both step-up and step-down transients, which is preferred in the Adaptive Voltage Positioning (AVP) technique used to reduce the output capacitance required for certain transients maximum output voltage deviation [84-86]. Aiming to achieve such characteristics, a new Coupled-Inductors Current-Doubler (CICD) topology [68] is presented in this chapter.

7.2 CICD Topology and Its Waveforms

Figure 7.1(a) shows the conventional current doubler (CCD) topology while Figure 7.1(b) shows the Coupled-Inductors Current-Doubler (CICD) topology presented in this chapter. As shown in Figure 7.1(b), the inductor L_1 is coupled with another inductor, L_{11}, in series with the diode D_1 with a turns ratio $n:1$, where $n>1$, and the inductor L_2 is coupled with another inductor, L_{22}, in series with the diode D_2 with the same turns ratio. Of course, D_1 and D_2 can be replaced with synchronous rectifiers if required, especially for low output voltage applications.



(a)



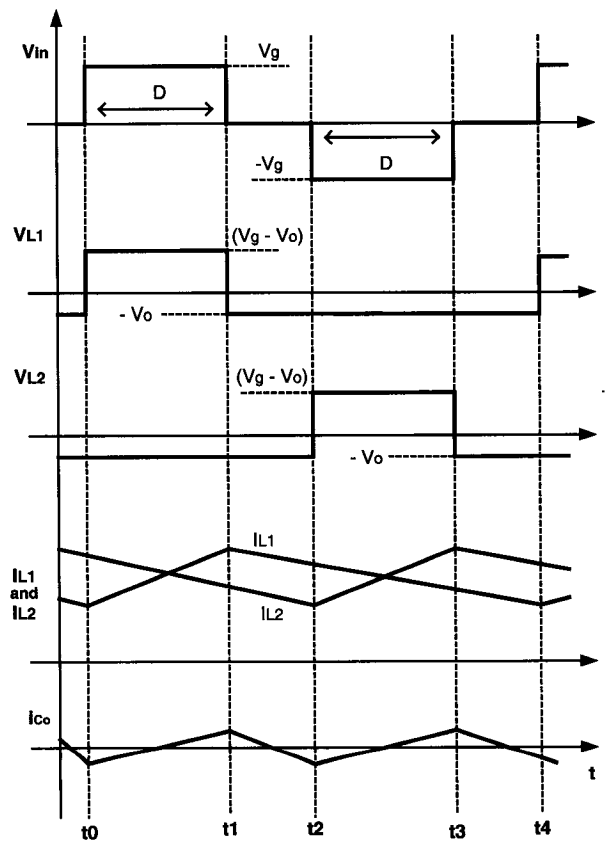
(b)

Figure 7.1: Current-Doubler Topologies: (a) Conventional Current-Doubler (CCD) and (b) Coupled- Inductor Current-Doubler (CICD)

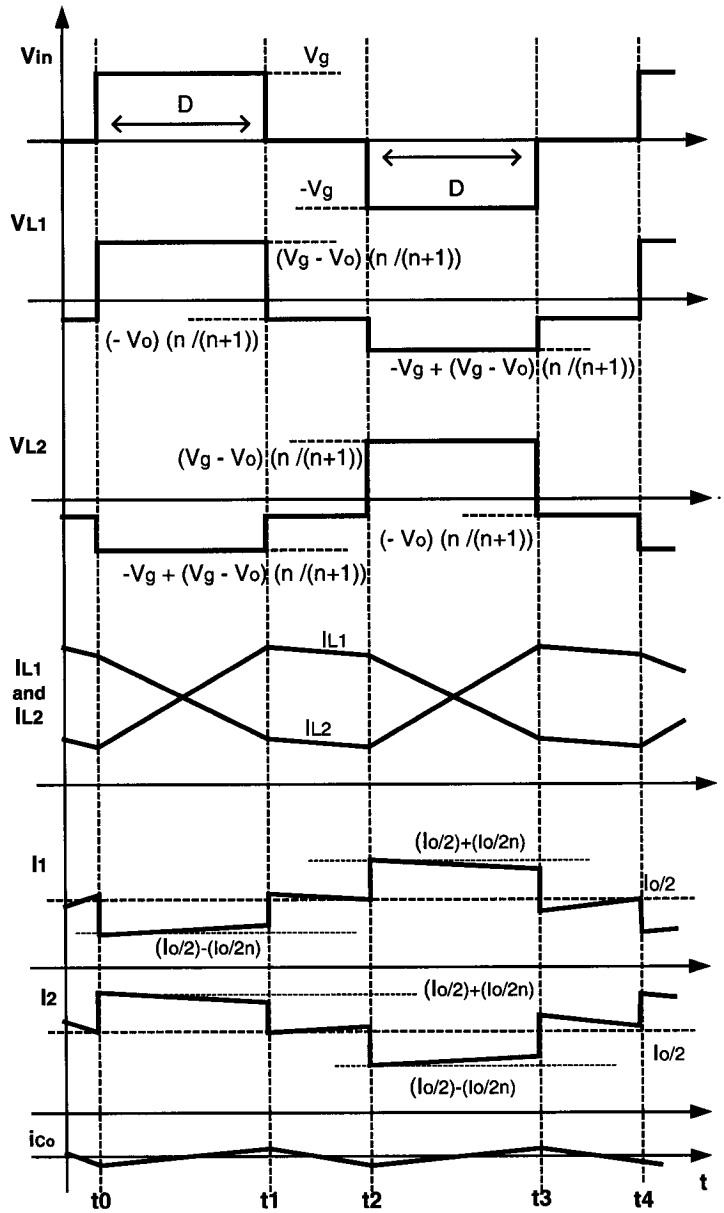
Assuming that the coupling coefficient k is equal to one, the coupled inductors turns ratio, n, is defined as:

$$n = \sqrt{\frac{L_1}{L_{11}}} = \sqrt{\frac{L_2}{L_{22}}} > 1,\ L_1 = L_2 = L,\ L_{11} = L_{22} \tag{7.2.1}$$

Figure 7.2(a) shows the ideal main switching waveforms of the CCD topology, while Figure 7.2(b) shows the main switching waveforms of the proposed CICD topology when symmetric control scheme is used. The coupling configuration of the CICD of Figure 7.2(b) causes the shape of the voltage across L_1 and L_2 to change from the shape of Figure 7.2(a) of the CCD to the shape of Figure 7.2(b) of the CICD. This coupling causes the currents through L_1 and L_2 to be re-shaped also, as shown in the figure, and to have more intend to cancel.



(a)



(b)

Figure 7.2: Current-Doubler Topologies Ideal Main Switching Waveforms: (a) Conventional Current-Doubler (CCD) Waveforms and (b) Proposed Coupled-Inductor Current-Doubler (CICD) Waveforms

7.3 Theoretical Analysis and Key Design Equations

Based on Figures 7.1 and 7.2, theoretical analysis and key design equations are presented here as follows:

A. Gain Equation:

By applying the volt-second balance across the inductors, the gain equations for the proposed CICD topology and the conventional CCD topology can be derived as follows:

$$\frac{V_o}{V_g} = \frac{n-1}{n} D,\ n > 1 \quad \text{(CICD Topology Gain Equation)} \tag{7.3.1}$$

$$\frac{V_o}{V_g} = D \quad \text{(CCD Topology Gain Equation)} \tag{7.3.2}$$

Figure 7.3(a) shows the additional voltage step-down ratio resulting from the coupling, or in other words, the ratio between Equations (7.3.1) and (7.3.2). It can be noticed that larger voltage step-down is achieved as n decreases and becomes closer to 1. When $n = 1$, the output voltage becomes zero. Larger duty cycle can be achieved in the case of the CICD compared to the CCD, assuming the same V_g.

B. Output Current Ripple Equation:

From Figure 7.2, and by using the slope of the currents' step-up and step-down of the inductors, the output current ripple equations can be derived as:

$$\Delta i_{co-CICD} = \frac{n^2 V_o}{V_g (n^2-1)\cdot(n+1)} \cdot \frac{(n-1)V_g - 2nV_o}{L \cdot f_s} = \left[\frac{n}{n+1}\right]^2 \cdot (1-2D) \cdot \frac{V_o}{L \cdot f_s} \quad \text{(CICD Topology Output Current Ripple)} \tag{7.3.3}$$

$$\Delta i_{co-CCD} = \frac{V_o}{V_g} \cdot \frac{V_g - 2V_o}{L \cdot f_s} = (1-2D) \cdot \frac{V_o}{L \cdot f_s} \qquad \text{(CCD Topology Output Current Ripple)}$$

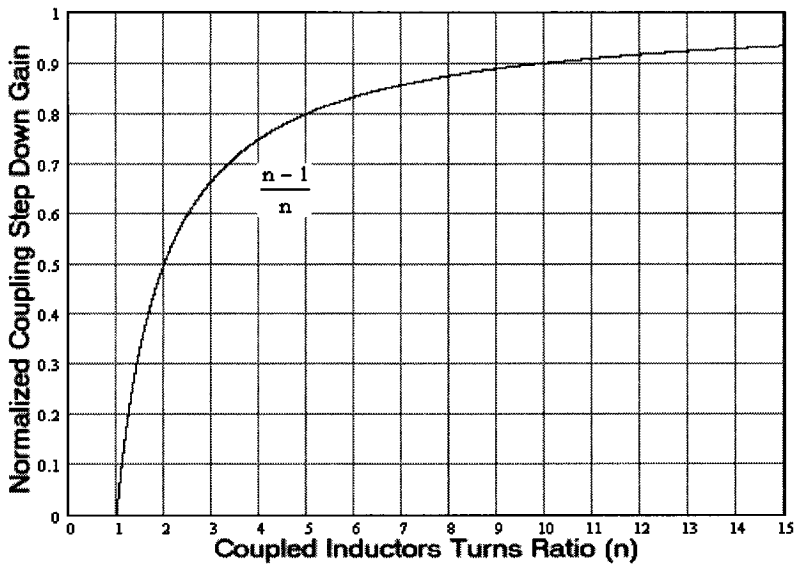
(7.3.4)

where: f_s is the switching frequency.

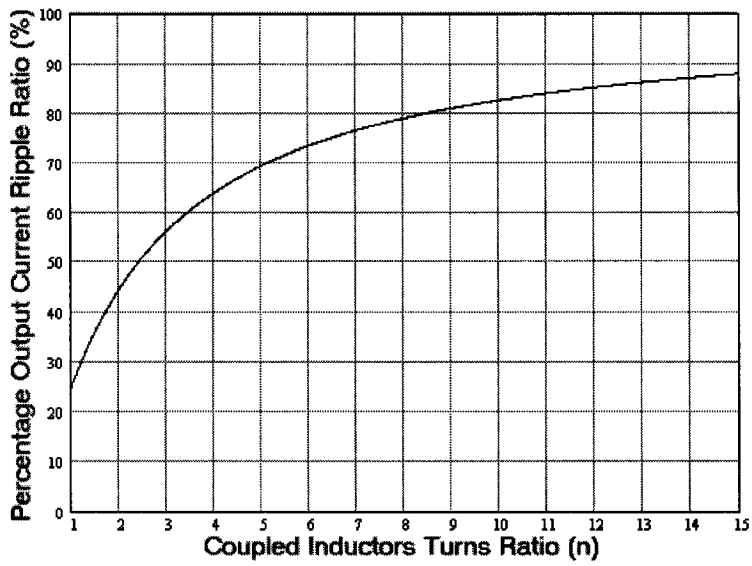
A way to compare Equations (7.3.3) and (7.3.4) is to take the ratio between them to yield,

$$\frac{\Delta i_{co-CICD}}{\Delta i_{co-CCD}} = \left[\frac{n}{n+1}\right]^2 \qquad n > 1 \qquad (7.3.5)$$

Figure 7.3(b) shows the plot of Equation (7.3.5) versus n, i.e., the output current ripple ratio between the CICD and the CCD topologies. As it is evident from the figure, the CICD current ripple decreases compared to the conventional CCD as n becomes smaller. For example, when $n = 2$, the CICD output current ripple is about 45 percent of that for the CCD topology. Therefore, even though the current ripple of each separate inductor is larger for the CICD compared to the CCD, the total output current is smaller.



(a)



(b)

Figure 7.3: (a) Normalized Coupling Step-Down Voltage Gain and (b) Percentage Output Current Ripple Ratio Versus the Turns Ratio n

C. Input Voltage and Input Current:

As shown in Equations (7.3.1) and (7.3.2), to keep the identical design for the same output voltage and output current at the same duty cycle for both the CICD topology and CCD topology, the input voltage V_{g-CICD} of the CICD topology should be larger than the input voltage V_{g-CCD} of the CCD topology as follows:

$$V_{g-CICD} = \frac{n}{n-1} \cdot V_{g-CCD} \qquad n > 1 \qquad (7.3.6)$$

Therefore, the input current i_{g-CICD} of the CICD topology is smaller than the input current i_{g-CCD} of the CCD topology as follows:

$$i_{g-CICD} = \frac{n-1}{n} \cdot i_{g-CCD} \qquad n > 1 \qquad (7.3.7)$$

This current is the secondary side current of the isolation transformer when isolated topology is used with any primary side such as half-bridge and full-bridge. Therefore, the isolation transformer secondary-side current is lower for the CICD topology, which can reduce the secondary-side winding losses especially for high output currents.

D. Switches' Voltage and Current Stresses:

The voltage stress on the conventional and proposed current doublers switches can be obtained by applying KVL for the loop, which include one of the switches, and yields:

$$V_{switch-CICD} = V_{g-CICD} \cdot \frac{n-1}{n} = \frac{V_o}{D}, \qquad n > 1$$

(CICD Topology Switch Voltage Stress) (7.3.8)

$$V_{switch-CCD} = V_{g-CCD} = \frac{V_o}{D}$$

(CCD Topology Switch Voltage Stress) (7.3.9)

By comparing Equations (7.3.8) and (7.3.9) to Equation (7.3.6), which governs the relationship between V_{g-CCD} and V_{g-CICD}, it is apparent that the voltage stress across the switches of both the CCD topology and the CICD topology is identical for the same output voltage and design.

For the same output current, the current stresses for both the CCD topology and the CICD topology switches are also the same since the full load current (I_o) will flow through one of the switches that is turned ON when the other switch is turned OFF.

7.4 Comparison Between the CICD and CCD Topologies and Design Considerations

As was shown earlier in this chapter, a larger output voltage step-down ratio can be achieved by the proposed CICD topology compared to the conventional CCD topology. Moreover, the output current ripple is reduced in the CICD topology.

It must be noted that even though in CCD topology the ripple can be reduced as D becomes closer to 0.5, in practical designs D is not designed to be equal to 0.5 for several reasons. These reasons include being able to have a regulation band (band to change D) when input or output disturbances occur and not to create short circuit condition by overlapping the switches' ON times. On the other hand, in the case of the proposed CICD topology, for any value of D, a smaller ripple can be achieved by choosing the appropriate inductors coupling turns ratio n. Symmetric transient response

can be also achieved for the CICD topology by choosing the appropriate n value to make the output current step-up slope and step-down slope equal.

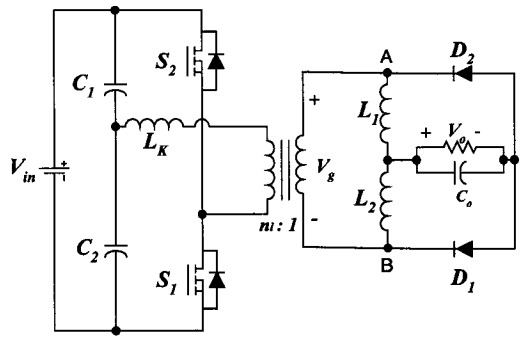
Even for the same output voltage and current, larger input voltage and smaller input current is required in the CICD case. It was shown that the switches' voltage and current stresses did not change from the CICD topology to the CCD topology. In fact, since the CICD input current, which is the isolation transformer secondary-side current in isolated topologies, is smaller, the conduction loss may be smaller and the transformer secondary winding required diameter will be smaller. Moreover, since part or all of the voltage step-down is achieved by the coupled inductors of the CICD, less isolation transformer primary turns are needed. Therefore, smaller isolation transformer size may be achieved.

Even though the coupling coefficient k of the coupled inductors should be designed as close as possible to one, and with minimum leakage inductance, to achieve better performance in the CICD topology, a small leakage inductance still exists in practical designs. This leakage inductance should be designed as small as possible for better performance. When this leakage inductance is very small, it can be utilized toward achieving soft switching for the primary side switches in addition to the isolation transformer-leakage inductance. It may also reduce the switches' reverse recovery losses by reducing the di/dt [69].

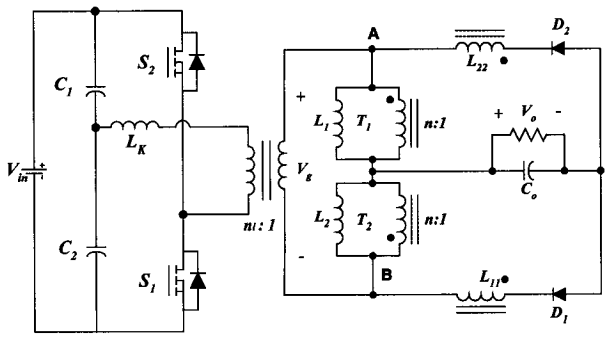
7.5 Simulation Results

Both the CCD and CICD topologies secondary side, as shown in Figure 7.4, were simulated using Pspice/Orcad to verify the theoretical results. Input and output voltages

for both simulations were $V_{in} = 36V \sim 75V$ and $V_o = 3.3V$, respectively, at full load current $I_o = 20A$. The switching frequency of $f_s = 300KHz$ was used. To achieve the same range of duty cycle ($D = 0.3 \sim 0.35$) at the nominal input voltage of $V_{in} = 48V$ for both topologies, the isolation transformer turns ratio for the conventional CCD simulation schematic was $n_i = 2$ and $n_i = 1$ in the proposed CICD simulation schematic, while the step-down is achieved by the coupled inductors' turns ratio being equal to $n = 2$. Another design value is the inductor value $L = 3\mu H$. Figures 7.5(a) and 7.5(b) show the simulation waveforms for the CCD and the CICD cases, respectively. It can be noticed that these waveforms agree with the theoretical results for the voltage step-down, current ripples and voltage and current stresses.

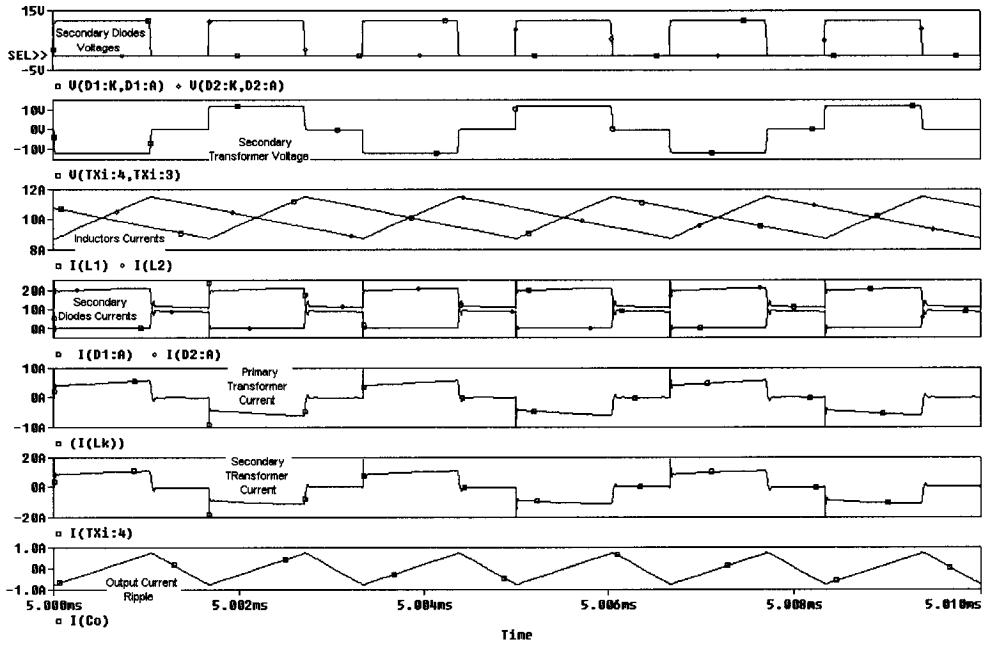


(a)

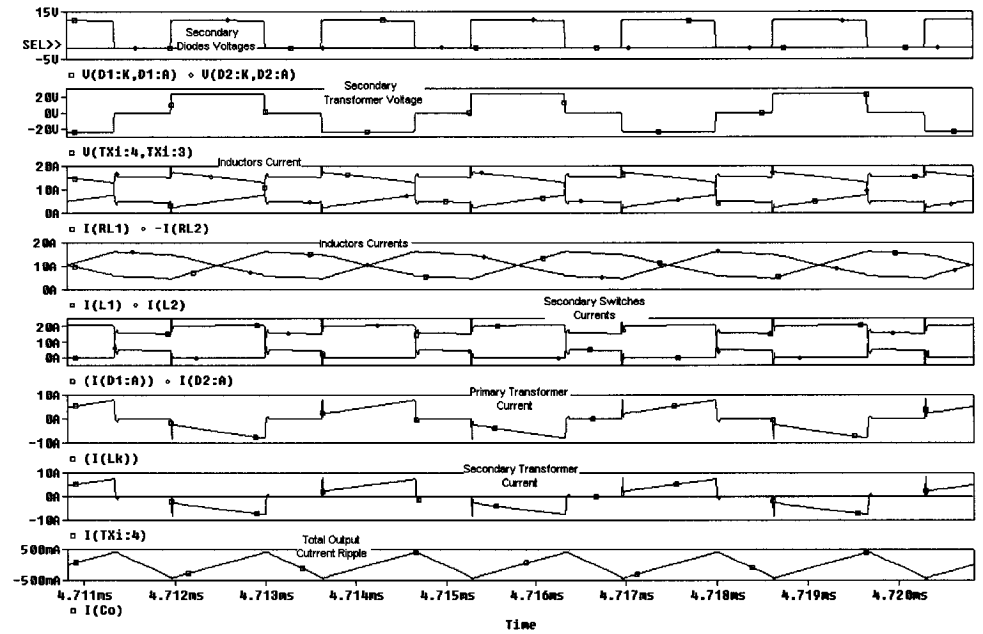


(b)

Figure 7.4: Isolated Half-Bridge Topology With: (a) CCD Topology and (b) CICD Topology



(a)



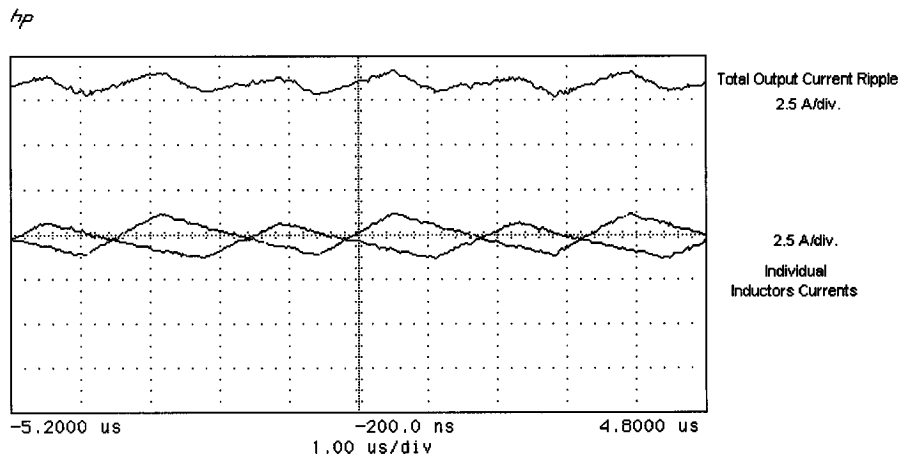
(b)

Figure 7.5: Simulation Results for: (a) The Conventional CCD Topology and (b) The CICD Topology

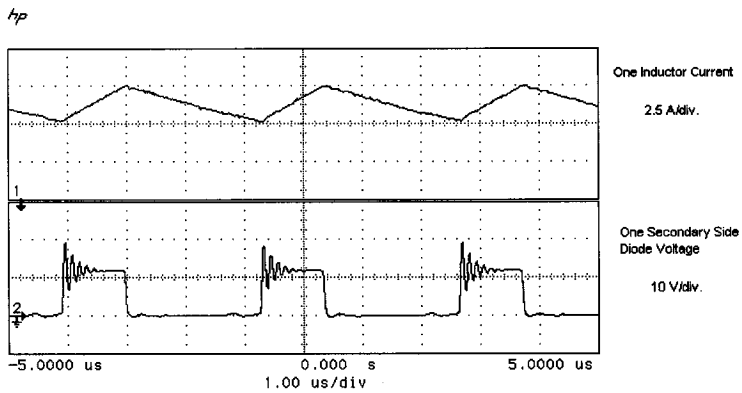
7.6 Experimental Study

Two half-bridge prototypes, with the CCD and CICD topologies secondary side as shown in Figure 7.4, were built in the laboratory to verify the theoretical and simulation results. Input and output voltages for both prototypes were $V_{in} = 36V \sim 75V$ and $V_o = 3.3V$, respectively, at full load current $I_o = 20A$. The switching frequency was equal to $f_s = 300KHz$. To achieve similar range of duty cycle ($D = 0.3 \sim 0.35$) at the nominal input voltage of $V_{in} = 48V$, the isolation transformer turns ratio for the conventional CCD prototype was $n_i = 2$ and $n_i = 1$ in the CICD prototype. The step-down is achieved by the coupled inductors turns ratio that is equal to $n = 2$. The inductor value was designed for $L = 3\mu H$.

Figures 7.6 and 7.7 show the experimental waveforms for the CCD and CICD cases, respectively. The results show that these waveforms agree with the theoretical results for the voltage step-down, current ripples and voltage and current stresses. However, because the values of the leakage inductances for the coupled inductors in the CICD topology are not easily controlled in the laboratory, the CICD individual inductor current waveforms look slightly different from the theoretical waveforms. Leakage inductance should be reduced to achieve better results. This can be done by using planner magnatics.

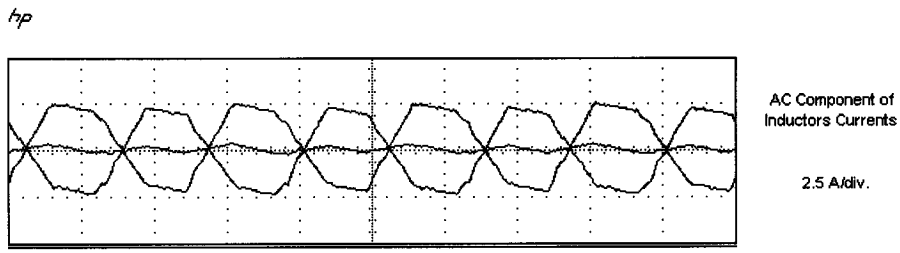


(a)

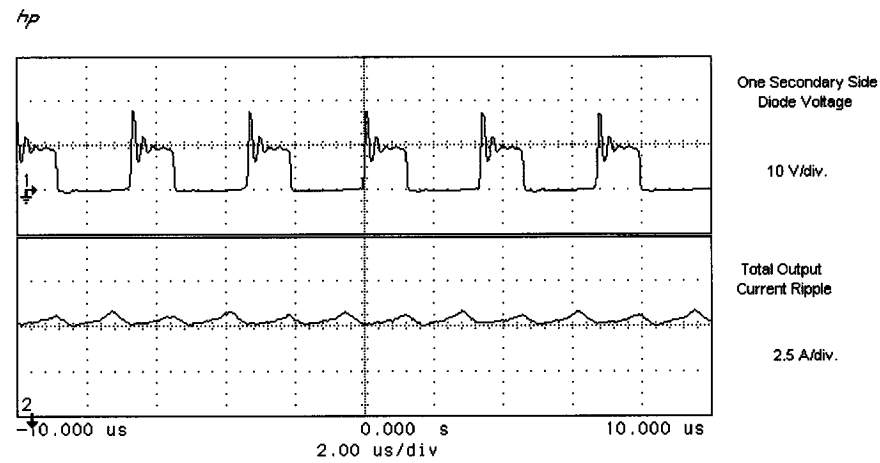


(b)

Figure 7.6: Experimental Waveforms with the CCD Topology: (a) Inductors and Output Currents Waveforms and (b) One Inductor Current and One Secondary Side Diode Voltage Waveforms



(a)



(b)

Figure 7.7: Experimental Waveforms with the CICD Topology: (a) Inductors Currents Waveforms and (b) Output Current and One Secondary Side Diode Voltage Waveforms

7.7 Summary

Coupled-Inductors Current-Doubler (CICD) topology was presented in this chapter that has many advantages over the Conventional Current-Doubler (CCD) topology. These advantages include higher voltage step-down ratio suitable for lower output voltages, smaller current doubler input current (smaller isolation transformer secondary winding current), better current ripple cancellation, smaller isolation transformer turns ratio and lower secondary turns current when used in isolated topology.

CICD can also be designed to achieve symmetric transient response at both step-up and step-down transients when used in non-isolated topology as will be shown in the next chapter.

CHAPTER 8

NON-ISOLATED MULTIPHASE HALF-BRIDGE-BUCK TOPOLOGY WITH INHERENT CURRENT SHARING CAPABILITY AND SOFT SWITCHING

8.1 Introduction

Unfortunately, most of the non-isolated buck-derived topologies work at hard switching, which degrades efficiency, especially at high switching frequency, that is preferred to achieve higher power density, lower ripple and faster transient response. If there is no requirement for isolation, the buck converter is the simplest topology for realizing step-down DC-DC conversion [24,68,70,71].

Considering the 5V/12V input voltage applications where non-isolated multiphase buck topology is usually used [3,4,24,30,35,41,56,59,60,68,70,71], when the output voltage is small compared to the input voltage, the switching duty ratio is very small, resulting in larger current ripple, higher input current peak and larger asymmetry in the transient response. Moreover, switches in most of these topologies work at hard switching.

Interleaved buck topologies were presented in the literature [7,30,59,60]. Those topologies still do not solve the small duty cycle and hard-switching problems and are

very sensitive to phases' asymmetry, for example when the switches and/or inductors traces or self resistances are not equal, they require a high-performance current-sharing loop to maintain equal current sharing between the phases [30,59,60].

In this chapter, a non-isolated multiphase Half-Bridge-Buck (HBB) topology is presented [68,70]. This topology makes it possible to achieve soft-switching and works at larger switching duty cycle with lower output voltages, and HBB does not require current sharing loop because of its inherent current sharing capability.

8.2 Topology and Possible Control Schemes

Figure 8.1 shows the presented HBB configuration for two phases. C_1 and C_2 are filter capacitors that each carry almost constant voltage equal to half of the input voltage V_{in} when the switches are driven symmetrically. Hence, the voltage applied between nodes A and B, V_{AB}, is equal to half of the input voltage when either S_1 or S_2 is ON. The inductor L_r is a small resonant inductor added for soft switching by utilizing the switches' junction capacitance when a soft-switching control method, such as complementary (asymmetric) control, is used. L_1 and L_2 are the two phase filter inductors and D_1 and D_2 are diodes that can be replaced by synchronous rectifiers. When S_1 is turned ON, D_1 is ON also; when S_2 is ON, D_2 is ON also.

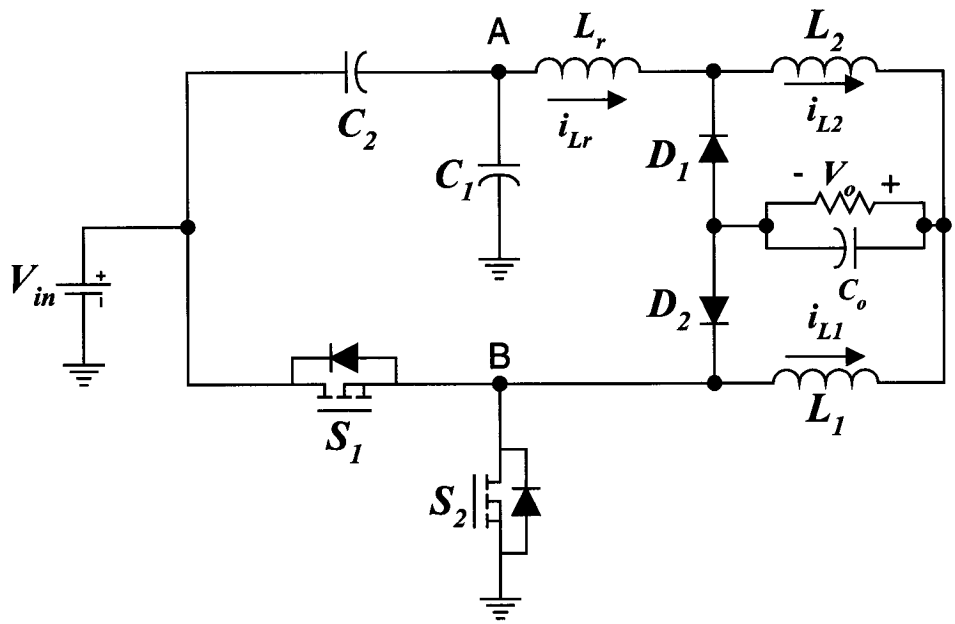


Figure 8.1: Half-Bridge-Buck (HBB) Converter

S_1 and S_2 can be driven by several control methods such as conventional symmetric control [72], complementary or asymmetric control [47] and DCS Control [51-53], which was presented in Chapter 4. Complementary control will be used as an example to illustrate and discuss the topology modes of operation especially that soft switching can be achieved when using this control method. Actually, in the 12V/5V applications, complementary control is a good candidate, since the input voltage variation is relatively small such as 11V~12.6V. Moreover, asymmetrically driven converters have usually lower conduction losses [47], which is important in some applications such as high-current applications.

Figure 8.2 shows the theoretical main switching waveforms of Figure 8.1 converter when complimentary control is used.

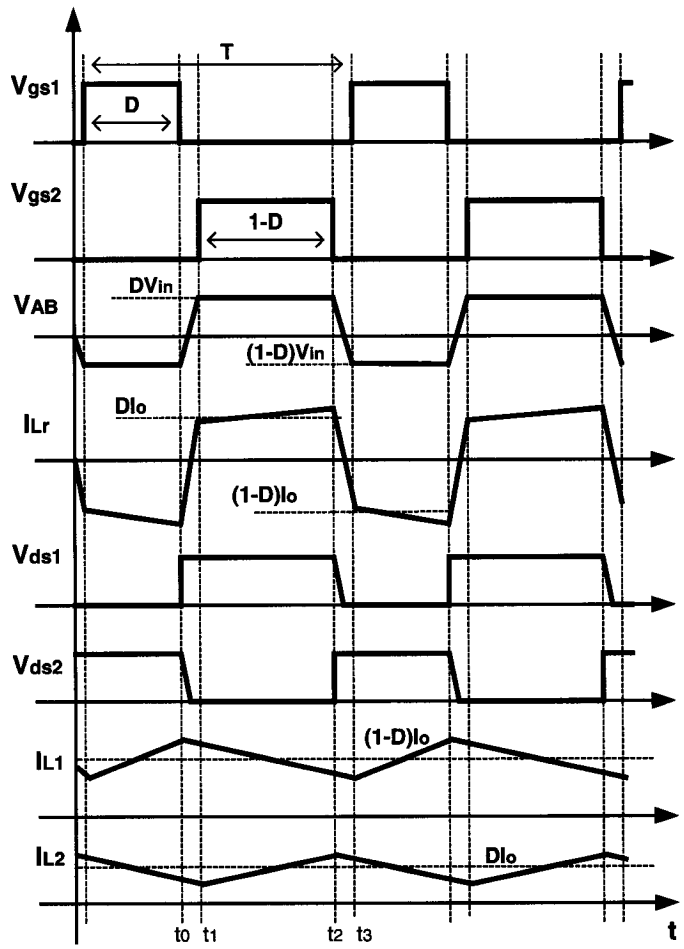


Figure 8.2: Main Switching Waveforms of Figure 8.1 when Complementary Control Is Used

The price of achieving soft-switching and low-output current ripple with lower conduction loss when complementary control is used is the increase of the asymmetric components' stresses as the output voltage decreases for the same input voltage. Using symmetric control, this drawback can be avoided at the expense of losing the soft-switching operation. Figure 8.3 shows the theoretical main switching waveforms of Figure 8.1 converter when symmetric control is used.

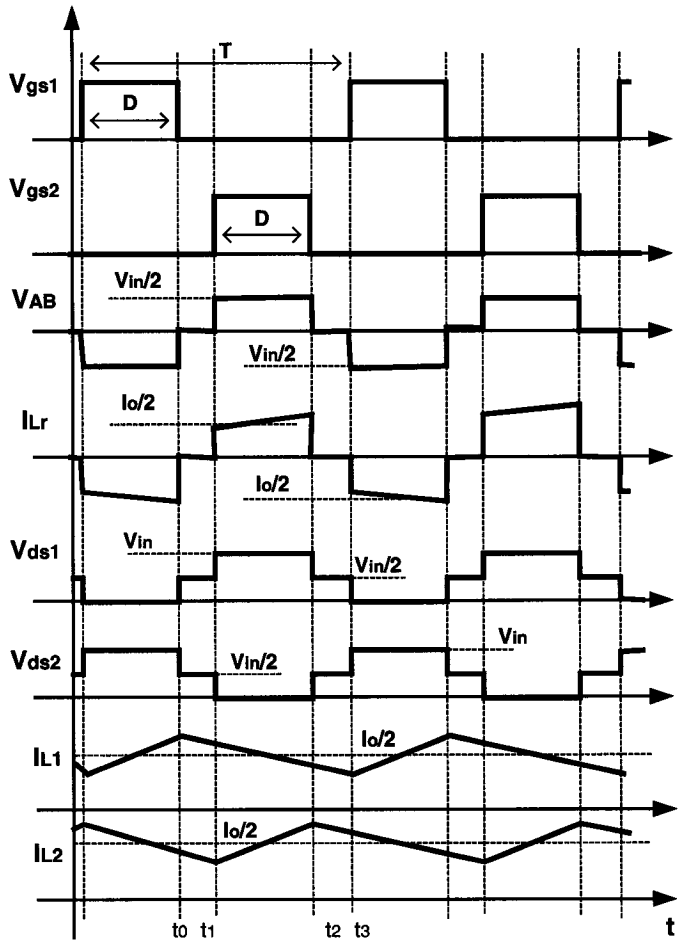


Figure 8.3: Main Switching Waveforms of Figure 8.1 when Symmetric Control Is Used

8.3 Topologies Comparison and Advantages

The HBB topology of Figure 8.1 with the different control schemes is compared to the conventional two-phase interleaved buck topology in this section as follows:

A. Voltage Conversion Ratio (Gain) and Switching Duty Ratio:

When the conventional symmetric control is used, the effective input voltage of the HBB topology is half compared to the conventional interleaved two-phase buck topology because of the capacitors' half-bridge configuration as shown in Figure 8.1. This will result in extended duty ratio for the same input and output voltages without

adding additional components. Hence, lower output voltage can be achieved with higher duty cycle and without adding additional magnatics to step down the voltage. The gain and duty ratio equations are given by:

$$\frac{V_o}{V_{in}} = D_1 \qquad \text{(Conventional Two Phase Buck)} \qquad (8.3.1)$$

$$\frac{V_o}{V_{in}} = \frac{D_2}{2} \Rightarrow D_2 = 2\frac{V_o}{V_{in}} \qquad \text{(HBB with Symmetric Control)} \qquad (8.3.2)$$

$$\frac{V_o}{V_{in}} = D_3(1-D_3) \Rightarrow D_3 = \frac{1}{2V_{in}}\left[V_{in} - \sqrt{V_{in}^2 - 4V_{in}V_o}\right]$$

$$\text{(HBB with Complementary Control)} \qquad (8.3.3)$$

where: $D_1, D_2, and\ D_3$ are the duty ratios (cycles) between zero and 0.5.

Figure 8.4 shows a plot for the duty ratios of Equations (8.3.1), (8.3.2) and (8.3.3) versus V_o for $V_{in} = 12$. It can be noticed that the duty ratio for the HBB is extended compared to the conventional two-phase buck for the same design.

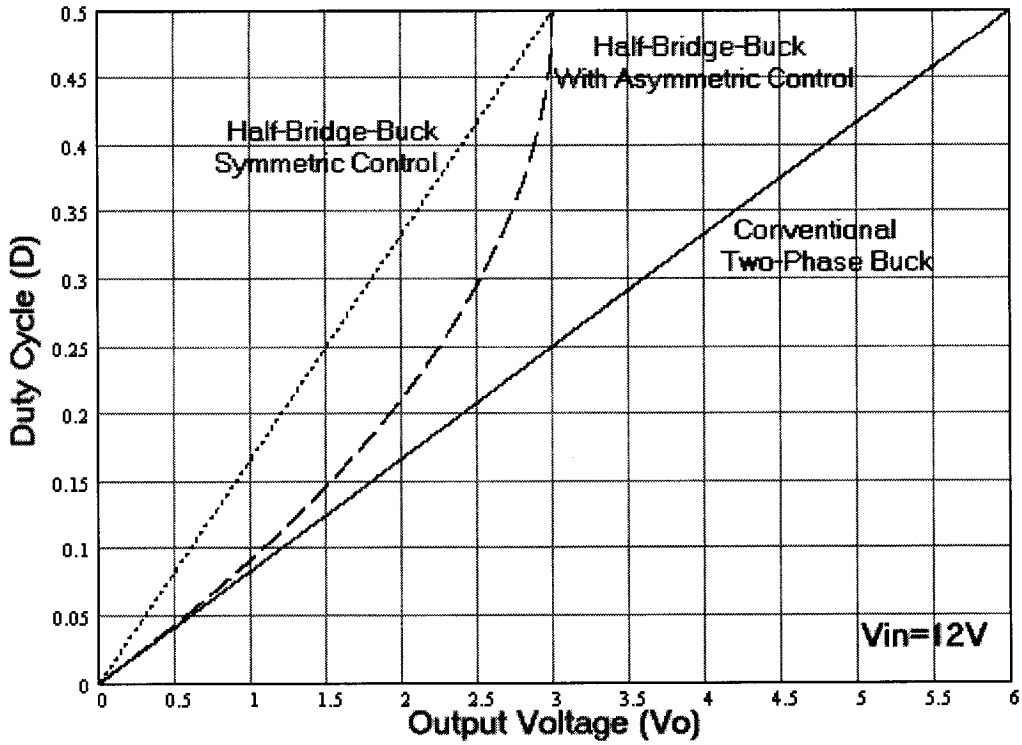


Figure 8.4: Duty Ratios Comparison

B. Soft-Switching Operation:

As discussed in the previous section, soft switching for the HBB can be achieved using complementary control scheme. This will result in higher converter efficiency especially at higher switching frequencies but with asymmetric components stresses.

C. Output Current Ripple:

The output current ripple equations are given by:

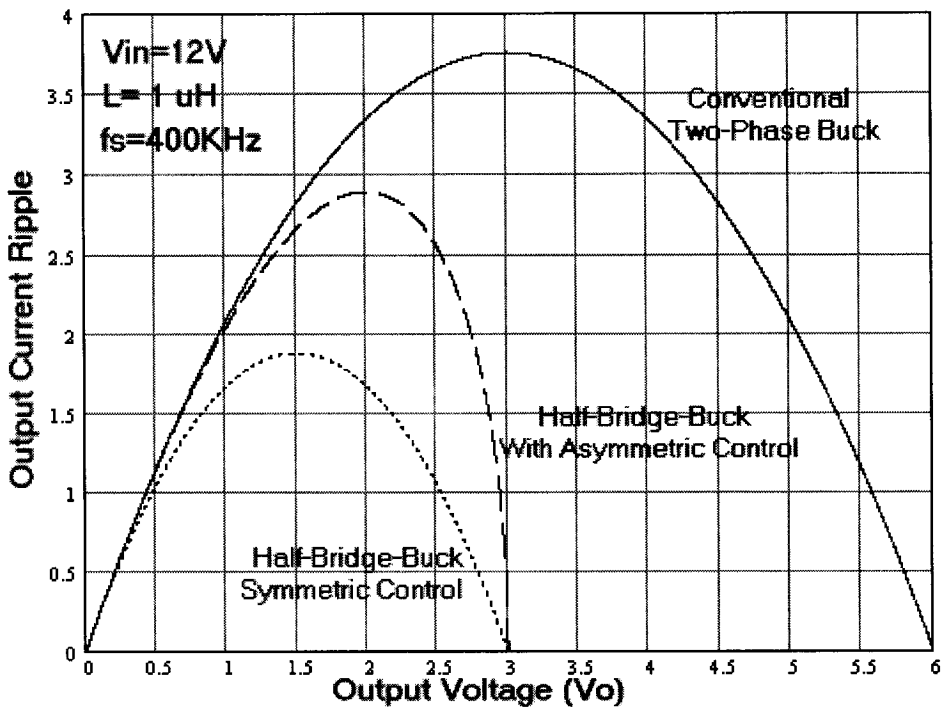
$$\Delta I_{co1} = \frac{D_1}{f_s}\frac{(V_{in}-2V_o)}{L} = \frac{V_o}{V_{in}f_s}\frac{(V_{in}-2V_o)}{L} \quad \text{(Conventional Two-Phase Buck)} \qquad (8.3.4)$$

$$\Delta I_{co2} = \frac{D_2}{2f_s}\frac{(V_{in}-4V_o)}{L} = \frac{V_o}{V_{in}f_s}\frac{(V_{in}-4V_o)}{L} \quad \text{(HBB with Symmetric Control)} \qquad (8.3.5)$$

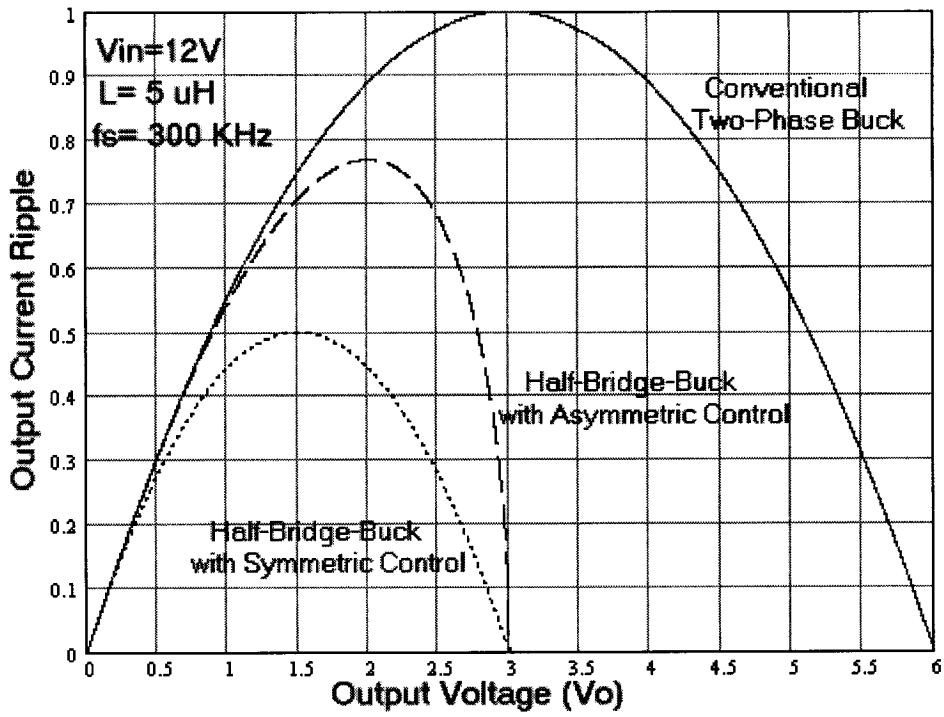
$$\Delta I_{co3} = \frac{V_o}{f_s}\left[\frac{(1-D_3)}{L_2} - \frac{D_3}{L_1}\right] = \frac{V_o}{f_s L}(1-2D_3) = \frac{V_o}{V_{in}}\frac{\sqrt{V_{in}^2 - 4V_{in}V_o}}{f_s L}, L = L_1 = L_2$$

(HBB with Complementary Control) (8.3.6)

Figures 8.5(a) and 8.5(b) show plots for the output current ripple of Equations (8.3.4), (8.3.5) and (8.3.6) versus V_o for $V_{in} = 12$, when $f_s = 400KHz$ and $L = 1\mu H$ and when $f_s = 300KHz$ and $L = 5\mu H$. It can be noted that lower current ripple is achieved by the HBB when conventional symmetric and asymmetric control schemes are used compared to the two-phase buck.



(a)



(b)

Figure 8.5: Output Current Ripple Comparison

D. Current Sharing:

The HBB converter has current sharing immunity against layout and components asymmetry because of the two capacitors existence when symmetric voltage-mode control is used. Hence, even if there is asymmetry between the inductors or switches resistances or their traces, the half-bridge buck will keep symmetric currents between the channels when conventional symmetric control is used. Therefore, current sharing control loop is not required (inherent current sharing).

When the conventional symmetric control is applied to the HBB of Figure 8.1, C_1 is charged through $V_{in} \rightarrow S_1 \rightarrow L_1 \rightarrow C_o \rightarrow D_1 \rightarrow L_r \rightarrow C_1$ conduction path, while C_2 is

discharged when S_1 is turned ON, and C_2 is charged through $V_{in} \rightarrow S_2 \rightarrow L_2 \rightarrow C_o \rightarrow D_2 \rightarrow L_r \rightarrow C_2$ conduction path, while C_1 is discharged when S_2 is turned ON. When both conduction paths have the same resistance and inductance, i.e. symmetric, each capacitor will have a voltage that is half of the input voltage on average. However, when both conduction paths do not have the same resistances and/or inductances, one of the capacitors will have an average voltage larger than the other. For example, if one conduction path has a total resistance larger the other, C_1 will have an average voltage smaller than half of the input voltage, since it will be discharged by a larger current and charged by smaller current compared to C_2 while maintaining the fact that the total voltage of both capacitors is always equal to the input voltage. This behavior causes the two channels, i.e. the inductors and switches, always to carry the same average current regardless of their asymmetry.

E. Conduction Loss:

In addition to the soft-switching operation achieved by asymmetric control applied to the HBB, conduction loss is greatly reduced because of the freewheeling period elimination.

F. Power Density and Efficiency:

The extended duty ratio was achieved without adding extra magnetics in the HBB. Hence, power density is not affected. Moreover, since soft switching is possible, larger switching frequencies can be used, which result in higher power density with improved efficiency.

G. Dynamic performance:

Operating at higher switching frequency results in improved dynamic performance. For the same output current ripple requirements, the output filter inductance can be smaller so that fast transient response can be achieved compared to the two-phase interleaved buck converter.

The HBB constrain is that the load ground has to be isolated from the source ground. This makes the HBB topology a second stage candidate in two-stage configuration, as will be discussed in the next section, or for applications where load ground is isolated from source ground, for example battery chargers.

8.4 Two-Stage Approach for DC-DC Converters

For high input voltage converters, such as 48V nominal input voltage DC-DC converters, electrical isolation is generally required. In two-stage converter approaches [101], the isolation transformer may be used in the first stage or the second stage. If the transformer is used in the second stage, the first stage topology may be buck or boost converter, and the second stage may be full bridge, half bridge, forward or push pull. The first stage provides a regulated voltage bus for the second stage, and the second stage steps down the voltage and provides electrical isolation. This configuration is suitable for wide input voltage range.

On the other hand, the isolation transformer can be used in the first stage, while the second stage is non-isolated. Such two-stage converter configuration is shown in Figure 8.6, where the first stage provides step-down intermediate voltage bus and transformer isolation and can be regulated or non-regulated. The second stage is designed

to tightly regulate the output voltage and meet the transient requirements, where the non-isolated buck-derived HBB converters may be employed [101]. It should be noted that intermediate bus voltage should be optimized according to the values of the output voltage and the converter power level.

Moreover, the Coupled-Inductors Current Doubler (CICD) [68] topology, which was presented in Chapter 7, can be also employed in the HBB topology.

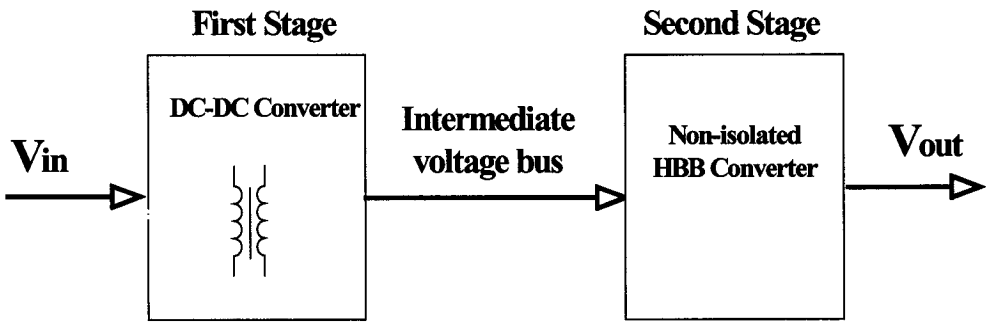


Figure 8.6: Two-Stage Approach for High Step-Down Fast Transient Converter

8.5 Simulation Results

The HBB topology was simulated with symmetric control and symmetric traces and components with $V_{in} = 12V$ and 1.8V/10A load as shown in the simulation results of Figure 8.7, with 300kHz frequency per switch, $L_1 = L_2 = 5\mu H$ and $L_r = L_s = 100nH$. In Figure 8.8, the duty cycle was set to 0.45 and soft switching was achieved at 2.4V/13.3A load.

The inductors' traces resistances were deliberately made different, first by $10m\Omega$ and then by $50m\Omega$, and were simulated for the same design of Figure 8.7, as shown in

Figure 8.9 and Figure 8.10, respectively. It can be noted that the two capacitors voltages were equal in Figure 8.7 when the traces were symmetric, whereas in Figures 8.9 and (8.10), as the traces difference increased, the capacitor voltages difference became larger while maintaining equal current sharing, as shown in the Figures. The sum of the capacitors voltages is equal to the input voltage at all cases. Also, the current sharing was maintained when a $10m\Omega$ difference was made in the diodes traces as shown in Figure 8.11.

Figure 8.12 shows the soft-switching achieved when asymmetric control is used at a duty cycle of 0.35. The current asymmetry can be noticed from the Figure.

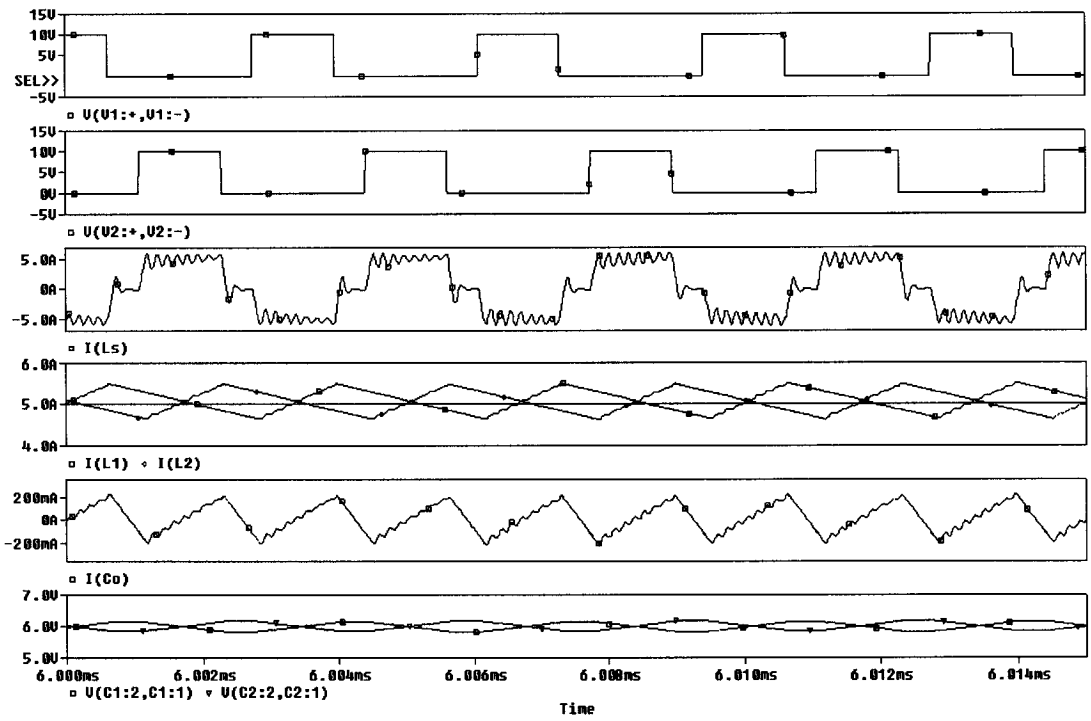


Figure 8.7: HBB with Symmetric Control and Symmetric Traces and Components Simulation Results

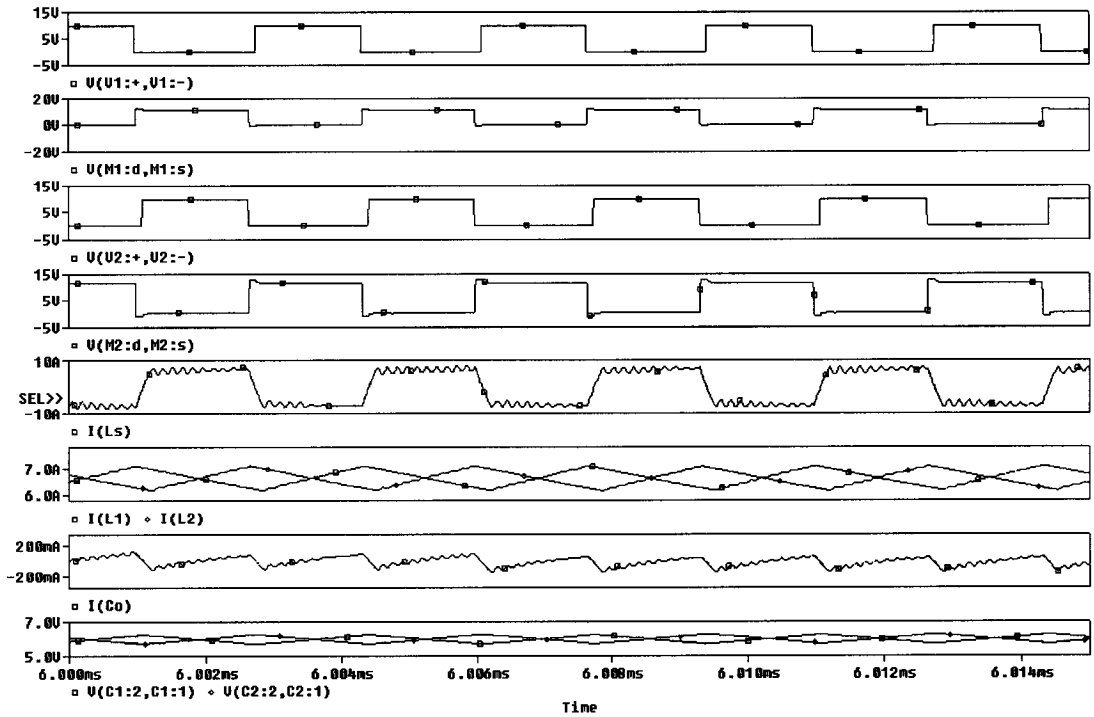


Figure 8.8: HBB with Symmetric Control and Symmetric Traces and Components

Simulation Results with Soft Switching

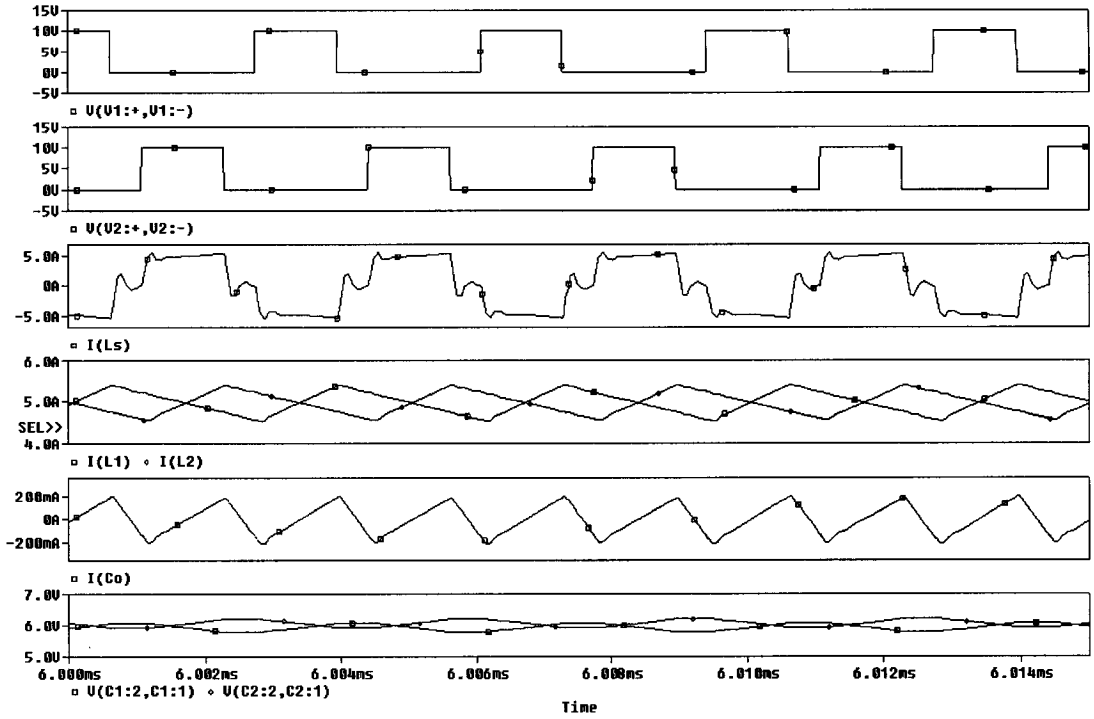


Figure 8.9: HBB with Symmetric Control and Asymmetric Traces and Components Simulation Results when the Inductors Traces Resistances Were Deliberately Made Different By $10m\Omega$

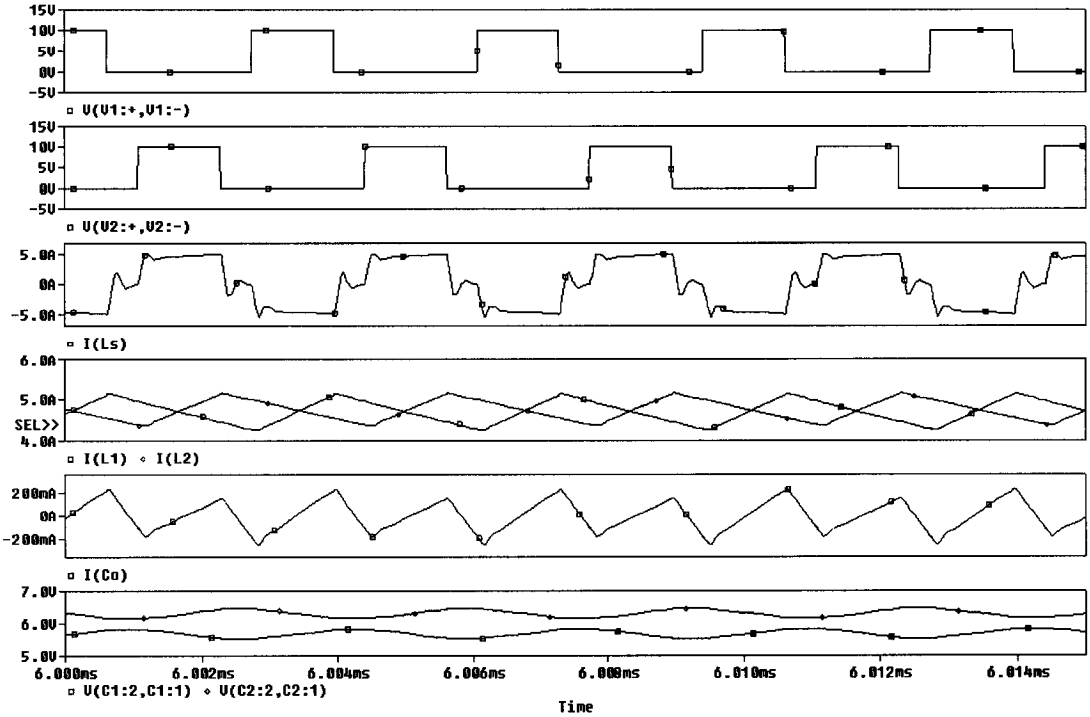


Figure 8.10: HBB with Symmetric Control and Asymmetric Traces and Components Simulation Results when the Inductors Traces Resistances Were Deliberately Made Different By $50m\Omega$

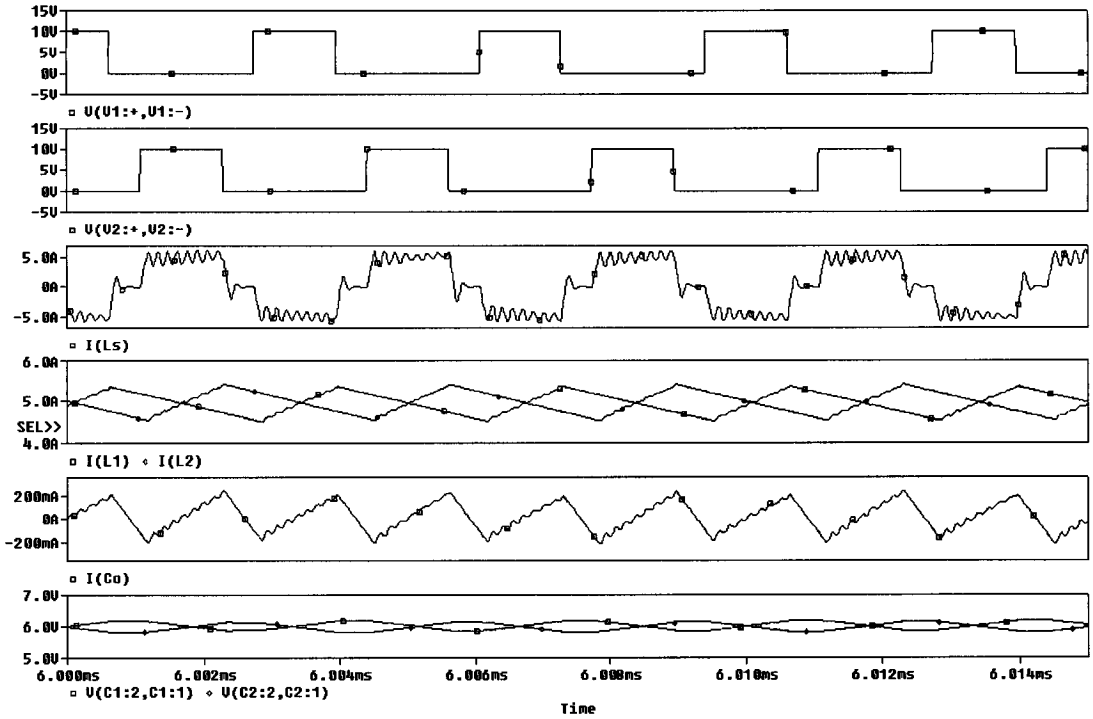


Figure 8.11: HBB with Symmetric Control and Asymmetric Traces and Components Simulation Results when the Diodes Traces Resistances Were Deliberately Made Different By $10m\Omega$

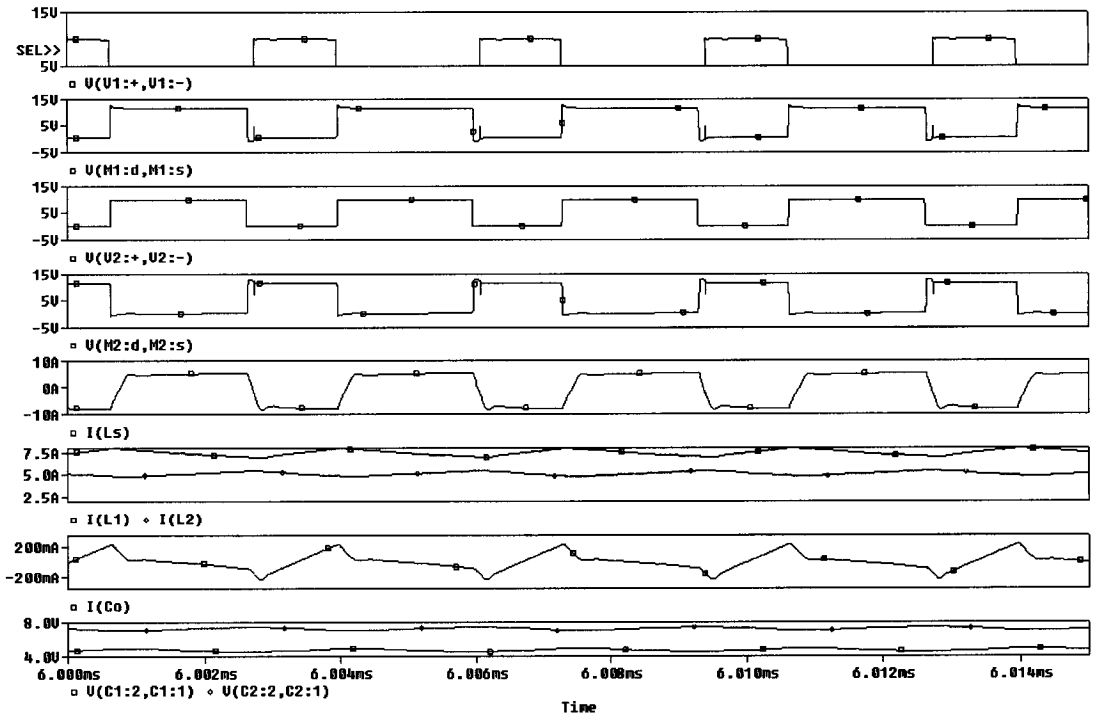


Figure 8.12: HBB with Asymmetric Control Simulation Results

8.6 Experimental Study

Two topology characteristics were tested, namely the extended duty ratio and inherent current sharing of the HBB topology and the soft switching of complementary-controlled HBB. The experimental results were as follows:

A. Extended Duty Ratio and Inherent Current Sharing of the HBB Topology Experimental Results:

An experimental prototype for the HBB topology of Figure 8.1 with symmetric control was built in the laboratory for experimental verification with $V_{in} = 12V$, $V_o = 1.8V$ and load current $I_o = 10A$. Each output inductor was equal to $L_1 = L_2 = 5\mu H$,

and the value of L_r was approximately 100nH. The switching frequency per switch was $f_s = 300kHz$.

The stepped-down output voltage was achieved with approximately $D = 0.35$ using the HBB topology compared to half of this duty cycle if a conventional two-phase buck was used ($D \approx 0.17$). At full load, each inductor current ripple was approximately 0.75A while the total current ripple was approximately 0.4A, which agrees with Figure 8.5(b).

Then, the HBB topology inherent current sharing capability was experimented. Figure 8.13 shows the experimental results when the inductors and switches traces and self-resistances are symmetric, which results in equal current sharing. Figure 8.14 shows the experimental waveforms when the inductors L_1 and L_2 traces resistances differ by $10m\Omega$. Figure 8.15 shows the experimental waveforms when D_1 and D_2 traces resistances differ by $10m\Omega$. It can be noticed that in both cases of Figures 8.14 and (8.15), the current sharing is maintained without the need to a current sharing compensation loop, since C_1 and C_2 voltages compensate for the difference to keep equal current sharing as described earlier in this chapter. Less than half of this difference in a two-phase buck channel will make a huge current difference [30,58,60].

B. Soft-Switching of Complementary-Controlled HBB Topology Experimental Results:

Figures 8.16 and 8.17 show the experimental results when asymmetric control is used at $D = 0.35$ and $D = 0.48$, respectively. It can be noted that soft switching is achieved but, unfortunately, with asymmetric components stresses when the duty cycle is far from 0.5.

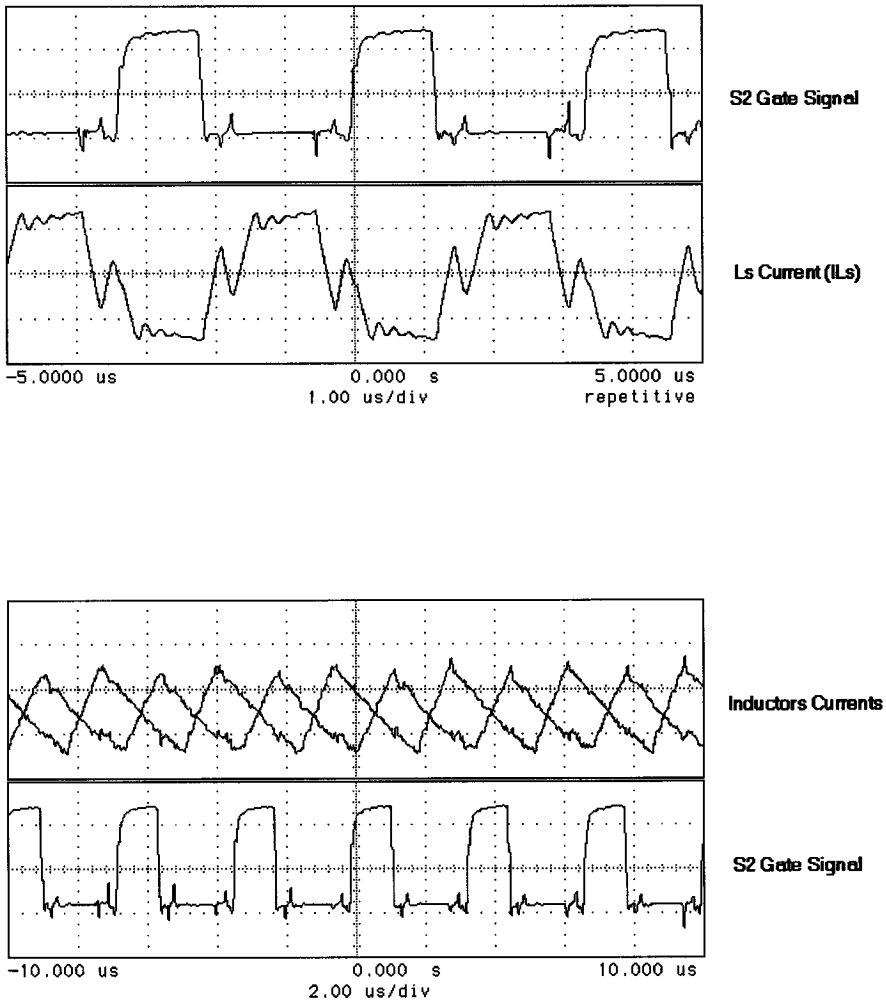


Figure 8.13: HBB Experimental Waveforms with Symmetric Control and Symmetric Traces

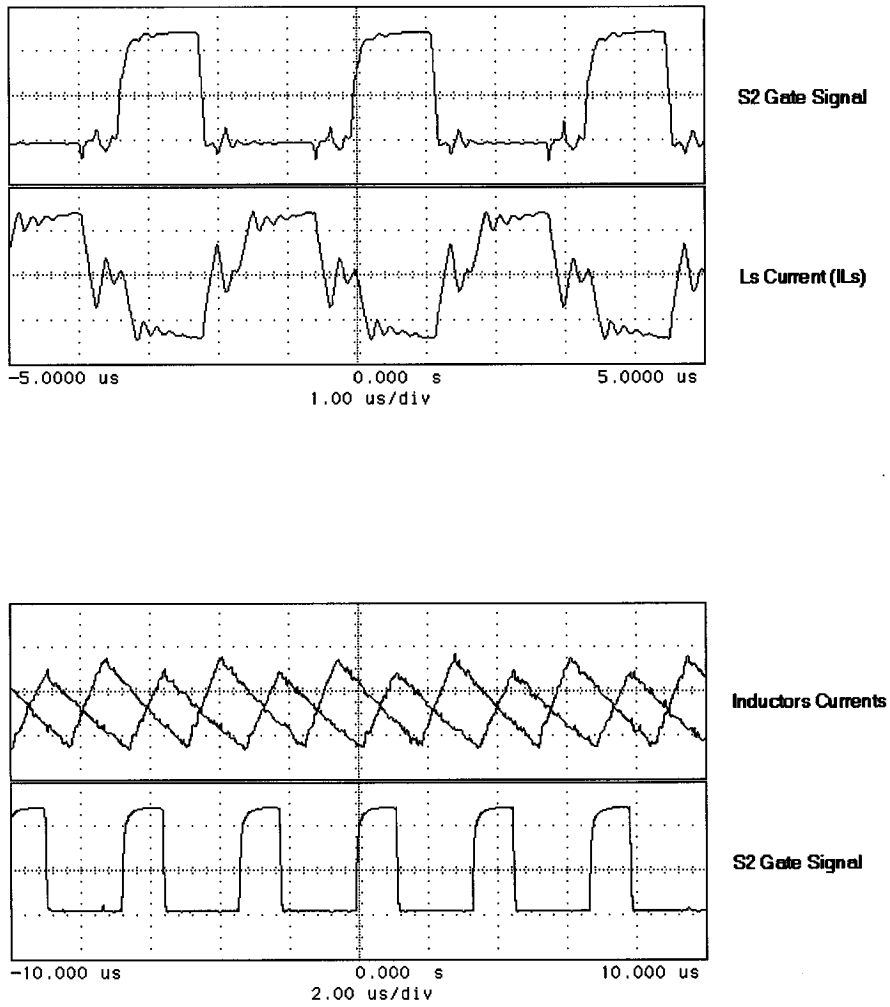


Figure 8.14: HBB Experimental Waveforms with Symmetric Control and $10m\Omega$ Asymmetry in the Inductors Traces

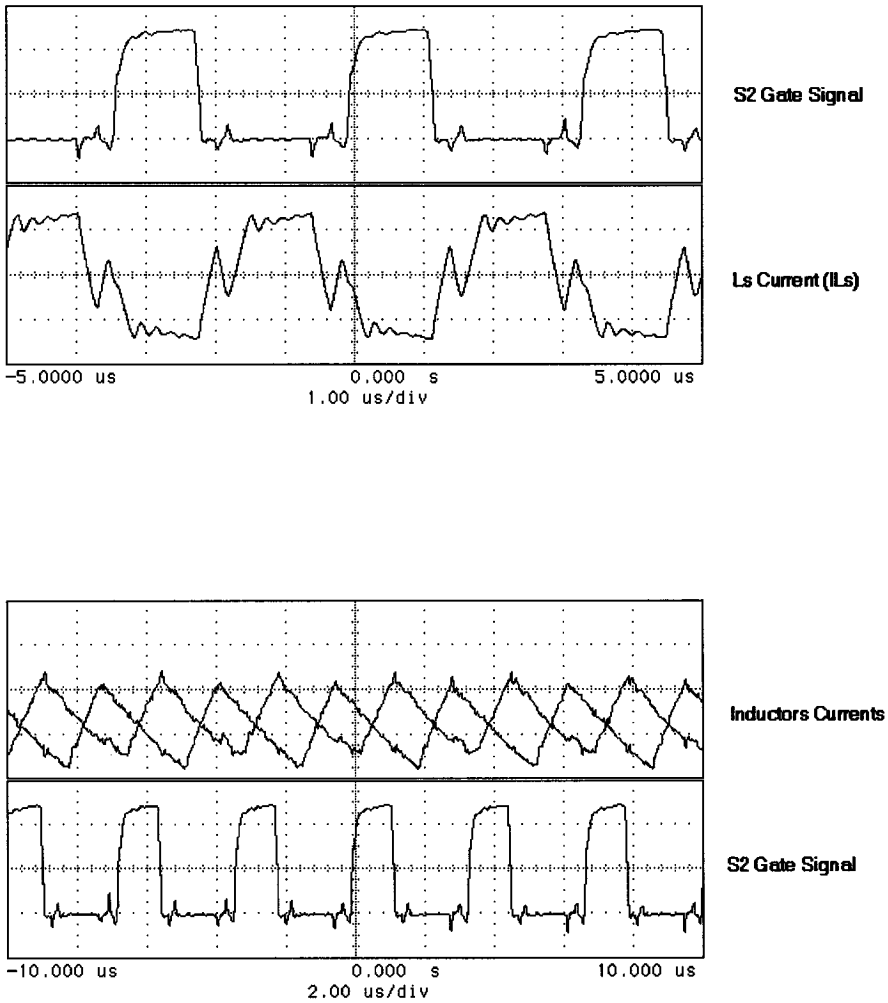


Figure 8.15: HBB Experimental Waveforms with Symmetric Control and $10m\Omega$ Asymmetry in the D_1 and D_2 Traces

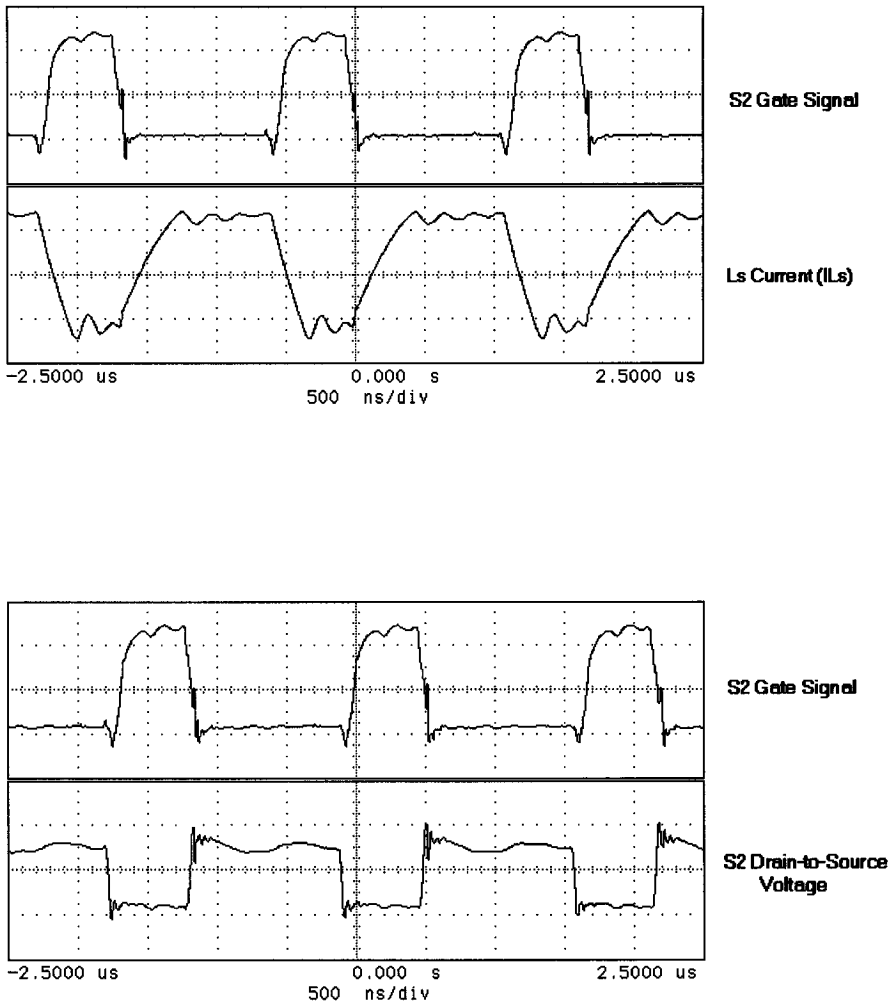
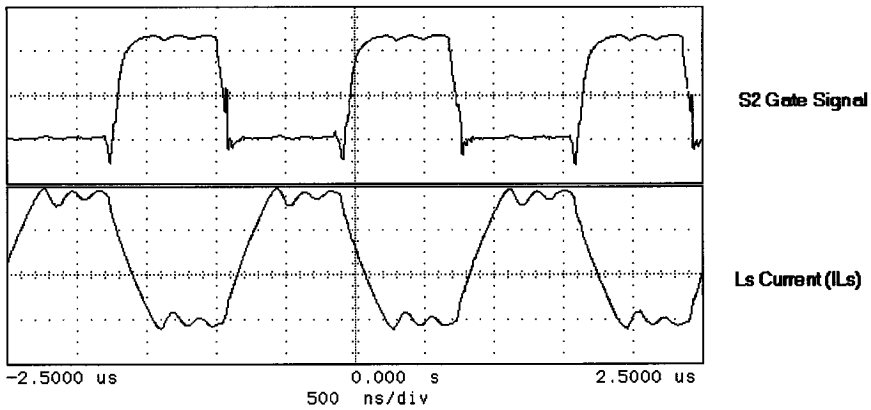
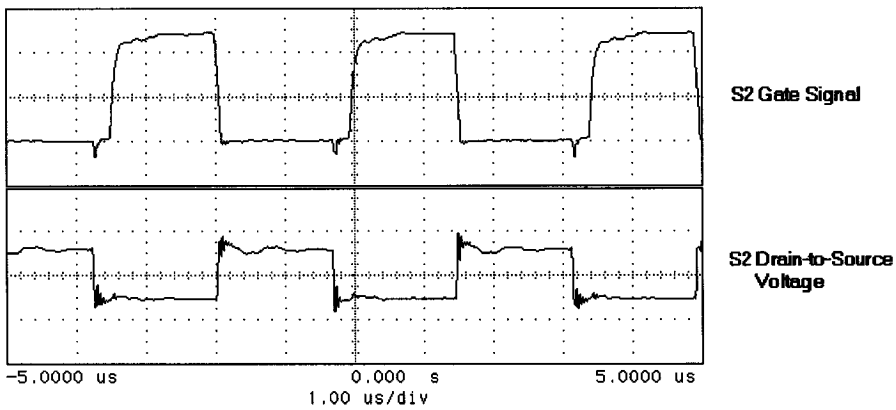


Figure 8.16: HBB Experimental Waveforms with Asymmetric Control at Soft-Switching Condition at D=0.35





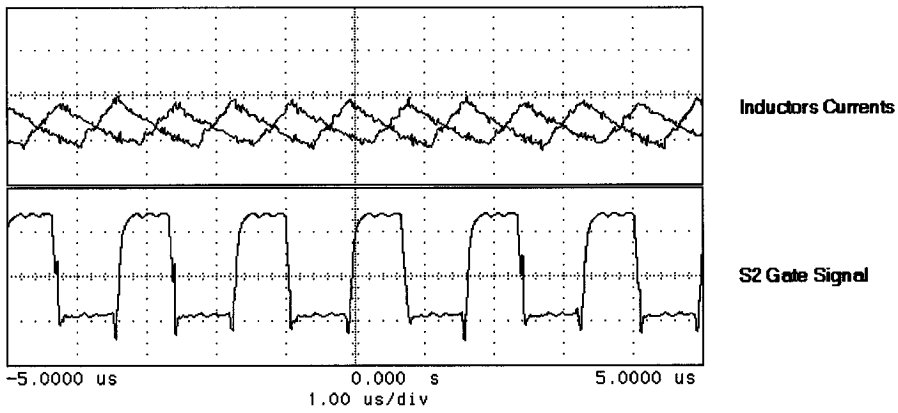


Figure 8.17: HBB Experimental Waveforms with Asymmetric Control at Soft-Switching Condition at D=0.48

8.7 Summary

Non-isolated Half-Bridge-Buck (HBB) topology was presented in this chapter, which has advantages including extended duty ratio, inherent current sharing, lower output current ripple and soft-switching when certain control schemes are used. Moreover, a two-stage scheme that utilized the HBB topology as a second stage was also presented. Both simulation and experimental studies were carried out.

CHAPTER 9

CONVERTER CONTROL TECHNIQUES AND DIGITAL CONTROL FOR FUTURE DC-DC CONVERTERS

9.1 Introduction

Several control techniques have been presented in the open literature in recent years to achieve fast transient response and lower output voltage deviation to satisfy VRMs and POLs requirements [7,28,30,58,60,73-79]. Theses techniques include those that use an error signal of negative feedback compensation with a reference compared to a constant frequency ramp signal [7,58,73-79] and those that have no feedback compensation [28,30] and use direct comparison with the controlled parameter (which is the output voltage here) to generate the required control signal(s).

In this chapter, a brief review and comparison between major control methods will be made followed by a presentation for an initial work for a control method concept and technique. Moreover, in this chapter, digital control is discussed as a candidate for future POL and VRM converters. Digital system structure, advantages, disadvantages and initial experimental setup are presented. Candidate method with its DSP algorithm are also presented, including the Maximum Efficiency Point Tracking (MEPT) method and algorithm.

9.2 Closed Loop System

Figure 9.1 shows a general basic block diagram for a controlled converter system. A negative feedback control is usually used to reduce the error between the output and the reference close to zero and maintain a stable system during steady state and transients [58]. It is desired to reduce the error to as close to zero as soon as possible, but unfortunately, the faster the system response is, the more difficult it is to maintain system stability. Hence, there is a trade off between the system response and its stability.

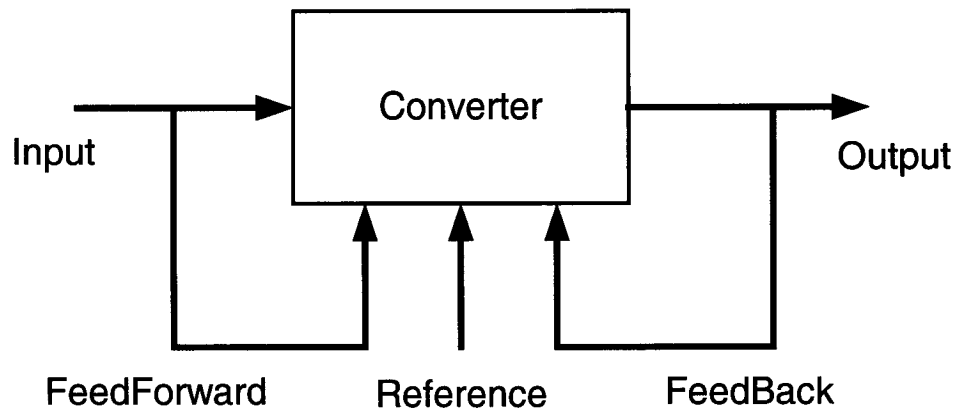


Figure 9.1: General Basic Block Diagram for A Controlled Converter System

Some systems use feedforward control [58] either alone or together with feedback control. Feedforward senses the input variations instead of output variations, and hence, it is less accurate than feedback control but is usually faster since it does not have to wait for the error signal. There is more to say about the comparison between feedback control and feedforward control but it is not an objective in this chapter. Here, only main feedback control methods will be briefly reviewed and compared.

Figure 9.2 shows a block diagram of a negative feedback converter system with a single feedback loop. It is easy to find that the reference-to-output closed loop transfer function is given by:

$$\frac{y(s)}{x(s)} = \frac{G(s)}{1+H(s)G(s)} \tag{9.2.1}$$

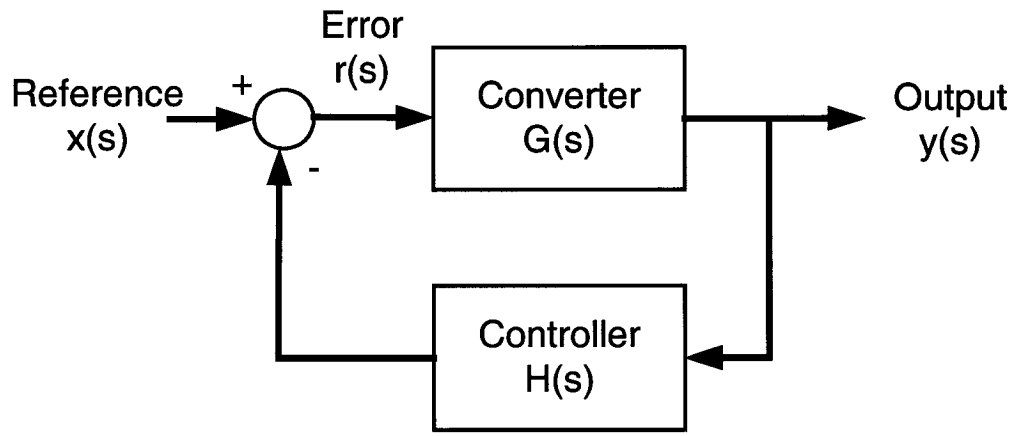


Figure 9.2: A Block Diagram of a Negative Feedback Converter System with a Single Feedback Loop

The objective of this closed loop system is to keep the system and the output stable at all conditions and independent of parameters variations such as load, input and converter components.

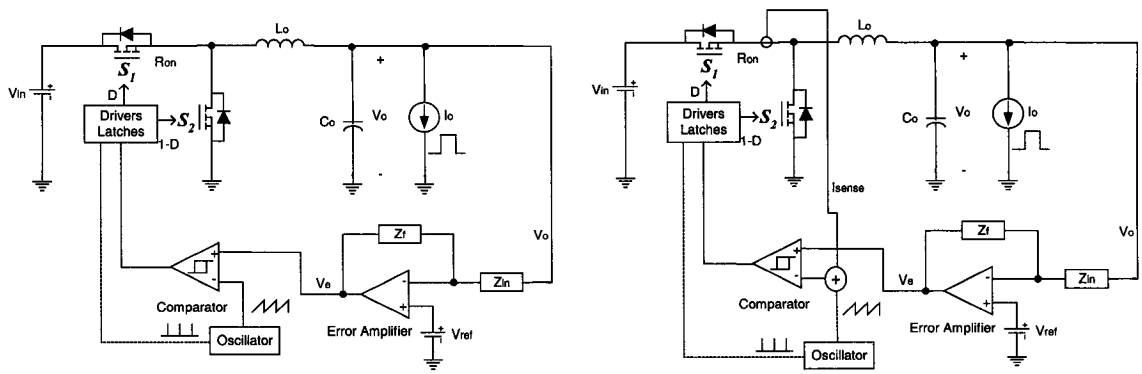
The DC-DC converter has a low-pass LC filter at its power stage output. This LC filter design is the first limit factor on the transient response speed to load transients before the controller limitations [27,58], as discussed in Chapter 2. Parameters sensing and controller speed response should minimize the additional delays of the feedback loop. Therefore, the controller or compensator cannot improve the dynamic characteristics of the power stage, but it can improve the closed loop system

characteristics for a minimum output filter requirement, which is desired for smaller size and lower cost, as discussed in Chapter 2. Therefore, design should be focused on the optimal power stage first, and then a good controller and compensator should be selected and designed to achieve a fast and stable closed loop converter system.

There are several control methods that can be used, each with its own characteristics, advantages, disadvantages and design procedure [7,28,30,58,60,73-79]. The next section will review and briefly compare some of these method including Pulse Width Modulation (PWM) controls.

9.3 Brief Review and Comparison of Control Techniques

Figure 9.3 shows simplified circuitries for some control methods applied to a single phase buck converter, namely: voltage-mode control [7,58], peak-current mode control [7,58,76], average-current mode control [7,58,73-75,77-79], voltage mode hysteretic control [28,30], and V^2 control [60].



(a) (b)

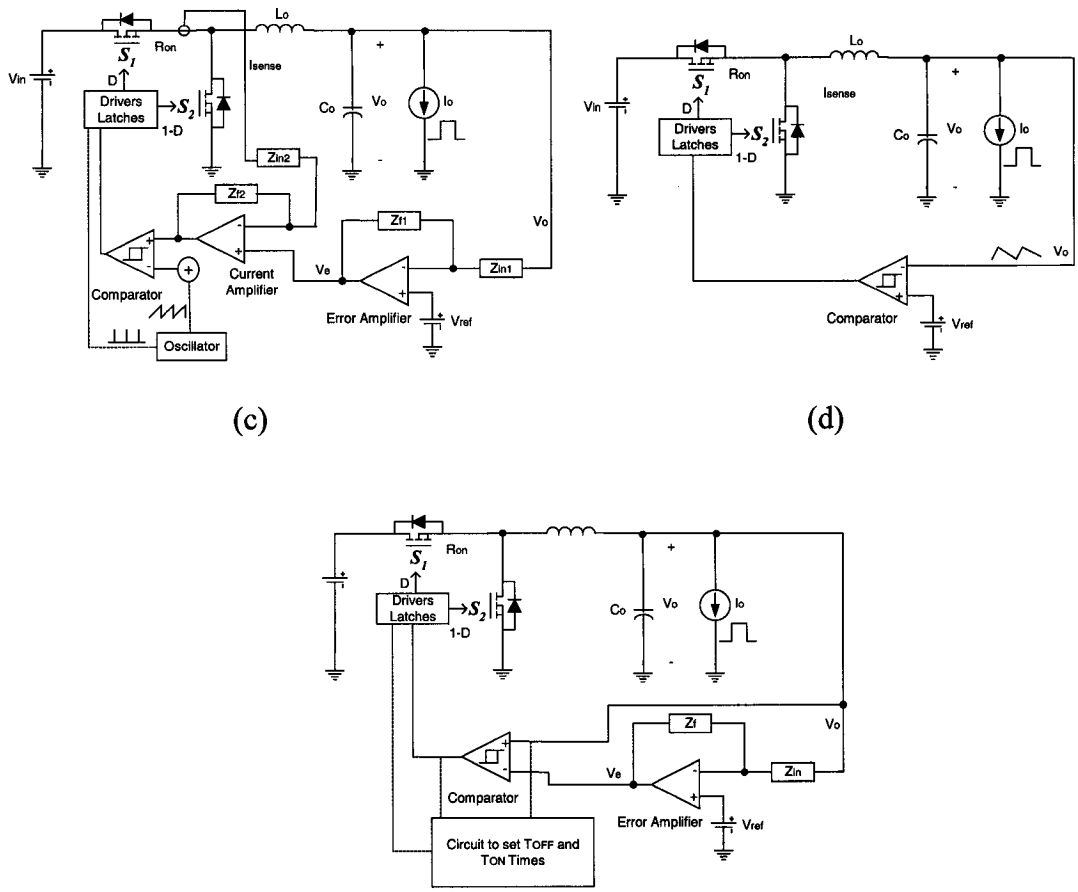


Figure 9.3: Simplified Circuitries for Some Control Methods Applied to a Single Phase Buck Converter: (a) Voltage-Mode Control, (b) Peak-Current Mode Control, (c) Average-Current Mode Control, (d) Voltage Mode Hysteretic Control and (e) V^2 Control

As a summary for the basic operation principle of each control method of Figure 9.3, the voltage-mode control senses the output voltage and compares it to a reference through a compensator to generate an error signal that is then compared to a constant frequency ramp signal to generate the driving signal for converter switches. In the peak-

current mode control, the inductor current is used as a ramp signal such that the appropriate switch is turned ON at the beginning of each switching cycle and turned OFF when the current signal peak hits the error signal of the voltage compensator. In the average-current mode control, the current ripple is subtracted from the voltage compensator error signal through summing amplifier. The resulted error signal is then compared to the ramp signal. In the voltage mode-hysteretic control, the compensation delays are avoided by directly comparing the output voltage to upper and lower limits through hysteretic comparator to directly turn ON or OFF the appropriate switches resulting in faster response but with a range of switching frequency that depends on converter parasitics, input and load variations. V^2 can be considered as a modified version of voltage-mode hysteretic control were the output voltage ripple is used as a ramp signal that is compared with the error signal of the voltage compensator.

In both voltage-mode and current-mode controls, the controller speed mainly depends on the feedback compensation bandwidth, which is a factor of the switching frequency that need to be increased for larger compensator bandwidth. While in hysteretic and V^2 controls, the feedback loop speed is higher and limited only by the components speed and technology. This higher speed sometimes comes at the expense of switching frequency range existence compared to fixed switching frequency as in voltage-mode and current-mode controls. Frequency compensation can be used to stabilize the switching frequency.

Moreover, hysteretic control has no limitation on switches conduction times, while in voltage-mode and current-mode controls may have limitation on switches conduction times when fixed switching frequency is used.

Another popular control technique that can be used and integrated with most or all of the voltage and current mode techniques is the droop compensation or Voltage Positioning (VP) technique [58,84-86]. As shown in Figure 9.4, the idea of voltage positioning technique is to make the output voltage as a function of the load so that the output voltage is close to the upper voltage window limit at no-load and close to the lower voltage window at full load to utilize the allowed voltage deviation window and hence reduce the required output capacitance. By using this method, the allowed voltage deviation can be increased up to two times, as show in Figure 9.4.

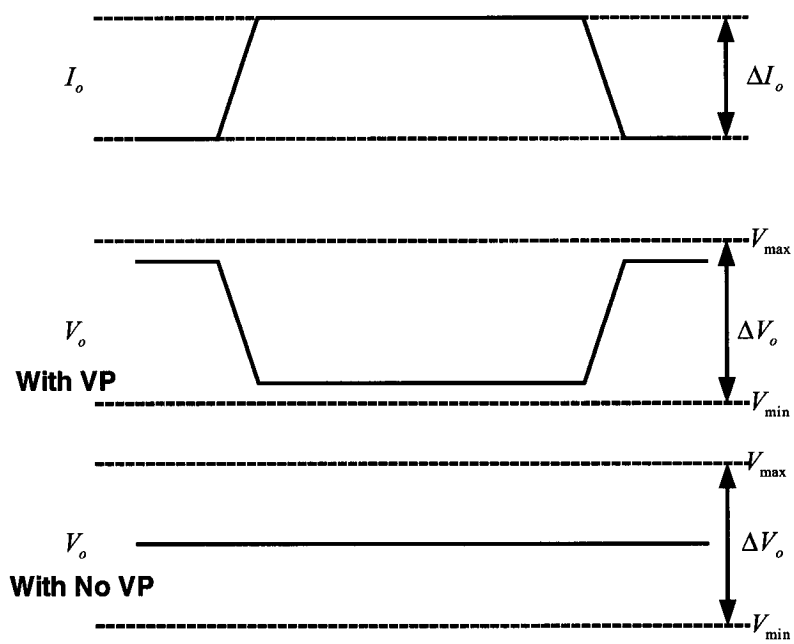
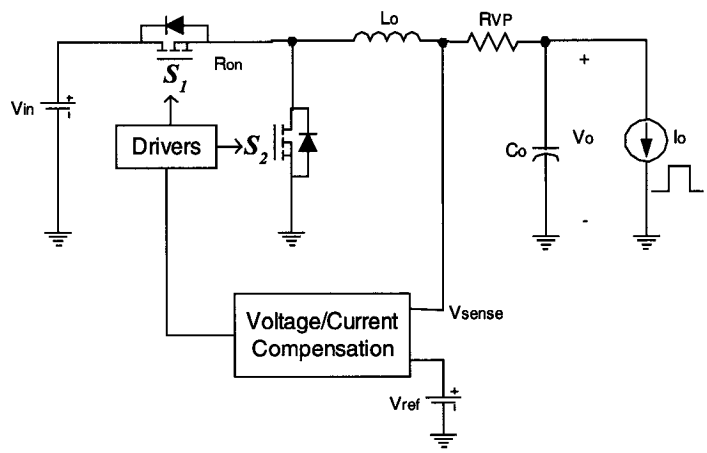


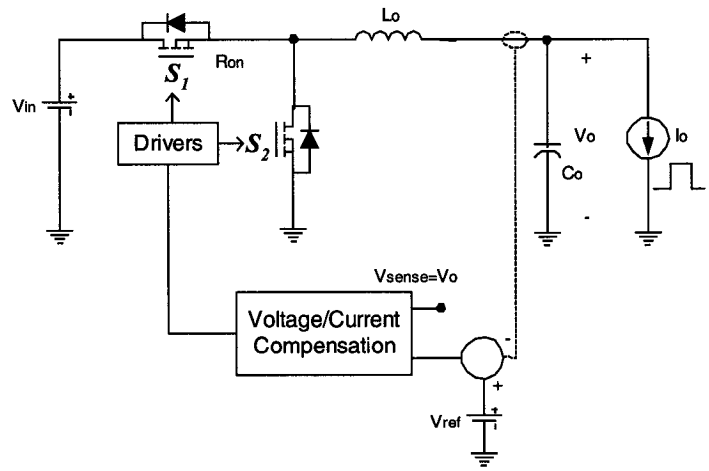
Figure 9.4: The Idea of Voltage Positioning Control Technique

There are two main types of voltage positioning technique implementation, namely, Passive Voltage Positioning (PVP) and Active Voltage Positioning (AVP). As shown in Figure 9.4(a), PVP is applied by adding a resistor between the controller output voltage sense point and the output capacitor, while AVP can be applied by subtracting a

voltage proportional to the output current from the controller voltage reference, as shown in Figure 9.4(b).



(a)



(b)

Figure 9.5: Voltage Positioning Implementations: (a) Passive Voltage Positioning (PVP) and (b) Active Voltage Positioning (AVP)

The PVP is easier to implement by adding a resistor, and it can follow the load more quickly compared to the AVP. However, the inserted resistor in PVP can cause large power losses especially for high current applications. The challenges in AVP design include its speed, which should be enough to follow load transients, and its accuracy to be able to utilize the allowed voltage transient window without deviating outside of it.

9.4 A Look at Controller Sensed Signals

Most of today's converter control methods depend on the output voltage sensing and sometime on other sensed signals such as the inductor current to generate the necessary control signals. Actually, sensing the converter output voltage, which is the controlled parameter here, may be sufficient to generate necessary control and duty cycle, ignoring protection and other additional functions that the controller usually should have, if the converter operates only in steady-state and with slow transients and without strict requirements on the voltage deviation. Consider the following two basic equations:

$$i_{co}(t) = C_o \frac{dv_{co}(t)}{dt} \tag{9.4.1}$$

$$v_{Lo}(t) = L_o \frac{di_{Lo}(t)}{dt} \tag{9.4.2}$$

It is evident from Equations (9.4.1) and (9.4.2) that both the output voltage, which is the output capacitor voltage, and the inductor current can not change instantaneously and need dt to change as a response to fast load transients. Hence, there is a considerable delay caused in sensing the load transients before the delays of the control loop, causing several cycles of delay. Therefore, another faster changing parameter has to be sensed to be able to identify the transient in one cycle and respond to it while not affecting the

controller stability. By taking a closer look at internal converter voltages and current variables, as shown in Figure 9.6 and in Equation (9.4.1), it can be noted that the capacitor current $i_{co}(t)$ can change almost instantaneously at load transients, and it is has the fastest response change to transients when compared to other converter variables.

Therefore, a better control technique has to be selected, one that uses conventional closed loop methods and senses appropriate parameters. Moreover, it will be a good characteristics of such a method to use simple conventional method during steady state, such as conventional voltage-mode control, and to have the ability to respond quickly, within one switching cycle, and extend the loop bandwidth during transients and reduce the impedance without the need to design a high bandwidth loop compensator and sacrifices the stability. The next section presents an initial and simple idea toward achieving such characteristics.

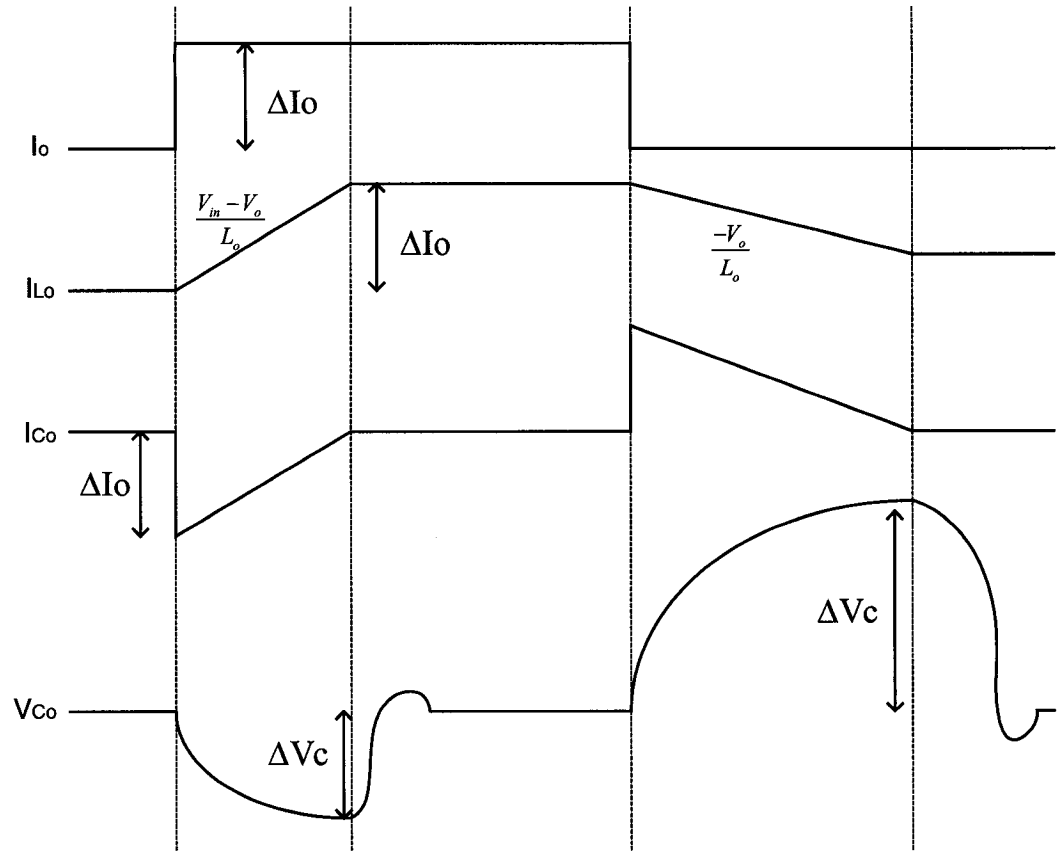


Figure 9.6: Converter Voltages and Current Varying During Load Transients

9.5 Fast Transient Response Control Scheme

Figure 9.7 shows basic schematics for the presented method, which will be referred to as $v_c i_c$ method for abbreviation, reflecting that information obtained contain v_c and i_c. This scheme may be considered as a version of current mode control or sliding mode control [80] but without the need of additional reference for the capacitor current.

The capacitor current, which has, in theory or ideally, zero average current in steady state, is subtracted from the final error signal of a conventional controller which can be one of those summarized in Figure 9.3. For example, if the controller was a simple

compensated voltage-mode controller, the result of subtracting the output capacitor current from the compensator error signal is compared to the ramp signal to generate the switching driving PWM signal. During load transients, the capacitor current change is faster than the output voltage and inductor current change, allowing faster transient response, possibly in one switching cycle, even if the compensation has low bandwidth. Moreover, the oscillation of the output voltage in voltage mode control is damped allowing output voltage to reach its steady-state value exponentially without oscillating around its reference value. During steady state, additional small steady-state error exists that is proportional to the capacitor current ripple, which should be compensated for.

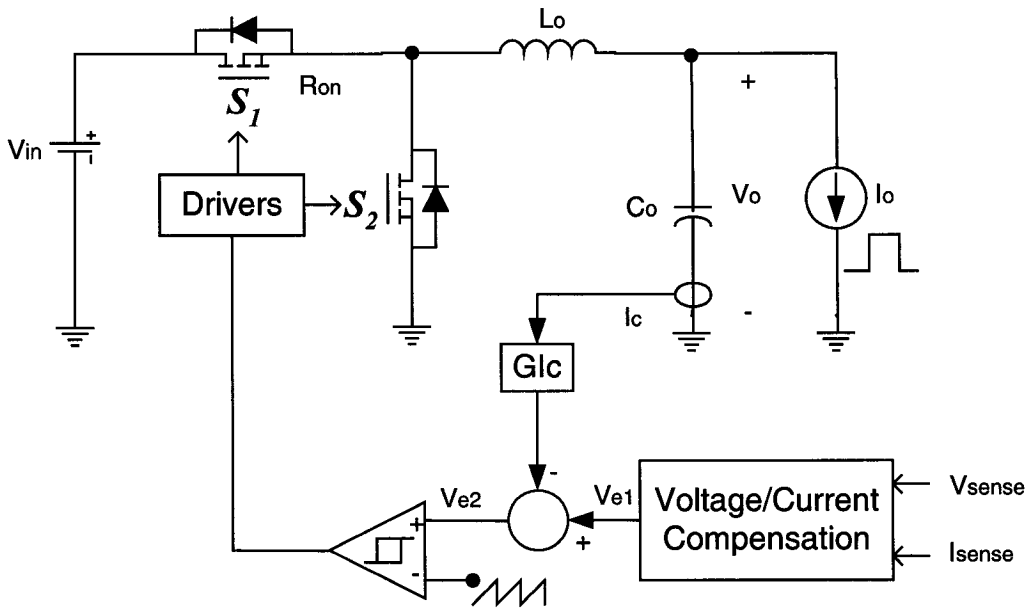


Figure 9.7: Basic Schematics for the $v_c i_c$ Presented Method

9.6 Design and Simulation Results

In this section, a voltage-mode controlled closed-loop buck converter with 2-poles 2-zeros compensator will be designed and simulated. Then for the same design and

compensator, the VcIc method will be used and simulated, by introducing the capacitor current signal s presented in the previous section and shown in Figure 9.7. The converter's main specs were as follows: $V_{in}=12V$, $V_o=1V$, $I_o=50A$, $C_o=5.6mF$, $ESR=0.1m\Omega$ and $f_s=500kHz$.

Figure 9.8 shows the schematics of the voltage-mode, closed-loop buck converter with 2-poles 2-zeros compensator. The transfer function of the 2-poles 2-zeros compensator can be derived as follows:

$$H_{comp}(s)=\frac{Z_2}{Z_1}=\frac{\frac{(\frac{1}{sC_1})(R_2+\frac{1}{sC_2})}{\frac{1}{sC_1}+\frac{1}{sC_2}+R_2}}{\frac{(R_1)(R_3+\frac{1}{sC_3})}{\frac{1}{sC_3}+R_3+R_1}}=G_{comp0}\frac{(1+\frac{s}{\omega_{ez1}})(1+\frac{s}{\omega_{ez2}})}{s(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{ep2}})}$$

where:

$$\omega_{ez1}=\frac{1}{R_2C_2},\ \omega_{ez2}=\frac{1}{(R_1+R_2)C_2},\ \omega_{p1}=\frac{1}{R_2(C_1C_2/(C_1+C_2))},\ \omega_{p1}=\frac{1}{R_3C_3},\text{ and}$$

$$G_{comp0}=\frac{1}{R_1(C_1+C_2)}.$$

The buck converter output-to-control transfer function is given by:

$$H_{buck}(s)=\frac{G_{buck0}(1+\frac{s}{2\cdot\pi\cdot f_{esr}})}{1+\frac{s}{Q\cdot\omega_o}+(\frac{s}{\omega_o})^2}$$

where:

$$G_{buck0} = \frac{V_{in}}{V_{ramp}},\ f_{esr} = \frac{1}{2\pi R_{esr} C_o},\ \omega_o = \frac{1}{\sqrt{C_o L_o}},\ \text{and}\ Q = R_o \sqrt{\frac{C_o}{L_o}}.$$

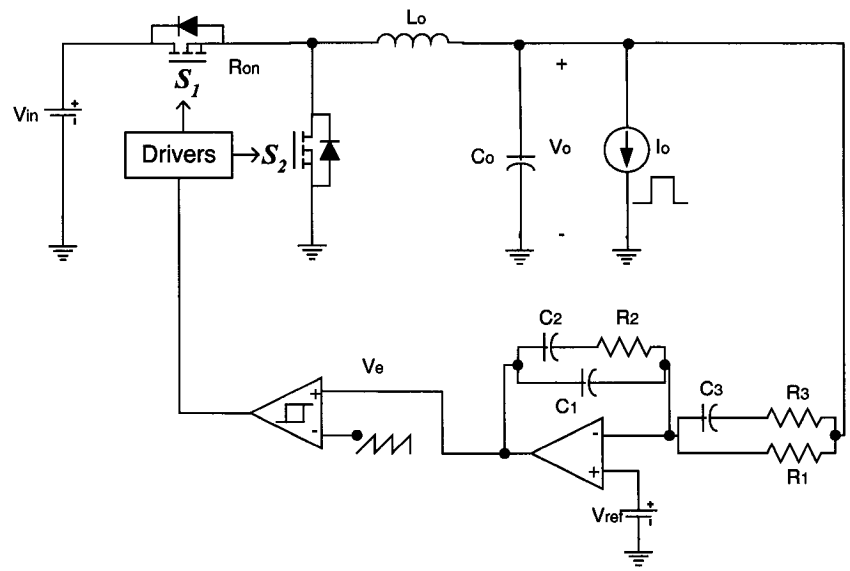


Figure 9.8: Schematics of the Voltage-Mode Closed Loop Buck Converter with 2-Poles 2-Zeros Compensator

A MathCad sheet was created with design steps and bode plots to simplify the compensator design. The following is the MathCad sheet capture:

Buck Closed Loop 2-Poles 2-Zeros Compensatior

Design

$V_o := 1 \quad V_{in} := 12 \quad Co := 5.6 \cdot 10^{-3} \quad Lo := 1 \cdot 10^{-6} \quad Ro := 0.02 \quad f_s := 500 \cdot 10^{3}$

$D := \frac{V_o}{V_{in}} \text{ float},6 \rightarrow 8.33333 \cdot 10^{-2}$ $\qquad R_{esr} := 0.1 \cdot 10^{-3}$

$\omega_o := \frac{1}{\sqrt{Co \cdot Lo}} \text{ float},6 \rightarrow 13363.1$ $\qquad f_o := \frac{\omega_o}{2 \cdot \pi} \text{ float},6 \rightarrow 2126.80$

$Q := Ro \cdot \sqrt{\frac{Co}{Lo}} \text{ float},6 \rightarrow 1.49666$ $\qquad f_{esr} := \frac{1}{2 \cdot \pi \cdot R_{esr} \cdot Co} \text{ float},6 \rightarrow 284205.$

$V_{ramp} := 1$

$G_{buck0} := \frac{V_{in}}{V_{ramp}} \rightarrow 12$

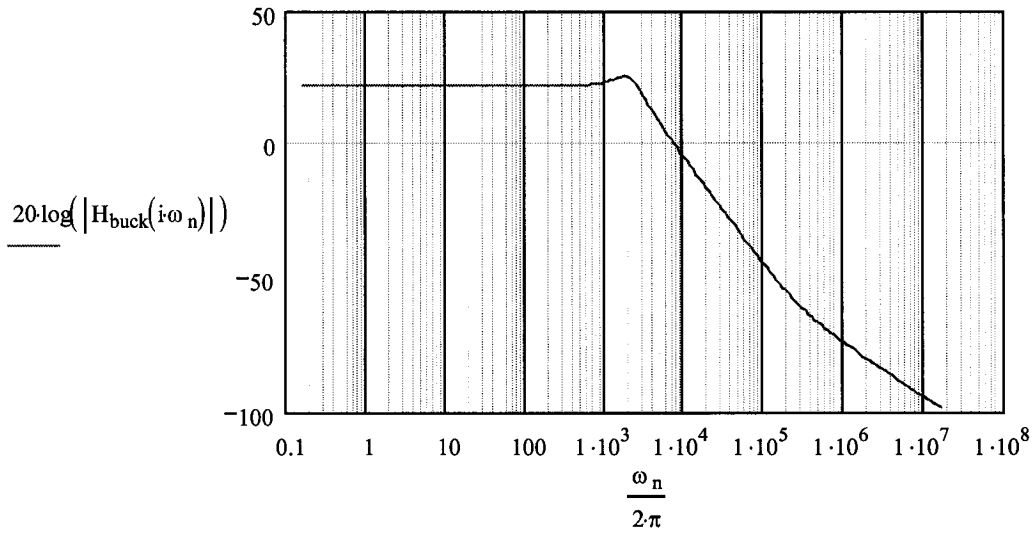
Converter Output-to-Control Transfer Function

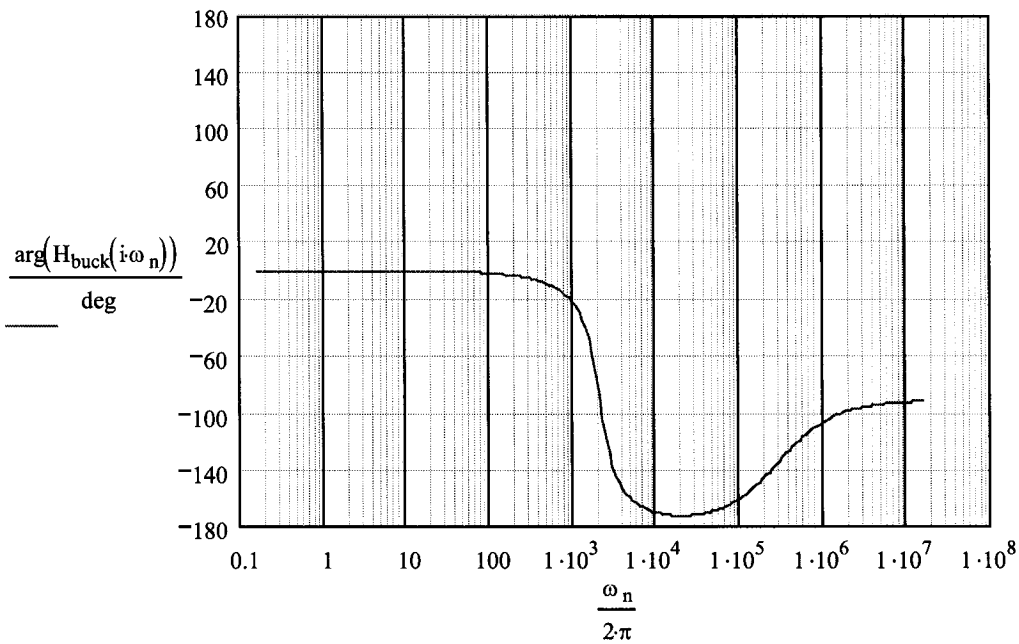
$$H_{buck}(s) := \frac{G_{buck0} \cdot \left(1 + \frac{s}{2 \cdot \pi \cdot f_{esr}}\right)}{1 + \frac{s}{(Q \cdot \omega_o)} + \left(\frac{s}{\omega_o}\right)^2}$$

Plot Open Loop Transfer Function

$n := 0..200$

$\omega_n := 10^{\frac{n}{25}}$





Crossover Frequency

$f_{xo} := 0.2 \cdot f_s \rightarrow 100000.0$

Current Gain at 0 dB

$H_0 := 20 \cdot \log(H_{buck}(0))\ \text{float},6 \rightarrow 21.5836$

Required Gain at Crossover Frequency

$h_{fxo} := 20 \cdot \log(|H_{buck}(i \cdot 2\pi \cdot f_{xo})|)\ \text{simplify} \rightarrow -44.797321175384197080$

Find 3dB Frequency

Initial Value $f_{fp} := 3050$

$H_0 - 20 \cdot \log(|H_{buck}(i \cdot 2\pi \cdot f_{fp})|)\ \text{float},6 \rightarrow 3.0840$

########(1)#########
Change the value of f_{fp} to achieve 3dB answer here with the help of the above curve tracing

2 Poles 2 Zeros Compensator Transfer Function

$$H_{comp}(s) = G_{comp0} \cdot \frac{\left(\frac{s}{\omega_{ez1}} + 1\right) \cdot \left(\frac{s}{\omega_{ez2}} + 1\right)}{s \cdot \left(\frac{s}{\omega_{ep1}} + 1\right) \cdot \left(\frac{s}{\omega_{ep2}} + 1\right)}$$

Poles and Zeros Locations

$f_{ez1} := \frac{f_{fp}}{5}\ \text{float},6 \rightarrow 610.$

$\omega_{ez1} := 2 \cdot \pi \cdot f_{ez1}\ \text{float},6 \rightarrow 3832.74$

$f_{ez2} := 1.1 \cdot f_{fp}\ \text{float},6 \rightarrow 3355.0$

$\omega_{ez2} := 2 \cdot \pi \cdot f_{ez2}\ \text{float},6 \rightarrow 21080.1$

$f_{ep1} := f_{esr}\ \text{float},6 \rightarrow 284205.$

$\omega_{ep1} := 2 \cdot \pi \cdot f_{ep1}\ \text{float},6 \rightarrow 1.78571 \cdot 10^6$

$f_{ep2} := 1.5 \cdot f_{xo}\ \text{float},6 \rightarrow 150000.$

$\omega_{ep2} := 2 \cdot \pi \cdot f_{ep2}\ \text{float},6 \rightarrow 942477.$

Initial Guess for Compensator Components Values

$C_1 := 2 \cdot 10^{-9}$ $C_2 := 1 \cdot 10^{-9}$ $C_3 := 5 \cdot 10^{-9}$ $R_1 := 1000$ $R_2 := 1000$ $R_3 := 1000$

Finding Compensator Components Values

Given

$R_1 = 75$ $C_1 = 1.0 \cdot 10^{-9}$

########(2)#########
Change the value of C1 and/or R1 to achieve the required h_{fxo}

$$\omega_{ep1} = \frac{1}{R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} \quad \omega_{ez1} = \frac{1}{R_2 \cdot C_2} \quad \omega_{ez2} = \frac{1}{(R_1 + R_3) \cdot C_3} \quad \omega_{ep2} = \frac{1}{R_3 \cdot C_3}$$

$$-20\log\left[\left|\frac{-1}{2} \cdot i \cdot \frac{(2 \cdot i \cdot R_2 \cdot \pi \cdot f_{xo} \cdot C_2 + 1)}{(\pi \cdot f_{xo})} \cdot \left[\frac{[2 \cdot i \cdot (R_3 \cdot C_3 + R_1 \cdot C_3) \cdot \pi \cdot f_{xo} + 1]}{[(2 \cdot i \cdot R_2 \cdot \pi \cdot f_{xo} \cdot C_2 \cdot C_1 + C_1 + C_2) \cdot (2 \cdot i \cdot R_3 \cdot \pi \cdot f_{xo} \cdot C_3 + 1) \cdot R_1]}\right]\right] = h_{fxo}$$

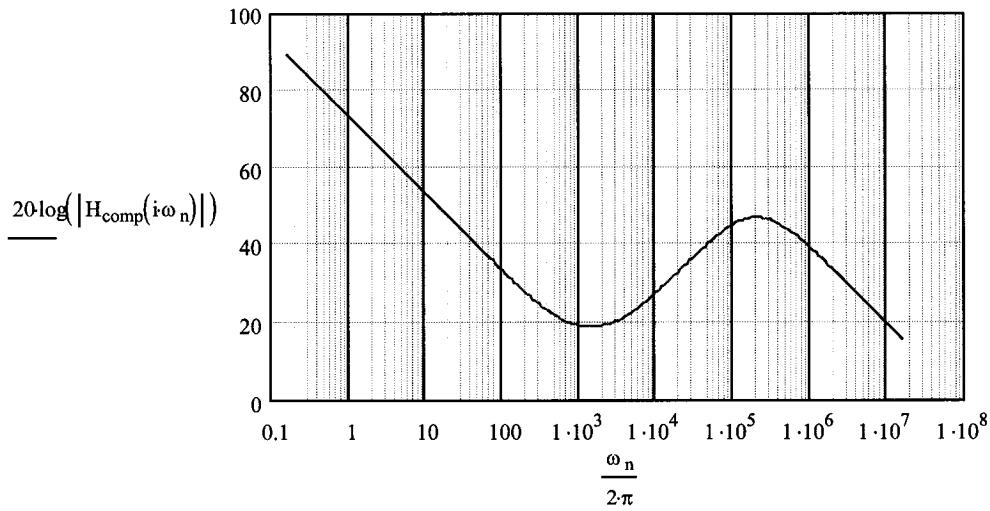
$$\begin{pmatrix} R_1 \\ R_2 \\ R_3 \\ C_1 \\ C_2 \\ C_3 \\ h_{fxo} \end{pmatrix} := \text{Find}(R_1, R_2, R_3, C_1, C_2, C_3, h_{fxo}) \text{ simplify} \rightarrow \begin{pmatrix} 75. \\ 561.20588238496292388 \\ 1.7158810714470604362 \\ 1.0000000000000000010 \cdot 10^{-9} \\ 4.649095059931015409310 \cdot 10^{-7} \\ 6.183609504288756335910 \cdot 10^{-7} \\ -44.849827489091210499 \end{pmatrix}$$

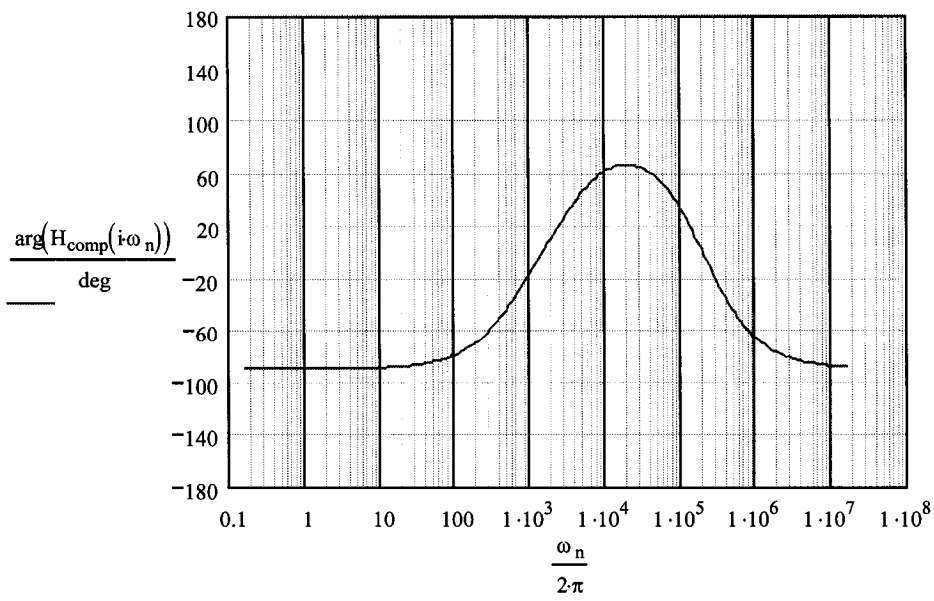
$$G_{comp0} := \frac{1}{R_1 \cdot (C_1 + C_2)} \text{ simplify } \rightarrow \frac{1}{[R_1 \cdot (C_1 + C_2)]}$$

$$G_{comp0} = 2.862 \times 10^4$$

$$H_{comp}(s) := G_{comp0} \cdot \frac{\left(\frac{s}{\omega_{ez1}} + 1\right) \cdot \left(\frac{s}{\omega_{ez2}} + 1\right)}{s \cdot \left(\frac{s}{\omega_{ep1}} + 1\right) \cdot \left(\frac{s}{\omega_{ep2}} + 1\right)}$$

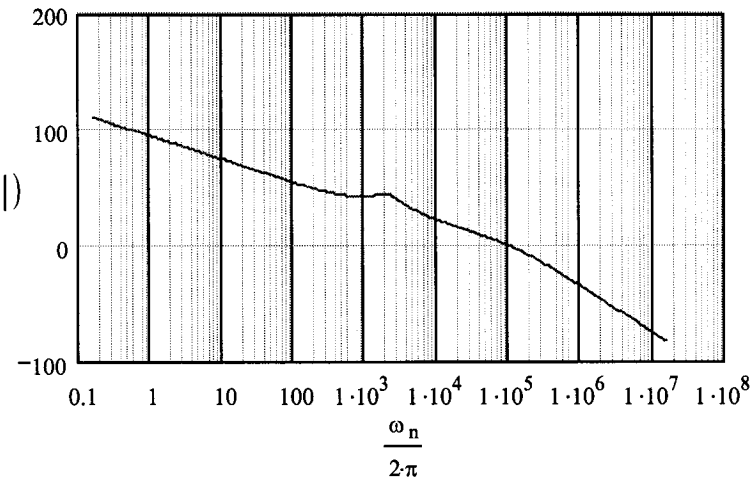
Plot Compensator Transfer Function



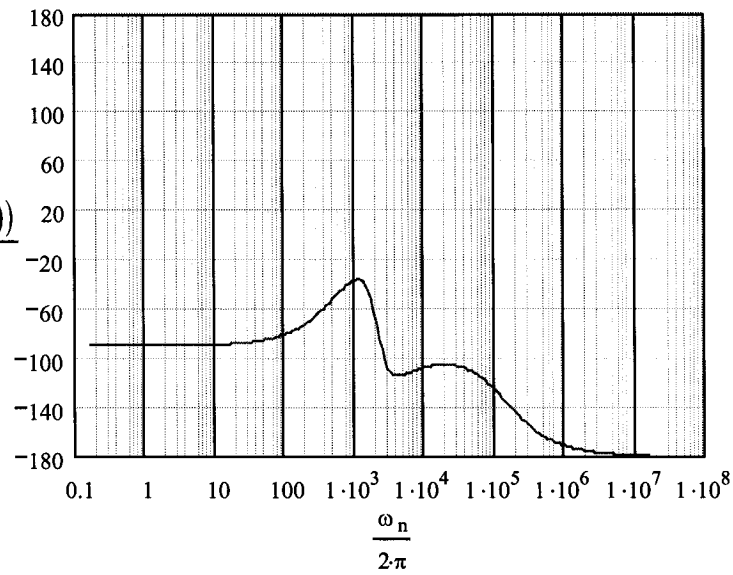


Plot Closed Loop Transfer Function

$20 \cdot \log\left(\left|H_{comp}(i \cdot \omega_n)\right| \cdot \left|H_{buck}(i \cdot \omega_n)\right|\right)$



$\frac{\arg\left(H_{comp}(i \cdot \omega_n) \cdot H_{buck}(i \cdot \omega_n)\right)}{deg}$

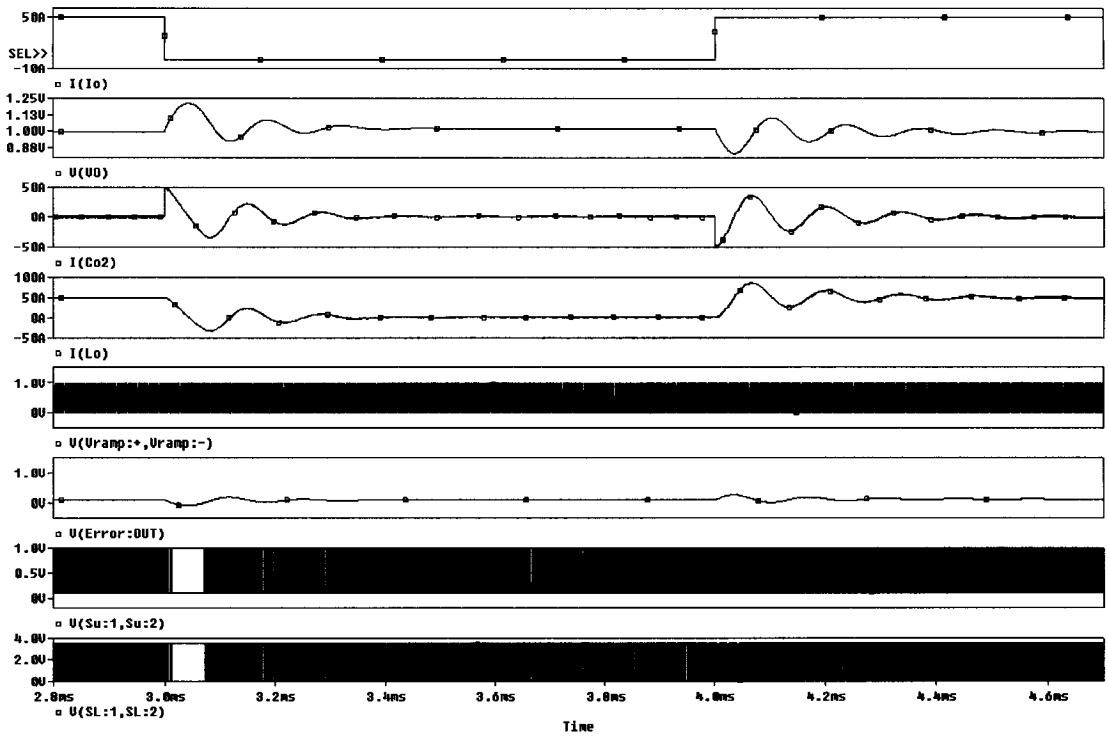


Check for Crossover frequency and Phase Margin

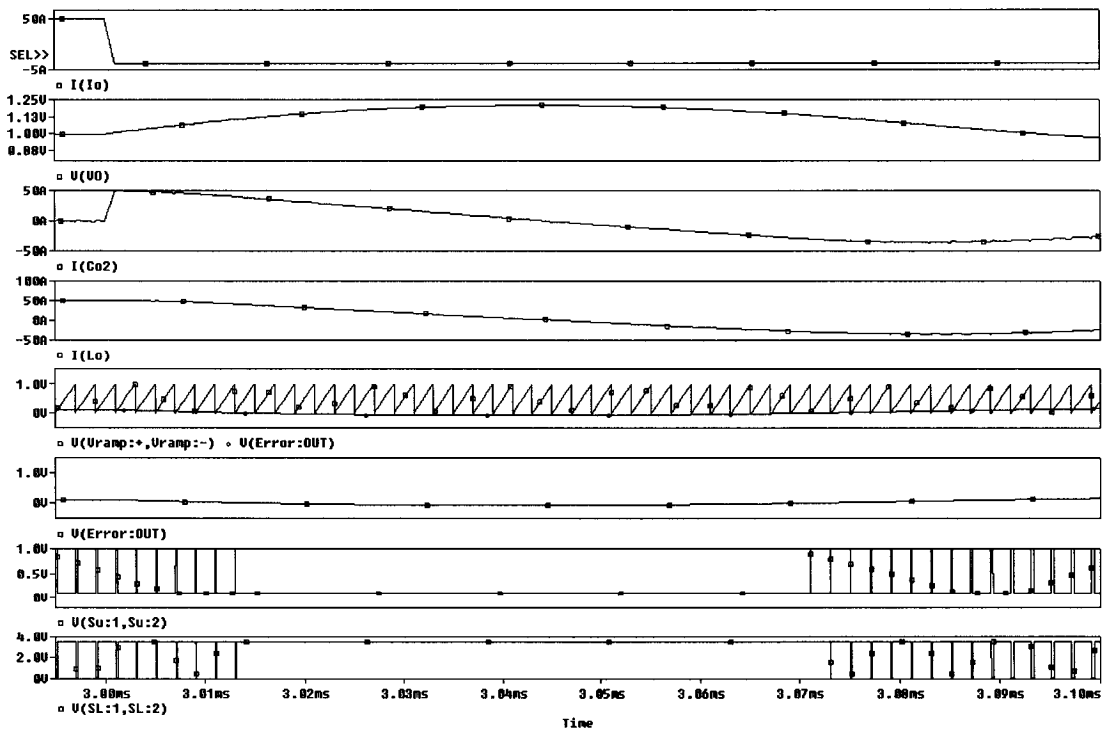
Design End

From the closed-loop transfer function bode plot, it can be noticed that the $100kHz$ crossover frequency was achieved at phase margin of about 55°, which completes the theoretical compensator components design.

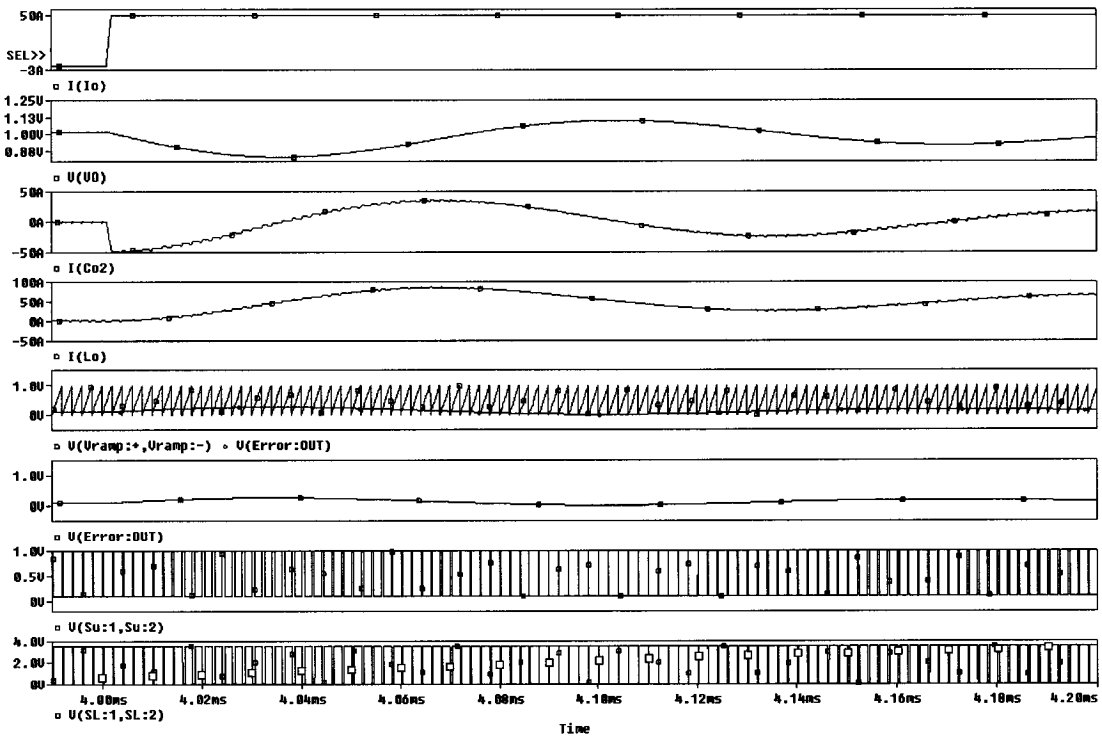
First, the schematics of Figure 9.8 with the designed compensator was simulated using Orcad/Pspice software. Then, after introducing the capacitor current signal as shown in Figure 9.7, the system was simulated again. Figures 9.9 and 9.10 show both cases simulation results respectively at $50A/\mu s$ current transient slew rate. In Figure 9.10 simulation, an extra 100ns delay time was added in the feedback loop to account for the extra delay that may be added by the extra summing amplifiers, which subtracts the capacitor current signal from the compensator error signal to generate the final error signal to be compared to the ramp signal. Comparing Figure 9.9 to Figure 9.10, measurements from simulations show that during load step-down transient, the output voltage deviation was reduced from 213mV to 170mV, while during load step-up transient, the output voltage deviation was reduced from 188mV to 40mV, which is considerable reduction in output voltage deviation.



(a)

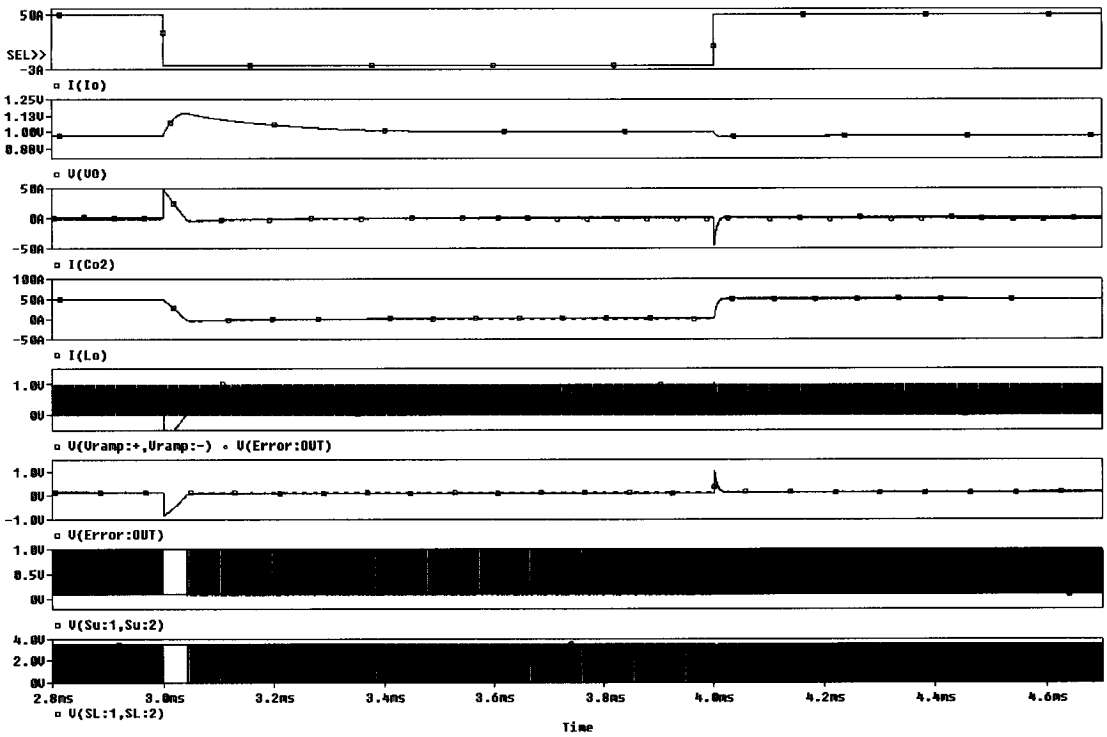


(b)

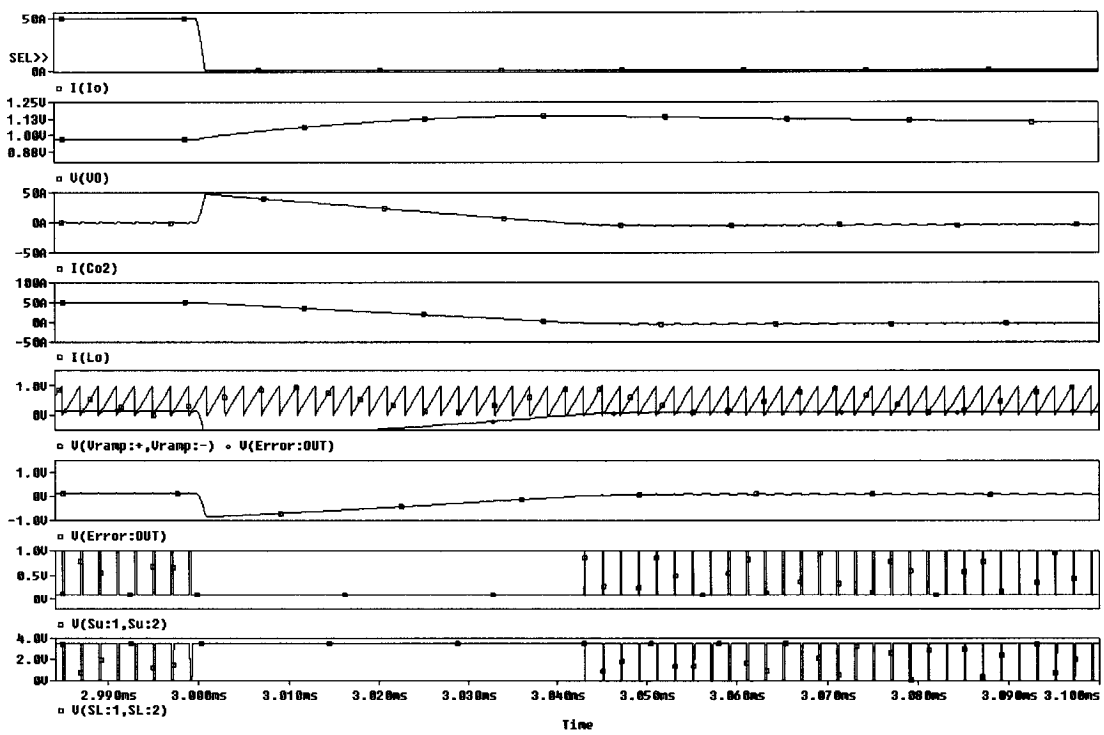


(c)

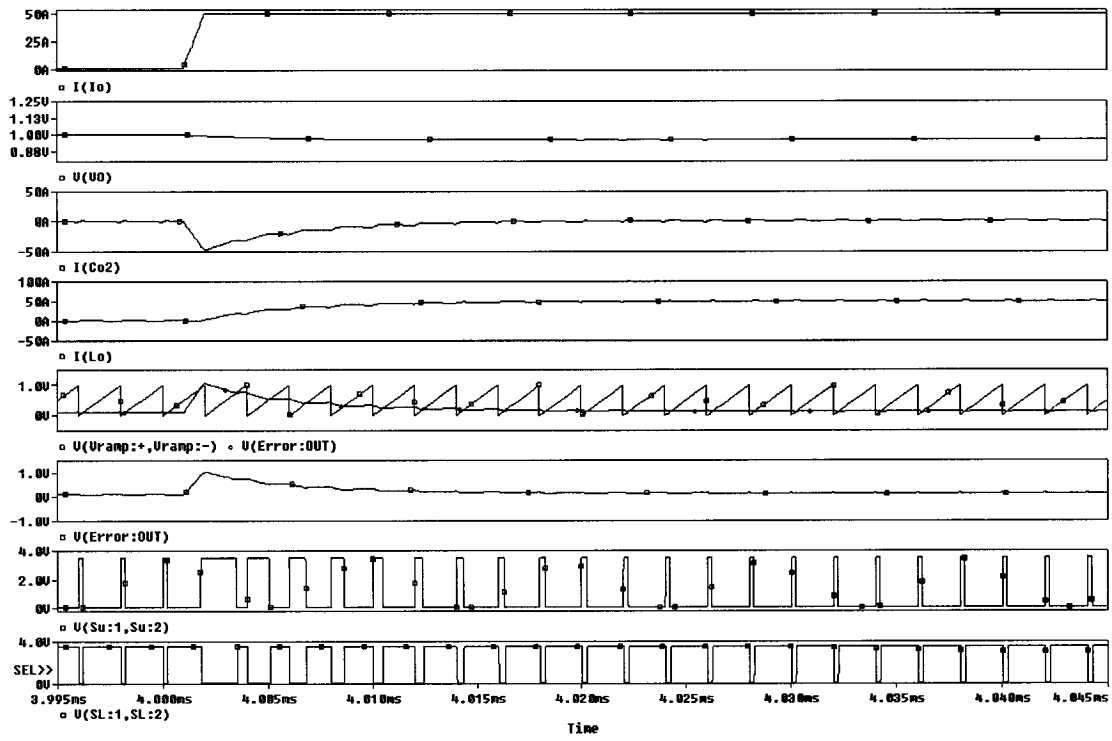
Figure 9.9: Simulation Results for Voltage-Mode Controlled Buck with the Designed 2-Poles 2-Zeros Compensator Without Introducing the Capacitor Current Signal: (a) Waveforms During Load Step-Down and Step-Up Transients ($50A/\mu s$), (b) Zoom on Waveforms During Load Step-Down (213mV Output Voltage Deviation) and (c) Zoom on Waveforms During Load Step-Up (188mV Output Voltage Deviation)



(a)



(b)



(c)

Figure 9.10: Simulation Results for Voltage-Mode Controlled Buck with the Designed 2-Poles 2-Zeros Compensator with Introducing the Capacitor Current Signal and Added Extra 100ns Delay Time to Account for the Extra Summing Amplifier Delay: (a) Waveforms During Load Step-Down and Step-Up Transients ($50A/\mu s$), (b) Zoom on Waveforms During Load Step-Down (170mV) Output Voltage Deviation) and (c) Zoom on Waveforms During Load Step-Up (40mV Output Voltage Deviation)

The gain of the additional summing amplifier can be selected depending on the sensed capacitor current signal level during full-load transients. The gain can be selected so that at full-load transients the sensed voltage magnitude, which is proportional to the capacitor current, is larger than the ramp signal amplitude. For the simulation example of

Figure 9.10, the capacitor sensed signal at full-load transients was 5mV, and the ramp signal amplitude was 1V. Therefore, the gain was selected to be 200 following the equation:

$$G_{Ic} \approx \frac{V_{ramp}}{V_{Ic-sensed}} \tag{9.6.1}$$

The presented method should sense the current in the closest capacitor to the load to avoid parasitic loop delays for faster response. This method also can be developed to be used in the new wave of transient current compensation circuitries/converters [81-83] that is used to absorb the transient current to reduce the voltage deviation as will be briefly introduced in the next section.

9.7 A New Wave of Transient Compensator Converters

Because of more stringent requirements expected in the future for POL and VRM converters, especially the tight, allowed voltage deviation at higher load current slew rate, a new wave of current/voltage compensator converters, or transient compensator converters [81-83], started to be considered as a candidate solution. Figure 9.11 shows an example of a general block diagram where a transient current compensator is used in parallel with the converter load.

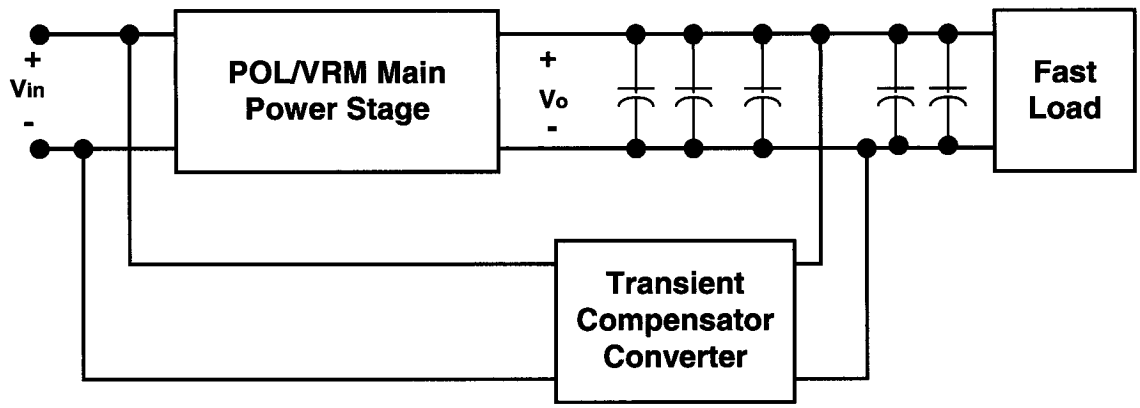


Figure 9.11: A General Block Diagram With a Transient Current Compensator Used in Parallel with the Converter's Load

The transient current/voltage compensator converter works only during severe load transients to either sink current during load step-down transients or supply current during load step-up transients as quickly as possible. In other words, the compensation converter takes part of the current (energy) that the output capacitance has to supply or sink until the converter with its output inductor is able to supply or sink that amount of transient current, thereby reducing the capacitor transient current magnitude that reduces the output voltage deviation. Such transient compensator converter should work faster than the main power stage, and it should have early transient detection, for example through the capacitor current close to the load or by sensing the current internally from the load if possible. Moreover, the transient current compensator converter should be designed with very low inductance path to achieve better transient performance.

Several challenges and disadvantages that should be reduced arise in designing this kind of transient compensator converter including additional power losses, including losses from switching and conduction, since it is designed to sink high current and work at higher frequency to be able to reduce output voltage deviation.

Basically, this solution is considered in order to change the topology characteristics in addition to the controller characteristics. The main reason for this, as discussed earlier, is that the transient response speed and deviation is not only a function of the controller speed, but also a function of the topology and its output filter. Actually, topology limitations are becoming a large limitation factor in the system response speed and deviation magnitude.

9.8 Digital Control System

Digital Control or Digital Signal Processing (DSP) control is a strong candidate for future on-board DC-DC converters, and in the field of power conversion in general, because of its many advantages [29,87,88]. These advantages include the ability to perform sophisticated and enhanced control schemes in a single programmable chip, control algorithm(s) can be easily modified or changed via software revisions, immunity to analog component variations, low power consumption, ease of integration and interfacing with digital systems and ability to provide good duty cycles matching for different phases.

A general block diagram for such digital controller system is shown in Figure 9.12. An Analog-to-Digital Converter (ADC) converts the sensed analog signals from the converter, including the output voltages, into digital format before they are read by the digital controller DSP chip. The DSP chip core and other peripherals process the digital information through a programmed algorithm and generate a control decision that is then converted to its final Digital Pulse Width Modulation (DPWM) format and is then outputted to the converter switches drivers and protection circuitries.

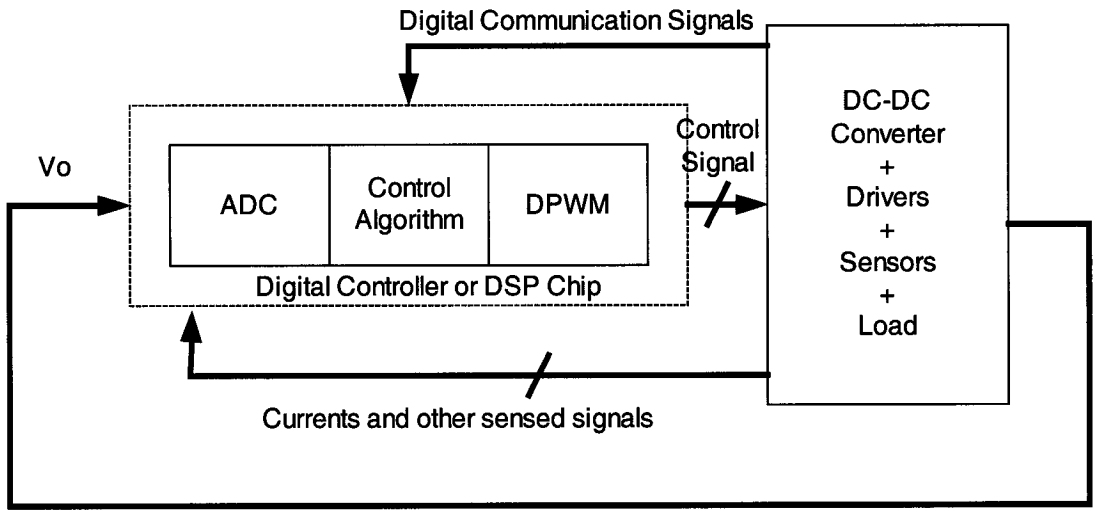


Figure 9.12: A General Block Diagram Digital Controller System

There are additional feedback control delays introduced in the digitally controlled system by the digital processing of mainly the ADC and the processor processing time in addition to the compensation, sensing and switches drivers delays. Therefore, the main expected drawback of DSP control is the additional delays, which can be minimized by using faster ADC and higher chip speed, and the cost of the digital system. However, in the recent years, faster DSPs at lower cost started to appear in the market [89,90], and it is expected that the speeds and the cost of DSPs will continue to improve dramatically in the future [89,90].

9.9 Digital Control System Delays and Design

The additional digital delay caused by the digital system can be approximated by:

$$t_{Digital} \approx t_{ADC}(f_{ADC}, n_{ADC}) + t_{Process}(f_{CLK}, I_n, n_{CLK}) + t_{other} \qquad (9.9.1)$$

where:

t_{ADC} is the delay time resulted from the ADC sample and hold, and it is a function of the ADC clock speed (f_{ADC}) and the number of clock cycles the ADC needs to convert (n_{ADC}).

$t_{Process}$ is the delay time caused by the DSP processing time that is mainly a function of the core clock frequency (f_{CLK}), the number of instructions used in the program (I_n), and the number of clock cycles needed to execute an instruction (n_{CLK}).

t_{othor} is other miscellaneous delay times that may include the time between when the control decision is ready and when the actual switch turns ON or OFF. This can also include safety margin delays.

The above yields to the following equations:

$$t_{ADC} = \frac{n_{ADC}}{f_{ADC}} \tag{9.9.2}$$

$$t_{Process} = \frac{I_n \cdot n_{CLK}}{f_{CLK}} \tag{9.9.3}$$

Therefore, for a converter system with a specific maximum allowed control loop delay, the delay budget allowed by the digital part should be determined, and upon this determination, the appropriate ADC and chip speed should be selected.

For example, assuming that the digital system delay should be limited to one switch switching cycle, then the digital delay budget is given by:

$$t_{budget} = t_s = \frac{1}{f_s} > t_{Digital} \tag{9.9.4}$$

Figure 9.13 shows possible design and digital system delays breakdown where it is assumed that the ADC is trigged to sample at the rising edge of each switching cycle. The additional digital system delays can be limited to less or more than switching cycle if desired. Another design parameter is to select the appropriate resolution or number of bits of the ADC, which depends on the sensing resolution required for a specific design.

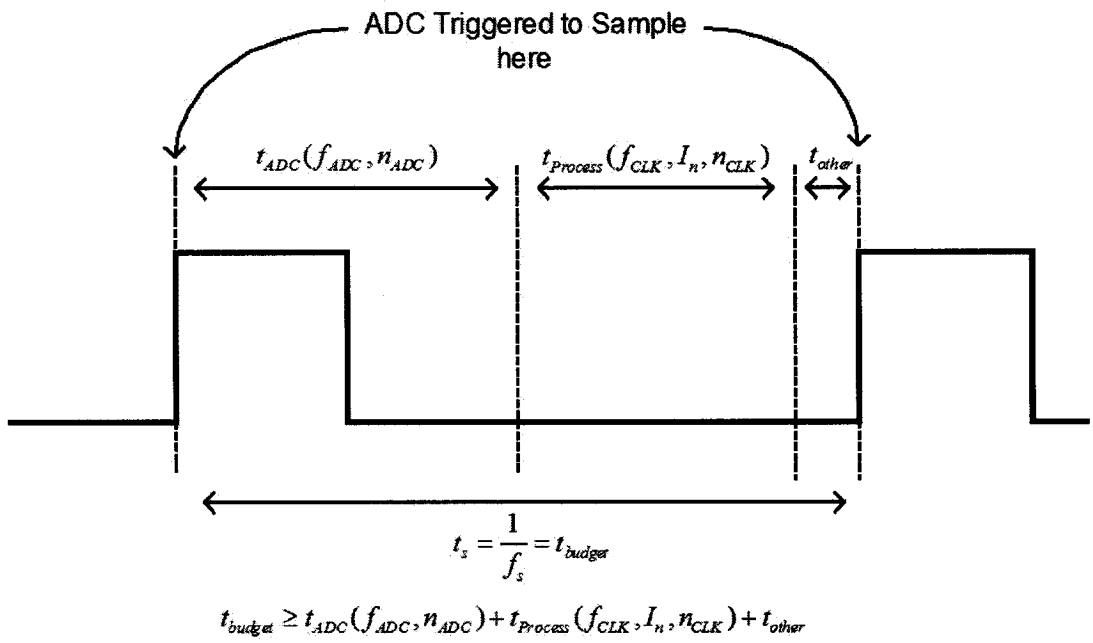


Figure 9.13: Time Delay Budget Calculations as a Function of the DSP System Delay Parameters

9.10 Initial Digital System Setup and DSP Controlled Multiphase Voltage-Mode Hysteretic Converter

This section will present an initial work completed for DSP closed loop system setup and experimentation. The experimental setup was for the Multiphase Voltage-Mode Hysteretic Converter [29] presented in Chapter 3.

Figure 9.14 shows the experimental setup block diagram, while Figure 9.15 shows the control algorithm flowchart.

The laboratory availability was for the TI DSP Chip and Evaluation Module of TMS320LF2407 [91], which has 33ns Instruction Cycle Time (30 MHz), which is relatively slow for this application (refer to [91] for more information on TMS320LF2407). This chip is geared toward control applications. However, it lacks the processing speed (30MHz). In addition, increase in processing power is necessary for advance control methods in the future.

The ADC used here is the TI 12-bit 53MHz ADS807 [92] with OPA642 [93] Op-Amp in its signal conditioning circuitry.

The power stage includes paralleled buck converters with the following main components:

- MOSFETs: SI4410DY.
- Output Capacitors: 3 SANYO OSCON of 820uF, 4V.
- Output Inductors: 28 A, $1\mu H$, T68-8/90 Core, 7-turns, 16AWG Wire.
- MOSFET Drivers: TPS2836.
- OP-AMP for current sense signal of the MOSFETs junctions amplification: OPA642.
- Vin = 5-12V input voltage source.

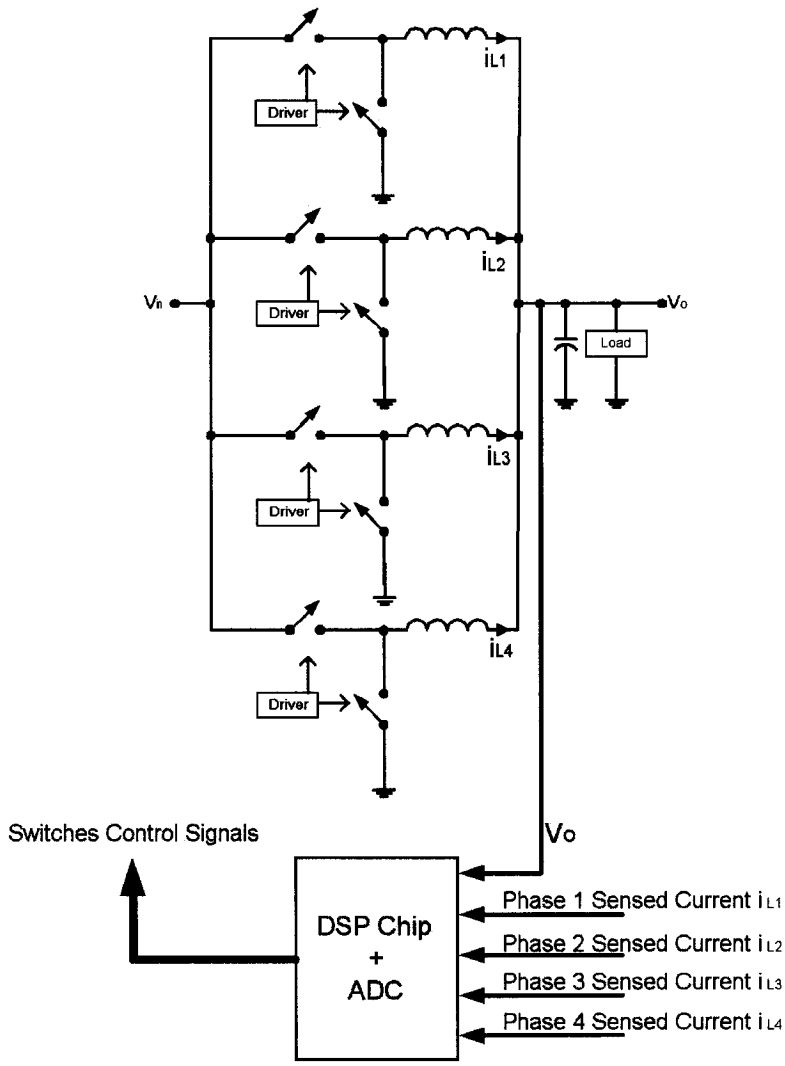


Figure 9.14: Block Diagram of Four-Phase Voltage-Mode Hysteretic-Controlled Interleaved Converters with DSP Control

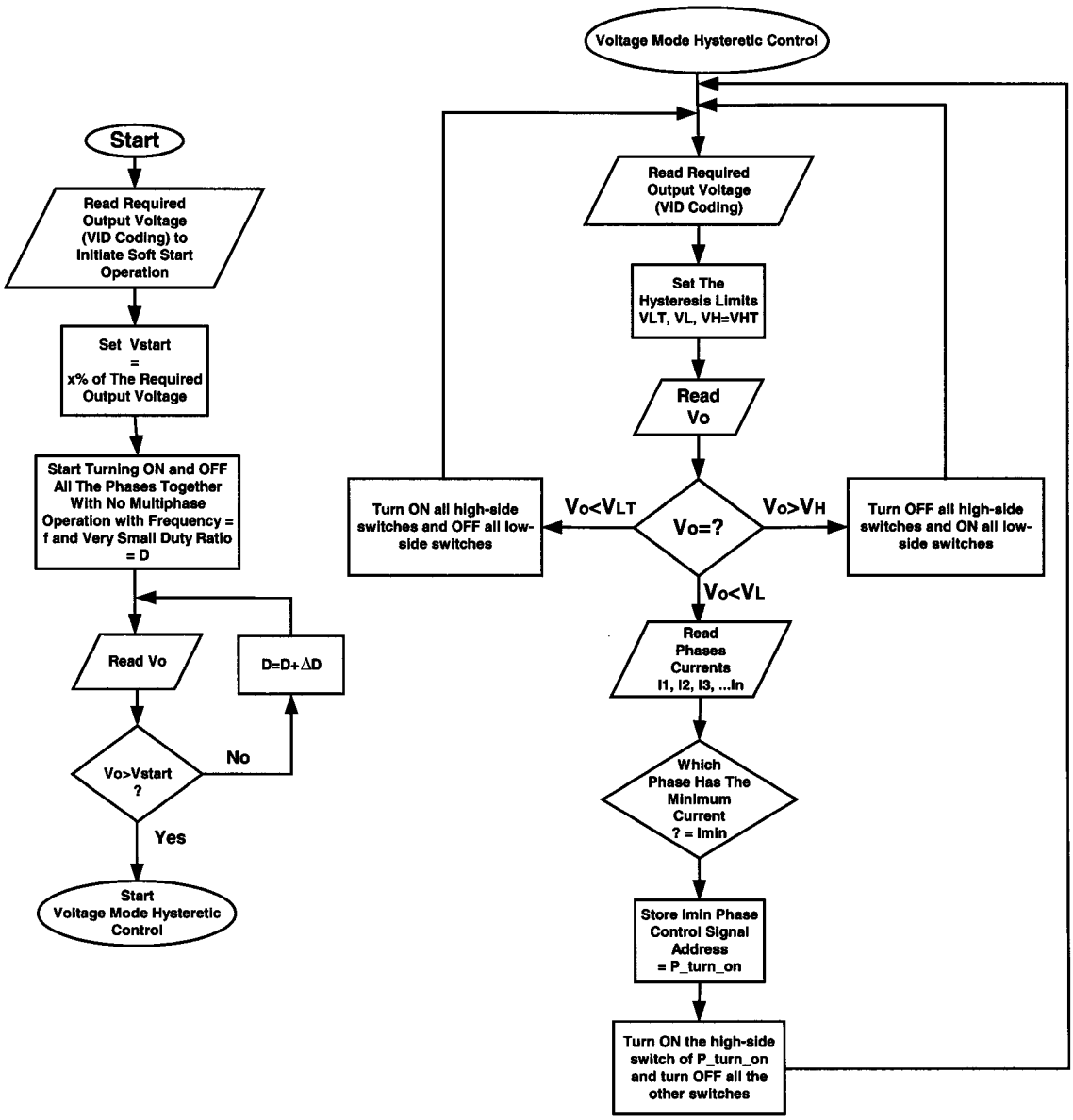


Figure 9.15: DSP Chip Program Flowchart

Figures 9.16, 9.17 and 9.18 show some initial experimental results for two-phase, three-phase and four-phase power stage, respectively. All are shown with the slow 30MHz TMS320F2407 DSP board, which limits the switching frequency and the minimum output voltage ripple.

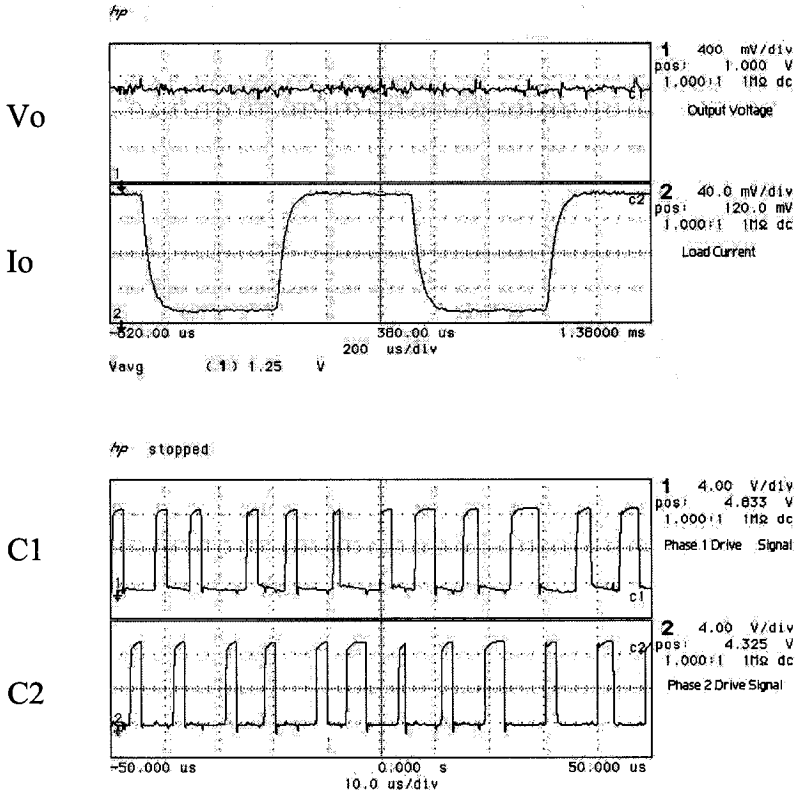


Figure 9.16: Experimental Results for Two-Phase Power Stage

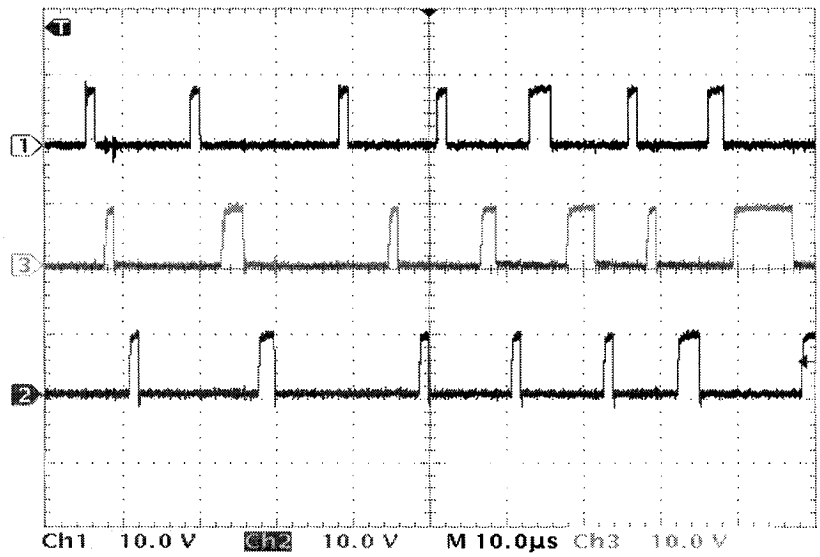


Figure 9.17: Experimental Results for Three-Phase Power Stage

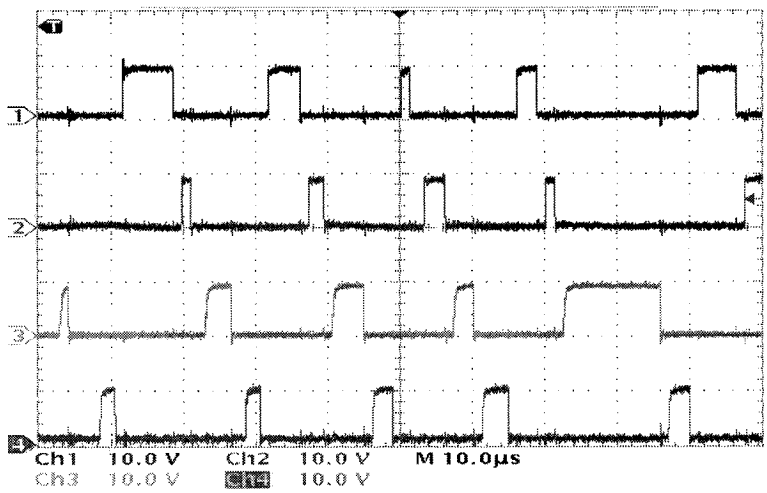


Figure 9.18: Experimental Results for Four-Phase Power Stage

9.11 Future Work to Be Continued on Digital Control

Faster programmable chips should be used in the future for better results and to achieve faster response, lower output voltage ripple, better current-sharing accuracy, higher switching frequency, better stability and to be able to integrate more functions and more complicated algorithms.

There are already high-speed programmable DSP chips available [89]. Some of them of several hundreds of Megahertz and are gearing towered Gigahertz speed range [90]. Moreover, some manufacturers have special programmable chips with their own structures that are geared and optimized for control applications.

Also, digital control system can be applied to isolated topologies such those discussed in earlier chapters. For example, Figure 9.19 shows an isolated half-bridge converter with secondary-side digital control scheme. Future algorithm work for Figure 9.19 should include output voltage control and compensation, protection, deadtime

optimization control or adaptive deadtime control [94-96], Active-Voltage Positioning (AVP) [84-86] and possibly other adaptive and/or predictive functions.

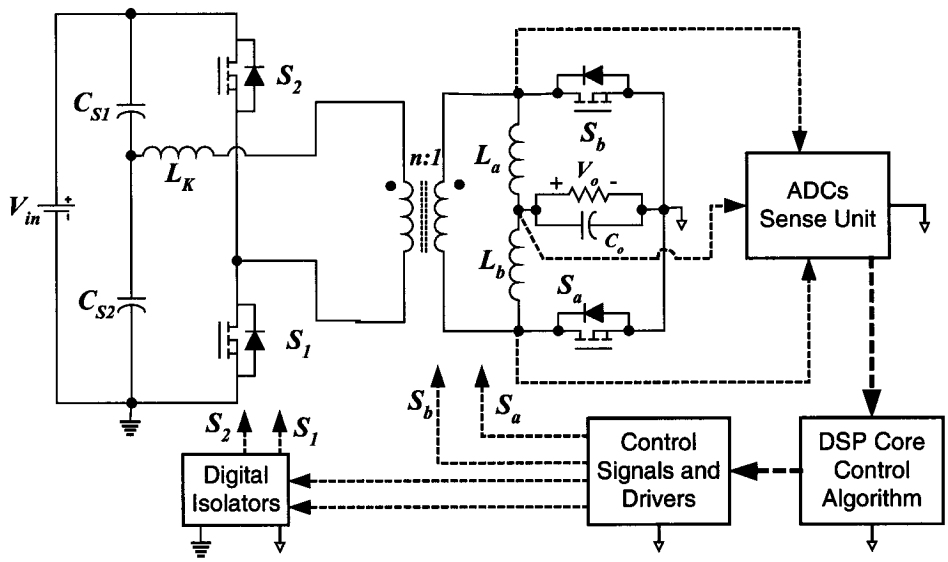


Figure 9.19: Isolated Half-Bridge Converter with Secondary-Side Digital Control Scheme

9.12 Maximum Efficiency Point Tracking (MEPT) and Dead Time Control

MOSFET's body-diodes conduction of the secondary side topology, such as current doubler, should be avoided for better efficiency, especially for low-output voltage, high-output current applications where the body-diodes conduction loss becomes more severe [94-96], which requires to design for the smallest possible dead time (delay time) between turning ON and OFF the primary-side switches and turning OFF and ON the corresponding secondary-side switches. At the same time, this dead time should be long enough to avoid the two secondary switches short circuit when the two of them are ON at the same instant and the voltage is applied from the primary side.

The selection and optimization of this dead time is not an easy task and is difficult to achieve at all load/input conditions. One way to accomplish it is to fix the dead time to

a constant value that satisfies the worst load/input condition. This can be achieved by a simple RC delay circuitry to set the dead time between turning ON and OFF the corresponding switches. This method is simple but unfortunately results in lower efficiency since the dead time has to be set long enough to cover the whole load/input range and to cover other variations such as temperature variations. Another way is to set the dead time by detecting the switch-body diode conduction [94] and modifying the dead time accordingly. This method reduces body diode losses and therefore improves efficiency. However, the body diodes still conduct and considerable losses still considerable especially at higher switching frequencies. This method is sometimes considered as an adaptive [94,96] method but in fact it is semi adaptive since it does not use the efficiency, which is the targeted parameter here, as the reference parameter that the dead time should adaptively change to optimize.

Efficiency is one of the most important parameters being targeted for optimization and maximization and effectively controlling converter parameters, such as dead time to greatly contribute to efficiency.

A method to be called Maximum Efficiency Point Tracking (MEPT) is presented here. This method is derived from the Maximum Power Point Tracking (MPPT) [97,98] used in Solar Array Systems. The MEPT method adaptively changes the parameter of interest, which is the dead time as an example here, while tracking the efficiency for maximum efficiency point detection that exists for certain optimized dead-time value. Figure 9.20 shows efficiency versus dead time curve that presents how MEPT can be used to optimize dead time control, while Figure 9.21 shows one possible MEPT DSP program algorithm for dead time optimization.

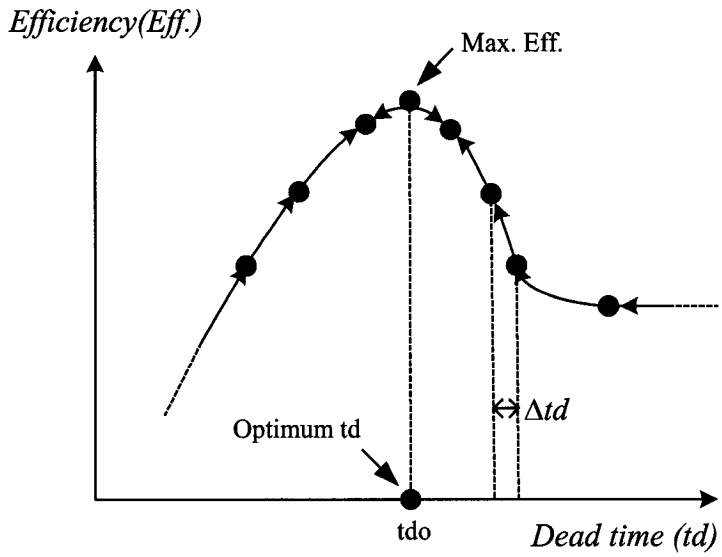


Figure 9.20: Efficiency Versus Dead Time Curve that Presents How MEPT Can Be Used to Optimize Dead Time Control

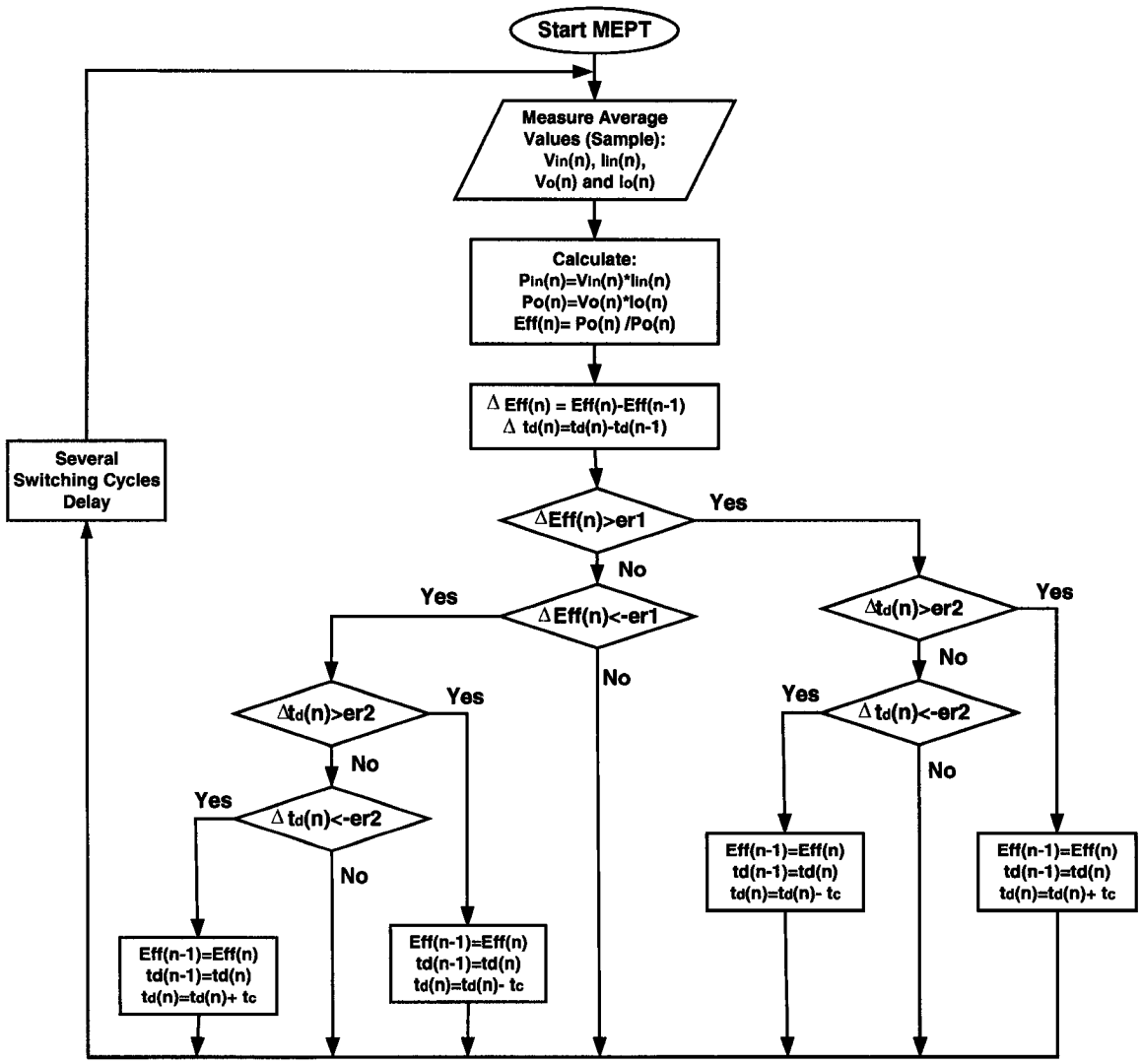


Figure 9.21: One Possible MEPT DSP Program Algorithm for Dead Time Optimization

As shown in the flowchart of Figure 9.21 together with Figure 9.20, the average values of the input voltage V_{in}, input current I_{in}, output voltage V_o and output current I_o are sampled each several switching cycles to calculate the current efficiency $Eff(n)$ from both input power and output power values at the current dead time set value $t_d(n)$. The difference between the current values $Eff(n)$ and $t_d(n)$ and the previously sampled

and stored values $Eff(n-1)$ and $t_d(n-1)$ is calculated as $\Delta Eff(n) = Eff(n) - Eff(n-1)$ and $\Delta t_d(n) = t_d(n) - t_d(n-1)$. $\Delta Eff(n)$ and $\Delta t_d(n)$ are respectively compared to set values er_1 and er_2 (er_1 and er_2 are usually small and larger than zero to avoid oscillation and instability around the MEPT point) to detect if the increment or decrement value t_c to the dead time value t_d caused efficiency increase or decrease. Then, the dead time t_d is incremented or decremented accordingly to detect the optimum dead time value t_{do} for the MEPT point.

Further detailed analysis, simulation and experimental verification are future work that may be found in literature in the future.

Finally, MEPT method can be used to optimize other parameters in the DC-DC converter and its distributed power system. This includes optimization of duty cycles and intermediate bus voltage in two-stage DC-DC converter topology.

9.13 Other Digital Control Algorithms

Digital control allows flexibility in solving several control issues. For example, the voltage balance of the two half-bridge topology input capacitors, where unbalance may occur between the two capacitors voltages because of channels asymmetry or because of control techniques such as current mode control. This unbalance can be easily compensated for using digital control, for example, by simply monitoring the capacitors mid point voltage and slowly changing the duty cycle of the appropriate switches until balance is achieved. Assume S_1 and S_2 are a symmetrically driven two half-bridge topology switches with t_{ON1} and t_{ON2} ON-time duration, respectively. If the two capacitor

voltages are equal, $V_{C1} = V_{C2}$, or in other words, the mid point voltage is equal to half of the input voltage, then $t_{ON1}(n) = t_{ON2}(n) = t_{ON}(n)$. When $V_{C1} > V_{C2}$ or $V_{C1} < V_{C2}$, one switch ON-time is incremented and the other is decremented several times by small step time Δt_c until balance is achieved. When $V_{C1} > V_{C2}$, $t_{ON1}(n) = t_{ON1}(n-1) - \Delta t_c$ and $t_{ON2}(n) = t_{ON2}(n-1) + \Delta t_c$ and when $V_{C1} < V_{C2}$, $t_{ON1}(n) = t_{ON1}(n-1) + \Delta t_c$ and $t_{ON2}(n) = t_{ON2}(n-1) - \Delta t_c$, while maintaining always $2t_{ON}(n) = t_{ON1}(n) + t_{ON2}(n)$.

Moreover, by digital algorithms, control schemes can be changed for same converter depending on certain parameters such as input voltage and/or load current. For example, for a half-bridge converter with an input voltage range of 36V~75V, asymmetric control can be used while the input voltage is 36V~50V to achieve soft-switching for both switches and then softly switch to symmetric control or DCS control, which can achieve soft-switching for one switch, when the input voltage is 51V~75V, so that symmetric components stresses can be achieved at high input voltage range and there is no need to design for high components ratings and the large voltage and currents asymmetry can be avoided. This control scheme may be called "Piecewise Control".

The detailed investigation and implementation of such methods is a future work.

9.14 Summary

In this chapter, some control techniques were briefly reviewed and compared. Then, a modified control technique was recommended and simulated for further investigation and experimental verification in the future. Moreover, a general block converter with transient compensation was introduced, which will be one of the subjects focused on in the future to satisfy lower voltage deviation requirements.

Moreover, programmable digital control is discussed as a candidate for DC-DC converters. Some system structures, design issues and initial experimental setup and results were also presented. Moreover, candidate method with its DSP algorithm was introduced, namely the Maximum Efficiency Point Tracking (MEPT) method and algorithm. Other possible algorithm schemes were also introduced for future detailed investigation and implementation. Future work includes digital system and algorithms developing for DC-DC converters control.

CHAPTER 10

SUMMARY AND FUTURE RESEACH

The speed and integration density of POL and VRM DC-DC converter's loads of DSPs, including microprocessors, are continuing to increase resulting in higher currents being drawn from these converters by such loads that may be in a magnitude of several hundreds of Amperes in the future, because of their more integrated functions, lower operating voltages of small fractions of one Volt for higher integration density, higher load transient current slew rates of several thousands of Amperes per micro second because of operating speed frequencies of tens of Giga Hertz that will impose a challenge in satisfying the output voltage deviation limits that are getting tighter as operating voltages decreases and more severe as current magnitude and slew rate increase.

Moreover, higher current and lower voltages required to be supplied by the converter are resulting in larger conduction and switching losses of components including switches causing lower converter efficiency, which also decreases as the switching frequency increases to satisfy transient requirements. Lower efficiency results in thermal issues and block the ability of achieving higher converter power/current density, i.e. smaller size, while the converter load integration density increases.

Chapters 1 and 2 summarized the expected semiconductor's road map and POL and VRM converters design issues and challenges. There is a difficult tradeoff between increasing the converter switching frequency while decreasing its output inductance to achieve faster transient response at lower output capacitance and maintaining acceptable converter efficiency at this high current and low voltage. As a result, it is apparent that the transient response speed is a function of the power stage design and topology as it is a function of the control loop design. In fact, power stage design has effects on many aspects including transient response, efficiency and thermal management and power/current density. Also, components and distribution parasitics play an important role in the design, not to mention the switches conduction and switching losses caused mainly by the ON-state resistance, gate capacitance and switch body diode conduction. Technology advancement in semiconductor switches is vital for such application in the future.

Chapters 3 and 9 presented control schemes toward achieving faster transient response. In Chapter 3, a multiphase voltage-mode hysteretic control with current sharing method applied to a non-isolated converter was presented. This control method combines the advantages of fast feedback control with no feedback compensation, phase interleaving for output current ripple cancellation and lower effective output inductance, lower switching frequency per phase and better thermal management. Moreover, analysis was presented including output voltage ripple and frequency equations and a stability condition equation for N interleaved phases considering converter components parasitics. In Chapter 9, major control schemes were reviewed, and it was shown that the controller must sense and utilize a fast slew rate signal that has a faster change during transient than

the output voltage and the inductor current. This variable was the capacitor current that can be introduced with any control scheme.

Chapters 4 and 5 reviewed candidate isolated topologies for future POL and VRM converters and presented two control schemes that achieve soft-switching operation for half-bridge topology switches that result in higher efficiency improvement at higher switching frequency and reduce isolation transformer leakage inductance ringing-related losses. It was shown in Chapter 4 that by simply shifting one switch driving signal rising edge closer towards the other half-bridge switch driving signal falling edge while keeping both signals symmetric, soft-switching can be achieved through DCS control while maintaining symmetric components stresses and no transformer DC bias. In Chapter 5, it was illustrated that by alternating switching signals between the two half-bridge switches using ADC control, soft-switching can be alternatively achieved for the two switches while also maintaining symmetric components stresses and no transformer DC bias even if the there was asymmetry in the control signals. Current-doubler secondary-side topology with synchronous rectifiers was used, along with the DCS and ADC controlled half-bridge primary side, as a strong candidate topology.

In Chapter 6, interleaved current doublers topology with parallel connected transformers at both primary and secondary sides was presented. This scheme realizes interleaving for isolated converters at primary side as is the case at the secondary side. This topology is a candidate topology for high-current applications. A generalization of this method was presented to result in a family of interleaved isolated DC-DC converters. Moreover, soft-switching methods presented in Chapters 4 and 5 can be combined with Chapter 6's method to achieve combined advantages.

Chapter 7 presented a coupled-inductors current-doubler DC-DC converter topology that utilizes coupled magnetics for further output voltage step-down in low-voltage applications and can be designed for low output ripple. Moreover, the current of the isolation transformer secondary side, which is large in high-current applications, is reduced.

In Chapter 8, it was shown how the half-bridge configuration could be used as non-isolated topology that can be a second stage candidate in a two-stage topology. This non-isolated half-bridge topology has the advantage of self-maintaining equal current sharing between its channels without the need for a current sharing loop. Compared to two-phase buck topology, the duty cycle is extended in the case of the non-isolated half-bridge topology because of the two-capacitor, two-switches configuration that steps down the voltage by two. Moreover, half-bridge soft-switching control methods can be utilized for this scheme to achieve soft switching.

Chapter 9 discussed digital control as a future candidate for POL and VRM converters due to its advantages, including the ability to perform sophisticated and enhanced control schemes in a single programmable chip, control algorithms can be easily modified or changed via software revisions, immunity to analog component variations, low power consumption, ease of integration and interfacing with digital systems and ability to provide good duty-cycles matching for different phases. Digital control system and its additional delays were discussed and initial experimental work on a DSP controller setup was presented. The Maximum Efficiency Point Tracking (MEPT) method was also presented as a future work that also can be used to optimize switches

dead-time control issue by using adaptive control to achieve better efficiency and converter performance. There is more to be done about digital control in the future.

In addition, other techniques were discussed in several chapters through this work. For example, the new wave of transient compensator converters that is used during transient periods to improve the main converter power stage transient response by supplying or sinking part of the transient current to minimize voltage deviations. Unfortunately, such converters are forced to take a large amount of current and exhibit large conduction and switching losses. Future challenges in designing such converter topologies include minimizing their losses and increasing their response speed.

Therefore, future research directions should include not only improvements in control schemes to achieve faster control loops, which is very important, but also improvement in power stage topologies and design, since the dynamic performance is a function of both. Moreover, power stage topology is not only important for dynamic characteristics, but also important for efficiency, thermal management and power/current density. Higher efficiency may allow higher switching frequency, which will improve the dynamic characteristics. Of course, technology improvements in components characteristics are also vital toward improving the converter efficiency and dynamics. Accurate variables (currents and voltages), sensing techniques and components, which are not discussed in this work, are also important to achieve accurate control at voltages that have very small allowed deviation windows.

Moreover, the design of the entire distributed power system is also important, i.e. not only the POL and VRM DC-DC stage, starting from front-end converter that may

have PFC (Power Factor Correction), to the intermediate bus converter, up to the POL and VRM DC-DC converters.

In the future, direct communication between the fast load and its converter may be necessary. This is essential, for example, to make the converter proactive instead of reactive, i.e., to respond to its load transient before they occur instead of after.

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